

Verilog Lab 1

Prof. Shih-Chieh Chang



Outline

- Workstation setting: MobaXterm
- Project



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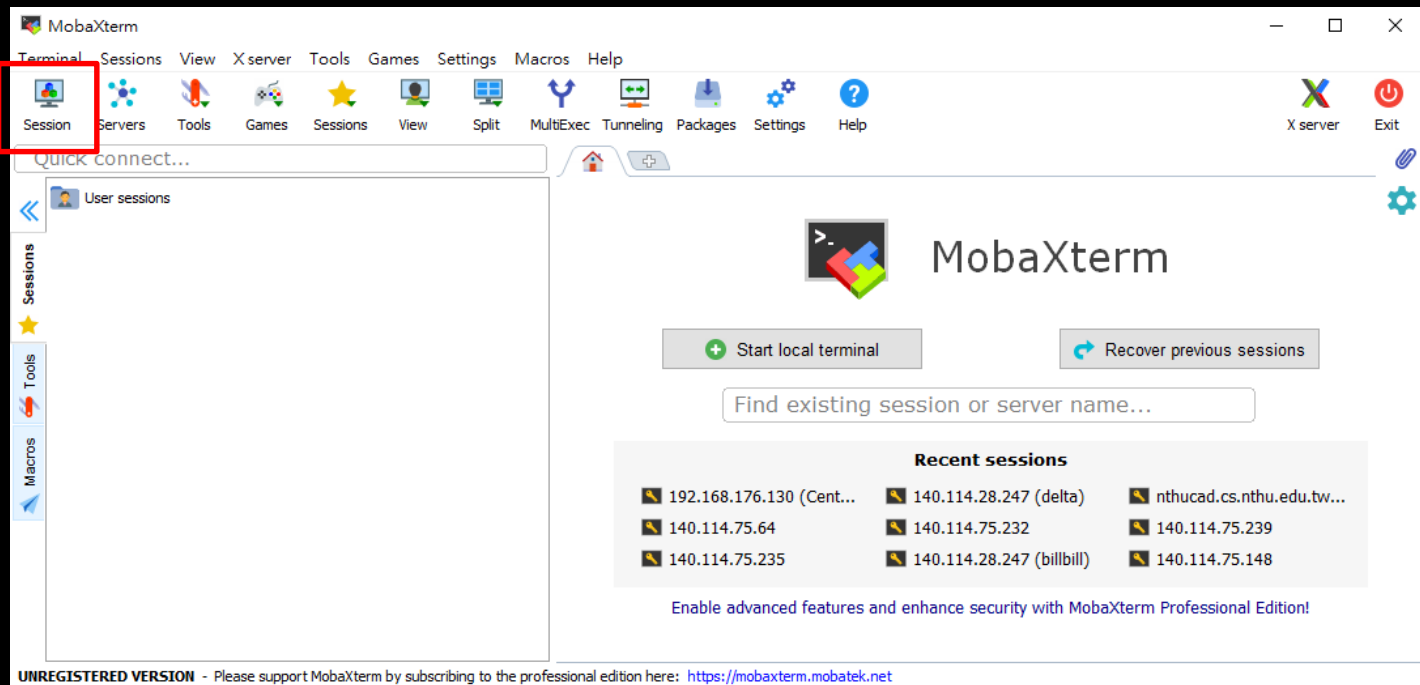


MobaXterm Download

- ▣ Download the free version of MobaXterm
 - https://www.azofreeware.com/2014/11/mobaxterm_portable.html



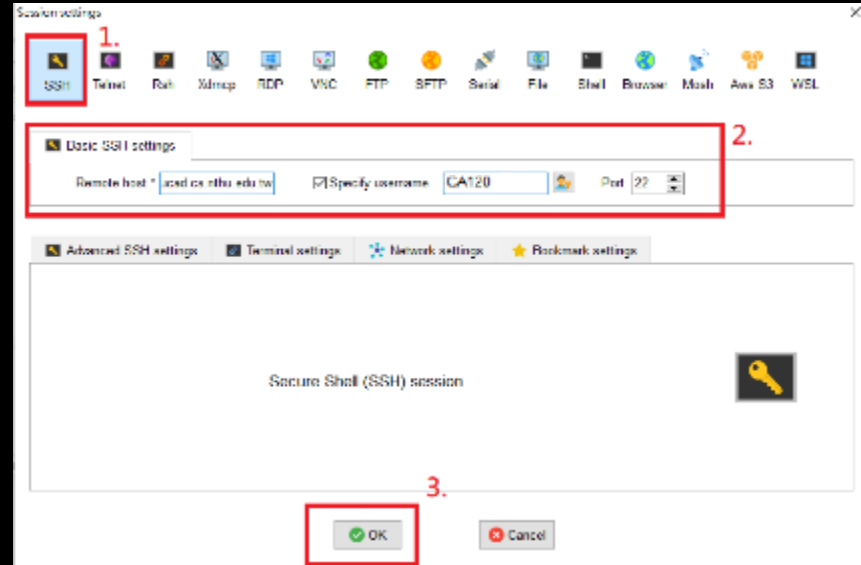
Workstation Setup



Workstation Setup (Cont.)

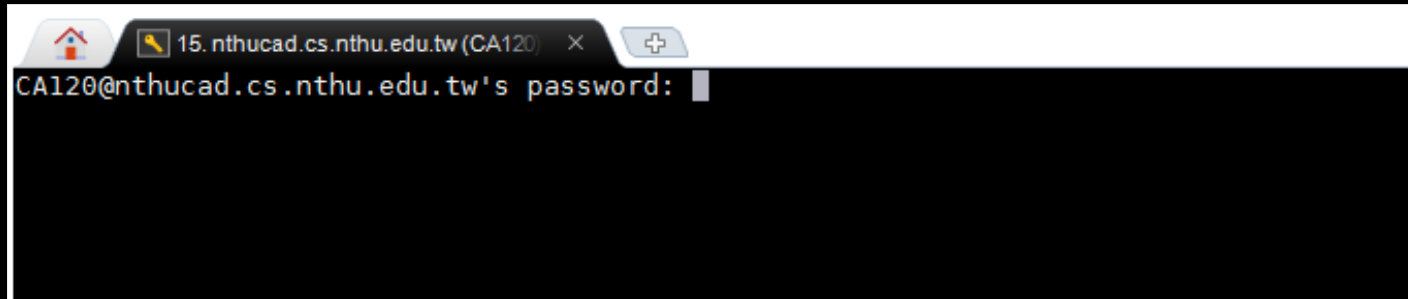
- Enter the following blank
 - Remote host: nthucad.cs.nthu.edu.tw
 - Specify username: (your account)
 - Port: 22

- Click “OK”



Login at the First Time

- Key in your initial password from e mail



Change your Password

- Type “passwd” to change your password

```
-----users---load average-----users---load average---
ic5  (l): 0   0.01, 0.04, 0.05  ||  ic18 (D): 0   -----
ic19 (D): 0   -----          ||  ic21 (l): 1   0.13, 0.11, 0.04
ic22 (l): 1   0.01, 0.04, 0.00  ||  ic23 (l): 1   0.14, 0.08, 0.02
ic24 (l): 1   0.05, 0.08, 0.03  ||  ic25 (l): 0   0.06, 0.03, 0.01
ic26 (l): 0   0.00, 0.00, 0.00  ||  ic27 (l): 1   0.16, 0.19, 0.09
ic28 (l): 1   0.06, 0.09, 0.04  ||  ic29 (D): 0   -----
ic30 (l): 0   0.08, 0.09, 0.02  ||  ic52 (l): 0   0.00, 0.00, 0.00
ic53 (l): 0   0.00, 0.00, 0.00  ||  ic54 (l): 3   0.00, 0.00, 0.00
ic56 (l): 1   0.00, 0.00, 0.00  ||  ic57 (l): 2   0.00, 0.00, 0.00
ic58 (l): 4   1.64, 1.80, 2.10  ||
last updated: Tue Mar 13 16:55:01 CST 2018
(l) Linux, (s) SunOS, (D) Shutdown

----- You have 3 process(es) before login -----
UID      PID  PPID  C  STIME TTY      TIME CMD
CA120    5548 5543  0  16:55 ?        00:00:00 sshd: CA120@notty
CA120    5550 5548  0  16:55 ?        00:00:00 tcsh -c /usr/libexec/openssh/sftp-server
CA120    5565 5550  0  16:55 ?        00:00:00 /usr/libexec/openssh/sftp-server

[CA120@nthucad ~]$ passwd
Changing password for user CA120.
Changing password for CA120
(current) UNIX password:
New UNIX password:
Retype new UNIX password:
passwd: all authentication tokens updated successfully.
[CA120@nthucad ~]$
```



Connecting to Workstation

- Find a workstation with less users

```
-----users---load average-----users---load average---
ic21 (l): 5    0.02, 0.04, 0.00    ||    ic22 (l): 2    0.02, 0.03, 0.00
ic23 (l): 3    0.31, 0.44, 0.36    ||    ic26 (l): 4    0.00, 0.02, 0.00
ic27 (D): 0    ----, ----, ----    ||    ic29 (D): 0    ----, ----, ----
ic30 (l): 0    2.30, 2.18, 2.07    ||    ic52 (D): 0    ----, ----, ----
ic53 (l): 0    0.00, 0.02, 0.00    ||    ic55 (l): 5    0.23, 0.13, 0.10
ic56 (D): 0    ----, ----, ----    ||    ic57 (l): 10   1.00, 1.00, 1.00
ic58 (l): 2    0.00, 0.00, 0.00    ||
last updated: Tue Apr 13 11:38:01 CST 2021
(l) Linux, (s) SunOS, (D) Shutdown
```



Connecting to Workstation (Cont.)

- Connect to a work station
 - `ssh -X icXX` (XX should be 21~58)



Connecting to Workstation (Cont.)

```
[CA120@nthucad ~]$ ssh -X ic26
The authenticity of host 'ic26 (192.168.75.56)' can't be established.
RSA key fingerprint is d5:5b:44:76:cc:40:6d:fa:d6:bc:4e:d1:10:c9:2d:5b.
Are you sure you want to continue connecting (yes/no)? yes
Warning: Permanently added 'ic26,192.168.75.56' (RSA) to the list of known hosts.
CA120@ic26's password:
Last login: Tue Mar 22 00:17:44 2016 from nthucad.cs.nthu.edu.tw
-----users---load average-----users---load average---
ic5 (l): 0 0.00, 0.01, 0.05 || ic18 (D): 0 0.00, 0.00, 0.00
ic19 (D): 0 0.00, 0.00, 0.00 || ic21 (l): 1 0.16, 0.06, 0.01
ic22 (l): 1 0.05, 0.03, 0.00 || ic23 (l): 1 0.06, 0.04, 0.01
ic24 (l): 1 0.01, 0.05, 0.01 || ic25 (l): 1 0.03, 0.04, 0.00
ic26 (l): 0 0.00, 0.00, 0.00 || ic27 (l): 1 0.07, 0.06, 0.06
ic28 (l): 0 0.00, 0.03, 0.01 || ic29 (D): 0 0.00, 0.00, 0.00
ic30 (l): 0 0.00, 0.00, 0.00 || ic52 (l): 0 0.00, 0.00, 0.00
ic53 (l): 0 0.00, 0.00, 0.00 || ic54 (l): 3 0.00, 0.00, 0.00
ic56 (l): 1 0.00, 0.00, 0.00 || ic57 (l): 2 0.00, 0.00, 0.00
ic58 (l): 4 1.81, 1.70, 1.84 ||
last updated: Tue Mar 13 17:08:01 CST 2018
(l) Linux, (s) SunOS, (D) Shutdown

-----NTHU CS VLSI/CAD News-----
.For gcc 4.8.5 on centos 5 or gcc 4.9.3 on centos 6, use command
"source /tools/linux/gnu/setup_toolkit.csh".
.For loading information, use command "lab_uptime".
.For platform information, use command "lab_plat".
.For apply new account, please fill this sheet:
https://goo.gl/ym7Qt5
.If you have any problem, please contact us:
az55000055@gmail.com
Synopsys licenses have set!
Cadence license have set!
[CA120@ic26 ~]$
```

Should be [XXXXX@icXX ~]\$ if connect successfully



Create directory

- Right click to create new directory “example”
or by command line “mkdir example”



Create directory

The screenshot displays the MobaXterm interface with an SSH session to `cichung20@nthucad.cs.nthu.edu.tw`. The left sidebar shows the file explorer for `/users/student/mr109/cichung20/`. A red box labeled '1.' highlights the 'New directory' option in the sidebar. The main terminal window shows the SSH session output, including the NTHU VLSI/CAD logo and system information. A red box labeled '2.' highlights a 'MobaXterm' dialog box that prompts for a new directory name, with 'example' entered in the text field.

1. Parent directory
New directory
New empty file
Refresh current folder
Upload to current folder

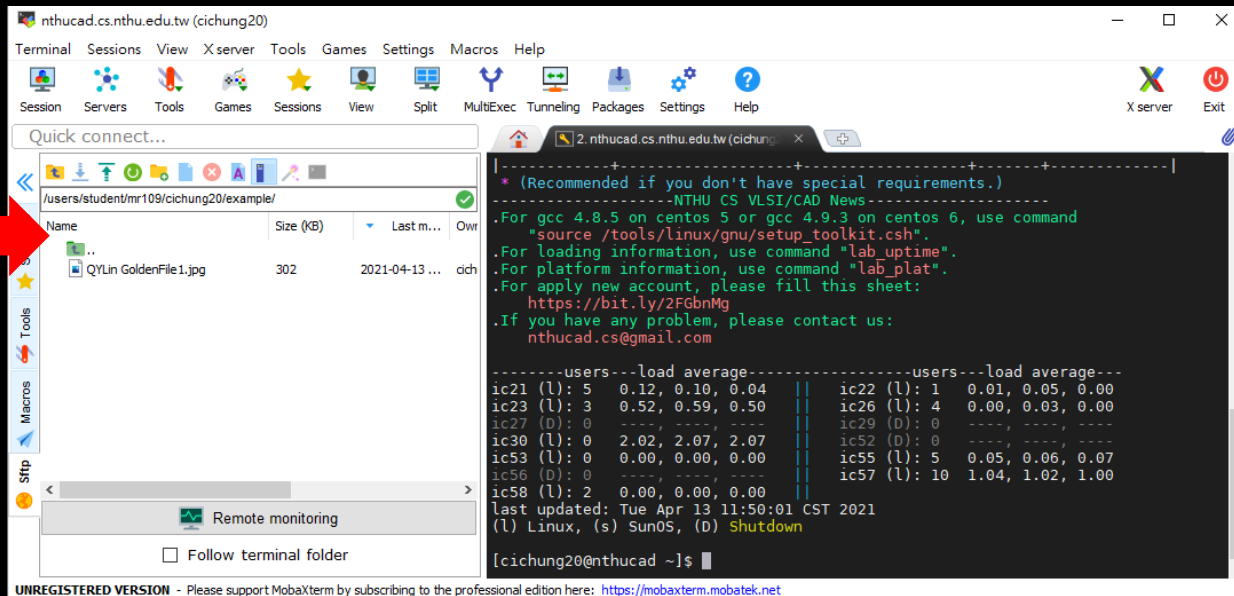
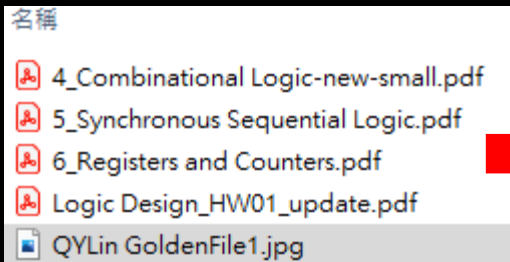
2. MobaXterm
Please enter the new directory name
example
OK Cancel

UNREGISTERED VERSION - Please support MobaXterm by subscribing to the professional edition here: <https://mobaxterm.mobatek.net>



Uploading Files

- Upload files
 - Upload your files by dragging them in to directory



Edit files in workstation

- ❑ Right click open with mobaXterm's editor
- ❑ Vim is available in workstation
- ❑ You can also edit in Windows then upload it

The screenshot displays a workstation interface with three main components:

- File Manager:** Shows a directory listing for `/users/student/mr109/cichung20/example/`. The file `verilog01.v` is selected, and a context menu is open with options like "Open", "Open with default text editor", "Download", "Delete", "Rename", "Copy file path", "Copy file path to terminal", "Properties", and "Permissions".
- Terminal Window:** Displays SSH connection status (SSH compression, SSH-browser, X11-forwarding, DISPLAY) and a login prompt. The login message shows the date and time: `login: Tue Apr 13 11:38:22 2021 from 140.114.75.65`. Below the login prompt is the NTHU VLSI/CAD logo.
- System Information Table:** A table listing system resources for various hosts.

Host	processor number	freq / # of core	Ram	OS
ic18	Xeon(R) E5530	2.40GHz/4C8Tx2	64G	CentOS 4.6
ic19	Xeon(R) E5530	2.40GHz/4C8Tx2	64G	CentOS 4.9
ic21-ic26	Xeon(R) X5570	2.93GHz/4C8Tx2	48G	CentOS 5.11
ic27-ic29	Xeon(R) E5-2643	3.30GHz/4C8Tx2	128G	CentOS 5.11
ic30	Xeon(R) E5-2637V2	3.50GHz/4C8Tx2	128G	CentOS 5.11
* ic52-ic53	Xeon(R) E5-2650V2	2.60GHz/8C16Tx2	64G	CentOS 5.11
* ic54-ic58	Xeon(R) E5-2650V2	2.60GHz/8C16Tx2	64G	CentOS 6.7

*(Recommended if you don't have special requirements.)

NTHU CS VLSI/CAD News-requirements



Run simulation

- Use NC verilog as standard simulation platform
- You can use any IDE/Editor to program



Run simulation (Cont.)

- ▣ \$ ncverilog all.v file you need
 - i.e. \$ ncverilog Test_Bench.v Simulator.v



Run simulation (Cont.)

```
[CA120@ic28 ~/sim]$ ncverilog Simulator.v Test_Bench.v
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
Loading snapshot worklib.Test_Bench.v ..... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
$0: 0
$1: 5
$2: 6
$3: 1
$4: 11
$5: 10
$6: 10
$7: 1
$8: 11
$9: 0
$10: 0
$11: 0
$12: 0
$13: 0
$14: 0
$15: 0
$16: 0
$17: 0
$18: 0
$19: 0
$20: 0
$21: 0
$22: 0
$23: 0
$24: 0
$25: 0
$26: 0
$27: 0
$28: 0
$29: 0
$30: 0
$31: 0
Simulation complete via $finish(1) at time 2010 NS + 0
./Test_Bench.v:47      #(`CYCLE_TIME*`END_CYCLE) $finish;
ncsim> exit
[CA120@ic28 ~/sim]$
```

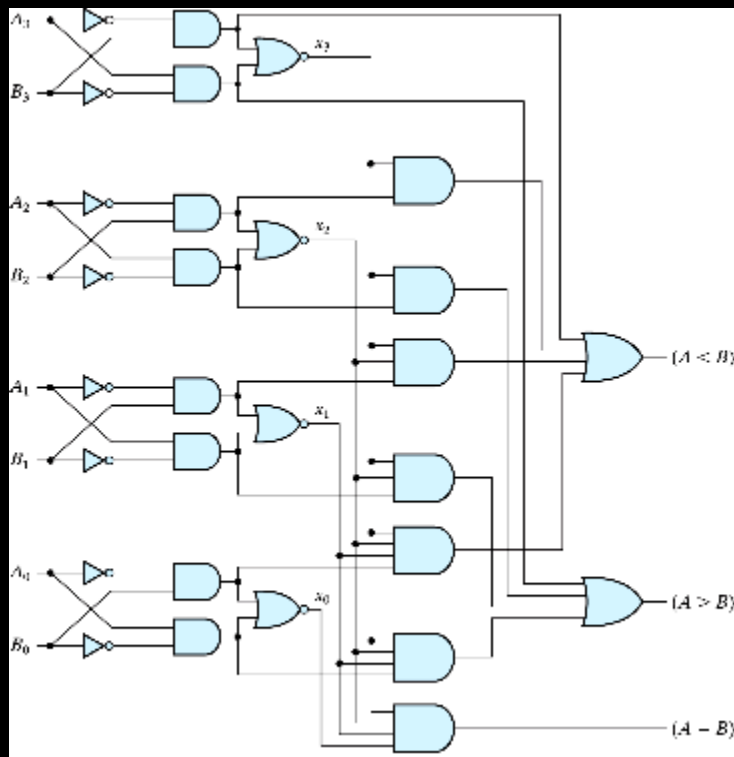


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4-bit Comparator



Rules

- $A_3A_2A_1A_0$, $B_3B_2B_1B_0$ are unsigned numbers
- Only basic logic gates are ALLOWED (and, or, nand, nor, not) ,no xor & xnor
- Please **AVOID** using
 1. Continuous assignment and conditional operators
 2. Behavioral operators (e.g., +, -, &, |, ^, &&, !, ~....., etc.)
 3. Behavioral operators are ALLOWED in your TESTBENCH
- Edit your own testbench



Please Follow The Format Below

```
module Comparator_4bits (A, B, A_lt_B, A_gt_B, A_eq_B);  
input [4-1:0] A;  
input [4-1:0] B;  
output A_lt_B, A_gt_B, A_eq_B;  
  
// here is your design  
  
endmodule
```



Submission

- Lab 1 code submission due date & time: 2021/04/22,11:59pm
- Please submit your Verilog codes to ILMS
 - Lab1_YourStudentID_Codes.v
- We will test your codes by our own testbench

