Lab 1: Shifter

Submission Due Dates:

Demo:	2021/10/05 17:20
Source Code:	2021/10/05 18:30
Report:	2021/10/10 23:59

Objective

Getting familiar with basic Verilog modeling styles.

Action Items

1 lab1_1.v (40%)

Write a Verilog module that models a **4-bit shifter** and test your module using the testbench file lab1_1_t.v. Note that if input port “dir” is equal to 0, the output will be a << b. Otherwise, the output will be a >> b. Test your design with lab1_1_t.v (see the description below).

a. IO list:
- ✔ Inputs: a, b, dir
- ✔ Output: d

b. **dir**: To control the shifting direction.

If dir == 0, then d = a << b.
If dir == 1, then d = a >> b.
(You can use << and >> directly in your code.)

c. You have to use the following template for your design:

```
`timescale 1ns/100ps
module lab1_1 (a, b, dir, d);
  input [3:0] a;
  input [1:0] b;
  input dir;
  output reg [3:0] d; /* Note that d can be either reg or
                         wire. It depends on how you design
                         your module. */
  // add your design here
endmodule
```

2 lab1_1_t.v (20%)

Complete the testbench lab1_1_t.v to verify your design. Check the TODO hints in the template code carefully. For incorrect results, you may see an error message like this:

```
Error:  a = XXXX, b = XX, d = XXXX, dir = X
```

where X are the corresponding data bits.

3 lab1_2.v (40%)

Write a Verilog module that models a **4-bit ALU** and test your module by using the testbench lab1_2_t.v. **The 4-bit ALU must reuse the previous 4-bit shifters (i.e., lab1_1) to shift the input. In other words, using << and >> is forbidden in the top module of lab 1_2.**

a. IO list:
   - ✔ Inputs: a, b, aluctr
   - ✔ Output: d

b. **aluctr**:

```
if aluctr == 2'b00:
        d = a << b
else if aluctr == 2'b01:
        d = a >> b
else if aluctr == 2'b10:
        d = a + b
else:
        d = a - b
```

(Note that << and >> are forbidden in the top module of lab1_2. You should reuse lab1_1 to shift the input.)

c. You have to use the following template for your design:

```
`timescale 1ns/100ps

module lab1_2 (a, b, aluctr, d);
  input [3:0] a;
  input [1:0] b;
  input [1:0] aluctr;
  output reg [3:0] d; /* Note that d can be either reg or
                         wire. It depends on how you design
                         your module. */
  // add your design here
endmodule
```

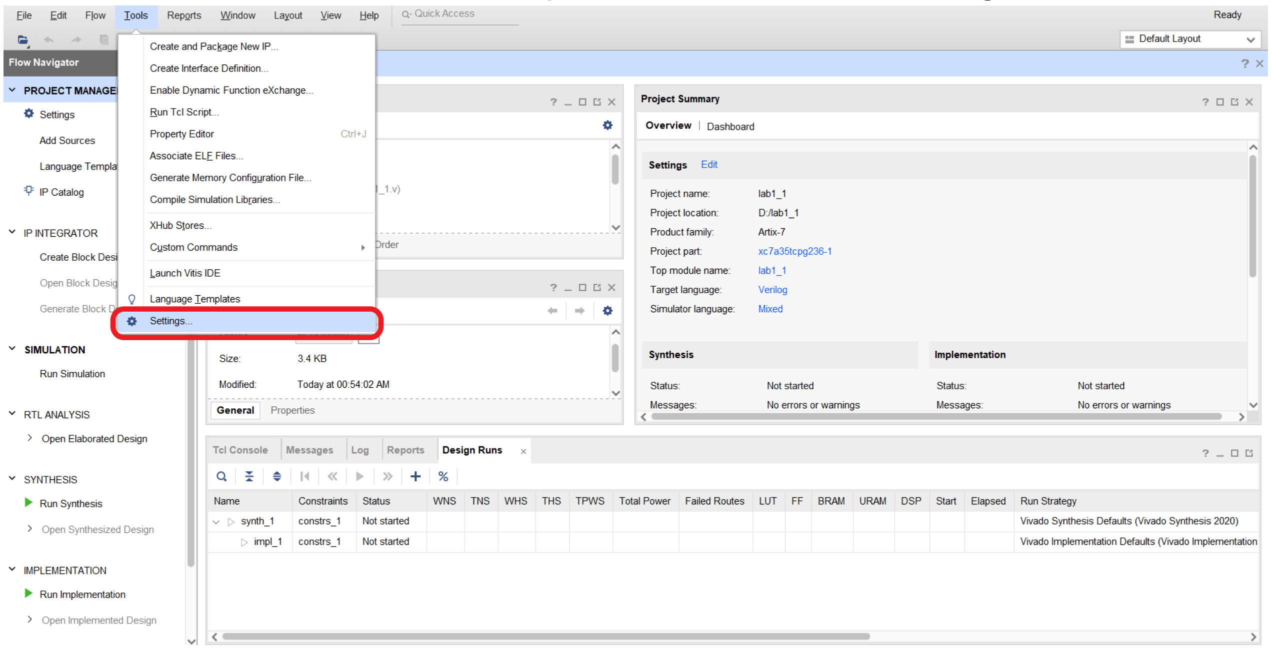
Attention

- ✔ DO NOT copy-and-paste code segments from the PDF materials. Occasionally, it will also paste invisible non-ASCII characters and lead to hard-to-debug syntax errors.
- ✔ You should hand in three source files, including **lab1_1.v, lab1_1_t.v, lab1_2.v**. Upload each source file directly! DO NOT hand in any compressed ZIP files!
- ✔ You should also hand in your report as **lab1_report_StudentID.pdf** (i.e., lab1_report_108456789.pdf).
- ✔ You should be able to answer questions of this lab from TA during the demo.

✔ You may also add a **$monitor** in the testbench to show all the inputs and outputs during the simulation.

✔ Before the simulation, you may need to change the runtime to 10000ns (or a large enough period) in “Simulation Settings”. See the guide below.

1. Click Tools at the top of Vivado and select settings.



Project name: lab1_1
Project location: D:/lab1_1
Product family: Artix-7
Project part: xc7a35tcpg236-1
Top module name: lab1_1
Target language: Verilog
Simulator language: Mixed

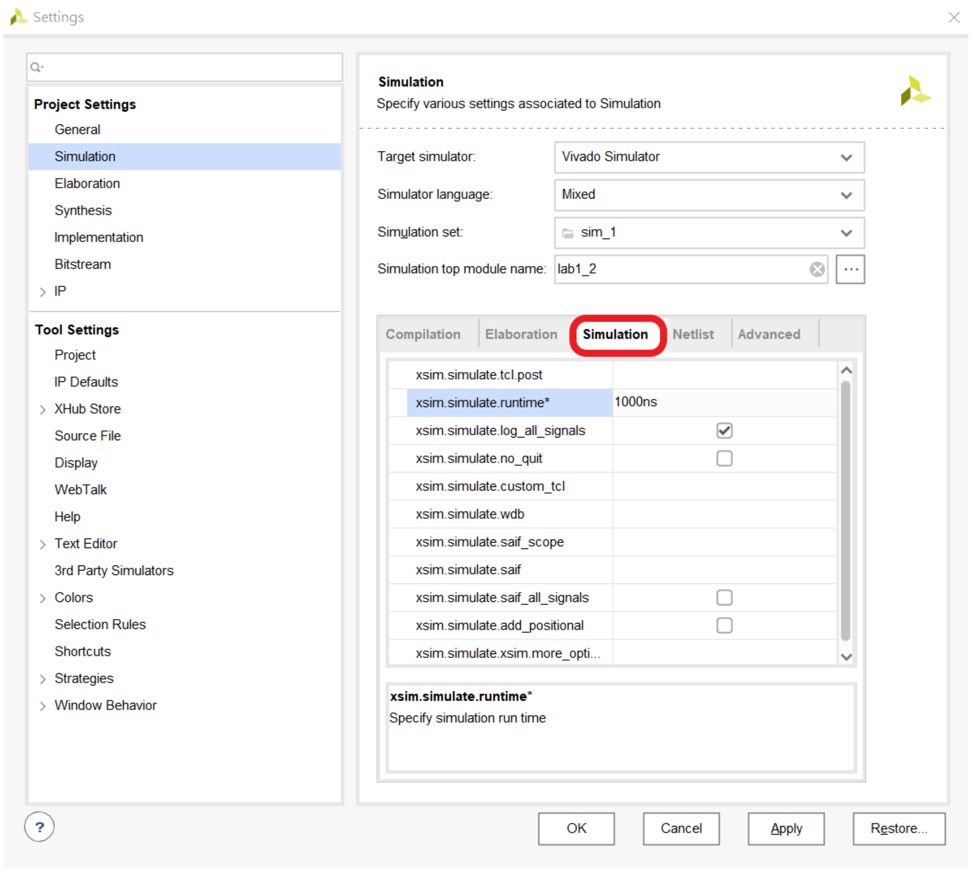
Synthesis
Status: Not started
Messages: No errors or warnings

Implementation
Status: Not started
Messages: No errors or warnings

Size: 3.4 KB
Modified: Today at 00:54:02 AM

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation

2. Select Simulation.



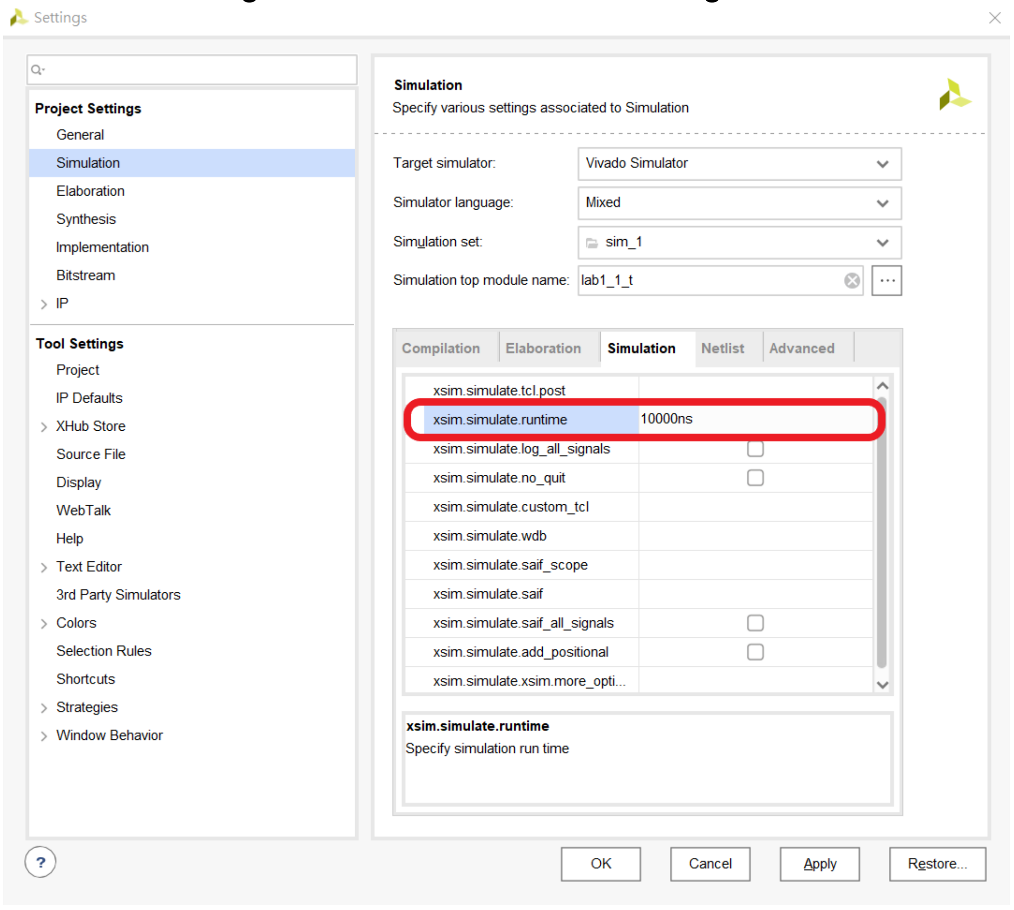
Simulation
Specify various settings associated to Simulation

Target simulator: Vivado Simulator
Simulator language: Mixed
Simulation set: sim_1
Simulation top module name: lab1_2

xsim.simulate.tcl.post	
xsim.simulate.runtime*	1000ns
xsim.simulate.log_all_signals	✓
xsim.simulate.no_quit	☐
xsim.simulate.custom_tcl	
xsim.simulate.wdb	
xsim.simulate.saif_scope	
xsim.simulate.saif	
xsim.simulate.saif_all_signals	☐
xsim.simulate.add_positional	☐
xsim.simulate.xsim.more_opti...	

xsim.simulate.runtime*
Specify simulation run time

3. Change runtime to 10000ns or a larger value.



Settings

Project Settings
- General
- Simulation
- Elaboration
- Synthesis
- Implementation
- Bitstream
- IP

Tool Settings
- Project
- IP Defaults
- XHub Store
- Source File
- Display
- WebTalk
- Help
- Text Editor
- 3rd Party Simulators
- Colors
- Selection Rules
- Shortcuts
- Strategies
- Window Behavior

Simulation
Specify various settings associated to Simulation

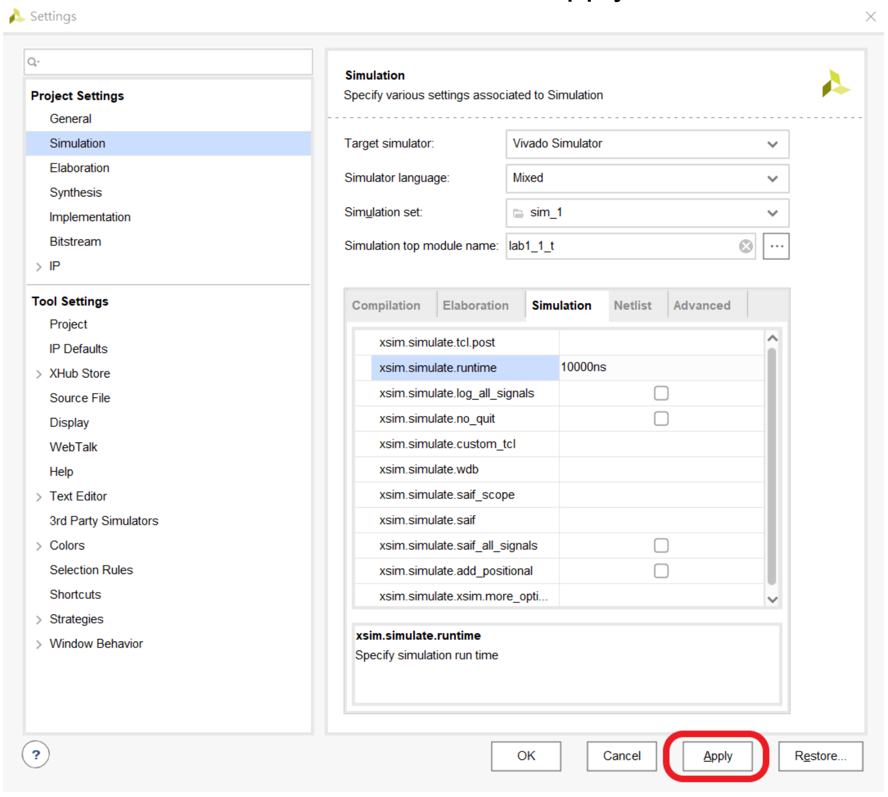
Target simulator:	Vivado Simulator
Simulator language:	Mixed
Simulation set:	sim_1
Simulation top module name:	lab1_1_t

Compilation | Elaboration | **Simulation** | Netlist | Advanced

xsim.simulate.tcl.post	
xsim.simulate.runtime	10000ns
xsim.simulate.log_all_signals	☐
xsim.simulate.no_quit	☐
xsim.simulate.custom_tcl	
xsim.simulate.wdb	
xsim.simulate.saif_scope	
xsim.simulate.saif	
xsim.simulate.saif_all_signals	☐
xsim.simulate.add_positional	☐
xsim.simulate.xsim.more_opti...	

xsim.simulate.runtime
Specify simulation run time

4. Remember to click Apply.



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Simulation
Specify various settings associated to Simulation

Target simulator:	Vivado Simulator
Simulator language:	Mixed
Simulation set:	sim_1
Simulation top module name:	lab1_1_t

Compilation | Elaboration | **Simulation** | Netlist | Advanced

xsim.simulate.tcl.post	
xsim.simulate.runtime	10000ns
xsim.simulate.log_all_signals	☐
xsim.simulate.no_quit	☐
xsim.simulate.custom_tcl	
xsim.simulate.wdb	
xsim.simulate.saif_scope	
xsim.simulate.saif	
xsim.simulate.saif_all_signals	☐
xsim.simulate.add_positional	☐
xsim.simulate.xsim.more_opti...	

xsim.simulate.runtime
Specify simulation run time