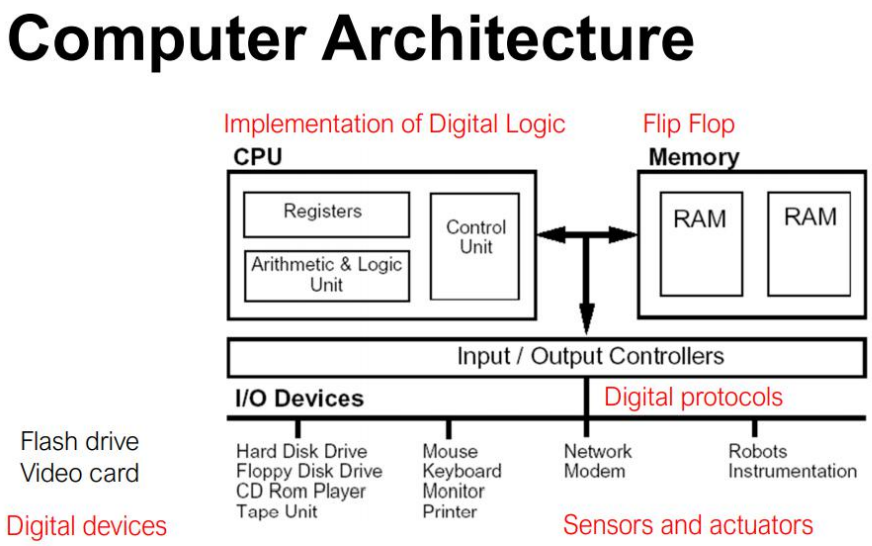
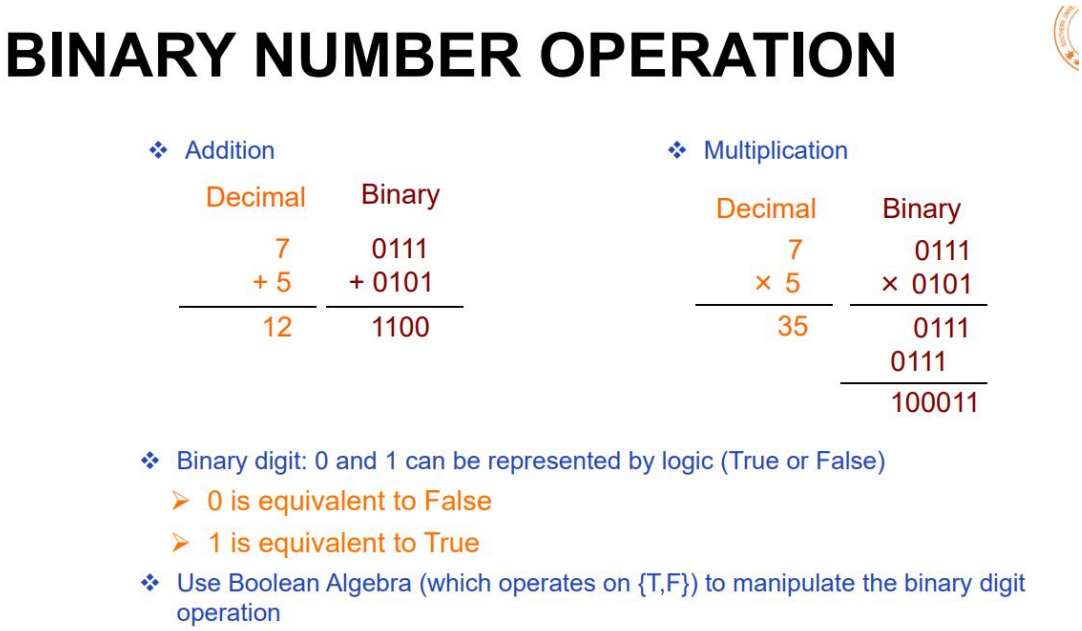
3-刘洪磊-week13

1. 计算机结构



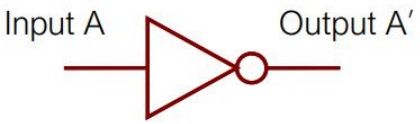
2. 二进制计算



3. 七种逻辑门

- Inverter (Not) – 1 input, 1 output
- AND – 2 or more inputs, 1 output
- NAND – 2 or more inputs, 1 output
- OR – 2 or more inputs, 1 output
- NOR – 2 or more inputs, 1 output
- XOR – 2 or more inputs, 1 output
- XNOR – 2 or more inputs, 1 output

3.1 Not



Input A	Output A′
0	1
1	0

3.2 And (二进制的乘法)

- AND gate: Output = A•B

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

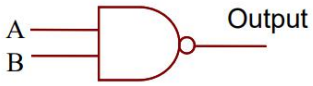
3.3 Or （二进制的加法）

- OR gate: Output = A+B

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

3.4 Nand

❖ NAND gate: Output = $\overline{A \cdot B}$



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

3.5 Nor

❖ NOR gate: Output = $\overline{A+B}$

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

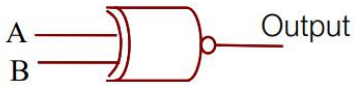
3.6 Xor

❖ XOR gate: Output = $A \oplus B$

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

3.7 Xnor

❖ XNOR gate: Output = $\overline{A \oplus B}$



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

4. 布尔运算规则

LAW OF BOOLEAN ALBEGRA

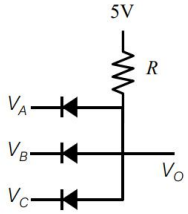
- 0+X = X
- 1+X = 1
- X′+X = 1
- 0•X = 0
- 1•X = X
- X•X = X
- X•X′ = 0
- (X′)′ = X
- X+Y = Y+X
- X•Y = Y•X

- X+(Y+Z) = (X+Y)+Z (Associativity)
- X•(Y•Z) = (X•Y)•Z (Associativity)
- X•(Y+Z) = X•Y+X•Z (Distributivity)
- X+X•Z = X
- X•(X+Y) = X
- (X+Y)•(X+Z) = X+Y•Z
- X′+XY = X′+Y
- (XY)′+(YZ)′+(XZ)′ = (XY)′+(XZ)′
- (X+Y)′ = X′ • Y′
- (XY)′ = X′+Y′ (DeMorgan's Law)

5. 模拟电路实现 AND

LOGIC GATE CONSTRUCTION

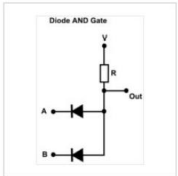
❖ AND gate



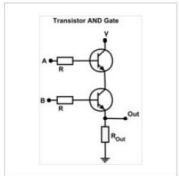
Input/Output Table

V_A	V_B	V_C	V_O
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

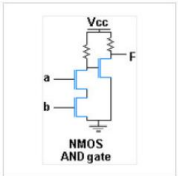
1 =
0 =



AND gate using diodes

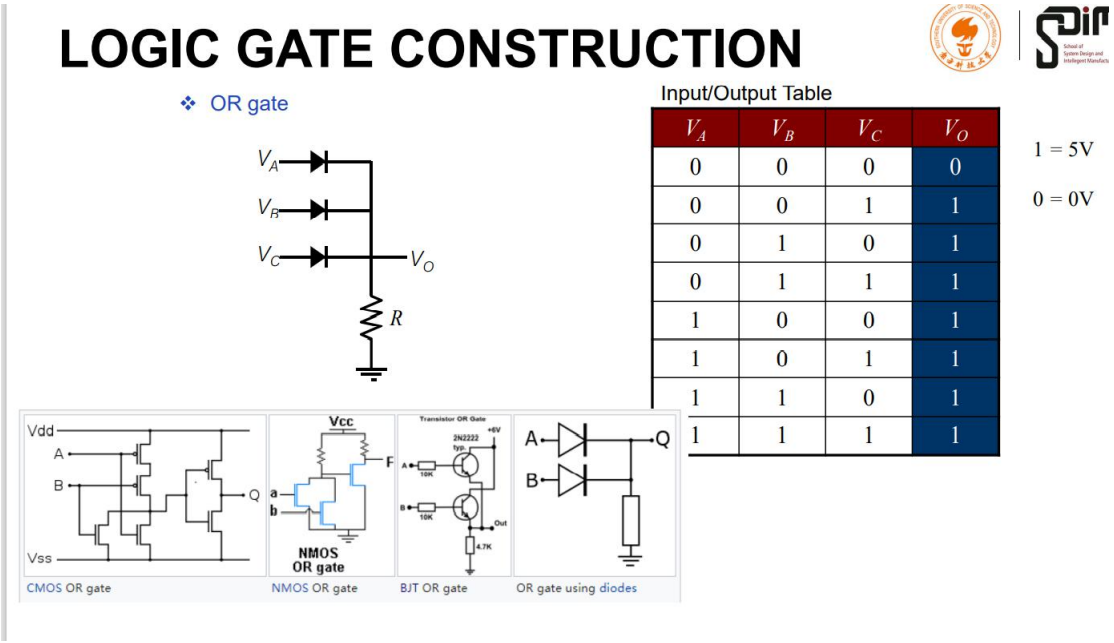


AND gate using transistors



NMOS AND gate

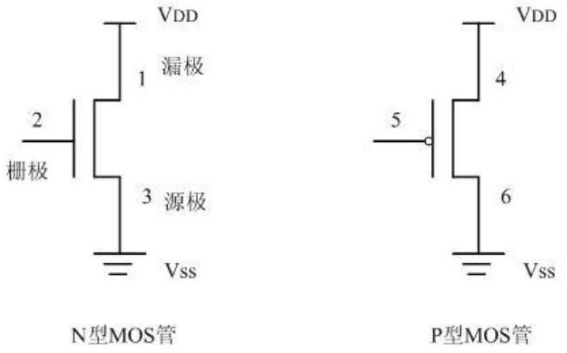
6. 模拟电路实现 OR



V_A	V_B	V_C	V_O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

1.NMOS 实现或门：

1、MOS 管　　MOS 管又分为两种类型：N 型和 P 型。如下图所示：



N型MOS管　　P型MOS管

以 N 型管为例，2 端为控制端，称为“栅极”；3 端通常接地，称为“源极”；源极电压记作 Vss，1 端接正电压，称为“漏极”，漏极电压记作 VDD。要使 1 端与 3 端导通，栅极 2 上要加高电平。

对 P 型管，栅极、源极、漏极分别为 5 端、4 端、6 端。要使 4 端与 6 端导通，栅极 5 要加低电平。

如果 AB 都为低电平，那么右方 NMOS 管会因为电压差导通，经过唯一一个电阻的压降之后，输出为低电平。如果 AB 中任意一个为高电平，那么左方就会导通一条通路，经过唯一一个电阻的压降之后，右方的 NMOS 管的 Vgs 就是 0-0=0，不导通，从而输出端的电平就是高电平。

2.三极管实现或门：当 AB 都为低电平，Q 输出为低电平，当 AB 中任意一个或两个为高电平，Q 输出为低电平。（此处可以用较小电流触发）

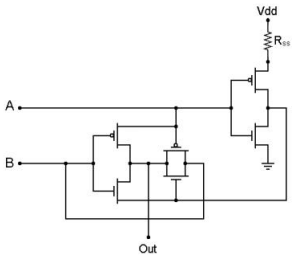
3.二极管实现或门：当 AB 都为低电平，Q 输出为低电平，当 AB 中任意一个或两个为高电

平，Q 输出为低电平。

7. 模拟电路实现 XOR

LOGIC GATE CONSTRUCTION

❖ XOR gate



Input/Output Table

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

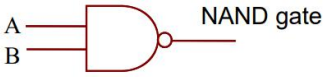
1 = 5V

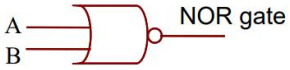
0 = 0V

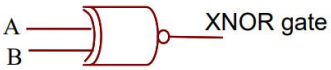
8. 门的记号

❖ Binary digit: 0 and 1 can be represented by logic (True or False)

- 0 is equivalent to False
- 1 is equivalent to True



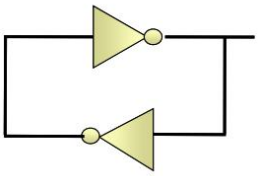




9. 存储

FLIP-FLOP

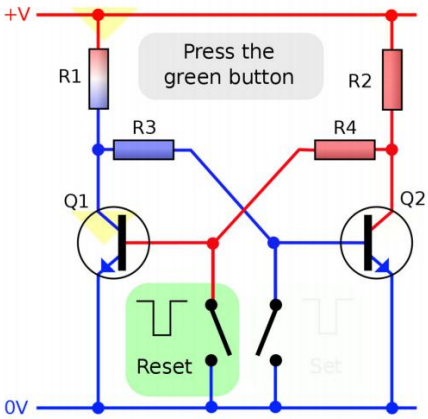
- When we set the output of a flip-flop to 0, it should stay at 0, and if we set the output to 1, it should stay at 1
- It can be achieved by having two inverters cross connect to each other
- It is also called memory operation by feedback



Static memories are based on this cross-coupled feedback inverter pair

- How to set the value?

Flip Flop Implementation



Analog circuit! Q: Understand why this works as expected.

此为双稳态电路，没有外来信号时，三极管始终保持原来的截止或饱和状态不变，当有外来信号触发时，原来截止的变为饱和状态并保持不变，原来饱和的变为截止状态也保持不变。

当 Q1 三极管关闭时，Q2 三极管会被开启并保持稳定。