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Amplifier Parameters

Input offset voltage

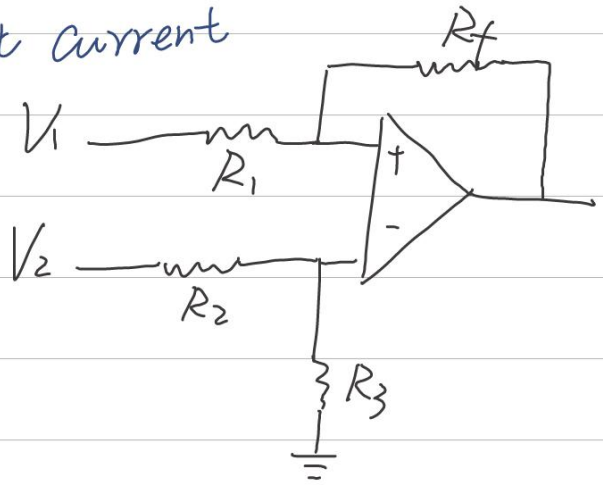
Offset voltage drift

Time or temperature $\frac{\Delta V_{os}}{\Delta T} = X\ \mu V/^{\circ}C$

Input bias current

Input offset current

失调



$$V_{out} = \frac{R_f}{R_1}(V_2 - V_1) + I_{offset} \cdot R_f$$

when $R_2 = R_1$, $R_3 = R_f$

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Input impedance 输入阻抗.

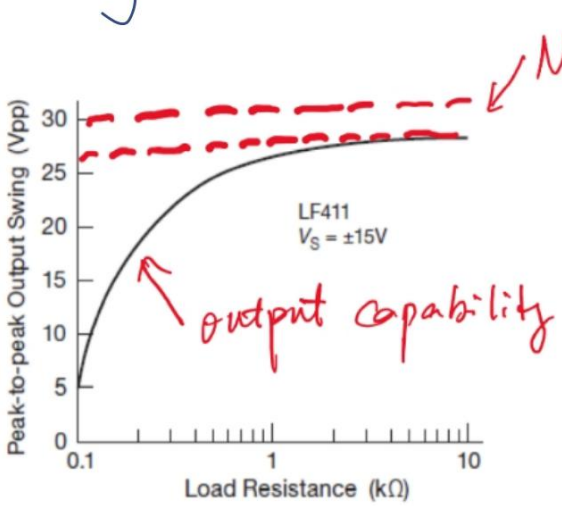
- Q: What is a typical input impedance value for BJT?
- Q: What is a typical input impedance value for FET?

都很大，BJT 相比 FET 小.

Common-mode input range

Differential input range

Output swing vs. load resistance



Output Impedance 输出阻抗 尽可能小

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Slew rate 压摆率

LF411 : 15 V/μs

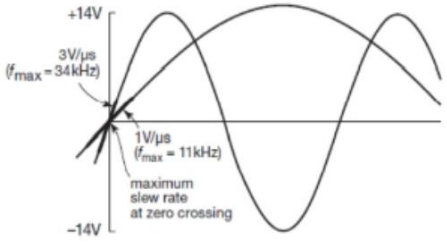
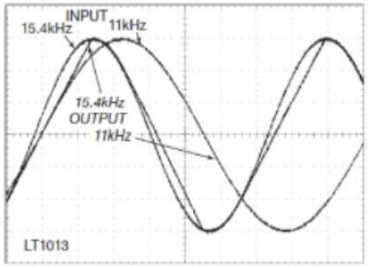


Figure 4.48. The maximum slew rate of a sinewave, SR=$2\pi Af$, occurs at the zero crossings.



Temperature dependence

Supply voltage and current

- Pay attention to the maximum values
- +5V or +15V

411 : ±5V → ±18V

Low power : 3V

Q ① why do we need a high rail?

② why do we need a low rail?

rail: 电源轨 限制了运放的输入输出信号并保持不失真.

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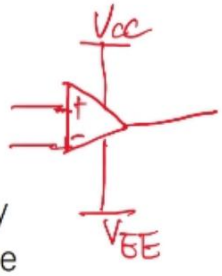
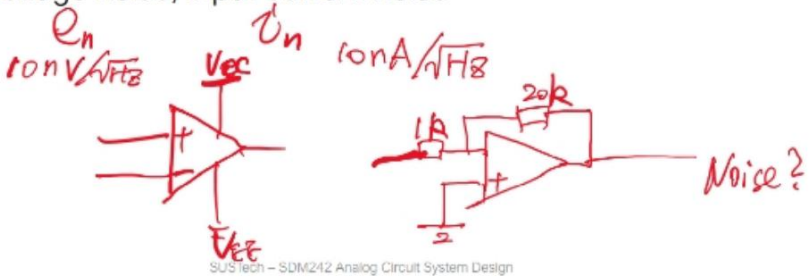
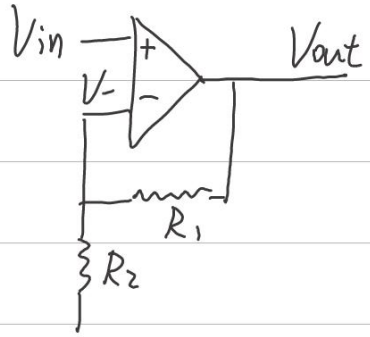
CMRR, PSRR, e_n, i_n

- Common mode rejection ratio
- Power supply rejection ratio
- Especially important at high frequency
- Input voltage noise, input current noise





Gain



开环

$$\begin{cases} (V_{in}-V_-)\cdot A = V_{out} \\ \dfrac{V_-}{R_2} = \dfrac{V_{out}}{R_1+R_2} \end{cases}$$

$$\Downarrow$$

$$V_- = \frac{R_2}{R_1+R_2} V_{out} = B V_{out}$$

$$\frac{A}{1+AB}$$

代回: $\dfrac{V_{out}}{V_{in}} = G = \dfrac{A}{1+AB}$

闭环

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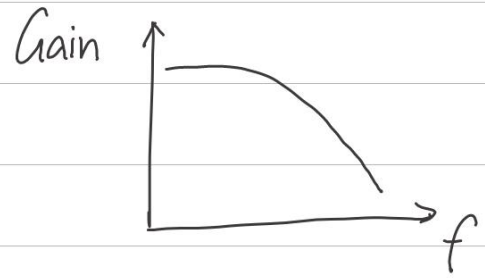
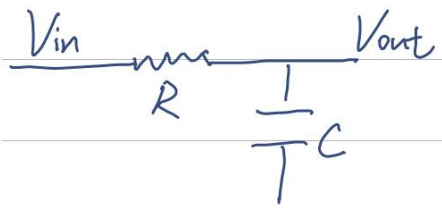
Bandwidth



$GBP = G \times B \qquad G = \frac{GBP}{B}$

$\log G = \log GBP - \log B$

多级放大器 $G_1 * G_2 * G_3$



$$G = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{jwC}}{R + \frac{1}{jwC}} = \frac{1}{1 + jwRC}$$

运放闭环 similar to 低通 filter

$w = 2\pi f$

全功率带宽BW：

全功率带宽定义为，在额定的负载时，运放的闭环增益为1倍条件下，将一个恒幅正弦大信号输入到运放的输入端，使运放输出幅度达到最大（允许一定失真）的信号频率。这个频率受到运放转换速率的限制。近似地，全功率带宽=转换速率/2πVop（Vop是运放的峰值输出幅度）。全功率带宽是一个很重要的指标，用于大信号处理中运放选型。

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Multistage Op-Amp

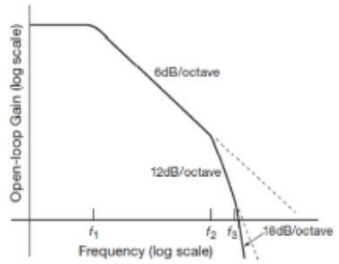

Figure 4.96. Multistage amplifier: gain versus frequency.

Magnitude

This will be disasterous!

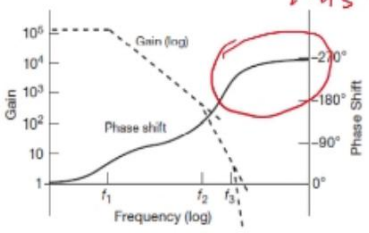

Figure 4.98. Gain and phase in a multistage amplifier.

phase

Stability Measures

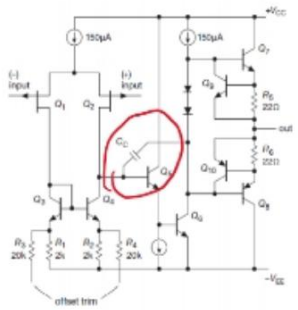

Figure 4.43. Simplified schematic of the LF411 op-amp.

purposely design

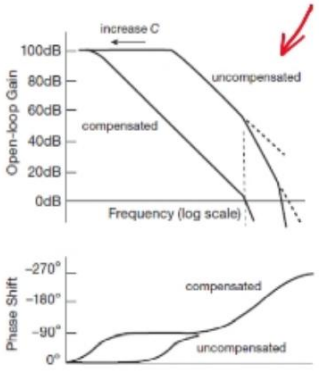

Figure 4.99. "Dominant-pole" compensation.

Intuition: Why C can help?

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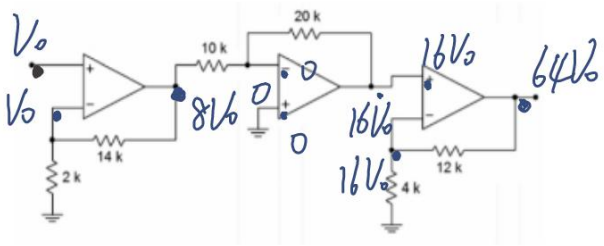
Cascaded op-amp



Question:

1. Is stability a concern here? Why?
2. All three are UA741 from ST, what is the final gain and upper break frequency?

1. No. There is no 180° phase difference between two amps

2. $\frac{V_{out}}{V_{in}} = \frac{64V_o}{V_o} = 64$

GBWP = 1MHz

运放① BW = $10^6/8$ = 125 kHz

运放② BW = $10^6/2$ = 500 kHz

运放③ BW = $10^6/4$ = 250 kHz

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一个运放的上截止频率 $f_H = \frac{10^6}{0.707} \approx 1.414 \times 10^6 Hz$