```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     2 ************************************************************************
                                                     3 *
                                                     4 *        EXPERIMENTAL pending further PoP definition
                                                     5 *
                                                     6 *        Zvector E6 instruction tests for VRR-a encoded:
                                                     7 *
                                                     8 *        E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                     9 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                    10 *        E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                    11 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                    12 *
                                                    13 *        and partial testing of
                                                    14 *
                                                    15 *        E675  VCRNF   - VECTOR FP CONVERT AND ROUND TO NNP
                                                    16 *
                                                    17 *        during cross check tests for VCLFNH and VCLFNL
                                                    18 *
                                                    19 *        James Wekel August 2024
                                                    20 ************************************************************************


                                                    22 ************************************************************************
                                                    23 *
                                                    24 *        basic instruction tests
                                                    25 *
                                                    26 ************************************************************************
                                                    27 *  This program tests EXPERIMENTAL functioning of the z/arch E6 VRR-a
                                                    28 *  Neural-network-processing-assist facility vector instructions.
                                                    29 *  These test are EXPERIMENTAL pending further PoP definition of
                                                    30 *  NNP-data-type-1.
                                                    31 *
                                                    32 *  If requested and if VXC == 0 after test instruction execution,
                                                    33 *  a cross check test is performed. A cross check uses the result
                                                    34 *  of the instruction test to recreate the test source.
                                                    35 *
                                                    36 *  Exceptions (including trapable IEEE exceptions) are not tested.
                                                    37 *
                                                    38 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    39 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    40 *  NOT designed to test all aspects of any of the instructions.
                                                    41 *
                                                    42 ************************************************************************
                                                    43 *
                                                    44 *    *Testcase zvector-e6-20-NNPconvert
                                                    45 *    *
                                                    46 *    *   EXPERIMENTAL pending further PoP definition
                                                    47 *    *
                                                    48 *    *   Zvector E6 instruction tests for VRR-a encoded:
                                                    49 *    *
                                                    50 *    *   E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                    51 *    *   E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                    52 *    *   E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                    53 *    *   E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                    54 *    *
                                                    55 *    *   # ------------------------------------------------------
                                                    56 *    *   #  This tests only the basic function of the instruction.
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   57 *    *   #  Exceptions are NOT tested.
                                                   58 *    *   # ------------------------------------------------------------
                                                   59 *    *
                                                   60 *    mainsize    2
                                                   61 *    numcpu      1
                                                   62 *    sysclear
                                                   63 *    archlvl     z/Arch
                                                   64 *
                                                   65 *    loadcore    "$(testpath)/zvector-e6-20-NNPconvert.core" 0x0
                                                   66 *
                                                   67 *    diag8cmd    enable    # (needed for messages to Hercules console)
                                                   68 *    runtest 2
                                                   69 *    diag8cmd    disable   # (reset back to default)
                                                   70 *
                                                   71 *    *Done
                                                   72 *
                                                   73 ***********************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   75 ***********************************************************************
                                                   76 *        FCHECK Macro - Is a Facility Bit set?
                                                   77 *
                                                   78 *        If the facility bit is NOT set, an message is issued and
                                                   79 *        the test is skipped.
                                                   80 *
                                                   81 *        Fcheck uses R0, R1 and R2
                                                   82 *
                                                   83 * eg.    FCHECK 134,'vector-packed-decimal'
                                                   84 ***********************************************************************
                                                   85          MACRO
                                                   86          FCHECK &BITNO,&NOTSETMSG
                                                   87 .*                        &BITNO : facility bit number to check
                                                   88 .*                        &NOTSETMSG : 'facility name'
                                                   89          LCLA  &FBBYTE           Facility bit in Byte
                                                   90          LCLA  &FBBIT            Facility bit within Byte
                                                   91
                                                   92          LCLA  &L(8)
                                                   93 &L(1)    SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                   94
                                                   95 &FBBYTE  SETA  &BITNO/8
                                                   96 &FBBIT   SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                   97 .*       MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                   98
                                                   99          B     X&SYSNDX
                                                  100 *                                       Fcheck data area
                                                  101 *                                       skip messgae
                                                  102 SKT&SYSNDX DC  C'          Skipping tests: '
                                                  103          DC    C&NOTSETMSG
                                                  104          DC    C' facility (bit &BITNO) is not installed.'
                                                  105 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                  106 *                                       facility bits
                                                  107          DS    FD                      gap
                                                  108 FB&SYSNDX DS   4FD
                                                  109          DS    FD                      gap
                                                  110 *
                                                  111 X&SYSNDX EQU *
                                                  112          LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                  113          STFLE FB&SYSNDX               get facility bits
                                                  114
                                                  115          XGR   R0,R0
                                                  116          IC    R0,FB&SYSNDX+&FBBYTE    get fbit byte
                                                  117          N     R0,=F'&FBBIT'           is bit set?
                                                  118          BNZ   XC&SYSNDX
                                                  119 *
                                                  120 * facility bit not set, issue message and exit
                                                  121 *
                                                  122          LA    R0,SKL&SYSNDX           message length
                                                  123          LA    R1,SKT&SYSNDX           message address
                                                  124          BAL   R2,MSG
                                                  125
                                                  126          B     EOJ
                                                  127 XC&SYSNDX EQU *
                                                  128          MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   130 ************************************************************************
                                                   131 *        Low core PSWs
                                                   132 ************************************************************************


                             00000000  000055D7   134 ZVE6TST  START 0
00000000                     00000000              135          USING ZVE6TST,R0            Low core addressability
                                                   136
                             00000140  00000000   137 SVOLDPSW EQU   ZVE6TST+X'140'        z/Arch Supervisor call old PSW


00000000                     00000000  000001A0   139          ORG   ZVE6TST+X'1A0'        z/Architecture RESTART PSW
000001A0  00000001 80000000                        140          DC    X'0000000180000000'
000001A8  00000000 00000200                        141          DC    AD(BEGIN)


000001B0                     000001B0  000001D0   143          ORG   ZVE6TST+X'1D0'        z/Architecture PROGRAM CHECK PSW
000001D0  00020001 80000000                        144          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                        145          DC    AD(X'DEAD')


000001E0                     000001E0  00000200   147          ORG   ZVE6TST+X'200'        Start of actual test program...
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   149
                                                   150 ************************************************************************
                                                   151 *                The actual "ZVE6TST" program itself...
                                                   152 ************************************************************************
                                                   153 *
                                                   154 *  Architecture Mode: z/Arch
                                                   155 *  Register Usage:
                                                   156 *
                                                   157 *   R0       (work)
                                                   158 *   R1-4     (work)
                                                   159 *   R5       Testing control table - current test base
                                                   160 *   R6       (work)
                                                   161 *   R7       msg return
                                                   162 *   R8       First base register
                                                   163 *   R9       Second base register
                                                   164 *   R10      Third base register
                                                   165 *   R11      E6TEST call return
                                                   166 *   R12      E6TESTS register
                                                   167 *   R13      (work)
                                                   168 *   R14      Subroutine call
                                                   169 *   R15      Secondary Subroutine call or work
                                                   170 *
                                                   171 ************************************************************************

00000200                      00000200             173          USING  BEGIN,R8               FIRST Base Register
00000200                      00001200             174          USING  BEGIN+4096,R9          SECOND Base Register
00000200                      00002200             175          USING  BEGIN+8192,R10         THIRD Base Register
                                                   176
00000200  0580                                     177 BEGIN    BALR   R8,0                    Initialize FIRST base register
00000202  0680                                     178          BCTR   R8,0                    Initialize FIRST base register
00000204  0680                                     179          BCTR   R8,0                    Initialize FIRST base register
                                                   180
00000206  4190 8800                   00000800     181          LA     R9,2048(,R8)            Initialize SECOND base register
0000020A  4190 9800                   00000800     182          LA     R9,2048(,R9)            Initialize SECOND base register
                                                   183
0000020E  41A0 9800                   00000800     184          LA     R10,2048(,R9)           Initialize THIRD base register
00000212  41A0 A800                   00000800     185          LA     R10,2048(,R10)          Initialize THIRD base register
                                                   186
00000216  B600 859C                   0000079C     187          STCTL  R0,R0,CTLR0             Store CR0 to enable AFP
0000021A  9604 859D                   0000079D     188          OI     CTLR0+1,X'04'           Turn on AFP bit
0000021E  9602 859D                   0000079D     189          OI     CTLR0+1,X'02'           Turn on Vector bit
00000222  B700 859C                   0000079C     190          LCTL   R0,R0,CTLR0             Reload updated CR0
                                                   191
                                                   192 ************************************************************************
                                                   193 * Is Neural-network-processing-assist facility 2 installed  (bit 165)
                                                   194 ************************************************************************
                                                   195
                                                   196          FCHECK 165,'Neural-network-processing-assist'
00000226  47F0 80C0                   000002C0     197+         B      X0001
                                                   198+*                                         Fcheck data area
                                                   199+*                                         skip messgae
0000022A  40404040 40404040                        200+SKT0001  DC     C'          Skipping tests: '
00000244  D585A499 81936095                        201+         DC     C'Neural-network-processing-assist'
00000264  40868183 899389A3                        202+         DC     C' facility (bit 165) is not installed.'
                              0000005F  00000001   203+SKL0001  EQU    *-SKT0001
                                                   204+*                                         facility bits
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00000290  00000000 00000000                        205+         DS    FD                      gap
00000298  00000000 00000000                        206+FB0001   DS    4FD
000002B8  00000000 00000000                        207+         DS    FD                      gap
                                                   208+*
                             000002C0  00000001    209+X0001    EQU   *
000002C0  4100 0004                  00000004      210+         LA    R0,((X0001-FB0001)/8)-1
000002C4  B2B0 8098                  00000298      211+         STFLE FB0001                  get facility bits
000002C8  B982 0000                                212+         XGR   R0,R0
000002CC  4300 80AC                  000002AC      213+         IC    R0,FB0001+20            get fbit byte
000002D0  5400 85F0                  000007F0      214+         N     R0,=F'4'                is bit set?
000002D4  4770 80E8                  000002E8      215+         BNZ   XC0001
                                                   216+*
                                                   217+* facility bit not set, issue message and exit
                                                   218+*
000002D8  4100 005F                  0000005F      219+         LA    R0,SKL0001              message length
000002DC  4110 802A                  0000022A      220+         LA    R1,SKT0001              message address
000002E0  4520 84B0                  000006B0      221+         BAL   R2,MSG
000002E4  47F0 8580                  00000780      222+         B     EOJ
                             000002E8  00000001    223+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   225 ***********************************************************************
                                                   226 *               Do tests in the E6TESTS table
                                                   227 ***********************************************************************
                                                   228
000002E8  58C0 85F4                      000007F4  229          L     R12,=A(E6TESTS)        get table of test addresses
                                                   230
                                 000002EC  00000001 231 NEXTE6   EQU   *
000002EC  5850 C000                      00000000  232          L     R5,0(0,R12)            get test address
000002F0  1255                                     233          LTR   R5,R5                     have a test?
000002F2  4780 846C                      0000066C  234          BZ    ENDTEST                      done?
                                                   235
000002F6                         00000000          236          USING E6TEST,R5
                                                   237
000002F6  4800 5004                      00000004  238          LH    R0,TNUM                save current test number
000002FA  5000 8E04                      00001004  239          ST    R0,TESTING             for easy reference
                                                   240
000002FE  58B0 5000                      00000000  241          L     R11,TSUB               get address of test routine
00000302  05BB                                     242          BALR  R11,R11                do test
                                                   243
00000304  45F0 813C                      0000033C  244          BAL   R15,XCHECK
                                                   245 *
                                                   246 * validate FPC first
                                                   247 *
00000308  D500 500A 5041                 00000041  248          CLC   FLG(1),FPC_R+1          expected FPC flags?
0000030E  4780 8116                      00000316  249          BE    CHECKVXC
00000312  4570 8310                      00000510  250          BAL   R7,FPCMSG               no, issue failed message
                                                   251
                                 00000316  00000001 252 CHECKVXC EQU   *
00000316  D500 500B 5042                 00000042  253          CLC   VXC(1),FPC_R+2          expected VXC?
0000031C  4780 8124                      00000324  254          BE    CHECKRES
00000320  4570 8382                      00000582  255          BAL   R7,VXCMSG               no, issue failed message
                                                   256
                                 00000324  00000001 257 CHECKRES EQU   *
                                                   258
                                                   259 * then validate results, if not inexact
                                                   260
                                                   261 *         XGR   R1,R1
                                                   262 *         IC    R1,FPC_R+1             FPC flags
                                                   263 *         N     R1,=XL4'00000008'      check inexact flag
                                                   264 *         LTR   R1,R1
                                                   265 *         BNZ   DONEXT
                                                   266
00000324  E310 501C 0014                 0000001C  267          LGF   R1,READDR              expected result address
0000032A  D50F 5028 1000         00000028  00000000 268          CLC   V1OUTPUT,0(R1)
00000330  4770 83F4                      000005F4  269          BNE   FAILMSG                no, issue failed message
                                                   270
                                 00000334  00000001 271 DONEXT   EQU   *
00000334  41C0 C004                      00000004  272          LA    R12,4(0,R12)           next test address
00000338  47F0 80EC                      000002EC  273          B     NEXTE6
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    275 *-----------------------------------------------------------------------
                                                    276 * cross check that the result can be converted back to the source
                                                    277 * where there were NO exceptions (DXC/VXC = 0)
                                                    278 *-----------------------------------------------------------------------
                                 0000033C  00000001 279 XCHECK   EQU   *
0000033C  D207 5050 85C0         00000050  000007C0 280          MVC   SKIPXC,=CL8'SKIP XC '
00000342  D500 5007 8600         00000007  00000800 281          CLC   XCSKIP,=CL1'S'          skip xcheck requested
00000348  478F 0000                        00000000 282          BE    0(R15)                  skip = S, so exit
0000034C  9500 5042                        00000042 283          CLI   FPC_R+2,0               Only Xcheck no VXC error
00000350  477F 0000                        00000000 284          BNZ   0(R15)                  some VXC error , so exit
                                                    285 *
                                                    286 *         cross check depends on the instruction
                                                    287 *
00000354  D207 5050 85C8         00000050  000007C8 288          MVC   SKIPXC,=CL8'        '
0000035A  D507 5010 85D0         00000010  000007D0 289          CLC   OPNAME,=CL8'VCNF'
00000360  4780 818C                        0000038C 290          BE    XCVCNF
                                                    291
00000364  D507 5010 85D8         00000010  000007D8 292          CLC   OPNAME,=CL8'VCLFNH'
0000036A  4780 81C0                        000003C0 293          BE    XCVCLFNH
                                                    294
0000036E  D507 5010 85E0         00000010  000007E0 295          CLC   OPNAME,=CL8'VCFN'
00000374  4780 81F4                        000003F4 296          BE    XCVCFN
                                                    297
00000378  D507 5010 85E8         00000010  000007E8 298          CLC   OPNAME,=CL8'VCLFNL'
0000037E  4780 8228                        00000428 299          BE    XCVCLFNL
                                                    300
00000382  D207 5050 85C0         00000050  000007C0 301          MVC   SKIPXC,=CL8'SKIP XC '
00000388  07FF                                      302          BR    R15                     return from xcheck
                                                    303
                                                    304 * cross check: VCNF     - VECTOR FP CONVERT TO NNP
                                                    305 *
0000038C                                            306 XCVCNF   DS    0F
0000038C  B29D 85A4                        000007A4 307          LFPC  FPCMOFF                 initialize FPC
                                                    308
00000390  E700 5028 0806                   00000028 309          VL    V16,V1OUTPUT
00000396  E6F0 0000 145D                            310          VCFN  V15,V16,1,0
0000039C  B29C 5078                        00000078 311          STFPC FPC_XC                  save FPC
000003A0  E7F0 5060 000E                   00000060 312          VST   V15,XCOUTPUT
                                                    313
000003A6  9500 507A                        0000007A 314          CLI   FPC_XC+2,0
000003AA  477F 0000                        00000000 315          BNZ   0(R15)                  some VXC error , so exit
                                                    316
000003AE  E310 500C 0014                   0000000C 317          LGF   R1,V2ADDR               expected source address
000003B4  D50F 5060 1000         00000060  00000000 318          CLC   XCOUTPUT,0(R1)
000003BA  4770 825C                        0000045C 319          BNE   XCFAILMSG
000003BE  07FF                                      320          BR    R15                     return from xcheck
                                                    321
                                                    322 * cross check: VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                    323 *
000003C0                                            324 XCVCLFNH DS    0F
000003C0  B29D 85A4                        000007A4 325          LFPC  FPCMOFF                 initialize FPC
                                                    326
000003C4  E700 5028 0806                   00000028 327          VL    V16,V1OUTPUT
000003CA  E6F0 0002 0675                            328          VCRNF V15,V16,V16,0,2
000003D0  B29C 5078                        00000078 329          STFPC FPC_XC                  save FPC
000003D4  E7F0 5060 000E                   00000060 330          VST   V15,XCOUTPUT
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   331
000003DA  9500 507A                     0000007A   332          CLI   FPC_XC+2,0
000003DE  477F 0000                     00000000   333          BNZ   0(R15)                 some VXC error , so exit
                                                   334
000003E2  E310 500C 0014                0000000C   335          LGF   R1,V2ADDR              expected source address
000003E8  D507 5060 1000                00000000   336          CLC   XCOUTPUT(8),0(R1)
000003EE  4770 825C                     0000045C   337          BNE   XCFAILMSG
000003F2  07FF                                     338          BR    R15                    return from xcheck
                                                   339
                                                   340 * cross check: VCFN     - VECTOR FP CONVERT FROM NNP
                                                   341 *
000003F4                                           342 XCVCFN   DS    0F
000003F4  B29D 85A4                     000007A4   343          LFPC  FPCMOFF                initialize FPC
                                                   344
000003F8  E700 5028 0806                00000028   345          VL    V16,V1OUTPUT
000003FE  E6F0 0001 0455                           346          VCNF  V15,V16,0,1
00000404  B29C 5078                     00000078   347          STFPC FPC_XC                 save FPC
00000408  E7F0 5060 000E                00000060   348          VST   V15,XCOUTPUT
                                                   349
0000040E  9500 507A                     0000007A   350          CLI   FPC_XC+2,0
00000412  477F 0000                     00000000   351          BNZ   0(R15)                 some VXC error , so exit
                                                   352
00000416  E310 500C 0014                0000000C   353          LGF   R1,V2ADDR              expected source address
0000041C  D50F 5060 1000      00000060  00000000   354          CLC   XCOUTPUT,0(R1)
00000422  4770 825C                     0000045C   355          BNE   XCFAILMSG
00000426  07FF                                     356          BR    R15                    return from xcheck
                                                   357
                                                   358 * cross check: VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   359 *
00000428                                           360 XCVCLFNL DS    0F
00000428  B29D 85A4                     000007A4   361          LFPC  FPCMOFF                initialize FPC
                                                   362
0000042C  E700 5028 0806                00000028   363          VL    V16,V1OUTPUT
00000432  E6F0 0002 0675                           364          VCRNF V15,V16,V16,0,2
00000438  B29C 5078                     00000078   365          STFPC FPC_XC                 save FPC
0000043C  E7F0 5060 000E                00000060   366          VST   V15,XCOUTPUT
                                                   367
00000442  9500 507A                     0000007A   368          CLI   FPC_XC+2,0
00000446  477F 0000                     00000000   369          BNZ   0(R15)                 some VXC error , so exit
                                                   370
0000044A  E310 500C 0014                0000000C   371          LGF   R1,V2ADDR              expected source address
00000450  D507 5060 1008                00000008   372          CLC   XCOUTPUT(8),8(R1)      low part of vector
00000456  4770 825C                     0000045C   373          BNE   XCFAILMSG
0000045A  07FF                                     374          BR    R15                    return from xcheck
                                                   375
                                                   376
                                                   377 * xcheck failed message
0000045C                                           378 XCFAILMSG DS   0H
0000045C  4820 5004                     00000004   379          LH    R2,TNUM                get test number and convert
00000460  4E20 8F90                     00001190   380          CVD   R2,DECNUM
00000464  D211 8F7A 8F64      0000117A  00001164   381          MVC   PRT3,EDIT
0000046A  DE11 8F7A 8F90      0000117A  00001190   382          ED    PRT3,DECNUM
00000470  D202 8F23 8F87      00001123  00001187   383          MVC   XCPTNUM(3),PRT3+13     fill in message with test #
                                                   384
00000476  D207 8F45 5010      00001145  00000010   385          MVC   XCPNAME,OPNAME         fill in message with instruction
                                                   386
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000047C  B982 0022                               387          XGR   R2,R2
00000480  4320 5008                     00000008  388          IC    R2,M3                  get m3 and convert
00000484  4E20 8F90                     00001190  389          CVD   R2,DECNUM
00000488  D211 8F7A 8F64      0000117A  00001164  390          MVC   PRT3,EDIT
0000048E  DE11 8F7A 8F90      0000117A  00001190  391          ED    PRT3,DECNUM
00000494  D201 8F56 8F88      00001156  00001188  392          MVC   XCPM3(2),PRT3+14       fill in message with m3 field
                                                  393 *
0000049A  B982 0022                               394          XGR   R2,R2
0000049E  4320 5009                     00000009  395          IC    R2,M4                  get m4 and convert
000004A2  4E20 8F90                     00001190  396          CVD   R2,DECNUM
000004A6  D211 8F7A 8F64      0000117A  00001164  397          MVC   PRT3,EDIT
000004AC  DE11 8F7A 8F90      0000117A  00001190  398          ED    PRT3,DECNUM
000004B2  D201 8F61 8F88      00001161  00001188  399          MVC   XCPM4(2),PRT3+14       fill in message with m4 field
                                                  400
000004B8  50F0 8308                     00000508  401          ST    R15,XCR15              save r15
000004BC  4100 004E                     0000004E  402          LA    R0,XCPLNG              message length
000004C0  4110 8F16                     00001116  403          LA    R1,XCPLINE             message address
000004C4  45F0 847A                     0000067A  404          BAL   R15,RPTERROR
000004C8  58F0 8308                     00000508  405          L     R15,XCR15
                                                  406
000004CC  5800 85F8                     000007F8  407          L     R0,=F'1'               set failed test indicator
000004D0  5000 8E00                     00001000  408          ST    R0,FAILED
000004D4  07FF                                    409          BR    R15                    return from xcheck
                                                  410
000004D8                                          411          DS    0FD
000004D8  00000000 00000000                       412 XCRESULT DS    XL16
000004E8  00000000 00000000                       413 XCV1     DS    XL16
000004F8  00000000 00000000                       414 XCV2     DS    XL16
00000508  00000000 00000000                       415 XCR15    DS    FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   417 ***********************************************************************
                                                   418 * FPC not as expected:
                                                   419 *        issue message with test number, instruction under test,
                                                   420 *              expected FPC and received FPC
                                                   421 ***********************************************************************
                                 00000510  00000001  422 FPCMSG   EQU   *
00000510  5800 85F8                        000007F8  423          L     R0,=F'1'                set failed test indicator
00000514  5000 8E00                        00001000  424          ST    R0,FAILED
                                                   425
00000518  4820 5004                        00000004  426          LH    R2,TNUM                 get test number and convert
0000051C  4E20 8F90                        00001190  427          CVD   R2,DECNUM
00000520  D211 8F7A 8F64      0000117A     00001164  428          MVC   PRT3,EDIT
00000526  DE11 8F7A 8F90      0000117A     00001190  429          ED    PRT3,DECNUM
0000052C  D202 8E15 8F87      00001015     00001187  430          MVC   FPCPNUM(3),PRT3+13      fill in message with test #
                                                   431
00000532  D207 8E39 5010      00001039     00000010  432          MVC   FPCPNAME,OPNAME         fill in message with instruction
                                                   433 *
00000538  B982 0022                                434          XGR   R2,R2
0000053C  4320 500A                        0000000A  435          IC    R2,FLG                  get expected flags and convert
00000540  4E20 8F90                        00001190  436          CVD   R2,DECNUM
00000544  D211 8F7A 8F64      0000117A     00001164  437          MVC   PRT3,EDIT
0000054A  DE11 8F7A 8F90      0000117A     00001190  438          ED    PRT3,DECNUM
00000550  D202 8E52 8F87      00001052     00001187  439          MVC   FPCPEXP(3),PRT3+13      fill in message with m3 field
                                                   440 *
00000556  B982 0022                                441          XGR   R2,R2
0000055A  4320 5041                        00000041  442          IC    R2,FPC_R+1              get received flags and convert
0000055E  4E20 8F90                        00001190  443          CVD   R2,DECNUM
00000562  D211 8F7A 8F64      0000117A     00001164  444          MVC   PRT3,EDIT
00000568  DE11 8F7A 8F90      0000117A     00001190  445          ED    PRT3,DECNUM
0000056E  D202 8E67 8F87      00001067     00001187  446          MVC   FPCPGOT(3),PRT3+13      fill in message with FPC got
                                                   447 *
00000574  4100 0063                        00000063  448          LA    R0,FPCPLNG              message length
00000578  4110 8E08                        00001008  449          LA    R1,FPCPLINE             message address
0000057C  45F0 847A                        0000067A  450          BAL   R15,RPTERROR
00000580  07F7                                     451          BR    R7
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   453 ***********************************************************************
                                                   454 * VXC not as expected:
                                                   455 *        issue message with test number, instruction under test,
                                                   456 *               expected FPC and received FPC
                                                   457 ***********************************************************************
                                 00000582  00000001  458 VXCMSG   EQU   *
00000582  5800 85F8                        000007F8  459          L     R0,=F'1'                set failed test indicator
00000586  5000 8E00                        00001000  460          ST    R0,FAILED
                                                   461
0000058A  4820 5004                        00000004  462          LH    R2,TNUM                 get test number and convert
0000058E  4E20 8F90                        00001190  463          CVD   R2,DECNUM
00000592  D211 8F7A 8F64      0000117A     00001164  464          MVC   PRT3,EDIT
00000598  DE11 8F7A 8F90      0000117A     00001190  465          ED    PRT3,DECNUM
0000059E  D202 8E78 8F87      00001078     00001187  466          MVC   VXCPNUM(3),PRT3+13      fill in message with test #
                                                   467
000005A4  D207 8E9C 5010      0000109C     00000010  468          MVC   VXCPNAME,OPNAME         fill in message with instruction
                                                   469 *
000005AA  B982 0022                                470          XGR   R2,R2
000005AE  4320 500B                        0000000B  471          IC    R2,VXC                  get expected flags and convert
000005B2  4E20 8F90                        00001190  472          CVD   R2,DECNUM
000005B6  D211 8F7A 8F64      0000117A     00001164  473          MVC   PRT3,EDIT
000005BC  DE11 8F7A 8F90      0000117A     00001190  474          ED    PRT3,DECNUM
000005C2  D202 8EB5 8F87      000010B5     00001187  475          MVC   VXCPEXP(3),PRT3+13      fill in message with m3 field
                                                   476 *
000005C8  B982 0022                                477          XGR   R2,R2
000005CC  4320 5042                        00000042  478          IC    R2,FPC_R+2              get received flags and convert
000005D0  4E20 8F90                        00001190  479          CVD   R2,DECNUM
000005D4  D211 8F7A 8F64      0000117A     00001164  480          MVC   PRT3,EDIT
000005DA  DE11 8F7A 8F90      0000117A     00001190  481          ED    PRT3,DECNUM
000005E0  D202 8ECA 8F87      000010CA     00001187  482          MVC   VXCPGOT(3),PRT3+13      fill in message with FPC got
                                                   483 *
000005E6  4100 0063                        00000063  484          LA    R0,VXCPLNG              message length
000005EA  4110 8E6B                        0000106B  485          LA    R1,VXCPLINE             message address
000005EE  45F0 847A                        0000067A  486          BAL   R15,RPTERROR
000005F2  07F7                                     487          BR    R7
                                                   488
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   490 ***********************************************************************
                                                   491 * result not as expected:
                                                   492 *        issue message with test number, instruction under test
                                                   493 *              and instruction m4
                                                   494 ***********************************************************************
                              000005F4  00000001   495 FAILMSG  EQU   *
000005F4  4820 5004                     00000004   496          LH    R2,TNUM                 get test number and convert
000005F8  4E20 8F90                     00001190   497          CVD   R2,DECNUM
000005FC  D211 8F7A 8F64      0000117A  00001164   498          MVC   PRT3,EDIT
00000602  DE11 8F7A 8F90      0000117A  00001190   499          ED    PRT3,DECNUM
00000608  D202 8EDB 8F87      000010DB  00001187   500          MVC   PRTNUM(3),PRT3+13       fill in message with test #
                                                   501
0000060E  D207 8EF6 5010      000010F6  00000010   502          MVC   PRTNAME,OPNAME          fill in message with instruction
                                                   503 *
00000614  B982 0022                                504          XGR   R2,R2
00000618  4320 5008                     00000008   505          IC    R2,M3                   get m3 and convert
0000061C  4E20 8F90                     00001190   506          CVD   R2,DECNUM
00000620  D211 8F7A 8F64      0000117A  00001164   507          MVC   PRT3,EDIT
00000626  DE11 8F7A 8F90      0000117A  00001190   508          ED    PRT3,DECNUM
0000062C  D201 8F07 8F88      00001107  00001188   509          MVC   PRTM3(2),PRT3+14        fill in message with m3 field
                                                   510 *
00000632  B982 0022                                511          XGR   R2,R2
00000636  4320 5009                     00000009   512          IC    R2,M4                   get m4 and convert
0000063A  4E20 8F90                     00001190   513          CVD   R2,DECNUM
0000063E  D211 8F7A 8F64      0000117A  00001164   514          MVC   PRT3,EDIT
00000644  DE11 8F7A 8F90      0000117A  00001190   515          ED    PRT3,DECNUM
0000064A  D201 8F13 8F88      00001113  00001188   516          MVC   PRTM4(2),PRT3+14        fill in message with m4 field
                                                   517 *
00000650  4100 0048                     00000048   518          LA    R0,PRTLNG               message length
00000654  4110 8ECE                     000010CE   519          LA    R1,PRTLINE              message address
00000658  45F0 847A                     0000067A   520          BAL   R15,RPTERROR


                                                   522 ***********************************************************************
                                                   523 * continue after a failed test
                                                   524 ***********************************************************************
                              0000065C  00000001   525 FAILCONT EQU   *
0000065C  5800 85F8                     000007F8   526          L     R0,=F'1'                set failed test indicator
00000660  5000 8E00                     00001000   527          ST    R0,FAILED
                                                   528
00000664  41C0 C004                     00000004   529          LA    R12,4(0,R12)            next test address
00000668  47F0 80EC                     000002EC   530          B     NEXTE6


                                                   532 ***********************************************************************
                                                   533 * end of testing; set ending psw
                                                   534 ***********************************************************************
                              0000066C  00000001   535 ENDTEST  EQU   *
0000066C  5810 8E00                     00001000   536          L     R1,FAILED               did a test fail?
00000670  1211                                     537          LTR   R1,R1
00000672  4780 8580                     00000780   538          BZ    EOJ                      No, exit
00000676  47F0 8598                     00000798   539          B     FAILTEST                 Yes, exit with BAD PSW
                                                   540
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   542 ************************************************************************
                                                   543 *        RPTERROR          Report instruction test in error
                                                   544 *                              R0 = MESSGAE LENGTH
                                                   545 *                              R1 = ADDRESS OF MESSAGE
                                                   546 ************************************************************************

0000067A  50F0 8498                     00000698   548 RPTERROR ST    R15,RPTSAVE            Save return address
0000067E  5050 849C                     0000069C   549          ST    R5,RPTSVR5             Save R5
                                                   550 *
                                                   551 *        Use Hercules Diagnose for Message to console
                                                   552 *
00000682  9002 84A0                     000006A0   553          STM   R0,R2,RPTDWSAV         save regs used by MSG
00000686  4520 84B0                     000006B0   554          BAL   R2,MSG                 call Hercules console MSG display
0000068A  9802 84A0                     000006A0   555          LM    R0,R2,RPTDWSAV         restore regs


0000068E  5850 849C                     0000069C   557          L     R5,RPTSVR5             Restore R5
00000692  58F0 8498                     00000698   558          L     R15,RPTSAVE            Restore return address
00000696  07FF                                     559          BR    R15                    Return to caller

00000698  00000000                                 561 RPTSAVE  DC    F'0'                   R15 save area
0000069C  00000000                                 562 RPTSVR5  DC    F'0'                   R5 save area

000006A0  00000000 00000000                        564 RPTDWSAV DC    2D'0'                  R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   566 ************************************************************************
                                                   567 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                   568 *              R2 = return address
                                                   569 ************************************************************************

000006B0  4900 85FC                    000007FC    571 MSG      CH    R0,=H'0'                Do we even HAVE a message?
000006B4  07D2                                     572          BNHR  R2                      No, ignore

000006B6  9002 84EC                    000006EC    574          STM   R0,R2,MSGSAVE           Save registers

000006BA  4900 85FE                    000007FE    576          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
000006BE  47D0 84C6                    000006C6    577          BNH   MSGOK                   Yes, continue
000006C2  4100 0064                    00000064    578          LA    R0,L'MSGMSG             No, set to maximum

000006C6  1820                                     580 MSGOK    LR    R2,R0                   Copy length to work register
000006C8  0620                                     581          BCTR  R2,0                    Minus-1 for execute
000006CA  4420 84F8                    000006F8    582          EX    R2,MSGMVC               Copy message to O/P buffer

000006CE  4120 200A                    0000000A    584          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
000006D2  4110 84FE                    000006FE    585          LA    R1,MSGCMD               Point to true command

000006D6  83120008                                 587          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
000006DA  4780 84E6                    000006E6    588          BZ    MSGRET                  Return if successful
                                                   589
000006DE  1222                                     590          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
000006E0  4780 84E6                    000006E6    591          BZ    MSGRET                    an error occurred but coninue
                                                   592
000006E4  0000                                     593          DC    H'0'                    CRASH for debugging purposes

000006E6  9802 84EC                    000006EC    595 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
000006EA  07F2                                     596          BR    R2                      Return to caller


000006EC  00000000 00000000                        598 MSGSAVE  DC    3F'0'                   Registers save area
000006F8  D200 8507 1000      00000707  00000000   599 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

000006FE  D4E2C7D5 D6C8405C                        601 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
00000707  40404040 40404040                        602 MSGMSG   DC    CL100' '                The message text to be displayed
                                                   603
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    605 ************************************************************************
                                                    606 *        Normal completion or Abnormal termination PSWs
                                                    607 ************************************************************************


00000770  00020001 80000000                         609 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000780  B2B2 8570                       00000770  611 EOJ      LPSWE EOJPSW               Normal completion


00000788  00020001 80000000                         613 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000798  B2B2 8588                       00000788  615 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                    617 ************************************************************************
                                                    618 *        Working Storage
                                                    619 ************************************************************************


0000079C  00000000                                  621 CTLR0    DS    F                     CR0
000007A0  00000000                                  622          DS    F
000007A4  00000000                                  623 FPCMOFF  DC    XL4'00000000'         FPC masks off
000007A8  F8000000                                  624 FPCMON   DC    XL4'F8000000'         FPC masks on
000007AC  80000000                                  625 FPCMIO   DC    XL4'80000000'         FPC mask invalid operation
000007B0  20000000                                  626 FPCMOV   DC    XL4'20000000'         FPC mask overflow
000007B4  10000000                                  627 FPCMUN   DC    XL4'10000000'         FPC mask underflow
000007B8  08000000                                  628 FPCMIE   DC    XL4'08000000'         FPC mask inexact


                                                    630
000007C0                                            631          LTORG ,                 Literals pool
000007C0  E2D2C9D7 40E7C340                         632                =CL8'SKIP XC '
000007C8  40404040 40404040                         633                =CL8'        '
000007D0  E5C3D5C6 40404040                         634                =CL8'VCNF'
000007D8  E5C3D3C6 D5C84040                         635                =CL8'VCLFNH'
000007E0  E5C3C6D5 40404040                         636                =CL8'VCFN'
000007E8  E5C3D3C6 D5D34040                         637                =CL8'VCLFNL'
000007F0  00000004                                  638                =F'4'
000007F4  0000548C                                  639                =A(E6TESTS)
000007F8  00000001                                  640                =F'1'
000007FC  0000                                      641                =H'0'
000007FE  0064                                      642                =AL2(L'MSGMSG)
00000800  E2                                        643                =CL1'S'
                                                    644
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          645 *        some constants
                                          646
                              00000400  00000001   647 K        EQU   1024             One KB
                              00001000  00000001   648 PAGE     EQU   (4*K)            Size of one page
                              00010000  00000001   649 K64      EQU   (64*K)           64 KB
                              00100000  00000001   650 MB       EQU   (K*K)             1 MB
                                                   651
                                                   652
                              AABBCCDD  00000001   653 REG2PATT EQU   X'AABBCCDD'    Polluted Register pattern
                              000000DD  00000001   654 REG2LOW  EQU         X'DD'    (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    656 *=====================================================================
                                                    657 *
                                                    658 *  NOTE: start data on an address that is easy to display
                                                    659 *        within Hercules
                                                    660 *
                                                    661 *=====================================================================
                                                    662
00000801                      00000801  00001000    663          ORG   ZVE6TST+X'1000'
00001000  00000000                                  664 FAILED   DC    F'0'                    some test failed?
00001004  00000000                                  665 TESTING  DC    F'0'                    current test #


                                                    667
                                                    668 ************************************************************************
                                                    669 *        TEST failed : FPC message
                                                    670 ************************************************************************
                                                    671 *
                                                    672 *        failed message and associated editting
                                                    673 *
00001008  40404040 4040E385                         674 FPCPLINE DC    C'      Test # '
00001015  A7A7A7                                    675 FPCPNUM  DC    C'xxx'
00001018  40A69996 958740C6                         676          DC    c' wrong FPC flags for instruction '
00001039  A7A7A7A7 A7A7A7A7                         677 FPCPNAME DC    CL8'xxxxxxxx'
00001041  4085A797 8583A385                         678          DC    C' expected: flags='
00001052  A7A7A7                                    679 FPCPEXP  DC    C'xxx'
00001055  6B                                        680          DC    C','
00001056  40998583 8589A585                         681          DC    C' received: flags='
00001067  A7A7A7                                    682 FPCPGOT  DC    C'xxx'
0000106A  4B                                        683          DC    C'.'
                              00000063  00000001    684 FPCPLNG  EQU   *-FPCPLINE


                                                    686
                                                    687 ************************************************************************
                                                    688 *        TEST failed : VXC message
                                                    689 ************************************************************************
                                                    690 *
                                                    691 *        failed message and associated editting
                                                    692 *
0000106B  40404040 4040E385                         693 VXCPLINE DC    C'      Test # '
00001078  A7A7A7                                    694 VXCPNUM  DC    C'xxx'
0000107B  40A69996 958740C6                         695          DC    c' wrong FPC VXC   for instruction '
0000109C  A7A7A7A7 A7A7A7A7                         696 VXCPNAME DC    CL8'xxxxxxxx'
000010A4  4085A797 8583A385                         697          DC    C' expected:   VXC='
000010B5  A7A7A7                                    698 VXCPEXP  DC    C'xxx'
000010B8  6B                                        699          DC    C','
000010B9  40998583 8589A585                         700          DC    C' received:   VXC='
000010CA  A7A7A7                                    701 VXCPGOT  DC    C'xxx'
000010CD  4B                                        702          DC    C'.'
                              00000063  00000001    703 VXCPLNG  EQU   *-VXCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    705 ***********************************************************************
                                                    706 *        TEST failed : result messgae
                                                    707 ***********************************************************************
                                                    708 *
                                                    709 *        failed message and associated editting
                                                    710 *
000010CE  40404040 4040E385                         711 PRTLINE  DC    C'      Test # '
000010DB  A7A7A7                                    712 PRTNUM   DC    C'xxx'
000010DE  40868189 93858440                         713          DC    c' failed for instruction '
000010F6  A7A7A7A7 A7A7A7A7                         714 PRTNAME  DC    CL8'xxxxxxxx'
000010FE  40A689A3 884094F3                         715          DC    C' with m3='
00001107  A7A7                                      716 PRTM3    DC    C'xx'
00001109  6B                                        717          DC    C','
0000110A  40A689A3 884094F4                         718          DC    C' with m4='
00001113  A7A7                                      719 PRTM4    DC    C'xx'
00001115  4B                                        720          DC    C'.'
                            00000048  00000001      721 PRTLNG   EQU   *-PRTLINE


                                                    723 ***********************************************************************
                                                    724 *        TEST failed : XCHECK
                                                    725 ***********************************************************************
                                                    726 *
                                                    727 *        XCHECK failed message
                                                    728 *
00001116  40404040 4040E385                         729 XCPLINE  DC    C'      Test # '
00001123  A7A7A7                                    730 XCPTNUM  DC    C'xxx'
00001126  40E7C3C8 C5C3D240                         731          DC    c' XCHECK failed for instruction '
00001145  A7A7A7A7 A7A7A7A7                         732 XCPNAME  DC    CL8'xxxxxxxx'
0000114D  40A689A3 884094F3                         733          DC    C' with m3='
00001156  A7A7                                      734 XCPM3    DC    C'xx'
00001158  40A689A3 884094F4                         735          DC    C' with m4='
00001161  A7A7                                      736 XCPM4    DC    C'xx'
00001163  4B                                        737          DC    C'.'
                            0000004E  00000001      738 XCPLNG   EQU   *-XCPLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    740 ***********************************************************************
                                                    741 *        TEST failed : message working storge
                                                    742 ***********************************************************************
00001164  40212020 20202020                         743 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                    744
00001176  7E7E7E6E                                  745          DC    C'===>'
0000117A  40404040 40404040                         746 PRT3     DC    CL18' '
0000118C  4C7E7E7E                                  747          DC    C'<===='
00001190  00000000 00000000                         748 DECNUM   DS    CL16


                                                    750 *
                                                    751 *        Vector instruction results, pollution and input
                                                    752 *
000011A0  00000000 00000000                         753          DS    XL16                                          gap
000011B0  FFFFFFFF FFFFFFFF                         754 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000011C0  12345678 90123456                         755 V1INPUT  DC    XL16'12345678901234567890123456789 01D'    V1 input
000011D0  00000000 00000000                         756          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    758 ************************************************************************
                                                    759 *        E6TEST DSECT
                                                    760 ************************************************************************


                                                    762 E6TEST   DSECT ,
00000000  00000000                                  763 TSUB     DC    A(0)              pointer  to test
00000004  0000                                      764 TNUM     DC    H'00'             Test Number
00000006  00                                        765          DC    X'00'
00000007  40                                        766 XCSKIP   DC    CL1' '            Y = skip cross check
00000008  00                                        767 M3       DC    HL1'00'           m3 used
00000009  00                                        768 M4       DC    HL1'00'           m4 used
0000000A  00                                        769 FLG      DC    X'00'             expected FPC flags
0000000B  00                                        770 VXC      DC    X'00'             VXC expected
0000000C  00000000                                  771 V2ADDR   DC    A(0)              address of v2: 16-byte packed decimal
00000010  40404040 40404040                         772 OPNAME   DC    CL8' '            E6 name
00000018  00000000                                  773 RELEN    DC    A(0)              result length
0000001C  00000000                                  774 READDR   DC    A(0)              expected result address
00000020  00000000 00000000                         775          DS    FD                   gap
00000028  00000000 00000000                         776 V1OUTPUT DS    XL16              V1 Output
00000038  00000000 00000000                         777          DS    FD                   gap
00000040  00000000                                  778 FPC_R    DS    F                 FPC after instruction
00000048  00000000 00000000                         779          DS    FD                   gap
00000050  40404040 40404040                         780 SKIPXC   DC    CL8' '            was cross check skipped?
00000058  00000000 00000000                         781          DS    FD                   gap
00000060  00000000 00000000                         782 XCOUTPUT DS    XL16              Cross check Output
00000070  00000000 00000000                         783          DS    FD                   gap
00000078  00000000                                  784 FPC_XC   DS    F                 FPC after cross check
00000080  00000000 00000000                         785          DS    FD                   gap
00000088  00000000                                  786 WK1      DS    F                 debug area
0000008C  00000000                                  787 WK2      DS    F
00000090                                            788          DS    0F
                                                    789 **
                                                    790 *        test routine will be here (from VRR-a macro)


                             00000000  000055D7    792 ZVE6TST  CSECT ,
000011E0                                            793          DS    0F


                                                    795 ************************************************************************
                                                    796 *     Macros to help build test tables
                                                    797 ************************************************************************


                                                    799 *
                                                    800 * macro to generate individual test
                                                    801 *
                                                    802          MACRO
                                                    803          VRR_A &INST,&M3,&M4,&FLAGS,&VXC,&SKIP
                                                    804 .*                              &INST  - VRR-a instruction under test
                                                    805 .*                              &m3    - m3 field
                                                    806 .*                              &m4    - m4 field
                                                    807 .*                              &flags - expected FPC flags (HEX)
                                                    808 .*                              &VXC   - expected VXC (HEX)
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                  .*                                &SKIP  - S = skip cross check
                                                           GBLA  &TNUM
                                                  &TNUM    SETA  &TNUM+1

                                                           DS    0FD
                                                           USING *,R5              base for test data and test routine

                                                  T&TNUM   DC    A(X&TNUM)         address of test routine
                                                           DC    H'&TNUM'          test number
                                                           DC    X'00'
                                                           DC    CL1'&SKIP'        Y = skip cross check
                                                           DC    HL1'&M3'          m3
                                                           DC    HL1'&M4'          m4
                                                  FLG&TNUM DC    X'&FLAGS'         expected FPC flags
                                                  VXC&TNUM DC    X'&VXC'           expected VXC
                                                  V2_&TNUM DC    A(RE&TNUM+16)     address of v2: 16-byte packed decimal
                                                           DC    CL8'&INST'        instruction name
                                                           DC    A(16)             result length
                                                           DC    A(RE&TNUM)        address of expected resul
                                                           DS    FD                gap
                                                  V1O&TNUM DS    XL16              V1 output
                                                           DS    FD                   gap
                                                  FPC_R_&TNUM DS F                 FPC after instruction
                                                           DS    FD                   gap
                                                           DC    CL8' '            was cross check skipped?
                                                           DS    FD                   gap
                                                  XCO&TNUM DS    XL16              Cross check Output
                                                           DS    FD                   gap
                                                  FPC_XC_&TNUM DS F                FPC after cross check
                                                           DS    FD                   gap
                                                           DS    F                 debug area
                                                           DS    F
                                                  .*
                                                  *
                                                  X&TNUM   DS    0F
                                                           LFPC  FPCMOFF           initialize FPC

                                                           LGF   R2,V2_&TNUM       get v2
                                                           VL    V22,0(R2)

                                                           &INST V22,V22,&M3,&M4   test instruction (dest is source)

                                                           STFPC FPC_R_&TNUM       save FPC
                                                           VST   V22,V1O&TNUM      save instruction result

                                                           BR    R11               return

                                                  RE&TNUM  DS    0F                expected 16 byte result
                                                           DROP  R5

                                                           MEND


                                                  *
                                                  * macro to generate table of pointers to individual tests
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   863 *
                                                   864          MACRO
                                                   865          PTTABLE
                                                   866          GBLA  &TNUM
                                                   867          LCLA  &CUR
                                                   868 &CUR     SETA  1
                                                   869 .*
                                                   870 TTABLE   DS    0F
                                                   871 .LOOP    ANOP
                                                   872 .*
                                                   873          DC    A(T&CUR)          TEST &CUR
                                                   874 .*
                                                   875 &CUR     SETA  &CUR+1
                                                   876          AIF   (&CUR LE &TNUM).LOOP
                                                   877 *
                                                   878          DC    A(0)              END OF TABLE
                                                   879          DC    A(0)
                                                   880 .*
                                                   881          MEND
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   883 ************************************************************************
                                                   884 *        E6 VRR-a tests
                                                   885 ************************************************************************
                                                   886         PRINT DATA
                                                   887 *
                                                   888 *        E655 VCNF     - VECTOR FP CONVERT TO NNP
                                                   889 *        E656 VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   890 *        E65D VCFN     - VECTOR FP CONVERT FROM NNP
                                                   891 *        E65E VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   892 *
                                                   893 *-----------------------------------------------------------------------
                                                   894 *   VRR-a   instruction, m3, m4, flags, VXC, SKIP
                                                   895 *   followed by
                                                   896 *              followed by
                                                   897 *              v1 - 16 byte expected result
                                                   898 *              v2 - 16 byte source
                                                   899 *
                                                   900 * note: VXC should always by 00 as the FPC mask is zero
                                                   901 *-----------------------------------------------------------------------
                                                   902 * VCNF     - VECTOR FP CONVERT TO NNP
                                                   903 *-----------------------------------------------------------------------
                                                   904 * tinyb -> dlfloat  (with cross check dlfloat -> tinyb)
                                                   905 *
                                                   906 * some of these tests use numbers from PoP SA22-7832-13,
                                                   907 * Figure 9-2. Examples of Floating-Point Numbers ( page 9-6 )
                                                   908 *
                                                   909 * +0     simple instruction test and 'test' test
                                                   910          VRR_A VCNF,0,1,00,00,N
000011E0                                           911+         DS    0FD
000011E0                       000011E0            912+         USING *,R5              base for test data and test routine
000011E0  00001270                                 913+T1       DC    A(X1)             address of test routine
000011E4  0001                                     914+         DC    H'1'              test number
000011E6  00                                       915+         DC    X'00'
000011E7  D5                                       916+         DC    CL1'N'            Y = skip cross check
000011E8  00                                       917+         DC    HL1'0'            m3
000011E9  01                                       918+         DC    HL1'1'            m4
000011EA  00                                       919+FLG1     DC    X'00'             expected FPC flags
000011EB  00                                       920+VXC1     DC    X'00'             expected VXC
000011EC  000012A4                                 921+V2_1     DC    A(RE1+16)         address of v2: 16-byte packed decimal
000011F0  E5C3D5C6 40404040                        922+         DC    CL8'VCNF'         instruction name
000011F8  00000010                                 923+         DC    A(16)             result length
000011FC  00001294                                 924+         DC    A(RE1)            address of expected resul
00001200  00000000 00000000                        925+         DS    FD                gap
00001208  00000000 00000000                        926+V1O1     DS    XL16              V1 output
00001210  00000000 00000000
00001218  00000000 00000000                        927+         DS    FD                   gap
00001220  00000000                                 928+FPC_R_1  DS    F                 FPC after instruction
00001228  00000000 00000000                        929+         DS    FD                   gap
00001230  40404040 40404040                        930+         DC    CL8' '            was cross check skipped?
00001238  00000000 00000000                        931+         DS    FD                   gap
00001240  00000000 00000000                        932+XCO1     DS    XL16              Cross check Output
00001248  00000000 00000000
00001250  00000000 00000000                        933+         DS    FD                   gap
00001258  00000000                                 934+FPC_XC_1 DS    F                 FPC after cross check
00001260  00000000 00000000                        935+         DS    FD                   gap
00001268  00000000                                 936+         DS    F                 debug area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000126C  00000000                                937+         DS    F
                                                  938+*
00001270                                          939+X1       DS    0F
00001270  B29D 85A4                     000007A4  940+         LFPC  FPCMOFF           initialize FPC
00001274  E320 500C 0014                000011EC  941+         LGF   R2,V2_1           get v2
0000127A  E762 0000 0806                00000000  942+         VL    V22,0(R2)
00001280  E666 0001 0C55                          943+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001286  B29C 9020                     00001220  944+         STFPC FPC_R_1           save FPC
0000128A  E760 9008 080E                00001208  945+         VST   V22,V1O1          save instruction result
00001290  07FB                                    946+         BR    R11               return
00001294                                          947+RE1      DS    0F                expected 16 byte result
00001294                                          948+         DROP  R5
00001294  00000000 00000000                       949          DC    XL16'00000000000000000000000000000000'
0000129C  00000000 00000000
000012A4  00000000 00000000                       950          DC    XL16'00000000000000000000000000000000'
000012AC  00000000 00000000
                                                  951
                                                  952 * 1.0, -1, .... -4096
                                                  953          VRR_A VCNF,0,1,00,00,N
000012B8                                          954+         DS    0FD
000012B8                        000012B8          955+         USING *,R5              base for test data and test routine
000012B8  00001348                                956+T2       DC    A(X2)             address of test routine
000012BC  0002                                    957+         DC    H'2'              test number
000012BE  00                                      958+         DC    X'00'
000012BF  D5                                      959+         DC    CL1'N'            Y = skip cross check
000012C0  00                                      960+         DC    HL1'0'            m3
000012C1  01                                      961+         DC    HL1'1'            m4
000012C2  00                                      962+FLG2     DC    X'00'             expected FPC flags
000012C3  00                                      963+VXC2     DC    X'00'             expected VXC
000012C4  0000137C                                964+V2_2     DC    A(RE2+16)         address of v2: 16-byte packed decimal
000012C8  E5C3D5C6 40404040                       965+         DC    CL8'VCNF'         instruction name
000012D0  00000010                                966+         DC    A(16)             result length
000012D4  0000136C                                967+         DC    A(RE2)            address of expected resul
000012D8  00000000 00000000                       968+         DS    FD                gap
000012E0  00000000 00000000                       969+V1O2     DS    XL16              V1 output
000012E8  00000000 00000000
000012F0  00000000 00000000                       970+         DS    FD                   gap
000012F8  00000000                                971+FPC_R_2  DS    F                 FPC after instruction
00001300  00000000 00000000                       972+         DS    FD                   gap
00001308  40404040 40404040                       973+         DC    CL8' '            was cross check skipped?
00001310  00000000 00000000                       974+         DS    FD                   gap
00001318  00000000 00000000                       975+XCO2     DS    XL16              Cross check Output
00001320  00000000 00000000
00001328  00000000 00000000                       976+         DS    FD                   gap
00001330  00000000                                977+FPC_XC_2 DS    F                 FPC after cross check
00001338  00000000 00000000                       978+         DS    FD                   gap
00001340  00000000                                979+         DS    F                 debug area
00001344  00000000                                980+         DS    F
                                                  981+*
00001348                                          982+X2       DS    0F
00001348  B29D 85A4                     000007A4  983+         LFPC  FPCMOFF           initialize FPC
0000134C  E320 500C 0014                000012C4  984+         LGF   R2,V2_2           get v2
00001352  E762 0000 0806                00000000  985+         VL    V22,0(R2)
00001358  E666 0001 0C55                          986+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000135E  B29C 5040                     000012F8  987+         STFPC FPC_R_2           save FPC
00001362  E760 5028 080E                000012E0  988+         VST   V22,V1O2          save instruction result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001368  07FB                                      989+         BR    R11                 return
0000136C                                            990+RE2      DS    0F                  expected 16 byte result
0000136C                                            991+         DROP  R5
0000136C  3E000000 BE000000                         992          DC    XL16'3E000000BE000000000000000000D800'
00001374  00000000 0000D800
0000137C  3C000000 BC000000                         993          DC    XL16'3C000000BC000000000000000000F000'
00001384  00000000 0000F000
                                                    994 * 0.5
                                                    995          VRR_A VCNF,0,1,00,00,N
00001390                                            996+         DS    0FD
00001390                      00001390              997+         USING *,R5                base for test data and test routine
00001390  00001420                                  998+T3       DC    A(X3)               address of test routine
00001394  0003                                      999+         DC    H'3'                test number
00001396  00                                       1000+         DC    X'00'
00001397  D5                                       1001+         DC    CL1'N'              Y = skip cross check
00001398  00                                       1002+         DC    HL1'0'              m3
00001399  01                                       1003+         DC    HL1'1'              m4
0000139A  00                                       1004+FLG3     DC    X'00'               expected FPC flags
0000139B  00                                       1005+VXC3     DC    X'00'               expected VXC
0000139C  00001454                                 1006+V2_3     DC    A(RE3+16)           address of v2: 16-byte packed decimal
000013A0  E5C3D5C6 40404040                        1007+         DC    CL8'VCNF'           instruction name
000013A8  00000010                                 1008+         DC    A(16)               result length
000013AC  00001444                                 1009+         DC    A(RE3)              address of expected resul
000013B0  00000000 00000000                        1010+         DS    FD                  gap
000013B8  00000000 00000000                        1011+V1O3     DS    XL16                V1 output
000013C0  00000000 00000000
000013C8  00000000 00000000                        1012+         DS    FD                     gap
000013D0  00000000                                 1013+FPC_R_3  DS    F                   FPC after instruction
000013D8  00000000 00000000                        1014+         DS    FD                     gap
000013E0  40404040 40404040                        1015+         DC    CL8' '              was cross check skipped?
000013E8  00000000 00000000                        1016+         DS    FD                     gap
000013F0  00000000 00000000                        1017+XCO3     DS    XL16                Cross check Output
000013F8  00000000 00000000
00001400  00000000 00000000                        1018+         DS    FD                     gap
00001408  00000000                                 1019+FPC_XC_3 DS    F                   FPC after cross check
00001410  00000000 00000000                        1020+         DS    FD                     gap
00001418  00000000                                 1021+         DS    F                   debug area
0000141C  00000000                                 1022+         DS    F
                                                   1023+*
00001420                                           1024+X3       DS    0F
00001420  B29D 85A4                    000007A4    1025+         LFPC  FPCMOFF             initialize FPC
00001424  E320 500C 0014               0000139C    1026+         LGF   R2,V2_3             get v2
0000142A  E762 0000 0806               00000000    1027+         VL    V22,0(R2)
00001430  E666 0001 0C55                           1028+         VCNF  V22,V22,0,1         test instruction (dest is source)
00001436  B29C 5040                    000013D0    1029+         STFPC FPC_R_3             save FPC
0000143A  E760 5028 080E               000013B8    1030+         VST   V22,V1O3            save instruction result
00001440  07FB                                     1031+         BR    R11                 return
00001444                                           1032+RE3      DS    0F                  expected 16 byte result
00001444                                           1033+         DROP  R5
00001444  3C000000 00000000                        1034          DC    XL16'3C000000000000000000000000D800'
0000144C  00000000 0000D800
00001454  38000000 00000000                        1035          DC    XL16'380000000000000000000000000F000'
0000145C  00000000 0000F000
                                                   1036
                                                   1037 * 1/64
                                                   1038          VRR_A VCNF,0,1,00,00,N
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001468                                           1039+         DS    0FD
00001468                     00001468              1040+         USING *,R5              base for test data and test routine
00001468  000014F8                                 1041+T4       DC    A(X4)             address of test routine
0000146C  0004                                     1042+         DC    H'4'              test number
0000146E  00                                       1043+         DC    X'00'
0000146F  D5                                       1044+         DC    CL1'N'            Y = skip cross check
00001470  00                                       1045+         DC    HL1'0'            m3
00001471  01                                       1046+         DC    HL1'1'            m4
00001472  00                                       1047+FLG4     DC    X'00'             expected FPC flags
00001473  00                                       1048+VXC4     DC    X'00'             expected VXC
00001474  0000152C                                 1049+V2_4     DC    A(RE4+16)         address of v2: 16-byte packed decimal
00001478  E5C3D5C6 40404040                        1050+         DC    CL8'VCNF'         instruction name
00001480  00000010                                 1051+         DC    A(16)             result length
00001484  0000151C                                 1052+         DC    A(RE4)            address of expected resul
00001488  00000000 00000000                        1053+         DS    FD                gap
00001490  00000000 00000000                        1054+V1O4     DS    XL16              V1 output
00001498  00000000 00000000
000014A0  00000000 00000000                        1055+         DS    FD                   gap
000014A8  00000000                                 1056+FPC_R_4  DS    F                 FPC after instruction
000014B0  00000000 00000000                        1057+         DS    FD                   gap
000014B8  40404040 40404040                        1058+         DC    CL8' '            was cross check skipped?
000014C0  00000000 00000000                        1059+         DS    FD                   gap
000014C8  00000000 00000000                        1060+XCO4     DS    XL16              Cross check Output
000014D0  00000000 00000000
000014D8  00000000 00000000                        1061+         DS    FD                   gap
000014E0  00000000                                 1062+FPC_XC_4 DS    F                 FPC after cross check
000014E8  00000000 00000000                        1063+         DS    FD                   gap
000014F0  00000000                                 1064+         DS    F                 debug area
000014F4  00000000                                 1065+         DS    F
                                                   1066+*
000014F8                                           1067+X4       DS    0F
000014F8  B29D 85A4                    000007A4    1068+         LFPC  FPCMOFF           initialize FPC
000014FC  E320 500C 0014               00001474    1069+         LGF   R2,V2_4           get v2
00001502  E762 0000 0806               00000000    1070+         VL    V22,0(R2)
00001508  E666 0001 0C55                           1071+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000150E  B29C 5040                    000014A8    1072+         STFPC FPC_R_4           save FPC
00001512  E760 5028 080E               00001490    1073+         VST   V22,V1O4          save instruction result
00001518  07FB                                     1074+         BR    R11               return
0000151C                                           1075+RE4      DS    0F                expected 16 byte result
0000151C                                           1076+         DROP  R5
0000151C  32000000 00000000                        1077          DC    XL16'32000000000000000000000000D800'
00001524  00000000 0000D800
0000152C  24000000 00000000                        1078          DC    XL16'24000000000000000000000000F000'
00001534  00000000 0000F000
                                                   1079
                                                   1080 * +0, -0
                                                   1081          VRR_A VCNF,0,1,00,00,N
00001540                                           1082+         DS    0FD
00001540                     00001540              1083+         USING *,R5              base for test data and test routine
00001540  000015D0                                 1084+T5       DC    A(X5)             address of test routine
00001544  0005                                     1085+         DC    H'5'              test number
00001546  00                                       1086+         DC    X'00'
00001547  D5                                       1087+         DC    CL1'N'            Y = skip cross check
00001548  00                                       1088+         DC    HL1'0'            m3
00001549  01                                       1089+         DC    HL1'1'            m4
0000154A  00                                       1090+FLG5     DC    X'00'             expected FPC flags
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000154B  00                                       1091+VXC5     DC    X'00'              expected VXC
0000154C  00001604                                 1092+V2_5     DC    A(RE5+16)          address of v2: 16-byte packed decimal
00001550  E5C3D5C6 40404040                        1093+         DC    CL8'VCNF'          instruction name
00001558  00000010                                 1094+         DC    A(16)              result length
0000155C  000015F4                                 1095+         DC    A(RE5)             address of expected resul
00001560  00000000 00000000                        1096+         DS    FD                 gap
00001568  00000000 00000000                        1097+V1O5     DS    XL16               V1 output
00001570  00000000 00000000
00001578  00000000 00000000                        1098+         DS    FD                    gap
00001580  00000000                                 1099+FPC_R_5  DS    F                  FPC after instruction
00001588  00000000 00000000                        1100+         DS    FD                    gap
00001590  40404040 40404040                        1101+         DC    CL8' '             was cross check skipped?
00001598  00000000 00000000                        1102+         DS    FD                    gap
000015A0  00000000 00000000                        1103+XCO5     DS    XL16               Cross check Output
000015A8  00000000 00000000
000015B0  00000000 00000000                        1104+         DS    FD                    gap
000015B8  00000000                                 1105+FPC_XC_5 DS    F                  FPC after cross check
000015C0  00000000 00000000                        1106+         DS    FD                    gap
000015C8  00000000                                 1107+         DS    F                  debug area
000015CC  00000000                                 1108+         DS    F
                                                   1109+*
000015D0                                           1110+X5       DS    0F
000015D0  B29D 85A4                     000007A4   1111+         LFPC  FPCMOFF            initialize FPC
000015D4  E320 500C 0014                0000154C   1112+         LGF   R2,V2_5            get v2
000015DA  E762 0000 0806                00000000   1113+         VL    V22,0(R2)
000015E0  E666 0001 0C55                           1114+         VCNF  V22,V22,0,1        test instruction (dest is source)
000015E6  B29C 5040                     00001580   1115+         STFPC FPC_R_5            save FPC
000015EA  E760 5028 080E                00001568   1116+         VST   V22,V1O5           save instruction result
000015F0  07FB                                     1117+         BR    R11                return
000015F4                                           1118+RE5      DS    0F                 expected 16 byte result
000015F4                                           1119+         DROP  R5
000015F4  00008000 00000000                        1120          DC    XL16'00008000000000000000000000000D800'
000015FC  00000000 0000D800
00001604  00008000 00000000                        1121          DC    XL16'00008000000000000000000000000F000'
0000160C  00000000 0000F000
                                                   1122
                                                   1123 * -15
                                                   1124          VRR_A VCNF,0,1,00,00,N
00001618                                           1125+         DS    0FD
00001618                        00001618           1126+         USING *,R5               base for test data and test routine
00001618  000016A8                                 1127+T6       DC    A(X6)              address of test routine
0000161C  0006                                     1128+         DC    H'6'               test number
0000161E  00                                       1129+         DC    X'00'
0000161F  D5                                       1130+         DC    CL1'N'             Y = skip cross check
00001620  00                                       1131+         DC    HL1'0'             m3
00001621  01                                       1132+         DC    HL1'1'             m4
00001622  00                                       1133+FLG6     DC    X'00'              expected FPC flags
00001623  00                                       1134+VXC6     DC    X'00'              expected VXC
00001624  000016DC                                 1135+V2_6     DC    A(RE6+16)          address of v2: 16-byte packed decimal
00001628  E5C3D5C6 40404040                        1136+         DC    CL8'VCNF'          instruction name
00001630  00000010                                 1137+         DC    A(16)              result length
00001634  000016CC                                 1138+         DC    A(RE6)             address of expected resul
00001638  00000000 00000000                        1139+         DS    FD                 gap
00001640  00000000 00000000                        1140+V1O6     DS    XL16               V1 output
00001648  00000000 00000000
00001650  00000000 00000000                        1141+         DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001658  00000000                                 1142+FPC_R_6  DS    F                 FPC after instruction
00001660  00000000 00000000                        1143+         DS    FD                   gap
00001668  40404040 40404040                        1144+         DC    CL8' '            was cross check skipped?
00001670  00000000 00000000                        1145+         DS    FD                   gap
00001678  00000000 00000000                        1146+XCO6     DS    XL16              Cross check Output
00001680  00000000 00000000
00001688  00000000 00000000                        1147+         DS    FD                   gap
00001690  00000000                                 1148+FPC_XC_6 DS    F                 FPC after cross check
00001698  00000000 00000000                        1149+         DS    FD                   gap
000016A0  00000000                                 1150+         DS    F                 debug area
000016A4  00000000                                 1151+         DS    F
                                                   1152+*
000016A8                                           1153+X6       DS    0F
000016A8  B29D 85A4                     000007A4   1154+         LFPC  FPCMOFF           initialize FPC
000016AC  E320 500C 0014                00001624   1155+         LGF   R2,V2_6           get v2
000016B2  E762 0000 0806                00000000   1156+         VL    V22,0(R2)
000016B8  E666 0001 0C55                           1157+         VCNF  V22,V22,0,1       test instruction (dest is source)
000016BE  B29C 5040                     00001658   1158+         STFPC FPC_R_6           save FPC
000016C2  E760 5028 080E                00001640   1159+         VST   V22,V1O6          save instruction result
000016C8  07FB                                     1160+         BR    R11               return
000016CC                                           1161+RE6      DS    0F                expected 16 byte result
000016CC                                           1162+         DROP  R5
000016CC  C5C00000 00000000                        1163          DC    XL16'C5C0000000000000000000000D800'
000016D4  00000000 0000D800
000016DC  CB800000 00000000                        1164          DC    XL16'CB800000000000000000000000F000'
000016E4  00000000 0000F000
                                                   1165
                                                   1166 * 20/7 (about)
                                                   1167          VRR_A VCNF,0,1,00,00,N
000016F0                                           1168+         DS    0FD
000016F0                        000016F0           1169+         USING *,R5              base for test data and test routine
000016F0  00001780                                 1170+T7       DC    A(X7)             address of test routine
000016F4  0007                                     1171+         DC    H'7'              test number
000016F6  00                                       1172+         DC    X'00'
000016F7  D5                                       1173+         DC    CL1'N'            Y = skip cross check
000016F8  00                                       1174+         DC    HL1'0'            m3
000016F9  01                                       1175+         DC    HL1'1'            m4
000016FA  00                                       1176+FLG7     DC    X'00'             expected FPC flags
000016FB  00                                       1177+VXC7     DC    X'00'             expected VXC
000016FC  000017B4                                 1178+V2_7     DC    A(RE7+16)         address of v2: 16-byte packed decimal
00001700  E5C3D5C6 40404040                        1179+         DC    CL8'VCNF'         instruction name
00001708  00000010                                 1180+         DC    A(16)             result length
0000170C  000017A4                                 1181+         DC    A(RE7)            address of expected resul
00001710  00000000 00000000                        1182+         DS    FD                gap
00001718  00000000 00000000                        1183+V1O7     DS    XL16              V1 output
00001720  00000000 00000000
00001728  00000000 00000000                        1184+         DS    FD                   gap
00001730  00000000                                 1185+FPC_R_7  DS    F                 FPC after instruction
00001738  00000000 00000000                        1186+         DS    FD                   gap
00001740  40404040 40404040                        1187+         DC    CL8' '            was cross check skipped?
00001748  00000000 00000000                        1188+         DS    FD                   gap
00001750  00000000 00000000                        1189+XCO7     DS    XL16              Cross check Output
00001758  00000000 00000000
00001760  00000000 00000000                        1190+         DS    FD                   gap
00001768  00000000                                 1191+FPC_XC_7 DS    F                 FPC after cross check
00001770  00000000 00000000                        1192+         DS    FD                   gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001778  00000000                                 1193+         DS    F                 debug area
0000177C  00000000                                 1194+         DS    F
                                                   1195+*
00001780                                           1196+X7       DS    0F
00001780  B29D 85A4                     000007A4   1197+         LFPC  FPCMOFF           initialize FPC
00001784  E320 500C 0014                000016FC   1198+         LGF   R2,V2_7           get v2
0000178A  E762 0000 0806                00000000   1199+         VL    V22,0(R2)
00001790  E666 0001 0C55                           1200+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001796  B29C 5040                     00001730   1201+         STFPC FPC_R_7           save FPC
0000179A  E760 5028 080E                00001718   1202+         VST   V22,V1O7          save instruction result
000017A0  07FB                                     1203+         BR    R11               return
000017A4                                           1204+RE7      DS    0F                expected 16 byte result
000017A4                                           1205+         DROP  R5
000017A4  40DB0000 00000000                        1206          DC    XL16'40DB0000000000000000000000D800'
000017AC  00000000 0000D800
000017B4  41B60000 00000000                        1207          DC    XL16'41B6000000000000000000000F000'
000017BC  00000000 0000F000
                                                   1208
                                                   1209 * additional tests
                                                   1210 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                   1211          VRR_A VCNF,0,1,00,00,S                skip xc - rounded
000017C8                                           1212+         DS    0FD
000017C8                        000017C8           1213+         USING *,R5              base for test data and test routine
000017C8  00001858                                 1214+T8       DC    A(X8)             address of test routine
000017CC  0008                                     1215+         DC    H'8'              test number
000017CE  00                                       1216+         DC    X'00'
000017CF  E2                                       1217+         DC    CL1'S'            Y = skip cross check
000017D0  00                                       1218+         DC    HL1'0'            m3
000017D1  01                                       1219+         DC    HL1'1'            m4
000017D2  00                                       1220+FLG8     DC    X'00'             expected FPC flags
000017D3  00                                       1221+VXC8     DC    X'00'             expected VXC
000017D4  0000188C                                 1222+V2_8     DC    A(RE8+16)         address of v2: 16-byte packed decimal
000017D8  E5C3D5C6 40404040                        1223+         DC    CL8'VCNF'         instruction name
000017E0  00000010                                 1224+         DC    A(16)             result length
000017E4  0000187C                                 1225+         DC    A(RE8)            address of expected resul
000017E8  00000000 00000000                        1226+         DS    FD                gap
000017F0  00000000 00000000                        1227+V1O8     DS    XL16              V1 output
000017F8  00000000 00000000
00001800  00000000 00000000                        1228+         DS    FD                   gap
00001808  00000000                                 1229+FPC_R_8  DS    F                 FPC after instruction
00001810  00000000 00000000                        1230+         DS    FD                   gap
00001818  40404040 40404040                        1231+         DC    CL8' '            was cross check skipped?
00001820  00000000 00000000                        1232+         DS    FD                   gap
00001828  00000000 00000000                        1233+XCO8     DS    XL16              Cross check Output
00001830  00000000 00000000
00001838  00000000 00000000                        1234+         DS    FD                   gap
00001840  00000000                                 1235+FPC_XC_8 DS    F                 FPC after cross check
00001848  00000000 00000000                        1236+         DS    FD                   gap
00001850  00000000                                 1237+         DS    F                 debug area
00001854  00000000                                 1238+         DS    F
                                                   1239+*
00001858                                           1240+X8       DS    0F
00001858  B29D 85A4                     000007A4   1241+         LFPC  FPCMOFF           initialize FPC
0000185C  E320 500C 0014                000017D4   1242+         LGF   R2,V2_8           get v2
00001862  E762 0000 0806                00000000   1243+         VL    V22,0(R2)
00001868  E666 0001 0C55                           1244+         VCNF  V22,V22,0,1       test instruction (dest is source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000186E  B29C 5040                     00001808  1245+         STFPC FPC_R_8          save FPC
00001872  E760 5028 080E                000017F0  1246+         VST   V22,V1O8         save instruction result
00001878  07FB                                    1247+         BR    R11              return
0000187C                                          1248+RE8      DS    0F               expected 16 byte result
0000187C                                          1249+         DROP  R5
0000187C  5E000000 00000000                       1250          DC    XL16'5E000000000000000000000000D800'
00001884  00000000 0000D800
0000188C  7BFF0000 00000000                       1251          DC    XL16'7BFF000000000000000000000000F000'
00001894  00000000 0000F000
                                                  1252
                                                  1253 * min tiny (normal): 2^-14 (0.00006103515625)
                                                  1254          VRR_A VCNF,0,1,00,00,N
000018A0                                          1255+         DS    0FD
000018A0                        000018A0          1256+         USING *,R5             base for test data and test routine
000018A0  00001930                                1257+T9       DC    A(X9)            address of test routine
000018A4  0009                                    1258+         DC    H'9'             test number
000018A6  00                                      1259+         DC    X'00'
000018A7  D5                                      1260+         DC    CL1'N'           Y = skip cross check
000018A8  00                                      1261+         DC    HL1'0'           m3
000018A9  01                                      1262+         DC    HL1'1'           m4
000018AA  00                                      1263+FLG9     DC    X'00'            expected FPC flags
000018AB  00                                      1264+VXC9     DC    X'00'            expected VXC
000018AC  00001964                                1265+V2_9     DC    A(RE9+16)        address of v2: 16-byte packed decimal
000018B0  E5C3D5C6 40404040                       1266+         DC    CL8'VCNF'        instruction name
000018B8  00000010                                1267+         DC    A(16)            result length
000018BC  00001954                                1268+         DC    A(RE9)           address of expected resul
000018C0  00000000 00000000                       1269+         DS    FD               gap
000018C8  00000000 00000000                       1270+V1O9     DS    XL16             V1 output
000018D0  00000000 00000000
000018D8  00000000 00000000                       1271+         DS    FD                  gap
000018E0  00000000                                1272+FPC_R_9  DS    F                FPC after instruction
000018E8  00000000 00000000                       1273+         DS    FD                  gap
000018F0  40404040 40404040                       1274+         DC    CL8' '           was cross check skipped?
000018F8  00000000 00000000                       1275+         DS    FD                  gap
00001900  00000000 00000000                       1276+XCO9     DS    XL16             Cross check Output
00001908  00000000 00000000
00001910  00000000 00000000                       1277+         DS    FD                  gap
00001918  00000000                                1278+FPC_XC_9 DS    F                FPC after cross check
00001920  00000000 00000000                       1279+         DS    FD                  gap
00001928  00000000                                1280+         DS    F                debug area
0000192C  00000000                                1281+         DS    F
                                                  1282+*
00001930                                          1283+X9       DS    0F
00001930  B29D 85A4                     000007A4  1284+         LFPC  FPCMOFF          initialize FPC
00001934  E320 500C 0014                000018AC  1285+         LGF   R2,V2_9          get v2
0000193A  E762 0000 0806                00000000  1286+         VL    V22,0(R2)
00001940  E666 0001 0C55                          1287+         VCNF  V22,V22,0,1      test instruction (dest is source)
00001946  B29C 5040                     000018E0  1288+         STFPC FPC_R_9          save FPC
0000194A  E760 5028 080E                000018C8  1289+         VST   V22,V1O9         save instruction result
00001950  07FB                                    1290+         BR    R11              return
00001954                                          1291+RE9      DS    0F               expected 16 byte result
00001954                                          1292+         DROP  R5
00001954  22000000 00000000                       1293          DC    XL16'220000000000000000000000000D800'
0000195C  00000000 0000D800
00001964  04000000 00000000                       1294          DC    XL16'040000000000000000000000000F000'
0000196C  00000000 0000F000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1295
                                                   1296 * min tiny (subnormal): 2^-24 (0.00000005960464477539062 5)
                                                   1297          VRR_A VCNF,0,1,00,00,N
00001978                                           1298+         DS    0FD
00001978                       00001978            1299+         USING *,R5              base for test data and test routine
00001978  00001A08                                 1300+T10      DC    A(X10)            address of test routine
0000197C  000A                                     1301+         DC    H'10'             test number
0000197E  00                                       1302+         DC    X'00'
0000197F  D5                                       1303+         DC    CL1'N'            Y = skip cross check
00001980  00                                       1304+         DC    HL1'0'            m3
00001981  01                                       1305+         DC    HL1'1'            m4
00001982  00                                       1306+FLG10    DC    X'00'             expected FPC flags
00001983  00                                       1307+VXC10    DC    X'00'             expected VXC
00001984  00001A3C                                 1308+V2_10    DC    A(RE10+16)        address of v2: 16-byte packed decimal
00001988  E5C3D5C6 40404040                        1309+         DC    CL8'VCNF'         instruction name
00001990  00000010                                 1310+         DC    A(16)             result length
00001994  00001A2C                                 1311+         DC    A(RE10)           address of expected resul
00001998  00000000 00000000                        1312+         DS    FD                gap
000019A0  00000000 00000000                        1313+V1O10    DS    XL16              V1 output
000019A8  00000000 00000000
000019B0  00000000 00000000                        1314+         DS    FD                   gap
000019B8  00000000                                 1315+FPC_R_10 DS    F                 FPC after instruction
000019C0  00000000 00000000                        1316+         DS    FD                   gap
000019C8  40404040 40404040                        1317+         DC    CL8' '            was cross check skipped?
000019D0  00000000 00000000                        1318+         DS    FD                   gap
000019D8  00000000 00000000                        1319+XCO10    DS    XL16              Cross check Output
000019E0  00000000 00000000
000019E8  00000000 00000000                        1320+         DS    FD                   gap
000019F0  00000000                                 1321+FPC_XC_10 DS   F                 FPC after cross check
000019F8  00000000 00000000                        1322+         DS    FD                   gap
00001A00  00000000                                 1323+         DS    F                 debug area
00001A04  00000000                                 1324+         DS    F
                                                   1325+*
00001A08                                           1326+X10      DS    0F
00001A08  B29D 85A4                     000007A4   1327+         LFPC  FPCMOFF           initialize FPC
00001A0C  E320 500C 0014                00001984   1328+         LGF   R2,V2_10          get v2
00001A12  E762 0000 0806                00000000   1329+         VL    V22,0(R2)
00001A18  E666 0001 0C55                           1330+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001A1E  B29C 5040                     000019B8   1331+         STFPC FPC_R_10          save FPC
00001A22  E760 5028 080E                000019A0   1332+         VST   V22,V1O10         save instruction result
00001A28  07FB                                     1333+         BR    R11               return
00001A2C                                           1334+RE10     DS    0F                expected 16 byte result
00001A2C                                           1335+         DROP  R5
00001A2C  0E000000 00000000                        1336          DC    XL16'0E000000000000000000000000D800'
00001A34  00000000 0000D800
00001A3C  00010000 00000000                        1337          DC    XL16'00010000000000000000000000F000'
00001A44  00000000 0000F000
                                                   1338
                                                   1339 * NAN,
                                                   1340          VRR_A VCNF,0,1,80,00,S           skip xcheck - includes NAN
00001A50                                           1341+         DS    0FD
00001A50                       00001A50            1342+         USING *,R5              base for test data and test routine
00001A50  00001AE0                                 1343+T11      DC    A(X11)            address of test routine
00001A54  000B                                     1344+         DC    H'11'             test number
00001A56  00                                       1345+         DC    X'00'
00001A57  E2                                       1346+         DC    CL1'S'            Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001A58  00                                      1347+         DC    HL1'0'            m3
00001A59  01                                      1348+         DC    HL1'1'            m4
00001A5A  80                                      1349+FLG11    DC    X'80'             expected FPC flags
00001A5B  00                                      1350+VXC11    DC    X'00'             expected VXC
00001A5C  00001B14                                1351+V2_11    DC    A(RE11+16)        address of v2: 16-byte packed decimal
00001A60  E5C3D5C6 40404040                       1352+         DC    CL8'VCNF'         instruction name
00001A68  00000010                                1353+         DC    A(16)             result length
00001A6C  00001B04                                1354+         DC    A(RE11)           address of expected resul
00001A70  00000000 00000000                       1355+         DS    FD                gap
00001A78  00000000 00000000                       1356+V1O11    DS    XL16              V1 output
00001A80  00000000 00000000
00001A88  00000000 00000000                       1357+         DS    FD                   gap
00001A90  00000000                                1358+FPC_R_11 DS    F                 FPC after instruction
00001A98  00000000 00000000                       1359+         DS    FD                   gap
00001AA0  40404040 40404040                       1360+         DC    CL8' '            was cross check skipped?
00001AA8  00000000 00000000                       1361+         DS    FD                   gap
00001AB0  00000000 00000000                       1362+XCO11    DS    XL16              Cross check Output
00001AB8  00000000 00000000
00001AC0  00000000 00000000                       1363+         DS    FD                   gap
00001AC8  00000000                                1364+FPC_XC_11 DS   F                 FPC after cross check
00001AD0  00000000 00000000                       1365+         DS    FD                   gap
00001AD8  00000000                                1366+         DS    F                 debug area
00001ADC  00000000                                1367+         DS    F
                                                  1368+*
00001AE0                                          1369+X11      DS    0F
00001AE0  B29D 85A4                     000007A4  1370+         LFPC  FPCMOFF           initialize FPC
00001AE4  E320 500C 0014                00001A5C  1371+         LGF   R2,V2_11          get v2
00001AEA  E762 0000 0806                00000000  1372+         VL    V22,0(R2)
00001AF0  E666 0001 0C55                          1373+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001AF6  B29C 5040                     00001A90  1374+         STFPC FPC_R_11          save FPC
00001AFA  E760 5028 080E                00001A78  1375+         VST   V22,V1O11         save instruction result
00001B00  07FB                                    1376+         BR    R11               return
00001B04                                          1377+RE11     DS    0F                expected 16 byte result
00001B04                                          1378+         DROP  R5
00001B04  FFFF0000 00000000                       1379          DC    XL16'FFFF0000000000000000000000D800'
00001B0C  00000000 0000D800
00001B14  FFFF0000 00000000                       1380          DC    XL16'FFFF0000000000000000000000F000'
00001B1C  00000000 0000F000
                                                  1381
                                                  1382 * inexact - bad m3
                                                  1383          VRR_A VCNF,5,1,08,00,S                    skip xc - inexact
00001B28                                          1384+         DS    0FD
00001B28                        00001B28          1385+         USING *,R5              base for test data and test routine
00001B28  00001BB8                                1386+T12      DC    A(X12)            address of test routine
00001B2C  000C                                    1387+         DC    H'12'             test number
00001B2E  00                                      1388+         DC    X'00'
00001B2F  E2                                      1389+         DC    CL1'S'            Y = skip cross check
00001B30  05                                      1390+         DC    HL1'5'            m3
00001B31  01                                      1391+         DC    HL1'1'            m4
00001B32  08                                      1392+FLG12    DC    X'08'             expected FPC flags
00001B33  00                                      1393+VXC12    DC    X'00'             expected VXC
00001B34  00001BEC                                1394+V2_12    DC    A(RE12+16)        address of v2: 16-byte packed decimal
00001B38  E5C3D5C6 40404040                       1395+         DC    CL8'VCNF'         instruction name
00001B40  00000010                                1396+         DC    A(16)             result length
00001B44  00001BDC                                1397+         DC    A(RE12)           address of expected resul
00001B48  00000000 00000000                       1398+         DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001B50  00000000 00000000                        1399+V1O12    DS    XL16              V1 output
00001B58  00000000 00000000
00001B60  00000000 00000000                        1400+         DS    FD                   gap
00001B68  00000000                                 1401+FPC_R_12 DS    F                 FPC after instruction
00001B70  00000000 00000000                        1402+         DS    FD                   gap
00001B78  40404040 40404040                        1403+         DC    CL8' '            was cross check skipped?
00001B80  00000000 00000000                        1404+         DS    FD                   gap
00001B88  00000000 00000000                        1405+XCO12    DS    XL16              Cross check Output
00001B90  00000000 00000000
00001B98  00000000 00000000                        1406+         DS    FD                   gap
00001BA0  00000000                                 1407+FPC_XC_12 DS   F                 FPC after cross check
00001BA8  00000000 00000000                        1408+         DS    FD                   gap
00001BB0  00000000                                 1409+         DS    F                 debug area
00001BB4  00000000                                 1410+         DS    F
                                                   1411+*
00001BB8                                           1412+X12      DS    0F
00001BB8  B29D 85A4                     000007A4   1413+         LFPC  FPCMOFF           initialize FPC
00001BBC  E320 500C 0014                00001B34   1414+         LGF   R2,V2_12          get v2
00001BC2  E762 0000 0806                00000000   1415+         VL    V22,0(R2)
00001BC8  E666 0001 5C55                           1416+         VCNF  V22,V22,5,1       test instruction (dest is source)
00001BCE  B29C 5040                     00001B68   1417+         STFPC FPC_R_12          save FPC
00001BD2  E760 5028 080E                00001B50   1418+         VST   V22,V1O12         save instruction result
00001BD8  07FB                                     1419+         BR    R11               return
00001BDC                                           1420+RE12     DS    0F                expected 16 byte result
00001BDC                                           1421+         DROP  R5
00001BDC  00000000 00000000                        1422          DC    XL16'00000000000000000000000000000000'
00001BE4  00000000 00000000
00001BEC  00010000 00000000                        1423          DC    XL16'00010000000000000000000000F000'
00001BF4  00000000 0000F000
                                                   1424
                                                   1425 * inexact - bad m4
                                                   1426          VRR_A VCNF,0,5,08,00,S                    skip xc - inexact
00001C00                                           1427+         DS    0FD
00001C00                        00001C00           1428+         USING *,R5              base for test data and test routine
00001C00  00001C90                                 1429+T13      DC    A(X13)            address of test routine
00001C04  000D                                     1430+         DC    H'13'             test number
00001C06  00                                       1431+         DC    X'00'
00001C07  E2                                       1432+         DC    CL1'S'            Y = skip cross check
00001C08  00                                       1433+         DC    HL1'0'            m3
00001C09  05                                       1434+         DC    HL1'5'            m4
00001C0A  08                                       1435+FLG13    DC    X'08'             expected FPC flags
00001C0B  00                                       1436+VXC13    DC    X'00'             expected VXC
00001C0C  00001CC4                                 1437+V2_13    DC    A(RE13+16)        address of v2: 16-byte packed decimal
00001C10  E5C3D5C6 40404040                        1438+         DC    CL8'VCNF'         instruction name
00001C18  00000010                                 1439+         DC    A(16)             result length
00001C1C  00001CB4                                 1440+         DC    A(RE13)           address of expected resul
00001C20  00000000 00000000                        1441+         DS    FD                gap
00001C28  00000000 00000000                        1442+V1O13    DS    XL16              V1 output
00001C30  00000000 00000000
00001C38  00000000 00000000                        1443+         DS    FD                   gap
00001C40  00000000                                 1444+FPC_R_13 DS    F                 FPC after instruction
00001C48  00000000 00000000                        1445+         DS    FD                   gap
00001C50  40404040 40404040                        1446+         DC    CL8' '            was cross check skipped?
00001C58  00000000 00000000                        1447+         DS    FD                   gap
00001C60  00000000 00000000                        1448+XCO13    DS    XL16              Cross check Output
00001C68  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001C70  00000000 00000000                       1449+         DS    FD                   gap
00001C78  00000000                                1450+FPC_XC_13 DS   F                 FPC after cross check
00001C80  00000000 00000000                       1451+         DS    FD                   gap
00001C88  00000000                                1452+         DS    F                 debug area
00001C8C  00000000                                1453+         DS    F
                                                  1454+*
00001C90                                          1455+X13      DS    0F
00001C90  B29D 85A4                     000007A4  1456+         LFPC  FPCMOFF           initialize FPC
00001C94  E320 500C 0014                00001C0C  1457+         LGF   R2,V2_13          get v2
00001C9A  E762 0000 0806                00000000  1458+         VL    V22,0(R2)
00001CA0  E666 0005 0C55                          1459+         VCNF  V22,V22,0,5       test instruction (dest is source)
00001CA6  B29C 5040                     00001C40  1460+         STFPC FPC_R_13          save FPC
00001CAA  E760 5028 080E                00001C28  1461+         VST   V22,V1O13         save instruction result
00001CB0  07FB                                    1462+         BR    R11               return
00001CB4                                          1463+RE13     DS    0F                expected 16 byte result
00001CB4                                          1464+         DROP  R5
00001CB4  00000000 00000000                       1465          DC    XL16'00000000000000000000000000000000'
00001CBC  00000000 00000000
00001CC4  00010000 00000000                       1466          DC    XL16'00010000000000000000000000000F000'
00001CCC  00000000 0000F000
                                                  1467
                                                  1468 * more tests
                                                  1469 * +3.140625, -3.140625
                                                  1470          VRR_A VCNF,0,1,00,00,N
00001CD8                                          1471+         DS    0FD
00001CD8                        00001CD8          1472+         USING *,R5              base for test data and test routine
00001CD8  00001D68                                1473+T14      DC    A(X14)            address of test routine
00001CDC  000E                                    1474+         DC    H'14'             test number
00001CDE  00                                      1475+         DC    X'00'
00001CDF  D5                                      1476+         DC    CL1'N'            Y = skip cross check
00001CE0  00                                      1477+         DC    HL1'0'            m3
00001CE1  01                                      1478+         DC    HL1'1'            m4
00001CE2  00                                      1479+FLG14    DC    X'00'             expected FPC flags
00001CE3  00                                      1480+VXC14    DC    X'00'             expected VXC
00001CE4  00001D9C                                1481+V2_14    DC    A(RE14+16)        address of v2: 16-byte packed decimal
00001CE8  E5C3D5C6 40404040                       1482+         DC    CL8'VCNF'         instruction name
00001CF0  00000010                                1483+         DC    A(16)             result length
00001CF4  00001D8C                                1484+         DC    A(RE14)           address of expected resul
00001CF8  00000000 00000000                       1485+         DS    FD                gap
00001D00  00000000 00000000                       1486+V1O14    DS    XL16              V1 output
00001D08  00000000 00000000
00001D10  00000000 00000000                       1487+         DS    FD                   gap
00001D18  00000000                                1488+FPC_R_14 DS    F                 FPC after instruction
00001D20  00000000 00000000                       1489+         DS    FD                   gap
00001D28  40404040 40404040                       1490+         DC    CL8' '            was cross check skipped?
00001D30  00000000 00000000                       1491+         DS    FD                   gap
00001D38  00000000 00000000                       1492+XCO14    DS    XL16              Cross check Output
00001D40  00000000 00000000
00001D48  00000000 00000000                       1493+         DS    FD                   gap
00001D50  00000000                                1494+FPC_XC_14 DS   F                 FPC after cross check
00001D58  00000000 00000000                       1495+         DS    FD                   gap
00001D60  00000000                                1496+         DS    F                 debug area
00001D64  00000000                                1497+         DS    F
                                                  1498+*
00001D68                                          1499+X14      DS    0F
00001D68  B29D 85A4                     000007A4  1500+         LFPC  FPCMOFF           initialize FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001D6C  E320 500C 0014                00001CE4  1501+         LGF   R2,V2_14          get v2
00001D72  E762 0000 0806                00000000  1502+         VL    V22,0(R2)
00001D78  E666 0001 0C55                          1503+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001D7E  B29C 5040                     00001D18  1504+         STFPC FPC_R_14          save FPC
00001D82  E760 5028 080E                00001D00  1505+         VST   V22,V1O14         save instruction result
00001D88  07FB                                    1506+         BR    R11               return
00001D8C                                          1507+RE14     DS    0F                expected 16 byte result
00001D8C                                          1508+         DROP  R5
00001D8C  42240000 C2240000                       1509          DC    XL16'42240000C224000000000000000D800'
00001D94  00000000 0000D800
00001D9C  44480000 C4480000                       1510          DC    XL16'44480000C448000000000000000F000'
00001DA4  00000000 0000F000
                                                  1511
                                                  1512 * +27.15625, -27.15625                           skip xc - lost digits
                                                  1513          VRR_A VCNF,0,1,00,00,S
00001DB0                                          1514+         DS    0FD
00001DB0                        00001DB0          1515+         USING *,R5              base for test data and test routine
00001DB0  00001E40                                1516+T15      DC    A(X15)            address of test routine
00001DB4  000F                                    1517+         DC    H'15'             test number
00001DB6  00                                      1518+         DC    X'00'
00001DB7  E2                                      1519+         DC    CL1'S'            Y = skip cross check
00001DB8  00                                      1520+         DC    HL1'0'            m3
00001DB9  01                                      1521+         DC    HL1'1'            m4
00001DBA  00                                      1522+FLG15    DC    X'00'             expected FPC flags
00001DBB  00                                      1523+VXC15    DC    X'00'             expected VXC
00001DBC  00001E74                                1524+V2_15    DC    A(RE15+16)        address of v2: 16-byte packed decimal
00001DC0  E5C3D5C6 40404040                       1525+         DC    CL8'VCNF'         instruction name
00001DC8  00000010                                1526+         DC    A(16)             result length
00001DCC  00001E64                                1527+         DC    A(RE15)           address of expected resul
00001DD0  00000000 00000000                       1528+         DS    FD                gap
00001DD8  00000000 00000000                       1529+V1O15    DS    XL16              V1 output
00001DE0  00000000 00000000
00001DE8  00000000 00000000                       1530+         DS    FD                   gap
00001DF0  00000000                                1531+FPC_R_15 DS    F                 FPC after instruction
00001DF8  00000000 00000000                       1532+         DS    FD                   gap
00001E00  40404040 40404040                       1533+         DC    CL8' '            was cross check skipped?
00001E08  00000000 00000000                       1534+         DS    FD                   gap
00001E10  00000000 00000000                       1535+XCO15    DS    XL16              Cross check Output
00001E18  00000000 00000000
00001E20  00000000 00000000                       1536+         DS    FD                   gap
00001E28  00000000                                1537+FPC_XC_15 DS   F                 FPC after cross check
00001E30  00000000 00000000                       1538+         DS    FD                   gap
00001E38  00000000                                1539+         DS    F                 debug area
00001E3C  00000000                                1540+         DS    F
                                                  1541+*
00001E40                                          1542+X15      DS    0F
00001E40  B29D 85A4                     000007A4  1543+         LFPC  FPCMOFF           initialize FPC
00001E44  E320 500C 0014                00001DBC  1544+         LGF   R2,V2_15          get v2
00001E4A  E762 0000 0806                00000000  1545+         VL    V22,0(R2)
00001E50  E666 0001 0C55                          1546+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001E56  B29C 5040                     00001DF0  1547+         STFPC FPC_R_15          save FPC
00001E5A  E760 5028 080E                00001DD8  1548+         VST   V22,V1O15         save instruction result
00001E60  07FB                                    1549+         BR    R11               return
00001E64                                          1550+RE15     DS    0F                expected 16 byte result
00001E64                                          1551+         DROP  R5
00001E64  2F650000 AF650000                       1552          DC    XL16'2F650000AF650000000000000000D800'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001E6C  00000000 0000D800
00001E74  1EC90000 9EC90000                         1553          DC    XL16'1EC900009EC90000000000000000F000'
00001E7C  00000000 0000F000
                                                    1554
                                                    1555 * +65504, -65504
                                                    1556          VRR_A VCNF,0,1,00,00,S                   skip xc - lost digits
00001E88                                            1557+         DS    0FD
00001E88                        00001E88            1558+         USING *,R5              base for test data and test routine
00001E88  00001F18                                  1559+T16      DC    A(X16)            address of test routine
00001E8C  0010                                      1560+         DC    H'16'             test number
00001E8E  00                                        1561+         DC    X'00'
00001E8F  E2                                        1562+         DC    CL1'S'            Y = skip cross check
00001E90  00                                        1563+         DC    HL1'0'            m3
00001E91  01                                        1564+         DC    HL1'1'            m4
00001E92  00                                        1565+FLG16    DC    X'00'             expected FPC flags
00001E93  00                                        1566+VXC16    DC    X'00'             expected VXC
00001E94  00001F4C                                  1567+V2_16    DC    A(RE16+16)        address of v2: 16-byte packed decimal
00001E98  E5C3D5C6 40404040                         1568+         DC    CL8'VCNF'         instruction name
00001EA0  00000010                                  1569+         DC    A(16)             result length
00001EA4  00001F3C                                  1570+         DC    A(RE16)           address of expected resul
00001EA8  00000000 00000000                         1571+         DS    FD                gap
00001EB0  00000000 00000000                         1572+V1O16    DS    XL16              V1 output
00001EB8  00000000 00000000
00001EC0  00000000 00000000                         1573+         DS    FD                   gap
00001EC8  00000000                                  1574+FPC_R_16 DS    F                 FPC after instruction
00001ED0  00000000 00000000                         1575+         DS    FD                   gap
00001ED8  40404040 40404040                         1576+         DC    CL8' '            was cross check skipped?
00001EE0  00000000 00000000                         1577+         DS    FD                   gap
00001EE8  00000000 00000000                         1578+XCO16    DS    XL16              Cross check Output
00001EF0  00000000 00000000
00001EF8  00000000 00000000                         1579+         DS    FD                   gap
00001F00  00000000                                  1580+FPC_XC_16 DS   F                 FPC after cross check
00001F08  00000000 00000000                         1581+         DS    FD                   gap
00001F10  00000000                                  1582+         DS    F                 debug area
00001F14  00000000                                  1583+         DS    F
                                                    1584+*
00001F18                                            1585+X16      DS    0F
00001F18  B29D 85A4                     000007A4    1586+         LFPC  FPCMOFF           initialize FPC
00001F1C  E320 500C 0014                00001E94    1587+         LGF   R2,V2_16          get v2
00001F22  E762 0000 0806                00000000    1588+         VL    V22,0(R2)
00001F28  E666 0001 0C55                            1589+         VCNF  V22,V22,0,1       test instruction (dest is source)
00001F2E  B29C 5040                     00001EC8    1590+         STFPC FPC_R_16          save FPC
00001F32  E760 5028 080E                00001EB0    1591+         VST   V22,V1O16         save instruction result
00001F38  07FB                                      1592+         BR    R11               return
00001F3C                                            1593+RE16     DS    0F                expected 16 byte result
00001F3C                                            1594+         DROP  R5
00001F3C  5E000000 DE000000                         1595          DC    XL16'5E000000DE000000000000000000D800'
00001F44  00000000 0000D800
00001F4C  7BFF0000 FBFF0000                         1596          DC    XL16'7BFF0000FBFF000000000000000F000'
00001F54  00000000 0000F000
                                                    1597
                                                    1598 * +Normal, -Normal
                                                    1599          VRR_A VCNF,0,1,00,00,N
00001F60                                            1600+         DS    0FD
00001F60                        00001F60            1601+         USING *,R5              base for test data and test routine
00001F60  00001FF0                                  1602+T17      DC    A(X17)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001F64  0011                                     1603+          DC    H'17'              test number
00001F66  00                                       1604+          DC    X'00'
00001F67  D5                                       1605+          DC    CL1'N'             Y = skip cross check
00001F68  00                                       1606+          DC    HL1'0'             m3
00001F69  01                                       1607+          DC    HL1'1'             m4
00001F6A  00                                       1608+FLG17     DC    X'00'              expected FPC flags
00001F6B  00                                       1609+VXC17     DC    X'00'              expected VXC
00001F6C  00002024                                 1610+V2_17     DC    A(RE17+16)         address of v2: 16-byte packed decimal
00001F70  E5C3D5C6 40404040                        1611+          DC    CL8'VCNF'          instruction name
00001F78  00000010                                 1612+          DC    A(16)              result length
00001F7C  00002014                                 1613+          DC    A(RE17)            address of expected resul
00001F80  00000000 00000000                        1614+          DS    FD                 gap
00001F88  00000000 00000000                        1615+V1O17     DS    XL16               V1 output
00001F90  00000000 00000000
00001F98  00000000 00000000                        1616+          DS    FD                    gap
00001FA0  00000000                                 1617+FPC_R_17  DS    F                  FPC after instruction
00001FA8  00000000 00000000                        1618+          DS    FD                    gap
00001FB0  40404040 40404040                        1619+          DC    CL8' '             was cross check skipped?
00001FB8  00000000 00000000                        1620+          DS    FD                    gap
00001FC0  00000000 00000000                        1621+XCO17     DS    XL16               Cross check Output
00001FC8  00000000 00000000
00001FD0  00000000 00000000                        1622+          DS    FD                    gap
00001FD8  00000000                                 1623+FPC_XC_17 DS    F                  FPC after cross check
00001FE0  00000000 00000000                        1624+          DS    FD                    gap
00001FE8  00000000                                 1625+          DS    F                  debug area
00001FEC  00000000                                 1626+          DS    F
                                                   1627+*
00001FF0                                           1628+X17       DS    0F
00001FF0  B29D 85A4                     000007A4   1629+          LFPC  FPCMOFF            initialize FPC
00001FF4  E320 500C 0014                00001F6C   1630+          LGF   R2,V2_17           get v2
00001FFA  E762 0000 0806                00000000   1631+          VL    V22,0(R2)
00002000  E666 0001 0C55                           1632+          VCNF  V22,V22,0,1        test instruction (dest is source)
00002006  B29C 5040                     00001FA0   1633+          STFPC FPC_R_17           save FPC
0000200A  E760 5028 080E                00001F88   1634+          VST   V22,V1O17          save instruction result
00002010  07FB                                     1635+          BR    R11                return
00002014                                           1636+RE17      DS    0F                 expected 16 byte result
00002014                                           1637+          DROP  R5
00002014  40800000 C0800000                        1638           DC    XL16'40800000C08000000000000000000D800'
0000201C  00000000 0000D800
00002024  41000000 C1000000                        1639           DC    XL16'41000000C10000000000000000000F000'
0000202C  00000000 0000F000
                                                   1640
                                                   1641 * +Subnormal, -Subnormal
                                                   1642           VRR_A VCNF,0,1,00,00,N
00002038                                           1643+          DS    0FD
00002038                        00002038           1644+          USING *,R5               base for test data and test routine
00002038  000020C8                                 1645+T18       DC    A(X18)             address of test routine
0000203C  0012                                     1646+          DC    H'18'              test number
0000203E  00                                       1647+          DC    X'00'
0000203F  D5                                       1648+          DC    CL1'N'             Y = skip cross check
00002040  00                                       1649+          DC    HL1'0'             m3
00002041  01                                       1650+          DC    HL1'1'             m4
00002042  00                                       1651+FLG18     DC    X'00'              expected FPC flags
00002043  00                                       1652+VXC18     DC    X'00'              expected VXC
00002044  000020FC                                 1653+V2_18     DC    A(RE18+16)         address of v2: 16-byte packed decimal
00002048  E5C3D5C6 40404040                        1654+          DC    CL8'VCNF'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002050  00000010                                 1655+         DC    A(16)              result length
00002054  000020EC                                 1656+         DC    A(RE18)            address of expected resul
00002058  00000000 00000000                        1657+         DS    FD                 gap
00002060  00000000 00000000                        1658+V1O18    DS    XL16               V1 output
00002068  00000000 00000000
00002070  00000000 00000000                        1659+         DS    FD                    gap
00002078  00000000                                 1660+FPC_R_18 DS    F                  FPC after instruction
00002080  00000000 00000000                        1661+         DS    FD                    gap
00002088  40404040 40404040                        1662+         DC    CL8' '             was cross check skipped?
00002090  00000000 00000000                        1663+         DS    FD                    gap
00002098  00000000 00000000                        1664+XCO18    DS    XL16               Cross check Output
000020A0  00000000 00000000
000020A8  00000000 00000000                        1665+         DS    FD                    gap
000020B0  00000000                                 1666+FPC_XC_18 DS   F                  FPC after cross check
000020B8  00000000 00000000                        1667+         DS    FD                    gap
000020C0  00000000                                 1668+         DS    F                  debug area
000020C4  00000000                                 1669+         DS    F
                                                   1670+*
000020C8                                           1671+X18      DS    0F
000020C8  B29D 85A4                     000007A4   1672+         LFPC  FPCMOFF            initialize FPC
000020CC  E320 500C 0014                00002044   1673+         LGF   R2,V2_18           get v2
000020D2  E762 0000 0806                00000000   1674+         VL    V22,0(R2)
000020D8  E666 0001 0C55                           1675+         VCNF  V22,V22,0,1        test instruction (dest is source)
000020DE  B29C 5040                     00002078   1676+         STFPC FPC_R_18           save FPC
000020E2  E760 5028 080E                00002060   1677+         VST   V22,V1O18          save instruction result
000020E8  07FB                                     1678+         BR    R11                return
000020EC                                           1679+RE18     DS    0F                 expected 16 byte result
000020EC                                           1680+         DROP  R5
000020EC  21FF0000 A1FF0000                        1681          DC    XL16'21FF0000A1FF000000000000000D800'
000020F4  00000000 0000D800
000020FC  03FF0000 83FF0000                        1682          DC    XL16'03FF000083FF000000000000000F000'
00002104  00000000 0000F000
                                                   1683
                                                   1684 * +Infinity, -Infinity                          skip xc - infinity
                                                   1685          VRR_A VCNF,0,1,20,00,S
00002110                                           1686+         DS    0FD
00002110                        00002110           1687+         USING *,R5               base for test data and test routine
00002110  000021A0                                 1688+T19      DC    A(X19)             address of test routine
00002114  0013                                     1689+         DC    H'19'              test number
00002116  00                                       1690+         DC    X'00'
00002117  E2                                       1691+         DC    CL1'S'             Y = skip cross check
00002118  00                                       1692+         DC    HL1'0'             m3
00002119  01                                       1693+         DC    HL1'1'             m4
0000211A  20                                       1694+FLG19    DC    X'20'              expected FPC flags
0000211B  00                                       1695+VXC19    DC    X'00'              expected VXC
0000211C  000021D4                                 1696+V2_19    DC    A(RE19+16)         address of v2: 16-byte packed decimal
00002120  E5C3D5C6 40404040                        1697+         DC    CL8'VCNF'          instruction name
00002128  00000010                                 1698+         DC    A(16)              result length
0000212C  000021C4                                 1699+         DC    A(RE19)            address of expected resul
00002130  00000000 00000000                        1700+         DS    FD                 gap
00002138  00000000 00000000                        1701+V1O19    DS    XL16               V1 output
00002140  00000000 00000000
00002148  00000000 00000000                        1702+         DS    FD                    gap
00002150  00000000                                 1703+FPC_R_19 DS    F                  FPC after instruction
00002158  00000000 00000000                        1704+         DS    FD                    gap
00002160  40404040 40404040                        1705+         DC    CL8' '             was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002168  00000000 00000000                        1706+          DS    FD                   gap
00002170  00000000 00000000                        1707+XCO19     DS    XL16               Cross check Output
00002178  00000000 00000000
00002180  00000000 00000000                        1708+          DS    FD                   gap
00002188  00000000                                 1709+FPC_XC_19 DS    F                  FPC after cross check
00002190  00000000 00000000                        1710+          DS    FD                   gap
00002198  00000000                                 1711+          DS    F                  debug area
0000219C  00000000                                 1712+          DS    F
                                                   1713+*
000021A0                                           1714+X19       DS    0F
000021A0  B29D 85A4                     000007A4   1715+          LFPC  FPCMOFF            initialize FPC
000021A4  E320 500C 0014                0000211C   1716+          LGF   R2,V2_19           get v2
000021AA  E762 0000 0806                00000000   1717+          VL    V22,0(R2)
000021B0  E666 0001 0C55                           1718+          VCNF  V22,V22,0,1        test instruction (dest is source)
000021B6  B29C 5040                     00002150   1719+          STFPC FPC_R_19           save FPC
000021BA  E760 5028 080E                00002138   1720+          VST   V22,V1O19          save instruction result
000021C0  07FB                                     1721+          BR    R11                return
000021C4                                           1722+RE19      DS    0F                 expected 16 byte result
000021C4                                           1723+          DROP  R5
000021C4  7FFF0000 FFFF0000                        1724           DC    XL16'7FFF0000FFFF000000000000000D800'
000021CC  00000000 0000D800
000021D4  7C000000 FC000000                        1725           DC    XL16'7C000000FC00000000000000000F000'
000021DC  00000000 0000F000
                                                   1726
                                                   1727 * +QNaN, -QNaN                                  skip xc - NaN
                                                   1728           VRR_A VCNF,0,1,80,00,S
000021E8                                           1729+          DS    0FD
000021E8                        000021E8           1730+          USING *,R5               base for test data and test routine
000021E8  00002278                                 1731+T20       DC    A(X20)             address of test routine
000021EC  0014                                     1732+          DC    H'20'              test number
000021EE  00                                       1733+          DC    X'00'
000021EF  E2                                       1734+          DC    CL1'S'             Y = skip cross check
000021F0  00                                       1735+          DC    HL1'0'             m3
000021F1  01                                       1736+          DC    HL1'1'             m4
000021F2  80                                       1737+FLG20     DC    X'80'              expected FPC flags
000021F3  00                                       1738+VXC20     DC    X'00'              expected VXC
000021F4  000022AC                                 1739+V2_20     DC    A(RE20+16)         address of v2: 16-byte packed decimal
000021F8  E5C3D5C6 40404040                        1740+          DC    CL8'VCNF'          instruction name
00002200  00000010                                 1741+          DC    A(16)              result length
00002204  0000229C                                 1742+          DC    A(RE20)            address of expected resul
00002208  00000000 00000000                        1743+          DS    FD                 gap
00002210  00000000 00000000                        1744+V1O20     DS    XL16               V1 output
00002218  00000000 00000000
00002220  00000000 00000000                        1745+          DS    FD                   gap
00002228  00000000                                 1746+FPC_R_20  DS    F                  FPC after instruction
00002230  00000000 00000000                        1747+          DS    FD                   gap
00002238  40404040 40404040                        1748+          DC    CL8' '             was cross check skipped?
00002240  00000000 00000000                        1749+          DS    FD                   gap
00002248  00000000 00000000                        1750+XCO20     DS    XL16               Cross check Output
00002250  00000000 00000000
00002258  00000000 00000000                        1751+          DS    FD                   gap
00002260  00000000                                 1752+FPC_XC_20 DS    F                  FPC after cross check
00002268  00000000 00000000                        1753+          DS    FD                   gap
00002270  00000000                                 1754+          DS    F                  debug area
00002274  00000000                                 1755+          DS    F
                                                   1756+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002278                                          1757+X20      DS    0F
00002278  B29D 85A4                     000007A4  1758+         LFPC  FPCMOFF           initialize FPC
0000227C  E320 500C 0014                000021F4  1759+         LGF   R2,V2_20          get v2
00002282  E762 0000 0806                00000000  1760+         VL    V22,0(R2)
00002288  E666 0001 0C55                          1761+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000228E  B29C A028                     00002228  1762+         STFPC FPC_R_20          save FPC
00002292  E760 A010 080E                00002210  1763+         VST   V22,V1O20         save instruction result
00002298  07FB                                    1764+         BR    R11               return
0000229C                                          1765+RE20     DS    0F                expected 16 byte result
0000229C                                          1766+         DROP  R5
0000229C  7FFF0000 FFFF0000                       1767          DC    XL16'7FFF0000FFFF0000000000000000D800'
000022A4  00000000 0000D800
000022AC  7E080000 FE080000                       1768          DC    XL16'7E080000FE080000000000000000F000'
000022B4  00000000 0000F000
                                                  1769
                                                  1770 * +SNaN, -SNaN                                   skip xc - NaN
                                                  1771          VRR_A VCNF,0,1,80,00,S
000022C0                                          1772+         DS    0FD
000022C0                        000022C0          1773+         USING *,R5              base for test data and test routine
000022C0  00002350                                1774+T21      DC    A(X21)            address of test routine
000022C4  0015                                    1775+         DC    H'21'             test number
000022C6  00                                      1776+         DC    X'00'
000022C7  E2                                      1777+         DC    CL1'S'            Y = skip cross check
000022C8  00                                      1778+         DC    HL1'0'            m3
000022C9  01                                      1779+         DC    HL1'1'            m4
000022CA  80                                      1780+FLG21    DC    X'80'             expected FPC flags
000022CB  00                                      1781+VXC21    DC    X'00'             expected VXC
000022CC  00002384                                1782+V2_21    DC    A(RE21+16)        address of v2: 16-byte packed decimal
000022D0  E5C3D5C6 40404040                       1783+         DC    CL8'VCNF'         instruction name
000022D8  00000010                                1784+         DC    A(16)             result length
000022DC  00002374                                1785+         DC    A(RE21)           address of expected resul
000022E0  00000000 00000000                       1786+         DS    FD                gap
000022E8  00000000 00000000                       1787+V1O21    DS    XL16              V1 output
000022F0  00000000 00000000
000022F8  00000000 00000000                       1788+         DS    FD                   gap
00002300  00000000                                1789+FPC_R_21 DS    F                 FPC after instruction
00002308  00000000 00000000                       1790+         DS    FD                   gap
00002310  40404040 40404040                       1791+         DC    CL8' '            was cross check skipped?
00002318  00000000 00000000                       1792+         DS    FD                   gap
00002320  00000000 00000000                       1793+XCO21    DS    XL16              Cross check Output
00002328  00000000 00000000
00002330  00000000 00000000                       1794+         DS    FD                   gap
00002338  00000000                                1795+FPC_XC_21 DS   F                 FPC after cross check
00002340  00000000 00000000                       1796+         DS    FD                   gap
00002348  00000000                                1797+         DS    F                 debug area
0000234C  00000000                                1798+         DS    F
                                                  1799+*
00002350                                          1800+X21      DS    0F
00002350  B29D 85A4                     000007A4  1801+         LFPC  FPCMOFF           initialize FPC
00002354  E320 500C 0014                000022CC  1802+         LGF   R2,V2_21          get v2
0000235A  E762 0000 0806                00000000  1803+         VL    V22,0(R2)
00002360  E666 0001 0C55                          1804+         VCNF  V22,V22,0,1       test instruction (dest is source)
00002366  B29C 5040                     00002300  1805+         STFPC FPC_R_21          save FPC
0000236A  E760 5028 080E                000022E8  1806+         VST   V22,V1O21         save instruction result
00002370  07FB                                    1807+         BR    R11               return
00002374                                          1808+RE21     DS    0F                expected 16 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002374                                           1809+         DROP  R5
00002374  7FFF0000 FFFF0000                        1810          DC    XL16'7FFF0000FFFF0000000000000000D800'
0000237C  00000000 0000D800
00002384  7C080000 FC080000                        1811          DC    XL16'7C080000FC080000000000000000F000'
0000238C  00000000 0000F000
                                                   1812
                                                   1813 * multiple exception types
                                                   1814 * +Infinity,  -QNaN                                skip xc - infinity
                                                   1815          VRR_A VCNF,0,1,A0,00,S
00002398                                           1816+         DS    0FD
00002398                        00002398           1817+         USING *,R5              base for test data and test routine
00002398  00002428                                 1818+T22      DC    A(X22)            address of test routine
0000239C  0016                                     1819+         DC    H'22'             test number
0000239E  00                                       1820+         DC    X'00'
0000239F  E2                                       1821+         DC    CL1'S'            Y = skip cross check
000023A0  00                                       1822+         DC    HL1'0'            m3
000023A1  01                                       1823+         DC    HL1'1'            m4
000023A2  A0                                       1824+FLG22    DC    X'A0'             expected FPC flags
000023A3  00                                       1825+VXC22    DC    X'00'             expected VXC
000023A4  0000245C                                 1826+V2_22    DC    A(RE22+16)        address of v2: 16-byte packed decimal
000023A8  E5C3D5C6 40404040                        1827+         DC    CL8'VCNF'         instruction name
000023B0  00000010                                 1828+         DC    A(16)             result length
000023B4  0000244C                                 1829+         DC    A(RE22)           address of expected resul
000023B8  00000000 00000000                        1830+         DS    FD                gap
000023C0  00000000 00000000                        1831+V1O22    DS    XL16              V1 output
000023C8  00000000 00000000
000023D0  00000000 00000000                        1832+         DS    FD                   gap
000023D8  00000000                                 1833+FPC_R_22 DS    F                 FPC after instruction
000023E0  00000000 00000000                        1834+         DS    FD                   gap
000023E8  40404040 40404040                        1835+         DC    CL8' '            was cross check skipped?
000023F0  00000000 00000000                        1836+         DS    FD                   gap
000023F8  00000000 00000000                        1837+XCO22    DS    XL16              Cross check Output
00002400  00000000 00000000
00002408  00000000 00000000                        1838+         DS    FD                   gap
00002410  00000000                                 1839+FPC_XC_22 DS   F                 FPC after cross check
00002418  00000000 00000000                        1840+         DS    FD                   gap
00002420  00000000                                 1841+         DS    F                 debug area
00002424  00000000                                 1842+         DS    F
                                                   1843+*
00002428                                           1844+X22      DS    0F
00002428  B29D 85A4                     000007A4   1845+         LFPC  FPCMOFF           initialize FPC
0000242C  E320 500C 0014                000023A4   1846+         LGF   R2,V2_22          get v2
00002432  E762 0000 0806                00000000   1847+         VL    V22,0(R2)
00002438  E666 0001 0C55                           1848+         VCNF  V22,V22,0,1       test instruction (dest is source)
0000243E  B29C 5040                     000023D8   1849+         STFPC FPC_R_22          save FPC
00002442  E760 5028 080E                000023C0   1850+         VST   V22,V1O22         save instruction result
00002448  07FB                                     1851+         BR    R11               return
0000244C                                           1852+RE22     DS    0F                expected 16 byte result
0000244C                                           1853+         DROP  R5
0000244C  7FFF0000 FFFF0000                        1854          DC    XL16'7FFF0000FFFF0000000000000000D800'
00002454  00000000 0000D800
0000245C  7C000000 FE080000                        1855          DC    XL16'7C000000FE080000000000000000F000'
00002464  00000000 0000F000
                                                   1856
                                                   1857 * +Infinity,  -QNaN, -SNaN                       skip xc - infinity
                                                   1858          VRR_A VCNF,0,1,A0,00,S
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002470                                           1859+         DS    0FD
00002470                     00002470              1860+         USING *,R5              base for test data and test routine
00002470  00002500                                 1861+T23      DC    A(X23)            address of test routine
00002474  0017                                     1862+         DC    H'23'             test number
00002476  00                                       1863+         DC    X'00'
00002477  E2                                       1864+         DC    CL1'S'            Y = skip cross check
00002478  00                                       1865+         DC    HL1'0'            m3
00002479  01                                       1866+         DC    HL1'1'            m4
0000247A  A0                                       1867+FLG23    DC    X'A0'             expected FPC flags
0000247B  00                                       1868+VXC23    DC    X'00'             expected VXC
0000247C  00002534                                 1869+V2_23    DC    A(RE23+16)        address of v2: 16-byte packed decimal
00002480  E5C3D5C6 40404040                        1870+         DC    CL8'VCNF'         instruction name
00002488  00000010                                 1871+         DC    A(16)             result length
0000248C  00002524                                 1872+         DC    A(RE23)           address of expected resul
00002490  00000000 00000000                        1873+         DS    FD                gap
00002498  00000000 00000000                        1874+V1O23    DS    XL16              V1 output
000024A0  00000000 00000000
000024A8  00000000 00000000                        1875+         DS    FD                   gap
000024B0  00000000                                 1876+FPC_R_23 DS    F                 FPC after instruction
000024B8  00000000 00000000                        1877+         DS    FD                   gap
000024C0  40404040 40404040                        1878+         DC    CL8' '            was cross check skipped?
000024C8  00000000 00000000                        1879+         DS    FD                   gap
000024D0  00000000 00000000                        1880+XCO23    DS    XL16              Cross check Output
000024D8  00000000 00000000
000024E0  00000000 00000000                        1881+         DS    FD                   gap
000024E8  00000000                                 1882+FPC_XC_23 DS   F                 FPC after cross check
000024F0  00000000 00000000                        1883+         DS    FD                   gap
000024F8  00000000                                 1884+         DS    F                 debug area
000024FC  00000000                                 1885+         DS    F
                                                   1886+*
00002500                                           1887+X23      DS    0F
00002500  B29D 85A4                     000007A4   1888+         LFPC  FPCMOFF           initialize FPC
00002504  E320 500C 0014                0000247C   1889+         LGF   R2,V2_23          get v2
0000250A  E762 0000 0806                00000000   1890+         VL    V22,0(R2)
00002510  E666 0001 0C55                           1891+         VCNF  V22,V22,0,1       test instruction (dest is source)
00002516  B29C 5040                     000024B0   1892+         STFPC FPC_R_23          save FPC
0000251A  E760 5028 080E                00002498   1893+         VST   V22,V1O23         save instruction result
00002520  07FB                                     1894+         BR    R11               return
00002524                                           1895+RE23     DS    0F                expected 16 byte result
00002524                                           1896+         DROP  R5
00002524  7FFF0000 FFFF0000                        1897          DC    XL16'7FFF0000FFFF0000FFFF00000000D800'
0000252C  FFFF0000 0000D800
00002534  7C000000 FE080000                        1898          DC    XL16'7C000000FE080000FC0800000000F000'
0000253C  FC080000 0000F000
                                                   1899
                                                   1900 *-----------------------------------------------------------------------
                                                   1901 * VCLFNH   - VECTOR FP CONVERT AND LENGTHEN FROM NNP HIGH
                                                   1902 *-----------------------------------------------------------------------
                                                   1903 *  dlfloat -> short float (with cross check: short float -> dlfloat)
                                                   1904 *
                                                   1905
                                                   1906 * +0, -0     simple instruction and 'test' test
                                                   1907          VRR_A VCLFNH,2,0,00,00,N
00002548                                           1908+         DS    0FD
00002548                     00002548              1909+         USING *,R5              base for test data and test routine
00002548  000025D8                                 1910+T24      DC    A(X24)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000254C  0018                                     1911+          DC    H'24'              test number
0000254E  00                                       1912+          DC    X'00'
0000254F  D5                                       1913+          DC    CL1'N'             Y = skip cross check
00002550  02                                       1914+          DC    HL1'2'             m3
00002551  00                                       1915+          DC    HL1'0'             m4
00002552  00                                       1916+FLG24     DC    X'00'              expected FPC flags
00002553  00                                       1917+VXC24     DC    X'00'              expected VXC
00002554  0000260C                                 1918+V2_24     DC    A(RE24+16)         address of v2: 16-byte packed decimal
00002558  E5C3D3C6 D5C84040                        1919+          DC    CL8'VCLFNH'        instruction name
00002560  00000010                                 1920+          DC    A(16)              result length
00002564  000025FC                                 1921+          DC    A(RE24)            address of expected resul
00002568  00000000 00000000                        1922+          DS    FD                 gap
00002570  00000000 00000000                        1923+V1O24     DS    XL16               V1 output
00002578  00000000 00000000
00002580  00000000 00000000                        1924+          DS    FD                    gap
00002588  00000000                                 1925+FPC_R_24  DS    F                  FPC after instruction
00002590  00000000 00000000                        1926+          DS    FD                    gap
00002598  40404040 40404040                        1927+          DC    CL8' '             was cross check skipped?
000025A0  00000000 00000000                        1928+          DS    FD                    gap
000025A8  00000000 00000000                        1929+XCO24     DS    XL16               Cross check Output
000025B0  00000000 00000000
000025B8  00000000 00000000                        1930+          DS    FD                    gap
000025C0  00000000                                 1931+FPC_XC_24 DS    F                  FPC after cross check
000025C8  00000000 00000000                        1932+          DS    FD                    gap
000025D0  00000000                                 1933+          DS    F                  debug area
000025D4  00000000                                 1934+          DS    F
                                                   1935+*
000025D8                                           1936+X24       DS    0F
000025D8  B29D 85A4                     000007A4   1937+          LFPC  FPCMOFF            initialize FPC
000025DC  E320 500C 0014                00002554   1938+          LGF   R2,V2_24           get v2
000025E2  E762 0000 0806                00000000   1939+          VL    V22,0(R2)
000025E8  E666 0000 2C56                           1940+          VCLFNH V22,V22,2,0       test instruction (dest is source)
000025EE  B29C 5040                     00002588   1941+          STFPC FPC_R_24           save FPC
000025F2  E760 5028 080E                00002570   1942+          VST   V22,V1O24          save instruction result
000025F8  07FB                                     1943+          BR    R11                return
000025FC                                           1944+RE24      DS    0F                 expected 16 byte result
000025FC                                           1945+          DROP  R5
000025FC  00000000 80000000                        1946           DC    XL16'00000000800000000000000000000000'
00002604  00000000 00000000
0000260C  00008000 00000000                        1947           DC    XL16'00008000000000000000000000000000'
00002614  00000000 00000000
                                                   1948
                                                   1949 * +1, -1
                                                   1950           VRR_A VCLFNH,2,0,00,00,N
00002620                                           1951+          DS    0FD
00002620                        00002620           1952+          USING *,R5               base for test data and test routine
00002620  000026B0                                 1953+T25       DC    A(X25)             address of test routine
00002624  0019                                     1954+          DC    H'25'              test number
00002626  00                                       1955+          DC    X'00'
00002627  D5                                       1956+          DC    CL1'N'             Y = skip cross check
00002628  02                                       1957+          DC    HL1'2'             m3
00002629  00                                       1958+          DC    HL1'0'             m4
0000262A  00                                       1959+FLG25     DC    X'00'              expected FPC flags
0000262B  00                                       1960+VXC25     DC    X'00'              expected VXC
0000262C  000026E4                                 1961+V2_25     DC    A(RE25+16)         address of v2: 16-byte packed decimal
00002630  E5C3D3C6 D5C84040                        1962+          DC    CL8'VCLFNH'        instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002638  00000010                                 1963+         DC    A(16)              result length
0000263C  000026D4                                 1964+         DC    A(RE25)            address of expected resul
00002640  00000000 00000000                        1965+         DS    FD                 gap
00002648  00000000 00000000                        1966+V1O25    DS    XL16               V1 output
00002650  00000000 00000000
00002658  00000000 00000000                        1967+         DS    FD                    gap
00002660  00000000                                 1968+FPC_R_25 DS    F                  FPC after instruction
00002668  00000000 00000000                        1969+         DS    FD                    gap
00002670  40404040 40404040                        1970+         DC    CL8' '             was cross check skipped?
00002678  00000000 00000000                        1971+         DS    FD                    gap
00002680  00000000 00000000                        1972+XCO25    DS    XL16               Cross check Output
00002688  00000000 00000000
00002690  00000000 00000000                        1973+         DS    FD                    gap
00002698  00000000                                 1974+FPC_XC_25 DS   F                  FPC after cross check
000026A0  00000000 00000000                        1975+         DS    FD                    gap
000026A8  00000000                                 1976+         DS    F                  debug area
000026AC  00000000                                 1977+         DS    F
                                                   1978+*
000026B0                                           1979+X25      DS    0F
000026B0  B29D 85A4                     000007A4   1980+         LFPC  FPCMOFF            initialize FPC
000026B4  E320 500C 0014                0000262C   1981+         LGF   R2,V2_25           get v2
000026BA  E762 0000 0806                00000000   1982+         VL    V22,0(R2)
000026C0  E666 0000 2C56                           1983+         VCLFNH V22,V22,2,0       test instruction (dest is source)
000026C6  B29C 5040                     00002660   1984+         STFPC FPC_R_25           save FPC
000026CA  E760 5028 080E                00002648   1985+         VST   V22,V1O25          save instruction result
000026D0  07FB                                     1986+         BR    R11                return
000026D4                                           1987+RE25     DS    0F                 expected 16 byte result
000026D4                                           1988+         DROP  R5
000026D4  3F800000 BF800000                        1989          DC    XL16'3F800000BF800000000000000000000'
000026DC  00000000 00000000
000026E4  3E00BE00 00000000                        1990          DC    XL16'3E00BE000000000000000000000000'
000026EC  00000000 00000000
                                                   1991
                                                   1992 * +0.5, -0.5
                                                   1993          VRR_A VCLFNH,2,0,00,00,N
000026F8                                           1994+         DS    0FD
000026F8                        000026F8           1995+         USING *,R5               base for test data and test routine
000026F8  00002788                                 1996+T26      DC    A(X26)             address of test routine
000026FC  001A                                     1997+         DC    H'26'              test number
000026FE  00                                       1998+         DC    X'00'
000026FF  D5                                       1999+         DC    CL1'N'             Y = skip cross check
00002700  02                                       2000+         DC    HL1'2'             m3
00002701  00                                       2001+         DC    HL1'0'             m4
00002702  00                                       2002+FLG26    DC    X'00'              expected FPC flags
00002703  00                                       2003+VXC26    DC    X'00'              expected VXC
00002704  000027BC                                 2004+V2_26    DC    A(RE26+16)         address of v2: 16-byte packed decimal
00002708  E5C3D3C6 D5C84040                        2005+         DC    CL8'VCLFNH'        instruction name
00002710  00000010                                 2006+         DC    A(16)              result length
00002714  000027AC                                 2007+         DC    A(RE26)            address of expected resul
00002718  00000000 00000000                        2008+         DS    FD                 gap
00002720  00000000 00000000                        2009+V1O26    DS    XL16               V1 output
00002728  00000000 00000000
00002730  00000000 00000000                        2010+         DS    FD                    gap
00002738  00000000                                 2011+FPC_R_26 DS    F                  FPC after instruction
00002740  00000000 00000000                        2012+         DS    FD                    gap
00002748  40404040 40404040                        2013+         DC    CL8' '             was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002750  00000000 00000000                        2014+          DS    FD                   gap
00002758  00000000 00000000                        2015+XCO26     DS    XL16               Cross check Output
00002760  00000000 00000000
00002768  00000000 00000000                        2016+          DS    FD                   gap
00002770  00000000                                 2017+FPC_XC_26 DS    F                  FPC after cross check
00002778  00000000 00000000                        2018+          DS    FD                   gap
00002780  00000000                                 2019+          DS    F                  debug area
00002784  00000000                                 2020+          DS    F
                                                   2021+*
00002788                                           2022+X26       DS    0F
00002788  B29D 85A4                     000007A4   2023+          LFPC  FPCMOFF            initialize FPC
0000278C  E320 500C 0014                00002704   2024+          LGF   R2,V2_26           get v2
00002792  E762 0000 0806                00000000   2025+          VL    V22,0(R2)
00002798  E666 0000 2C56                           2026+          VCLFNH V22,V22,2,0       test instruction (dest is source)
0000279E  B29C 5040                     00002738   2027+          STFPC FPC_R_26           save FPC
000027A2  E760 5028 080E                00002720   2028+          VST   V22,V1O26          save instruction result
000027A8  07FB                                     2029+          BR    R11                return
000027AC                                           2030+RE26      DS    0F                 expected 16 byte result
000027AC                                           2031+          DROP  R5
000027AC  3F000000 BF000000                        2032           DC    XL16'3F000000BF000000000000000000000000'
000027B4  00000000 00000000
000027BC  3C00BC00 00000000                        2033           DC    XL16'3C00BC000000000000000000000000000'
000027C4  00000000 00000000
                                                   2034
                                                   2035 * 1/64, -1/64
                                                   2036           VRR_A VCLFNH,2,0,00,00,N
000027D0                                           2037+          DS    0FD
000027D0                        000027D0           2038+          USING *,R5               base for test data and test routine
000027D0  00002860                                 2039+T27       DC    A(X27)             address of test routine
000027D4  001B                                     2040+          DC    H'27'              test number
000027D6  00                                       2041+          DC    X'00'
000027D7  D5                                       2042+          DC    CL1'N'             Y = skip cross check
000027D8  02                                       2043+          DC    HL1'2'             m3
000027D9  00                                       2044+          DC    HL1'0'             m4
000027DA  00                                       2045+FLG27     DC    X'00'              expected FPC flags
000027DB  00                                       2046+VXC27     DC    X'00'              expected VXC
000027DC  00002894                                 2047+V2_27     DC    A(RE27+16)         address of v2: 16-byte packed decimal
000027E0  E5C3D3C6 D5C84040                        2048+          DC    CL8'VCLFNH'        instruction name
000027E8  00000010                                 2049+          DC    A(16)              result length
000027EC  00002884                                 2050+          DC    A(RE27)            address of expected resul
000027F0  00000000 00000000                        2051+          DS    FD                 gap
000027F8  00000000 00000000                        2052+V1O27     DS    XL16               V1 output
00002800  00000000 00000000
00002808  00000000 00000000                        2053+          DS    FD                   gap
00002810  00000000                                 2054+FPC_R_27  DS    F                  FPC after instruction
00002818  00000000 00000000                        2055+          DS    FD                   gap
00002820  40404040 40404040                        2056+          DC    CL8' '             was cross check skipped?
00002828  00000000 00000000                        2057+          DS    FD                   gap
00002830  00000000 00000000                        2058+XCO27     DS    XL16               Cross check Output
00002838  00000000 00000000
00002840  00000000 00000000                        2059+          DS    FD                   gap
00002848  00000000                                 2060+FPC_XC_27 DS    F                  FPC after cross check
00002850  00000000 00000000                        2061+          DS    FD                   gap
00002858  00000000                                 2062+          DS    F                  debug area
0000285C  00000000                                 2063+          DS    F
                                                   2064+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002860                                          2065+X27      DS    0F
00002860  B29D 85A4                     000007A4  2066+         LFPC  FPCMOFF           initialize FPC
00002864  E320 500C 0014                000027DC  2067+         LGF   R2,V2_27          get v2
0000286A  E762 0000 0806                00000000  2068+         VL    V22,0(R2)
00002870  E666 0000 2C56                          2069+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002876  B29C 5040                     00002810  2070+         STFPC FPC_R_27          save FPC
0000287A  E760 5028 080E                000027F8  2071+         VST   V22,V1O27         save instruction result
00002880  07FB                                    2072+         BR    R11               return
00002884                                          2073+RE27     DS    0F                expected 16 byte result
00002884                                          2074+         DROP  R5
00002884  3C800000 BC800000                       2075          DC    XL16'3C800000BC800000000000000000000'
0000288C  00000000 00000000
00002894  3200B200 00000000                       2076          DC    XL16'3200B200000000000000000000000000'
0000289C  00000000 00000000
                                                  2077
                                                  2078 * +15, -15
                                                  2079          VRR_A VCLFNH,2,0,00,00,N
000028A8                                          2080+         DS    0FD
000028A8                        000028A8          2081+         USING *,R5              base for test data and test routine
000028A8  00002938                                2082+T28      DC    A(X28)            address of test routine
000028AC  001C                                    2083+         DC    H'28'             test number
000028AE  00                                      2084+         DC    X'00'
000028AF  D5                                      2085+         DC    CL1'N'            Y = skip cross check
000028B0  02                                      2086+         DC    HL1'2'            m3
000028B1  00                                      2087+         DC    HL1'0'            m4
000028B2  00                                      2088+FLG28    DC    X'00'             expected FPC flags
000028B3  00                                      2089+VXC28    DC    X'00'             expected VXC
000028B4  0000296C                                2090+V2_28    DC    A(RE28+16)        address of v2: 16-byte packed decimal
000028B8  E5C3D3C6 D5C84040                       2091+         DC    CL8'VCLFNH'       instruction name
000028C0  00000010                                2092+         DC    A(16)             result length
000028C4  0000295C                                2093+         DC    A(RE28)           address of expected resul
000028C8  00000000 00000000                       2094+         DS    FD                gap
000028D0  00000000 00000000                       2095+V1O28    DS    XL16              V1 output
000028D8  00000000 00000000
000028E0  00000000 00000000                       2096+         DS    FD                   gap
000028E8  00000000                                2097+FPC_R_28 DS    F                 FPC after instruction
000028F0  00000000 00000000                       2098+         DS    FD                   gap
000028F8  40404040 40404040                       2099+         DC    CL8' '            was cross check skipped?
00002900  00000000 00000000                       2100+         DS    FD                   gap
00002908  00000000 00000000                       2101+XCO28    DS    XL16              Cross check Output
00002910  00000000 00000000
00002918  00000000 00000000                       2102+         DS    FD                   gap
00002920  00000000                                2103+FPC_XC_28 DS   F                 FPC after cross check
00002928  00000000 00000000                       2104+         DS    FD                   gap
00002930  00000000                                2105+         DS    F                 debug area
00002934  00000000                                2106+         DS    F
                                                  2107+*
00002938                                          2108+X28      DS    0F
00002938  B29D 85A4                     000007A4  2109+         LFPC  FPCMOFF           initialize FPC
0000293C  E320 500C 0014                000028B4  2110+         LGF   R2,V2_28          get v2
00002942  E762 0000 0806                00000000  2111+         VL    V22,0(R2)
00002948  E666 0000 2C56                          2112+         VCLFNH V22,V22,2,0      test instruction (dest is source)
0000294E  B29C 5040                     000028E8  2113+         STFPC FPC_R_28          save FPC
00002952  E760 5028 080E                000028D0  2114+         VST   V22,V1O28         save instruction result
00002958  07FB                                    2115+         BR    R11               return
0000295C                                          2116+RE28     DS    0F                expected 16 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000295C                                           2117+         DROP  R5
0000295C  41700000 C1700000                        2118          DC    XL16'41700000C1700000000000000000000'
00002964  00000000 00000000
0000296C  45C0C5C0 00000000                        2119          DC    XL16'45C0C5C0000000000000000000000000'
00002974  00000000 00000000
                                                   2120
                                                   2121 * +20/7, -20/7 (about)
                                                   2122          VRR_A VCLFNH,2,0,00,00,N
00002980                                           2123+         DS    0FD
00002980                      00002980             2124+         USING *,R5              base for test data and test routine
00002980  00002A10                                 2125+T29      DC    A(X29)            address of test routine
00002984  001D                                     2126+         DC    H'29'             test number
00002986  00                                       2127+         DC    X'00'
00002987  D5                                       2128+         DC    CL1'N'            Y = skip cross check
00002988  02                                       2129+         DC    HL1'2'            m3
00002989  00                                       2130+         DC    HL1'0'            m4
0000298A  00                                       2131+FLG29    DC    X'00'             expected FPC flags
0000298B  00                                       2132+VXC29    DC    X'00'             expected VXC
0000298C  00002A44                                 2133+V2_29    DC    A(RE29+16)        address of v2: 16-byte packed decimal
00002990  E5C3D3C6 D5C84040                        2134+         DC    CL8'VCLFNH'       instruction name
00002998  00000010                                 2135+         DC    A(16)             result length
0000299C  00002A34                                 2136+         DC    A(RE29)           address of expected resul
000029A0  00000000 00000000                        2137+         DS    FD                gap
000029A8  00000000 00000000                        2138+V1O29    DS    XL16              V1 output
000029B0  00000000 00000000
000029B8  00000000 00000000                        2139+         DS    FD                   gap
000029C0  00000000                                 2140+FPC_R_29 DS    F                 FPC after instruction
000029C8  00000000 00000000                        2141+         DS    FD                   gap
000029D0  40404040 40404040                        2142+         DC    CL8' '            was cross check skipped?
000029D8  00000000 00000000                        2143+         DS    FD                   gap
000029E0  00000000 00000000                        2144+XCO29    DS    XL16              Cross check Output
000029E8  00000000 00000000
000029F0  00000000 00000000                        2145+         DS    FD                   gap
000029F8  00000000                                 2146+FPC_XC_29 DS   F                 FPC after cross check
00002A00  00000000 00000000                        2147+         DS    FD                   gap
00002A08  00000000                                 2148+         DS    F                 debug area
00002A0C  00000000                                 2149+         DS    F
                                                   2150+*
00002A10                                           2151+X29      DS    0F
00002A10  B29D 85A4                     000007A4   2152+         LFPC  FPCMOFF           initialize FPC
00002A14  E320 500C 0014                0000298C   2153+         LGF   R2,V2_29          get v2
00002A1A  E762 0000 0806                00000000   2154+         VL    V22,0(R2)
00002A20  E666 0000 2C56                           2155+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002A26  B29C 5040                     000029C0   2156+         STFPC FPC_R_29          save FPC
00002A2A  E760 5028 080E                000029A8   2157+         VST   V22,V1O29         save instruction result
00002A30  07FB                                     2158+         BR    R11               return
00002A34                                           2159+RE29     DS    0F                expected 16 byte result
00002A34                                           2160+         DROP  R5
00002A34  4036C000 C036C000                        2161          DC    XL16'4036C000C036C000000000000000000'
00002A3C  00000000 00000000
00002A44  40DBC0DB 00000000                        2162          DC    XL16'40DBC0DB000000000000000000000000'
00002A4C  00000000 00000000
                                                   2163
                                                   2164 * additional tests
                                                   2165 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                   2166          VRR_A VCLFNH,2,0,00,00,N
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002A58                                           2167+         DS    0FD
00002A58                     00002A58              2168+         USING *,R5              base for test data and test routine
00002A58  00002AE8                                 2169+T30      DC    A(X30)            address of test routine
00002A5C  001E                                     2170+         DC    H'30'             test number
00002A5E  00                                       2171+         DC    X'00'
00002A5F  D5                                       2172+         DC    CL1'N'            Y = skip cross check
00002A60  02                                       2173+         DC    HL1'2'            m3
00002A61  00                                       2174+         DC    HL1'0'            m4
00002A62  00                                       2175+FLG30    DC    X'00'             expected FPC flags
00002A63  00                                       2176+VXC30    DC    X'00'             expected VXC
00002A64  00002B1C                                 2177+V2_30    DC    A(RE30+16)        address of v2: 16-byte packed decimal
00002A68  E5C3D3C6 D5C84040                        2178+         DC    CL8'VCLFNH'       instruction name
00002A70  00000010                                 2179+         DC    A(16)             result length
00002A74  00002B0C                                 2180+         DC    A(RE30)           address of expected resul
00002A78  00000000 00000000                        2181+         DS    FD                gap
00002A80  00000000 00000000                        2182+V1O30    DS    XL16              V1 output
00002A88  00000000 00000000
00002A90  00000000 00000000                        2183+         DS    FD                   gap
00002A98  00000000                                 2184+FPC_R_30 DS    F                 FPC after instruction
00002AA0  00000000 00000000                        2185+         DS    FD                   gap
00002AA8  40404040 40404040                        2186+         DC    CL8' '            was cross check skipped?
00002AB0  00000000 00000000                        2187+         DS    FD                   gap
00002AB8  00000000 00000000                        2188+XCO30    DS    XL16              Cross check Output
00002AC0  00000000 00000000
00002AC8  00000000 00000000                        2189+         DS    FD                   gap
00002AD0  00000000                                 2190+FPC_XC_30 DS   F                 FPC after cross check
00002AD8  00000000 00000000                        2191+         DS    FD                   gap
00002AE0  00000000                                 2192+         DS    F                 debug area
00002AE4  00000000                                 2193+         DS    F
                                                   2194+*
00002AE8                                           2195+X30      DS    0F
00002AE8  B29D 85A4                     000007A4   2196+         LFPC  FPCMOFF           initialize FPC
00002AEC  E320 500C 0014                00002A64   2197+         LGF   R2,V2_30          get v2
00002AF2  E762 0000 0806                00000000   2198+         VL    V22,0(R2)
00002AF8  E666 0000 2C56                           2199+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002AFE  B29C 5040                     00002A98   2200+         STFPC FPC_R_30          save FPC
00002B02  E760 5028 080E                00002A80   2201+         VST   V22,V1O30         save instruction result
00002B08  07FB                                     2202+         BR    R11               return
00002B0C                                           2203+RE30     DS    0F                expected 16 byte result
00002B0C                                           2204+         DROP  R5
00002B0C  47800000 00000000                        2205          DC    XL16'47800000000000000000000000000000'
00002B14  00000000 00000000
00002B1C  5E000000 00000000                        2206          DC    XL16'5E00000000000000000000000000000'
00002B24  00000000 00000000
                                                   2207
                                                   2208 * max  dlfloat:  2^(33)-2ulp
                                                   2209          VRR_A VCLFNH,2,0,00,00,N
00002B30                                           2210+         DS    0FD
00002B30                     00002B30              2211+         USING *,R5              base for test data and test routine
00002B30  00002BC0                                 2212+T31      DC    A(X31)            address of test routine
00002B34  001F                                     2213+         DC    H'31'             test number
00002B36  00                                       2214+         DC    X'00'
00002B37  D5                                       2215+         DC    CL1'N'            Y = skip cross check
00002B38  02                                       2216+         DC    HL1'2'            m3
00002B39  00                                       2217+         DC    HL1'0'            m4
00002B3A  00                                       2218+FLG31    DC    X'00'             expected FPC flags
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002B3B  00                                       2219+VXC31    DC    X'00'              expected VXC
00002B3C  00002BF4                                 2220+V2_31    DC    A(RE31+16)         address of v2: 16-byte packed decimal
00002B40  E5C3D3C6 D5C84040                        2221+         DC    CL8'VCLFNH'        instruction name
00002B48  00000010                                 2222+         DC    A(16)              result length
00002B4C  00002BE4                                 2223+         DC    A(RE31)            address of expected resul
00002B50  00000000 00000000                        2224+         DS    FD                 gap
00002B58  00000000 00000000                        2225+V1O31    DS    XL16               V1 output
00002B60  00000000 00000000
00002B68  00000000 00000000                        2226+         DS    FD                    gap
00002B70  00000000                                 2227+FPC_R_31 DS    F                  FPC after instruction
00002B78  00000000 00000000                        2228+         DS    FD                    gap
00002B80  40404040 40404040                        2229+         DC    CL8' '             was cross check skipped?
00002B88  00000000 00000000                        2230+         DS    FD                    gap
00002B90  00000000 00000000                        2231+XCO31    DS    XL16               Cross check Output
00002B98  00000000 00000000
00002BA0  00000000 00000000                        2232+         DS    FD                    gap
00002BA8  00000000                                 2233+FPC_XC_31 DS   F                  FPC after cross check
00002BB0  00000000 00000000                        2234+         DS    FD                    gap
00002BB8  00000000                                 2235+         DS    F                  debug area
00002BBC  00000000                                 2236+         DS    F
                                                   2237+*
00002BC0                                           2238+X31      DS    0F
00002BC0  B29D 85A4                     000007A4   2239+         LFPC  FPCMOFF            initialize FPC
00002BC4  E320 500C 0014                00002B3C   2240+         LGF   R2,V2_31           get v2
00002BCA  E762 0000 0806                00000000   2241+         VL    V22,0(R2)
00002BD0  E666 0000 2C56                           2242+         VCLFNH V22,V22,2,0       test instruction (dest is source)
00002BD6  B29C 5040                     00002B70   2243+         STFPC FPC_R_31           save FPC
00002BDA  E760 5028 080E                00002B58   2244+         VST   V22,V1O31          save instruction result
00002BE0  07FB                                     2245+         BR    R11                return
00002BE4                                           2246+RE31     DS    0F                 expected 16 byte result
00002BE4                                           2247+         DROP  R5
00002BE4  4FFF8000 00000000                        2248          DC    XL16'4FFF8000000000000000000000000000'
00002BEC  00000000 00000000
00002BF4  7FFE0000 00000000                        2249          DC    XL16'7FFE0000000000000000000000000000'
00002BFC  00000000 00000000
                                                   2250
                                                   2251 * min  dlfloat: 2^(-31)*+ulp
                                                   2252          VRR_A VCLFNH,2,0,00,00,N
00002C08                                           2253+         DS    0FD
00002C08                        00002C08           2254+         USING *,R5               base for test data and test routine
00002C08  00002C98                                 2255+T32      DC    A(X32)             address of test routine
00002C0C  0020                                     2256+         DC    H'32'              test number
00002C0E  00                                       2257+         DC    X'00'
00002C0F  D5                                       2258+         DC    CL1'N'             Y = skip cross check
00002C10  02                                       2259+         DC    HL1'2'             m3
00002C11  00                                       2260+         DC    HL1'0'             m4
00002C12  00                                       2261+FLG32    DC    X'00'              expected FPC flags
00002C13  00                                       2262+VXC32    DC    X'00'              expected VXC
00002C14  00002CCC                                 2263+V2_32    DC    A(RE32+16)         address of v2: 16-byte packed decimal
00002C18  E5C3D3C6 D5C84040                        2264+         DC    CL8'VCLFNH'        instruction name
00002C20  00000010                                 2265+         DC    A(16)              result length
00002C24  00002CBC                                 2266+         DC    A(RE32)            address of expected resul
00002C28  00000000 00000000                        2267+         DS    FD                 gap
00002C30  00000000 00000000                        2268+V1O32    DS    XL16               V1 output
00002C38  00000000 00000000
00002C40  00000000 00000000                        2269+         DS    FD                    gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002C48  00000000                                 2270+FPC_R_32 DS    F                 FPC after instruction
00002C50  00000000 00000000                        2271+         DS    FD                   gap
00002C58  40404040 40404040                        2272+         DC    CL8' '            was cross check skipped?
00002C60  00000000 00000000                        2273+         DS    FD                   gap
00002C68  00000000 00000000                        2274+XCO32    DS    XL16              Cross check Output
00002C70  00000000 00000000
00002C78  00000000 00000000                        2275+         DS    FD                   gap
00002C80  00000000                                 2276+FPC_XC_32 DS   F                 FPC after cross check
00002C88  00000000 00000000                        2277+         DS    FD                   gap
00002C90  00000000                                 2278+         DS    F                 debug area
00002C94  00000000                                 2279+         DS    F
                                                   2280+*
00002C98                                           2281+X32      DS    0F
00002C98  B29D 85A4                     000007A4   2282+         LFPC  FPCMOFF           initialize FPC
00002C9C  E320 500C 0014                00002C14   2283+         LGF   R2,V2_32          get v2
00002CA2  E762 0000 0806                00000000   2284+         VL    V22,0(R2)
00002CA8  E666 0000 2C56                           2285+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002CAE  B29C 5040                     00002C48   2286+         STFPC FPC_R_32          save FPC
00002CB2  E760 5028 080E                00002C30   2287+         VST   V22,V1O32         save instruction result
00002CB8  07FB                                     2288+         BR    R11               return
00002CBC                                           2289+RE32     DS    0F                expected 16 byte result
00002CBC                                           2290+         DROP  R5
00002CBC  30004000 00000000                        2291          DC    XL16'30004000000000000000000000000000'
00002CC4  00000000 00000000
00002CCC  00010000 00000000                        2292          DC    XL16'00010000000000000000000000000000'
00002CD4  00000000 00000000
                                                   2293
                                                   2294 * +Infinity, -Infinity
                                                   2295          VRR_A VCLFNH,2,0,80,00,S              skip xcheck - infinity
00002CE0                                           2296+         DS    0FD
00002CE0                        00002CE0           2297+         USING *,R5              base for test data and test routine
00002CE0  00002D70                                 2298+T33      DC    A(X33)            address of test routine
00002CE4  0021                                     2299+         DC    H'33'             test number
00002CE6  00                                       2300+         DC    X'00'
00002CE7  E2                                       2301+         DC    CL1'S'            Y = skip cross check
00002CE8  02                                       2302+         DC    HL1'2'            m3
00002CE9  00                                       2303+         DC    HL1'0'            m4
00002CEA  80                                       2304+FLG33    DC    X'80'             expected FPC flags
00002CEB  00                                       2305+VXC33    DC    X'00'             expected VXC
00002CEC  00002DA4                                 2306+V2_33    DC    A(RE33+16)        address of v2: 16-byte packed decimal
00002CF0  E5C3D3C6 D5C84040                        2307+         DC    CL8'VCLFNH'       instruction name
00002CF8  00000010                                 2308+         DC    A(16)             result length
00002CFC  00002D94                                 2309+         DC    A(RE33)           address of expected resul
00002D00  00000000 00000000                        2310+         DS    FD                gap
00002D08  00000000 00000000                        2311+V1O33    DS    XL16              V1 output
00002D10  00000000 00000000
00002D18  00000000 00000000                        2312+         DS    FD                   gap
00002D20  00000000                                 2313+FPC_R_33 DS    F                 FPC after instruction
00002D28  00000000 00000000                        2314+         DS    FD                   gap
00002D30  40404040 40404040                        2315+         DC    CL8' '            was cross check skipped?
00002D38  00000000 00000000                        2316+         DS    FD                   gap
00002D40  00000000 00000000                        2317+XCO33    DS    XL16              Cross check Output
00002D48  00000000 00000000
00002D50  00000000 00000000                        2318+         DS    FD                   gap
00002D58  00000000                                 2319+FPC_XC_33 DS   F                 FPC after cross check
00002D60  00000000 00000000                        2320+         DS    FD                   gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002D68  00000000                                 2321+         DS    F                 debug area
00002D6C  00000000                                 2322+         DS    F
                                                   2323+*
00002D70                                           2324+X33      DS    0F
00002D70  B29D 85A4                     000007A4   2325+         LFPC  FPCMOFF           initialize FPC
00002D74  E320 500C 0014                00002CEC   2326+         LGF   R2,V2_33          get v2
00002D7A  E762 0000 0806                00000000   2327+         VL    V22,0(R2)
00002D80  E666 0000 2C56                           2328+         VCLFNH V22,V22,2,0      test instruction (dest is source)
00002D86  B29C 5040                     00002D20   2329+         STFPC FPC_R_33          save FPC
00002D8A  E760 5028 080E                00002D08   2330+         VST   V22,V1O33         save instruction result
00002D90  07FB                                     2331+         BR    R11               return
00002D94                                           2332+RE33     DS    0F                expected 16 byte result
00002D94                                           2333+         DROP  R5
00002D94  7FC00000 00000000                        2334          DC    XL16'7FC00000000000007FC0000000000000'
00002D9C  7FC00000 00000000
00002DA4  7FFF0000 FFFF0000                        2335          DC    XL16'7FFF0000FFFF00000000000000000000'
00002DAC  00000000 00000000
                                                   2336
                                                   2337 * inexact - bad m3
                                                   2338          VRR_A VCLFNH,5,0,08,00,S                skip xc - inexact
00002DB8                                           2339+         DS    0FD
00002DB8                        00002DB8           2340+         USING *,R5              base for test data and test routine
00002DB8  00002E48                                 2341+T34      DC    A(X34)            address of test routine
00002DBC  0022                                     2342+         DC    H'34'             test number
00002DBE  00                                       2343+         DC    X'00'
00002DBF  E2                                       2344+         DC    CL1'S'            Y = skip cross check
00002DC0  05                                       2345+         DC    HL1'5'            m3
00002DC1  00                                       2346+         DC    HL1'0'            m4
00002DC2  08                                       2347+FLG34    DC    X'08'             expected FPC flags
00002DC3  00                                       2348+VXC34    DC    X'00'             expected VXC
00002DC4  00002E7C                                 2349+V2_34    DC    A(RE34+16)        address of v2: 16-byte packed decimal
00002DC8  E5C3D3C6 D5C84040                        2350+         DC    CL8'VCLFNH'       instruction name
00002DD0  00000010                                 2351+         DC    A(16)             result length
00002DD4  00002E6C                                 2352+         DC    A(RE34)           address of expected resul
00002DD8  00000000 00000000                        2353+         DS    FD                gap
00002DE0  00000000 00000000                        2354+V1O34    DS    XL16              V1 output
00002DE8  00000000 00000000
00002DF0  00000000 00000000                        2355+         DS    FD                   gap
00002DF8  00000000                                 2356+FPC_R_34 DS    F                 FPC after instruction
00002E00  00000000 00000000                        2357+         DS    FD                   gap
00002E08  40404040 40404040                        2358+         DC    CL8' '            was cross check skipped?
00002E10  00000000 00000000                        2359+         DS    FD                   gap
00002E18  00000000 00000000                        2360+XCO34    DS    XL16              Cross check Output
00002E20  00000000 00000000
00002E28  00000000 00000000                        2361+         DS    FD                   gap
00002E30  00000000                                 2362+FPC_XC_34 DS   F                 FPC after cross check
00002E38  00000000 00000000                        2363+         DS    FD                   gap
00002E40  00000000                                 2364+         DS    F                 debug area
00002E44  00000000                                 2365+         DS    F
                                                   2366+*
00002E48                                           2367+X34      DS    0F
00002E48  B29D 85A4                     000007A4   2368+         LFPC  FPCMOFF           initialize FPC
00002E4C  E320 500C 0014                00002DC4   2369+         LGF   R2,V2_34          get v2
00002E52  E762 0000 0806                00000000   2370+         VL    V22,0(R2)
00002E58  E666 0000 5C56                           2371+         VCLFNH V22,V22,5,0      test instruction (dest is source)
00002E5E  B29C 5040                     00002DF8   2372+         STFPC FPC_R_34          save FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002E62  E760 5028 080E                00002DE0  2373+          VST   V22,V1O34         save instruction result
00002E68  07FB                                    2374+          BR    R11               return
00002E6C                                          2375+RE34      DS    0F                expected 16 byte result
00002E6C                                          2376+          DROP  R5
00002E6C  00000000 00000000                       2377           DC    XL16'00000000000000000000000000000000'
00002E74  00000000 00000000
00002E7C  00010000 00000000                       2378           DC    XL16'00010000000000000000000000000F000'
00002E84  00000000 0000F000
                                                  2379
                                                  2380 * inexact - bad m4
                                                  2381           VRR_A VCLFNH,2,5,08,00,S                    skip xc - inexact
00002E90                                          2382+          DS    0FD
00002E90                        00002E90          2383+          USING *,R5              base for test data and test routine
00002E90  00002F20                                2384+T35       DC    A(X35)            address of test routine
00002E94  0023                                    2385+          DC    H'35'             test number
00002E96  00                                      2386+          DC    X'00'
00002E97  E2                                      2387+          DC    CL1'S'            Y = skip cross check
00002E98  02                                      2388+          DC    HL1'2'            m3
00002E99  05                                      2389+          DC    HL1'5'            m4
00002E9A  08                                      2390+FLG35     DC    X'08'             expected FPC flags
00002E9B  00                                      2391+VXC35     DC    X'00'             expected VXC
00002E9C  00002F54                                2392+V2_35     DC    A(RE35+16)        address of v2: 16-byte packed decimal
00002EA0  E5C3D3C6 D5C84040                       2393+          DC    CL8'VCLFNH'       instruction name
00002EA8  00000010                                2394+          DC    A(16)             result length
00002EAC  00002F44                                2395+          DC    A(RE35)           address of expected resul
00002EB0  00000000 00000000                       2396+          DS    FD                gap
00002EB8  00000000 00000000                       2397+V1O35     DS    XL16              V1 output
00002EC0  00000000 00000000
00002EC8  00000000 00000000                       2398+          DS    FD                   gap
00002ED0  00000000                                2399+FPC_R_35  DS    F                 FPC after instruction
00002ED8  00000000 00000000                       2400+          DS    FD                   gap
00002EE0  40404040 40404040                       2401+          DC    CL8' '            was cross check skipped?
00002EE8  00000000 00000000                       2402+          DS    FD                   gap
00002EF0  00000000 00000000                       2403+XCO35     DS    XL16              Cross check Output
00002EF8  00000000 00000000
00002F00  00000000 00000000                       2404+          DS    FD                   gap
00002F08  00000000                                2405+FPC_XC_35 DS    F                 FPC after cross check
00002F10  00000000 00000000                       2406+          DS    FD                   gap
00002F18  00000000                                2407+          DS    F                 debug area
00002F1C  00000000                                2408+          DS    F
                                                  2409+*
00002F20                                          2410+X35       DS    0F
00002F20  B29D 85A4                     000007A4  2411+          LFPC  FPCMOFF           initialize FPC
00002F24  E320 500C 0014                00002E9C  2412+          LGF   R2,V2_35          get v2
00002F2A  E762 0000 0806                00000000  2413+          VL    V22,0(R2)
00002F30  E666 0005 2C56                          2414+          VCLFNH V22,V22,2,5      test instruction (dest is source)
00002F36  B29C 5040                     00002ED0  2415+          STFPC FPC_R_35          save FPC
00002F3A  E760 5028 080E                00002EB8  2416+          VST   V22,V1O35         save instruction result
00002F40  07FB                                    2417+          BR    R11               return
00002F44                                          2418+RE35      DS    0F                expected 16 byte result
00002F44                                          2419+          DROP  R5
00002F44  00000000 00000000                       2420           DC    XL16'00000000000000000000000000000000'
00002F4C  00000000 00000000
00002F54  00010000 00000000                       2421           DC    XL16'00010000000000000000000000000F000'
00002F5C  00000000 0000F000
                                                  2422
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2423 * more tests
                                                   2424 * +3.140625, -3.140625
                                                   2425          VRR_A VCLFNH,2,0,00,00,N
00002F68                                           2426+         DS    0FD
00002F68                       00002F68            2427+         USING *,R5              base for test data and test routine
00002F68  00002FF8                                 2428+T36      DC    A(X36)            address of test routine
00002F6C  0024                                     2429+         DC    H'36'             test number
00002F6E  00                                       2430+         DC    X'00'
00002F6F  D5                                       2431+         DC    CL1'N'            Y = skip cross check
00002F70  02                                       2432+         DC    HL1'2'            m3
00002F71  00                                       2433+         DC    HL1'0'            m4
00002F72  00                                       2434+FLG36    DC    X'00'             expected FPC flags
00002F73  00                                       2435+VXC36    DC    X'00'             expected VXC
00002F74  0000302C                                 2436+V2_36    DC    A(RE36+16)        address of v2: 16-byte packed decimal
00002F78  E5C3D3C6 D5C84040                        2437+         DC    CL8'VCLFNH'       instruction name
00002F80  00000010                                 2438+         DC    A(16)             result length
00002F84  0000301C                                 2439+         DC    A(RE36)           address of expected resul
00002F88  00000000 00000000                        2440+         DS    FD                gap
00002F90  00000000 00000000                        2441+V1O36    DS    XL16              V1 output
00002F98  00000000 00000000
00002FA0  00000000 00000000                        2442+         DS    FD                   gap
00002FA8  00000000                                 2443+FPC_R_36 DS    F                 FPC after instruction
00002FB0  00000000 00000000                        2444+         DS    FD                   gap
00002FB8  40404040 40404040                        2445+         DC    CL8' '            was cross check skipped?
00002FC0  00000000 00000000                        2446+         DS    FD                   gap
00002FC8  00000000 00000000                        2447+XCO36    DS    XL16              Cross check Output
00002FD0  00000000 00000000
00002FD8  00000000 00000000                        2448+         DS    FD                   gap
00002FE0  00000000                                 2449+FPC_XC_36 DS   F                 FPC after cross check
00002FE8  00000000 00000000                        2450+         DS    FD                   gap
00002FF0  00000000                                 2451+         DS    F                 debug area
00002FF4  00000000                                 2452+         DS    F
                                                   2453+*
00002FF8                                           2454+X36      DS    0F
00002FF8  B29D 85A4                    000007A4    2455+         LFPC  FPCMOFF           initialize FPC
00002FFC  E320 500C 0014               00002F74    2456+         LGF   R2,V2_36          get v2
00003002  E762 0000 0806               00000000    2457+         VL    V22,0(R2)
00003008  E666 0000 2C56                           2458+         VCLFNH V22,V22,2,0      test instruction (dest is source)
0000300E  B29C 5040                    00002FA8    2459+         STFPC FPC_R_36          save FPC
00003012  E760 5028 080E               00002F90    2460+         VST   V22,V1O36         save instruction result
00003018  07FB                                     2461+         BR    R11               return
0000301C                                           2462+RE36     DS    0F                expected 16 byte result
0000301C                                           2463+         DROP  R5
0000301C  40890000 00000000                        2464          DC    XL16'4089000000000000C089000000000000'
00003024  C0890000 00000000
0000302C  42240000 C2240000                        2465          DC    XL16'42240000C224000000000000000000'
00003034  00000000 00000000
                                                   2466
                                                   2467
                                                   2468 * +27.15625, -27.15625
                                                   2469          VRR_A VCLFNH,2,0,00,00,N
00003040                                           2470+         DS    0FD
00003040                       00003040            2471+         USING *,R5              base for test data and test routine
00003040  000030D0                                 2472+T37      DC    A(X37)            address of test routine
00003044  0025                                     2473+         DC    H'37'             test number
00003046  00                                       2474+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003047  D5                                       2475+          DC    CL1'N'            Y = skip cross check
00003048  02                                       2476+          DC    HL1'2'            m3
00003049  00                                       2477+          DC    HL1'0'            m4
0000304A  00                                       2478+FLG37     DC    X'00'             expected FPC flags
0000304B  00                                       2479+VXC37     DC    X'00'             expected VXC
0000304C  00003104                                 2480+V2_37     DC    A(RE37+16)        address of v2: 16-byte packed decimal
00003050  E5C3D3C6 D5C84040                        2481+          DC    CL8'VCLFNH'       instruction name
00003058  00000010                                 2482+          DC    A(16)             result length
0000305C  000030F4                                 2483+          DC    A(RE37)           address of expected resul
00003060  00000000 00000000                        2484+          DS    FD                gap
00003068  00000000 00000000                        2485+V1O37     DS    XL16              V1 output
00003070  00000000 00000000
00003078  00000000 00000000                        2486+          DS    FD                   gap
00003080  00000000                                 2487+FPC_R_37  DS    F                 FPC after instruction
00003088  00000000 00000000                        2488+          DS    FD                   gap
00003090  40404040 40404040                        2489+          DC    CL8' '            was cross check skipped?
00003098  00000000 00000000                        2490+          DS    FD                   gap
000030A0  00000000 00000000                        2491+XCO37     DS    XL16              Cross check Output
000030A8  00000000 00000000
000030B0  00000000 00000000                        2492+          DS    FD                   gap
000030B8  00000000                                 2493+FPC_XC_37 DS    F                 FPC after cross check
000030C0  00000000 00000000                        2494+          DS    FD                   gap
000030C8  00000000                                 2495+          DS    F                 debug area
000030CC  00000000                                 2496+          DS    F
                                                   2497+*
000030D0                                           2498+X37       DS    0F
000030D0  B29D 85A4                     000007A4   2499+          LFPC  FPCMOFF           initialize FPC
000030D4  E320 500C 0014                0000304C   2500+          LGF   R2,V2_37          get v2
000030DA  E762 0000 0806                00000000   2501+          VL    V22,0(R2)
000030E0  E666 0000 2C56                           2502+          VCLFNH V22,V22,2,0      test instruction (dest is source)
000030E6  B29C 5040                     00003080   2503+          STFPC FPC_R_37          save FPC
000030EA  E760 5028 080E                00003068   2504+          VST   V22,V1O37         save instruction result
000030F0  07FB                                     2505+          BR    R11               return
000030F4                                           2506+RE37      DS    0F                expected 16 byte result
000030F4                                           2507+          DROP  R5
000030F4  3BD94000 00000000                        2508           DC    XL16'3BD9400000000000BBD9400000000000'
000030FC  BBD94000 00000000
00003104  2F650000 AF650000                        2509           DC    XL16'2F650000AF650000000000000000000'
0000310C  00000000 00000000
                                                   2510
                                                   2511 * +65504, -65504
                                                   2512           VRR_A VCLFNH,2,0,00,00,N
00003118                                           2513+          DS    0FD
00003118                        00003118           2514+          USING *,R5              base for test data and test routine
00003118  000031A8                                 2515+T38       DC    A(X38)            address of test routine
0000311C  0026                                     2516+          DC    H'38'             test number
0000311E  00                                       2517+          DC    X'00'
0000311F  D5                                       2518+          DC    CL1'N'            Y = skip cross check
00003120  02                                       2519+          DC    HL1'2'            m3
00003121  00                                       2520+          DC    HL1'0'            m4
00003122  00                                       2521+FLG38     DC    X'00'             expected FPC flags
00003123  00                                       2522+VXC38     DC    X'00'             expected VXC
00003124  000031DC                                 2523+V2_38     DC    A(RE38+16)        address of v2: 16-byte packed decimal
00003128  E5C3D3C6 D5C84040                        2524+          DC    CL8'VCLFNH'       instruction name
00003130  00000010                                 2525+          DC    A(16)             result length
00003134  000031CC                                 2526+          DC    A(RE38)           address of expected resul
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003138  00000000 00000000                        2527+          DS    FD                 gap
00003140  00000000 00000000                        2528+V1O38     DS    XL16               V1 output
00003148  00000000 00000000
00003150  00000000 00000000                        2529+          DS    FD                    gap
00003158  00000000                                 2530+FPC_R_38  DS    F                  FPC after instruction
00003160  00000000 00000000                        2531+          DS    FD                    gap
00003168  40404040 40404040                        2532+          DC    CL8' '             was cross check skipped?
00003170  00000000 00000000                        2533+          DS    FD                    gap
00003178  00000000 00000000                        2534+XCO38     DS    XL16               Cross check Output
00003180  00000000 00000000
00003188  00000000 00000000                        2535+          DS    FD                    gap
00003190  00000000                                 2536+FPC_XC_38 DS    F                  FPC after cross check
00003198  00000000 00000000                        2537+          DS    FD                    gap
000031A0  00000000                                 2538+          DS    F                  debug area
000031A4  00000000                                 2539+          DS    F
                                                   2540+*
000031A8                                           2541+X38       DS    0F
000031A8  B29D 85A4                     000007A4   2542+          LFPC  FPCMOFF            initialize FPC
000031AC  E320 500C 0014                00003124   2543+          LGF   R2,V2_38           get v2
000031B2  E762 0000 0806                00000000   2544+          VL    V22,0(R2)
000031B8  E666 0000 2C56                           2545+          VCLFNH V22,V22,2,0       test instruction (dest is source)
000031BE  B29C 5040                     00003158   2546+          STFPC FPC_R_38           save FPC
000031C2  E760 5028 080E                00003140   2547+          VST   V22,V1O38          save instruction result
000031C8  07FB                                     2548+          BR    R11                return
000031CC                                           2549+RE38      DS    0F                 expected 16 byte result
000031CC                                           2550+          DROP  R5
000031CC  47800000 00000000                        2551           DC    XL16'4780000000000000C780000000000000'
000031D4  C7800000 00000000
000031DC  5E000000 DE000000                        2552           DC    XL16'5E000000DE000000000000000000000000'
000031E4  00000000 00000000
                                                   2553
                                                   2554 * +Normal, -Normal (2.5)
                                                   2555           VRR_A VCLFNH,2,0,00,00,N
000031F0                                           2556+          DS    0FD
000031F0                        000031F0           2557+          USING *,R5               base for test data and test routine
000031F0  00003280                                 2558+T39       DC    A(X39)             address of test routine
000031F4  0027                                     2559+          DC    H'39'              test number
000031F6  00                                       2560+          DC    X'00'
000031F7  D5                                       2561+          DC    CL1'N'             Y = skip cross check
000031F8  02                                       2562+          DC    HL1'2'             m3
000031F9  00                                       2563+          DC    HL1'0'             m4
000031FA  00                                       2564+FLG39     DC    X'00'              expected FPC flags
000031FB  00                                       2565+VXC39     DC    X'00'              expected VXC
000031FC  000032B4                                 2566+V2_39     DC    A(RE39+16)         address of v2: 16-byte packed decimal
00003200  E5C3D3C6 D5C84040                        2567+          DC    CL8'VCLFNH'        instruction name
00003208  00000010                                 2568+          DC    A(16)              result length
0000320C  000032A4                                 2569+          DC    A(RE39)            address of expected resul
00003210  00000000 00000000                        2570+          DS    FD                 gap
00003218  00000000 00000000                        2571+V1O39     DS    XL16               V1 output
00003220  00000000 00000000
00003228  00000000 00000000                        2572+          DS    FD                    gap
00003230  00000000                                 2573+FPC_R_39  DS    F                  FPC after instruction
00003238  00000000 00000000                        2574+          DS    FD                    gap
00003240  40404040 40404040                        2575+          DC    CL8' '             was cross check skipped?
00003248  00000000 00000000                        2576+          DS    FD                    gap
00003250  00000000 00000000                        2577+XCO39     DS    XL16               Cross check Output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00003258  00000000 00000000
00003260  00000000 00000000                        2578+          DS    FD                   gap
00003268  00000000                                 2579+FPC_XC_39 DS    F                 FPC after cross check
00003270  00000000 00000000                        2580+          DS    FD                   gap
00003278  00000000                                 2581+          DS    F                 debug area
0000327C  00000000                                 2582+          DS    F
                                                   2583+*
00003280                                           2584+X39       DS    0F
00003280  B29D 85A4                     000007A4   2585+          LFPC  FPCMOFF           initialize FPC
00003284  E320 500C 0014                000031FC   2586+          LGF   R2,V2_39          get v2
0000328A  E762 0000 0806                00000000   2587+          VL    V22,0(R2)
00003290  E666 0000 2C56                           2588+          VCLFNH V22,V22,2,0      test instruction (dest is source)
00003296  B29C 5040                     00003230   2589+          STFPC FPC_R_39          save FPC
0000329A  E760 5028 080E                00003218   2590+          VST   V22,V1O39         save instruction result
000032A0  07FB                                     2591+          BR    R11               return
000032A4                                           2592+RE39      DS    0F                expected 16 byte result
000032A4                                           2593+          DROP  R5
000032A4  40200000 00000000                        2594           DC    XL16'4020000000000000C020000000000000'
000032AC  C0200000 00000000
000032B4  40800000 C0800000                        2595           DC    XL16'40800000C0800000000000000000000'
000032BC  00000000 00000000
                                                   2596
                                                   2597 * +0.00006097, -0.00006097 (about)
                                                   2598           VRR_A VCLFNH,2,0,00,00,N
000032C8                                           2599+          DS    0FD
000032C8                        000032C8           2600+          USING *,R5              base for test data and test routine
000032C8  00003358                                 2601+T40       DC    A(X40)            address of test routine
000032CC  0028                                     2602+          DC    H'40'             test number
000032CE  00                                       2603+          DC    X'00'
000032CF  D5                                       2604+          DC    CL1'N'            Y = skip cross check
000032D0  02                                       2605+          DC    HL1'2'            m3
000032D1  00                                       2606+          DC    HL1'0'            m4
000032D2  00                                       2607+FLG40     DC    X'00'             expected FPC flags
000032D3  00                                       2608+VXC40     DC    X'00'             expected VXC
000032D4  0000338C                                 2609+V2_40     DC    A(RE40+16)        address of v2: 16-byte packed decimal
000032D8  E5C3D3C6 D5C84040                        2610+          DC    CL8'VCLFNH'       instruction name
000032E0  00000010                                 2611+          DC    A(16)             result length
000032E4  0000337C                                 2612+          DC    A(RE40)           address of expected resul
000032E8  00000000 00000000                        2613+          DS    FD                gap
000032F0  00000000 00000000                        2614+V1O40     DS    XL16              V1 output
000032F8  00000000 00000000
00003300  00000000 00000000                        2615+          DS    FD                   gap
00003308  00000000                                 2616+FPC_R_40  DS    F                 FPC after instruction
00003310  00000000 00000000                        2617+          DS    FD                   gap
00003318  40404040 40404040                        2618+          DC    CL8' '            was cross check skipped?
00003320  00000000 00000000                        2619+          DS    FD                   gap
00003328  00000000 00000000                        2620+XCO40     DS    XL16              Cross check Output
00003330  00000000 00000000
00003338  00000000 00000000                        2621+          DS    FD                   gap
00003340  00000000                                 2622+FPC_XC_40 DS    F                 FPC after cross check
00003348  00000000 00000000                        2623+          DS    FD                   gap
00003350  00000000                                 2624+          DS    F                 debug area
00003354  00000000                                 2625+          DS    F
                                                   2626+*
00003358                                           2627+X40       DS    0F
00003358  B29D 85A4                     000007A4   2628+          LFPC  FPCMOFF           initialize FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000335C  E320 500C 0014                 000032D4  2629+         LGF   R2,V2_40          get v2
00003362  E762 0000 0806                 00000000  2630+         VL    V22,0(R2)
00003368  E666 0000 2C56                           2631+         VCLFNH V22,V22,2,0       test instruction (dest is source)
0000336E  B29C 5040                      00003308  2632+         STFPC FPC_R_40           save FPC
00003372  E760 5028 080E                 000032F0  2633+         VST   V22,V1O40          save instruction result
00003378  07FB                                     2634+         BR    R11                return
0000337C                                           2635+RE40     DS    0F                 expected 16 byte result
0000337C                                           2636+         DROP  R5
0000337C  387FC000 00000000                        2637          DC    XL16'387FC00000000000B87FC00000000000'
00003384  B87FC000 00000000
0000338C  21FF0000 A1FF0000                        2638          DC    XL16'21FF0000A1FF00000000000000000000'
00003394  00000000 00000000
                                                   2639
                                                   2640 *-----------------------------------------------------------------
                                                   2641 *  VCFN     - VECTOR FP CONVERT FROM NNP
                                                   2642 *-----------------------------------------------------------------
                                                   2643 *  dlfloat -> tiny float (with cross check: tiny float -> dlfloat)
                                                   2644 *
                                                   2645
                                                   2646 * +0, -0     simple instruction and 'test' test
                                                   2647          VRR_A VCFN,1,0,00,00,N
000033A0                                           2648+         DS    0FD
000033A0                         000033A0          2649+         USING *,R5               base for test data and test routine
000033A0  00003430                                 2650+T41      DC    A(X41)             address of test routine
000033A4  0029                                     2651+         DC    H'41'              test number
000033A6  00                                       2652+         DC    X'00'
000033A7  D5                                       2653+         DC    CL1'N'             Y = skip cross check
000033A8  01                                       2654+         DC    HL1'1'             m3
000033A9  00                                       2655+         DC    HL1'0'             m4
000033AA  00                                       2656+FLG41    DC    X'00'              expected FPC flags
000033AB  00                                       2657+VXC41    DC    X'00'              expected VXC
000033AC  00003464                                 2658+V2_41    DC    A(RE41+16)         address of v2: 16-byte packed decimal
000033B0  E5C3C6D5 40404040                        2659+         DC    CL8'VCFN'          instruction name
000033B8  00000010                                 2660+         DC    A(16)              result length
000033BC  00003454                                 2661+         DC    A(RE41)            address of expected resul
000033C0  00000000 00000000                        2662+         DS    FD                 gap
000033C8  00000000 00000000                        2663+V1O41    DS    XL16               V1 output
000033D0  00000000 00000000
000033D8  00000000 00000000                        2664+         DS    FD                    gap
000033E0  00000000                                 2665+FPC_R_41 DS    F                  FPC after instruction
000033E8  00000000 00000000                        2666+         DS    FD                    gap
000033F0  40404040 40404040                        2667+         DC    CL8' '             was cross check skipped?
000033F8  00000000 00000000                        2668+         DS    FD                    gap
00003400  00000000 00000000                        2669+XCO41    DS    XL16               Cross check Output
00003408  00000000 00000000
00003410  00000000 00000000                        2670+         DS    FD                    gap
00003418  00000000                                 2671+FPC_XC_41 DS   F                  FPC after cross check
00003420  00000000 00000000                        2672+         DS    FD                    gap
00003428  00000000                                 2673+         DS    F                  debug area
0000342C  00000000                                 2674+         DS    F
                                                   2675+*
00003430                                           2676+X41      DS    0F
00003430  B29D 85A4                      000007A4  2677+         LFPC  FPCMOFF            initialize FPC
00003434  E320 500C 0014                 000033AC  2678+         LGF   R2,V2_41           get v2
0000343A  E762 0000 0806                 00000000  2679+         VL    V22,0(R2)
00003440  E666 0000 1C5D                           2680+         VCFN  V22,V22,1,0        test instruction (dest is source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003446  B29C 5040                     000033E0  2681+         STFPC FPC_R_41          save FPC
0000344A  E760 5028 080E                000033C8  2682+         VST   V22,V1O41         save instruction result
00003450  07FB                                    2683+         BR    R11               return
00003454                                          2684+RE41     DS    0F                expected 16 byte result
00003454                                          2685+         DROP  R5
00003454  00008000 00000000                       2686          DC    XL16'00008000000000000000000000000000'
0000345C  00000000 00000000
00003464  00008000 00000000                       2687          DC    XL16'00008000000000000000000000000000'
0000346C  00000000 00000000
                                                  2688
                                                  2689 * 1.0, -1
                                                  2690          VRR_A VCFN,1,0,00,00,N
00003478                                          2691+         DS    0FD
00003478                        00003478          2692+         USING *,R5              base for test data and test routine
00003478  00003508                                2693+T42      DC    A(X42)            address of test routine
0000347C  002A                                    2694+         DC    H'42'             test number
0000347E  00                                      2695+         DC    X'00'
0000347F  D5                                      2696+         DC    CL1'N'            Y = skip cross check
00003480  01                                      2697+         DC    HL1'1'            m3
00003481  00                                      2698+         DC    HL1'0'            m4
00003482  00                                      2699+FLG42    DC    X'00'             expected FPC flags
00003483  00                                      2700+VXC42    DC    X'00'             expected VXC
00003484  0000353C                                2701+V2_42    DC    A(RE42+16)        address of v2: 16-byte packed decimal
00003488  E5C3C6D5 40404040                       2702+         DC    CL8'VCFN'         instruction name
00003490  00000010                                2703+         DC    A(16)             result length
00003494  0000352C                                2704+         DC    A(RE42)           address of expected resul
00003498  00000000 00000000                       2705+         DS    FD                gap
000034A0  00000000 00000000                       2706+V1O42    DS    XL16              V1 output
000034A8  00000000 00000000
000034B0  00000000 00000000                       2707+         DS    FD                   gap
000034B8  00000000                                2708+FPC_R_42 DS    F                 FPC after instruction
000034C0  00000000 00000000                       2709+         DS    FD                   gap
000034C8  40404040 40404040                       2710+         DC    CL8' '            was cross check skipped?
000034D0  00000000 00000000                       2711+         DS    FD                   gap
000034D8  00000000 00000000                       2712+XCO42    DS    XL16              Cross check Output
000034E0  00000000 00000000
000034E8  00000000 00000000                       2713+         DS    FD                   gap
000034F0  00000000                                2714+FPC_XC_42 DS   F                 FPC after cross check
000034F8  00000000 00000000                       2715+         DS    FD                   gap
00003500  00000000                                2716+         DS    F                 debug area
00003504  00000000                                2717+         DS    F
                                                  2718+*
00003508                                          2719+X42      DS    0F
00003508  B29D 85A4                     000007A4  2720+         LFPC  FPCMOFF           initialize FPC
0000350C  E320 500C 0014                00003484  2721+         LGF   R2,V2_42          get v2
00003512  E762 0000 0806                00000000  2722+         VL    V22,0(R2)
00003518  E666 0000 1C5D                          2723+         VCFN  V22,V22,1,0       test instruction (dest is source)
0000351E  B29C 5040                     000034B8  2724+         STFPC FPC_R_42          save FPC
00003522  E760 5028 080E                000034A0  2725+         VST   V22,V1O42         save instruction result
00003528  07FB                                    2726+         BR    R11               return
0000352C                                          2727+RE42     DS    0F                expected 16 byte result
0000352C                                          2728+         DROP  R5
0000352C  3C000000 BC000000                       2729          DC    XL16'3C000000BC00000000000000000F000'
00003534  00000000 0000F000
0000353C  3E000000 BE000000                       2730          DC    XL16'3E000000BE00000000000000000D800'
00003544  00000000 0000D800
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2731
                                                   2732 * 0.5
                                                   2733          VRR_A VCFN,1,0,00,00,N
00003550                                           2734+         DS    0FD
00003550                       00003550            2735+         USING *,R5              base for test data and test routine
00003550  000035E0                                 2736+T43      DC    A(X43)            address of test routine
00003554  002B                                     2737+         DC    H'43'             test number
00003556  00                                       2738+         DC    X'00'
00003557  D5                                       2739+         DC    CL1'N'            Y = skip cross check
00003558  01                                       2740+         DC    HL1'1'            m3
00003559  00                                       2741+         DC    HL1'0'            m4
0000355A  00                                       2742+FLG43    DC    X'00'             expected FPC flags
0000355B  00                                       2743+VXC43    DC    X'00'             expected VXC
0000355C  00003614                                 2744+V2_43    DC    A(RE43+16)        address of v2: 16-byte packed decimal
00003560  E5C3C6D5 40404040                        2745+         DC    CL8'VCFN'         instruction name
00003568  00000010                                 2746+         DC    A(16)             result length
0000356C  00003604                                 2747+         DC    A(RE43)           address of expected resul
00003570  00000000 00000000                        2748+         DS    FD                gap
00003578  00000000 00000000                        2749+V1O43    DS    XL16              V1 output
00003580  00000000 00000000
00003588  00000000 00000000                        2750+         DS    FD                   gap
00003590  00000000                                 2751+FPC_R_43 DS    F                 FPC after instruction
00003598  00000000 00000000                        2752+         DS    FD                   gap
000035A0  40404040 40404040                        2753+         DC    CL8' '            was cross check skipped?
000035A8  00000000 00000000                        2754+         DS    FD                   gap
000035B0  00000000 00000000                        2755+XCO43    DS    XL16              Cross check Output
000035B8  00000000 00000000
000035C0  00000000 00000000                        2756+         DS    FD                   gap
000035C8  00000000                                 2757+FPC_XC_43 DS   F                 FPC after cross check
000035D0  00000000 00000000                        2758+         DS    FD                   gap
000035D8  00000000                                 2759+         DS    F                 debug area
000035DC  00000000                                 2760+         DS    F
                                                   2761+*
000035E0                                           2762+X43      DS    0F
000035E0  B29D 85A4                     000007A4   2763+         LFPC  FPCMOFF           initialize FPC
000035E4  E320 500C 0014                0000355C   2764+         LGF   R2,V2_43          get v2
000035EA  E762 0000 0806                00000000   2765+         VL    V22,0(R2)
000035F0  E666 0000 1C5D                           2766+         VCFN  V22,V22,1,0       test instruction (dest is source)
000035F6  B29C 5040                     00003590   2767+         STFPC FPC_R_43          save FPC
000035FA  E760 5028 080E                00003578   2768+         VST   V22,V1O43         save instruction result
00003600  07FB                                     2769+         BR    R11               return
00003604                                           2770+RE43     DS    0F                expected 16 byte result
00003604                                           2771+         DROP  R5
00003604  38000000 00000000                        2772          DC    XL16'380000000000000000000000000F000'
0000360C  00000000 0000F000
00003614  3C000000 00000000                        2773          DC    XL16'3C000000000000000000000000D800'
0000361C  00000000 0000D800
                                                   2774
                                                   2775 * 1/64
                                                   2776          VRR_A VCFN,1,0,00,00,N
00003628                                           2777+         DS    0FD
00003628                       00003628            2778+         USING *,R5              base for test data and test routine
00003628  000036B8                                 2779+T44      DC    A(X44)            address of test routine
0000362C  002C                                     2780+         DC    H'44'             test number
0000362E  00                                       2781+         DC    X'00'
0000362F  D5                                       2782+         DC    CL1'N'            Y = skip cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003630  01                                       2783+         DC    HL1'1'            m3
00003631  00                                       2784+         DC    HL1'0'            m4
00003632  00                                       2785+FLG44    DC    X'00'             expected FPC flags
00003633  00                                       2786+VXC44    DC    X'00'             expected VXC
00003634  000036EC                                 2787+V2_44    DC    A(RE44+16)        address of v2: 16-byte packed decimal
00003638  E5C3C6D5 40404040                        2788+         DC    CL8'VCFN'         instruction name
00003640  00000010                                 2789+         DC    A(16)             result length
00003644  000036DC                                 2790+         DC    A(RE44)           address of expected resul
00003648  00000000 00000000                        2791+         DS    FD                gap
00003650  00000000 00000000                        2792+V1O44    DS    XL16              V1 output
00003658  00000000 00000000
00003660  00000000 00000000                        2793+         DS    FD                   gap
00003668  00000000                                 2794+FPC_R_44 DS    F                 FPC after instruction
00003670  00000000 00000000                        2795+         DS    FD                   gap
00003678  40404040 40404040                        2796+         DC    CL8' '            was cross check skipped?
00003680  00000000 00000000                        2797+         DS    FD                   gap
00003688  00000000 00000000                        2798+XCO44    DS    XL16              Cross check Output
00003690  00000000 00000000
00003698  00000000 00000000                        2799+         DS    FD                   gap
000036A0  00000000                                 2800+FPC_XC_44 DS   F                 FPC after cross check
000036A8  00000000 00000000                        2801+         DS    FD                   gap
000036B0  00000000                                 2802+         DS    F                 debug area
000036B4  00000000                                 2803+         DS    F
                                                   2804+*
000036B8                                           2805+X44      DS    0F
000036B8  B29D 85A4                     000007A4   2806+         LFPC  FPCMOFF           initialize FPC
000036BC  E320 500C 0014                00003634   2807+         LGF   R2,V2_44          get v2
000036C2  E762 0000 0806                00000000   2808+         VL    V22,0(R2)
000036C8  E666 0000 1C5D                           2809+         VCFN  V22,V22,1,0       test instruction (dest is source)
000036CE  B29C 5040                     00003668   2810+         STFPC FPC_R_44          save FPC
000036D2  E760 5028 080E                00003650   2811+         VST   V22,V1O44         save instruction result
000036D8  07FB                                     2812+         BR    R11               return
000036DC                                           2813+RE44     DS    0F                expected 16 byte result
000036DC                                           2814+         DROP  R5
000036DC  24000000 00000000                        2815          DC    XL16'24000000000000000000000000000F000'
000036E4  00000000 0000F000
000036EC  32000000 00000000                        2816          DC    XL16'32000000000000000000000000000D800'
000036F4  00000000 0000D800
                                                   2817
                                                   2818 * +0, -0
                                                   2819          VRR_A VCFN,1,0,00,00,N
00003700                                           2820+         DS    0FD
00003700                        00003700           2821+         USING *,R5              base for test data and test routine
00003700  00003790                                 2822+T45      DC    A(X45)            address of test routine
00003704  002D                                     2823+         DC    H'45'             test number
00003706  00                                       2824+         DC    X'00'
00003707  D5                                       2825+         DC    CL1'N'            Y = skip cross check
00003708  01                                       2826+         DC    HL1'1'            m3
00003709  00                                       2827+         DC    HL1'0'            m4
0000370A  00                                       2828+FLG45    DC    X'00'             expected FPC flags
0000370B  00                                       2829+VXC45    DC    X'00'             expected VXC
0000370C  000037C4                                 2830+V2_45    DC    A(RE45+16)        address of v2: 16-byte packed decimal
00003710  E5C3C6D5 40404040                        2831+         DC    CL8'VCFN'         instruction name
00003718  00000010                                 2832+         DC    A(16)             result length
0000371C  000037B4                                 2833+         DC    A(RE45)           address of expected resul
00003720  00000000 00000000                        2834+         DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003728  00000000 00000000                        2835+V1O45    DS    XL16              V1 output
00003730  00000000 00000000
00003738  00000000 00000000                        2836+         DS    FD                   gap
00003740  00000000                                 2837+FPC_R_45 DS    F                 FPC after instruction
00003748  00000000 00000000                        2838+         DS    FD                   gap
00003750  40404040 40404040                        2839+         DC    CL8' '            was cross check skipped?
00003758  00000000 00000000                        2840+         DS    FD                   gap
00003760  00000000 00000000                        2841+XCO45    DS    XL16              Cross check Output
00003768  00000000 00000000
00003770  00000000 00000000                        2842+         DS    FD                   gap
00003778  00000000                                 2843+FPC_XC_45 DS   F                 FPC after cross check
00003780  00000000 00000000                        2844+         DS    FD                   gap
00003788  00000000                                 2845+         DS    F                 debug area
0000378C  00000000                                 2846+         DS    F
                                                   2847+*
00003790                                           2848+X45      DS    0F
00003790  B29D 85A4                     000007A4   2849+         LFPC  FPCMOFF           initialize FPC
00003794  E320 500C 0014                0000370C   2850+         LGF   R2,V2_45          get v2
0000379A  E762 0000 0806                00000000   2851+         VL    V22,0(R2)
000037A0  E666 0000 1C5D                           2852+         VCFN  V22,V22,1,0       test instruction (dest is source)
000037A6  B29C 5040                     00003740   2853+         STFPC FPC_R_45          save FPC
000037AA  E760 5028 080E                00003728   2854+         VST   V22,V1O45         save instruction result
000037B0  07FB                                     2855+         BR    R11               return
000037B4                                           2856+RE45     DS    0F                expected 16 byte result
000037B4                                           2857+         DROP  R5
000037B4  00008000 00000000                        2858          DC    XL16'00008000000000000000000000F000'
000037BC  00000000 0000F000
000037C4  00008000 00000000                        2859          DC    XL16'00008000000000000000000000D800'
000037CC  00000000 0000D800
                                                   2860
                                                   2861 * -15
                                                   2862          VRR_A VCFN,1,0,00,00,N
000037D8                                           2863+         DS    0FD
000037D8                        000037D8           2864+         USING *,R5              base for test data and test routine
000037D8  00003868                                 2865+T46      DC    A(X46)            address of test routine
000037DC  002E                                     2866+         DC    H'46'             test number
000037DE  00                                       2867+         DC    X'00'
000037DF  D5                                       2868+         DC    CL1'N'            Y = skip cross check
000037E0  01                                       2869+         DC    HL1'1'            m3
000037E1  00                                       2870+         DC    HL1'0'            m4
000037E2  00                                       2871+FLG46    DC    X'00'             expected FPC flags
000037E3  00                                       2872+VXC46    DC    X'00'             expected VXC
000037E4  0000389C                                 2873+V2_46    DC    A(RE46+16)        address of v2: 16-byte packed decimal
000037E8  E5C3C6D5 40404040                        2874+         DC    CL8'VCFN'         instruction name
000037F0  00000010                                 2875+         DC    A(16)             result length
000037F4  0000388C                                 2876+         DC    A(RE46)           address of expected resul
000037F8  00000000 00000000                        2877+         DS    FD                gap
00003800  00000000 00000000                        2878+V1O46    DS    XL16              V1 output
00003808  00000000 00000000
00003810  00000000 00000000                        2879+         DS    FD                   gap
00003818  00000000                                 2880+FPC_R_46 DS    F                 FPC after instruction
00003820  00000000 00000000                        2881+         DS    FD                   gap
00003828  40404040 40404040                        2882+         DC    CL8' '            was cross check skipped?
00003830  00000000 00000000                        2883+         DS    FD                   gap
00003838  00000000 00000000                        2884+XCO46    DS    XL16              Cross check Output
00003840  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003848  00000000 00000000                        2885+          DS    FD                   gap
00003850  00000000                                 2886+FPC_XC_46 DS    F                  FPC after cross check
00003858  00000000 00000000                        2887+          DS    FD                   gap
00003860  00000000                                 2888+          DS    F                  debug area
00003864  00000000                                 2889+          DS    F
                                                   2890+*
00003868                                           2891+X46       DS    0F
00003868  B29D 85A4                     000007A4   2892+          LFPC  FPCMOFF            initialize FPC
0000386C  E320 500C 0014                000037E4   2893+          LGF   R2,V2_46           get v2
00003872  E762 0000 0806                00000000   2894+          VL    V22,0(R2)
00003878  E666 0000 1C5D                           2895+          VCFN  V22,V22,1,0        test instruction (dest is source)
0000387E  B29C 5040                     00003818   2896+          STFPC FPC_R_46           save FPC
00003882  E760 5028 080E                00003800   2897+          VST   V22,V1O46          save instruction result
00003888  07FB                                     2898+          BR    R11                return
0000388C                                           2899+RE46      DS    0F                 expected 16 byte result
0000388C                                           2900+          DROP  R5
0000388C  CB800000 00000000                        2901           DC    XL16'CB800000000000000000000000F000'
00003894  00000000 0000F000
0000389C  C5C00000 00000000                        2902           DC    XL16'C5C000000000000000000000000D800'
000038A4  00000000 0000D800
                                                   2903
                                                   2904 * 20/7 (about)
                                                   2905           VRR_A VCFN,1,0,00,00,N
000038B0                                           2906+          DS    0FD
000038B0                        000038B0           2907+          USING *,R5               base for test data and test routine
000038B0  00003940                                 2908+T47       DC    A(X47)             address of test routine
000038B4  002F                                     2909+          DC    H'47'              test number
000038B6  00                                       2910+          DC    X'00'
000038B7  D5                                       2911+          DC    CL1'N'             Y = skip cross check
000038B8  01                                       2912+          DC    HL1'1'             m3
000038B9  00                                       2913+          DC    HL1'0'             m4
000038BA  00                                       2914+FLG47     DC    X'00'              expected FPC flags
000038BB  00                                       2915+VXC47     DC    X'00'              expected VXC
000038BC  00003974                                 2916+V2_47     DC    A(RE47+16)         address of v2: 16-byte packed decimal
000038C0  E5C3C6D5 40404040                        2917+          DC    CL8'VCFN'          instruction name
000038C8  00000010                                 2918+          DC    A(16)              result length
000038CC  00003964                                 2919+          DC    A(RE47)            address of expected resul
000038D0  00000000 00000000                        2920+          DS    FD                 gap
000038D8  00000000 00000000                        2921+V1O47     DS    XL16               V1 output
000038E0  00000000 00000000
000038E8  00000000 00000000                        2922+          DS    FD                   gap
000038F0  00000000                                 2923+FPC_R_47  DS    F                  FPC after instruction
000038F8  00000000 00000000                        2924+          DS    FD                   gap
00003900  40404040 40404040                        2925+          DC    CL8' '             was cross check skipped?
00003908  00000000 00000000                        2926+          DS    FD                   gap
00003910  00000000 00000000                        2927+XCO47     DS    XL16               Cross check Output
00003918  00000000 00000000
00003920  00000000 00000000                        2928+          DS    FD                   gap
00003928  00000000                                 2929+FPC_XC_47 DS    F                  FPC after cross check
00003930  00000000 00000000                        2930+          DS    FD                   gap
00003938  00000000                                 2931+          DS    F                  debug area
0000393C  00000000                                 2932+          DS    F
                                                   2933+*
00003940                                           2934+X47       DS    0F
00003940  B29D 85A4                     000007A4   2935+          LFPC  FPCMOFF            initialize FPC
00003944  E320 500C 0014                000038BC   2936+          LGF   R2,V2_47           get v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000394A  E762 0000 0806                00000000  2937+         VL    V22,0(R2)
00003950  E666 0000 1C5D                          2938+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003956  B29C 5040                     000038F0  2939+         STFPC FPC_R_47          save FPC
0000395A  E760 5028 080E                000038D8  2940+         VST   V22,V1O47         save instruction result
00003960  07FB                                    2941+         BR    R11               return
00003964                                          2942+RE47     DS    0F                expected 16 byte result
00003964                                          2943+         DROP  R5
00003964  41B60000 00000000                       2944          DC    XL16'41B6000000000000000000000F000'
0000396C  00000000 0000F000
00003974  40DB0000 00000000                       2945          DC    XL16'40DB000000000000000000000D800'
0000397C  00000000 0000D800
                                                  2946
                                                  2947 * additional tests
                                                  2948 * max  tiny:  (1 - 2^-11) * 2^16 (65504) +1 (overflow)
                                                  2949          VRR_A VCFN,1,0,20,00,S
00003988                                          2950+         DS    0FD
00003988                        00003988          2951+         USING *,R5              base for test data and test routine
00003988  00003A18                                2952+T48      DC    A(X48)            address of test routine
0000398C  0030                                    2953+         DC    H'48'             test number
0000398E  00                                      2954+         DC    X'00'
0000398F  E2                                      2955+         DC    CL1'S'            Y = skip cross check
00003990  01                                      2956+         DC    HL1'1'            m3
00003991  00                                      2957+         DC    HL1'0'            m4
00003992  20                                      2958+FLG48    DC    X'20'             expected FPC flags
00003993  00                                      2959+VXC48    DC    X'00'             expected VXC
00003994  00003A4C                                2960+V2_48    DC    A(RE48+16)        address of v2: 16-byte packed decimal
00003998  E5C3C6D5 40404040                       2961+         DC    CL8'VCFN'         instruction name
000039A0  00000010                                2962+         DC    A(16)             result length
000039A4  00003A3C                                2963+         DC    A(RE48)           address of expected resul
000039A8  00000000 00000000                       2964+         DS    FD                gap
000039B0  00000000 00000000                       2965+V1O48    DS    XL16              V1 output
000039B8  00000000 00000000
000039C0  00000000 00000000                       2966+         DS    FD                   gap
000039C8  00000000                                2967+FPC_R_48 DS    F                 FPC after instruction
000039D0  00000000 00000000                       2968+         DS    FD                   gap
000039D8  40404040 40404040                       2969+         DC    CL8' '            was cross check skipped?
000039E0  00000000 00000000                       2970+         DS    FD                   gap
000039E8  00000000 00000000                       2971+XCO48    DS    XL16              Cross check Output
000039F0  00000000 00000000
000039F8  00000000 00000000                       2972+         DS    FD                   gap
00003A00  00000000                                2973+FPC_XC_48 DS   F                 FPC after cross check
00003A08  00000000 00000000                       2974+         DS    FD                   gap
00003A10  00000000                                2975+         DS    F                 debug area
00003A14  00000000                                2976+         DS    F
                                                  2977+*
00003A18                                          2978+X48      DS    0F
00003A18  B29D 85A4                     000007A4  2979+         LFPC  FPCMOFF           initialize FPC
00003A1C  E320 500C 0014                00003994  2980+         LGF   R2,V2_48          get v2
00003A22  E762 0000 0806                00000000  2981+         VL    V22,0(R2)
00003A28  E666 0000 1C5D                          2982+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003A2E  B29C 5040                     000039C8  2983+         STFPC FPC_R_48          save FPC
00003A32  E760 5028 080E                000039B0  2984+         VST   V22,V1O48         save instruction result
00003A38  07FB                                    2985+         BR    R11               return
00003A3C                                          2986+RE48     DS    0F                expected 16 byte result
00003A3C                                          2987+         DROP  R5
00003A3C  7C000000 00000000                       2988          DC    XL16'7C000000000000000000000F000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003A44  00000000 0000F000
00003A4C  5E000000 00000000                         2989          DC    XL16'5E000000000000000000000000D800'
00003A54  00000000 0000D800
                                                    2990
                                                    2991 * min tiny (normal): 2^-14 (0.00006103515625)
                                                    2992          VRR_A VCFN,1,0,00,00,N
00003A60                                            2993+         DS    0FD
00003A60                            00003A60        2994+         USING *,R5              base for test data and test routine
00003A60  00003AF0                                  2995+T49      DC    A(X49)            address of test routine
00003A64  0031                                      2996+         DC    H'49'             test number
00003A66  00                                        2997+         DC    X'00'
00003A67  D5                                        2998+         DC    CL1'N'            Y = skip cross check
00003A68  01                                        2999+         DC    HL1'1'            m3
00003A69  00                                        3000+         DC    HL1'0'            m4
00003A6A  00                                        3001+FLG49    DC    X'00'             expected FPC flags
00003A6B  00                                        3002+VXC49    DC    X'00'             expected VXC
00003A6C  00003B24                                  3003+V2_49    DC    A(RE49+16)        address of v2: 16-byte packed decimal
00003A70  E5C3C6D5 40404040                         3004+         DC    CL8'VCFN'         instruction name
00003A78  00000010                                  3005+         DC    A(16)             result length
00003A7C  00003B14                                  3006+         DC    A(RE49)           address of expected resul
00003A80  00000000 00000000                         3007+         DS    FD                gap
00003A88  00000000 00000000                         3008+V1O49    DS    XL16              V1 output
00003A90  00000000 00000000
00003A98  00000000 00000000                         3009+         DS    FD                   gap
00003AA0  00000000                                  3010+FPC_R_49 DS    F                 FPC after instruction
00003AA8  00000000 00000000                         3011+         DS    FD                   gap
00003AB0  40404040 40404040                         3012+         DC    CL8' '            was cross check skipped?
00003AB8  00000000 00000000                         3013+         DS    FD                   gap
00003AC0  00000000 00000000                         3014+XCO49    DS    XL16              Cross check Output
00003AC8  00000000 00000000
00003AD0  00000000 00000000                         3015+         DS    FD                   gap
00003AD8  00000000                                  3016+FPC_XC_49 DS   F                 FPC after cross check
00003AE0  00000000 00000000                         3017+         DS    FD                   gap
00003AE8  00000000                                  3018+         DS    F                 debug area
00003AEC  00000000                                  3019+         DS    F
                                                    3020+*
00003AF0                                            3021+X49      DS    0F
00003AF0  B29D 85A4                       000007A4  3022+         LFPC  FPCMOFF           initialize FPC
00003AF4  E320 500C 0014                  00003A6C  3023+         LGF   R2,V2_49          get v2
00003AFA  E762 0000 0806                  00000000  3024+         VL    V22,0(R2)
00003B00  E666 0000 1C5D                            3025+         VCFN  V22,V22,1,0       test instruction (dest is source)
00003B06  B29C 5040                       00003AA0  3026+         STFPC FPC_R_49          save FPC
00003B0A  E760 5028 080E                  00003A88  3027+         VST   V22,V1O49         save instruction result
00003B10  07FB                                      3028+         BR    R11               return
00003B14                                            3029+RE49     DS    0F                expected 16 byte result
00003B14                                            3030+         DROP  R5
00003B14  04000000 00000000                         3031          DC    XL16'04000000000000000000000000F000'
00003B1C  00000000 0000F000
00003B24  22000000 00000000                         3032          DC    XL16'22000000000000000000000000D800'
00003B2C  00000000 0000D800
                                                    3033
                                                    3034 * min tiny (subnormal): 2^-24 (0.000000059604644775390625) (underflow)
                                                    3035          VRR_A VCFN,1,0,10,00,N
00003B38                                            3036+         DS    0FD
00003B38                            00003B38        3037+         USING *,R5              base for test data and test routine
00003B38  00003BC8                                  3038+T50      DC    A(X50)            address of test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003B3C  0032                                     3039+          DC    H'50'              test number
00003B3E  00                                       3040+          DC    X'00'
00003B3F  D5                                       3041+          DC    CL1'N'             Y = skip cross check
00003B40  01                                       3042+          DC    HL1'1'             m3
00003B41  00                                       3043+          DC    HL1'0'             m4
00003B42  10                                       3044+FLG50     DC    X'10'              expected FPC flags
00003B43  00                                       3045+VXC50     DC    X'00'              expected VXC
00003B44  00003BFC                                 3046+V2_50     DC    A(RE50+16)         address of v2: 16-byte packed decimal
00003B48  E5C3C6D5 40404040                        3047+          DC    CL8'VCFN'          instruction name
00003B50  00000010                                 3048+          DC    A(16)              result length
00003B54  00003BEC                                 3049+          DC    A(RE50)            address of expected resul
00003B58  00000000 00000000                        3050+          DS    FD                 gap
00003B60  00000000 00000000                        3051+V1O50     DS    XL16               V1 output
00003B68  00000000 00000000
00003B70  00000000 00000000                        3052+          DS    FD                    gap
00003B78  00000000                                 3053+FPC_R_50  DS    F                  FPC after instruction
00003B80  00000000 00000000                        3054+          DS    FD                    gap
00003B88  40404040 40404040                        3055+          DC    CL8' '             was cross check skipped?
00003B90  00000000 00000000                        3056+          DS    FD                    gap
00003B98  00000000 00000000                        3057+XCO50     DS    XL16               Cross check Output
00003BA0  00000000 00000000
00003BA8  00000000 00000000                        3058+          DS    FD                    gap
00003BB0  00000000                                 3059+FPC_XC_50 DS    F                  FPC after cross check
00003BB8  00000000 00000000                        3060+          DS    FD                    gap
00003BC0  00000000                                 3061+          DS    F                  debug area
00003BC4  00000000                                 3062+          DS    F
                                                   3063+*
00003BC8                                           3064+X50       DS    0F
00003BC8  B29D 85A4                     000007A4   3065+          LFPC  FPCMOFF            initialize FPC
00003BCC  E320 500C 0014                00003B44   3066+          LGF   R2,V2_50           get v2
00003BD2  E762 0000 0806                00000000   3067+          VL    V22,0(R2)
00003BD8  E666 0000 1C5D                           3068+          VCFN  V22,V22,1,0        test instruction (dest is source)
00003BDE  B29C 5040                     00003B78   3069+          STFPC FPC_R_50           save FPC
00003BE2  E760 5028 080E                00003B60   3070+          VST   V22,V1O50          save instruction result
00003BE8  07FB                                     3071+          BR    R11                return
00003BEC                                           3072+RE50      DS    0F                 expected 16 byte result
00003BEC                                           3073+          DROP  R5
00003BEC  00010000 00000000                        3074           DC    XL16'00010000000000000000000000000F000'
00003BF4  00000000 0000F000
00003BFC  0E000000 00000000                        3075           DC    XL16'0E000000000000000000000000000D800'
00003C04  00000000 0000D800
                                                   3076
                                                   3077 *  2 underflows
                                                   3078           VRR_A VCFN,1,0,10,00,S
00003C10                                           3079+          DS    0FD
00003C10                        00003C10           3080+          USING *,R5               base for test data and test routine
00003C10  00003CA0                                 3081+T51       DC    A(X51)             address of test routine
00003C14  0033                                     3082+          DC    H'51'              test number
00003C16  00                                       3083+          DC    X'00'
00003C17  E2                                       3084+          DC    CL1'S'             Y = skip cross check
00003C18  01                                       3085+          DC    HL1'1'             m3
00003C19  00                                       3086+          DC    HL1'0'             m4
00003C1A  10                                       3087+FLG51     DC    X'10'              expected FPC flags
00003C1B  00                                       3088+VXC51     DC    X'00'              expected VXC
00003C1C  00003CD4                                 3089+V2_51     DC    A(RE51+16)         address of v2: 16-byte packed decimal
00003C20  E5C3C6D5 40404040                        3090+          DC    CL8'VCFN'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003C28  00000010                                 3091+          DC    A(16)              result length
00003C2C  00003CC4                                 3092+          DC    A(RE51)            address of expected resul
00003C30  00000000 00000000                        3093+          DS    FD                 gap
00003C38  00000000 00000000                        3094+V1O51     DS    XL16               V1 output
00003C40  00000000 00000000
00003C48  00000000 00000000                        3095+          DS    FD                    gap
00003C50  00000000                                 3096+FPC_R_51  DS    F                  FPC after instruction
00003C58  00000000 00000000                        3097+          DS    FD                    gap
00003C60  40404040 40404040                        3098+          DC    CL8' '             was cross check skipped?
00003C68  00000000 00000000                        3099+          DS    FD                    gap
00003C70  00000000 00000000                        3100+XCO51     DS    XL16               Cross check Output
00003C78  00000000 00000000
00003C80  00000000 00000000                        3101+          DS    FD                    gap
00003C88  00000000                                 3102+FPC_XC_51 DS    F                  FPC after cross check
00003C90  00000000 00000000                        3103+          DS    FD                    gap
00003C98  00000000                                 3104+          DS    F                  debug area
00003C9C  00000000                                 3105+          DS    F
                                                   3106+*
00003CA0                                           3107+X51       DS    0F
00003CA0  B29D 85A4                     000007A4   3108+          LFPC  FPCMOFF            initialize FPC
00003CA4  E320 500C 0014                00003C1C   3109+          LGF   R2,V2_51           get v2
00003CAA  E762 0000 0806                00000000   3110+          VL    V22,0(R2)
00003CB0  E666 0000 1C5D                           3111+          VCFN  V22,V22,1,0        test instruction (dest is source)
00003CB6  B29C 5040                     00003C50   3112+          STFPC FPC_R_51           save FPC
00003CBA  E760 5028 080E                00003C38   3113+          VST   V22,V1O51          save instruction result
00003CC0  07FB                                     3114+          BR    R11                return
00003CC4                                           3115+RE51      DS    0F                 expected 16 byte result
00003CC4                                           3116+          DROP  R5
00003CC4  00000000 00000000                        3117           DC    XL16'000000000000000000000000000F000'
00003CCC  00000000 0000F000
00003CD4  0A000B00 00000000                        3118           DC    XL16'0A000B000000000000000000000D800'
00003CDC  00000000 0000D800
                                                   3119
                                                   3120 * +infinity, -Infinity
                                                   3121           VRR_A VCFN,1,0,80,00,S                   skip xc - invalid
00003CE8                                           3122+          DS    0FD
00003CE8                        00003CE8           3123+          USING *,R5               base for test data and test routine
00003CE8  00003D78                                 3124+T52       DC    A(X52)             address of test routine
00003CEC  0034                                     3125+          DC    H'52'              test number
00003CEE  00                                       3126+          DC    X'00'
00003CEF  E2                                       3127+          DC    CL1'S'             Y = skip cross check
00003CF0  01                                       3128+          DC    HL1'1'             m3
00003CF1  00                                       3129+          DC    HL1'0'             m4
00003CF2  80                                       3130+FLG52     DC    X'80'              expected FPC flags
00003CF3  00                                       3131+VXC52     DC    X'00'              expected VXC
00003CF4  00003DAC                                 3132+V2_52     DC    A(RE52+16)         address of v2: 16-byte packed decimal
00003CF8  E5C3C6D5 40404040                        3133+          DC    CL8'VCFN'          instruction name
00003D00  00000010                                 3134+          DC    A(16)              result length
00003D04  00003D9C                                 3135+          DC    A(RE52)            address of expected resul
00003D08  00000000 00000000                        3136+          DS    FD                 gap
00003D10  00000000 00000000                        3137+V1O52     DS    XL16               V1 output
00003D18  00000000 00000000
00003D20  00000000 00000000                        3138+          DS    FD                    gap
00003D28  00000000                                 3139+FPC_R_52  DS    F                  FPC after instruction
00003D30  00000000 00000000                        3140+          DS    FD                    gap
00003D38  40404040 40404040                        3141+          DC    CL8' '             was cross check skipped?
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003D40  00000000 00000000                        3142+          DS    FD                   gap
00003D48  00000000 00000000                        3143+XCO52     DS    XL16               Cross check Output
00003D50  00000000 00000000
00003D58  00000000 00000000                        3144+          DS    FD                   gap
00003D60  00000000                                 3145+FPC_XC_52 DS    F                  FPC after cross check
00003D68  00000000 00000000                        3146+          DS    FD                   gap
00003D70  00000000                                 3147+          DS    F                  debug area
00003D74  00000000                                 3148+          DS    F
                                                   3149+*
00003D78                                           3150+X52       DS    0F
00003D78  B29D 85A4                     000007A4   3151+          LFPC  FPCMOFF            initialize FPC
00003D7C  E320 500C 0014                00003CF4   3152+          LGF   R2,V2_52           get v2
00003D82  E762 0000 0806                00000000   3153+          VL    V22,0(R2)
00003D88  E666 0000 1C5D                           3154+          VCFN  V22,V22,1,0        test instruction (dest is source)
00003D8E  B29C 5040                     00003D28   3155+          STFPC FPC_R_52           save FPC
00003D92  E760 5028 080E                00003D10   3156+          VST   V22,V1O52          save instruction result
00003D98  07FB                                     3157+          BR    R11                return
00003D9C                                           3158+RE52      DS    0F                 expected 16 byte result
00003D9C                                           3159+          DROP  R5
00003D9C  7E000000 7E000000                        3160           DC    XL16'7E0000007E00000000000000000F000'
00003DA4  00000000 0000F000
00003DAC  7FFF0000 FFFF0000                        3161           DC    XL16'7FFF0000FFFF000000000000000D800'
00003DB4  00000000 0000D800
                                                   3162
                                                   3163 * inexact - bad m3
                                                   3164           VRR_A VCFN,5,0,08,00,S                   skip xc - inexact
00003DC0                                           3165+          DS    0FD
00003DC0                        00003DC0           3166+          USING *,R5               base for test data and test routine
00003DC0  00003E50                                 3167+T53       DC    A(X53)             address of test routine
00003DC4  0035                                     3168+          DC    H'53'              test number
00003DC6  00                                       3169+          DC    X'00'
00003DC7  E2                                       3170+          DC    CL1'S'             Y = skip cross check
00003DC8  05                                       3171+          DC    HL1'5'             m3
00003DC9  00                                       3172+          DC    HL1'0'             m4
00003DCA  08                                       3173+FLG53     DC    X'08'              expected FPC flags
00003DCB  00                                       3174+VXC53     DC    X'00'              expected VXC
00003DCC  00003E84                                 3175+V2_53     DC    A(RE53+16)         address of v2: 16-byte packed decimal
00003DD0  E5C3C6D5 40404040                        3176+          DC    CL8'VCFN'          instruction name
00003DD8  00000010                                 3177+          DC    A(16)              result length
00003DDC  00003E74                                 3178+          DC    A(RE53)            address of expected resul
00003DE0  00000000 00000000                        3179+          DS    FD                 gap
00003DE8  00000000 00000000                        3180+V1O53     DS    XL16               V1 output
00003DF0  00000000 00000000
00003DF8  00000000 00000000                        3181+          DS    FD                   gap
00003E00  00000000                                 3182+FPC_R_53  DS    F                  FPC after instruction
00003E08  00000000 00000000                        3183+          DS    FD                   gap
00003E10  40404040 40404040                        3184+          DC    CL8' '             was cross check skipped?
00003E18  00000000 00000000                        3185+          DS    FD                   gap
00003E20  00000000 00000000                        3186+XCO53     DS    XL16               Cross check Output
00003E28  00000000 00000000
00003E30  00000000 00000000                        3187+          DS    FD                   gap
00003E38  00000000                                 3188+FPC_XC_53 DS    F                  FPC after cross check
00003E40  00000000 00000000                        3189+          DS    FD                   gap
00003E48  00000000                                 3190+          DS    F                  debug area
00003E4C  00000000                                 3191+          DS    F
                                                   3192+*
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00003E50                                          3193+X53      DS    0F
00003E50  B29D 85A4                     000007A4  3194+          LFPC  FPCMOFF           initialize FPC
00003E54  E320 500C 0014                00003DCC  3195+          LGF   R2,V2_53          get v2
00003E5A  E762 0000 0806                00000000  3196+          VL    V22,0(R2)
00003E60  E666 0000 5C5D                          3197+          VCFN  V22,V22,5,0       test instruction (dest is source)
00003E66  B29C 5040                     00003E00  3198+          STFPC FPC_R_53          save FPC
00003E6A  E760 5028 080E                00003DE8  3199+          VST   V22,V1O53         save instruction result
00003E70  07FB                                    3200+          BR    R11               return
00003E74                                          3201+RE53      DS    0F                expected 16 byte result
00003E74                                          3202+          DROP  R5
00003E74  00000000 00000000                       3203           DC    XL16'00000000000000000000000000000000'
00003E7C  00000000 00000000
00003E84  00010000 00000000                       3204           DC    XL16'00010000000000000000000000000F000'
00003E8C  00000000 0000F000
                                                  3205
                                                  3206 * inexact - bad m4
                                                  3207           VRR_A VCFN,0,5,08,00,S                    skip xc - inexact
00003E98                                          3208+          DS    0FD
00003E98                        00003E98          3209+          USING *,R5              base for test data and test routine
00003E98  00003F28                                3210+T54       DC    A(X54)            address of test routine
00003E9C  0036                                    3211+          DC    H'54'             test number
00003E9E  00                                      3212+          DC    X'00'
00003E9F  E2                                      3213+          DC    CL1'S'            Y = skip cross check
00003EA0  00                                      3214+          DC    HL1'0'            m3
00003EA1  05                                      3215+          DC    HL1'5'            m4
00003EA2  08                                      3216+FLG54     DC    X'08'             expected FPC flags
00003EA3  00                                      3217+VXC54     DC    X'00'             expected VXC
00003EA4  00003F5C                                3218+V2_54     DC    A(RE54+16)        address of v2: 16-byte packed decimal
00003EA8  E5C3C6D5 40404040                       3219+          DC    CL8'VCFN'         instruction name
00003EB0  00000010                                3220+          DC    A(16)             result length
00003EB4  00003F4C                                3221+          DC    A(RE54)           address of expected resul
00003EB8  00000000 00000000                       3222+          DS    FD                gap
00003EC0  00000000 00000000                       3223+V1O54     DS    XL16              V1 output
00003EC8  00000000 00000000
00003ED0  00000000 00000000                       3224+          DS    FD                   gap
00003ED8  00000000                                3225+FPC_R_54  DS    F                 FPC after instruction
00003EE0  00000000 00000000                       3226+          DS    FD                   gap
00003EE8  40404040 40404040                       3227+          DC    CL8' '            was cross check skipped?
00003EF0  00000000 00000000                       3228+          DS    FD                   gap
00003EF8  00000000 00000000                       3229+XCO54     DS    XL16              Cross check Output
00003F00  00000000 00000000
00003F08  00000000 00000000                       3230+          DS    FD                   gap
00003F10  00000000                                3231+FPC_XC_54 DS    F                 FPC after cross check
00003F18  00000000 00000000                       3232+          DS    FD                   gap
00003F20  00000000                                3233+          DS    F                 debug area
00003F24  00000000                                3234+          DS    F
                                                  3235+*
00003F28                                          3236+X54       DS    0F
00003F28  B29D 85A4                     000007A4  3237+          LFPC  FPCMOFF           initialize FPC
00003F2C  E320 500C 0014                00003EA4  3238+          LGF   R2,V2_54          get v2
00003F32  E762 0000 0806                00000000  3239+          VL    V22,0(R2)
00003F38  E666 0005 0C5D                          3240+          VCFN  V22,V22,0,5       test instruction (dest is source)
00003F3E  B29C 5040                     00003ED8  3241+          STFPC FPC_R_54          save FPC
00003F42  E760 5028 080E                00003EC0  3242+          VST   V22,V1O54         save instruction result
00003F48  07FB                                    3243+          BR    R11               return
00003F4C                                          3244+RE54      DS    0F                expected 16 byte result
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003F4C                                           3245+         DROP  R5
00003F4C  00000000 00000000                        3246          DC    XL16'00000000000000000000000000000000'
00003F54  00000000 00000000
00003F5C  00010000 00000000                        3247          DC    XL16'00010000000000000000000000000F000'
00003F64  00000000 0000F000
                                                   3248
                                                   3249 * more tests
                                                   3250 * +3.140625, -3.140625
                                                   3251          VRR_A VCFN,1,0,00,00,N
00003F70                                           3252+         DS    0FD
00003F70                       00003F70            3253+         USING *,R5              base for test data and test routine
00003F70  00004000                                 3254+T55      DC    A(X55)            address of test routine
00003F74  0037                                     3255+         DC    H'55'             test number
00003F76  00                                       3256+         DC    X'00'
00003F77  D5                                       3257+         DC    CL1'N'            Y = skip cross check
00003F78  01                                       3258+         DC    HL1'1'            m3
00003F79  00                                       3259+         DC    HL1'0'            m4
00003F7A  00                                       3260+FLG55    DC    X'00'             expected FPC flags
00003F7B  00                                       3261+VXC55    DC    X'00'             expected VXC
00003F7C  00004034                                 3262+V2_55    DC    A(RE55+16)        address of v2: 16-byte packed decimal
00003F80  E5C3C6D5 40404040                        3263+         DC    CL8'VCFN'         instruction name
00003F88  00000010                                 3264+         DC    A(16)             result length
00003F8C  00004024                                 3265+         DC    A(RE55)           address of expected resul
00003F90  00000000 00000000                        3266+         DS    FD                gap
00003F98  00000000 00000000                        3267+V1O55    DS    XL16              V1 output
00003FA0  00000000 00000000
00003FA8  00000000 00000000                        3268+         DS    FD                   gap
00003FB0  00000000                                 3269+FPC_R_55 DS    F                 FPC after instruction
00003FB8  00000000 00000000                        3270+         DS    FD                   gap
00003FC0  40404040 40404040                        3271+         DC    CL8' '            was cross check skipped?
00003FC8  00000000 00000000                        3272+         DS    FD                   gap
00003FD0  00000000 00000000                        3273+XCO55    DS    XL16              Cross check Output
00003FD8  00000000 00000000
00003FE0  00000000 00000000                        3274+         DS    FD                   gap
00003FE8  00000000                                 3275+FPC_XC_55 DS   F                 FPC after cross check
00003FF0  00000000 00000000                        3276+         DS    FD                   gap
00003FF8  00000000                                 3277+         DS    F                 debug area
00003FFC  00000000                                 3278+         DS    F
                                                   3279+*
00004000                                           3280+X55      DS    0F
00004000  B29D 85A4                    000007A4    3281+         LFPC  FPCMOFF           initialize FPC
00004004  E320 500C 0014               00003F7C    3282+         LGF   R2,V2_55          get v2
0000400A  E762 0000 0806               00000000    3283+         VL    V22,0(R2)
00004010  E666 0000 1C5D                           3284+         VCFN  V22,V22,1,0       test instruction (dest is source)
00004016  B29C 5040                    00003FB0    3285+         STFPC FPC_R_55          save FPC
0000401A  E760 5028 080E               00003F98    3286+         VST   V22,V1O55         save instruction result
00004020  07FB                                     3287+         BR    R11               return
00004024                                           3288+RE55     DS    0F                expected 16 byte result
00004024                                           3289+         DROP  R5
00004024  44480000 C4480000                        3290          DC    XL16'44480000C44800000000000000000000'
0000402C  00000000 00000000
00004034  42240000 C2240000                        3291          DC    XL16'42240000C22400000000000000000000'
0000403C  00000000 00000000
                                                   3292
                                                   3293
                                                   3294 * +27.15625, -27.15625
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3295          VRR_A VCFN,1,0,00,00,N
00004048                                           3296+         DS    0FD
00004048                     00004048              3297+         USING *,R5              base for test data and test routine
00004048  000040D8                                 3298+T56      DC    A(X56)            address of test routine
0000404C  0038                                     3299+         DC    H'56'             test number
0000404E  00                                       3300+         DC    X'00'
0000404F  D5                                       3301+         DC    CL1'N'            Y = skip cross check
00004050  01                                       3302+         DC    HL1'1'            m3
00004051  00                                       3303+         DC    HL1'0'            m4
00004052  00                                       3304+FLG56    DC    X'00'             expected FPC flags
00004053  00                                       3305+VXC56    DC    X'00'             expected VXC
00004054  0000410C                                 3306+V2_56    DC    A(RE56+16)        address of v2: 16-byte packed decimal
00004058  E5C3C6D5 40404040                        3307+         DC    CL8'VCFN'         instruction name
00004060  00000010                                 3308+         DC    A(16)             result length
00004064  000040FC                                 3309+         DC    A(RE56)           address of expected resul
00004068  00000000 00000000                        3310+         DS    FD                gap
00004070  00000000 00000000                        3311+V1O56    DS    XL16              V1 output
00004078  00000000 00000000
00004080  00000000 00000000                        3312+         DS    FD                   gap
00004088  00000000                                 3313+FPC_R_56 DS    F                 FPC after instruction
00004090  00000000 00000000                        3314+         DS    FD                   gap
00004098  40404040 40404040                        3315+         DC    CL8' '            was cross check skipped?
000040A0  00000000 00000000                        3316+         DS    FD                   gap
000040A8  00000000 00000000                        3317+XCO56    DS    XL16              Cross check Output
000040B0  00000000 00000000
000040B8  00000000 00000000                        3318+         DS    FD                   gap
000040C0  00000000                                 3319+FPC_XC_56 DS   F                 FPC after cross check
000040C8  00000000 00000000                        3320+         DS    FD                   gap
000040D0  00000000                                 3321+         DS    F                 debug area
000040D4  00000000                                 3322+         DS    F
                                                   3323+*
000040D8                                           3324+X56      DS    0F
000040D8  B29D 85A4                     000007A4   3325+         LFPC  FPCMOFF           initialize FPC
000040DC  E320 500C 0014                00004054   3326+         LGF   R2,V2_56          get v2
000040E2  E762 0000 0806                00000000   3327+         VL    V22,0(R2)
000040E8  E666 0000 1C5D                           3328+         VCFN  V22,V22,1,0       test instruction (dest is source)
000040EE  B29C 5040                     00004088   3329+         STFPC FPC_R_56          save FPC
000040F2  E760 5028 080E                00004070   3330+         VST   V22,V1O56         save instruction result
000040F8  07FB                                     3331+         BR    R11               return
000040FC                                           3332+RE56     DS    0F                expected 16 byte result
000040FC                                           3333+         DROP  R5
000040FC  1ECA0000 9ECA0000                        3334          DC    XL16'1ECA00009ECA00000000000000000000'
00004104  00000000 00000000
0000410C  2F650000 AF650000                        3335          DC    XL16'2F650000AF650000000000000000000'
00004114  00000000 00000000
                                                   3336
                                                   3337 * +65536, -65536 (overflow)
                                                   3338          VRR_A VCFN,1,0,20,00,S
00004120                                           3339+         DS    0FD
00004120                     00004120              3340+         USING *,R5              base for test data and test routine
00004120  000041B0                                 3341+T57      DC    A(X57)            address of test routine
00004124  0039                                     3342+         DC    H'57'             test number
00004126  00                                       3343+         DC    X'00'
00004127  E2                                       3344+         DC    CL1'S'            Y = skip cross check
00004128  01                                       3345+         DC    HL1'1'            m3
00004129  00                                       3346+         DC    HL1'0'            m4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000412A  20                                       3347+FLG57    DC    X'20'              expected FPC flags
0000412B  00                                       3348+VXC57    DC    X'00'              expected VXC
0000412C  000041E4                                 3349+V2_57    DC    A(RE57+16)         address of v2: 16-byte packed decimal
00004130  E5C3C6D5 40404040                        3350+         DC    CL8'VCFN'          instruction name
00004138  00000010                                 3351+         DC    A(16)              result length
0000413C  000041D4                                 3352+         DC    A(RE57)            address of expected resul
00004140  00000000 00000000                        3353+         DS    FD                 gap
00004148  00000000 00000000                        3354+V1O57    DS    XL16               V1 output
00004150  00000000 00000000
00004158  00000000 00000000                        3355+         DS    FD                    gap
00004160  00000000                                 3356+FPC_R_57 DS    F                  FPC after instruction
00004168  00000000 00000000                        3357+         DS    FD                    gap
00004170  40404040 40404040                        3358+         DC    CL8' '             was cross check skipped?
00004178  00000000 00000000                        3359+         DS    FD                    gap
00004180  00000000 00000000                        3360+XCO57    DS    XL16               Cross check Output
00004188  00000000 00000000
00004190  00000000 00000000                        3361+         DS    FD                    gap
00004198  00000000                                 3362+FPC_XC_57 DS   F                  FPC after cross check
000041A0  00000000 00000000                        3363+         DS    FD                    gap
000041A8  00000000                                 3364+         DS    F                  debug area
000041AC  00000000                                 3365+         DS    F
                                                   3366+*
000041B0                                           3367+X57      DS    0F
000041B0  B29D 85A4                     000007A4   3368+         LFPC  FPCMOFF            initialize FPC
000041B4  E320 500C 0014                0000412C   3369+         LGF   R2,V2_57           get v2
000041BA  E762 0000 0806                00000000   3370+         VL    V22,0(R2)
000041C0  E666 0000 1C5D                           3371+         VCFN  V22,V22,1,0        test instruction (dest is source)
000041C6  B29C 5040                     00004160   3372+         STFPC FPC_R_57           save FPC
000041CA  E760 5028 080E                00004148   3373+         VST   V22,V1O57          save instruction result
000041D0  07FB                                     3374+         BR    R11                return
000041D4                                           3375+RE57     DS    0F                 expected 16 byte result
000041D4                                           3376+         DROP  R5
000041D4  7C000000 FC000000                        3377          DC    XL16'7C000000FC00000000000000000000'
000041DC  00000000 00000000
000041E4  5E000000 DE000000                        3378          DC    XL16'5E000000DE00000000000000000000'
000041EC  00000000 00000000
                                                   3379
                                                   3380 * +Normal, -Normal (2.5)
                                                   3381          VRR_A VCFN,1,0,00,00,N
000041F8                                           3382+         DS    0FD
000041F8                        000041F8           3383+         USING *,R5               base for test data and test routine
000041F8  00004288                                 3384+T58      DC    A(X58)             address of test routine
000041FC  003A                                     3385+         DC    H'58'              test number
000041FE  00                                       3386+         DC    X'00'
000041FF  D5                                       3387+         DC    CL1'N'             Y = skip cross check
00004200  01                                       3388+         DC    HL1'1'             m3
00004201  00                                       3389+         DC    HL1'0'             m4
00004202  00                                       3390+FLG58    DC    X'00'              expected FPC flags
00004203  00                                       3391+VXC58    DC    X'00'              expected VXC
00004204  000042BC                                 3392+V2_58    DC    A(RE58+16)         address of v2: 16-byte packed decimal
00004208  E5C3C6D5 40404040                        3393+         DC    CL8'VCFN'          instruction name
00004210  00000010                                 3394+         DC    A(16)              result length
00004214  000042AC                                 3395+         DC    A(RE58)            address of expected resul
00004218  00000000 00000000                        3396+         DS    FD                 gap
00004220  00000000 00000000                        3397+V1O58    DS    XL16               V1 output
00004228  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004230  00000000 00000000                        3398+          DS    FD                   gap
00004238  00000000                                 3399+FPC_R_58 DS    F                  FPC after instruction
00004240  00000000 00000000                        3400+          DS    FD                   gap
00004248  40404040 40404040                        3401+          DC    CL8' '             was cross check skipped?
00004250  00000000 00000000                        3402+          DS    FD                   gap
00004258  00000000 00000000                        3403+XCO58     DS    XL16               Cross check Output
00004260  00000000 00000000
00004268  00000000 00000000                        3404+          DS    FD                   gap
00004270  00000000                                 3405+FPC_XC_58 DS    F                  FPC after cross check
00004278  00000000 00000000                        3406+          DS    FD                   gap
00004280  00000000                                 3407+          DS    F                  debug area
00004284  00000000                                 3408+          DS    F
                                                   3409+*
00004288                                           3410+X58       DS    0F
00004288  B29D 85A4                     000007A4   3411+          LFPC  FPCMOFF            initialize FPC
0000428C  E320 500C 0014                00004204   3412+          LGF   R2,V2_58           get v2
00004292  E762 0000 0806                00000000   3413+          VL    V22,0(R2)
00004298  E666 0000 1C5D                           3414+          VCFN  V22,V22,1,0        test instruction (dest is source)
0000429E  B29C 5040                     00004238   3415+          STFPC FPC_R_58           save FPC
000042A2  E760 5028 080E                00004220   3416+          VST   V22,V1O58          save instruction result
000042A8  07FB                                     3417+          BR    R11                return
000042AC                                           3418+RE58      DS    0F                 expected 16 byte result
000042AC                                           3419+          DROP  R5
000042AC  41000000 C1000000                        3420           DC    XL16'41000000C1000000000000000000000'
000042B4  00000000 00000000
000042BC  40800000 C0800000                        3421           DC    XL16'40800000C0800000000000000000000'
000042C4  00000000 00000000
                                                   3422
                                                   3423 * +0.00006097, -0.00006097 (about)                  (underflow)
                                                   3424           VRR_A VCFN,1,0,10,00,N
000042D0                                           3425+          DS    0FD
000042D0                        000042D0           3426+          USING *,R5               base for test data and test routine
000042D0  00004360                                 3427+T59       DC    A(X59)             address of test routine
000042D4  003B                                     3428+          DC    H'59'              test number
000042D6  00                                       3429+          DC    X'00'
000042D7  D5                                       3430+          DC    CL1'N'             Y = skip cross check
000042D8  01                                       3431+          DC    HL1'1'             m3
000042D9  00                                       3432+          DC    HL1'0'             m4
000042DA  10                                       3433+FLG59     DC    X'10'              expected FPC flags
000042DB  00                                       3434+VXC59     DC    X'00'              expected VXC
000042DC  00004394                                 3435+V2_59     DC    A(RE59+16)         address of v2: 16-byte packed decimal
000042E0  E5C3C6D5 40404040                        3436+          DC    CL8'VCFN'          instruction name
000042E8  00000010                                 3437+          DC    A(16)              result length
000042EC  00004384                                 3438+          DC    A(RE59)            address of expected resul
000042F0  00000000 00000000                        3439+          DS    FD                 gap
000042F8  00000000 00000000                        3440+V1O59     DS    XL16               V1 output
00004300  00000000 00000000
00004308  00000000 00000000                        3441+          DS    FD                   gap
00004310  00000000                                 3442+FPC_R_59 DS    F                  FPC after instruction
00004318  00000000 00000000                        3443+          DS    FD                   gap
00004320  40404040 40404040                        3444+          DC    CL8' '             was cross check skipped?
00004328  00000000 00000000                        3445+          DS    FD                   gap
00004330  00000000 00000000                        3446+XCO59     DS    XL16               Cross check Output
00004338  00000000 00000000
00004340  00000000 00000000                        3447+          DS    FD                   gap
00004348  00000000                                 3448+FPC_XC_59 DS    F                  FPC after cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004350  00000000 00000000                        3449+         DS    FD                   gap
00004358  00000000                                 3450+         DS    F                  debug area
0000435C  00000000                                 3451+         DS    F
                                                   3452+*
00004360                                           3453+X59      DS    0F
00004360  B29D 85A4                     000007A4   3454+         LFPC  FPCMOFF            initialize FPC
00004364  E320 500C 0014                000042DC   3455+         LGF   R2,V2_59           get v2
0000436A  E762 0000 0806                00000000   3456+         VL    V22,0(R2)
00004370  E666 0000 1C5D                           3457+         VCFN  V22,V22,1,0        test instruction (dest is source)
00004376  B29C 5040                     00004310   3458+         STFPC FPC_R_59           save FPC
0000437A  E760 5028 080E                000042F8   3459+         VST   V22,V1O59          save instruction result
00004380  07FB                                     3460+         BR    R11                return
00004384                                           3461+RE59     DS    0F                 expected 16 byte result
00004384                                           3462+         DROP  R5
00004384  03FF0000 83FF0000                        3463          DC    XL16'03FF000083FF00000000000000000000'
0000438C  00000000 00000000
00004394  21FF0000 A1FF0000                        3464          DC    XL16'21FF0000A1FF00000000000000000000'
0000439C  00000000 00000000
                                                   3465
                                                   3466 * multiple exception types
                                                   3467 *  +Infinity, overflow
                                                   3468          VRR_A VCFN,1,0,A0,00,S                     skip xc - infinity
000043A8                                           3469+         DS    0FD
000043A8                        000043A8           3470+         USING *,R5               base for test data and test routine
000043A8  00004438                                 3471+T60      DC    A(X60)             address of test routine
000043AC  003C                                     3472+         DC    H'60'              test number
000043AE  00                                       3473+         DC    X'00'
000043AF  E2                                       3474+         DC    CL1'S'             Y = skip cross check
000043B0  01                                       3475+         DC    HL1'1'             m3
000043B1  00                                       3476+         DC    HL1'0'             m4
000043B2  A0                                       3477+FLG60    DC    X'A0'              expected FPC flags
000043B3  00                                       3478+VXC60    DC    X'00'              expected VXC
000043B4  0000446C                                 3479+V2_60    DC    A(RE60+16)         address of v2: 16-byte packed decimal
000043B8  E5C3C6D5 40404040                        3480+         DC    CL8'VCFN'          instruction name
000043C0  00000010                                 3481+         DC    A(16)              result length
000043C4  0000445C                                 3482+         DC    A(RE60)            address of expected resul
000043C8  00000000 00000000                        3483+         DS    FD                 gap
000043D0  00000000 00000000                        3484+V1O60    DS    XL16               V1 output
000043D8  00000000 00000000
000043E0  00000000 00000000                        3485+         DS    FD                   gap
000043E8  00000000                                 3486+FPC_R_60 DS    F                  FPC after instruction
000043F0  00000000 00000000                        3487+         DS    FD                   gap
000043F8  40404040 40404040                        3488+         DC    CL8' '             was cross check skipped?
00004400  00000000 00000000                        3489+         DS    FD                   gap
00004408  00000000 00000000                        3490+XCO60    DS    XL16               Cross check Output
00004410  00000000 00000000
00004418  00000000 00000000                        3491+         DS    FD                   gap
00004420  00000000                                 3492+FPC_XC_60 DS   F                  FPC after cross check
00004428  00000000 00000000                        3493+         DS    FD                   gap
00004430  00000000                                 3494+         DS    F                  debug area
00004434  00000000                                 3495+         DS    F
                                                   3496+*
00004438                                           3497+X60      DS    0F
00004438  B29D 85A4                     000007A4   3498+         LFPC  FPCMOFF            initialize FPC
0000443C  E320 500C 0014                000043B4   3499+         LGF   R2,V2_60           get v2
00004442  E762 0000 0806                00000000   3500+         VL    V22,0(R2)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004448  E666 0000 1C5D                           3501+         VCFN  V22,V22,1,0       test instruction (dest is source)
0000444E  B29C 5040                       000043E8 3502+         STFPC FPC_R_60          save FPC
00004452  E760 5028 080E                  000043D0 3503+         VST   V22,V1O60         save instruction result
00004458  07FB                                     3504+         BR    R11               return
0000445C                                           3505+RE60     DS    0F                expected 16 byte result
0000445C                                           3506+         DROP  R5
0000445C  7E000000 7C000000                        3507          DC    XL16'7E0000007C000000000000000000000'
00004464  00000000 00000000
0000446C  7FFF0000 5E000000                        3508          DC    XL16'7FFF00005E000000000000000000000'
00004474  00000000 00000000
                                                   3509
                                                   3510 * Underflow,  -65536 (overflow)              skip xc - dropped digits
                                                   3511          VRR_A VCFN,1,0,30,00,S
00004480                                           3512+         DS    0FD
00004480                       00004480            3513+         USING *,R5              base for test data and test routine
00004480  00004510                                 3514+T61      DC    A(X61)            address of test routine
00004484  003D                                     3515+         DC    H'61'             test number
00004486  00                                       3516+         DC    X'00'
00004487  E2                                       3517+         DC    CL1'S'            Y = skip cross check
00004488  01                                       3518+         DC    HL1'1'            m3
00004489  00                                       3519+         DC    HL1'0'            m4
0000448A  30                                       3520+FLG61    DC    X'30'             expected FPC flags
0000448B  00                                       3521+VXC61    DC    X'00'             expected VXC
0000448C  00004544                                 3522+V2_61    DC    A(RE61+16)        address of v2: 16-byte packed decimal
00004490  E5C3C6D5 40404040                        3523+         DC    CL8'VCFN'         instruction name
00004498  00000010                                 3524+         DC    A(16)             result length
0000449C  00004534                                 3525+         DC    A(RE61)           address of expected resul
000044A0  00000000 00000000                        3526+         DS    FD                gap
000044A8  00000000 00000000                        3527+V1O61    DS    XL16              V1 output
000044B0  00000000 00000000
000044B8  00000000 00000000                        3528+         DS    FD                   gap
000044C0  00000000                                 3529+FPC_R_61 DS    F                 FPC after instruction
000044C8  00000000 00000000                        3530+         DS    FD                   gap
000044D0  40404040 40404040                        3531+         DC    CL8' '            was cross check skipped?
000044D8  00000000 00000000                        3532+         DS    FD                   gap
000044E0  00000000 00000000                        3533+XCO61    DS    XL16              Cross check Output
000044E8  00000000 00000000
000044F0  00000000 00000000                        3534+         DS    FD                   gap
000044F8  00000000                                 3535+FPC_XC_61 DS   F                 FPC after cross check
00004500  00000000 00000000                        3536+         DS    FD                   gap
00004508  00000000                                 3537+         DS    F                 debug area
0000450C  00000000                                 3538+         DS    F
                                                   3539+*
00004510                                           3540+X61      DS    0F
00004510  B29D 85A4                       000007A4 3541+         LFPC  FPCMOFF           initialize FPC
00004514  E320 500C 0014                  0000448C 3542+         LGF   R2,V2_61          get v2
0000451A  E762 0000 0806                  00000000 3543+         VL    V22,0(R2)
00004520  E666 0000 1C5D                           3544+         VCFN  V22,V22,1,0       test instruction (dest is source)
00004526  B29C 5040                       000044C0 3545+         STFPC FPC_R_61          save FPC
0000452A  E760 5028 080E                  000044A8 3546+         VST   V22,V1O61         save instruction result
00004530  07FB                                     3547+         BR    R11               return
00004534                                           3548+RE61     DS    0F                expected 16 byte result
00004534                                           3549+         DROP  R5
00004534  00000000 7C000000                        3550          DC    XL16'000000007C000000000000000000000'
0000453C  00000000 00000000
00004544  0A000000 5E000000                        3551          DC    XL16'0A0000005E000000000000000000000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000454C  00000000 00000000
                                                   3552
                                                   3553 * +Infinity, Underflow,  -65536 (overflow)         skip xc - infinity
                                                   3554          VRR_A VCFN,1,0,B0,00,S
00004558                                           3555+         DS    0FD
00004558                       00004558            3556+         USING *,R5              base for test data and test routine
00004558  000045E8                                 3557+T62      DC    A(X62)            address of test routine
0000455C  003E                                     3558+         DC    H'62'             test number
0000455E  00                                       3559+         DC    X'00'
0000455F  E2                                       3560+         DC    CL1'S'            Y = skip cross check
00004560  01                                       3561+         DC    HL1'1'            m3
00004561  00                                       3562+         DC    HL1'0'            m4
00004562  B0                                       3563+FLG62    DC    X'B0'             expected FPC flags
00004563  00                                       3564+VXC62    DC    X'00'             expected VXC
00004564  0000461C                                 3565+V2_62    DC    A(RE62+16)        address of v2: 16-byte packed decimal
00004568  E5C3C6D5 40404040                        3566+         DC    CL8'VCFN'         instruction name
00004570  00000010                                 3567+         DC    A(16)             result length
00004574  0000460C                                 3568+         DC    A(RE62)           address of expected resul
00004578  00000000 00000000                        3569+         DS    FD                gap
00004580  00000000 00000000                        3570+V1O62    DS    XL16              V1 output
00004588  00000000 00000000
00004590  00000000 00000000                        3571+         DS    FD                   gap
00004598  00000000                                 3572+FPC_R_62 DS    F                 FPC after instruction
000045A0  00000000 00000000                        3573+         DS    FD                   gap
000045A8  40404040 40404040                        3574+         DC    CL8' '            was cross check skipped?
000045B0  00000000 00000000                        3575+         DS    FD                   gap
000045B8  00000000 00000000                        3576+XCO62    DS    XL16              Cross check Output
000045C0  00000000 00000000
000045C8  00000000 00000000                        3577+         DS    FD                   gap
000045D0  00000000                                 3578+FPC_XC_62 DS   F                 FPC after cross check
000045D8  00000000 00000000                        3579+         DS    FD                   gap
000045E0  00000000                                 3580+         DS    F                 debug area
000045E4  00000000                                 3581+         DS    F
                                                   3582+*
000045E8                                           3583+X62      DS    0F
000045E8  B29D 85A4                    000007A4    3584+         LFPC  FPCMOFF           initialize FPC
000045EC  E320 500C 0014               00004564    3585+         LGF   R2,V2_62          get v2
000045F2  E762 0000 0806               00000000    3586+         VL    V22,0(R2)
000045F8  E666 0000 1C5D                           3587+         VCFN  V22,V22,1,0       test instruction (dest is source)
000045FE  B29C 5040                    00004598    3588+         STFPC FPC_R_62          save FPC
00004602  E760 5028 080E               00004580    3589+         VST   V22,V1O62         save instruction result
00004608  07FB                                     3590+         BR    R11               return
0000460C                                           3591+RE62     DS    0F                expected 16 byte result
0000460C                                           3592+         DROP  R5
0000460C  7E000000 00000000                        3593          DC    XL16'7E00000000000007C00000000000000'
00004614  7C000000 00000000
0000461C  7FFF0000 0A000000                        3594          DC    XL16'7FFF00000A0000005E00000000000000'
00004624  5E000000 00000000
                                                   3595
                                                   3596 *-----------------------------------------------------------------------
                                                   3597 * VCLFNL   - VECTOR FP CONVERT AND LENGTHEN FROM NNP LOW
                                                   3598 *-----------------------------------------------------------------------
                                                   3599 *  dlfloat -> short float (with cross check: short float -> dlfloat)
                                                   3600 *
                                                   3601
                                                   3602 * +0, -0     simple instruction and 'test' test
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3603          VRR_A VCLFNL,2,0,00,00,N
00004630                                           3604+         DS    0FD
00004630                     00004630              3605+         USING *,R5              base for test data and test routine
00004630  000046C0                                 3606+T63      DC    A(X63)            address of test routine
00004634  003F                                     3607+         DC    H'63'             test number
00004636  00                                       3608+         DC    X'00'
00004637  D5                                       3609+         DC    CL1'N'            Y = skip cross check
00004638  02                                       3610+         DC    HL1'2'            m3
00004639  00                                       3611+         DC    HL1'0'            m4
0000463A  00                                       3612+FLG63    DC    X'00'             expected FPC flags
0000463B  00                                       3613+VXC63    DC    X'00'             expected VXC
0000463C  000046F4                                 3614+V2_63    DC    A(RE63+16)        address of v2: 16-byte packed decimal
00004640  E5C3D3C6 D5D34040                        3615+         DC    CL8'VCLFNL'       instruction name
00004648  00000010                                 3616+         DC    A(16)             result length
0000464C  000046E4                                 3617+         DC    A(RE63)           address of expected resul
00004650  00000000 00000000                        3618+         DS    FD                gap
00004658  00000000 00000000                        3619+V1O63    DS    XL16              V1 output
00004660  00000000 00000000
00004668  00000000 00000000                        3620+         DS    FD                   gap
00004670  00000000                                 3621+FPC_R_63 DS    F                 FPC after instruction
00004678  00000000 00000000                        3622+         DS    FD                   gap
00004680  40404040 40404040                        3623+         DC    CL8' '            was cross check skipped?
00004688  00000000 00000000                        3624+         DS    FD                   gap
00004690  00000000 00000000                        3625+XCO63    DS    XL16              Cross check Output
00004698  00000000 00000000
000046A0  00000000 00000000                        3626+         DS    FD                   gap
000046A8  00000000                                 3627+FPC_XC_63 DS   F                 FPC after cross check
000046B0  00000000 00000000                        3628+         DS    FD                   gap
000046B8  00000000                                 3629+         DS    F                 debug area
000046BC  00000000                                 3630+         DS    F
                                                   3631+*
000046C0                                           3632+X63      DS    0F
000046C0  B29D 85A4                    000007A4    3633+         LFPC  FPCMOFF           initialize FPC
000046C4  E320 500C 0014               0000463C    3634+         LGF   R2,V2_63          get v2
000046CA  E762 0000 0806               00000000    3635+         VL    V22,0(R2)
000046D0  E666 0000 2C5E                           3636+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000046D6  B29C 5040                    00004670    3637+         STFPC FPC_R_63          save FPC
000046DA  E760 5028 080E               00004658    3638+         VST   V22,V1O63         save instruction result
000046E0  07FB                                     3639+         BR    R11               return
000046E4                                           3640+RE63     DS    0F                expected 16 byte result
000046E4                                           3641+         DROP  R5
000046E4  00000000 80000000                        3642          DC    XL16'00000000800000000000000000000000'
000046EC  00000000 00000000
000046F4  00000000 00000000                        3643          DC    XL16'00000000000000000000800000000000'
000046FC  00008000 00000000
                                                   3644
                                                   3645 * +1, -1
                                                   3646          VRR_A VCLFNL,2,0,00,00,N
00004708                                           3647+         DS    0FD
00004708                     00004708              3648+         USING *,R5              base for test data and test routine
00004708  00004798                                 3649+T64      DC    A(X64)            address of test routine
0000470C  0040                                     3650+         DC    H'64'             test number
0000470E  00                                       3651+         DC    X'00'
0000470F  D5                                       3652+         DC    CL1'N'            Y = skip cross check
00004710  02                                       3653+         DC    HL1'2'            m3
00004711  00                                       3654+         DC    HL1'0'            m4
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004712  00                                       3655+FLG64    DC    X'00'              expected FPC flags
00004713  00                                       3656+VXC64    DC    X'00'              expected VXC
00004714  000047CC                                 3657+V2_64    DC    A(RE64+16)         address of v2: 16-byte packed decimal
00004718  E5C3D3C6 D5D34040                        3658+         DC    CL8'VCLFNL'        instruction name
00004720  00000010                                 3659+         DC    A(16)              result length
00004724  000047BC                                 3660+         DC    A(RE64)            address of expected resul
00004728  00000000 00000000                        3661+         DS    FD                 gap
00004730  00000000 00000000                        3662+V1O64    DS    XL16               V1 output
00004738  00000000 00000000
00004740  00000000 00000000                        3663+         DS    FD                    gap
00004748  00000000                                 3664+FPC_R_64 DS    F                  FPC after instruction
00004750  00000000 00000000                        3665+         DS    FD                    gap
00004758  40404040 40404040                        3666+         DC    CL8' '             was cross check skipped?
00004760  00000000 00000000                        3667+         DS    FD                    gap
00004768  00000000 00000000                        3668+XCO64    DS    XL16               Cross check Output
00004770  00000000 00000000
00004778  00000000 00000000                        3669+         DS    FD                    gap
00004780  00000000                                 3670+FPC_XC_64 DS   F                  FPC after cross check
00004788  00000000 00000000                        3671+         DS    FD                    gap
00004790  00000000                                 3672+         DS    F                  debug area
00004794  00000000                                 3673+         DS    F
                                                   3674+*
00004798                                           3675+X64      DS    0F
00004798  B29D 85A4                     000007A4   3676+         LFPC  FPCMOFF            initialize FPC
0000479C  E320 500C 0014                00004714   3677+         LGF   R2,V2_64           get v2
000047A2  E762 0000 0806                00000000   3678+         VL    V22,0(R2)
000047A8  E666 0000 2C5E                           3679+         VCLFNL V22,V22,2,0       test instruction (dest is source)
000047AE  B29C 5040                     00004748   3680+         STFPC FPC_R_64           save FPC
000047B2  E760 5028 080E                00004730   3681+         VST   V22,V1O64          save instruction result
000047B8  07FB                                     3682+         BR    R11                return
000047BC                                           3683+RE64     DS    0F                 expected 16 byte result
000047BC                                           3684+         DROP  R5
000047BC  3F800000 BF800000                        3685          DC    XL16'3F800000BF800000000000000000000'
000047C4  00000000 00000000
000047CC  00000000 00000000                        3686          DC    XL16'00000000000000003E00BE0000000000'
000047D4  3E00BE00 00000000
                                                   3687
                                                   3688 * +0.5, -0.5
                                                   3689          VRR_A VCLFNL,2,0,00,00,N
000047E0                                           3690+         DS    0FD
000047E0                        000047E0           3691+         USING *,R5               base for test data and test routine
000047E0  00004870                                 3692+T65      DC    A(X65)             address of test routine
000047E4  0041                                     3693+         DC    H'65'              test number
000047E6  00                                       3694+         DC    X'00'
000047E7  D5                                       3695+         DC    CL1'N'             Y = skip cross check
000047E8  02                                       3696+         DC    HL1'2'             m3
000047E9  00                                       3697+         DC    HL1'0'             m4
000047EA  00                                       3698+FLG65    DC    X'00'              expected FPC flags
000047EB  00                                       3699+VXC65    DC    X'00'              expected VXC
000047EC  000048A4                                 3700+V2_65    DC    A(RE65+16)         address of v2: 16-byte packed decimal
000047F0  E5C3D3C6 D5D34040                        3701+         DC    CL8'VCLFNL'        instruction name
000047F8  00000010                                 3702+         DC    A(16)              result length
000047FC  00004894                                 3703+         DC    A(RE65)            address of expected resul
00004800  00000000 00000000                        3704+         DS    FD                 gap
00004808  00000000 00000000                        3705+V1O65    DS    XL16               V1 output
00004810  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004818  00000000 00000000                        3706+          DS    FD                   gap
00004820  00000000                                 3707+FPC_R_65 DS    F                  FPC after instruction
00004828  00000000 00000000                        3708+          DS    FD                   gap
00004830  40404040 40404040                        3709+          DC    CL8' '             was cross check skipped?
00004838  00000000 00000000                        3710+          DS    FD                   gap
00004840  00000000 00000000                        3711+XCO65     DS    XL16               Cross check Output
00004848  00000000 00000000
00004850  00000000 00000000                        3712+          DS    FD                   gap
00004858  00000000                                 3713+FPC_XC_65 DS    F                  FPC after cross check
00004860  00000000 00000000                        3714+          DS    FD                   gap
00004868  00000000                                 3715+          DS    F                  debug area
0000486C  00000000                                 3716+          DS    F
                                                   3717+*
00004870                                           3718+X65       DS    0F
00004870  B29D 85A4                     000007A4   3719+          LFPC  FPCMOFF            initialize FPC
00004874  E320 500C 0014                000047EC   3720+          LGF   R2,V2_65           get v2
0000487A  E762 0000 0806                00000000   3721+          VL    V22,0(R2)
00004880  E666 0000 2C5E                           3722+          VCLFNL V22,V22,2,0       test instruction (dest is source)
00004886  B29C 5040                     00004820   3723+          STFPC FPC_R_65           save FPC
0000488A  E760 5028 080E                00004808   3724+          VST   V22,V1O65          save instruction result
00004890  07FB                                     3725+          BR    R11                return
00004894                                           3726+RE65      DS    0F                 expected 16 byte result
00004894                                           3727+          DROP  R5
00004894  3F000000 BF000000                        3728           DC    XL16'3F000000BF000000000000000000000000'
0000489C  00000000 00000000
000048A4  00000000 00000000                        3729           DC    XL16'0000000000000003C00BC0000000000'
000048AC  3C00BC00 00000000
                                                   3730
                                                   3731 * 1/64, -1/64
                                                   3732           VRR_A VCLFNL,2,0,00,00,N
000048B8                                           3733+          DS    0FD
000048B8                        000048B8           3734+          USING *,R5               base for test data and test routine
000048B8  00004948                                 3735+T66       DC    A(X66)             address of test routine
000048BC  0042                                     3736+          DC    H'66'              test number
000048BE  00                                       3737+          DC    X'00'
000048BF  D5                                       3738+          DC    CL1'N'             Y = skip cross check
000048C0  02                                       3739+          DC    HL1'2'             m3
000048C1  00                                       3740+          DC    HL1'0'             m4
000048C2  00                                       3741+FLG66     DC    X'00'              expected FPC flags
000048C3  00                                       3742+VXC66     DC    X'00'              expected VXC
000048C4  0000497C                                 3743+V2_66     DC    A(RE66+16)         address of v2: 16-byte packed decimal
000048C8  E5C3D3C6 D5D34040                        3744+          DC    CL8'VCLFNL'        instruction name
000048D0  00000010                                 3745+          DC    A(16)              result length
000048D4  0000496C                                 3746+          DC    A(RE66)            address of expected resul
000048D8  00000000 00000000                        3747+          DS    FD                 gap
000048E0  00000000 00000000                        3748+V1O66     DS    XL16               V1 output
000048E8  00000000 00000000
000048F0  00000000 00000000                        3749+          DS    FD                   gap
000048F8  00000000                                 3750+FPC_R_66 DS    F                  FPC after instruction
00004900  00000000 00000000                        3751+          DS    FD                   gap
00004908  40404040 40404040                        3752+          DC    CL8' '             was cross check skipped?
00004910  00000000 00000000                        3753+          DS    FD                   gap
00004918  00000000 00000000                        3754+XCO66     DS    XL16               Cross check Output
00004920  00000000 00000000
00004928  00000000 00000000                        3755+          DS    FD                   gap
00004930  00000000                                 3756+FPC_XC_66 DS    F                  FPC after cross check
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004938  00000000 00000000                        3757+         DS    FD                   gap
00004940  00000000                                 3758+         DS    F                 debug area
00004944  00000000                                 3759+         DS    F
                                                   3760+*
00004948                                           3761+X66      DS    0F
00004948  B29D 85A4                     000007A4   3762+         LFPC  FPCMOFF           initialize FPC
0000494C  E320 500C 0014                000048C4   3763+         LGF   R2,V2_66          get v2
00004952  E762 0000 0806                00000000   3764+         VL    V22,0(R2)
00004958  E666 0000 2C5E                           3765+         VCLFNL V22,V22,2,0      test instruction (dest is source)
0000495E  B29C 5040                     000048F8   3766+         STFPC FPC_R_66          save FPC
00004962  E760 5028 080E                000048E0   3767+         VST   V22,V1O66         save instruction result
00004968  07FB                                     3768+         BR    R11               return
0000496C                                           3769+RE66     DS    0F                expected 16 byte result
0000496C                                           3770+         DROP  R5
0000496C  3C800000 BC800000                        3771          DC    XL16'3C800000BC80000000000000000000'
00004974  00000000 00000000
0000497C  00000000 00000000                        3772          DC    XL16'00000000000000003200B20000000000'
00004984  3200B200 00000000
                                                   3773
                                                   3774 * +15, -15
                                                   3775          VRR_A VCLFNL,2,0,00,00,N
00004990                                           3776+         DS    0FD
00004990                        00004990           3777+         USING *,R5              base for test data and test routine
00004990  00004A20                                 3778+T67      DC    A(X67)            address of test routine
00004994  0043                                     3779+         DC    H'67'             test number
00004996  00                                       3780+         DC    X'00'
00004997  D5                                       3781+         DC    CL1'N'            Y = skip cross check
00004998  02                                       3782+         DC    HL1'2'            m3
00004999  00                                       3783+         DC    HL1'0'            m4
0000499A  00                                       3784+FLG67    DC    X'00'             expected FPC flags
0000499B  00                                       3785+VXC67    DC    X'00'             expected VXC
0000499C  00004A54                                 3786+V2_67    DC    A(RE67+16)        address of v2: 16-byte packed decimal
000049A0  E5C3D3C6 D5D34040                        3787+         DC    CL8'VCLFNL'       instruction name
000049A8  00000010                                 3788+         DC    A(16)             result length
000049AC  00004A44                                 3789+         DC    A(RE67)           address of expected resul
000049B0  00000000 00000000                        3790+         DS    FD                gap
000049B8  00000000 00000000                        3791+V1O67    DS    XL16              V1 output
000049C0  00000000 00000000
000049C8  00000000 00000000                        3792+         DS    FD                   gap
000049D0  00000000                                 3793+FPC_R_67 DS    F                 FPC after instruction
000049D8  00000000 00000000                        3794+         DS    FD                   gap
000049E0  40404040 40404040                        3795+         DC    CL8' '            was cross check skipped?
000049E8  00000000 00000000                        3796+         DS    FD                   gap
000049F0  00000000 00000000                        3797+XCO67    DS    XL16              Cross check Output
000049F8  00000000 00000000
00004A00  00000000 00000000                        3798+         DS    FD                   gap
00004A08  00000000                                 3799+FPC_XC_67 DS   F                 FPC after cross check
00004A10  00000000 00000000                        3800+         DS    FD                   gap
00004A18  00000000                                 3801+         DS    F                 debug area
00004A1C  00000000                                 3802+         DS    F
                                                   3803+*
00004A20                                           3804+X67      DS    0F
00004A20  B29D 85A4                     000007A4   3805+         LFPC  FPCMOFF           initialize FPC
00004A24  E320 500C 0014                0000499C   3806+         LGF   R2,V2_67          get v2
00004A2A  E762 0000 0806                00000000   3807+         VL    V22,0(R2)
00004A30  E666 0000 2C5E                           3808+         VCLFNL V22,V22,2,0      test instruction (dest is source)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004A36  B29C 5040                     000049D0  3809+         STFPC FPC_R_67          save FPC
00004A3A  E760 5028 080E                000049B8  3810+         VST   V22,V1O67         save instruction result
00004A40  07FB                                    3811+         BR    R11               return
00004A44                                          3812+RE67     DS    0F                expected 16 byte result
00004A44                                          3813+         DROP  R5
00004A44  41700000 C1700000                       3814          DC    XL16'41700000C17000000000000000000000'
00004A4C  00000000 00000000
00004A54  00000000 00000000                       3815          DC    XL16'00000000000000045C0C5C000000000'
00004A5C  45C0C5C0 00000000
                                                  3816
                                                  3817 * +20/7, -20/7 (about)
                                                  3818          VRR_A VCLFNL,2,0,00,00,N
00004A68                                          3819+         DS    0FD
00004A68                        00004A68          3820+         USING *,R5              base for test data and test routine
00004A68  00004AF8                                3821+T68      DC    A(X68)            address of test routine
00004A6C  0044                                    3822+         DC    H'68'             test number
00004A6E  00                                      3823+         DC    X'00'
00004A6F  D5                                      3824+         DC    CL1'N'            Y = skip cross check
00004A70  02                                      3825+         DC    HL1'2'            m3
00004A71  00                                      3826+         DC    HL1'0'            m4
00004A72  00                                      3827+FLG68    DC    X'00'             expected FPC flags
00004A73  00                                      3828+VXC68    DC    X'00'             expected VXC
00004A74  00004B2C                                3829+V2_68    DC    A(RE68+16)        address of v2: 16-byte packed decimal
00004A78  E5C3D3C6 D5D34040                       3830+         DC    CL8'VCLFNL'       instruction name
00004A80  00000010                                3831+         DC    A(16)             result length
00004A84  00004B1C                                3832+         DC    A(RE68)           address of expected resul
00004A88  00000000 00000000                       3833+         DS    FD                gap
00004A90  00000000 00000000                       3834+V1O68    DS    XL16              V1 output
00004A98  00000000 00000000
00004AA0  00000000 00000000                       3835+         DS    FD                   gap
00004AA8  00000000                                3836+FPC_R_68 DS    F                 FPC after instruction
00004AB0  00000000 00000000                       3837+         DS    FD                   gap
00004AB8  40404040 40404040                       3838+         DC    CL8' '            was cross check skipped?
00004AC0  00000000 00000000                       3839+         DS    FD                   gap
00004AC8  00000000 00000000                       3840+XCO68    DS    XL16              Cross check Output
00004AD0  00000000 00000000
00004AD8  00000000 00000000                       3841+         DS    FD                   gap
00004AE0  00000000                                3842+FPC_XC_68 DS   F                 FPC after cross check
00004AE8  00000000 00000000                       3843+         DS    FD                   gap
00004AF0  00000000                                3844+         DS    F                 debug area
00004AF4  00000000                                3845+         DS    F
                                                  3846+*
00004AF8                                          3847+X68      DS    0F
00004AF8  B29D 85A4                     000007A4  3848+         LFPC  FPCMOFF           initialize FPC
00004AFC  E320 500C 0014                00004A74  3849+         LGF   R2,V2_68          get v2
00004B02  E762 0000 0806                00000000  3850+         VL    V22,0(R2)
00004B08  E666 0000 2C5E                          3851+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004B0E  B29C 5040                     00004AA8  3852+         STFPC FPC_R_68          save FPC
00004B12  E760 5028 080E                00004A90  3853+         VST   V22,V1O68         save instruction result
00004B18  07FB                                    3854+         BR    R11               return
00004B1C                                          3855+RE68     DS    0F                expected 16 byte result
00004B1C                                          3856+         DROP  R5
00004B1C  4036C000 C036C000                       3857          DC    XL16'4036C000C036C000000000000000000'
00004B24  00000000 00000000
00004B2C  00000000 00000000                       3858          DC    XL16'00000000000000040DBC0DB00000000'
00004B34  40DBC0DB 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3859
                                                   3860 * additional tests
                                                   3861 * max  tiny:  (1 - 2^-11) * 2^16 (65504)
                                                   3862          VRR_A VCLFNL,2,0,00,00,N
00004B40                                           3863+         DS    0FD
00004B40                       00004B40            3864+         USING *,R5              base for test data and test routine
00004B40  00004BD0                                 3865+T69      DC    A(X69)            address of test routine
00004B44  0045                                     3866+         DC    H'69'             test number
00004B46  00                                       3867+         DC    X'00'
00004B47  D5                                       3868+         DC    CL1'N'            Y = skip cross check
00004B48  02                                       3869+         DC    HL1'2'            m3
00004B49  00                                       3870+         DC    HL1'0'            m4
00004B4A  00                                       3871+FLG69    DC    X'00'             expected FPC flags
00004B4B  00                                       3872+VXC69    DC    X'00'             expected VXC
00004B4C  00004C04                                 3873+V2_69    DC    A(RE69+16)        address of v2: 16-byte packed decimal
00004B50  E5C3D3C6 D5D34040                        3874+         DC    CL8'VCLFNL'       instruction name
00004B58  00000010                                 3875+         DC    A(16)             result length
00004B5C  00004BF4                                 3876+         DC    A(RE69)           address of expected resul
00004B60  00000000 00000000                        3877+         DS    FD                gap
00004B68  00000000 00000000                        3878+V1O69    DS    XL16              V1 output
00004B70  00000000 00000000
00004B78  00000000 00000000                        3879+         DS    FD                   gap
00004B80  00000000                                 3880+FPC_R_69 DS    F                 FPC after instruction
00004B88  00000000 00000000                        3881+         DS    FD                   gap
00004B90  40404040 40404040                        3882+         DC    CL8' '            was cross check skipped?
00004B98  00000000 00000000                        3883+         DS    FD                   gap
00004BA0  00000000 00000000                        3884+XCO69    DS    XL16              Cross check Output
00004BA8  00000000 00000000
00004BB0  00000000 00000000                        3885+         DS    FD                   gap
00004BB8  00000000                                 3886+FPC_XC_69 DS   F                 FPC after cross check
00004BC0  00000000 00000000                        3887+         DS    FD                   gap
00004BC8  00000000                                 3888+         DS    F                 debug area
00004BCC  00000000                                 3889+         DS    F
                                                   3890+*
00004BD0                                           3891+X69      DS    0F
00004BD0  B29D 85A4                    000007A4    3892+         LFPC  FPCMOFF           initialize FPC
00004BD4  E320 500C 0014               00004B4C    3893+         LGF   R2,V2_69          get v2
00004BDA  E762 0000 0806               00000000    3894+         VL    V22,0(R2)
00004BE0  E666 0000 2C5E                           3895+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004BE6  B29C 5040                    00004B80    3896+         STFPC FPC_R_69          save FPC
00004BEA  E760 5028 080E               00004B68    3897+         VST   V22,V1O69         save instruction result
00004BF0  07FB                                     3898+         BR    R11               return
00004BF4                                           3899+RE69     DS    0F                expected 16 byte result
00004BF4                                           3900+         DROP  R5
00004BF4  47800000 00000000                        3901          DC    XL16'47800000000000000000000000000000'
00004BFC  00000000 00000000
00004C04  00000000 00000000                        3902          DC    XL16'00000000000000005E00000000000000'
00004C0C  5E000000 00000000
                                                   3903
                                                   3904 * max  dlfloat:  2^(33)-2ulp
                                                   3905          VRR_A VCLFNL,2,0,00,00,N
00004C18                                           3906+         DS    0FD
00004C18                       00004C18            3907+         USING *,R5              base for test data and test routine
00004C18  00004CA8                                 3908+T70      DC    A(X70)            address of test routine
00004C1C  0046                                     3909+         DC    H'70'             test number
00004C1E  00                                       3910+         DC    X'00'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004C1F  D5                                       3911+          DC    CL1'N'            Y = skip cross check
00004C20  02                                       3912+          DC    HL1'2'            m3
00004C21  00                                       3913+          DC    HL1'0'            m4
00004C22  00                                       3914+FLG70     DC    X'00'             expected FPC flags
00004C23  00                                       3915+VXC70     DC    X'00'             expected VXC
00004C24  00004CDC                                 3916+V2_70     DC    A(RE70+16)        address of v2: 16-byte packed decimal
00004C28  E5C3D3C6 D5D34040                        3917+          DC    CL8'VCLFNL'       instruction name
00004C30  00000010                                 3918+          DC    A(16)             result length
00004C34  00004CCC                                 3919+          DC    A(RE70)           address of expected resul
00004C38  00000000 00000000                        3920+          DS    FD                gap
00004C40  00000000 00000000                        3921+V1O70     DS    XL16              V1 output
00004C48  00000000 00000000
00004C50  00000000 00000000                        3922+          DS    FD                   gap
00004C58  00000000                                 3923+FPC_R_70  DS    F                 FPC after instruction
00004C60  00000000 00000000                        3924+          DS    FD                   gap
00004C68  40404040 40404040                        3925+          DC    CL8' '            was cross check skipped?
00004C70  00000000 00000000                        3926+          DS    FD                   gap
00004C78  00000000 00000000                        3927+XCO70     DS    XL16              Cross check Output
00004C80  00000000 00000000
00004C88  00000000 00000000                        3928+          DS    FD                   gap
00004C90  00000000                                 3929+FPC_XC_70 DS    F                 FPC after cross check
00004C98  00000000 00000000                        3930+          DS    FD                   gap
00004CA0  00000000                                 3931+          DS    F                 debug area
00004CA4  00000000                                 3932+          DS    F
                                                   3933+*
00004CA8                                           3934+X70       DS    0F
00004CA8  B29D 85A4                     000007A4   3935+          LFPC  FPCMOFF           initialize FPC
00004CAC  E320 500C 0014                00004C24   3936+          LGF   R2,V2_70          get v2
00004CB2  E762 0000 0806                00000000   3937+          VL    V22,0(R2)
00004CB8  E666 0000 2C5E                           3938+          VCLFNL V22,V22,2,0      test instruction (dest is source)
00004CBE  B29C 5040                     00004C58   3939+          STFPC FPC_R_70          save FPC
00004CC2  E760 5028 080E                00004C40   3940+          VST   V22,V1O70         save instruction result
00004CC8  07FB                                     3941+          BR    R11               return
00004CCC                                           3942+RE70      DS    0F                expected 16 byte result
00004CCC                                           3943+          DROP  R5
00004CCC  4FFF8000 00000000                        3944           DC    XL16'4FFF8000000000000000000000000000'
00004CD4  00000000 00000000
00004CDC  00000000 00000000                        3945           DC    XL16'00000000000000007FFE000000000000'
00004CE4  7FFE0000 00000000
                                                   3946
                                                   3947 * min  dlfloat: 2^(-31)*+ulp
                                                   3948           VRR_A VCLFNL,2,0,00,00,N
00004CF0                                           3949+          DS    0FD
00004CF0                        00004CF0           3950+          USING *,R5              base for test data and test routine
00004CF0  00004D80                                 3951+T71       DC    A(X71)            address of test routine
00004CF4  0047                                     3952+          DC    H'71'             test number
00004CF6  00                                       3953+          DC    X'00'
00004CF7  D5                                       3954+          DC    CL1'N'            Y = skip cross check
00004CF8  02                                       3955+          DC    HL1'2'            m3
00004CF9  00                                       3956+          DC    HL1'0'            m4
00004CFA  00                                       3957+FLG71     DC    X'00'             expected FPC flags
00004CFB  00                                       3958+VXC71     DC    X'00'             expected VXC
00004CFC  00004DB4                                 3959+V2_71     DC    A(RE71+16)        address of v2: 16-byte packed decimal
00004D00  E5C3D3C6 D5D34040                        3960+          DC    CL8'VCLFNL'       instruction name
00004D08  00000010                                 3961+          DC    A(16)             result length
00004D0C  00004DA4                                 3962+          DC    A(RE71)           address of expected resul
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004D10  00000000 00000000                        3963+          DS    FD                gap
00004D18  00000000 00000000                        3964+V1O71     DS    XL16              V1 output
00004D20  00000000 00000000
00004D28  00000000 00000000                        3965+          DS    FD                   gap
00004D30  00000000                                 3966+FPC_R_71  DS    F                 FPC after instruction
00004D38  00000000 00000000                        3967+          DS    FD                   gap
00004D40  40404040 40404040                        3968+          DC    CL8' '            was cross check skipped?
00004D48  00000000 00000000                        3969+          DS    FD                   gap
00004D50  00000000 00000000                        3970+XCO71     DS    XL16              Cross check Output
00004D58  00000000 00000000
00004D60  00000000 00000000                        3971+          DS    FD                   gap
00004D68  00000000                                 3972+FPC_XC_71 DS    F                 FPC after cross check
00004D70  00000000 00000000                        3973+          DS    FD                   gap
00004D78  00000000                                 3974+          DS    F                 debug area
00004D7C  00000000                                 3975+          DS    F
                                                   3976+*
00004D80                                           3977+X71       DS    0F
00004D80  B29D 85A4                     000007A4   3978+          LFPC  FPCMOFF           initialize FPC
00004D84  E320 500C 0014                00004CFC   3979+          LGF   R2,V2_71          get v2
00004D8A  E762 0000 0806                00000000   3980+          VL    V22,0(R2)
00004D90  E666 0000 2C5E                           3981+          VCLFNL V22,V22,2,0      test instruction (dest is source)
00004D96  B29C 5040                     00004D30   3982+          STFPC FPC_R_71          save FPC
00004D9A  E760 5028 080E                00004D18   3983+          VST   V22,V1O71         save instruction result
00004DA0  07FB                                     3984+          BR    R11               return
00004DA4                                           3985+RE71      DS    0F                expected 16 byte result
00004DA4                                           3986+          DROP  R5
00004DA4  30004000 00000000                        3987           DC    XL16'30004000000000000000000000000000'
00004DAC  00000000 00000000
00004DB4  00000000 00000000                        3988           DC    XL16'00000000000000000001000000000000'
00004DBC  00010000 00000000
                                                   3989
                                                   3990 * +Infinity, -Infinity
                                                   3991           VRR_A VCLFNL,2,0,80,00,S          skip xcheck - includes NAN
00004DC8                                           3992+          DS    0FD
00004DC8                        00004DC8           3993+          USING *,R5              base for test data and test routine
00004DC8  00004E58                                 3994+T72       DC    A(X72)            address of test routine
00004DCC  0048                                     3995+          DC    H'72'             test number
00004DCE  00                                       3996+          DC    X'00'
00004DCF  E2                                       3997+          DC    CL1'S'            Y = skip cross check
00004DD0  02                                       3998+          DC    HL1'2'            m3
00004DD1  00                                       3999+          DC    HL1'0'            m4
00004DD2  80                                       4000+FLG72     DC    X'80'             expected FPC flags
00004DD3  00                                       4001+VXC72     DC    X'00'             expected VXC
00004DD4  00004E8C                                 4002+V2_72     DC    A(RE72+16)        address of v2: 16-byte packed decimal
00004DD8  E5C3D3C6 D5D34040                        4003+          DC    CL8'VCLFNL'       instruction name
00004DE0  00000010                                 4004+          DC    A(16)             result length
00004DE4  00004E7C                                 4005+          DC    A(RE72)           address of expected resul
00004DE8  00000000 00000000                        4006+          DS    FD                gap
00004DF0  00000000 00000000                        4007+V1O72     DS    XL16              V1 output
00004DF8  00000000 00000000
00004E00  00000000 00000000                        4008+          DS    FD                   gap
00004E08  00000000                                 4009+FPC_R_72  DS    F                 FPC after instruction
00004E10  00000000 00000000                        4010+          DS    FD                   gap
00004E18  40404040 40404040                        4011+          DC    CL8' '            was cross check skipped?
00004E20  00000000 00000000                        4012+          DS    FD                   gap
00004E28  00000000 00000000                        4013+XCO72     DS    XL16              Cross check Output
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004E30  00000000 00000000
00004E38  00000000 00000000                        4014+         DS    FD                   gap
00004E40  00000000                                 4015+FPC_XC_72 DS   F                 FPC after cross check
00004E48  00000000 00000000                        4016+         DS    FD                   gap
00004E50  00000000                                 4017+         DS    F                 debug area
00004E54  00000000                                 4018+         DS    F
                                                   4019+*
00004E58                                           4020+X72      DS    0F
00004E58  B29D 85A4                     000007A4   4021+         LFPC  FPCMOFF           initialize FPC
00004E5C  E320 500C 0014                00004DD4   4022+         LGF   R2,V2_72          get v2
00004E62  E762 0000 0806                00000000   4023+         VL    V22,0(R2)
00004E68  E666 0000 2C5E                           4024+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00004E6E  B29C 5040                     00004E08   4025+         STFPC FPC_R_72          save FPC
00004E72  E760 5028 080E                00004DF0   4026+         VST   V22,V1O72         save instruction result
00004E78  07FB                                     4027+         BR    R11               return
00004E7C                                           4028+RE72     DS    0F                expected 16 byte result
00004E7C                                           4029+         DROP  R5
00004E7C  7FC00000 00000000                        4030          DC    XL16'7FC0000000000007FC0000000000000'
00004E84  7FC00000 00000000
00004E8C  00000000 00000000                        4031          DC    XL16'0000000000000007FFF0000FFFF0000'
00004E94  7FFF0000 FFFF0000
                                                   4032
                                                   4033 * inexact - bad m3
                                                   4034          VRR_A VCLFNL,5,0,08,00,S                skip xc - inexact
00004EA0                                           4035+         DS    0FD
00004EA0                        00004EA0           4036+         USING *,R5              base for test data and test routine
00004EA0  00004F30                                 4037+T73      DC    A(X73)            address of test routine
00004EA4  0049                                     4038+         DC    H'73'             test number
00004EA6  00                                       4039+         DC    X'00'
00004EA7  E2                                       4040+         DC    CL1'S'            Y = skip cross check
00004EA8  05                                       4041+         DC    HL1'5'            m3
00004EA9  00                                       4042+         DC    HL1'0'            m4
00004EAA  08                                       4043+FLG73    DC    X'08'             expected FPC flags
00004EAB  00                                       4044+VXC73    DC    X'00'             expected VXC
00004EAC  00004F64                                 4045+V2_73    DC    A(RE73+16)        address of v2: 16-byte packed decimal
00004EB0  E5C3D3C6 D5D34040                        4046+         DC    CL8'VCLFNL'       instruction name
00004EB8  00000010                                 4047+         DC    A(16)             result length
00004EBC  00004F54                                 4048+         DC    A(RE73)           address of expected resul
00004EC0  00000000 00000000                        4049+         DS    FD                gap
00004EC8  00000000 00000000                        4050+V1O73    DS    XL16              V1 output
00004ED0  00000000 00000000
00004ED8  00000000 00000000                        4051+         DS    FD                   gap
00004EE0  00000000                                 4052+FPC_R_73 DS    F                 FPC after instruction
00004EE8  00000000 00000000                        4053+         DS    FD                   gap
00004EF0  40404040 40404040                        4054+         DC    CL8' '            was cross check skipped?
00004EF8  00000000 00000000                        4055+         DS    FD                   gap
00004F00  00000000 00000000                        4056+XCO73    DS    XL16              Cross check Output
00004F08  00000000 00000000
00004F10  00000000 00000000                        4057+         DS    FD                   gap
00004F18  00000000                                 4058+FPC_XC_73 DS   F                 FPC after cross check
00004F20  00000000 00000000                        4059+         DS    FD                   gap
00004F28  00000000                                 4060+         DS    F                 debug area
00004F2C  00000000                                 4061+         DS    F
                                                   4062+*
00004F30                                           4063+X73      DS    0F
00004F30  B29D 85A4                     000007A4   4064+         LFPC  FPCMOFF           initialize FPC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004F34  E320 500C 0014                00004EAC  4065+         LGF   R2,V2_73          get v2
00004F3A  E762 0000 0806                00000000  4066+         VL    V22,0(R2)
00004F40  E666 0000 5C5E                          4067+         VCLFNL V22,V22,5,0      test instruction (dest is source)
00004F46  B29C 5040                     00004EE0  4068+         STFPC FPC_R_73          save FPC
00004F4A  E760 5028 080E                00004EC8  4069+         VST   V22,V1O73         save instruction result
00004F50  07FB                                    4070+         BR    R11               return
00004F54                                          4071+RE73     DS    0F                expected 16 byte result
00004F54                                          4072+         DROP  R5
00004F54  00000000 00000000                       4073          DC    XL16'00000000000000000000000000000000'
00004F5C  00000000 00000000
00004F64  00000000 0000F000                       4074          DC    XL16'000000000000F0000001000000000000'
00004F6C  00010000 00000000
                                                  4075
                                                  4076 * inexact - bad m4
                                                  4077          VRR_A VCLFNL,2,5,08,00,S                    skip xc - inexact
00004F78                                          4078+         DS    0FD
00004F78                        00004F78          4079+         USING *,R5              base for test data and test routine
00004F78  00005008                                4080+T74      DC    A(X74)            address of test routine
00004F7C  004A                                    4081+         DC    H'74'             test number
00004F7E  00                                      4082+         DC    X'00'
00004F7F  E2                                      4083+         DC    CL1'S'            Y = skip cross check
00004F80  02                                      4084+         DC    HL1'2'            m3
00004F81  05                                      4085+         DC    HL1'5'            m4
00004F82  08                                      4086+FLG74    DC    X'08'             expected FPC flags
00004F83  00                                      4087+VXC74    DC    X'00'             expected VXC
00004F84  0000503C                                4088+V2_74    DC    A(RE74+16)        address of v2: 16-byte packed decimal
00004F88  E5C3D3C6 D5D34040                       4089+         DC    CL8'VCLFNL'       instruction name
00004F90  00000010                                4090+         DC    A(16)             result length
00004F94  0000502C                                4091+         DC    A(RE74)           address of expected resul
00004F98  00000000 00000000                       4092+         DS    FD                gap
00004FA0  00000000 00000000                       4093+V1O74    DS    XL16              V1 output
00004FA8  00000000 00000000
00004FB0  00000000 00000000                       4094+         DS    FD                   gap
00004FB8  00000000                                4095+FPC_R_74 DS    F                 FPC after instruction
00004FC0  00000000 00000000                       4096+         DS    FD                   gap
00004FC8  40404040 40404040                       4097+         DC    CL8' '            was cross check skipped?
00004FD0  00000000 00000000                       4098+         DS    FD                   gap
00004FD8  00000000 00000000                       4099+XCO74    DS    XL16              Cross check Output
00004FE0  00000000 00000000
00004FE8  00000000 00000000                       4100+         DS    FD                   gap
00004FF0  00000000                                4101+FPC_XC_74 DS   F                 FPC after cross check
00004FF8  00000000 00000000                       4102+         DS    FD                   gap
00005000  00000000                                4103+         DS    F                 debug area
00005004  00000000                                4104+         DS    F
                                                  4105+*
00005008                                          4106+X74      DS    0F
00005008  B29D 85A4                     000007A4  4107+         LFPC  FPCMOFF           initialize FPC
0000500C  E320 500C 0014                00004F84  4108+         LGF   R2,V2_74          get v2
00005012  E762 0000 0806                00000000  4109+         VL    V22,0(R2)
00005018  E666 0005 2C5E                          4110+         VCLFNL V22,V22,2,5      test instruction (dest is source)
0000501E  B29C 5040                     00004FB8  4111+         STFPC FPC_R_74          save FPC
00005022  E760 5028 080E                00004FA0  4112+         VST   V22,V1O74         save instruction result
00005028  07FB                                    4113+         BR    R11               return
0000502C                                          4114+RE74     DS    0F                expected 16 byte result
0000502C                                          4115+         DROP  R5
0000502C  00000000 00000000                       4116          DC    XL16'00000000000000000000000000000000'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005034  00000000 00000000
0000503C  00000000 0000F000                         4117          DC    XL16'000000000000F0000001000000000000'
00005044  00010000 00000000
                                                    4118
                                                    4119 * more tests
                                                    4120 * +3.140625, -3.140625
                                                    4121          VRR_A VCLFNL,2,0,00,00,N
00005050                                            4122+         DS    0FD
00005050                      00005050              4123+         USING *,R5              base for test data and test routine
00005050  000050E0                                  4124+T75      DC    A(X75)            address of test routine
00005054  004B                                      4125+         DC    H'75'             test number
00005056  00                                        4126+         DC    X'00'
00005057  D5                                        4127+         DC    CL1'N'            Y = skip cross check
00005058  02                                        4128+         DC    HL1'2'            m3
00005059  00                                        4129+         DC    HL1'0'            m4
0000505A  00                                        4130+FLG75    DC    X'00'             expected FPC flags
0000505B  00                                        4131+VXC75    DC    X'00'             expected VXC
0000505C  00005114                                  4132+V2_75    DC    A(RE75+16)        address of v2: 16-byte packed decimal
00005060  E5C3D3C6 D5D34040                         4133+         DC    CL8'VCLFNL'       instruction name
00005068  00000010                                  4134+         DC    A(16)             result length
0000506C  00005104                                  4135+         DC    A(RE75)           address of expected resul
00005070  00000000 00000000                         4136+         DS    FD                gap
00005078  00000000 00000000                         4137+V1O75    DS    XL16              V1 output
00005080  00000000 00000000
00005088  00000000 00000000                         4138+         DS    FD                   gap
00005090  00000000                                  4139+FPC_R_75 DS    F                 FPC after instruction
00005098  00000000 00000000                         4140+         DS    FD                   gap
000050A0  40404040 40404040                         4141+         DC    CL8' '            was cross check skipped?
000050A8  00000000 00000000                         4142+         DS    FD                   gap
000050B0  00000000 00000000                         4143+XCO75    DS    XL16              Cross check Output
000050B8  00000000 00000000
000050C0  00000000 00000000                         4144+         DS    FD                   gap
000050C8  00000000                                  4145+FPC_XC_75 DS   F                 FPC after cross check
000050D0  00000000 00000000                         4146+         DS    FD                   gap
000050D8  00000000                                  4147+         DS    F                 debug area
000050DC  00000000                                  4148+         DS    F
                                                    4149+*
000050E0                                            4150+X75      DS    0F
000050E0  B29D 85A4                     000007A4    4151+         LFPC  FPCMOFF           initialize FPC
000050E4  E320 500C 0014                0000505C    4152+         LGF   R2,V2_75          get v2
000050EA  E762 0000 0806                00000000    4153+         VL    V22,0(R2)
000050F0  E666 0000 2C5E                            4154+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000050F6  B29C 5040                     00005090    4155+         STFPC FPC_R_75          save FPC
000050FA  E760 5028 080E                00005078    4156+         VST   V22,V1O75         save instruction result
00005100  07FB                                      4157+         BR    R11               return
00005104                                            4158+RE75     DS    0F                expected 16 byte result
00005104                                            4159+         DROP  R5
00005104  40890000 00000000                         4160          DC    XL16'4089000000000000C089000000000000'
0000510C  C0890000 00000000
00005114  00000000 00000000                         4161          DC    XL16'00000000000000004224000 0C2240000'
0000511C  42240000 C2240000
                                                    4162
                                                    4163
                                                    4164 * +27.15625, -27.15625
                                                    4165          VRR_A VCLFNL,2,0,00,00,N
00005128                                            4166+         DS    0FD
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005128                     00005128             4167+         USING *,R5              base for test data and test routine
00005128  000051B8                                4168+T76      DC    A(X76)            address of test routine
0000512C  004C                                    4169+         DC    H'76'             test number
0000512E  00                                      4170+         DC    X'00'
0000512F  D5                                      4171+         DC    CL1'N'            Y = skip cross check
00005130  02                                      4172+         DC    HL1'2'            m3
00005131  00                                      4173+         DC    HL1'0'            m4
00005132  00                                      4174+FLG76    DC    X'00'             expected FPC flags
00005133  00                                      4175+VXC76    DC    X'00'             expected VXC
00005134  000051EC                                4176+V2_76    DC    A(RE76+16)        address of v2: 16-byte packed decimal
00005138  E5C3D3C6 D5D34040                       4177+         DC    CL8'VCLFNL'       instruction name
00005140  00000010                                4178+         DC    A(16)             result length
00005144  000051DC                                4179+         DC    A(RE76)           address of expected resul
00005148  00000000 00000000                       4180+         DS    FD                gap
00005150  00000000 00000000                       4181+V1O76    DS    XL16              V1 output
00005158  00000000 00000000
00005160  00000000 00000000                       4182+         DS    FD                   gap
00005168  00000000                                4183+FPC_R_76 DS    F                 FPC after instruction
00005170  00000000 00000000                       4184+         DS    FD                   gap
00005178  40404040 40404040                       4185+         DC    CL8' '            was cross check skipped?
00005180  00000000 00000000                       4186+         DS    FD                   gap
00005188  00000000 00000000                       4187+XCO76    DS    XL16              Cross check Output
00005190  00000000 00000000
00005198  00000000 00000000                       4188+         DS    FD                   gap
000051A0  00000000                                4189+FPC_XC_76 DS   F                 FPC after cross check
000051A8  00000000 00000000                       4190+         DS    FD                   gap
000051B0  00000000                                4191+         DS    F                 debug area
000051B4  00000000                                4192+         DS    F
                                                  4193+*
000051B8                                          4194+X76      DS    0F
000051B8  B29D 85A4                     000007A4  4195+         LFPC  FPCMOFF           initialize FPC
000051BC  E320 500C 0014                00005134  4196+         LGF   R2,V2_76          get v2
000051C2  E762 0000 0806                00000000  4197+         VL    V22,0(R2)
000051C8  E666 0000 2C5E                          4198+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000051CE  B29C 5040                     00005168  4199+         STFPC FPC_R_76          save FPC
000051D2  E760 5028 080E                00005150  4200+         VST   V22,V1O76         save instruction result
000051D8  07FB                                    4201+         BR    R11               return
000051DC                                          4202+RE76     DS    0F                expected 16 byte result
000051DC                                          4203+         DROP  R5
000051DC  3BD94000 00000000                       4204          DC    XL16'3BD9400000000000BBD9400000000000'
000051E4  BBD94000 00000000
000051EC  00000000 00000000                       4205          DC    XL16'0000000000000002F650000AF650000'
000051F4  2F650000 AF650000
                                                  4206
                                                  4207 * +65504, -65504
                                                  4208          VRR_A VCLFNL,2,0,00,00,N
00005200                                          4209+         DS    0FD
00005200                     00005200             4210+         USING *,R5              base for test data and test routine
00005200  00005290                                4211+T77      DC    A(X77)            address of test routine
00005204  004D                                    4212+         DC    H'77'             test number
00005206  00                                      4213+         DC    X'00'
00005207  D5                                      4214+         DC    CL1'N'            Y = skip cross check
00005208  02                                      4215+         DC    HL1'2'            m3
00005209  00                                      4216+         DC    HL1'0'            m4
0000520A  00                                      4217+FLG77    DC    X'00'             expected FPC flags
0000520B  00                                      4218+VXC77    DC    X'00'             expected VXC
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000520C  000052C4                                 4219+V2_77    DC    A(RE77+16)        address of v2: 16-byte packed decimal
00005210  E5C3D3C6 D5D34040                        4220+         DC    CL8'VCLFNL'       instruction name
00005218  00000010                                 4221+         DC    A(16)             result length
0000521C  000052B4                                 4222+         DC    A(RE77)           address of expected resul
00005220  00000000 00000000                        4223+         DS    FD                gap
00005228  00000000 00000000                        4224+V1O77    DS    XL16              V1 output
00005230  00000000 00000000
00005238  00000000 00000000                        4225+         DS    FD                   gap
00005240  00000000                                 4226+FPC_R_77 DS    F                 FPC after instruction
00005248  00000000 00000000                        4227+         DS    FD                   gap
00005250  40404040 40404040                        4228+         DC    CL8' '            was cross check skipped?
00005258  00000000 00000000                        4229+         DS    FD                   gap
00005260  00000000 00000000                        4230+XCO77    DS    XL16              Cross check Output
00005268  00000000 00000000
00005270  00000000 00000000                        4231+         DS    FD                   gap
00005278  00000000                                 4232+FPC_XC_77 DS   F                 FPC after cross check
00005280  00000000 00000000                        4233+         DS    FD                   gap
00005288  00000000                                 4234+         DS    F                 debug area
0000528C  00000000                                 4235+         DS    F
                                                   4236+*
00005290                                           4237+X77      DS    0F
00005290  B29D 85A4                     000007A4   4238+         LFPC  FPCMOFF           initialize FPC
00005294  E320 500C 0014                0000520C   4239+         LGF   R2,V2_77          get v2
0000529A  E762 0000 0806                00000000   4240+         VL    V22,0(R2)
000052A0  E666 0000 2C5E                           4241+         VCLFNL V22,V22,2,0      test instruction (dest is source)
000052A6  B29C 5040                     00005240   4242+         STFPC FPC_R_77          save FPC
000052AA  E760 5028 080E                00005228   4243+         VST   V22,V1O77         save instruction result
000052B0  07FB                                     4244+         BR    R11               return
000052B4                                           4245+RE77     DS    0F                expected 16 byte result
000052B4                                           4246+         DROP  R5
000052B4  47800000 00000000                        4247          DC    XL16'4780000000000000C780000000000000'
000052BC  C7800000 00000000
000052C4  00000000 00000000                        4248          DC    XL16'0000000000000000005E000000DE000000'
000052CC  5E000000 DE000000
                                                   4249
                                                   4250 * +Normal, -Normal (2.5)
                                                   4251          VRR_A VCLFNL,2,0,00,00,N
000052D8                                           4252+         DS    0FD
000052D8                        000052D8           4253+         USING *,R5              base for test data and test routine
000052D8  00005368                                 4254+T78      DC    A(X78)            address of test routine
000052DC  004E                                     4255+         DC    H'78'             test number
000052DE  00                                       4256+         DC    X'00'
000052DF  D5                                       4257+         DC    CL1'N'            Y = skip cross check
000052E0  02                                       4258+         DC    HL1'2'            m3
000052E1  00                                       4259+         DC    HL1'0'            m4
000052E2  00                                       4260+FLG78    DC    X'00'             expected FPC flags
000052E3  00                                       4261+VXC78    DC    X'00'             expected VXC
000052E4  0000539C                                 4262+V2_78    DC    A(RE78+16)        address of v2: 16-byte packed decimal
000052E8  E5C3D3C6 D5D34040                        4263+         DC    CL8'VCLFNL'       instruction name
000052F0  00000010                                 4264+         DC    A(16)             result length
000052F4  0000538C                                 4265+         DC    A(RE78)           address of expected resul
000052F8  00000000 00000000                        4266+         DS    FD                gap
00005300  00000000 00000000                        4267+V1O78    DS    XL16              V1 output
00005308  00000000 00000000
00005310  00000000 00000000                        4268+         DS    FD                   gap
00005318  00000000                                 4269+FPC_R_78 DS    F                 FPC after instruction
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005320  00000000 00000000                        4270+          DS    FD                    gap
00005328  40404040 40404040                        4271+          DC    CL8' '             was cross check skipped?
00005330  00000000 00000000                        4272+          DS    FD                    gap
00005338  00000000 00000000                        4273+XCO78     DS    XL16               Cross check Output
00005340  00000000 00000000
00005348  00000000 00000000                        4274+          DS    FD                    gap
00005350  00000000                                 4275+FPC_XC_78 DS    F                  FPC after cross check
00005358  00000000 00000000                        4276+          DS    FD                    gap
00005360  00000000                                 4277+          DS    F                  debug area
00005364  00000000                                 4278+          DS    F
                                                   4279+*
00005368                                           4280+X78       DS    0F
00005368  B29D 85A4                     000007A4   4281+          LFPC  FPCMOFF            initialize FPC
0000536C  E320 500C 0014                000052E4   4282+          LGF   R2,V2_78           get v2
00005372  E762 0000 0806                00000000   4283+          VL    V22,0(R2)
00005378  E666 0000 2C5E                           4284+          VCLFNL V22,V22,2,0       test instruction (dest is source)
0000537E  B29C 5040                     00005318   4285+          STFPC FPC_R_78           save FPC
00005382  E760 5028 080E                00005300   4286+          VST   V22,V1O78          save instruction result
00005388  07FB                                     4287+          BR    R11                return
0000538C                                           4288+RE78      DS    0F                 expected 16 byte result
0000538C                                           4289+          DROP  R5
0000538C  40200000 00000000                        4290           DC    XL16'4020000000000000C020000000000000'
00005394  C0200000 00000000
0000539C  00000000 00000000                        4291           DC    XL16'00000000000000004080000C0800000'
000053A4  40800000 C0800000
                                                   4292
                                                   4293 * +0.00006097, -0.00006097 (about)
                                                   4294           VRR_A VCLFNL,2,0,00,00,N
000053B0                                           4295+          DS    0FD
000053B0                        000053B0           4296+          USING *,R5               base for test data and test routine
000053B0  00005440                                 4297+T79       DC    A(X79)             address of test routine
000053B4  004F                                     4298+          DC    H'79'              test number
000053B6  00                                       4299+          DC    X'00'
000053B7  D5                                       4300+          DC    CL1'N'             Y = skip cross check
000053B8  02                                       4301+          DC    HL1'2'             m3
000053B9  00                                       4302+          DC    HL1'0'             m4
000053BA  00                                       4303+FLG79     DC    X'00'              expected FPC flags
000053BB  00                                       4304+VXC79     DC    X'00'              expected VXC
000053BC  00005474                                 4305+V2_79     DC    A(RE79+16)         address of v2: 16-byte packed decimal
000053C0  E5C3D3C6 D5D34040                        4306+          DC    CL8'VCLFNL'        instruction name
000053C8  00000010                                 4307+          DC    A(16)              result length
000053CC  00005464                                 4308+          DC    A(RE79)            address of expected resul
000053D0  00000000 00000000                        4309+          DS    FD                 gap
000053D8  00000000 00000000                        4310+V1O79     DS    XL16               V1 output
000053E0  00000000 00000000
000053E8  00000000 00000000                        4311+          DS    FD                    gap
000053F0  00000000                                 4312+FPC_R_79 DS    F                  FPC after instruction
000053F8  00000000 00000000                        4313+          DS    FD                    gap
00005400  40404040 40404040                        4314+          DC    CL8' '             was cross check skipped?
00005408  00000000 00000000                        4315+          DS    FD                    gap
00005410  00000000 00000000                        4316+XCO79     DS    XL16               Cross check Output
00005418  00000000 00000000
00005420  00000000 00000000                        4317+          DS    FD                    gap
00005428  00000000                                 4318+FPC_XC_79 DS    F                  FPC after cross check
00005430  00000000 00000000                        4319+          DS    FD                    gap
00005438  00000000                                 4320+          DS    F                  debug area
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000543C  00000000                                4321+         DS    F
                                                  4322+*
00005440                                          4323+X79      DS    0F
00005440  B29D 85A4                     000007A4  4324+         LFPC  FPCMOFF           initialize FPC
00005444  E320 500C 0014                000053BC  4325+         LGF   R2,V2_79          get v2
0000544A  E762 0000 0806                00000000  4326+         VL    V22,0(R2)
00005450  E666 0000 2C5E                          4327+         VCLFNL V22,V22,2,0      test instruction (dest is source)
00005456  B29C 5040                     000053F0  4328+         STFPC FPC_R_79          save FPC
0000545A  E760 5028 080E                000053D8  4329+         VST   V22,V1O79         save instruction result
00005460  07FB                                    4330+         BR    R11               return
00005464                                          4331+RE79     DS    0F                expected 16 byte result
00005464                                          4332+         DROP  R5
00005464  387FC000 00000000                       4333          DC    XL16'387FC00000000000B87FC00000000000'
0000546C  B87FC000 00000000
00005474  00000000 00000000                       4334          DC    XL16'00000000000000021FF0000A1FF0000'
0000547C  21FF0000 A1FF0000
                                                  4335
                                                  4336
                                                  4337
00005484  00000000                                4338          DC    F'0'     END OF TABLE
00005488  00000000                                4339          DC    F'0'
                                                  4340 *
                                                  4341 * table of pointers to individual tests
                                                  4342 *
0000548C                                          4343 E6TESTS  DS    0F
                                                  4344          PTTABLE
0000548C                                          4345+TTABLE   DS    0F
0000548C  000011E0                                4346+         DC    A(T1)             TEST &CUR
00005490  000012B8                                4347+         DC    A(T2)             TEST &CUR
00005494  00001390                                4348+         DC    A(T3)             TEST &CUR
00005498  00001468                                4349+         DC    A(T4)             TEST &CUR
0000549C  00001540                                4350+         DC    A(T5)             TEST &CUR
000054A0  00001618                                4351+         DC    A(T6)             TEST &CUR
000054A4  000016F0                                4352+         DC    A(T7)             TEST &CUR
000054A8  000017C8                                4353+         DC    A(T8)             TEST &CUR
000054AC  000018A0                                4354+         DC    A(T9)             TEST &CUR
000054B0  00001978                                4355+         DC    A(T10)            TEST &CUR
000054B4  00001A50                                4356+         DC    A(T11)            TEST &CUR
000054B8  00001B28                                4357+         DC    A(T12)            TEST &CUR
000054BC  00001C00                                4358+         DC    A(T13)            TEST &CUR
000054C0  00001CD8                                4359+         DC    A(T14)            TEST &CUR
000054C4  00001DB0                                4360+         DC    A(T15)            TEST &CUR
000054C8  00001E88                                4361+         DC    A(T16)            TEST &CUR
000054CC  00001F60                                4362+         DC    A(T17)            TEST &CUR
000054D0  00002038                                4363+         DC    A(T18)            TEST &CUR
000054D4  00002110                                4364+         DC    A(T19)            TEST &CUR
000054D8  000021E8                                4365+         DC    A(T20)            TEST &CUR
000054DC  000022C0                                4366+         DC    A(T21)            TEST &CUR
000054E0  00002398                                4367+         DC    A(T22)            TEST &CUR
000054E4  00002470                                4368+         DC    A(T23)            TEST &CUR
000054E8  00002548                                4369+         DC    A(T24)            TEST &CUR
000054EC  00002620                                4370+         DC    A(T25)            TEST &CUR
000054F0  000026F8                                4371+         DC    A(T26)            TEST &CUR
000054F4  000027D0                                4372+         DC    A(T27)            TEST &CUR
000054F8  000028A8                                4373+         DC    A(T28)            TEST &CUR
000054FC  00002980                                4374+         DC    A(T29)            TEST &CUR
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005500  00002A58                          4375+         DC    A(T30)            TEST &CUR
00005504  00002B30                          4376+         DC    A(T31)            TEST &CUR
00005508  00002C08                          4377+         DC    A(T32)            TEST &CUR
0000550C  00002CE0                          4378+         DC    A(T33)            TEST &CUR
00005510  00002DB8                          4379+         DC    A(T34)            TEST &CUR
00005514  00002E90                          4380+         DC    A(T35)            TEST &CUR
00005518  00002F68                          4381+         DC    A(T36)            TEST &CUR
0000551C  00003040                          4382+         DC    A(T37)            TEST &CUR
00005520  00003118                          4383+         DC    A(T38)            TEST &CUR
00005524  000031F0                          4384+         DC    A(T39)            TEST &CUR
00005528  000032C8                          4385+         DC    A(T40)            TEST &CUR
0000552C  000033A0                          4386+         DC    A(T41)            TEST &CUR
00005530  00003478                          4387+         DC    A(T42)            TEST &CUR
00005534  00003550                          4388+         DC    A(T43)            TEST &CUR
00005538  00003628                          4389+         DC    A(T44)            TEST &CUR
0000553C  00003700                          4390+         DC    A(T45)            TEST &CUR
00005540  000037D8                          4391+         DC    A(T46)            TEST &CUR
00005544  000038B0                          4392+         DC    A(T47)            TEST &CUR
00005548  00003988                          4393+         DC    A(T48)            TEST &CUR
0000554C  00003A60                          4394+         DC    A(T49)            TEST &CUR
00005550  00003B38                          4395+         DC    A(T50)            TEST &CUR
00005554  00003C10                          4396+         DC    A(T51)            TEST &CUR
00005558  00003CE8                          4397+         DC    A(T52)            TEST &CUR
0000555C  00003DC0                          4398+         DC    A(T53)            TEST &CUR
00005560  00003E98                          4399+         DC    A(T54)            TEST &CUR
00005564  00003F70                          4400+         DC    A(T55)            TEST &CUR
00005568  00004048                          4401+         DC    A(T56)            TEST &CUR
0000556C  00004120                          4402+         DC    A(T57)            TEST &CUR
00005570  000041F8                          4403+         DC    A(T58)            TEST &CUR
00005574  000042D0                          4404+         DC    A(T59)            TEST &CUR
00005578  000043A8                          4405+         DC    A(T60)            TEST &CUR
0000557C  00004480                          4406+         DC    A(T61)            TEST &CUR
00005580  00004558                          4407+         DC    A(T62)            TEST &CUR
00005584  00004630                          4408+         DC    A(T63)            TEST &CUR
00005588  00004708                          4409+         DC    A(T64)            TEST &CUR
0000558C  000047E0                          4410+         DC    A(T65)            TEST &CUR
00005590  000048B8                          4411+         DC    A(T66)            TEST &CUR
00005594  00004990                          4412+         DC    A(T67)            TEST &CUR
00005598  00004A68                          4413+         DC    A(T68)            TEST &CUR
0000559C  00004B40                          4414+         DC    A(T69)            TEST &CUR
000055A0  00004C18                          4415+         DC    A(T70)            TEST &CUR
000055A4  00004CF0                          4416+         DC    A(T71)            TEST &CUR
000055A8  00004DC8                          4417+         DC    A(T72)            TEST &CUR
000055AC  00004EA0                          4418+         DC    A(T73)            TEST &CUR
000055B0  00004F78                          4419+         DC    A(T74)            TEST &CUR
000055B4  00005050                          4420+         DC    A(T75)            TEST &CUR
000055B8  00005128                          4421+         DC    A(T76)            TEST &CUR
000055BC  00005200                          4422+         DC    A(T77)            TEST &CUR
000055C0  000052D8                          4423+         DC    A(T78)            TEST &CUR
000055C4  000053B0                          4424+         DC    A(T79)            TEST &CUR
                                            4425+*
000055C8  00000000                          4426+         DC    A(0)              END OF TABLE
000055CC  00000000                          4427+         DC    A(0)
                                            4428
000055D0  00000000                          4429          DC    F'0'     END OF TABLE
000055D4  00000000                          4430          DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                          4432 ************************************************************************
                                          4433 *        Register equates
                                          4434 ************************************************************************


                             00000000  00000001  4436 R0       EQU   0
                             00000001  00000001  4437 R1       EQU   1
                             00000002  00000001  4438 R2       EQU   2
                             00000003  00000001  4439 R3       EQU   3
                             00000004  00000001  4440 R4       EQU   4
                             00000005  00000001  4441 R5       EQU   5
                             00000006  00000001  4442 R6       EQU   6
                             00000007  00000001  4443 R7       EQU   7
                             00000008  00000001  4444 R8       EQU   8
                             00000009  00000001  4445 R9       EQU   9
                             0000000A  00000001  4446 R10      EQU   10
                             0000000B  00000001  4447 R11      EQU   11
                             0000000C  00000001  4448 R12      EQU   12
                             0000000D  00000001  4449 R13      EQU   13
                             0000000E  00000001  4450 R14      EQU   14
                             0000000F  00000001  4451 R15      EQU   15


                                          4453 ************************************************************************
                                          4454 *        Register equates
                                          4455 ************************************************************************


                             00000000  00000001  4457 FPR0     EQU   0
                             00000001  00000001  4458 FPR1     EQU   1
                             00000002  00000001  4459 FPR2     EQU   2
                             00000003  00000001  4460 FPR3     EQU   3
                             00000004  00000001  4461 FPR4     EQU   4
                             00000005  00000001  4462 FPR5     EQU   5
                             00000006  00000001  4463 FPR6     EQU   6
                             00000007  00000001  4464 FPR7     EQU   7
                             00000008  00000001  4465 FPR8     EQU   8
                             00000009  00000001  4466 FPR9     EQU   9
                             0000000A  00000001  4467 FPR10    EQU   10
                             0000000B  00000001  4468 FPR11    EQU   11
                             0000000C  00000001  4469 FPR12    EQU   12
                             0000000D  00000001  4470 FPR13    EQU   13
                             0000000E  00000001  4471 FPR14    EQU   14
                             0000000F  00000001  4472 FPR15    EQU   15


                                          4474 ************************************************************************
                                          4475 *        Register equates
                                          4476 ************************************************************************


                             00000000  00000001  4478 V0       EQU   0
                             00000001  00000001  4479 V1       EQU   1
                             00000002  00000001  4480 V2       EQU   2
                             00000003  00000001  4481 V3       EQU   3
                             00000004  00000001  4482 V4       EQU   4
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                               00000005  00000001  4483 V5       EQU   5
                               00000006  00000001  4484 V6       EQU   6
                               00000007  00000001  4485 V7       EQU   7
                               00000008  00000001  4486 V8       EQU   8
                               00000009  00000001  4487 V9       EQU   9
                               0000000A  00000001  4488 V10      EQU   10
                               0000000B  00000001  4489 V11      EQU   11
                               0000000C  00000001  4490 V12      EQU   12
                               0000000D  00000001  4491 V13      EQU   13
                               0000000E  00000001  4492 V14      EQU   14
                               0000000F  00000001  4493 V15      EQU   15
                               00000010  00000001  4494 V16      EQU   16
                               00000011  00000001  4495 V17      EQU   17
                               00000012  00000001  4496 V18      EQU   18
                               00000013  00000001  4497 V19      EQU   19
                               00000014  00000001  4498 V20      EQU   20
                               00000015  00000001  4499 V21      EQU   21
                               00000016  00000001  4500 V22      EQU   22
                               00000017  00000001  4501 V23      EQU   23
                               00000018  00000001  4502 V24      EQU   24
                               00000019  00000001  4503 V25      EQU   25
                               0000001A  00000001  4504 V26      EQU   26
                               0000001B  00000001  4505 V27      EQU   27
                               0000001C  00000001  4506 V28      EQU   28
                               0000001D  00000001  4507 V29      EQU   29
                               0000001E  00000001  4508 V30      EQU   30
                               0000001F  00000001  4509 V31      EQU   31
                                                   4510
                                                   4511          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
BEGIN	I	00000200	2	177	141	173	174	175									
CHECKRES	U	00000324	1	257	254												
CHECKVXC	U	00000316	1	252	249												
CTLR0	F	0000079C	4	621	187	188	189	190									
DECNUM	C	00001190	16	748	380	382	389	391	396	398	427	429	436	438	443	445	463
					465	472	474	479	481	497	499	506	508	513	515		
DONEXT	U	00000334	1	271													
E6TEST	4	00000000	144	762	236												
E6TESTS	F	0000548C	4	4343	229												
EDIT	X	00001164	18	743	381	390	397	428	437	444	464	473	480	498	507	514	
ENDTEST	U	0000066C	1	535	234												
EOJ	I	00000780	4	611	222	538											
EOJPSW	D	00000770	8	609	611												
FAILCONT	U	0000065C	1	525													
FAILED	F	00001000	4	664	408	424	460	527	536								
FAILMSG	U	000005F4	1	495	269												
FAILPSW	D	00000788	8	613	615												
FAILTEST	I	00000798	4	615	539												
FB0001	F	00000298	8	206	210	211	213										
FLG	X	0000000A	1	769	248	435											
FLG1	X	000011EA	1	919													
FLG10	X	00001982	1	1306													
FLG11	X	00001A5A	1	1349													
FLG12	X	00001B32	1	1392													
FLG13	X	00001C0A	1	1435													
FLG14	X	00001CE2	1	1479													
FLG15	X	00001DBA	1	1522													
FLG16	X	00001E92	1	1565													
FLG17	X	00001F6A	1	1608													
FLG18	X	00002042	1	1651													
FLG19	X	0000211A	1	1694													
FLG2	X	000012C2	1	962													
FLG20	X	000021F2	1	1737													
FLG21	X	000022CA	1	1780													
FLG22	X	000023A2	1	1824													
FLG23	X	0000247A	1	1867													
FLG24	X	00002552	1	1916													
FLG25	X	0000262A	1	1959													
FLG26	X	00002702	1	2002													
FLG27	X	000027DA	1	2045													
FLG28	X	000028B2	1	2088													
FLG29	X	0000298A	1	2131													
FLG3	X	0000139A	1	1004													
FLG30	X	00002A62	1	2175													
FLG31	X	00002B3A	1	2218													
FLG32	X	00002C12	1	2261													
FLG33	X	00002CEA	1	2304													
FLG34	X	00002DC2	1	2347													
FLG35	X	00002E9A	1	2390													
FLG36	X	00002F72	1	2434													
FLG37	X	0000304A	1	2478													
FLG38	X	00003122	1	2521													
FLG39	X	000031FA	1	2564													
FLG4	X	00001472	1	1047													
FLG40	X	000032D2	1	2607													
FLG41	X	000033AA	1	2656													

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FLG42	X	00003482	1	2699	
FLG43	X	0000355A	1	2742	
FLG44	X	00003632	1	2785	
FLG45	X	0000370A	1	2828	
FLG46	X	000037E2	1	2871	
FLG47	X	000038BA	1	2914	
FLG48	X	00003992	1	2958	
FLG49	X	00003A6A	1	3001	
FLG5	X	0000154A	1	1090	
FLG50	X	00003B42	1	3044	
FLG51	X	00003C1A	1	3087	
FLG52	X	00003CF2	1	3130	
FLG53	X	00003DCA	1	3173	
FLG54	X	00003EA2	1	3216	
FLG55	X	00003F7A	1	3260	
FLG56	X	00004052	1	3304	
FLG57	X	0000412A	1	3347	
FLG58	X	00004202	1	3390	
FLG59	X	000042DA	1	3433	
FLG6	X	00001622	1	1133	
FLG60	X	000043B2	1	3477	
FLG61	X	0000448A	1	3520	
FLG62	X	00004562	1	3563	
FLG63	X	0000463A	1	3612	
FLG64	X	00004712	1	3655	
FLG65	X	000047EA	1	3698	
FLG66	X	000048C2	1	3741	
FLG67	X	0000499A	1	3784	
FLG68	X	00004A72	1	3827	
FLG69	X	00004B4A	1	3871	
FLG7	X	000016FA	1	1176	
FLG70	X	00004C22	1	3914	
FLG71	X	00004CFA	1	3957	
FLG72	X	00004DD2	1	4000	
FLG73	X	00004EAA	1	4043	
FLG74	X	00004F82	1	4086	
FLG75	X	0000505A	1	4130	
FLG76	X	00005132	1	4174	
FLG77	X	0000520A	1	4217	
FLG78	X	000052E2	1	4260	
FLG79	X	000053BA	1	4303	
FLG8	X	000017D2	1	1220	
FLG9	X	000018AA	1	1263	
FPCMIE	X	000007B8	4	628	
FPCMIO	X	000007AC	4	625	
FPCMOFF	X	000007A4	4	623	307 325 343 361 940 983 1025 1068 1111 1154 1197 1241 1284 1327 1370 1413 1456 1500 1543 1586 1629 1672 1715 1758 1801 1845 1888 1937 1980 2023 2066 2109 2152 2196 2239 2282 2325 2368 2411 2455 2499 2542 2585 2628 2677 2720 2763 2806 2849 2892 2935 2979 3022 3065 3108 3151 3194 3237 3281 3325 3368 3411 3454 3498 3541 3584 3633 3676 3719 3762 3805 3848 3892 3935 3978 4021 4064 4107 4151 4195 4238 4281 4324
FPCMON	X	000007A8	4	624	
FPCMOV	X	000007B0	4	626	
FPCMSG	U	00000510	1	422	250
FPCMUN	X	000007B4	4	627	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
FPCPEXP	C	00001052	3	679	439			
FPCPGOT	C	00001067	3	682	446			
FPCPLINE	C	00001008	13	674	684	449		
FPCPLNG	U	00000063	1	684	448			
FPCPNAME	C	00001039	8	677	432			
FPCPNUM	C	00001015	3	675	430			
FPC_R	F	00000040	4	778	248	253	283	442	478
FPC_R_1	F	00001220	4	928	944			
FPC_R_10	F	000019B8	4	1315	1331			
FPC_R_11	F	00001A90	4	1358	1374			
FPC_R_12	F	00001B68	4	1401	1417			
FPC_R_13	F	00001C40	4	1444	1460			
FPC_R_14	F	00001D18	4	1488	1504			
FPC_R_15	F	00001DF0	4	1531	1547			
FPC_R_16	F	00001EC8	4	1574	1590			
FPC_R_17	F	00001FA0	4	1617	1633			
FPC_R_18	F	00002078	4	1660	1676			
FPC_R_19	F	00002150	4	1703	1719			
FPC_R_2	F	000012F8	4	971	987			
FPC_R_20	F	00002228	4	1746	1762			
FPC_R_21	F	00002300	4	1789	1805			
FPC_R_22	F	000023D8	4	1833	1849			
FPC_R_23	F	000024B0	4	1876	1892			
FPC_R_24	F	00002588	4	1925	1941			
FPC_R_25	F	00002660	4	1968	1984			
FPC_R_26	F	00002738	4	2011	2027			
FPC_R_27	F	00002810	4	2054	2070			
FPC_R_28	F	000028E8	4	2097	2113			
FPC_R_29	F	000029C0	4	2140	2156			
FPC_R_3	F	000013D0	4	1013	1029			
FPC_R_30	F	00002A98	4	2184	2200			
FPC_R_31	F	00002B70	4	2227	2243			
FPC_R_32	F	00002C48	4	2270	2286			
FPC_R_33	F	00002D20	4	2313	2329			
FPC_R_34	F	00002DF8	4	2356	2372			
FPC_R_35	F	00002ED0	4	2399	2415			
FPC_R_36	F	00002FA8	4	2443	2459			
FPC_R_37	F	00003080	4	2487	2503			
FPC_R_38	F	00003158	4	2530	2546			
FPC_R_39	F	00003230	4	2573	2589			
FPC_R_4	F	000014A8	4	1056	1072			
FPC_R_40	F	00003308	4	2616	2632			
FPC_R_41	F	000033E0	4	2665	2681			
FPC_R_42	F	000034B8	4	2708	2724			
FPC_R_43	F	00003590	4	2751	2767			
FPC_R_44	F	00003668	4	2794	2810			
FPC_R_45	F	00003740	4	2837	2853			
FPC_R_46	F	00003818	4	2880	2896			
FPC_R_47	F	000038F0	4	2923	2939			
FPC_R_48	F	000039C8	4	2967	2983			
FPC_R_49	F	00003AA0	4	3010	3026			
FPC_R_5	F	00001580	4	1099	1115			
FPC_R_50	F	00003B78	4	3053	3069			
FPC_R_51	F	00003C50	4	3096	3112			
FPC_R_52	F	00003D28	4	3139	3155			
FPC_R_53	F	00003E00	4	3182	3198			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES							
FPC_R_54	F	00003ED8	4	3225	3241							
FPC_R_55	F	00003FB0	4	3269	3285							
FPC_R_56	F	00004088	4	3313	3329							
FPC_R_57	F	00004160	4	3356	3372							
FPC_R_58	F	00004238	4	3399	3415							
FPC_R_59	F	00004310	4	3442	3458							
FPC_R_6	F	00001658	4	1142	1158							
FPC_R_60	F	000043E8	4	3486	3502							
FPC_R_61	F	000044C0	4	3529	3545							
FPC_R_62	F	00004598	4	3572	3588							
FPC_R_63	F	00004670	4	3621	3637							
FPC_R_64	F	00004748	4	3664	3680							
FPC_R_65	F	00004820	4	3707	3723							
FPC_R_66	F	000048F8	4	3750	3766							
FPC_R_67	F	000049D0	4	3793	3809							
FPC_R_68	F	00004AA8	4	3836	3852							
FPC_R_69	F	00004B80	4	3880	3896							
FPC_R_7	F	00001730	4	1185	1201							
FPC_R_70	F	00004C58	4	3923	3939							
FPC_R_71	F	00004D30	4	3966	3982							
FPC_R_72	F	00004E08	4	4009	4025							
FPC_R_73	F	00004EE0	4	4052	4068							
FPC_R_74	F	00004FB8	4	4095	4111							
FPC_R_75	F	00005090	4	4139	4155							
FPC_R_76	F	00005168	4	4183	4199							
FPC_R_77	F	00005240	4	4226	4242							
FPC_R_78	F	00005318	4	4269	4285							
FPC_R_79	F	000053F0	4	4312	4328							
FPC_R_8	F	00001808	4	1229	1245							
FPC_R_9	F	000018E0	4	1272	1288							
FPC_XC	F	00000078	4	784	311	314	329	332	347	350	365	368
FPC_XC_1	F	00001258	4	934								
FPC_XC_10	F	000019F0	4	1321								
FPC_XC_11	F	00001AC8	4	1364								
FPC_XC_12	F	00001BA0	4	1407								
FPC_XC_13	F	00001C78	4	1450								
FPC_XC_14	F	00001D50	4	1494								
FPC_XC_15	F	00001E28	4	1537								
FPC_XC_16	F	00001F00	4	1580								
FPC_XC_17	F	00001FD8	4	1623								
FPC_XC_18	F	000020B0	4	1666								
FPC_XC_19	F	00002188	4	1709								
FPC_XC_2	F	00001330	4	977								
FPC_XC_20	F	00002260	4	1752								
FPC_XC_21	F	00002338	4	1795								
FPC_XC_22	F	00002410	4	1839								
FPC_XC_23	F	000024E8	4	1882								
FPC_XC_24	F	000025C0	4	1931								
FPC_XC_25	F	00002698	4	1974								
FPC_XC_26	F	00002770	4	2017								
FPC_XC_27	F	00002848	4	2060								
FPC_XC_28	F	00002920	4	2103								
FPC_XC_29	F	000029F8	4	2146								
FPC_XC_3	F	00001408	4	1019								
FPC_XC_30	F	00002AD0	4	2190								
FPC_XC_31	F	00002BA8	4	2233								

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
FPC_XC_32	F	00002C80	4	2276	
FPC_XC_33	F	00002D58	4	2319	
FPC_XC_34	F	00002E30	4	2362	
FPC_XC_35	F	00002F08	4	2405	
FPC_XC_36	F	00002FE0	4	2449	
FPC_XC_37	F	000030B8	4	2493	
FPC_XC_38	F	00003190	4	2536	
FPC_XC_39	F	00003268	4	2579	
FPC_XC_4	F	000014E0	4	1062	
FPC_XC_40	F	00003340	4	2622	
FPC_XC_41	F	00003418	4	2671	
FPC_XC_42	F	000034F0	4	2714	
FPC_XC_43	F	000035C8	4	2757	
FPC_XC_44	F	000036A0	4	2800	
FPC_XC_45	F	00003778	4	2843	
FPC_XC_46	F	00003850	4	2886	
FPC_XC_47	F	00003928	4	2929	
FPC_XC_48	F	00003A00	4	2973	
FPC_XC_49	F	00003AD8	4	3016	
FPC_XC_5	F	000015B8	4	1105	
FPC_XC_50	F	00003BB0	4	3059	
FPC_XC_51	F	00003C88	4	3102	
FPC_XC_52	F	00003D60	4	3145	
FPC_XC_53	F	00003E38	4	3188	
FPC_XC_54	F	00003F10	4	3231	
FPC_XC_55	F	00003FE8	4	3275	
FPC_XC_56	F	000040C0	4	3319	
FPC_XC_57	F	00004198	4	3362	
FPC_XC_58	F	00004270	4	3405	
FPC_XC_59	F	00004348	4	3448	
FPC_XC_6	F	00001690	4	1148	
FPC_XC_60	F	00004420	4	3492	
FPC_XC_61	F	000044F8	4	3535	
FPC_XC_62	F	000045D0	4	3578	
FPC_XC_63	F	000046A8	4	3627	
FPC_XC_64	F	00004780	4	3670	
FPC_XC_65	F	00004858	4	3713	
FPC_XC_66	F	00004930	4	3756	
FPC_XC_67	F	00004A08	4	3799	
FPC_XC_68	F	00004AE0	4	3842	
FPC_XC_69	F	00004BB8	4	3886	
FPC_XC_7	F	00001768	4	1191	
FPC_XC_70	F	00004C90	4	3929	
FPC_XC_71	F	00004D68	4	3972	
FPC_XC_72	F	00004E40	4	4015	
FPC_XC_73	F	00004F18	4	4058	
FPC_XC_74	F	00004FF0	4	4101	
FPC_XC_75	F	000050C8	4	4145	
FPC_XC_76	F	000051A0	4	4189	
FPC_XC_77	F	00005278	4	4232	
FPC_XC_78	F	00005350	4	4275	
FPC_XC_79	F	00005428	4	4318	
FPC_XC_8	F	00001840	4	1235	
FPC_XC_9	F	00001918	4	1278	
FPR0	U	00000000	1	4457	
FPR1	U	00000001	1	4458	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
FPR10	U	0000000A	1	4467													
FPR11	U	0000000B	1	4468													
FPR12	U	0000000C	1	4469													
FPR13	U	0000000D	1	4470													
FPR14	U	0000000E	1	4471													
FPR15	U	0000000F	1	4472													
FPR2	U	00000002	1	4459													
FPR3	U	00000003	1	4460													
FPR4	U	00000004	1	4461													
FPR5	U	00000005	1	4462													
FPR6	U	00000006	1	4463													
FPR7	U	00000007	1	4464													
FPR8	U	00000008	1	4465													
FPR9	U	00000009	1	4466													
IMAGE	1	00000000	21976	0													
K	U	00000400	1	647	648	649	650										
K64	U	00010000	1	649													
M3	U	00000008	1	767	388	505											
M4	U	00000009	1	768	395	512											
MB	U	00100000	1	650													
MSG	I	000006B0	4	571	221	554											
MSGCMD	C	000006FE	9	601	584	585											
MSGMSG	C	00000707	100	602	578	599	576										
MSGMVC	I	000006F8	6	599	582												
MSGOK	I	000006C6	2	580	577												
MSGRET	I	000006E6	4	595	588	591											
MSGSAVE	F	000006EC	4	598	574	595											
NEXTE6	U	000002EC	1	231	273	530											
OPNAME	C	00000010	8	772	289	292	295	298	385	432	468	502					
PAGE	U	00001000	1	648													
PRT3	C	0000117A	18	746	381	382	383	390	391	392	397	398	399	428	429	430	437
					438	439	444	445	446	464	465	466	473	474	475	480	481
					482	498	499	500	507	508	509	514	515	516			
PRTLINE	C	000010CE	13	711	721	519											
PRTLNG	U	00000048	1	721	518												
PRTM3	C	00001107	2	716	509												
PRTM4	C	00001113	2	719	516												
PRTNAME	C	000010F6	8	714	502												
PRTNUM	C	000010DB	3	712	500												
R0	U	00000000	1	4436	135	187	190	210	212	213	214	219	238	239	402	407	408
					423	424	448	459	460	484	518	526	527	553	555	571	574
					576	578	580	595									
R1	U	00000001	1	4437	220	267	268	317	318	335	336	353	354	371	372	403	449
					485	519	536	537	585	599							
R10	U	0000000A	1	4446	175	184	185										
R11	U	0000000B	1	4447	241	242	946	989	1031	1074	1117	1160	1203	1247	1290	1333	1376
					1419	1462	1506	1549	1592	1635	1678	1721	1764	1807	1851	1894	1943
					1986	2029	2072	2115	2158	2202	2245	2288	2331	2374	2417	2461	2505
					2548	2591	2634	2683	2726	2769	2812	2855	2898	2941	2985	3028	3071
					3114	3157	3200	3243	3287	3331	3374	3417	3460	3504	3547	3590	3639
					3682	3725	3768	3811	3854	3898	3941	3984	4027	4070	4113	4157	4201
					4244	4287	4330										
R12	U	0000000C	1	4448	229	232	272	529									
R13	U	0000000D	1	4449													
R14	U	0000000E	1	4450													
R15	U	0000000F	1	4451	244	282	284	302	315	320	333	338	351	356	369	374	401

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					404	405	409	450	486	520	548	558	559				
R2	U	00000002	1	4438	221	379	380	387	388	389	394	395	396	426	427	434	435
					436	441	442	443	462	463	470	471	472	477	478	479	496
					497	504	505	506	511	512	513	553	554	555	572	574	580
					581	582	584	590	595	596	941	942	984	985	1026	1027	1069
					1070	1112	1113	1155	1156	1198	1199	1242	1243	1285	1286	1328	1329
					1371	1372	1414	1415	1457	1458	1501	1502	1544	1545	1587	1588	1630
					1631	1673	1674	1716	1717	1759	1760	1802	1803	1846	1847	1889	1890
					1938	1939	1981	1982	2024	2025	2067	2068	2110	2111	2153	2154	2197
					2198	2240	2241	2283	2284	2326	2327	2369	2370	2412	2413	2456	2457
					2500	2501	2543	2544	2586	2587	2629	2630	2678	2679	2721	2722	2764
					2765	2807	2808	2850	2851	2893	2894	2936	2937	2980	2981	3023	3024
					3066	3067	3109	3110	3152	3153	3195	3196	3238	3239	3282	3283	3326
					3327	3369	3370	3412	3413	3455	3456	3499	3500	3542	3543	3585	3586
					3634	3635	3677	3678	3720	3721	3763	3764	3806	3807	3849	3850	3893
					3894	3936	3937	3979	3980	4022	4023	4065	4066	4108	4109	4152	4153
					4196	4197	4239	4240	4282	4283	4325	4326					
R3	U	00000003	1	4439													
R4	U	00000004	1	4440													
R5	U	00000005	1	4441	232	233	236	549	557	912	948	955	991	997	1033	1040	1076
					1083	1119	1126	1162	1169	1205	1213	1249	1256	1292	1299	1335	1342
					1378	1385	1421	1428	1464	1472	1508	1515	1551	1558	1594	1601	1637
					1644	1680	1687	1723	1730	1766	1773	1809	1817	1853	1860	1896	1909
					1945	1952	1988	1995	2031	2038	2074	2081	2117	2124	2160	2168	2204
					2211	2247	2254	2290	2297	2333	2340	2376	2383	2419	2427	2463	2471
					2507	2514	2550	2557	2593	2600	2636	2649	2685	2692	2728	2735	2771
					2778	2814	2821	2857	2864	2900	2907	2943	2951	2987	2994	3030	3037
					3073	3080	3116	3123	3159	3166	3202	3209	3245	3253	3289	3297	3333
					3340	3376	3383	3419	3426	3462	3470	3506	3513	3549	3556	3592	3605
					3641	3648	3684	3691	3727	3734	3770	3777	3813	3820	3856	3864	3900
					3907	3943	3950	3986	3993	4029	4036	4072	4079	4115	4123	4159	4167
					4203	4210	4246	4253	4289	4296	4332						
R6	U	00000006	1	4442													
R7	U	00000007	1	4443	250	255	451	487									
R8	U	00000008	1	4444	173	177	178	179	181								
R9	U	00000009	1	4445	174	181	182	184									
RE1	F	00001294	4	947	921	924											
RE10	F	00001A2C	4	1334	1308	1311											
RE11	F	00001B04	4	1377	1351	1354											
RE12	F	00001BDC	4	1420	1394	1397											
RE13	F	00001CB4	4	1463	1437	1440											
RE14	F	00001D8C	4	1507	1481	1484											
RE15	F	00001E64	4	1550	1524	1527											
RE16	F	00001F3C	4	1593	1567	1570											
RE17	F	00002014	4	1636	1610	1613											
RE18	F	000020EC	4	1679	1653	1656											
RE19	F	000021C4	4	1722	1696	1699											
RE2	F	0000136C	4	990	964	967											
RE20	F	0000229C	4	1765	1739	1742											
RE21	F	00002374	4	1808	1782	1785											
RE22	F	0000244C	4	1852	1826	1829											
RE23	F	00002524	4	1895	1869	1872											
RE24	F	000025FC	4	1944	1918	1921											
RE25	F	000026D4	4	1987	1961	1964											
RE26	F	000027AC	4	2030	2004	2007											
RE27	F	00002884	4	2073	2047	2050											

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
RE28	F	0000295C	4	2116	2090	2093
RE29	F	00002A34	4	2159	2133	2136
RE3	F	00001444	4	1032	1006	1009
RE30	F	00002B0C	4	2203	2177	2180
RE31	F	00002BE4	4	2246	2220	2223
RE32	F	00002CBC	4	2289	2263	2266
RE33	F	00002D94	4	2332	2306	2309
RE34	F	00002E6C	4	2375	2349	2352
RE35	F	00002F44	4	2418	2392	2395
RE36	F	0000301C	4	2462	2436	2439
RE37	F	000030F4	4	2506	2480	2483
RE38	F	000031CC	4	2549	2523	2526
RE39	F	000032A4	4	2592	2566	2569
RE4	F	0000151C	4	1075	1049	1052
RE40	F	0000337C	4	2635	2609	2612
RE41	F	00003454	4	2684	2658	2661
RE42	F	0000352C	4	2727	2701	2704
RE43	F	00003604	4	2770	2744	2747
RE44	F	000036DC	4	2813	2787	2790
RE45	F	000037B4	4	2856	2830	2833
RE46	F	0000388C	4	2899	2873	2876
RE47	F	00003964	4	2942	2916	2919
RE48	F	00003A3C	4	2986	2960	2963
RE49	F	00003B14	4	3029	3003	3006
RE5	F	000015F4	4	1118	1092	1095
RE50	F	00003BEC	4	3072	3046	3049
RE51	F	00003CC4	4	3115	3089	3092
RE52	F	00003D9C	4	3158	3132	3135
RE53	F	00003E74	4	3201	3175	3178
RE54	F	00003F4C	4	3244	3218	3221
RE55	F	00004024	4	3288	3262	3265
RE56	F	000040FC	4	3332	3306	3309
RE57	F	000041D4	4	3375	3349	3352
RE58	F	000042AC	4	3418	3392	3395
RE59	F	00004384	4	3461	3435	3438
RE6	F	000016CC	4	1161	1135	1138
RE60	F	0000445C	4	3505	3479	3482
RE61	F	00004534	4	3548	3522	3525
RE62	F	0000460C	4	3591	3565	3568
RE63	F	000046E4	4	3640	3614	3617
RE64	F	000047BC	4	3683	3657	3660
RE65	F	00004894	4	3726	3700	3703
RE66	F	0000496C	4	3769	3743	3746
RE67	F	00004A44	4	3812	3786	3789
RE68	F	00004B1C	4	3855	3829	3832
RE69	F	00004BF4	4	3899	3873	3876
RE7	F	000017A4	4	1204	1178	1181
RE70	F	00004CCC	4	3942	3916	3919
RE71	F	00004DA4	4	3985	3959	3962
RE72	F	00004E7C	4	4028	4002	4005
RE73	F	00004F54	4	4071	4045	4048
RE74	F	0000502C	4	4114	4088	4091
RE75	F	00005104	4	4158	4132	4135
RE76	F	000051DC	4	4202	4176	4179
RE77	F	000052B4	4	4245	4219	4222
RE78	F	0000538C	4	4288	4262	4265

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE79	F	00005464	4	4331	4305	4308		
RE8	F	0000187C	4	1248	1222	1225		
RE9	F	00001954	4	1291	1265	1268		
READDR	A	0000001C	4	774	267			
REG2LOW	U	000000DD	1	654				
REG2PATT	U	AABBCCDD	1	653				
RELEN	A	00000018	4	773				
RPTDWSAV	D	000006A0	8	564	553	555		
RPTERROR	I	0000067A	4	548	404	450	486	520
RPTSAVE	F	00000698	4	561	548	558		
RPTSVR5	F	0000069C	4	562	549	557		
SKIPXC	C	00000050	8	780	280	288	301	
SKL0001	U	0000005F	1	203	219			
SKT0001	C	0000022A	26	200	203	220		
SVOLDPSW	U	00000140	0	137				
T1	A	000011E0	4	913	4346			
T10	A	00001978	4	1300	4355			
T11	A	00001A50	4	1343	4356			
T12	A	00001B28	4	1386	4357			
T13	A	00001C00	4	1429	4358			
T14	A	00001CD8	4	1473	4359			
T15	A	00001DB0	4	1516	4360			
T16	A	00001E88	4	1559	4361			
T17	A	00001F60	4	1602	4362			
T18	A	00002038	4	1645	4363			
T19	A	00002110	4	1688	4364			
T2	A	000012B8	4	956	4347			
T20	A	000021E8	4	1731	4365			
T21	A	000022C0	4	1774	4366			
T22	A	00002398	4	1818	4367			
T23	A	00002470	4	1861	4368			
T24	A	00002548	4	1910	4369			
T25	A	00002620	4	1953	4370			
T26	A	000026F8	4	1996	4371			
T27	A	000027D0	4	2039	4372			
T28	A	000028A8	4	2082	4373			
T29	A	00002980	4	2125	4374			
T3	A	00001390	4	998	4348			
T30	A	00002A58	4	2169	4375			
T31	A	00002B30	4	2212	4376			
T32	A	00002C08	4	2255	4377			
T33	A	00002CE0	4	2298	4378			
T34	A	00002DB8	4	2341	4379			
T35	A	00002E90	4	2384	4380			
T36	A	00002F68	4	2428	4381			
T37	A	00003040	4	2472	4382			
T38	A	00003118	4	2515	4383			
T39	A	000031F0	4	2558	4384			
T4	A	00001468	4	1041	4349			
T40	A	000032C8	4	2601	4385			
T41	A	000033A0	4	2650	4386			
T42	A	00003478	4	2693	4387			
T43	A	00003550	4	2736	4388			
T44	A	00003628	4	2779	4389			
T45	A	00003700	4	2822	4390			
T46	A	000037D8	4	2865	4391			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES							
T47	A	000038B0	4	2908	4392							
T48	A	00003988	4	2952	4393							
T49	A	00003A60	4	2995	4394							
T5	A	00001540	4	1084	4350							
T50	A	00003B38	4	3038	4395							
T51	A	00003C10	4	3081	4396							
T52	A	00003CE8	4	3124	4397							
T53	A	00003DC0	4	3167	4398							
T54	A	00003E98	4	3210	4399							
T55	A	00003F70	4	3254	4400							
T56	A	00004048	4	3298	4401							
T57	A	00004120	4	3341	4402							
T58	A	000041F8	4	3384	4403							
T59	A	000042D0	4	3427	4404							
T6	A	00001618	4	1127	4351							
T60	A	000043A8	4	3471	4405							
T61	A	00004480	4	3514	4406							
T62	A	00004558	4	3557	4407							
T63	A	00004630	4	3606	4408							
T64	A	00004708	4	3649	4409							
T65	A	000047E0	4	3692	4410							
T66	A	000048B8	4	3735	4411							
T67	A	00004990	4	3778	4412							
T68	A	00004A68	4	3821	4413							
T69	A	00004B40	4	3865	4414							
T7	A	000016F0	4	1170	4352							
T70	A	00004C18	4	3908	4415							
T71	A	00004CF0	4	3951	4416							
T72	A	00004DC8	4	3994	4417							
T73	A	00004EA0	4	4037	4418							
T74	A	00004F78	4	4080	4419							
T75	A	00005050	4	4124	4420							
T76	A	00005128	4	4168	4421							
T77	A	00005200	4	4211	4422							
T78	A	000052D8	4	4254	4423							
T79	A	000053B0	4	4297	4424							
T8	A	000017C8	4	1214	4353							
T9	A	000018A0	4	1257	4354							
TESTING	F	00001004	4	665	239							
TNUM	H	00000004	2	764	238	379	426	462	496			
TSUB	A	00000000	4	763	241							
TTABLE	F	0000548C	4	4345								
V0	U	00000000	1	4478								
V1	U	00000001	1	4479								
V10	U	0000000A	1	4488								
V11	U	0000000B	1	4489								
V12	U	0000000C	1	4490								
V13	U	0000000D	1	4491								
V14	U	0000000E	1	4492								
V15	U	0000000F	1	4493	310	312	328	330	346	348	364	366
V16	U	00000010	1	4494	309	310	327	328	345	346	363	364
V17	U	00000011	1	4495								
V18	U	00000012	1	4496								
V19	U	00000013	1	4497								
V1FUDGE	X	000011B0	16	754								
V1INPUT	X	000011C0	16	755								

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V101	X	00001208	16	926	945
V1010	X	000019A0	16	1313	1332
V1011	X	00001A78	16	1356	1375
V1012	X	00001B50	16	1399	1418
V1013	X	00001C28	16	1442	1461
V1014	X	00001D00	16	1486	1505
V1015	X	00001DD8	16	1529	1548
V1016	X	00001EB0	16	1572	1591
V1017	X	00001F88	16	1615	1634
V1018	X	00002060	16	1658	1677
V1019	X	00002138	16	1701	1720
V102	X	000012E0	16	969	988
V1020	X	00002210	16	1744	1763
V1021	X	000022E8	16	1787	1806
V1022	X	000023C0	16	1831	1850
V1023	X	00002498	16	1874	1893
V1024	X	00002570	16	1923	1942
V1025	X	00002648	16	1966	1985
V1026	X	00002720	16	2009	2028
V1027	X	000027F8	16	2052	2071
V1028	X	000028D0	16	2095	2114
V1029	X	000029A8	16	2138	2157
V103	X	000013B8	16	1011	1030
V1030	X	00002A80	16	2182	2201
V1031	X	00002B58	16	2225	2244
V1032	X	00002C30	16	2268	2287
V1033	X	00002D08	16	2311	2330
V1034	X	00002DE0	16	2354	2373
V1035	X	00002EB8	16	2397	2416
V1036	X	00002F90	16	2441	2460
V1037	X	00003068	16	2485	2504
V1038	X	00003140	16	2528	2547
V1039	X	00003218	16	2571	2590
V104	X	00001490	16	1054	1073
V1040	X	000032F0	16	2614	2633
V1041	X	000033C8	16	2663	2682
V1042	X	000034A0	16	2706	2725
V1043	X	00003578	16	2749	2768
V1044	X	00003650	16	2792	2811
V1045	X	00003728	16	2835	2854
V1046	X	00003800	16	2878	2897
V1047	X	000038D8	16	2921	2940
V1048	X	000039B0	16	2965	2984
V1049	X	00003A88	16	3008	3027
V105	X	00001568	16	1097	1116
V1050	X	00003B60	16	3051	3070
V1051	X	00003C38	16	3094	3113
V1052	X	00003D10	16	3137	3156
V1053	X	00003DE8	16	3180	3199
V1054	X	00003EC0	16	3223	3242
V1055	X	00003F98	16	3267	3286
V1056	X	00004070	16	3311	3330
V1057	X	00004148	16	3354	3373
V1058	X	00004220	16	3397	3416
V1059	X	000042F8	16	3440	3459
V106	X	00001640	16	1140	1159

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1O60	X	000043D0	16	3484	3503												
V1O61	X	000044A8	16	3527	3546												
V1O62	X	00004580	16	3570	3589												
V1O63	X	00004658	16	3619	3638												
V1O64	X	00004730	16	3662	3681												
V1O65	X	00004808	16	3705	3724												
V1O66	X	000048E0	16	3748	3767												
V1O67	X	000049B8	16	3791	3810												
V1O68	X	00004A90	16	3834	3853												
V1O69	X	00004B68	16	3878	3897												
V1O7	X	00001718	16	1183	1202												
V1O70	X	00004C40	16	3921	3940												
V1O71	X	00004D18	16	3964	3983												
V1O72	X	00004DF0	16	4007	4026												
V1O73	X	00004EC8	16	4050	4069												
V1O74	X	00004FA0	16	4093	4112												
V1O75	X	00005078	16	4137	4156												
V1O76	X	00005150	16	4181	4200												
V1O77	X	00005228	16	4224	4243												
V1O78	X	00005300	16	4267	4286												
V1O79	X	000053D8	16	4310	4329												
V1O8	X	000017F0	16	1227	1246												
V1O9	X	000018C8	16	1270	1289												
V1OUTPUT	X	00000028	16	776	268	309	327	345	363								
V2	U	00000002	1	4480													
V20	U	00000014	1	4498													
V21	U	00000015	1	4499													
V22	U	00000016	1	4500	942	943	945	985	986	988	1027	1028	1030	1070	1071	1073	1113
					1114	1116	1156	1157	1159	1199	1200	1202	1243	1244	1246	1286	1287
					1289	1329	1330	1332	1372	1373	1375	1415	1416	1418	1458	1459	1461
					1502	1503	1505	1545	1546	1548	1588	1589	1591	1631	1632	1634	1674
					1675	1677	1717	1718	1720	1760	1761	1763	1803	1804	1806	1847	1848
					1850	1890	1891	1893	1939	1940	1942	1982	1983	1985	2025	2026	2028
					2068	2069	2071	2111	2112	2114	2154	2155	2157	2198	2199	2201	2241
					2242	2244	2284	2285	2287	2327	2328	2330	2370	2371	2373	2413	2414
					2416	2457	2458	2460	2501	2502	2504	2544	2545	2547	2587	2588	2590
					2630	2631	2633	2679	2680	2682	2722	2723	2725	2765	2766	2768	2808
					2809	2811	2851	2852	2854	2894	2895	2897	2937	2938	2940	2981	2982
					2984	3024	3025	3027	3067	3068	3070	3110	3111	3113	3153	3154	3156
					3196	3197	3199	3239	3240	3242	3283	3284	3286	3327	3328	3330	3370
					3371	3373	3413	3414	3416	3456	3457	3459	3500	3501	3503	3543	3544
					3546	3586	3587	3589	3635	3636	3638	3678	3679	3681	3721	3722	3724
					3764	3765	3767	3807	3808	3810	3850	3851	3853	3894	3895	3897	3937
					3938	3940	3980	3981	3983	4023	4024	4026	4066	4067	4069	4109	4110
					4112	4153	4154	4156	4197	4198	4200	4240	4241	4243	4283	4284	4286
					4326	4327	4329										
V23	U	00000017	1	4501													
V24	U	00000018	1	4502													
V25	U	00000019	1	4503													
V26	U	0000001A	1	4504													
V27	U	0000001B	1	4505													
V28	U	0000001C	1	4506													
V29	U	0000001D	1	4507													
V2ADDR	A	0000000C	4	771	317	335	353	371									
V2_1	A	000011EC	4	921	941												
V2_10	A	00001984	4	1308	1328												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V2_11	A	00001A5C	4	1351	1371
V2_12	A	00001B34	4	1394	1414
V2_13	A	00001C0C	4	1437	1457
V2_14	A	00001CE4	4	1481	1501
V2_15	A	00001DBC	4	1524	1544
V2_16	A	00001E94	4	1567	1587
V2_17	A	00001F6C	4	1610	1630
V2_18	A	00002044	4	1653	1673
V2_19	A	0000211C	4	1696	1716
V2_2	A	000012C4	4	964	984
V2_20	A	000021F4	4	1739	1759
V2_21	A	000022CC	4	1782	1802
V2_22	A	000023A4	4	1826	1846
V2_23	A	0000247C	4	1869	1889
V2_24	A	00002554	4	1918	1938
V2_25	A	0000262C	4	1961	1981
V2_26	A	00002704	4	2004	2024
V2_27	A	000027DC	4	2047	2067
V2_28	A	000028B4	4	2090	2110
V2_29	A	0000298C	4	2133	2153
V2_3	A	0000139C	4	1006	1026
V2_30	A	00002A64	4	2177	2197
V2_31	A	00002B3C	4	2220	2240
V2_32	A	00002C14	4	2263	2283
V2_33	A	00002CEC	4	2306	2326
V2_34	A	00002DC4	4	2349	2369
V2_35	A	00002E9C	4	2392	2412
V2_36	A	00002F74	4	2436	2456
V2_37	A	0000304C	4	2480	2500
V2_38	A	00003124	4	2523	2543
V2_39	A	000031FC	4	2566	2586
V2_4	A	00001474	4	1049	1069
V2_40	A	000032D4	4	2609	2629
V2_41	A	000033AC	4	2658	2678
V2_42	A	00003484	4	2701	2721
V2_43	A	0000355C	4	2744	2764
V2_44	A	00003634	4	2787	2807
V2_45	A	0000370C	4	2830	2850
V2_46	A	000037E4	4	2873	2893
V2_47	A	000038BC	4	2916	2936
V2_48	A	00003994	4	2960	2980
V2_49	A	00003A6C	4	3003	3023
V2_5	A	0000154C	4	1092	1112
V2_50	A	00003B44	4	3046	3066
V2_51	A	00003C1C	4	3089	3109
V2_52	A	00003CF4	4	3132	3152
V2_53	A	00003DCC	4	3175	3195
V2_54	A	00003EA4	4	3218	3238
V2_55	A	00003F7C	4	3262	3282
V2_56	A	00004054	4	3306	3326
V2_57	A	0000412C	4	3349	3369
V2_58	A	00004204	4	3392	3412
V2_59	A	000042DC	4	3435	3455
V2_6	A	00001624	4	1135	1155
V2_60	A	000043B4	4	3479	3499
V2_61	A	0000448C	4	3522	3542

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
V2_62	A	00004564	4	3565	3585	
V2_63	A	0000463C	4	3614	3634	
V2_64	A	00004714	4	3657	3677	
V2_65	A	000047EC	4	3700	3720	
V2_66	A	000048C4	4	3743	3763	
V2_67	A	0000499C	4	3786	3806	
V2_68	A	00004A74	4	3829	3849	
V2_69	A	00004B4C	4	3873	3893	
V2_7	A	000016FC	4	1178	1198	
V2_70	A	00004C24	4	3916	3936	
V2_71	A	00004CFC	4	3959	3979	
V2_72	A	00004DD4	4	4002	4022	
V2_73	A	00004EAC	4	4045	4065	
V2_74	A	00004F84	4	4088	4108	
V2_75	A	0000505C	4	4132	4152	
V2_76	A	00005134	4	4176	4196	
V2_77	A	0000520C	4	4219	4239	
V2_78	A	000052E4	4	4262	4282	
V2_79	A	000053BC	4	4305	4325	
V2_8	A	000017D4	4	1222	1242	
V2_9	A	000018AC	4	1265	1285	
V3	U	00000003	1	4481		
V30	U	0000001E	1	4508		
V31	U	0000001F	1	4509		
V4	U	00000004	1	4482		
V5	U	00000005	1	4483		
V6	U	00000006	1	4484		
V7	U	00000007	1	4485		
V8	U	00000008	1	4486		
V9	U	00000009	1	4487		
VXC	X	0000000B	1	770	253	471
VXC1	X	000011EB	1	920		
VXC10	X	00001983	1	1307		
VXC11	X	00001A5B	1	1350		
VXC12	X	00001B33	1	1393		
VXC13	X	00001C0B	1	1436		
VXC14	X	00001CE3	1	1480		
VXC15	X	00001DBB	1	1523		
VXC16	X	00001E93	1	1566		
VXC17	X	00001F6B	1	1609		
VXC18	X	00002043	1	1652		
VXC19	X	0000211B	1	1695		
VXC2	X	000012C3	1	963		
VXC20	X	000021F3	1	1738		
VXC21	X	000022CB	1	1781		
VXC22	X	000023A3	1	1825		
VXC23	X	0000247B	1	1868		
VXC24	X	00002553	1	1917		
VXC25	X	0000262B	1	1960		
VXC26	X	00002703	1	2003		
VXC27	X	000027DB	1	2046		
VXC28	X	000028B3	1	2089		
VXC29	X	0000298B	1	2132		
VXC3	X	0000139B	1	1005		
VXC30	X	00002A63	1	2176		
VXC31	X	00002B3B	1	2219		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
VXC32	X	00002C13	1	2262	
VXC33	X	00002CEB	1	2305	
VXC34	X	00002DC3	1	2348	
VXC35	X	00002E9B	1	2391	
VXC36	X	00002F73	1	2435	
VXC37	X	0000304B	1	2479	
VXC38	X	00003123	1	2522	
VXC39	X	000031FB	1	2565	
VXC4	X	00001473	1	1048	
VXC40	X	000032D3	1	2608	
VXC41	X	000033AB	1	2657	
VXC42	X	00003483	1	2700	
VXC43	X	0000355B	1	2743	
VXC44	X	00003633	1	2786	
VXC45	X	0000370B	1	2829	
VXC46	X	000037E3	1	2872	
VXC47	X	000038BB	1	2915	
VXC48	X	00003993	1	2959	
VXC49	X	00003A6B	1	3002	
VXC5	X	0000154B	1	1091	
VXC50	X	00003B43	1	3045	
VXC51	X	00003C1B	1	3088	
VXC52	X	00003CF3	1	3131	
VXC53	X	00003DCB	1	3174	
VXC54	X	00003EA3	1	3217	
VXC55	X	00003F7B	1	3261	
VXC56	X	00004053	1	3305	
VXC57	X	0000412B	1	3348	
VXC58	X	00004203	1	3391	
VXC59	X	000042DB	1	3434	
VXC6	X	00001623	1	1134	
VXC60	X	000043B3	1	3478	
VXC61	X	0000448B	1	3521	
VXC62	X	00004563	1	3564	
VXC63	X	0000463B	1	3613	
VXC64	X	00004713	1	3656	
VXC65	X	000047EB	1	3699	
VXC66	X	000048C3	1	3742	
VXC67	X	0000499B	1	3785	
VXC68	X	00004A73	1	3828	
VXC69	X	00004B4B	1	3872	
VXC7	X	000016FB	1	1177	
VXC70	X	00004C23	1	3915	
VXC71	X	00004CFB	1	3958	
VXC72	X	00004DD3	1	4001	
VXC73	X	00004EAB	1	4044	
VXC74	X	00004F83	1	4087	
VXC75	X	0000505B	1	4131	
VXC76	X	00005133	1	4175	
VXC77	X	0000520B	1	4218	
VXC78	X	000052E3	1	4261	
VXC79	X	000053BB	1	4304	
VXC8	X	000017D3	1	1221	
VXC9	X	000018AB	1	1264	
VXCMSG	U	00000582	1	458	255
VXCPEXP	C	000010B5	3	698	475

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
VXCPGOT	C	000010CA	3	701	482	
VXCPLINE	C	0000106B	13	693	703	485
VXCPLNG	U	00000063	1	703	484	
VXCPNAME	C	0000109C	8	696	468	
VXCPNUM	C	00001078	3	694	466	
WK1	F	00000088	4	786		
WK2	F	0000008C	4	787		
X0001	U	000002C0	1	209	197	210
X1	F	00001270	4	939	913	
X10	F	00001A08	4	1326	1300	
X11	F	00001AE0	4	1369	1343	
X12	F	00001BB8	4	1412	1386	
X13	F	00001C90	4	1455	1429	
X14	F	00001D68	4	1499	1473	
X15	F	00001E40	4	1542	1516	
X16	F	00001F18	4	1585	1559	
X17	F	00001FF0	4	1628	1602	
X18	F	000020C8	4	1671	1645	
X19	F	000021A0	4	1714	1688	
X2	F	00001348	4	982	956	
X20	F	00002278	4	1757	1731	
X21	F	00002350	4	1800	1774	
X22	F	00002428	4	1844	1818	
X23	F	00002500	4	1887	1861	
X24	F	000025D8	4	1936	1910	
X25	F	000026B0	4	1979	1953	
X26	F	00002788	4	2022	1996	
X27	F	00002860	4	2065	2039	
X28	F	00002938	4	2108	2082	
X29	F	00002A10	4	2151	2125	
X3	F	00001420	4	1024	998	
X30	F	00002AE8	4	2195	2169	
X31	F	00002BC0	4	2238	2212	
X32	F	00002C98	4	2281	2255	
X33	F	00002D70	4	2324	2298	
X34	F	00002E48	4	2367	2341	
X35	F	00002F20	4	2410	2384	
X36	F	00002FF8	4	2454	2428	
X37	F	000030D0	4	2498	2472	
X38	F	000031A8	4	2541	2515	
X39	F	00003280	4	2584	2558	
X4	F	000014F8	4	1067	1041	
X40	F	00003358	4	2627	2601	
X41	F	00003430	4	2676	2650	
X42	F	00003508	4	2719	2693	
X43	F	000035E0	4	2762	2736	
X44	F	000036B8	4	2805	2779	
X45	F	00003790	4	2848	2822	
X46	F	00003868	4	2891	2865	
X47	F	00003940	4	2934	2908	
X48	F	00003A18	4	2978	2952	
X49	F	00003AF0	4	3021	2995	
X5	F	000015D0	4	1110	1084	
X50	F	00003BC8	4	3064	3038	
X51	F	00003CA0	4	3107	3081	
X52	F	00003D78	4	3150	3124	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
X53	F	00003E50	4	3193	3167			
X54	F	00003F28	4	3236	3210			
X55	F	00004000	4	3280	3254			
X56	F	000040D8	4	3324	3298			
X57	F	000041B0	4	3367	3341			
X58	F	00004288	4	3410	3384			
X59	F	00004360	4	3453	3427			
X6	F	000016A8	4	1153	1127			
X60	F	00004438	4	3497	3471			
X61	F	00004510	4	3540	3514			
X62	F	000045E8	4	3583	3557			
X63	F	000046C0	4	3632	3606			
X64	F	00004798	4	3675	3649			
X65	F	00004870	4	3718	3692			
X66	F	00004948	4	3761	3735			
X67	F	00004A20	4	3804	3778			
X68	F	00004AF8	4	3847	3821			
X69	F	00004BD0	4	3891	3865			
X7	F	00001780	4	1196	1170			
X70	F	00004CA8	4	3934	3908			
X71	F	00004D80	4	3977	3951			
X72	F	00004E58	4	4020	3994			
X73	F	00004F30	4	4063	4037			
X74	F	00005008	4	4106	4080			
X75	F	000050E0	4	4150	4124			
X76	F	000051B8	4	4194	4168			
X77	F	00005290	4	4237	4211			
X78	F	00005368	4	4280	4254			
X79	F	00005440	4	4323	4297			
X8	F	00001858	4	1240	1214			
X9	F	00001930	4	1283	1257			
XC0001	U	000002E8	1	223	215			
XCFAILMSG	H	0000045C	2	378	319	337	355	373
XCHECK	U	0000033C	1	279	244			
XCO1	X	00001240	16	932				
XCO10	X	000019D8	16	1319				
XCO11	X	00001AB0	16	1362				
XCO12	X	00001B88	16	1405				
XCO13	X	00001C60	16	1448				
XCO14	X	00001D38	16	1492				
XCO15	X	00001E10	16	1535				
XCO16	X	00001EE8	16	1578				
XCO17	X	00001FC0	16	1621				
XCO18	X	00002098	16	1664				
XCO19	X	00002170	16	1707				
XCO2	X	00001318	16	975				
XCO20	X	00002248	16	1750				
XCO21	X	00002320	16	1793				
XCO22	X	000023F8	16	1837				
XCO23	X	000024D0	16	1880				
XCO24	X	000025A8	16	1929				
XCO25	X	00002680	16	1972				
XCO26	X	00002758	16	2015				
XCO27	X	00002830	16	2058				
XCO28	X	00002908	16	2101				
XCO29	X	000029E0	16	2144				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
XC03	X	000013F0	16	1017	
XC030	X	00002AB8	16	2188	
XC031	X	00002B90	16	2231	
XC032	X	00002C68	16	2274	
XC033	X	00002D40	16	2317	
XC034	X	00002E18	16	2360	
XC035	X	00002EF0	16	2403	
XC036	X	00002FC8	16	2447	
XC037	X	000030A0	16	2491	
XC038	X	00003178	16	2534	
XC039	X	00003250	16	2577	
XC04	X	000014C8	16	1060	
XC040	X	00003328	16	2620	
XC041	X	00003400	16	2669	
XC042	X	000034D8	16	2712	
XC043	X	000035B0	16	2755	
XC044	X	00003688	16	2798	
XC045	X	00003760	16	2841	
XC046	X	00003838	16	2884	
XC047	X	00003910	16	2927	
XC048	X	000039E8	16	2971	
XC049	X	00003AC0	16	3014	
XC05	X	000015A0	16	1103	
XC050	X	00003B98	16	3057	
XC051	X	00003C70	16	3100	
XC052	X	00003D48	16	3143	
XC053	X	00003E20	16	3186	
XC054	X	00003EF8	16	3229	
XC055	X	00003FD0	16	3273	
XC056	X	000040A8	16	3317	
XC057	X	00004180	16	3360	
XC058	X	00004258	16	3403	
XC059	X	00004330	16	3446	
XC06	X	00001678	16	1146	
XC060	X	00004408	16	3490	
XC061	X	000044E0	16	3533	
XC062	X	000045B8	16	3576	
XC063	X	00004690	16	3625	
XC064	X	00004768	16	3668	
XC065	X	00004840	16	3711	
XC066	X	00004918	16	3754	
XC067	X	000049F0	16	3797	
XC068	X	00004AC8	16	3840	
XC069	X	00004BA0	16	3884	
XC07	X	00001750	16	1189	
XC070	X	00004C78	16	3927	
XC071	X	00004D50	16	3970	
XC072	X	00004E28	16	4013	
XC073	X	00004F00	16	4056	
XC074	X	00004FD8	16	4099	
XC075	X	000050B0	16	4143	
XC076	X	00005188	16	4187	
XC077	X	00005260	16	4230	
XC078	X	00005338	16	4273	
XC079	X	00005410	16	4316	
XC08	X	00001828	16	1233	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES						
XCO9	X	00001900	16	1276							
XCOUTPUT	X	00000060	16	782	312	318	330	336	348	354	366	372
XCPLINE	C	00001116	13	729	738	403						
XCPLNG	U	0000004E	1	738	402							
XCPM3	C	00001156	2	734	392							
XCPM4	C	00001161	2	736	399							
XCPNAME	C	00001145	8	732	385							
XCPTNUM	C	00001123	3	730	383							
XCR15	F	00000508	8	415	401	405						
XCRESULT	X	000004D8	16	412							
XCSKIP	C	00000007	1	766	281							
XCV1	X	000004E8	16	413							
XCV2	X	000004F8	16	414							
XCVCFN	F	000003F4	4	342	296							
XCVCLFNH	F	000003C0	4	324	293							
XCVCLFNL	F	00000428	4	360	299							
XCVCNF	F	0000038C	4	306	290							
ZVE6TST	J	00000000	21976	134	137	139	143	147	663	135		
=A(E6TESTS)	A	000007F4	4	639	229							
=AL2(L'MSGMSG)	R	000007FE	2	642	576							
=CL1'S'	C	00000800	1	643	281							
=CL8' '	C	000007C8	8	633	288							
=CL8'SKIP XC '	C	000007C0	8	632	280	301						
=CL8'VCFN'	C	000007E0	8	636	295							
=CL8'VCLFNH'	C	000007D8	8	635	292							
=CL8'VCLFNL'	C	000007E8	8	637	298							
=CL8'VCNF'	C	000007D0	8	634	289							
=F'1'	F	000007F8	4	640	407	423	459	526				
=F'4'	F	000007F0	4	638	214							
=H'0'	H	000007FC	2	641	571							

```
 MACRO   DEFN  REFERENCES

FCHECK     86    196
PTTABLE   865   4344
VRR_A     803    910    953    995   1038   1081   1124   1167   1211   1254   1297   1340   1383   1426   1470   1513   1556   1599
                1642   1685   1728   1771   1815   1858   1907   1950   1993   2036   2079   2122   2166   2209   2252   2295   2338
                2381   2425   2469   2512   2555   2598   2647   2690   2733   2776   2819   2862   2905   2949   2992   3035   3078
                3121   3164   3207   3251   3295   3338   3381   3424   3468   3511   3554   3603   3646   3689   3732   3775   3818
                3862   3905   3948   3991   4034   4077   4121   4165   4208   4251   4294
```

```
   DESC     SYMBOL   SIZE     POS        ADDR

Entry: 0

Image      IMAGE    21976  0000-55D7  0000-55D7
  Region            21976  0000-55D7  0000-55D7
    CSECT  ZVE6TST  21976  0000-55D7  0000-55D7
```

```
   STMT                        FILE NAME
1     /devstor/sharedvfp/tests/zvector-e6-20-NNPconvert.asm

** NO ERRORS FOUND **
```