```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                     2 ************************************************************************
                                                     3 *
                                                     4 *   Zvector E7 instruction tests for VRR-c encoded:
                                                     5 *
                                                     6 *   E7A1 VMLH   - Vector Multiply Logical High
                                                     7 *   E7A2 VML    - Vector Multiply Low
                                                     8 *   E7A3 VMH    - Vector Multiply High
                                                     9 *   E7A4 VMLE   - Vector Multiply Logical Even
                                                    10 *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                    11 *   E7A6 VME    - Vector Multiply Even
                                                    12 *   E7A7 VMO    - Vector Multiply Odd
                                                    13 *
                                                    14 *        James Wekel March 2025
                                                    15 *                     July 2025 - Vector-enhancements facility 3 update
                                                    16 ************************************************************************


                                                    18 ************************************************************************
                                                    19 *
                                                    20 *        basic instruction tests
                                                    21 *
                                                    22 ************************************************************************
                                                    23 *  This program tests proper functioning of the z/arch E7 VRR-c vector
                                                    24 *  multiply (logical high, low, high, logical even, logical odd,
                                                    25 *  even, and odd) instructions.
                                                    26 *  Exceptions are not tested.
                                                    27 *
                                                    28 *  PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
                                                    29 *  obvious coding errors.  None of the tests are thorough.  They are
                                                    30 *  NOT designed to test all aspects of any of the instructions.
                                                    31 *
                                                    32 *************************************************************************
                                                    33 *
                                                    34 *   *Testcase zvector-e7-09-multiply
                                                    35 *   *
                                                    36 *   *   Zvector E7 instruction tests for VRR-c encoded:
                                                    37 *   *
                                                    38 *   *   E7A1 VMLH   - Vector Multiply Logical High
                                                    39 *   *   E7A2 VML    - Vector Multiply Low
                                                    40 *   *   E7A3 VMH    - Vector Multiply High
                                                    41 *   *   E7A4 VMLE   - Vector Multiply Logical Even
                                                    42 *   *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                    43 *   *   E7A6 VME    - Vector Multiply Even
                                                    44 *   *   E7A7 VMO    - Vector Multiply Odd
                                                    45 *   *
                                                    46 *   *   # ------------------------------------------------------------
                                                    47 *   *   #  This tests only the basic function of the instructions.
                                                    48 *   *   #  Exceptions are NOT tested.
                                                    49 *   *   # ------------------------------------------------------------
                                                    50 *   *
                                                    51 *   mainsize    2
                                                    52 *   numcpu      1
                                                    53 *   sysclear
                                                    54 *   archlvl     z/Arch
                                                    55 *
                                                    56 *   loadcore    "$(testpath)/zvector-e7-09-multiply.core" 0x0
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                 57 *
                                                 58 *   diag8cmd    enable    # (needed for messages to Hercules console)
                                                 59 *   runtest     2
                                                 60 *   diag8cmd    disable   # (reset back to default)
                                                 61 *
                                                 62 *   *Done
                                                 63 *
                                                 64 ************************************************************************
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   66 ************************************************************************
                                                   67 *        FCHECK Macro - Is a Facility Bit set?
                                                   68 *
                                                   69 *        If the facility bit is NOT set, an message is issued and
                                                   70 *        the test is skipped.
                                                   71 *
                                                   72 *        Fcheck uses R0, R1 and R2
                                                   73 *
                                                   74 * eg.    FCHECK 134,'vector-packed-decimal'
                                                   75 ************************************************************************
                                                   76         MACRO
                                                   77         FCHECK &BITNO,&NOTSETMSG
                                                   78 .*                        &BITNO : facility bit number to check
                                                   79 .*                        &NOTSETMSG : 'facility name'
                                                   80         LCLA  &FBBYTE           Facility bit in Byte
                                                   81         LCLA  &FBBIT            Facility bit within Byte
                                                   82
                                                   83         LCLA  &L(8)
                                                   84 &L(1)   SetA  128,64,32,16,8,4,2,1  bit positions within byte
                                                   85
                                                   86 &FBBYTE SETA  &BITNO/8
                                                   87 &FBBIT  SETA  &L((&BITNO-(&FBBYTE*8))+1)
                                                   88 .*      MNOTE 0,'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
                                                   89
                                                   90         B     X&SYSNDX
                                                   91 *                                       Fcheck data area
                                                   92 *                                       skip messgae
                                                   93 SKT&SYSNDX DC  C'    Skipping tests: '
                                                   94         DC    C&NOTSETMSG
                                                   95         DC    C' (bit &BITNO) is not installed.'
                                                   96 SKL&SYSNDX EQU *-SKT&SYSNDX
                                                   97 *                                       facility bits
                                                   98         DS    FD                       gap
                                                   99 FB&SYSNDX DS   4FD
                                                  100         DS    FD                       gap
                                                  101 *
                                                  102 X&SYSNDX EQU *
                                                  103         LA    R0,((X&SYSNDX-FB&SYSNDX)/8)-1
                                                  104         STFLE FB&SYSNDX                get facility bits
                                                  105
                                                  106         XGR   R0,R0
                                                  107         IC    R0,FB&SYSNDX+&FBBYTE     get fbit byte
                                                  108         N     R0,=F'&FBBIT'            is bit set?
                                                  109         BNZ   XC&SYSNDX
                                                  110 *
                                                  111 * facility bit not set, issue message and exit
                                                  112 *
                                                  113         LA    R0,SKL&SYSNDX            message length
                                                  114         LA    R1,SKT&SYSNDX            message address
                                                  115         BAL   R2,MSG
                                                  116
                                                  117         B     EOJ
                                                  118 XC&SYSNDX EQU *
                                                  119         MEND
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   121 ***********************************************************************
                                                   122 *        Low core PSWs
                                                   123 ***********************************************************************
                              00000000  000066BB   124 ZVE7TST  START 0
00000000                      00000000             125          USING ZVE7TST,R0            Low core addressability
                                                   126
                              00000140  00000000   127 SVOLDPSW EQU   ZVE7TST+X'140'        z/Arch Supervisor call old PSW

00000000                      00000000  000001A0   129          ORG   ZVE7TST+X'1A0'        z/Architecure RESTART PSW
000001A0  00000001 80000000                        130          DC    X'0000000180000000'
000001A8  00000000 00000200                        131          DC    AD(BEGIN)

000001B0                      000001B0  000001D0   133          ORG   ZVE7TST+X'1D0'        z/Architecure PROGRAM CHECK PSW
000001D0  00020001 80000000                        134          DC    X'0002000180000000'
000001D8  00000000 0000DEAD                        135          DC    AD(X'DEAD')

000001E0                      000001E0  00000200   137          ORG   ZVE7TST+X'200'        Start of actual test program...

                                                   139 ***********************************************************************
                                                   140 *                The actual "ZVE7TST" program itself...
                                                   141 ***********************************************************************
                                                   142 *
                                                   143 *  Architecture Mode: z/Arch
                                                   144 *  Register Usage:
                                                   145 *
                                                   146 *   R0       (work)
                                                   147 *   R1-4     (work)
                                                   148 *   R5       Testing control table - current test base
                                                   149 *   R6-R7    (work)
                                                   150 *   R8       First base register
                                                   151 *   R9       Second base register
                                                   152 *   R10      Third base register
                                                   153 *   R11      E7TEST call return
                                                   154 *   R12      E7TESTS register
                                                   155 *   R13      (work)
                                                   156 *   R14      Subroutine call
                                                   157 *   R15      Secondary Subroutine call or work
                                                   158 *
                                                   159 ************************************************************************

00000200                      00000200             161          USING  BEGIN,R8        FIRST Base Register
00000200                      00001200             162          USING  BEGIN+4096,R9   SECOND Base Register
00000200                      00002200             163          USING  BEGIN+8192,R10  THIRD Base Register

00000200  0580                                     165 BEGIN    BALR  R8,0             Initalize FIRST base register
00000202  0680                                     166          BCTR  R8,0             Initalize FIRST base register
00000204  0680                                     167          BCTR  R8,0             Initalize FIRST base register

00000206  4190 8800                   00000800     169          LA    R9,2048(,R8)     Initalize SECOND base register
0000020A  4190 9800                   00000800     170          LA    R9,2048(,R9)     Initalize SECOND base register
                                                   171
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000020E  41A0 9800                     00000800   172          LA    R10,2048(,R9)    Initalize THIRD base register
00000212  41A0 A800                     00000800   173          LA    R10,2048(,R10)   Initalize THIRD base register
                                                   174
00000216  B600 833C                     0000053C   175          STCTL R0,R0,CTLR0      Store CR0 to enable AFP
0000021A  9604 833D                     0000053D   176          OI    CTLR0+1,X'04'    Turn on AFP bit
0000021E  9602 833D                     0000053D   177          OI    CTLR0+1,X'02'    Turn on Vector bit
00000222  B700 833C                     0000053C   178          LCTL  R0,R0,CTLR0      Reload updated CR0
                                                   179
                                                   180 ************************************************************************
                                                   181 * Is z/Architecture vector facility installed  (bit 129)
                                                   182 ************************************************************************
                                                   183
                                                   184          FCHECK 129,'z/Architecture vector facility'
00000226  47F0 80A8                     000002A8   185+         B     X0001
                                                   186+*                                     Fcheck data area
                                                   187+*                                     skip messgae
0000022A  40404040 E2928997                        188+SKT0001  DC    C'    Skipping tests: '
0000023E  A961C199 838889A3                        189+         DC    C'z/Architecture vector facility'
0000025C  404D8289 A340F1F2                        190+         DC    C' (bit 129) is not installed.'
                             0000004E  00000001    191+SKL0001  EQU   *-SKT0001
                                                   192+*                                     facility bits
00000278  00000000 00000000                        193+         DS    FD                   gap
00000280  00000000 00000000                        194+FB0001   DS    4FD
000002A0  00000000 00000000                        195+         DS    FD                   gap
                                                   196+*
                             000002A8  00000001    197+X0001    EQU   *
000002A8  4100 0004                     00000004   198+         LA    R0,((X0001-FB0001)/8)-1
000002AC  B2B0 8080                     00000280   199+         STFLE FB0001               get facility bits
000002B0  B982 0000                                200+         XGR   R0,R0
000002B4  4300 8090                     00000290   201+         IC    R0,FB0001+16         get fbit byte
000002B8  5400 8344                     00000544   202+         N     R0,=F'64'            is bit set?
000002BC  4770 80D0                     000002D0   203+         BNZ   XC0001
                                                   204+*
                                                   205+* facility bit not set, issue message and exit
                                                   206+*
000002C0  4100 004E                     0000004E   207+         LA    R0,SKL0001           message length
000002C4  4110 802A                     0000022A   208+         LA    R1,SKT0001           message address
000002C8  4520 8258                     00000458   209+         BAL   R2,MSG
000002CC  47F0 8320                     00000520   210+         B     EOJ
                             000002D0  00000001    211+XC0001   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   213 ************************************************************************
                                                   214 * Is z/Architecture vector facility installed  (bit 198)
                                                   215 ************************************************************************
                                                   216
                                                   217          FCHECK 198,'Vector-enhancements facility 3'
000002D0  47F0 8158                    00000358    218+         B     X0002
                                                   219+*                                     Fcheck data area
                                                   220+*                                     skip messgae
000002D4  40404040 E2928997                        221+SKT0002  DC    C'    Skipping tests: '
000002E8  E58583A3 96996085                        222+         DC    C'Vector-enhancements facility 3'
00000306  404D8289 A340F1F9                        223+         DC    C' (bit 198) is not installed.'
                             0000004E  00000001    224+SKL0002  EQU   *-SKT0002
                                                   225+*                                     facility bits
00000328  00000000 00000000                        226+         DS    FD                    gap
00000330  00000000 00000000                        227+FB0002   DS    4FD
00000350  00000000 00000000                        228+         DS    FD                    gap
                                                   229+*
                             00000358  00000001    230+X0002    EQU   *
00000358  4100 0004                    00000004    231+         LA    R0,((X0002-FB0002)/8)-1
0000035C  B2B0 8130                    00000330    232+         STFLE FB0002                get facility bits
00000360  B982 0000                                233+         XGR   R0,R0
00000364  4300 8148                    00000348    234+         IC    R0,FB0002+24          get fbit byte
00000368  5400 8348                    00000548    235+         N     R0,=F'2'              is bit set?
0000036C  4770 8180                    00000380    236+         BNZ   XC0002
                                                   237+*
                                                   238+* facility bit not set, issue message and exit
                                                   239+*
00000370  4100 004E                    0000004E    240+         LA    R0,SKL0002            message length
00000374  4110 80D4                    000002D4    241+         LA    R1,SKT0002            message address
00000378  4520 8258                    00000458    242+         BAL   R2,MSG
0000037C  47F0 8320                    00000520    243+         B     EOJ
                             00000380  00000001    244+XC0002   EQU   *
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                            246 ***********************************************************************
                                            247 *               Do tests in the E7TESTS table
                                            248 ***********************************************************************
                                            249
00000380  58C0 834C                   0000054C  250          L     R12,=A(E7TESTS)       get table of test addresses
                                            251
                              00000384  00000001  252 NEXTE7   EQU   *
00000384  5850 C000                   00000000  253          L     R5,0(0,R12)       get test address
00000388  1255                                  254          LTR   R5,R5                  have a test?
0000038A  4780 81CE                   000003CE  255          BZ    ENDTEST                   done?
                                            256
0000038E                      00000000          257          USING E7TEST,R5
                                            258
0000038E  4800 5004                   00000004  259          LH    R0,TNUM           save current test number
00000392  5000 8E04                   00001004  260          ST    R0,TESTING        for easy reference
                                            261
00000396  E710 8E94 0006              00001094  262          VL    V1,V1FUDGE
0000039C  58B0 5000                   00000000  263          L     R11,TSUB          get address of test routine
000003A0  05BB                                  264          BALR  R11,R11           do test
                                            265
000003A2  E310 501C 0014              0000001C  266          LGF   R1,READDR         get address of expected result
000003A8  D50F 5028 1000      00000028  00000000  267          CLC   V1OUTPUT,0(R1)    valid?
000003AE  4770 81BA                   000003BA  268          BNE   FAILMSG                no, issue failed message
                                            269
000003B2  41C0 C004                   00000004  270          LA    R12,4(0,R12)      next test address
000003B6  47F0 8184                   00000384  271          B     NEXTE7
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                              273 ***********************************************************************
                                              274 * result not as expected:
                                              275 *        issue message with test number, instruction under test
                                              276 *              and instruction m4
                                              277 ***********************************************************************
                            000003BA  00000001  278 FAILMSG  EQU   *
000003BA  45F0 81DC                   000003DC  279          BAL   R15,RPTERROR


                                              281 ***********************************************************************
                                              282 * continue after a failed test
                                              283 ***********************************************************************
                            000003BE  00000001  284 FAILCONT EQU   *
000003BE  5800 8350                   00000550  285          L     R0,=F'1'          set failed test indicator
000003C2  5000 8E00                   00001000  286          ST    R0,FAILED
                                              287
000003C6  41C0 C004                   00000004  288          LA    R12,4(0,R12)      next test address
000003CA  47F0 8184                   00000384  289          B     NEXTE7


                                              291 ***********************************************************************
                                              292 * end of testing; set ending psw
                                              293 ***********************************************************************
                            000003CE  00000001  294 ENDTEST  EQU   *
000003CE  5810 8E00                   00001000  295          L     R1,FAILED         did a test fail?
000003D2  1211                                  296          LTR   R1,R1
000003D4  4780 8320                   00000520  297          BZ    EOJ               No, exit
000003D8  47F0 8338                   00000538  298          B     FAILTEST          Yes, exit with BAD PSW
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   300 ************************************************************************
                                                   301 *        RPTERROR                  Report instruction test in error
                                                   302 ************************************************************************

000003DC  50F0 8240                      00000440   304 RPTERROR ST    R15,RPTSAVE          Save return address
000003E0  5050 8244                      00000444   305          ST    R5,RPTSVR5           Save R5
                                                    306 *
000003E4  4820 5004                      00000004   307          LH    R2,TNUM              get test number and convert
000003E8  4E20 8E73                      00001073   308          CVD   R2,DECNUM
000003EC  D211 8E5D 8E47      0000105D   00001047   309          MVC   PRT3,EDIT
000003F2  DE11 8E5D 8E73      0000105D   00001073   310          ED    PRT3,DECNUM
000003F8  D202 8E18 8E6A      00001018   0000106A   311          MVC   PRTNUM(3),PRT3+13    fill in message with test #
                                                    312
000003FE  D207 8E33 5008      00001033   00000008   313          MVC   PRTNAME,OPNAME       fill in message with instruction
                                                    314 *
00000404  E320 5007 0076                 00000007   315          LB    R2,m4                get m4 and convert
0000040A  4E20 8E73                      00001073   316          CVD   R2,DECNUM
0000040E  D211 8E5D 8E47      0000105D   00001047   317          MVC   PRT3,EDIT
00000414  DE11 8E5D 8E73      0000105D   00001073   318          ED    PRT3,DECNUM
0000041A  D201 8E44 8E6B      00001044   0000106B   319          MVC   PRTM4(2),PRT3+14     fill in message with m4 field

                                                    321 *
                                                    322 *        Use Hercules Diagnose for Message to console
                                                    323 *
00000420  9002 8248                      00000448   324          STM   R0,R2,RPTDWSAV       save regs used by MSG
00000424  4100 003F                      0000003F   325          LA    R0,PRTLNG            message length
00000428  4110 8E08                      00001008   326          LA    R1,PRTLINE           messagfe address
0000042C  4520 8258                      00000458   327          BAL   R2,MSG               call Hercules console MSG display
00000430  9802 8248                      00000448   328          LM    R0,R2,RPTDWSAV       restore regs


00000434  5850 8244                      00000444   330          L     R5,RPTSVR5         Restore R5
00000438  58F0 8240                      00000440   331          L     R15,RPTSAVE        Restore return address
0000043C  07FF                                      332          BR    R15                Return to caller

00000440  00000000                                  334 RPTSAVE  DC    F'0'               R15 save area
00000444  00000000                                  335 RPTSVR5  DC    F'0'               R5 save area

00000448  00000000 00000000                         337 RPTDWSAV DC    2D'0'              R0-R2 save area for MSG call
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    339 ************************************************************************
                                                    340 *        Issue HERCULES MESSAGE pointed to by R1, length in R0
                                                    341 *              R2 = return address
                                                    342 ************************************************************************

00000458  4900 8354                       00000554  344 MSG      CH    R0,=H'0'                Do we even HAVE a message?
0000045C  07D2                                      345          BNHR  R2                      No, ignore

0000045E  9002 8294                       00000494  347          STM   R0,R2,MSGSAVE           Save registers

00000462  4900 8356                       00000556  349          CH    R0,=AL2(L'MSGMSG)       Message length within limits?
00000466  47D0 826E                       0000046E  350          BNH   MSGOK                   Yes, continue
0000046A  4100 005F                       0000005F  351          LA    R0,L'MSGMSG             No, set to maximum

0000046E  1820                                      353 MSGOK    LR    R2,R0                   Copy length to work register
00000470  0620                                      354          BCTR  R2,0                    Minus-1 for execute
00000472  4420 82A0                       000004A0  355          EX    R2,MSGMVC               Copy message to O/P buffer

00000476  4120 200A                       0000000A  357          LA    R2,1+L'MSGCMD(,R2)      Calculate true command length
0000047A  4110 82A6                       000004A6  358          LA    R1,MSGCMD               Point to true command

0000047E  83120008                                  360          DC    X'83',X'12',X'0008'     Issue Hercules Diagnose X'008'
00000482  4780 828E                       0000048E  361          BZ    MSGRET                  Return if successful
                                                    362
00000486  1222                                      363          LTR   R2,R2                   Is Diag8 Ry (R2) 0?
00000488  4780 828E                       0000048E  364          BZ    MSGRET                    an error occurred but coninue
                                                    365
0000048C  0000                                      366          DC    H'0'                    CRASH for debugging purposes

0000048E  9802 8294                       00000494  368 MSGRET   LM    R0,R2,MSGSAVE           Restore registers
00000492  07F2                                      369          BR    R2                      Return to caller


00000494  00000000 00000000                         371 MSGSAVE  DC    3F'0'                   Registers save area
000004A0  D200 82AF 1000      000004AF  00000000    372 MSGMVC   MVC   MSGMSG(0),0(R1)          Executed instruction

000004A6  D4E2C7D5 D6C8405C                         374 MSGCMD   DC    C'MSGNOH * '            *** HERCULES MESSAGE COMMAND ***
000004AF  40404040 40404040                         375 MSGMSG   DC    CL95' '                 The message text to be displayed
                                                    376
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    378 ************************************************************************
                                                    379 *        Normal completion or Abnormal termination PSWs
                                                    380 ************************************************************************


00000510  00020001 80000000                         382 EOJPSW   DC    0D'0',X'0002000180000000',AD(0)

00000520  B2B2 8310                       00000510  384 EOJ      LPSWE EOJPSW               Normal completion


00000528  00020001 80000000                         386 FAILPSW  DC    0D'0',X'0002000180000000',AD(X'BAD')

00000538  B2B2 8328                       00000528  388 FAILTEST LPSWE FAILPSW              Abnormal termination


                                                    390 ************************************************************************
                                                    391 *        Working Storage
                                                    392 ************************************************************************


0000053C  00000000                                  394 CTLR0    DS    F                 CR0
00000540  00000000                                  395          DS    F

00000544                                            397          LTORG ,                 Literals pool
00000544  00000040                                  398                =F'64'
00000548  00000002                                  399                =F'2'
0000054C  00006478                                  400                =A(E7TESTS)
00000550  00000001                                  401                =F'1'
00000554  0000                                      402                =H'0'
00000556  005F                                      403                =AL2(L'MSGMSG)
                                                    404
                                                    405 *        some constants
                                                    406
                                00000400  00000001  407 K        EQU   1024              One KB
                                00001000  00000001  408 PAGE     EQU   (4*K)             Size of one page
                                00010000  00000001  409 K64      EQU   (64*K)            64 KB
                                00100000  00000001  410 MB       EQU   (K*K)              1 MB
                                                    411
                                AABBCCDD  00000001  412 REG2PATT EQU   X'AABBCCDD'    Polluted Register pattern
                                000000DD  00000001  413 REG2LOW  EQU         X'DD'    (last byte above)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    415 *=====================================================================
                                                    416 *
                                                    417 *  NOTE: start data on an address that is easy to display
                                                    418 *        within Hercules
                                                    419 *
                                                    420 *=====================================================================
                                                    421
00000558                      00000558  00001000    422          ORG   ZVE7TST+X'1000'
00001000  00000000                                  423 FAILED   DC    F'0'                      some test failed?
00001004  00000000                                  424 TESTING  DC    F'0'                      current test number


                                                    426 *
                                                    427 *        failed message and associated editting
                                                    428 *
00001008  40404040 40404040                         429 PRTLINE  DC    C'         Test # '
00001018  A7A7A7                                    430 PRTNUM   DC    C'xxx'
0000101B  40868189 93858440                         431          DC    c' failed for instruction '
00001033  A7A7A7A7 A7A7A7A7                         432 PRTNAME  DC    CL8'xxxxxxxx'
0000103B  40A689A3 884094F4                         433          DC    C' with m4='
00001044  A7A7                                      434 PRTm4    DC    C'xx'
00001046  4B                                        435          DC    C'.'
                              0000003F  00000001    436 PRTLNG   EQU   *-PRTLINE
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    438 ************************************************************************
                                                    439 *        TEST failed : message working storge
                                                    440 ************************************************************************
00001047  40212020 20202020                         441 EDIT     DC    XL18'402120202020202020202020202020202020'
                                                    442
00001059  7E7E7E6E                                  443          DC    C'===>'
0000105D  40404040 40404040                         444 PRT3     DC    CL18' '
0000106F  4C7E7E7E                                  445          DC    C'<===='
00001073  00000000 00000000                         446 DECNUM   DS    CL16


                                                    448 ************************************************************************
                                                    449 *        Vector instruction results, pollution and input
                                                    450 ************************************************************************
00001084                                            451          DS    0F
00001084  00000000 00000000                         452          DS    XL16                                        gap
00001094  FFFFFFFF FFFFFFFF                         453 V1FUDGE  DC    XL16'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'    V1 FUDGE
000010A4  00000000 00000000                         454          DS    XL16
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    456 ************************************************************************
                                                    457 *        E7TEST DSECT
                                                    458 ************************************************************************


                                                    460 E7TEST   DSECT ,
00000000  00000000                                  461 TSUB     DC    A(0)           pointer  to test
00000004  0000                                      462 TNUM     DC    H'00'          Test Number
00000006  00                                        463          DC    X'00'
00000007  00                                        464 M4       DC    HL1'00'        m4 used
                                                    465
00000008  40404040 40404040                         466 OPNAME   DC    CL8' '         E7 name
00000010  00000000                                  467 V2ADDR   DC    A(0)           address of v2 source
00000014  00000000                                  468 V3ADDR   DC    A(0)           address of v3 source
00000018  00000000                                  469 RELEN    DC    A(0)           RESULT LENGTH
0000001C  00000000                                  470 READDR   DC    A(0)           result (expected) address
00000020  00000000 00000000                         471          DS    FD                gap
00000028  00000000 00000000                         472 V1OUTPUT DS    XL16           V1 Output
00000038  00000000 00000000                         473          DS    FD                gap
                                                    474
                                                    475 *        test routine will be here (from VRR-c macro)
                                                    476 *
                                                    477 *        followed by
                                                    478 *              EXPECTED RESULT


                          00000000  000066BB       480 ZVE7TST  CSECT ,
000010B4                                            481          DS    0F


                                                    483 ************************************************************************
                                                    484 *     Macros to help build test tables
                                                    485 ************************************************************************


                                                    487 *
                                                    488 * macro to generate individual test
                                                    489 *
                                                    490          MACRO
                                                    491          VRR_C &INST,&M4
                                                    492 .*                              &INST   - VRR-c instruction under test
                                                    493 .*                              &m4     - m4 field
                                                    494
                                                    495          GBLA  &TNUM
                                                    496 &TNUM    SETA  &TNUM+1
                                                    497
                                                    498          DS    0FD
                                                    499          USING *,R5             base for test data and test routine
                                                    500
                                                    501 T&TNUM   DC    A(X&TNUM)        address of test routine
                                                    502          DC    H'&TNUM'         test number
                                                    503          DC    X'00'
                                                    504          DC    HL1'&M4'         m4
                                                    505          DC    CL8'&INST'       instruction name
                                                    506          DC    A(RE&TNUM+16)    address of v2 source
```

```
 LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   507          DC    A(RE&TNUM+32)     address of v3 source
                                                   508          DC    A(16)             result length
                                                   509 REA&TNUM DC    A(RE&TNUM)        result address
                                                   510          DS    FD                gap
                                                   511 V1O&TNUM DS    XL16              V1 output
                                                   512          DS    FD                gap
                                                   513 .*
                                                   514 *
                                                   515 X&TNUM   DS    0F
                                                   516          LGF   R1,V2ADDR         load v2 source
                                                   517          VL    v22,0(R1)         use v22 to test decoder
                                                   518
                                                   519          LGF   R1,V3ADDR         load v3 source
                                                   520          VL    v23,0(R1)         use v23 to test decoder
                                                   521
                                                   522          &INST V22,V22,V23,&M4    test instruction (dest is a source)
                                                   523          VST   V22,V1O&TNUM       save v1 output
                                                   524
                                                   525          BR    R11               return
                                                   526
                                                   527 RE&TNUM  DC    0F                xl16 expected result
                                                   528
                                                   529          DROP  R5
                                                   530          MEND


                                                   532 *
                                                   533 * macro to generate table of pointers to individual tests
                                                   534 *
                                                   535          MACRO
                                                   536          PTTABLE
                                                   537          GBLA  &TNUM
                                                   538          LCLA  &CUR
                                                   539 &CUR     SETA  1
                                                   540 .*
                                                   541 TTABLE   DS    0F
                                                   542 .LOOP    ANOP
                                                   543 .*
                                                   544          DC    A(T&CUR)
                                                   545 .*
                                                   546 &CUR     SETA  &CUR+1
                                                   547          AIF   (&CUR LE &TNUM).LOOP
                                                   548 *
                                                   549          DC    A(0)              END OF TABLE
                                                   550          DC    A(0)
                                                   551 .*
                                                   552          MEND
                                                   553
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                    555 ************************************************************************
                                                    556 *        E7 VRR-c tests
                                                    557 ************************************************************************
                                                    558         PRINT DATA
                                                    559
                                                    560 *   E7A1 VMLH   - Vector Multiply Logical High
                                                    561 *   E7A2 VML    - Vector Multiply Low
                                                    562 *   E7A3 VMH    - Vector Multiply High
                                                    563 *   E7A4 VMLE   - Vector Multiply Logical Even
                                                    564 *   E7A5 VMLO   - Vector Multiply Logical Odd
                                                    565 *   E7A6 VME    - Vector Multiply Even
                                                    566 *   E7A7 VMO    - Vector Multiply Odd
                                                    567
                                                    568 *        VRR-c instruction, m4
                                                    569 *              followed by
                                                    570 *                 16 byte expected result (V1)
                                                    571 *                 16 byte V2 source
                                                    572 *                 16 byte V3 source
                                                    573 *-----------------------------------------------------------------
                                                    574 *  VMLH   - Vector Multiply Logical High
                                                    575 *-----------------------------------------------------------------
                                                    576 * Byte
                                                    577         VRR_C VMLH,0
000010B8                                            578+        DS    0FD
000010B8                       000010B8             579+        USING *,R5              base for test data and test routine
000010B8  000010F8                                  580+T1      DC    A(X1)             address of test routine
000010BC  0001                                      581+        DC    H'1'              test number
000010BE  00                                        582+        DC    X'00'
000010BF  00                                        583+        DC    HL1'0'            m4
000010C0  E5D4D3C8 40404040                         584+        DC    CL8'VMLH'         instruction name
000010C8  00001130                                  585+        DC    A(RE1+16)         address of v2 source
000010CC  00001140                                  586+        DC    A(RE1+32)         address of v3 source
000010D0  00000010                                  587+        DC    A(16)             result length
000010D4  00001120                                  588+REA1    DC    A(RE1)            result address
000010D8  00000000 00000000                         589+        DS    FD                gap
000010E0  00000000 00000000                         590+V1O1    DS    XL16              V1 output
000010E8  00000000 00000000
000010F0  00000000 00000000                         591+        DS    FD                gap
                                                    592+*
000010F8                                            593+X1      DS    0F
000010F8  E310 5010 0014                00000010    594+        LGF   R1,V2ADDR         load v2 source
000010FE  E761 0000 0806                00000000    595+        VL    v22,0(R1)         use v22 to test decoder
00001104  E310 5014 0014                00000014    596+        LGF   R1,V3ADDR         load v3 source
0000110A  E771 0000 0806                00000000    597+        VL    v23,0(R1)         use v23 to test decoder
00001110  E766 7000 0EA1                            598+        VMLH  V22,V22,V23,0      test instruction (dest is a source)
00001116  E760 5028 080E                000010E0    599+        VST   V22,V1O1           save v1 output
0000111C  07FB                                      600+        BR    R11               return
00001120                                            601+RE1     DC    0F                xl16 expected result
00001120                                            602+        DROP  R5
00001120  FE000000 00000002                         603         DC    XL16'FE00000000000002 0000000C000000F4'   result
00001128  0000000C 000000F4
00001130  FF000000 00000019                         604         DC    XL16'FF00000000000019 00000038000000FA'   v2
00001138  00000038 000000FA
00001140  FF000000 00000019                         605         DC    XL16'FF00000000000019 00000038000000FA'   v3
00001148  00000038 000000FA
                                                    606
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

                                                   607          VRR_C VMLH,0
00001150                                           608+         DS    0FD
00001150                     00001150              609+         USING *,R5              base for test data and test routine
00001150  00001190                                 610+T2       DC    A(X2)             address of test routine
00001154  0002                                     611+         DC    H'2'              test number
00001156  00                                       612+         DC    X'00'
00001157  00                                       613+         DC    HL1'0'            m4
00001158  E5D4D3C8 40404040                        614+         DC    CL8'VMLH'         instruction name
00001160  000011C8                                 615+         DC    A(RE2+16)         address of v2 source
00001164  000011D8                                 616+         DC    A(RE2+32)         address of v3 source
00001168  00000010                                 617+         DC    A(16)             result length
0000116C  000011B8                                 618+REA2     DC    A(RE2)            result address
00001170  00000000 00000000                        619+         DS    FD                gap
00001178  00000000 00000000                        620+V1O2     DS    XL16              V1 output
00001180  00000000 00000000
00001188  00000000 00000000                        621+         DS    FD                gap
                                                   622+*
00001190                                           623+X2       DS    0F
00001190  E310 5010 0014                00000010   624+         LGF   R1,V2ADDR         load v2 source
00001196  E761 0000 0806                00000000   625+         VL    v22,0(R1)         use v22 to test decoder
0000119C  E310 5014 0014                00000014   626+         LGF   R1,V3ADDR         load v3 source
000011A2  E771 0000 0806                00000000   627+         VL    v23,0(R1)         use v23 to test decoder
000011A8  E766 7000 0EA1                           628+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
000011AE  E760 5028 080E                00001178   629+         VST   V22,V1O2           save v1 output
000011B4  07FB                                     630+         BR    R11               return
000011B8                                           631+RE2      DC    0F                xl16 expected result
000011B8                                           632+         DROP  R5
000011B8  FE000000 00000019                        633          DC    XL16'FE00000000000019 00000038000000FA'   result
000011C0  00000038 000000FA
000011C8  FF020304 05060750                        634          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000011D0  090A0B78 0C0D0EFD
000011D8  FF020304 05060750                        635          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000011E0  090A0B78 0D0E0FFD
                                                   636
                                                   637          VRR_C VMLH,0
000011E8                                           638+         DS    0FD
000011E8                     000011E8              639+         USING *,R5              base for test data and test routine
000011E8  00001228                                 640+T3       DC    A(X3)             address of test routine
000011EC  0003                                     641+         DC    H'3'              test number
000011EE  00                                       642+         DC    X'00'
000011EF  00                                       643+         DC    HL1'0'            m4
000011F0  E5D4D3C8 40404040                        644+         DC    CL8'VMLH'         instruction name
000011F8  00001260                                 645+         DC    A(RE3+16)         address of v2 source
000011FC  00001270                                 646+         DC    A(RE3+32)         address of v3 source
00001200  00000010                                 647+         DC    A(16)             result length
00001204  00001250                                 648+REA3     DC    A(RE3)            result address
00001208  00000000 00000000                        649+         DS    FD                gap
00001210  00000000 00000000                        650+V1O3     DS    XL16              V1 output
00001218  00000000 00000000
00001220  00000000 00000000                        651+         DS    FD                gap
                                                   652+*
00001228                                           653+X3       DS    0F
00001228  E310 5010 0014                00000010   654+         LGF   R1,V2ADDR         load v2 source
0000122E  E761 0000 0806                00000000   655+         VL    v22,0(R1)         use v22 to test decoder
00001234  E310 5014 0014                00000014   656+         LGF   R1,V3ADDR         load v3 source
0000123A  E771 0000 0806                00000000   657+         VL    v23,0(R1)         use v23 to test decoder
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001240  E766 7000 0EA1                          658+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
00001246  E760 9010 080E                00001210  659+         VST   V22,V1O3           save v1 output
0000124C  07FB                                    660+         BR    R11                return
00001250                                          661+RE3      DC    0F                 xl16 expected result
00001250                                          662+         DROP  R5
00001250  FE000000 0000000C                       663          DC    XL16'FE0000000000000C 0000001C000000FB'   result
00001258  0000001C 000000FB
00001260  FF020304 05060750                       664          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00001268  090A0B78 0C0D0EFD
00001270  FF010102 02030328                       665          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00001278  0405053C 060707FE
                                                  666
                                                  667          VRR_C VMLH,0
00001280                                          668+         DS    0FD
00001280                      00001280            669+         USING *,R5               base for test data and test routine
00001280  000012C0                                670+T4       DC    A(X4)              address of test routine
00001284  0004                                    671+         DC    H'4'               test number
00001286  00                                      672+         DC    X'00'
00001287  00                                      673+         DC    HL1'0'             m4
00001288  E5D4D3C8 40404040                       674+         DC    CL8'VMLH'          instruction name
00001290  000012F8                                675+         DC    A(RE4+16)          address of v2 source
00001294  00001308                                676+         DC    A(RE4+32)          address of v3 source
00001298  00000010                                677+         DC    A(16)              result length
0000129C  000012E8                                678+REA4     DC    A(RE4)             result address
000012A0  00000000 00000000                       679+         DS    FD                 gap
000012A8  00000000 00000000                       680+V1O4     DS    XL16               V1 output
000012B0  00000000 00000000
000012B8  00000000 00000000                       681+         DS    FD                 gap
                                                  682+*
000012C0                                          683+X4       DS    0F
000012C0  E310 5010 0014                00000010  684+         LGF   R1,V2ADDR          load v2 source
000012C6  E761 0000 0806                00000000  685+         VL    v22,0(R1)          use v22 to test decoder
000012CC  E310 5014 0014                00000014  686+         LGF   R1,V3ADDR          load v3 source
000012D2  E771 0000 0806                00000000  687+         VL    v23,0(R1)          use v23 to test decoder
000012D8  E766 7000 0EA1                          688+         VMLH  V22,V22,V23,0      test instruction (dest is a source)
000012DE  E760 5028 080E                000012A8  689+         VST   V22,V1O4           save v1 output
000012E4  07FB                                    690+         BR    R11                return
000012E8                                          691+RE4      DC    0F                 xl16 expected result
000012E8                                          692+         DROP  R5
000012E8  FE000000 00000003                       693          DC    XL16'FE00000000000003 00000007000000FC'   result
000012F0  00000007 000000FC
000012F8  FF020304 05060750                       694          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00001300  090A0B78 0C0D0EFD
00001308  FF000000 0000000A                       695          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00001310  0101010F 010101FF
                                                  696
                                                  697
                                                  698 * Halfword
                                                  699          VRR_C VMLH,1
00001318                                          700+         DS    0FD
00001318                      00001318            701+         USING *,R5               base for test data and test routine
00001318  00001358                                702+T5       DC    A(X5)              address of test routine
0000131C  0005                                    703+         DC    H'5'               test number
0000131E  00                                      704+         DC    X'00'
0000131F  01                                      705+         DC    HL1'1'             m4
00001320  E5D4D3C8 40404040                       706+         DC    CL8'VMLH'          instruction name
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001328  00001390                                 707+         DC    A(RE5+16)         address of v2 source
0000132C  000013A0                                 708+         DC    A(RE5+32)         address of v3 source
00001330  00000010                                 709+         DC    A(16)             result length
00001334  00001380                                 710+REA5     DC    A(RE5)            result address
00001338  00000000 00000000                        711+         DS    FD                gap
00001340  00000000 00000000                        712+V1O5     DS    XL16              V1 output
00001348  00000000 00000000
00001350  00000000 00000000                        713+         DS    FD                gap
                                                   714+*
00001358                                           715+X5       DS    0F
00001358  E310 5010 0014                 00000010  716+         LGF   R1,V2ADDR         load v2 source
0000135E  E761 0000 0806                 00000000  717+         VL    v22,0(R1)         use v22 to test decoder
00001364  E310 5014 0014                 00000014  718+         LGF   R1,V3ADDR         load v3 source
0000136A  E771 0000 0806                 00000000  719+         VL    v23,0(R1)         use v23 to test decoder
00001370  E766 7000 1EA1                           720+         VMLH  V22,V22,V23,1      test instruction (dest is a source)
00001376  E760 5028 080E                 00001340  721+         VST   V22,V1O5           save v1 output
0000137C  07FB                                     722+         BR    R11               return
00001380                                           723+RE5      DC    0F                xl16 expected result
00001380                                           724+         DROP  R5
00001380  FFFE0000 00000000                        725          DC    XL16'FFFE000000000000 000000000000DF15'   result
00001388  00000000 0000DF15
00001390  FFFF0000 00000019                        726          DC    XL16'FFFF000000000019 000000380000EEFA'   v2
00001398  00000038 0000EEFA
000013A0  FFFF0000 00000019                        727          DC    XL16'FFFF000000000019 000000380000EEFA'   v3
000013A8  00000038 0000EEFA
                                                   728
                                                   729          VRR_C VMLH,1
000013B0                                           730+         DS    0FD
000013B0                         000013B0          731+         USING *,R5              base for test data and test routine
000013B0  000013F0                                 732+T6       DC    A(X6)             address of test routine
000013B4  0006                                     733+         DC    H'6'              test number
000013B6  00                                       734+         DC    X'00'
000013B7  01                                       735+         DC    HL1'1'            m4
000013B8  E5D4D3C8 40404040                        736+         DC    CL8'VMLH'         instruction name
000013C0  00001428                                 737+         DC    A(RE6+16)         address of v2 source
000013C4  00001438                                 738+         DC    A(RE6+32)         address of v3 source
000013C8  00000010                                 739+         DC    A(16)             result length
000013CC  00001418                                 740+REA6     DC    A(RE6)            result address
000013D0  00000000 00000000                        741+         DS    FD                gap
000013D8  00000000 00000000                        742+V1O6     DS    XL16              V1 output
000013E0  00000000 00000000
000013E8  00000000 00000000                        743+         DS    FD                gap
                                                   744+*
000013F0                                           745+X6       DS    0F
000013F0  E310 5010 0014                 00000010  746+         LGF   R1,V2ADDR         load v2 source
000013F6  E761 0000 0806                 00000000  747+         VL    v22,0(R1)         use v22 to test decoder
000013FC  E310 5014 0014                 00000014  748+         LGF   R1,V3ADDR         load v3 source
00001402  E771 0000 0806                 00000000  749+         VL    v23,0(R1)         use v23 to test decoder
00001408  E766 7000 1EA1                           750+         VMLH  V22,V22,V23,1      test instruction (dest is a source)
0000140E  E760 5028 080E                 000013D8  751+         VST   V22,V1O6           save v1 output
00001414  07FB                                     752+         BR    R11               return
00001418                                           753+RE6      DC    0F                xl16 expected result
00001418                                           754+         DROP  R5
00001418  FE040009 00190035                        755          DC    XL16'FE04000900190035 00510083009D00EF'   result
00001420  00510083 009D00EF
00001428  FF020304 05060750                        756          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001430  090A0B78 0C0D0EFD
00001438  FF020304 05060750                          757          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00001440  090A0B78 0D0E0FFD
                                                     758
                                                     759          VRR_C VMLH,1
00001448                                             760+         DS    0FD
00001448                      00001448               761+         USING *,R5              base for test data and test routine
00001448  00001488                                   762+T7       DC    A(X7)             address of test routine
0000144C  0007                                       763+         DC    H'7'              test number
0000144E  00                                         764+         DC    X'00'
0000144F  01                                         765+         DC    HL1'1'            m4
00001450  E5D4D3C8 40404040                          766+         DC    CL8'VMLH'         instruction name
00001458  000014C0                                   767+         DC    A(RE7+16)         address of v2 source
0000145C  000014D0                                   768+         DC    A(RE7+32)         address of v3 source
00001460  00000010                                   769+         DC    A(16)             result length
00001464  000014B0                                   770+REA7     DC    A(RE7)            result address
00001468  00000000 00000000                          771+         DS    FD                gap
00001470  00000000 00000000                          772+V1O7     DS    XL16              V1 output
00001478  00000000 00000000
00001480  00000000 00000000                          773+         DS    FD                gap
                                                     774+*
00001488                                             775+X7       DS    0F
00001488  E310 5010 0014                 00000010    776+         LGF   R1,V2ADDR         load v2 source
0000148E  E761 0000 0806                 00000000    777+         VL    v22,0(R1)         use v22 to test decoder
00001494  E310 5014 0014                 00000014    778+         LGF   R1,V3ADDR         load v3 source
0000149A  E771 0000 0806                 00000000    779+         VL    v23,0(R1)         use v23 to test decoder
000014A0  E766 7000 1EA1                             780+         VMLH  V22,V22,V23,1      test instruction (dest is a source)
000014A6  E760 5028 080E                 00001470    781+         VST   V22,V1O7           save v1 output
000014AC  07FB                                       782+         BR    R11               return
000014B0                                             783+RE7      DC    0F                xl16 expected result
000014B0                                             784+         DROP  R5
000014B0  FE030003 000A0017                          785          DC    XL16'FE030003000A0017 0024003C00480077'   result
000014B8  0024003C 00480077
000014C0  FF020304 05060750                          786          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000014C8  090A0B78 0C0D0EFD
000014D0  FF010102 02030328                          787          DC    XL16'FF01010202030328 0405053C060707FE'   v3
000014D8  0405053C 060707FE
                                                     788
                                                     789          VRR_C VMLH,1
000014E0                                             790+         DS    0FD
000014E0                      000014E0               791+         USING *,R5              base for test data and test routine
000014E0  00001520                                   792+T8       DC    A(X8)             address of test routine
000014E4  0008                                       793+         DC    H'8'              test number
000014E6  00                                         794+         DC    X'00'
000014E7  01                                         795+         DC    HL1'1'            m4
000014E8  E5D4D3C8 40404040                          796+         DC    CL8'VMLH'         instruction name
000014F0  00001558                                   797+         DC    A(RE8+16)         address of v2 source
000014F4  00001568                                   798+         DC    A(RE8+32)         address of v3 source
000014F8  00000010                                   799+         DC    A(16)             result length
000014FC  00001548                                   800+REA8     DC    A(RE8)            result address
00001500  00000000 00000000                          801+         DS    FD                gap
00001508  00000000 00000000                          802+V1O8     DS    XL16              V1 output
00001510  00000000 00000000
00001518  00000000 00000000                          803+         DS    FD                gap
                                                     804+*
00001520                                             805+X8       DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001520  E310 5010 0014                00000010   806+         LGF   R1,V2ADDR         load v2 source
00001526  E761 0000 0806                00000000   807+         VL    v22,0(R1)         use v22 to test decoder
0000152C  E310 5014 0014                00000014   808+         LGF   R1,V3ADDR         load v3 source
00001532  E771 0000 0806                00000000   809+         VL    v23,0(R1)         use v23 to test decoder
00001538  E766 7000 1EA1                           810+         VMLH  V22,V22,V23,1      test instruction (dest is a source)
0000153E  E760 5028 080E                00001508   811+         VST   V22,V1O8          save v1 output
00001544  07FB                                     812+         BR    R11               return
00001548                                           813+RE8      DC    0F                xl16 expected result
00001548                                           814+         DROP  R5
00001548  FE020000 00000000                        815          DC    XL16'FE02000000000000 0009000C000C001D'   result
00001550  0009000C 000C001D
00001558  FF020304 05060750                        816          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00001560  090A0B78 0C0D0EFD
00001568  FF000000 0000000A                        817          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00001570  0101010F 010101FF
                                                   818
                                                   819 * Word
                                                   820          VRR_C VMLH,2
00001578                                           821+         DS    0FD
00001578                     00001578              822+         USING *,R5              base for test data and test routine
00001578  000015B8                                 823+T9       DC    A(X9)             address of test routine
0000157C  0009                                     824+         DC    H'9'              test number
0000157E  00                                       825+         DC    X'00'
0000157F  02                                       826+         DC    HL1'2'            m4
00001580  E5D4D3C8 40404040                        827+         DC    CL8'VMLH'         instruction name
00001588  000015F0                                 828+         DC    A(RE9+16)         address of v2 source
0000158C  00001600                                 829+         DC    A(RE9+32)         address of v3 source
00001590  00000010                                 830+         DC    A(16)             result length
00001594  000015E0                                 831+REA9     DC    A(RE9)            result address
00001598  00000000 00000000                        832+         DS    FD                gap
000015A0  00000000 00000000                        833+V1O9     DS    XL16              V1 output
000015A8  00000000 00000000
000015B0  00000000 00000000                        834+         DS    FD                gap
                                                   835+*
000015B8                                           836+X9       DS    0F
000015B8  E310 5010 0014                00000010   837+         LGF   R1,V2ADDR         load v2 source
000015BE  E761 0000 0806                00000000   838+         VL    v22,0(R1)         use v22 to test decoder
000015C4  E310 5014 0014                00000014   839+         LGF   R1,V3ADDR         load v3 source
000015CA  E771 0000 0806                00000000   840+         VL    v23,0(R1)         use v23 to test decoder
000015D0  E766 7000 2EA1                           841+         VMLH  V22,V22,V23,2      test instruction (dest is a source)
000015D6  E760 5028 080E                000015A0   842+         VST   V22,V1O9          save v1 output
000015DC  07FB                                     843+         BR    R11               return
000015E0                                           844+RE9      DC    0F                xl16 expected result
000015E0                                           845+         DROP  R5
000015E0  FFFFFFFE 00000002                        846          DC    XL16'FFFFFFFE00000002 00000000DF01235A'   result
000015E8  00000000 DF01235A
000015F0  FFFFFFFF 00019000                        847          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000015F8  00000038 EEEEEEFA
00001600  FFFFFFFF 00019000                        848          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v3
00001608  00000038 EEEEEEFA
                                                   849
                                                   850          VRR_C VMLH,2
00001610                                           851+         DS    0FD
00001610                     00001610              852+         USING *,R5              base for test data and test routine
00001610  00001650                                 853+T10      DC    A(X10)            address of test routine
00001614  000A                                     854+         DC    H'10'             test number
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001616  00                                      855+         DC    X'00'
00001617  02                                      856+         DC    HL1'2'            m4
00001618  E5D4D3C8 40404040                       857+         DC    CL8'VMLH'         instruction name
00001620  00001688                                858+         DC    A(RE10+16)        address of v2 source
00001624  00001698                                859+         DC    A(RE10+32)        address of v3 source
00001628  00000010                                860+         DC    A(16)             result length
0000162C  00001678                                861+REA10    DC    A(RE10)           result address
00001630  00000000 00000000                       862+         DS    FD                gap
00001638  00000000 00000000                       863+V1O10    DS    XL16              V1 output
00001640  00000000 00000000
00001648  00000000 00000000                       864+         DS    FD                gap
                                                  865+*
00001650                                          866+X10      DS    0F
00001650  E310 5010 0014                 00000010 867+         LGF   R1,V2ADDR         load v2 source
00001656  E761 0000 0806                 00000000 868+         VL    v22,0(R1)         use v22 to test decoder
0000165C  E310 5014 0014                 00000014 869+         LGF   R1,V3ADDR         load v3 source
00001662  E771 0000 0806                 00000000 870+         VL    v23,0(R1)         use v23 to test decoder
00001668  E766 7000 2EA1                          871+         VMLH  V22,V22,V23,2      test instruction (dest is a source)
0000166E  E760 5028 080E                 00001638 872+         VST   V22,V1O10          save v1 output
00001674  07FB                                    873+         BR    R11               return
00001678                                          874+RE10     DC    0F                xl16 expected result
00001678                                          875+         DROP  R5
00001678  FE050206 00193C6D                       876          DC    XL16'FE05020600193C6D 0051B52B00AA6E58'   result
00001680  0051B52B 00AA6E58
00001688  FF020304 05060750                       877          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00001690  090A0B0C 0D0E0F7F
00001698  FF020304 05060750                       878          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v3
000016A0  090A0B0C 0D0E0F7F
                                                  879
                                                  880          VRR_C VMLH,2
000016A8                                          881+         DS    0FD
000016A8                         000016A8         882+         USING *,R5              base for test data and test routine
000016A8  000016E8                                883+T11      DC    A(X11)            address of test routine
000016AC  000B                                    884+         DC    H'11'             test number
000016AE  00                                      885+         DC    X'00'
000016AF  02                                      886+         DC    HL1'2'            m4
000016B0  E5D4D3C8 40404040                       887+         DC    CL8'VMLH'         instruction name
000016B8  00001720                                888+         DC    A(RE11+16)        address of v2 source
000016BC  00001730                                889+         DC    A(RE11+32)        address of v3 source
000016C0  00000010                                890+         DC    A(16)             result length
000016C4  00001710                                891+REA11    DC    A(RE11)           result address
000016C8  00000000 00000000                       892+         DS    FD                gap
000016D0  00000000 00000000                       893+V1O11    DS    XL16              V1 output
000016D8  00000000 00000000
000016E0  00000000 00000000                       894+         DS    FD                gap
                                                  895+*
000016E8                                          896+X11      DS    0F
000016E8  E310 5010 0014                 00000010 897+         LGF   R1,V2ADDR         load v2 source
000016EE  E761 0000 0806                 00000000 898+         VL    v22,0(R1)         use v22 to test decoder
000016F4  E310 5014 0014                 00000014 899+         LGF   R1,V3ADDR         load v3 source
000016FA  E771 0000 0806                 00000000 900+         VL    v23,0(R1)         use v23 to test decoder
00001700  E766 7000 2EA1                          901+         VMLH  V22,V22,V23,2      test instruction (dest is a source)
00001706  E760 5028 080E                 000016D0 902+         VST   V22,V1O11          save v1 output
0000170C  07FB                                    903+         BR    R11               return
00001710                                          904+RE11     DC    0F                xl16 expected result
00001710                                          905+         DROP  R5
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001710  FE040103 000A1B30                          906          DC    XL16'FE040103000A1B30 0024558D004EB01D'   result
00001718  0024558D 004EB01D
00001720  FF020304 05060750                          907          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00001728  090A0B0C 0D0E0F7F
00001730  FF010102 02030328                          908          DC    XL16'FF01010202030328 0405053C0607073F'   v3
00001738  0405053C 0607073F
                                                     909
                                                     910          VRR_C VMLH,2
00001740                                             911+         DS    0FD
00001740                       00001740              912+         USING *,R5              base for test data and test routine
00001740  00001780                                   913+T12      DC    A(X12)            address of test routine
00001744  000C                                       914+         DC    H'12'             test number
00001746  00                                         915+         DC    X'00'
00001747  02                                         916+         DC    HL1'2'            m4
00001748  E5D4D3C8 40404040                          917+         DC    CL8'VMLH'         instruction name
00001750  000017B8                                   918+         DC    A(RE12+16)        address of v2 source
00001754  000017C8                                   919+         DC    A(RE12+32)        address of v3 source
00001758  00000010                                   920+         DC    A(16)             result length
0000175C  000017A8                                   921+REA12    DC    A(RE12)           result address
00001760  00000000 00000000                          922+         DS    FD                gap
00001768  00000000 00000000                          923+V1O12    DS    XL16              V1 output
00001770  00000000 00000000
00001778  00000000 00000000                          924+         DS    FD                gap
                                                     925+*
00001780                                             926+X12      DS    0F
00001780  E310 5010 0014                 00000010    927+         LGF   R1,V2ADDR         load v2 source
00001786  E761 0000 0806                 00000000    928+         VL    v22,0(R1)         use v22 to test decoder
0000178C  E310 5014 0014                 00000014    929+         LGF   R1,V3ADDR         load v3 source
00001792  E771 0000 0806                 00000000    930+         VL    v23,0(R1)         use v23 to test decoder
00001798  E766 7000 2EA1                             931+         VMLH  V22,V22,V23,2      test instruction (dest is a source)
0000179E  E760 5028 080E                 00001768    932+         VST   V22,V1O12          save v1 output
000017A4  07FB                                       933+         BR    R11               return
000017A8                                             934+RE12     DC    0F                xl16 expected result
000017A8                                             935+         DROP  R5
000017A8  FE030100 00000000                          936          DC    XL16'FE03010000000000 0009131E000D1B2B'   result
000017B0  0009131E 000D1B2B
000017B8  FF020304 05060750                          937          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000017C0  090A0B0C 0D0E0F7F
000017C8  FF000000 0000000A                          938          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
000017D0  0101010F 0101010F
                                                     939
                                                     940 * Doubleword
                                                     941          VRR_C VMLH,3
000017D8                                             942+         DS    0FD
000017D8                       000017D8              943+         USING *,R5              base for test data and test routine
000017D8  00001818                                   944+T13      DC    A(X13)            address of test routine
000017DC  000D                                       945+         DC    H'13'             test number
000017DE  00                                         946+         DC    X'00'
000017DF  03                                         947+         DC    HL1'3'            m4
000017E0  E5D4D3C8 40404040                          948+         DC    CL8'VMLH'         instruction name
000017E8  00001850                                   949+         DC    A(RE13+16)        address of v2 source
000017EC  00001860                                   950+         DC    A(RE13+32)        address of v3 source
000017F0  00000010                                   951+         DC    A(16)             result length
000017F4  00001840                                   952+REA13    DC    A(RE13)           result address
000017F8  00000000 00000000                          953+         DS    FD                gap
00001800  00000000 00000000                          954+V1O13    DS    XL16              V1 output
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001808  00000000 00000000
00001810  00000000 00000000                        955+         DS    FD                gap
                                                   956+*
00001818                                           957+X13      DS    0F
00001818  E310 5010 0014                 00000010  958+         LGF   R1,V2ADDR         load v2 source
0000181E  E761 0000 0806                 00000000  959+         VL    v22,0(R1)         use v22 to test decoder
00001824  E310 5014 0014                 00000014  960+         LGF   R1,V3ADDR         load v3 source
0000182A  E771 0000 0806                 00000000  961+         VL    v23,0(R1)         use v23 to test decoder
00001830  E766 7000 3EA1                           962+         VMLH  V22,V22,V23,3      test instruction (dest is a source)
00001836  E760 5028 080E                 00001800  963+         VST   V22,V1O13          save v1 output
0000183C  07FB                                     964+         BR    R11               return
00001840                                           965+RE13     DC    0F                xl16 expected result
00001840                                           966+         DROP  R5
00001840  FFFFFFFE 00032000                        967          DC    XL16'FFFFFFFE00032000 0000000000000C77'   result
00001848  00000000 00000C77
00001850  FFFFFFFF 00019000                        968          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00001858  00000038 EEEEEEFA
00001860  FFFFFFFF 00019000                        969          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00001868  00000038 0EEEEEFA
                                                   970
                                                   971          VRR_C VMLH,3
00001870                                           972+         DS    0FD
00001870                       00001870            973+         USING *,R5              base for test data and test routine
00001870  000018B0                                 974+T14      DC    A(X14)            address of test routine
00001874  000E                                     975+         DC    H'14'             test number
00001876  00                                       976+         DC    X'00'
00001877  03                                       977+         DC    HL1'3'            m4
00001878  E5D4D3C8 40404040                        978+         DC    CL8'VMLH'         instruction name
00001880  000018E8                                 979+         DC    A(RE14+16)        address of v2 source
00001884  000018F8                                 980+         DC    A(RE14+32)        address of v3 source
00001888  00000010                                 981+         DC    A(16)             result length
0000188C  000018D8                                 982+REA14    DC    A(RE14)           result address
00001890  00000000 00000000                        983+         DS    FD                gap
00001898  00000000 00000000                        984+V1O14    DS    XL16              V1 output
000018A0  00000000 00000000
000018A8  00000000 00000000                        985+         DS    FD                gap
                                                   986+*
000018B0                                           987+X14      DS    0F
000018B0  E310 5010 0014                 00000010  988+         LGF   R1,V2ADDR         load v2 source
000018B6  E761 0000 0806                 00000000  989+         VL    v22,0(R1)         use v22 to test decoder
000018BC  E310 5014 0014                 00000014  990+         LGF   R1,V3ADDR         load v3 source
000018C2  E771 0000 0806                 00000000  991+         VL    v23,0(R1)         use v23 to test decoder
000018C8  E766 7000 3EA1                           992+         VMLH  V22,V22,V23,3      test instruction (dest is a source)
000018CE  E760 5028 080E                 00001898  993+         VST   V22,V1O14          save v1 output
000018D4  07FB                                     994+         BR    R11               return
000018D8                                           995+RE14     DC    0F                xl16 expected result
000018D8                                           996+         DROP  R5
000018D8  01010308 111F3396                        997          DC    XL16'01010308111F3396 0051B52F8692B4F6'   result
000018E0  0051B52F 8692B4F6
000018E8  FF020304 05060750                        998          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000018F0  090A0B0C 0D0E0F7F
000018F8  01020304 05060750                        999          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00001900  090A0B78 0D0E0F7F
                                                  1000
                                                  1001          VRR_C VMLH,3
00001908                                          1002+         DS    0FD
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001908                     00001908            1003+         USING *,R5              base for test data and test routine
00001908  00001948                               1004+T15      DC    A(X15)            address of test routine
0000190C  000F                                   1005+         DC    H'15'             test number
0000190E  00                                     1006+         DC    X'00'
0000190F  03                                     1007+         DC    HL1'3'            m4
00001910  E5D4D3C8 40404040                      1008+         DC    CL8'VMLH'         instruction name
00001918  00001980                               1009+         DC    A(RE15+16)        address of v2 source
0000191C  00001990                               1010+         DC    A(RE15+32)        address of v3 source
00001920  00000010                               1011+         DC    A(16)             result length
00001924  00001970                               1012+REA15    DC    A(RE15)           result address
00001928  00000000 00000000                      1013+         DS    FD                gap
00001930  00000000 00000000                      1014+V1O15    DS    XL16              V1 output
00001938  00000000 00000000
00001940  00000000 00000000                      1015+         DS    FD                gap
                                                 1016+*
00001948                                         1017+X15      DS    0F
00001948  E310 5010 0014                 00000010 1018+         LGF   R1,V2ADDR         load v2 source
0000194E  E761 0000 0806                 00000000 1019+         VL    v22,0(R1)         use v22 to test decoder
00001954  E310 5014 0014                 00000014 1020+         LGF   R1,V3ADDR         load v3 source
0000195A  E771 0000 0806                 00000000 1021+         VL    v23,0(R1)         use v23 to test decoder
00001960  E766 7000 3EA1                          1022+         VMLH  V22,V22,V23,3      test instruction (dest is a source)
00001966  E760 5028 080E                 00001930 1023+         VST   V22,V1O15          save v1 output
0000196C  07FB                                   1024+         BR    R11               return
00001970                                         1025+RE15     DC    0F                xl16 expected result
00001970                                         1026+         DROP  R5
00001970  00010003 050C1344                      1027          DC    XL16'00010003050C1344 0024558DB838C862'   result
00001978  0024558D B838C862
00001980  FF020304 05060750                      1028          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00001988  090A0B0C 0D0E0F7F
00001990  00010102 02030328                      1029          DC    XL16'0001010202030328 0405053C0607073F'   v3
00001998  0405053C 0607073F
                                                 1030
                                                 1031          VRR_C VMLH,3
000019A0                                         1032+         DS    0FD
000019A0                     000019A0            1033+         USING *,R5              base for test data and test routine
000019A0  000019E0                               1034+T16      DC    A(X16)            address of test routine
000019A4  0010                                   1035+         DC    H'16'             test number
000019A6  00                                     1036+         DC    X'00'
000019A7  03                                     1037+         DC    HL1'3'            m4
000019A8  E5D4D3C8 40404040                      1038+         DC    CL8'VMLH'         instruction name
000019B0  00001A18                               1039+         DC    A(RE16+16)        address of v2 source
000019B4  00001A28                               1040+         DC    A(RE16+32)        address of v3 source
000019B8  00000010                               1041+         DC    A(16)             result length
000019BC  00001A08                               1042+REA16    DC    A(RE16)           result address
000019C0  00000000 00000000                      1043+         DS    FD                gap
000019C8  00000000 00000000                      1044+V1O16    DS    XL16              V1 output
000019D0  00000000 00000000
000019D8  00000000 00000000                      1045+         DS    FD                gap
                                                 1046+*
000019E0                                         1047+X16      DS    0F
000019E0  E310 5010 0014                 00000010 1048+         LGF   R1,V2ADDR         load v2 source
000019E6  E761 0000 0806                 00000000 1049+         VL    v22,0(R1)         use v22 to test decoder
000019EC  E310 5014 0014                 00000014 1050+         LGF   R1,V3ADDR         load v3 source
000019F2  E771 0000 0806                 00000000 1051+         VL    v23,0(R1)         use v23 to test decoder
000019F8  E766 7000 3EA1                          1052+         VMLH  V22,V22,V23,3      test instruction (dest is a source)
000019FE  E760 5028 080E                 000019C8 1053+         VST   V22,V1O16          save v1 output
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001A04  07FB                                     1054+         BR    R11                 return
00001A08                                           1055+RE16     DC    0F                  xl16 expected result
00001A08                                           1056+         DROP  R5
00001A08  00000000 00000009                        1057          DC    XL16'0000000000000009 0009131EA8C3DFFE'   result
00001A10  0009131E A8C3DFFE
00001A18  FF020304 05060750                        1058          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00001A20  090A0B0C 0D0E0F7F
00001A28  00000000 0000000A                        1059          DC    XL16'000000000000000A 0101010F0101010F'   v3
00001A30  0101010F 0101010F
                                                   1060
                                                   1061 * Quadword
                                                   1062          VRR_C VMLH,4
00001A38                                           1063+         DS    0FD
00001A38                     00001A38              1064+         USING *,R5                base for test data and test routine
00001A38  00001A78                                 1065+T17      DC    A(X17)              address of test routine
00001A3C  0011                                     1066+         DC    H'17'               test number
00001A3E  00                                       1067+         DC    X'00'
00001A3F  04                                       1068+         DC    HL1'4'              m4
00001A40  E5D4D3C8 40404040                        1069+         DC    CL8'VMLH'           instruction name
00001A48  00001AB0                                 1070+         DC    A(RE17+16)          address of v2 source
00001A4C  00001AC0                                 1071+         DC    A(RE17+32)          address of v3 source
00001A50  00000010                                 1072+         DC    A(16)               result length
00001A54  00001AA0                                 1073+REA17    DC    A(RE17)             result address
00001A58  00000000 00000000                        1074+         DS    FD                  gap
00001A60  00000000 00000000                        1075+V1O17    DS    XL16                V1 output
00001A68  00000000 00000000
00001A70  00000000 00000000                        1076+         DS    FD                  gap
                                                   1077+*
00001A78                                           1078+X17      DS    0F
00001A78  E310 5010 0014                 00000010  1079+         LGF   R1,V2ADDR           load v2 source
00001A7E  E761 0000 0806                 00000000  1080+         VL    v22,0(R1)           use v22 to test decoder
00001A84  E310 5014 0014                 00000014  1081+         LGF   R1,V3ADDR           load v3 source
00001A8A  E771 0000 0806                 00000000  1082+         VL    v23,0(R1)           use v23 to test decoder
00001A90  E766 7000 4EA1                           1083+         VMLH  V22,V22,V23,4        test instruction (dest is a source)
00001A96  E760 5028 080E                 00001A60  1084+         VST   V22,V1O17            save v1 output
00001A9C  07FB                                     1085+         BR    R11                 return
00001AA0                                           1086+RE17     DC    0F                  xl16 expected result
00001AA0                                           1087+         DROP  R5
00001AA0  E1000000 00000000                        1088          DC    XL16'E1000000 00000000 00000000 00000000'   result
00001AA8  00000000 00000000
00001AB0  F0000000 00000000                        1089          DC    XL16'F0000000 00000000 00000000 00000000'   v2
00001AB8  00000000 00000000
00001AC0  F0000000 00000000                        1090          DC    XL16'F0000000 00000000 00000000 00000000'   v3
00001AC8  00000000 00000000
                                                   1091
                                                   1092          VRR_C VMLH,4
00001AD0                                           1093+         DS    0FD
00001AD0                     00001AD0              1094+         USING *,R5                base for test data and test routine
00001AD0  00001B10                                 1095+T18      DC    A(X18)              address of test routine
00001AD4  0012                                     1096+         DC    H'18'               test number
00001AD6  00                                       1097+         DC    X'00'
00001AD7  04                                       1098+         DC    HL1'4'              m4
00001AD8  E5D4D3C8 40404040                        1099+         DC    CL8'VMLH'           instruction name
00001AE0  00001B48                                 1100+         DC    A(RE18+16)          address of v2 source
00001AE4  00001B58                                 1101+         DC    A(RE18+32)          address of v3 source
00001AE8  00000010                                 1102+         DC    A(16)               result length
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001AEC  00001B38                                 1103+REA18    DC    A(RE18)            result address
00001AF0  00000000 00000000                        1104+         DS    FD                 gap
00001AF8  00000000 00000000                        1105+V1O18    DS    XL16               V1 output
00001B00  00000000 00000000
00001B08  00000000 00000000                        1106+         DS    FD                 gap
                                                   1107+*
00001B10                                           1108+X18      DS    0F
00001B10  E310 5010 0014                 00000010  1109+         LGF   R1,V2ADDR          load v2 source
00001B16  E761 0000 0806                 00000000  1110+         VL    v22,0(R1)          use v22 to test decoder
00001B1C  E310 5014 0014                 00000014  1111+         LGF   R1,V3ADDR          load v3 source
00001B22  E771 0000 0806                 00000000  1112+         VL    v23,0(R1)          use v23 to test decoder
00001B28  E766 7000 4EA1                           1113+         VMLH  V22,V22,V23,4       test instruction (dest is a source)
00001B2E  E760 5028 080E                 00001AF8  1114+         VST   V22,V1O18           save v1 output
00001B34  07FB                                     1115+         BR    R11                return
00001B38                                           1116+RE18     DC    0F                 xl16 expected result
00001B38                                           1117+         DROP  R5
00001B38  E101C200 E1000000                        1118          DC    XL16'E101C200 E1000000 00000000 00000000'   result
00001B40  00000000 00000000
00001B48  F000F000 00000000                        1119          DC    XL16'F000F000 00000000 00000000 00000000'   v2
00001B50  00000000 00000000
00001B58  F000F000 00000000                        1120          DC    XL16'F000F000 00000000 00000000 00000000'   v3
00001B60  00000000 00000000
                                                   1121
                                                   1122          VRR_C VMLH,4
00001B68                                           1123+         DS    0FD
00001B68                      00001B68             1124+         USING *,R5               base for test data and test routine
00001B68  00001BA8                                 1125+T19      DC    A(X19)             address of test routine
00001B6C  0013                                     1126+         DC    H'19'              test number
00001B6E  00                                       1127+         DC    X'00'
00001B6F  04                                       1128+         DC    HL1'4'             m4
00001B70  E5D4D3C8 40404040                        1129+         DC    CL8'VMLH'          instruction name
00001B78  00001BE0                                 1130+         DC    A(RE19+16)         address of v2 source
00001B7C  00001BF0                                 1131+         DC    A(RE19+32)         address of v3 source
00001B80  00000010                                 1132+         DC    A(16)              result length
00001B84  00001BD0                                 1133+REA19    DC    A(RE19)            result address
00001B88  00000000 00000000                        1134+         DS    FD                 gap
00001B90  00000000 00000000                        1135+V1O19    DS    XL16               V1 output
00001B98  00000000 00000000
00001BA0  00000000 00000000                        1136+         DS    FD                 gap
                                                   1137+*
00001BA8                                           1138+X19      DS    0F
00001BA8  E310 5010 0014                 00000010  1139+         LGF   R1,V2ADDR          load v2 source
00001BAE  E761 0000 0806                 00000000  1140+         VL    v22,0(R1)          use v22 to test decoder
00001BB4  E310 5014 0014                 00000014  1141+         LGF   R1,V3ADDR          load v3 source
00001BBA  E771 0000 0806                 00000000  1142+         VL    v23,0(R1)          use v23 to test decoder
00001BC0  E766 7000 4EA1                           1143+         VMLH  V22,V22,V23,4       test instruction (dest is a source)
00001BC6  E760 5028 080E                 00001B90  1144+         VST   V22,V1O19           save v1 output
00001BCC  07FB                                     1145+         BR    R11                return
00001BD0                                           1146+RE19     DC    0F                 xl16 expected result
00001BD0                                           1147+         DROP  R5
00001BD0  E101C201 C200E100                        1148          DC    XL16'E101C201 C200E100 00000000 00000000'   result
00001BD8  00000000 00000000
00001BE0  F000F000 F0000000                        1149          DC    XL16'F000F000 F0000000 00000000 00000000'   v2
00001BE8  00000000 00000000
00001BF0  F000F000 00000000                        1150          DC    XL16'F000F000 00000000 00000000 00000000'   v3
00001BF8  00000000 00000000
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1151
                                                   1152          VRR_C VMLH,4
00001C00                                           1153+         DS    0FD
00001C00                       00001C00            1154+         USING *,R5              base for test data and test routine
00001C00  00001C40                                 1155+T20      DC    A(X20)            address of test routine
00001C04  0014                                     1156+         DC    H'20'             test number
00001C06  00                                       1157+         DC    X'00'
00001C07  04                                       1158+         DC    HL1'4'            m4
00001C08  E5D4D3C8 40404040                        1159+         DC    CL8'VMLH'         instruction name
00001C10  00001C78                                 1160+         DC    A(RE20+16)        address of v2 source
00001C14  00001C88                                 1161+         DC    A(RE20+32)        address of v3 source
00001C18  00000010                                 1162+         DC    A(16)             result length
00001C1C  00001C68                                 1163+REA20    DC    A(RE20)           result address
00001C20  00000000 00000000                        1164+         DS    FD                gap
00001C28  00000000 00000000                        1165+V1O20    DS    XL16              V1 output
00001C30  00000000 00000000
00001C38  00000000 00000000                        1166+         DS    FD                gap
                                                   1167+*
00001C40                                           1168+X20      DS    0F
00001C40  E310 5010 0014                 00000010  1169+         LGF   R1,V2ADDR         load v2 source
00001C46  E761 0000 0806                 00000000  1170+         VL    v22,0(R1)         use v22 to test decoder
00001C4C  E310 5014 0014                 00000014  1171+         LGF   R1,V3ADDR         load v3 source
00001C52  E771 0000 0806                 00000000  1172+         VL    v23,0(R1)         use v23 to test decoder
00001C58  E766 7000 4EA1                           1173+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001C5E  E760 5028 080E                 00001C28  1174+         VST   V22,V1O20          save v1 output
00001C64  07FB                                     1175+         BR    R11               return
00001C68                                           1176+RE20     DC    0F                xl16 expected result
00001C68                                           1177+         DROP  R5
00001C68  E101C201 C200E100                        1178          DC    XL16'E101C201 C200E100 E100E100 E1000000'   result
00001C70  E100E100 E1000000
00001C78  F000F000 F0000000                        1179          DC    XL16'F000F000 F0000000 00000000 00000000'   v2
00001C80  00000000 00000000
00001C88  F000F000 00000000                        1180          DC    XL16'F000F000 00000000 F0000000 00000000'   v3
00001C90  F0000000 00000000
                                                   1181
                                                   1182          VRR_C VMLH,4
00001C98                                           1183+         DS    0FD
00001C98                       00001C98            1184+         USING *,R5              base for test data and test routine
00001C98  00001CD8                                 1185+T21      DC    A(X21)            address of test routine
00001C9C  0015                                     1186+         DC    H'21'             test number
00001C9E  00                                       1187+         DC    X'00'
00001C9F  04                                       1188+         DC    HL1'4'            m4
00001CA0  E5D4D3C8 40404040                        1189+         DC    CL8'VMLH'         instruction name
00001CA8  00001D10                                 1190+         DC    A(RE21+16)        address of v2 source
00001CAC  00001D20                                 1191+         DC    A(RE21+32)        address of v3 source
00001CB0  00000010                                 1192+         DC    A(16)             result length
00001CB4  00001D00                                 1193+REA21    DC    A(RE21)           result address
00001CB8  00000000 00000000                        1194+         DS    FD                gap
00001CC0  00000000 00000000                        1195+V1O21    DS    XL16              V1 output
00001CC8  00000000 00000000
00001CD0  00000000 00000000                        1196+         DS    FD                gap
                                                   1197+*
00001CD8                                           1198+X21      DS    0F
00001CD8  E310 5010 0014                 00000010  1199+         LGF   R1,V2ADDR         load v2 source
00001CDE  E761 0000 0806                 00000000  1200+         VL    v22,0(R1)         use v22 to test decoder
00001CE4  E310 5014 0014                 00000014  1201+         LGF   R1,V3ADDR         load v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001CEA  E771 0000 0806                00000000  1202+         VL    v23,0(R1)         use v23 to test decoder
00001CF0  E766 7000 4EA1                          1203+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001CF6  E760 5028 080E                00001CC0  1204+         VST   V22,V1O21          save v1 output
00001CFC  07FB                                    1205+         BR    R11               return
00001D00                                          1206+RE21     DC    0F                xl16 expected result
00001D00                                          1207+         DROP  R5
00001D00  00000001 00000001                       1208          DC    XL16'00000001 00000001 00000001 00000000'   result
00001D08  00000001 00000000
00001D10  FFFFFFFF FFFFFFFF                       1209          DC    XL16'FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF'   v2
00001D18  FFFFFFFF FFFFFFFF
00001D20  00000001 00000001                       1210          DC    XL16'00000001 00000001 00000001 00000001'   v3
00001D28  00000001 00000001
                                                  1211
                                                  1212          VRR_C VMLH,4
00001D30                                          1213+         DS    0FD
00001D30                     00001D30             1214+         USING *,R5              base for test data and test routine
00001D30  00001D70                                1215+T22      DC    A(X22)            address of test routine
00001D34  0016                                    1216+         DC    H'22'             test number
00001D36  00                                      1217+         DC    X'00'
00001D37  04                                      1218+         DC    HL1'4'            m4
00001D38  E5D4D3C8 40404040                       1219+         DC    CL8'VMLH'         instruction name
00001D40  00001DA8                                1220+         DC    A(RE22+16)        address of v2 source
00001D44  00001DB8                                1221+         DC    A(RE22+32)        address of v3 source
00001D48  00000010                                1222+         DC    A(16)             result length
00001D4C  00001D98                                1223+REA22    DC    A(RE22)           result address
00001D50  00000000 00000000                       1224+         DS    FD                gap
00001D58  00000000 00000000                       1225+V1O22    DS    XL16              V1 output
00001D60  00000000 00000000
00001D68  00000000 00000000                       1226+         DS    FD                gap
                                                  1227+*
00001D70                                          1228+X22      DS    0F
00001D70  E310 5010 0014                00000010  1229+         LGF   R1,V2ADDR         load v2 source
00001D76  E761 0000 0806                00000000  1230+         VL    v22,0(R1)         use v22 to test decoder
00001D7C  E310 5014 0014                00000014  1231+         LGF   R1,V3ADDR         load v3 source
00001D82  E771 0000 0806                00000000  1232+         VL    v23,0(R1)         use v23 to test decoder
00001D88  E766 7000 4EA1                          1233+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001D8E  E760 5028 080E                00001D58  1234+         VST   V22,V1O22          save v1 output
00001D94  07FB                                    1235+         BR    R11               return
00001D98                                          1236+RE22     DC    0F                xl16 expected result
00001D98                                          1237+         DROP  R5
00001D98  FFFFFFFE 00032000                       1238          DC    XL16'FFFFFFFE 00032000 FFFCE073 6EDDDD83'   result
00001DA0  FFFCE073 6EDDDD83
00001DA8  FFFFFFFF 00019000                       1239          DC    XL16'FFFFFFFF 00019000 00000038 EEEEEEFA'   v2
00001DB0  00000038 EEEEEEFA
00001DB8  FFFFFFFF 00019000                       1240          DC    XL16'FFFFFFFF 00019000 00000038 0EEEEEFA'   v3
00001DC0  00000038 0EEEEEFA
                                                  1241
                                                  1242          VRR_C VMLH,4
00001DC8                                          1243+         DS    0FD
00001DC8                     00001DC8             1244+         USING *,R5              base for test data and test routine
00001DC8  00001E08                                1245+T23      DC    A(X23)            address of test routine
00001DCC  0017                                    1246+         DC    H'23'             test number
00001DCE  00                                      1247+         DC    X'00'
00001DCF  04                                      1248+         DC    HL1'4'            m4
00001DD0  E5D4D3C8 40404040                       1249+         DC    CL8'VMLH'         instruction name
00001DD8  00001E40                                1250+         DC    A(RE23+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001DDC  00001E50                                 1251+         DC    A(RE23+32)        address of v3 source
00001DE0  00000010                                 1252+         DC    A(16)             result length
00001DE4  00001E30                                 1253+REA23    DC    A(RE23)           result address
00001DE8  00000000 00000000                        1254+         DS    FD                gap
00001DF0  00000000 00000000                        1255+V1O23    DS    XL16              V1 output
00001DF8  00000000 00000000
00001E00  00000000 00000000                        1256+         DS    FD                gap
                                                   1257+*
00001E08                                           1258+X23      DS    0F
00001E08  E310 5010 0014                 00000010  1259+         LGF   R1,V2ADDR         load v2 source
00001E0E  E761 0000 0806                 00000000  1260+         VL    v22,0(R1)         use v22 to test decoder
00001E14  E310 5014 0014                 00000014  1261+         LGF   R1,V3ADDR         load v3 source
00001E1A  E771 0000 0806                 00000000  1262+         VL    v23,0(R1)         use v23 to test decoder
00001E20  E766 7000 4EA1                           1263+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001E26  E760 5028 080E                 00001DF0  1264+         VST   V22,V1O23          save v1 output
00001E2C  07FB                                     1265+         BR    R11               return
00001E30                                           1266+RE23     DC    0F                xl16 expected result
00001E30                                           1267+         DROP  R5
00001E30  01010308 111F3396                        1268          DC    XL16'01010308 111F3396 72BF86C3 CAFA7483'   result
00001E38  72BF86C3 CAFA7483
00001E40  FF020304 05060750                        1269          DC    XL16'FF020304 05060750 090A0B0C 0D0E0F7F'   v2
00001E48  090A0B0C 0D0E0F7F
00001E50  01020304 05060750                        1270          DC    XL16'01020304 05060750 090A0B78 0D0E0F7F'   v3
00001E58  090A0B78 0D0E0F7F
                                                   1271
                                                   1272          VRR_C VMLH,4
00001E60                                           1273+         DS    0FD
00001E60                       00001E60            1274+         USING *,R5              base for test data and test routine
00001E60  00001EA0                                 1275+T24      DC    A(X24)            address of test routine
00001E64  0018                                     1276+         DC    H'24'             test number
00001E66  00                                       1277+         DC    X'00'
00001E67  04                                       1278+         DC    HL1'4'            m4
00001E68  E5D4D3C8 40404040                        1279+         DC    CL8'VMLH'         instruction name
00001E70  00001ED8                                 1280+         DC    A(RE24+16)        address of v2 source
00001E74  00001EE8                                 1281+         DC    A(RE24+32)        address of v3 source
00001E78  00000010                                 1282+         DC    A(16)             result length
00001E7C  00001EC8                                 1283+REA24    DC    A(RE24)           result address
00001E80  00000000 00000000                        1284+         DS    FD                gap
00001E88  00000000 00000000                        1285+V1O24    DS    XL16              V1 output
00001E90  00000000 00000000
00001E98  00000000 00000000                        1286+         DS    FD                gap
                                                   1287+*
00001EA0                                           1288+X24      DS    0F
00001EA0  E310 5010 0014                 00000010  1289+         LGF   R1,V2ADDR         load v2 source
00001EA6  E761 0000 0806                 00000000  1290+         VL    v22,0(R1)         use v22 to test decoder
00001EAC  E310 5014 0014                 00000014  1291+         LGF   R1,V3ADDR         load v3 source
00001EB2  E771 0000 0806                 00000000  1292+         VL    v23,0(R1)         use v23 to test decoder
00001EB8  E766 7000 4EA1                           1293+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001EBE  E760 5028 080E                 00001E88  1294+         VST   V22,V1O24          save v1 output
00001EC4  07FB                                     1295+         BR    R11               return
00001EC8                                           1296+RE24     DC    0F                xl16 expected result
00001EC8                                           1297+         DROP  R5
00001EC8  00010003 050C1344                        1298          DC    XL16'00010003 050C1344 0AD40FD0 ABE579A1'   result
00001ED0  0AD40FD0 ABE579A1
00001ED8  FF020304 05060750                        1299          DC    XL16'FF020304 05060750 090A0B0C 0D0E0F7F'   v2
00001EE0  090A0B0C 0D0E0F7F
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00001EE8  00010102 02030328                        1300          DC    XL16'00010102 02030328 0405053C 0607073F'   v3
00001EF0  0405053C 0607073F
                                                   1301
                                                   1302          VRR_C VMLH,4
00001EF8                                           1303+         DS    0FD
00001EF8                     00001EF8              1304+         USING *,R5              base for test data and test routine
00001EF8  00001F38                                 1305+T25      DC    A(X25)            address of test routine
00001EFC  0019                                     1306+         DC    H'25'             test number
00001EFE  00                                       1307+         DC    X'00'
00001EFF  04                                       1308+         DC    HL1'4'            m4
00001F00  E5D4D3C8 40404040                        1309+         DC    CL8'VMLH'         instruction name
00001F08  00001F70                                 1310+         DC    A(RE25+16)        address of v2 source
00001F0C  00001F80                                 1311+         DC    A(RE25+32)        address of v3 source
00001F10  00000010                                 1312+         DC    A(16)             result length
00001F14  00001F60                                 1313+REA25    DC    A(RE25)           result address
00001F18  00000000 00000000                        1314+         DS    FD                gap
00001F20  00000000 00000000                        1315+V1O25    DS    XL16              V1 output
00001F28  00000000 00000000
00001F30  00000000 00000000                        1316+         DS    FD                gap
                                                   1317+*
00001F38                                           1318+X25      DS    0F
00001F38  E310 5010 0014                00000010   1319+         LGF   R1,V2ADDR         load v2 source
00001F3E  E761 0000 0806                00000000   1320+         VL    v22,0(R1)         use v22 to test decoder
00001F44  E310 5014 0014                00000014   1321+         LGF   R1,V3ADDR         load v3 source
00001F4A  E771 0000 0806                00000000   1322+         VL    v23,0(R1)         use v23 to test decoder
00001F50  E766 7000 4EA1                           1323+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001F56  E760 5028 080E                00001F20   1324+         VST   V22,V1O25          save v1 output
00001F5C  07FB                                     1325+         BR    R11               return
00001F60                                           1326+RE25     DC    0F                xl16 expected result
00001F60                                           1327+         DROP  R5
00001F60  00000000 00000009                        1328          DC    XL16'00000000 00000009 F714203B 2D668781'   result
00001F68  F714203B 2D668781
00001F70  FF020304 05060750                        1329          DC    XL16'FF020304 05060750 090A0B0C 0D0E0F7F'   v2
00001F78  090A0B0C 0D0E0F7F
00001F80  00000000 0000000A                        1330          DC    XL16'00000000 0000000A 0101010F 0101010F'   v3
00001F88  0101010F 0101010F
                                                   1331
                                                   1332          VRR_C VMLH,4
00001F90                                           1333+         DS    0FD
00001F90                     00001F90              1334+         USING *,R5              base for test data and test routine
00001F90  00001FD0                                 1335+T26      DC    A(X26)            address of test routine
00001F94  001A                                     1336+         DC    H'26'             test number
00001F96  00                                       1337+         DC    X'00'
00001F97  04                                       1338+         DC    HL1'4'            m4
00001F98  E5D4D3C8 40404040                        1339+         DC    CL8'VMLH'         instruction name
00001FA0  00002008                                 1340+         DC    A(RE26+16)        address of v2 source
00001FA4  00002018                                 1341+         DC    A(RE26+32)        address of v3 source
00001FA8  00000010                                 1342+         DC    A(16)             result length
00001FAC  00001FF8                                 1343+REA26    DC    A(RE26)           result address
00001FB0  00000000 00000000                        1344+         DS    FD                gap
00001FB8  00000000 00000000                        1345+V1O26    DS    XL16              V1 output
00001FC0  00000000 00000000
00001FC8  00000000 00000000                        1346+         DS    FD                gap
                                                   1347+*
00001FD0                                           1348+X26      DS    0F
00001FD0  E310 5010 0014                00000010   1349+         LGF   R1,V2ADDR         load v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00001FD6  E761 0000 0806                00000000  1350+         VL    v22,0(R1)         use v22 to test decoder
00001FDC  E310 5014 0014                00000014  1351+         LGF   R1,V3ADDR         load v3 source
00001FE2  E771 0000 0806                00000000  1352+         VL    v23,0(R1)         use v23 to test decoder
00001FE8  E766 7000 4EA1                          1353+         VMLH  V22,V22,V23,4      test instruction (dest is a source)
00001FEE  E760 5028 080E                00001FB8  1354+         VST   V22,V1O26          save v1 output
00001FF4  07FB                                    1355+         BR    R11               return
00001FF8                                          1356+RE26     DC    0F                xl16 expected result
00001FF8                                          1357+         DROP  R5
00001FF8  4665B5B7 6BD3F0C3                       1358          DC    XL16'4665B5B7 6BD3F0C3 4C8D873A A8D2B95D'   result
00002000  4C8D873A A8D2B95D
00002008  50515253 54555657                       1359          DC    XL16'50515253 54555657 58595A5B 5C5D5E5F'   v2
00002010  58595A5B 5C5D5E5F
00002018  E0616263 64656667                       1360          DC    XL16'E0616263 64656667 68696A6B 6C6D6E6F'   v3
00002020  68696A6B 6C6D6E6F
                                                  1361
                                                  1362 *-------------------------------------------------------------------
                                                  1363 *  VML    - Vector Multiply Low
                                                  1364 *-------------------------------------------------------------------
                                                  1365 * Byte
                                                  1366          VRR_C VML,0
00002028                                          1367+         DS    0FD
00002028                        00002028          1368+         USING *,R5              base for test data and test routine
00002028  00002068                                1369+T27      DC    A(X27)            address of test routine
0000202C  001B                                    1370+         DC    H'27'             test number
0000202E  00                                      1371+         DC    X'00'
0000202F  00                                      1372+         DC    HL1'0'            m4
00002030  E5D4D340 40404040                       1373+         DC    CL8'VML'          instruction name
00002038  000020A0                                1374+         DC    A(RE27+16)        address of v2 source
0000203C  000020B0                                1375+         DC    A(RE27+32)        address of v3 source
00002040  00000010                                1376+         DC    A(16)             result length
00002044  00002090                                1377+REA27    DC    A(RE27)           result address
00002048  00000000 00000000                       1378+         DS    FD                gap
00002050  00000000 00000000                       1379+V1O27    DS    XL16              V1 output
00002058  00000000 00000000
00002060  00000000 00000000                       1380+         DS    FD                gap
                                                  1381+*
00002068                                          1382+X27      DS    0F
00002068  E310 5010 0014                00000010  1383+         LGF   R1,V2ADDR         load v2 source
0000206E  E761 0000 0806                00000000  1384+         VL    v22,0(R1)         use v22 to test decoder
00002074  E310 5014 0014                00000014  1385+         LGF   R1,V3ADDR         load v3 source
0000207A  E771 0000 0806                00000000  1386+         VL    v23,0(R1)         use v23 to test decoder
00002080  E766 7000 0EA2                          1387+         VML   V22,V22,V23,0      test instruction (dest is a source)
00002086  E760 5028 080E                00002050  1388+         VST   V22,V1O27          save v1 output
0000208C  07FB                                    1389+         BR    R11               return
00002090                                          1390+RE27     DC    0F                xl16 expected result
00002090                                          1391+         DROP  R5
00002090  01000000 00000071                       1392          DC    XL16'0100000000000071 0000004000000024'   result
00002098  00000040 00000024
000020A0  FF000000 00000019                       1393          DC    XL16'FF00000000000019 00000038000000FA'   v2
000020A8  00000038 000000FA
000020B0  FF000000 00000019                       1394          DC    XL16'FF00000000000019 00000038000000FA'   v3
000020B8  00000038 000000FA
                                                  1395
                                                  1396          VRR_C VML,0
000020C0                                          1397+         DS    0FD
000020C0                        000020C0          1398+         USING *,R5              base for test data and test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000020C0  00002100                                 1399+T28      DC    A(X28)            address of test routine
000020C4  001C                                     1400+         DC    H'28'             test number
000020C6  00                                       1401+         DC    X'00'
000020C7  00                                       1402+         DC    HL1'0'            m4
000020C8  E5D4D340 40404040                        1403+         DC    CL8'VML'          instruction name
000020D0  00002138                                 1404+         DC    A(RE28+16)        address of v2 source
000020D4  00002148                                 1405+         DC    A(RE28+32)        address of v3 source
000020D8  00000010                                 1406+         DC    A(16)             result length
000020DC  00002128                                 1407+REA28    DC    A(RE28)           result address
000020E0  00000000 00000000                        1408+         DS    FD                gap
000020E8  00000000 00000000                        1409+V1O28    DS    XL16              V1 output
000020F0  00000000 00000000
000020F8  00000000 00000000                        1410+         DS    FD                gap
                                                   1411+*
00002100                                           1412+X28      DS    0F
00002100  E310 5010 0014                 00000010  1413+         LGF   R1,V2ADDR         load v2 source
00002106  E761 0000 0806                 00000000  1414+         VL    v22,0(R1)         use v22 to test decoder
0000210C  E310 5014 0014                 00000014  1415+         LGF   R1,V3ADDR         load v3 source
00002112  E771 0000 0806                 00000000  1416+         VL    v23,0(R1)         use v23 to test decoder
00002118  E766 7000 0EA2                           1417+         VML   V22,V22,V23,0      test instruction (dest is a source)
0000211E  E760 5028 080E                 000020E8  1418+         VST   V22,V1O28          save v1 output
00002124  07FB                                     1419+         BR    R11               return
00002128                                           1420+RE28     DC    0F                xl16 expected result
00002128                                           1421+         DROP  R5
00002128  01040910 19243140                        1422          DC    XL16'0104091019243140 51647990A9C4E100'   result
00002130  51647990 A9C4E100
00002138  FF020304 05060708                        1423          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002140  090A0B0C 0D0E0F10
00002148  FF020304 05060708                        1424          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00002150  090A0B0C 0D0E0F10
                                                   1425
                                                   1426          VRR_C VML,0
00002158                                           1427+         DS    0FD
00002158                      00002158             1428+         USING *,R5              base for test data and test routine
00002158  00002198                                 1429+T29      DC    A(X29)            address of test routine
0000215C  001D                                     1430+         DC    H'29'             test number
0000215E  00                                       1431+         DC    X'00'
0000215F  00                                       1432+         DC    HL1'0'            m4
00002160  E5D4D340 40404040                        1433+         DC    CL8'VML'          instruction name
00002168  000021D0                                 1434+         DC    A(RE29+16)        address of v2 source
0000216C  000021E0                                 1435+         DC    A(RE29+32)        address of v3 source
00002170  00000010                                 1436+         DC    A(16)             result length
00002174  000021C0                                 1437+REA29    DC    A(RE29)           result address
00002178  00000000 00000000                        1438+         DS    FD                gap
00002180  00000000 00000000                        1439+V1O29    DS    XL16              V1 output
00002188  00000000 00000000
00002190  00000000 00000000                        1440+         DS    FD                gap
                                                   1441+*
00002198                                           1442+X29      DS    0F
00002198  E310 5010 0014                 00000010  1443+         LGF   R1,V2ADDR         load v2 source
0000219E  E761 0000 0806                 00000000  1444+         VL    v22,0(R1)         use v22 to test decoder
000021A4  E310 5014 0014                 00000014  1445+         LGF   R1,V3ADDR         load v3 source
000021AA  E771 0000 0806                 00000000  1446+         VL    v23,0(R1)         use v23 to test decoder
000021B0  E766 7000 0EA2                           1447+         VML   V22,V22,V23,0      test instruction (dest is a source)
000021B6  E760 5028 080E                 00002180  1448+         VST   V22,V1O29          save v1 output
000021BC  07FB                                     1449+         BR    R11               return
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000021C0                                           1450+RE29     DC    0F                xl16 expected result
000021C0                                           1451+         DROP  R5
000021C0  01020308 0A121520                        1452          DC    XL16'010203080A121520 243237484E626980'   result
000021C8  24323748 4E626980
000021D0  FF020304 05060708                        1453          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000021D8  090A0B0C 0D0E0F10
000021E0  FF010102 02030304                        1454          DC    XL16'FF01010202030304 0405050606070708'   v3
000021E8  04050506 06070708
                                                   1455
                                                   1456          VRR_C VML,0
000021F0                                           1457+         DS    0FD
000021F0                      000021F0             1458+         USING *,R5              base for test data and test routine
000021F0  00002230                                 1459+T30      DC    A(X30)            address of test routine
000021F4  001E                                     1460+         DC    H'30'             test number
000021F6  00                                       1461+         DC    X'00'
000021F7  00                                       1462+         DC    HL1'0'            m4
000021F8  E5D4D340 40404040                        1463+         DC    CL8'VML'          instruction name
00002200  00002268                                 1464+         DC    A(RE30+16)        address of v2 source
00002204  00002278                                 1465+         DC    A(RE30+32)        address of v3 source
00002208  00000010                                 1466+         DC    A(16)             result length
0000220C  00002258                                 1467+REA30    DC    A(RE30)           result address
00002210  00000000 00000000                        1468+         DS    FD                gap
00002218  00000000 00000000                        1469+V1O30    DS    XL16              V1 output
00002220  00000000 00000000
00002228  00000000 00000000                        1470+         DS    FD                gap
                                                   1471+*
00002230                                           1472+X30      DS    0F
00002230  E310 5010 0014                 00000010  1473+         LGF   R1,V2ADDR         load v2 source
00002236  E761 0000 0806                 00000000  1474+         VL    v22,0(R1)         use v22 to test decoder
0000223C  E310 5014 0014                 00000014  1475+         LGF   R1,V3ADDR         load v3 source
00002242  E771 0000 0806                 00000000  1476+         VL    v23,0(R1)         use v23 to test decoder
00002248  E766 7000 0EA2                           1477+         VML   V22,V22,V23,0      test instruction (dest is a source)
0000224E  E760 A018 080E                 00002218  1478+         VST   V22,V1O30          save v1 output
00002254  07FB                                     1479+         BR    R11               return
00002258                                           1480+RE30     DC    0F                xl16 expected result
00002258                                           1481+         DROP  R5
00002258  01000000 00000008                        1482          DC    XL16'0100000000000008 090A0B0C0D0E0F20'   result
00002260  090A0B0C 0D0E0F20
00002268  FF020304 05060708                        1483          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002270  090A0B0C 0D0E0F10
00002278  FF000000 00000001                        1484          DC    XL16'FF00000000000001 0101010101010102'   v3
00002280  01010101 01010102
                                                   1485
                                                   1486 * Halfword
                                                   1487          VRR_C VML,1
00002288                                           1488+         DS    0FD
00002288                      00002288             1489+         USING *,R5              base for test data and test routine
00002288  000022C8                                 1490+T31      DC    A(X31)            address of test routine
0000228C  001F                                     1491+         DC    H'31'             test number
0000228E  00                                       1492+         DC    X'00'
0000228F  01                                       1493+         DC    HL1'1'            m4
00002290  E5D4D340 40404040                        1494+         DC    CL8'VML'          instruction name
00002298  00002300                                 1495+         DC    A(RE31+16)        address of v2 source
0000229C  00002310                                 1496+         DC    A(RE31+32)        address of v3 source
000022A0  00000010                                 1497+         DC    A(16)             result length
000022A4  000022F0                                 1498+REA31    DC    A(RE31)           result address
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000022A8  00000000 00000000                        1499+          DS    FD                gap
000022B0  00000000 00000000                        1500+V1O31     DS    XL16              V1 output
000022B8  00000000 00000000
000022C0  00000000 00000000                        1501+          DS    FD                gap
                                                   1502+*
000022C8                                           1503+X31       DS    0F
000022C8  E310 5010 0014                 00000010  1504+          LGF   R1,V2ADDR         load v2 source
000022CE  E761 0000 0806                 00000000  1505+          VL    v22,0(R1)         use v22 to test decoder
000022D4  E310 5014 0014                 00000014  1506+          LGF   R1,V3ADDR         load v3 source
000022DA  E771 0000 0806                 00000000  1507+          VL    v23,0(R1)         use v23 to test decoder
000022E0  E766 7000 1EA2                           1508+          VML   V22,V22,V23,1      test instruction (dest is a source)
000022E6  E760 5028 080E                 000022B0  1509+          VST   V22,V1O31          save v1 output
000022EC  07FB                                     1510+          BR    R11               return
000022F0                                           1511+RE31      DC    0F                xl16 expected result
000022F0                                           1512+          DROP  R5
000022F0  00010000 00000271                        1513           DC    XL16'0001000000000271 00000C400000CC24'   result
000022F8  00000C40 0000CC24
00002300  FFFF0000 00000019                        1514           DC    XL16'FFFF000000000019 000000380000EEFA'   v2
00002308  00000038 0000EEFA
00002310  FFFF0000 00000019                        1515           DC    XL16'FFFF000000000019 000000380000EEFA'   v3
00002318  00000038 0000EEFA
                                                   1516
                                                   1517           VRR_C VML,1
00002320                                           1518+          DS    0FD
00002320                       00002320            1519+          USING *,R5              base for test data and test routine
00002320  00002360                                 1520+T32       DC    A(X32)            address of test routine
00002324  0020                                     1521+          DC    H'32'             test number
00002326  00                                       1522+          DC    X'00'
00002327  01                                       1523+          DC    HL1'1'            m4
00002328  E5D4D340 40404040                        1524+          DC    CL8'VML'          instruction name
00002330  00002398                                 1525+          DC    A(RE32+16)        address of v2 source
00002334  000023A8                                 1526+          DC    A(RE32+32)        address of v3 source
00002338  00000010                                 1527+          DC    A(16)             result length
0000233C  00002388                                 1528+REA32     DC    A(RE32)           result address
00002340  00000000 00000000                        1529+          DS    FD                gap
00002348  00000000 00000000                        1530+V1O32     DS    XL16              V1 output
00002350  00000000 00000000
00002358  00000000 00000000                        1531+          DS    FD                gap
                                                   1532+*
00002360                                           1533+X32       DS    0F
00002360  E310 5010 0014                 00000010  1534+          LGF   R1,V2ADDR         load v2 source
00002366  E761 0000 0806                 00000000  1535+          VL    v22,0(R1)         use v22 to test decoder
0000236C  E310 5014 0014                 00000014  1536+          LGF   R1,V3ADDR         load v3 source
00002372  E771 0000 0806                 00000000  1537+          VL    v23,0(R1)         use v23 to test decoder
00002378  E766 7000 1EA2                           1538+          VML   V22,V22,V23,1      test instruction (dest is a source)
0000237E  E760 5028 080E                 00002348  1539+          VST   V22,V1O32          save v1 output
00002384  07FB                                     1540+          BR    R11               return
00002388                                           1541+RE32      DC    0F                xl16 expected result
00002388                                           1542+          DROP  R5
00002388  FC041810 3C247040                        1543           DC    XL16'FC0418103C247040 B46408906CC4E100'   result
00002390  B4640890 6CC4E100
00002398  FF020304 05060708                        1544           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000023A0  090A0B0C 0D0E0F10
000023A8  FF020304 05060708                        1545           DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
000023B0  090A0B0C 0D0E0F10
                                                   1546
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   1547          VRR_C VML,1
000023B8                                           1548+         DS    0FD
000023B8                     000023B8              1549+         USING *,R5              base for test data and test routine
000023B8  000023F8                                 1550+T33      DC    A(X33)            address of test routine
000023BC  0021                                     1551+         DC    H'33'             test number
000023BE  00                                       1552+         DC    X'00'
000023BF  01                                       1553+         DC    HL1'1'            m4
000023C0  E5D4D340 40404040                        1554+         DC    CL8'VML'          instruction name
000023C8  00002430                                 1555+         DC    A(RE33+16)        address of v2 source
000023CC  00002440                                 1556+         DC    A(RE33+32)        address of v3 source
000023D0  00000010                                 1557+         DC    A(16)             result length
000023D4  00002420                                 1558+REA33    DC    A(RE33)           result address
000023D8  00000000 00000000                        1559+         DS    FD                gap
000023E0  00000000 00000000                        1560+V1O33    DS    XL16              V1 output
000023E8  00000000 00000000
000023F0  00000000 00000000                        1561+         DS    FD                gap
                                                   1562+*
000023F8                                           1563+X33      DS    0F
000023F8  E310 5010 0014                 00000010  1564+         LGF   R1,V2ADDR         load v2 source
000023FE  E761 0000 0806                 00000000  1565+         VL    v22,0(R1)         use v22 to test decoder
00002404  E310 5014 0014                 00000014  1566+         LGF   R1,V3ADDR         load v3 source
0000240A  E771 0000 0806                 00000000  1567+         VL    v23,0(R1)         use v23 to test decoder
00002410  E766 7000 1EA2                           1568+         VML   V22,V22,V23,1      test instruction (dest is a source)
00002416  E760 5028 080E                 000023E0  1569+         VST   V22,V1O33          save v1 output
0000241C  07FB                                     1570+         BR    R11               return
00002420                                           1571+RE33     DC    0F                xl16 expected result
00002420                                           1572+         DROP  R5
00002420  FD020A08 1B123420                        1573          DC    XL16'FD020A081B123420 55327E48AF62E880'   result
00002428  55327E48 AF62E880
00002430  FF020304 05060708                        1574          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002438  090A0B0C 0D0E0F10
00002440  FF010102 02030304                        1575          DC    XL16'FF01010202030304 0405050606070708'   v3
00002448  04050506 06070708
                                                   1576
                                                   1577          VRR_C VML,1
00002450                                           1578+         DS    0FD
00002450                     00002450              1579+         USING *,R5              base for test data and test routine
00002450  00002490                                 1580+T34      DC    A(X34)            address of test routine
00002454  0022                                     1581+         DC    H'34'             test number
00002456  00                                       1582+         DC    X'00'
00002457  01                                       1583+         DC    HL1'1'            m4
00002458  E5D4D340 40404040                        1584+         DC    CL8'VML'          instruction name
00002460  000024C8                                 1585+         DC    A(RE34+16)        address of v2 source
00002464  000024D8                                 1586+         DC    A(RE34+32)        address of v3 source
00002468  00000010                                 1587+         DC    A(16)             result length
0000246C  000024B8                                 1588+REA34    DC    A(RE34)           result address
00002470  00000000 00000000                        1589+         DS    FD                gap
00002478  00000000 00000000                        1590+V1O34    DS    XL16              V1 output
00002480  00000000 00000000
00002488  00000000 00000000                        1591+         DS    FD                gap
                                                   1592+*
00002490                                           1593+X34      DS    0F
00002490  E310 5010 0014                 00000010  1594+         LGF   R1,V2ADDR         load v2 source
00002496  E761 0000 0806                 00000000  1595+         VL    v22,0(R1)         use v22 to test decoder
0000249C  E310 5014 0014                 00000014  1596+         LGF   R1,V3ADDR         load v3 source
000024A2  E771 0000 0806                 00000000  1597+         VL    v23,0(R1)         use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000024A8  E766 7000 1EA2                           1598+         VML   V22,V22,V23,1      test instruction (dest is a source)
000024AE  E760 5028 080E                 00002478  1599+         VST   V22,V1O34          save v1 output
000024B4  07FB                                     1600+         BR    R11               return
000024B8                                           1601+RE34     DC    0F                xl16 expected result
000024B8                                           1602+         DROP  R5
000024B8  FE000000 00000708                        1603          DC    XL16'FE00000000000708 130A170C1B0E2E20'   result
000024C0  130A170C 1B0E2E20
000024C8  FF020304 05060708                        1604          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
000024D0  090A0B0C 0D0E0F10
000024D8  FF000000 00000001                        1605          DC    XL16'FF00000000000001 0101010101010102'   v3
000024E0  01010101 01010102
                                                   1606
                                                   1607 * Word
                                                   1608          VRR_C VML,2
000024E8                                           1609+         DS    0FD
000024E8                     000024E8              1610+         USING *,R5              base for test data and test routine
000024E8  00002528                                 1611+T35      DC    A(X35)            address of test routine
000024EC  0023                                     1612+         DC    H'35'             test number
000024EE  00                                       1613+         DC    X'00'
000024EF  02                                       1614+         DC    HL1'2'            m4
000024F0  E5D4D340 40404040                        1615+         DC    CL8'VML'          instruction name
000024F8  00002560                                 1616+         DC    A(RE35+16)        address of v2 source
000024FC  00002570                                 1617+         DC    A(RE35+32)        address of v3 source
00002500  00000010                                 1618+         DC    A(16)             result length
00002504  00002550                                 1619+REA35    DC    A(RE35)           result address
00002508  00000000 00000000                        1620+         DS    FD                gap
00002510  00000000 00000000                        1621+V1O35    DS    XL16              V1 output
00002518  00000000 00000000
00002520  00000000 00000000                        1622+         DS    FD                gap
                                                   1623+*
00002528                                           1624+X35      DS    0F
00002528  E310 5010 0014                 00000010  1625+         LGF   R1,V2ADDR         load v2 source
0000252E  E761 0000 0806                 00000000  1626+         VL    v22,0(R1)         use v22 to test decoder
00002534  E310 5014 0014                 00000014  1627+         LGF   R1,V3ADDR         load v3 source
0000253A  E771 0000 0806                 00000000  1628+         VL    v23,0(R1)         use v23 to test decoder
00002540  E766 7000 2EA2                           1629+         VML   V22,V22,V23,2      test instruction (dest is a source)
00002546  E760 5028 080E                 00002510  1630+         VST   V22,V1O35          save v1 output
0000254C  07FB                                     1631+         BR    R11               return
00002550                                           1632+RE35     DC    0F                xl16 expected result
00002550                                           1633+         DROP  R5
00002550  00000001 71000000                        1634          DC    XL16'0000000171000000 00000C400FEDCC24'   result
00002558  00000C40 0FEDCC24
00002560  FFFFFFFF 00019000                        1635          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00002568  00000038 EEEEEEFA
00002570  FFFFFFFF 00019000                        1636          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v3
00002578  00000038 EEEEEEFA
                                                   1637
                                                   1638          VRR_C VML,2
00002580                                           1639+         DS    0FD
00002580                     00002580              1640+         USING *,R5              base for test data and test routine
00002580  000025C0                                 1641+T36      DC    A(X36)            address of test routine
00002584  0024                                     1642+         DC    H'36'             test number
00002586  00                                       1643+         DC    X'00'
00002587  02                                       1644+         DC    HL1'2'            m4
00002588  E5D4D340 40404040                        1645+         DC    CL8'VML'          instruction name
00002590  000025F8                                 1646+         DC    A(RE36+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002594  00002608                                 1647+         DC    A(RE36+32)        address of v3 source
00002598  00000010                                 1648+         DC    A(16)             result length
0000259C  000025E8                                 1649+REA36    DC    A(RE36)           result address
000025A0  00000000 00000000                        1650+         DS    FD                gap
000025A8  00000000 00000000                        1651+V1O36    DS    XL16              V1 output
000025B0  00000000 00000000
000025B8  00000000 00000000                        1652+         DS    FD                gap
                                                   1653+*
000025C0                                           1654+X36      DS    0F
000025C0  E310 5010 0014                00000010   1655+         LGF   R1,V2ADDR         load v2 source
000025C6  E761 0000 0806                00000000   1656+         VL    v22,0(R1)         use v22 to test decoder
000025CC  E310 5014 0014                00000014   1657+         LGF   R1,V3ADDR         load v3 source
000025D2  E771 0000 0806                00000000   1658+         VL    v23,0(R1)         use v23 to test decoder
000025D8  E766 7000 2EA2                           1659+         VML   V22,V22,V23,2      test instruction (dest is a source)
000025DE  E760 5028 080E                000025A8   1660+         VST   V22,V1O36          save v1 output
000025E4  07FB                                     1661+         BR    R11               return
000025E8                                           1662+RE36     DC    0F                xl16 expected result
000025E8                                           1663+         DROP  R5
000025E8  04191810 A4917040                        1664          DC    XL16'04191810A4917040 B56A089046A2E100'   result
000025F0  B56A0890 46A2E100
000025F8  FF020304 05060708                        1665          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002600  090A0B0C 0D0E0F10
00002608  FF020304 05060708                        1666          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v3
00002610  090A0B0C 0D0E0F10
                                                   1667
                                                   1668          VRR_C VML,2
00002618                                           1669+         DS    0FD
00002618                        00002618           1670+         USING *,R5              base for test data and test routine
00002618  00002658                                 1671+T37      DC    A(X37)            address of test routine
0000261C  0025                                     1672+         DC    H'37'             test number
0000261E  00                                       1673+         DC    X'00'
0000261F  02                                       1674+         DC    HL1'2'            m4
00002620  E5D4D340 40404040                        1675+         DC    CL8'VML'          instruction name
00002628  00002690                                 1676+         DC    A(RE37+16)        address of v2 source
0000262C  000026A0                                 1677+         DC    A(RE37+32)        address of v3 source
00002630  00000010                                 1678+         DC    A(16)             result length
00002634  00002680                                 1679+REA37    DC    A(RE37)           result address
00002638  00000000 00000000                        1680+         DS    FD                gap
00002640  00000000 00000000                        1681+V1O37    DS    XL16              V1 output
00002648  00000000 00000000
00002650  00000000 00000000                        1682+         DS    FD                gap
                                                   1683+*
00002658                                           1684+X37      DS    0F
00002658  E310 5010 0014                00000010   1685+         LGF   R1,V2ADDR         load v2 source
0000265E  E761 0000 0806                00000000   1686+         VL    v22,0(R1)         use v22 to test decoder
00002664  E310 5014 0014                00000014   1687+         LGF   R1,V3ADDR         load v3 source
0000266A  E771 0000 0806                00000000   1688+         VL    v23,0(R1)         use v23 to test decoder
00002670  E766 7000 2EA2                           1689+         VML   V22,V22,V23,2      test instruction (dest is a source)
00002676  E760 5028 080E                00002640   1690+         VST   V22,V1O37          save v1 output
0000267C  07FB                                     1691+         BR    R11               return
00002680                                           1692+RE37     DC    0F                xl16 expected result
00002680                                           1693+         DROP  R5
00002680  FF0B0A08 4B453420                        1694          DC    XL16'FF0B0A084B453420 CFAF7E489449E880'   result
00002688  CFAF7E48 9449E880
00002690  FF020304 05060708                        1695          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002698  090A0B0C 0D0E0F10
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000026A0  FF010102 02030304                        1696          DC    XL16'FF01010202030304 0405050606070708'   v3
000026A8  04050506 06070708
                                                   1697
                                                   1698          VRR_C VML,2
000026B0                                           1699+         DS    0FD
000026B0                       000026B0            1700+         USING *,R5              base for test data and test routine
000026B0  000026F0                                 1701+T38      DC    A(X38)            address of test routine
000026B4  0026                                     1702+         DC    H'38'             test number
000026B6  00                                       1703+         DC    X'00'
000026B7  02                                       1704+         DC    HL1'2'            m4
000026B8  E5D4D340 40404040                        1705+         DC    CL8'VML'          instruction name
000026C0  00002728                                 1706+         DC    A(RE38+16)        address of v2 source
000026C4  00002738                                 1707+         DC    A(RE38+32)        address of v3 source
000026C8  00000010                                 1708+         DC    A(16)             result length
000026CC  00002718                                 1709+REA38    DC    A(RE38)           result address
000026D0  00000000 00000000                        1710+         DS    FD                gap
000026D8  00000000 00000000                        1711+V1O38    DS    XL16              V1 output
000026E0  00000000 00000000
000026E8  00000000 00000000                        1712+         DS    FD                gap
                                                   1713+*
000026F0                                           1714+X38      DS    0F
000026F0  E310 5010 0014                 00000010  1715+         LGF   R1,V2ADDR         load v2 source
000026F6  E761 0000 0806                 00000000  1716+         VL    v22,0(R1)         use v22 to test decoder
000026FC  E310 5014 0014                 00000014  1717+         LGF   R1,V3ADDR         load v3 source
00002702  E771 0000 0806                 00000000  1718+         VL    v23,0(R1)         use v23 to test decoder
00002708  E766 7000 2EA2                           1719+         VML   V22,V22,V23,2      test instruction (dest is a source)
0000270E  E760 5028 080E                 000026D8  1720+         VST   V22,V1O38          save v1 output
00002714  07FB                                     1721+         BR    R11               return
00002718                                           1722+RE38     DC    0F                xl16 expected result
00002718                                           1723+         DROP  R5
00002718  FC000000 05060708                        1724          DC    XL16'FC00000005060708 2A21170C473B2E20'   result
00002720  2A21170C 473B2E20
00002728  FF020304 05060708                        1725          DC    XL16'FF02030405060708 090A0B0C0D0E0F10'   v2
00002730  090A0B0C 0D0E0F10
00002738  FF000000 00000001                        1726          DC    XL16'FF00000000000001 0101010101010102'   v3
00002740  01010101 01010102
                                                   1727
                                                   1728 * Doubleword
                                                   1729          VRR_C VML,3
00002748                                           1730+         DS    0FD
00002748                       00002748            1731+         USING *,R5              base for test data and test routine
00002748  00002788                                 1732+T39      DC    A(X39)            address of test routine
0000274C  0027                                     1733+         DC    H'39'             test number
0000274E  00                                       1734+         DC    X'00'
0000274F  03                                       1735+         DC    HL1'3'            m4
00002750  E5D4D340 40404040                        1736+         DC    CL8'VML'          instruction name
00002758  000027C0                                 1737+         DC    A(RE39+16)        address of v2 source
0000275C  000027D0                                 1738+         DC    A(RE39+32)        address of v3 source
00002760  00000010                                 1739+         DC    A(16)             result length
00002764  000027B0                                 1740+REA39    DC    A(RE39)           result address
00002768  00000000 00000000                        1741+         DS    FD                gap
00002770  00000000 00000000                        1742+V1O39    DS    XL16              V1 output
00002778  00000000 00000000
00002780  00000000 00000000                        1743+         DS    FD                gap
                                                   1744+*
00002788                                           1745+X39      DS    0F
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002788  E310 5010 0014                00000010 1746+         LGF   R1,V2ADDR         load v2 source
0000278E  E761 0000 0806                00000000 1747+         VL    v22,0(R1)         use v22 to test decoder
00002794  E310 5014 0014                00000014 1748+         LGF   R1,V3ADDR         load v3 source
0000279A  E771 0000 0806                00000000 1749+         VL    v23,0(R1)         use v23 to test decoder
000027A0  E766 7000 3EA2                         1750+         VML   V22,V22,V23,3      test instruction (dest is a source)
000027A6  E760 5028 080E                00002770 1751+         VST   V22,V1O39          save v1 output
000027AC  07FB                                   1752+         BR    R11               return
000027B0                                         1753+RE39     DC    0F                xl16 expected result
000027B0                                         1754+         DROP  R5
000027B0  FFFCE002 71000000                      1755          DC    XL16'FFFCE00271000000 96789F9F4FEDCC24'   result
000027B8  96789F9F 4FEDCC24
000027C0  FFFFFFFF 00019000                      1756          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000027C8  00000038 EEEEEEFA
000027D0  FFFFFFFF 00019000                      1757          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
000027D8  00000038 0EEEEEFA
                                                 1758
                                                 1759          VRR_C VML,3
000027E0                                         1760+         DS    0FD
000027E0                     000027E0            1761+         USING *,R5              base for test data and test routine
000027E0  00002820                               1762+T40      DC    A(X40)            address of test routine
000027E4  0028                                   1763+         DC    H'40'             test number
000027E6  00                                     1764+         DC    X'00'
000027E7  03                                     1765+         DC    HL1'3'            m4
000027E8  E5D4D340 40404040                      1766+         DC    CL8'VML'          instruction name
000027F0  00002858                               1767+         DC    A(RE40+16)        address of v2 source
000027F4  00002868                               1768+         DC    A(RE40+32)        address of v3 source
000027F8  00000010                               1769+         DC    A(16)             result length
000027FC  00002848                               1770+REA40    DC    A(RE40)           result address
00002800  00000000 00000000                      1771+         DS    FD                gap
00002808  00000000 00000000                      1772+V1O40    DS    XL16              V1 output
00002810  00000000 00000000
00002818  00000000 00000000                      1773+         DS    FD                gap
                                                 1774+*
00002820                                         1775+X40      DS    0F
00002820  E310 5010 0014                00000010 1776+         LGF   R1,V2ADDR         load v2 source
00002826  E761 0000 0806                00000000 1777+         VL    v22,0(R1)         use v22 to test decoder
0000282C  E310 5014 0014                00000014 1778+         LGF   R1,V3ADDR         load v3 source
00002832  E771 0000 0806                00000000 1779+         VL    v23,0(R1)         use v23 to test decoder
00002838  E766 7000 3EA2                         1780+         VML   V22,V22,V23,3      test instruction (dest is a source)
0000283E  E760 5028 080E                00002808 1781+         VST   V22,V1O40          save v1 output
00002844  07FB                                   1782+         BR    R11               return
00002848                                         1783+RE40     DC    0F                xl16 expected result
00002848                                         1784+         DROP  R5
00002848  69B556ED 77F57900                      1785          DC    XL16'69B556ED77F57900 152B55D498D42101'   result
00002850  152B55D4 98D42101
00002858  FF020304 05060750                      1786          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002860  090A0B0C 0D0E0F7F
00002868  01020304 05060750                      1787          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00002870  090A0B78 0D0E0F7F
                                                 1788
                                                 1789          VRR_C VML,3
00002878                                         1790+         DS    0FD
00002878                     00002878            1791+         USING *,R5              base for test data and test routine
00002878  000028B8                               1792+T41      DC    A(X41)            address of test routine
0000287C  0029                                   1793+         DC    H'41'             test number
0000287E  00                                     1794+         DC    X'00'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000287F  03                                       1795+         DC    HL1'3'            m4
00002880  E5D4D340 40404040                        1796+         DC    CL8'VML'          instruction name
00002888  000028F0                                 1797+         DC    A(RE41+16)        address of v2 source
0000288C  00002900                                 1798+         DC    A(RE41+32)        address of v3 source
00002890  00000010                                 1799+         DC    A(16)             result length
00002894  000028E0                                 1800+REA41    DC    A(RE41)           result address
00002898  00000000 00000000                        1801+         DS    FD                gap
000028A0  00000000 00000000                        1802+V1O41    DS    XL16              V1 output
000028A8  00000000 00000000
000028B0  00000000 00000000                        1803+         DS    FD                gap
                                                   1804+*
000028B8                                           1805+X41      DS    0F
000028B8  E310 5010 0014                00000010   1806+         LGF   R1,V2ADDR         load v2 source
000028BE  E761 0000 0806                00000000   1807+         VL    v22,0(R1)         use v22 to test decoder
000028C4  E310 5014 0014                00000014   1808+         LGF   R1,V3ADDR         load v3 source
000028CA  E771 0000 0806                00000000   1809+         VL    v23,0(R1)         use v23 to test decoder
000028D0  E766 7000 3EA2                           1810+         VML   V22,V22,V23,3      test instruction (dest is a source)
000028D6  E760 5028 080E                000028A0   1811+         VST   V22,V1O41          save v1 output
000028DC  07FB                                     1812+         BR    R11               return
000028E0                                           1813+RE41     DC    0F                xl16 expected result
000028E0                                           1814+         DROP  R5
000028E0  06D2FE70 90F71480                        1815          DC    XL16'06D2FE7090F71480 B47CD8D5FF5B4941'   result
000028E8  B47CD8D5 FF5B4941
000028F0  FF020304 05060750                        1816          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000028F8  090A0B0C 0D0E0F7F
00002900  00010102 02030328                        1817          DC    XL16'0001010202030328 0405053C0607073F'   v3
00002908  0405053C 0607073F
                                                   1818
                                                   1819          VRR_C VML,3
00002910                                           1820+         DS    0FD
00002910                        00002910           1821+         USING *,R5              base for test data and test routine
00002910  00002950                                 1822+T42      DC    A(X42)            address of test routine
00002914  002A                                     1823+         DC    H'42'             test number
00002916  00                                       1824+         DC    X'00'
00002917  03                                       1825+         DC    HL1'3'            m4
00002918  E5D4D340 40404040                        1826+         DC    CL8'VML'          instruction name
00002920  00002988                                 1827+         DC    A(RE42+16)        address of v2 source
00002924  00002998                                 1828+         DC    A(RE42+32)        address of v3 source
00002928  00000010                                 1829+         DC    A(16)             result length
0000292C  00002978                                 1830+REA42    DC    A(RE42)           result address
00002930  00000000 00000000                        1831+         DS    FD                gap
00002938  00000000 00000000                        1832+V1O42    DS    XL16              V1 output
00002940  00000000 00000000
00002948  00000000 00000000                        1833+         DS    FD                gap
                                                   1834+*
00002950                                           1835+X42      DS    0F
00002950  E310 5010 0014                00000010   1836+         LGF   R1,V2ADDR         load v2 source
00002956  E761 0000 0806                00000000   1837+         VL    v22,0(R1)         use v22 to test decoder
0000295C  E310 5014 0014                00000014   1838+         LGF   R1,V3ADDR         load v3 source
00002962  E771 0000 0806                00000000   1839+         VL    v23,0(R1)         use v23 to test decoder
00002968  E766 7000 3EA2                           1840+         VML   V22,V22,V23,3      test instruction (dest is a source)
0000296E  E760 5028 080E                00002938   1841+         VST   V22,V1O42          save v1 output
00002974  07FB                                     1842+         BR    R11               return
00002978                                           1843+RE42     DC    0F                xl16 expected result
00002978                                           1844+         DROP  R5
00002978  F6141E28 323C4920                        1845          DC    XL16'F6141E28323C4920 091C345060616771'   result
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002980  091C3450 60616771
00002988  FF020304 05060750                         1846          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002990  090A0B0C 0D0E0F7F
00002998  00000000 0000000A                         1847          DC    XL16'000000000000000A 0101010F0101010F'   v3
000029A0  0101010F 0101010F
                                                    1848
                                                    1849 * Quadword
                                                    1850          VRR_C VML,4
000029A8                                            1851+         DS    0FD
000029A8                      000029A8              1852+         USING *,R5              base for test data and test routine
000029A8  000029E8                                  1853+T43      DC    A(X43)            address of test routine
000029AC  002B                                      1854+         DC    H'43'             test number
000029AE  00                                        1855+         DC    X'00'
000029AF  04                                        1856+         DC    HL1'4'            m4
000029B0  E5D4D340 40404040                         1857+         DC    CL8'VML'          instruction name
000029B8  00002A20                                  1858+         DC    A(RE43+16)        address of v2 source
000029BC  00002A30                                  1859+         DC    A(RE43+32)        address of v3 source
000029C0  00000010                                  1860+         DC    A(16)             result length
000029C4  00002A10                                  1861+REA43    DC    A(RE43)           result address
000029C8  00000000 00000000                         1862+         DS    FD                gap
000029D0  00000000 00000000                         1863+V1O43    DS    XL16              V1 output
000029D8  00000000 00000000
000029E0  00000000 00000000                         1864+         DS    FD                gap
                                                    1865+*
000029E8                                            1866+X43      DS    0F
000029E8  E310 5010 0014                 00000010   1867+         LGF   R1,V2ADDR         load v2 source
000029EE  E761 0000 0806                 00000000   1868+         VL    v22,0(R1)         use v22 to test decoder
000029F4  E310 5014 0014                 00000014   1869+         LGF   R1,V3ADDR         load v3 source
000029FA  E771 0000 0806                 00000000   1870+         VL    v23,0(R1)         use v23 to test decoder
00002A00  E766 7000 4EA2                            1871+         VML   V22,V22,V23,4      test instruction (dest is a source)
00002A06  E760 5028 080E                 000029D0   1872+         VST   V22,V1O43          save v1 output
00002A0C  07FB                                      1873+         BR    R11               return
00002A10                                            1874+RE43     DC    0F                xl16 expected result
00002A10                                            1875+         DROP  R5
00002A10  02D2AEB6 AACD4C77                         1876          DC    XL16'02D2AEB6AACD4C77 96789F9F4FEDCC24'   result
00002A18  96789F9F 4FEDCC24
00002A20  FFFFFFFF 00019000                         1877          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00002A28  00000038 EEEEEEFA
00002A30  FFFFFFFF 00019000                         1878          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00002A38  00000038 0EEEEEFA
                                                    1879
                                                    1880          VRR_C VML,4
00002A40                                            1881+         DS    0FD
00002A40                      00002A40              1882+         USING *,R5              base for test data and test routine
00002A40  00002A80                                  1883+T44      DC    A(X44)            address of test routine
00002A44  002C                                      1884+         DC    H'44'             test number
00002A46  00                                        1885+         DC    X'00'
00002A47  04                                        1886+         DC    HL1'4'            m4
00002A48  E5D4D340 40404040                         1887+         DC    CL8'VML'          instruction name
00002A50  00002AB8                                  1888+         DC    A(RE44+16)        address of v2 source
00002A54  00002AC8                                  1889+         DC    A(RE44+32)        address of v3 source
00002A58  00000010                                  1890+         DC    A(16)             result length
00002A5C  00002AA8                                  1891+REA44    DC    A(RE44)           result address
00002A60  00000000 00000000                         1892+         DS    FD                gap
00002A68  00000000 00000000                         1893+V1O44    DS    XL16              V1 output
00002A70  00000000 00000000
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002A78  00000000 00000000                        1894+         DS    FD                gap
                                                   1895+*
00002A80                                           1896+X44      DS    0F
00002A80  E310 5010 0014                 00000010  1897+         LGF   R1,V2ADDR         load v2 source
00002A86  E761 0000 0806                 00000000  1898+         VL    v22,0(R1)         use v22 to test decoder
00002A8C  E310 5014 0014                 00000014  1899+         LGF   R1,V3ADDR         load v3 source
00002A92  E771 0000 0806                 00000000  1900+         VL    v23,0(R1)         use v23 to test decoder
00002A98  E766 7000 4EA2                           1901+         VML   V22,V22,V23,4      test instruction (dest is a source)
00002A9E  E760 5028 080E                 00002A68  1902+         VST   V22,V1O44          save v1 output
00002AA4  07FB                                     1903+         BR    R11               return
00002AA8                                           1904+RE44     DC    0F                xl16 expected result
00002AA8                                           1905+         DROP  R5
00002AA8  499AFA6A 24295656                        1906          DC    XL16'499AFA6A24295656 152B55D498D42101'   result
00002AB0  152B55D4 98D42101
00002AB8  FF020304 05060750                        1907          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002AC0  090A0B0C 0D0E0F7F
00002AC8  01020304 05060750                        1908          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00002AD0  090A0B78 0D0E0F7F
                                                   1909
                                                   1910          VRR_C VML,4
00002AD8                                           1911+         DS    0FD
00002AD8                     00002AD8              1912+         USING *,R5              base for test data and test routine
00002AD8  00002B18                                 1913+T45      DC    A(X45)            address of test routine
00002ADC  002D                                     1914+         DC    H'45'             test number
00002ADE  00                                       1915+         DC    X'00'
00002ADF  04                                       1916+         DC    HL1'4'            m4
00002AE0  E5D4D340 40404040                        1917+         DC    CL8'VML'          instruction name
00002AE8  00002B50                                 1918+         DC    A(RE45+16)        address of v2 source
00002AEC  00002B60                                 1919+         DC    A(RE45+32)        address of v3 source
00002AF0  00000010                                 1920+         DC    A(16)             result length
00002AF4  00002B40                                 1921+REA45    DC    A(RE45)           result address
00002AF8  00000000 00000000                        1922+         DS    FD                gap
00002B00  00000000 00000000                        1923+V1O45    DS    XL16              V1 output
00002B08  00000000 00000000
00002B10  00000000 00000000                        1924+         DS    FD                gap
                                                   1925+*
00002B18                                           1926+X45      DS    0F
00002B18  E310 5010 0014                 00000010  1927+         LGF   R1,V2ADDR         load v2 source
00002B1E  E761 0000 0806                 00000000  1928+         VL    v22,0(R1)         use v22 to test decoder
00002B24  E310 5014 0014                 00000014  1929+         LGF   R1,V3ADDR         load v3 source
00002B2A  E771 0000 0806                 00000000  1930+         VL    v23,0(R1)         use v23 to test decoder
00002B30  E766 7000 4EA2                           1931+         VML   V22,V22,V23,4      test instruction (dest is a source)
00002B36  E760 5028 080E                 00002B00  1932+         VST   V22,V1O45          save v1 output
00002B3C  07FB                                     1933+         BR    R11               return
00002B40                                           1934+RE45     DC    0F                xl16 expected result
00002B40                                           1935+         DROP  R5
00002B40  A5AC7D14 92F5ADEA                        1936          DC    XL16'A5AC7D1492F5ADEA B47CD8D5FF5B4941'   result
00002B48  B47CD8D5 FF5B4941
00002B50  FF020304 05060750                        1937          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002B58  090A0B0C 0D0E0F7F
00002B60  00010102 02030328                        1938          DC    XL16'0001010202030328 0405053C0607073F'   v3
00002B68  0405053C 0607073F
                                                   1939
                                                   1940          VRR_C VML,4
00002B70                                           1941+         DS    0FD
00002B70                     00002B70              1942+         USING *,R5              base for test data and test routine
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002B70  00002BB0                                 1943+T46      DC    A(X46)            address of test routine
00002B74  002E                                     1944+         DC    H'46'             test number
00002B76  00                                       1945+         DC    X'00'
00002B77  04                                       1946+         DC    HL1'4'            m4
00002B78  E5D4D340 40404040                        1947+         DC    CL8'VML'          instruction name
00002B80  00002BE8                                 1948+         DC    A(RE46+16)        address of v2 source
00002B84  00002BF8                                 1949+         DC    A(RE46+32)        address of v3 source
00002B88  00000010                                 1950+         DC    A(16)             result length
00002B8C  00002BD8                                 1951+REA46    DC    A(RE46)           result address
00002B90  00000000 00000000                        1952+         DS    FD                gap
00002B98  00000000 00000000                        1953+V1O46    DS    XL16              V1 output
00002BA0  00000000 00000000
00002BA8  00000000 00000000                        1954+         DS    FD                gap
                                                   1955+*
00002BB0                                           1956+X46      DS    0F
00002BB0  E310 5010 0014                 00000010  1957+         LGF   R1,V2ADDR         load v2 source
00002BB6  E761 0000 0806                 00000000  1958+         VL    v22,0(R1)         use v22 to test decoder
00002BBC  E310 5014 0014                 00000014  1959+         LGF   R1,V3ADDR         load v3 source
00002BC2  E771 0000 0806                 00000000  1960+         VL    v23,0(R1)         use v23 to test decoder
00002BC8  E766 7000 4EA2                           1961+         VML   V22,V22,V23,4      test instruction (dest is a source)
00002BCE  E760 5028 080E                 00002B98  1962+         VST   V22,V1O46          save v1 output
00002BD4  07FB                                     1963+         BR    R11               return
00002BD8                                           1964+RE46     DC    0F                xl16 expected result
00002BD8                                           1965+         DROP  R5
00002BD8  FD497B95 D40238A4                        1966          DC    XL16'FD497B95D40238A4 091C345060616771'   result
00002BE0  091C3450 60616771
00002BE8  FF020304 05060750                        1967          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002BF0  090A0B0C 0D0E0F7F
00002BF8  00000000 0000000A                        1968          DC    XL16'000000000000000A 0101010F0101010F'   v3
00002C00  0101010F 0101010F
                                                   1969
                                                   1970 *-----------------------------------------------------------------
                                                   1971 *  VMH    - Vector Multiply High
                                                   1972 *-----------------------------------------------------------------
                                                   1973 * Byte
                                                   1974          VRR_C VMH,0
00002C08                                           1975+         DS    0FD
00002C08                         00002C08          1976+         USING *,R5              base for test data and test routine
00002C08  00002C48                                 1977+T47      DC    A(X47)            address of test routine
00002C0C  002F                                     1978+         DC    H'47'             test number
00002C0E  00                                       1979+         DC    X'00'
00002C0F  00                                       1980+         DC    HL1'0'            m4
00002C10  E5D4C840 40404040                        1981+         DC    CL8'VMH'          instruction name
00002C18  00002C80                                 1982+         DC    A(RE47+16)        address of v2 source
00002C1C  00002C90                                 1983+         DC    A(RE47+32)        address of v3 source
00002C20  00000010                                 1984+         DC    A(16)             result length
00002C24  00002C70                                 1985+REA47    DC    A(RE47)           result address
00002C28  00000000 00000000                        1986+         DS    FD                gap
00002C30  00000000 00000000                        1987+V1O47    DS    XL16              V1 output
00002C38  00000000 00000000
00002C40  00000000 00000000                        1988+         DS    FD                gap
                                                   1989+*
00002C48                                           1990+X47      DS    0F
00002C48  E310 5010 0014                 00000010  1991+         LGF   R1,V2ADDR         load v2 source
00002C4E  E761 0000 0806                 00000000  1992+         VL    v22,0(R1)         use v22 to test decoder
00002C54  E310 5014 0014                 00000014  1993+         LGF   R1,V3ADDR         load v3 source
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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002C5A  E771 0000 0806                00000000  1994+         VL    v23,0(R1)         use v23 to test decoder
00002C60  E766 7000 0EA3                          1995+         VMH   V22,V22,V23,0      test instruction (dest is a source)
00002C66  E760 5028 080E                00002C30  1996+         VST   V22,V1O47          save v1 output
00002C6C  07FB                                    1997+         BR    R11               return
00002C70                                          1998+RE47     DC    0F                xl16 expected result
00002C70                                          1999+         DROP  R5
00002C70  00000000 00000002                       2000          DC    XL16'0000000000000002 0000000C00000000'   result
00002C78  0000000C 00000000
00002C80  FF000000 00000019                       2001          DC    XL16'FF00000000000019 00000038000000FA'   v2
00002C88  00000038 000000FA
00002C90  FF000000 00000019                       2002          DC    XL16'FF00000000000019 00000038000000FA'   v3
00002C98  00000038 000000FA
                                                  2003
                                                  2004          VRR_C VMH,0
00002CA0                                          2005+         DS    0FD
00002CA0                      00002CA0            2006+         USING *,R5              base for test data and test routine
00002CA0  00002CE0                                2007+T48      DC    A(X48)            address of test routine
00002CA4  0030                                    2008+         DC    H'48'             test number
00002CA6  00                                      2009+         DC    X'00'
00002CA7  00                                      2010+         DC    HL1'0'            m4
00002CA8  E5D4C840 40404040                       2011+         DC    CL8'VMH'          instruction name
00002CB0  00002D18                                2012+         DC    A(RE48+16)        address of v2 source
00002CB4  00002D28                                2013+         DC    A(RE48+32)        address of v3 source
00002CB8  00000010                                2014+         DC    A(16)             result length
00002CBC  00002D08                                2015+REA48    DC    A(RE48)           result address
00002CC0  00000000 00000000                       2016+         DS    FD                gap
00002CC8  00000000 00000000                       2017+V1O48    DS    XL16              V1 output
00002CD0  00000000 00000000
00002CD8  00000000 00000000                       2018+         DS    FD                gap
                                                  2019+*
00002CE0                                          2020+X48      DS    0F
00002CE0  E310 5010 0014                00000010  2021+         LGF   R1,V2ADDR         load v2 source
00002CE6  E761 0000 0806                00000000  2022+         VL    v22,0(R1)         use v22 to test decoder
00002CEC  E310 5014 0014                00000014  2023+         LGF   R1,V3ADDR         load v3 source
00002CF2  E771 0000 0806                00000000  2024+         VL    v23,0(R1)         use v23 to test decoder
00002CF8  E766 7000 0EA3                          2025+         VMH   V22,V22,V23,0      test instruction (dest is a source)
00002CFE  E760 5028 080E                00002CC8  2026+         VST   V22,V1O48          save v1 output
00002D04  07FB                                    2027+         BR    R11               return
00002D08                                          2028+RE48     DC    0F                xl16 expected result
00002D08                                          2029+         DROP  R5
00002D08  FF000000 00000019                       2030          DC    XL16'FF00000000000019 000000050000003F'   result
00002D10  00000005 0000003F
00002D18  FF020304 05060750                       2031          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002D20  090A0B0C 0D0E0F7F
00002D28  01020304 05060750                       2032          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00002D30  090A0B78 0D0E0F7F
                                                  2033
                                                  2034          VRR_C VMH,0
00002D38                                          2035+         DS    0FD
00002D38                      00002D38            2036+         USING *,R5              base for test data and test routine
00002D38  00002D78                                2037+T49      DC    A(X49)            address of test routine
00002D3C  0031                                    2038+         DC    H'49'             test number
00002D3E  00                                      2039+         DC    X'00'
00002D3F  00                                      2040+         DC    HL1'0'            m4
00002D40  E5D4C840 40404040                       2041+         DC    CL8'VMH'          instruction name
00002D48  00002DB0                                2042+         DC    A(RE49+16)        address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002D4C  00002DC0                                 2043+         DC    A(RE49+32)        address of v3 source
00002D50  00000010                                 2044+         DC    A(16)             result length
00002D54  00002DA0                                 2045+REA49    DC    A(RE49)           result address
00002D58  00000000 00000000                        2046+         DS    FD                gap
00002D60  00000000 00000000                        2047+V1O49    DS    XL16              V1 output
00002D68  00000000 00000000
00002D70  00000000 00000000                        2048+         DS    FD                gap
                                                   2049+*
00002D78                                           2050+X49      DS    0F
00002D78  E310 5010 0014                 00000010  2051+         LGF   R1,V2ADDR         load v2 source
00002D7E  E761 0000 0806                 00000000  2052+         VL    v22,0(R1)         use v22 to test decoder
00002D84  E310 5014 0014                 00000014  2053+         LGF   R1,V3ADDR         load v3 source
00002D8A  E771 0000 0806                 00000000  2054+         VL    v23,0(R1)         use v23 to test decoder
00002D90  E766 7000 0EA3                           2055+         VMH   V22,V22,V23,0      test instruction (dest is a source)
00002D96  E760 5028 080E                 00002D60  2056+         VST   V22,V1O49          save v1 output
00002D9C  07FB                                     2057+         BR    R11               return
00002DA0                                           2058+RE49     DC    0F                xl16 expected result
00002DA0                                           2059+         DROP  R5
00002DA0  00000000 0000000C                        2060          DC    XL16'000000000000000C 000000020000001F'   result
00002DA8  00000002 0000001F
00002DB0  FF020304 05060750                        2061          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002DB8  090A0B0C 0D0E0F7F
00002DC0  00010102 02030328                        2062          DC    XL16'0001010202030328 0405053C0607073F'   v3
00002DC8  0405053C 0607073F
                                                   2063
                                                   2064          VRR_C VMH,0
00002DD0                                           2065+         DS    0FD
00002DD0                      00002DD0             2066+         USING *,R5              base for test data and test routine
00002DD0  00002E10                                 2067+T50      DC    A(X50)            address of test routine
00002DD4  0032                                     2068+         DC    H'50'             test number
00002DD6  00                                       2069+         DC    X'00'
00002DD7  00                                       2070+         DC    HL1'0'            m4
00002DD8  E5D4C840 40404040                        2071+         DC    CL8'VMH'          instruction name
00002DE0  00002E48                                 2072+         DC    A(RE50+16)        address of v2 source
00002DE4  00002E58                                 2073+         DC    A(RE50+32)        address of v3 source
00002DE8  00000010                                 2074+         DC    A(16)             result length
00002DEC  00002E38                                 2075+REA50    DC    A(RE50)           result address
00002DF0  00000000 00000000                        2076+         DS    FD                gap
00002DF8  00000000 00000000                        2077+V1O50    DS    XL16              V1 output
00002E00  00000000 00000000
00002E08  00000000 00000000                        2078+         DS    FD                gap
                                                   2079+*
00002E10                                           2080+X50      DS    0F
00002E10  E310 5010 0014                 00000010  2081+         LGF   R1,V2ADDR         load v2 source
00002E16  E761 0000 0806                 00000000  2082+         VL    v22,0(R1)         use v22 to test decoder
00002E1C  E310 5014 0014                 00000014  2083+         LGF   R1,V3ADDR         load v3 source
00002E22  E771 0000 0806                 00000000  2084+         VL    v23,0(R1)         use v23 to test decoder
00002E28  E766 7000 0EA3                           2085+         VMH   V22,V22,V23,0      test instruction (dest is a source)
00002E2E  E760 5028 080E                 00002DF8  2086+         VST   V22,V1O50          save v1 output
00002E34  07FB                                     2087+         BR    R11               return
00002E38                                           2088+RE50     DC    0F                xl16 expected result
00002E38                                           2089+         DROP  R5
00002E38  00000000 00000003                        2090          DC    XL16'0000000000000003 0000000000000007'   result
00002E40  00000000 00000007
00002E48  FF020304 05060750                        2091          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002E50  090A0B0C 0D0E0F7F
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00002E58  00000000 0000000A                        2092          DC    XL16'000000000000000A 0101010F0101010F'   v3
00002E60  0101010F 0101010F
                                                   2093
                                                   2094 * Halfword
                                                   2095          VRR_C VMH,1
00002E68                                           2096+         DS    0FD
00002E68                      00002E68             2097+         USING *,R5              base for test data and test routine
00002E68  00002EA8                                 2098+T51      DC    A(X51)            address of test routine
00002E6C  0033                                     2099+         DC    H'51'             test number
00002E6E  00                                       2100+         DC    X'00'
00002E6F  01                                       2101+         DC    HL1'1'            m4
00002E70  E5D4C840 40404040                        2102+         DC    CL8'VMH'          instruction name
00002E78  00002EE0                                 2103+         DC    A(RE51+16)        address of v2 source
00002E7C  00002EF0                                 2104+         DC    A(RE51+32)        address of v3 source
00002E80  00000010                                 2105+         DC    A(16)             result length
00002E84  00002ED0                                 2106+REA51    DC    A(RE51)           result address
00002E88  00000000 00000000                        2107+         DS    FD                gap
00002E90  00000000 00000000                        2108+V1O51    DS    XL16              V1 output
00002E98  00000000 00000000
00002EA0  00000000 00000000                        2109+         DS    FD                gap
                                                   2110+*
00002EA8                                           2111+X51      DS    0F
00002EA8  E310 5010 0014                 00000010  2112+         LGF   R1,V2ADDR         load v2 source
00002EAE  E761 0000 0806                 00000000  2113+         VL    v22,0(R1)         use v22 to test decoder
00002EB4  E310 5014 0014                 00000014  2114+         LGF   R1,V3ADDR         load v3 source
00002EBA  E771 0000 0806                 00000000  2115+         VL    v23,0(R1)         use v23 to test decoder
00002EC0  E766 7000 1EA3                           2116+         VMH   V22,V22,V23,1      test instruction (dest is a source)
00002EC6  E760 5028 080E                 00002E90  2117+         VST   V22,V1O51          save v1 output
00002ECC  07FB                                     2118+         BR    R11               return
00002ED0                                           2119+RE51     DC    0F                xl16 expected result
00002ED0                                           2120+         DROP  R5
00002ED0  00000000 00000000                        2121          DC    XL16'0000000000000000 0000000000000121'   result
00002ED8  00000000 00000121
00002EE0  FFFF0000 00000019                        2122          DC    XL16'FFFF000000000019 000000380000EEFA'   v2
00002EE8  00000038 0000EEFA
00002EF0  FFFF0000 00000019                        2123          DC    XL16'FFFF000000000019 000000380000EEFA'   v3
00002EF8  00000038 0000EEFA
                                                   2124
                                                   2125          VRR_C VMH,1
00002F00                                           2126+         DS    0FD
00002F00                      00002F00             2127+         USING *,R5              base for test data and test routine
00002F00  00002F40                                 2128+T52      DC    A(X52)            address of test routine
00002F04  0034                                     2129+         DC    H'52'             test number
00002F06  00                                       2130+         DC    X'00'
00002F07  01                                       2131+         DC    HL1'1'            m4
00002F08  E5D4C840 40404040                        2132+         DC    CL8'VMH'          instruction name
00002F10  00002F78                                 2133+         DC    A(RE52+16)        address of v2 source
00002F14  00002F88                                 2134+         DC    A(RE52+32)        address of v3 source
00002F18  00000010                                 2135+         DC    A(16)             result length
00002F1C  00002F68                                 2136+REA52    DC    A(RE52)           result address
00002F20  00000000 00000000                        2137+         DS    FD                gap
00002F28  00000000 00000000                        2138+V1O52    DS    XL16              V1 output
00002F30  00000000 00000000
00002F38  00000000 00000000                        2139+         DS    FD                gap
                                                   2140+*
00002F40                                           2141+X52      DS    0F
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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00002F40  E310 5010 0014                00000010  2142+         LGF   R1,V2ADDR         load v2 source
00002F46  E761 0000 0806                00000000  2143+         VL    v22,0(R1)         use v22 to test decoder
00002F4C  E310 5014 0014                00000014  2144+         LGF   R1,V3ADDR         load v3 source
00002F52  E771 0000 0806                00000000  2145+         VL    v23,0(R1)         use v23 to test decoder
00002F58  E766 7000 1EA3                          2146+         VMH   V22,V22,V23,1      test instruction (dest is a source)
00002F5E  E760 5028 080E                00002F28  2147+         VST   V22,V1O52          save v1 output
00002F64  07FB                                    2148+         BR    R11               return
00002F68                                          2149+RE52     DC    0F                xl16 expected result
00002F68                                          2150+         DROP  R5
00002F68  FFFF0009 00190035                       2151          DC    XL16'FFFF000900190035 0051007E00AA00F0'   result
00002F70  0051007E 00AA00F0
00002F78  FF020304 05060750                       2152          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00002F80  090A0B0C 0D0E0F7F
00002F88  01020304 05060750                       2153          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00002F90  090A0B78 0D0E0F7F
                                                  2154
                                                  2155          VRR_C VMH,1
00002F98                                          2156+         DS    0FD
00002F98                        00002F98          2157+         USING *,R5              base for test data and test routine
00002F98  00002FD8                                2158+T53      DC    A(X53)            address of test routine
00002F9C  0035                                    2159+         DC    H'53'             test number
00002F9E  00                                      2160+         DC    X'00'
00002F9F  01                                      2161+         DC    HL1'1'            m4
00002FA0  E5D4C840 40404040                       2162+         DC    CL8'VMH'          instruction name
00002FA8  00003010                                2163+         DC    A(RE53+16)        address of v2 source
00002FAC  00003020                                2164+         DC    A(RE53+32)        address of v3 source
00002FB0  00000010                                2165+         DC    A(16)             result length
00002FB4  00003000                                2166+REA53    DC    A(RE53)           result address
00002FB8  00000000 00000000                       2167+         DS    FD                gap
00002FC0  00000000 00000000                       2168+V1O53    DS    XL16              V1 output
00002FC8  00000000 00000000
00002FD0  00000000 00000000                       2169+         DS    FD                gap
                                                  2170+*
00002FD8                                          2171+X53      DS    0F
00002FD8  E310 5010 0014                00000010  2172+         LGF   R1,V2ADDR         load v2 source
00002FDE  E761 0000 0806                00000000  2173+         VL    v22,0(R1)         use v22 to test decoder
00002FE4  E310 5014 0014                00000014  2174+         LGF   R1,V3ADDR         load v3 source
00002FEA  E771 0000 0806                00000000  2175+         VL    v23,0(R1)         use v23 to test decoder
00002FF0  E766 7000 1EA3                          2176+         VMH   V22,V22,V23,1      test instruction (dest is a source)
00002FF6  E760 5028 080E                00002FC0  2177+         VST   V22,V1O53          save v1 output
00002FFC  07FB                                    2178+         BR    R11               return
00003000                                          2179+RE53     DC    0F                xl16 expected result
00003000                                          2180+         DROP  R5
00003000  FFFF0003 000A0017                       2181          DC    XL16'FFFF0003000A0017 00240039004E0070'   result
00003008  00240039 004E0070
00003010  FF020304 05060750                       2182          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003018  090A0B0C 0D0E0F7F
00003020  00010102 02030328                       2183          DC    XL16'0001010202030328 0405053C0607073F'   v3
00003028  0405053C 0607073F
                                                  2184
                                                  2185          VRR_C VMH,1
00003030                                          2186+         DS    0FD
00003030                        00003030          2187+         USING *,R5              base for test data and test routine
00003030  00003070                                2188+T54      DC    A(X54)            address of test routine
00003034  0036                                    2189+         DC    H'54'             test number
00003036  00                                      2190+         DC    X'00'
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003037  01                                       2191+         DC    HL1'1'            m4
00003038  E5D4C840 40404040                        2192+         DC    CL8'VMH'          instruction name
00003040  000030A8                                 2193+         DC    A(RE54+16)        address of v2 source
00003044  000030B8                                 2194+         DC    A(RE54+32)        address of v3 source
00003048  00000010                                 2195+         DC    A(16)             result length
0000304C  00003098                                 2196+REA54    DC    A(RE54)           result address
00003050  00000000 00000000                        2197+         DS    FD                gap
00003058  00000000 00000000                        2198+V1O54    DS    XL16              V1 output
00003060  00000000 00000000
00003068  00000000 00000000                        2199+         DS    FD                gap
                                                   2200+*
00003070                                           2201+X54      DS    0F
00003070  E310 5010 0014                 00000010  2202+         LGF   R1,V2ADDR         load v2 source
00003076  E761 0000 0806                 00000000  2203+         VL    v22,0(R1)         use v22 to test decoder
0000307C  E310 5014 0014                 00000014  2204+         LGF   R1,V3ADDR         load v3 source
00003082  E771 0000 0806                 00000000  2205+         VL    v23,0(R1)         use v23 to test decoder
00003088  E766 7000 1EA3                           2206+         VMH   V22,V22,V23,1      test instruction (dest is a source)
0000308E  E760 5028 080E                 00003058  2207+         VST   V22,V1O54          save v1 output
00003094  07FB                                     2208+         BR    R11               return
00003098                                           2209+RE54     DC    0F                xl16 expected result
00003098                                           2210+         DROP  R5
00003098  00000000 00000000                        2211          DC    XL16'0000000000000000 0009000B000D0010'   result
000030A0  0009000B 000D0010
000030A8  FF020304 05060750                        2212          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000030B0  090A0B0C 0D0E0F7F
000030B8  00000000 0000000A                        2213          DC    XL16'000000000000000A 0101010F0101010F'   v3
000030C0  0101010F 0101010F
                                                   2214
                                                   2215 * Word
                                                   2216          VRR_C VMH,2
000030C8                                           2217+         DS    0FD
000030C8                         000030C8          2218+         USING *,R5              base for test data and test routine
000030C8  00003108                                 2219+T55      DC    A(X55)            address of test routine
000030CC  0037                                     2220+         DC    H'55'             test number
000030CE  00                                       2221+         DC    X'00'
000030CF  02                                       2222+         DC    HL1'2'            m4
000030D0  E5D4C840 40404040                        2223+         DC    CL8'VMH'          instruction name
000030D8  00003140                                 2224+         DC    A(RE55+16)        address of v2 source
000030DC  00003150                                 2225+         DC    A(RE55+32)        address of v3 source
000030E0  00000010                                 2226+         DC    A(16)             result length
000030E4  00003130                                 2227+REA55    DC    A(RE55)           result address
000030E8  00000000 00000000                        2228+         DS    FD                gap
000030F0  00000000 00000000                        2229+V1O55    DS    XL16              V1 output
000030F8  00000000 00000000
00003100  00000000 00000000                        2230+         DS    FD                gap
                                                   2231+*
00003108                                           2232+X55      DS    0F
00003108  E310 5010 0014                 00000010  2233+         LGF   R1,V2ADDR         load v2 source
0000310E  E761 0000 0806                 00000000  2234+         VL    v22,0(R1)         use v22 to test decoder
00003114  E310 5014 0014                 00000014  2235+         LGF   R1,V3ADDR         load v3 source
0000311A  E771 0000 0806                 00000000  2236+         VL    v23,0(R1)         use v23 to test decoder
00003120  E766 7000 2EA3                           2237+         VMH   V22,V22,V23,2      test instruction (dest is a source)
00003126  E760 5028 080E                 000030F0  2238+         VST   V22,V1O55          save v1 output
0000312C  07FB                                     2239+         BR    R11               return
00003130                                           2240+RE55     DC    0F                xl16 expected result
00003130                                           2241+         DROP  R5
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003130  00000000 00000002                        2242          DC    XL16'0000000000000002 00000000FF012345'   result
00003138  00000000 FF012345
00003140  FFFFFFFF 00019000                        2243          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00003148  00000038 EEEEEEFA
00003150  FFFFFFFF 00019000                        2244          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00003158  00000038 0EEEEEFA
                                                   2245
                                                   2246          VRR_C VMH,2
00003160                                           2247+         DS    0FD
00003160                      00003160             2248+         USING *,R5              base for test data and test routine
00003160  000031A0                                 2249+T56      DC    A(X56)            address of test routine
00003164  0038                                     2250+         DC    H'56'             test number
00003166  00                                       2251+         DC    X'00'
00003167  02                                       2252+         DC    HL1'2'            m4
00003168  E5D4C840 40404040                        2253+         DC    CL8'VMH'          instruction name
00003170  000031D8                                 2254+         DC    A(RE56+16)        address of v2 source
00003174  000031E8                                 2255+         DC    A(RE56+32)        address of v3 source
00003178  00000010                                 2256+         DC    A(16)             result length
0000317C  000031C8                                 2257+REA56    DC    A(RE56)           result address
00003180  00000000 00000000                        2258+         DS    FD                gap
00003188  00000000 00000000                        2259+V1O56    DS    XL16              V1 output
00003190  00000000 00000000
00003198  00000000 00000000                        2260+         DS    FD                gap
                                                   2261+*
000031A0                                           2262+X56      DS    0F
000031A0  E310 5010 0014                00000010   2263+         LGF   R1,V2ADDR         load v2 source
000031A6  E761 0000 0806                00000000   2264+         VL    v22,0(R1)         use v22 to test decoder
000031AC  E310 5014 0014                00000014   2265+         LGF   R1,V3ADDR         load v3 source
000031B2  E771 0000 0806                00000000   2266+         VL    v23,0(R1)         use v23 to test decoder
000031B8  E766 7000 2EA3                           2267+         VMH   V22,V22,V23,2      test instruction (dest is a source)
000031BE  E760 5028 080E                00003188   2268+         VST   V22,V1O56          save v1 output
000031C4  07FB                                     2269+         BR    R11               return
000031C8                                           2270+RE56     DC    0F                xl16 expected result
000031C8                                           2271+         DROP  R5
000031C8  FFFF0004 00193C6D                        2272          DC    XL16'FFFF000400193C6D 0051B52F00AA6E58'   result
000031D0  0051B52F 00AA6E58
000031D8  FF020304 05060750                        2273          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000031E0  090A0B0C 0D0E0F7F
000031E8  01020304 05060750                        2274          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
000031F0  090A0B78 0D0E0F7F
                                                   2275
                                                   2276          VRR_C VMH,2
000031F8                                           2277+         DS    0FD
000031F8                      000031F8             2278+         USING *,R5              base for test data and test routine
000031F8  00003238                                 2279+T57      DC    A(X57)            address of test routine
000031FC  0039                                     2280+         DC    H'57'             test number
000031FE  00                                       2281+         DC    X'00'
000031FF  02                                       2282+         DC    HL1'2'            m4
00003200  E5D4C840 40404040                        2283+         DC    CL8'VMH'          instruction name
00003208  00003270                                 2284+         DC    A(RE57+16)        address of v2 source
0000320C  00003280                                 2285+         DC    A(RE57+32)        address of v3 source
00003210  00000010                                 2286+         DC    A(16)             result length
00003214  00003260                                 2287+REA57    DC    A(RE57)           result address
00003218  00000000 00000000                        2288+         DS    FD                gap
00003220  00000000 00000000                        2289+V1O57    DS    XL16              V1 output
00003228  00000000 00000000
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003230  00000000 00000000                        2290+         DS    FD                gap
                                                   2291+*
00003238                                           2292+X57      DS    0F
00003238  E310 5010 0014                 00000010  2293+         LGF   R1,V2ADDR         load v2 source
0000323E  E761 0000 0806                 00000000  2294+         VL    v22,0(R1)         use v22 to test decoder
00003244  E310 5014 0014                 00000014  2295+         LGF   R1,V3ADDR         load v3 source
0000324A  E771 0000 0806                 00000000  2296+         VL    v23,0(R1)         use v23 to test decoder
00003250  E766 7000 2EA3                           2297+         VMH   V22,V22,V23,2      test instruction (dest is a source)
00003256  E760 5028 080E                 00003220  2298+         VST   V22,V1O57          save v1 output
0000325C  07FB                                     2299+         BR    R11               return
00003260                                           2300+RE57     DC    0F                xl16 expected result
00003260                                           2301+         DROP  R5
00003260  FFFFFF01 000A1B30                        2302          DC    XL16'FFFFFF01000A1B30 0024558D004EB01D'   result
00003268  0024558D 004EB01D
00003270  FF020304 05060750                        2303          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003278  090A0B0C 0D0E0F7F
00003280  00010102 02030328                        2304          DC    XL16'0001010202030328 0405053C0607073F'   v3
00003288  0405053C 0607073F
                                                   2305
                                                   2306          VRR_C VMH,2
00003290                                           2307+         DS    0FD
00003290                         00003290          2308+         USING *,R5              base for test data and test routine
00003290  000032D0                                 2309+T58      DC    A(X58)            address of test routine
00003294  003A                                     2310+         DC    H'58'             test number
00003296  00                                       2311+         DC    X'00'
00003297  02                                       2312+         DC    HL1'2'            m4
00003298  E5D4C840 40404040                        2313+         DC    CL8'VMH'          instruction name
000032A0  00003308                                 2314+         DC    A(RE58+16)        address of v2 source
000032A4  00003318                                 2315+         DC    A(RE58+32)        address of v3 source
000032A8  00000010                                 2316+         DC    A(16)             result length
000032AC  000032F8                                 2317+REA58    DC    A(RE58)           result address
000032B0  00000000 00000000                        2318+         DS    FD                gap
000032B8  00000000 00000000                        2319+V1O58    DS    XL16              V1 output
000032C0  00000000 00000000
000032C8  00000000 00000000                        2320+         DS    FD                gap
                                                   2321+*
000032D0                                           2322+X58      DS    0F
000032D0  E310 5010 0014                 00000010  2323+         LGF   R1,V2ADDR         load v2 source
000032D6  E761 0000 0806                 00000000  2324+         VL    v22,0(R1)         use v22 to test decoder
000032DC  E310 5014 0014                 00000014  2325+         LGF   R1,V3ADDR         load v3 source
000032E2  E771 0000 0806                 00000000  2326+         VL    v23,0(R1)         use v23 to test decoder
000032E8  E766 7000 2EA3                           2327+         VMH   V22,V22,V23,2      test instruction (dest is a source)
000032EE  E760 5028 080E                 000032B8  2328+         VST   V22,V1O58          save v1 output
000032F4  07FB                                     2329+         BR    R11               return
000032F8                                           2330+RE58     DC    0F                xl16 expected result
000032F8                                           2331+         DROP  R5
000032F8  00000000 00000000                        2332          DC    XL16'0000000000000000 0009131E000D1B2B'   result
00003300  0009131E 000D1B2B
00003308  FF020304 05060750                        2333          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003310  090A0B0C 0D0E0F7F
00003318  00000000 0000000A                        2334          DC    XL16'000000000000000A 0101010F0101010F'   v3
00003320  0101010F 0101010F
                                                   2335
                                                   2336 * Doubleword
                                                   2337          VRR_C VMH,3
00003328                                           2338+         DS    0FD
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003328                     00003328             2339+         USING *,R5              base for test data and test routine
00003328  00003368                                2340+T59      DC    A(X59)            address of test routine
0000332C  003B                                    2341+         DC    H'59'             test number
0000332E  00                                      2342+         DC    X'00'
0000332F  03                                      2343+         DC    HL1'3'            m4
00003330  E5D4C840 40404040                       2344+         DC    CL8'VMH'          instruction name
00003338  000033A0                                2345+         DC    A(RE59+16)        address of v2 source
0000333C  000033B0                                2346+         DC    A(RE59+32)        address of v3 source
00003340  00000010                                2347+         DC    A(16)             result length
00003344  00003390                                2348+REA59    DC    A(RE59)           result address
00003348  00000000 00000000                       2349+         DS    FD                gap
00003350  00000000 00000000                       2350+V1O59    DS    XL16              V1 output
00003358  00000000 00000000
00003360  00000000 00000000                       2351+         DS    FD                gap
                                                  2352+*
00003368                                          2353+X59      DS    0F
00003368  E310 5010 0014                 00000010 2354+         LGF   R1,V2ADDR         load v2 source
0000336E  E761 0000 0806                 00000000 2355+         VL    v22,0(R1)         use v22 to test decoder
00003374  E310 5014 0014                 00000014 2356+         LGF   R1,V3ADDR         load v3 source
0000337A  E771 0000 0806                 00000000 2357+         VL    v23,0(R1)         use v23 to test decoder
00003380  E766 7000 3EA3                          2358+         VMH   V22,V22,V23,3      test instruction (dest is a source)
00003386  E760 5028 080E                 00003350 2359+         VST   V22,V1O59          save v1 output
0000338C  07FB                                    2360+         BR    R11               return
00003390                                          2361+RE59     DC    0F                xl16 expected result
00003390                                          2362+         DROP  R5
00003390  00000000 00000000                       2363          DC    XL16'0000000000000000 0000000000000C77'   result
00003398  00000000 00000C77
000033A0  FFFFFFFF 00019000                       2364          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000033A8  00000038 EEEEEEFA
000033B0  FFFFFFFF 00019000                       2365          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
000033B8  00000038 0EEEEEFA
                                                  2366
                                                  2367          VRR_C VMH,3
000033C0                                          2368+         DS    0FD
000033C0                     000033C0             2369+         USING *,R5              base for test data and test routine
000033C0  00003400                                2370+T60      DC    A(X60)            address of test routine
000033C4  003C                                    2371+         DC    H'60'             test number
000033C6  00                                      2372+         DC    X'00'
000033C7  03                                      2373+         DC    HL1'3'            m4
000033C8  E5D4C840 40404040                       2374+         DC    CL8'VMH'          instruction name
000033D0  00003438                                2375+         DC    A(RE60+16)        address of v2 source
000033D4  00003448                                2376+         DC    A(RE60+32)        address of v3 source
000033D8  00000010                                2377+         DC    A(16)             result length
000033DC  00003428                                2378+REA60    DC    A(RE60)           result address
000033E0  00000000 00000000                       2379+         DS    FD                gap
000033E8  00000000 00000000                       2380+V1O60    DS    XL16              V1 output
000033F0  00000000 00000000
000033F8  00000000 00000000                       2381+         DS    FD                gap
                                                  2382+*
00003400                                          2383+X60      DS    0F
00003400  E310 5010 0014                 00000010 2384+         LGF   R1,V2ADDR         load v2 source
00003406  E761 0000 0806                 00000000 2385+         VL    v22,0(R1)         use v22 to test decoder
0000340C  E310 5014 0014                 00000014 2386+         LGF   R1,V3ADDR         load v3 source
00003412  E771 0000 0806                 00000000 2387+         VL    v23,0(R1)         use v23 to test decoder
00003418  E766 7000 3EA3                          2388+         VMH   V22,V22,V23,3      test instruction (dest is a source)
0000341E  E760 5028 080E                 000033E8 2389+         VST   V22,V1O60          save v1 output
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003424  07FB                                     2390+         BR    R11                 return
00003428                                           2391+RE60     DC    0F                  xl16 expected result
00003428                                           2392+         DROP  R5
00003428  FFFF0004 0C192C46                        2393          DC    XL16'FFFF00040C192C46 0051B52F8692B4F6'   result
00003430  0051B52F 8692B4F6
00003438  FF020304 05060750                        2394          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003440  090A0B0C 0D0E0F7F
00003448  01020304 05060750                        2395          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00003450  090A0B78 0D0E0F7F
                                                   2396
                                                   2397          VRR_C VMH,3
00003458                                           2398+         DS    0FD
00003458                      00003458             2399+         USING *,R5                base for test data and test routine
00003458  00003498                                 2400+T61      DC    A(X61)              address of test routine
0000345C  003D                                     2401+         DC    H'61'               test number
0000345E  00                                       2402+         DC    X'00'
0000345F  03                                       2403+         DC    HL1'3'              m4
00003460  E5D4C840 40404040                        2404+         DC    CL8'VMH'            instruction name
00003468  000034D0                                 2405+         DC    A(RE61+16)          address of v2 source
0000346C  000034E0                                 2406+         DC    A(RE61+32)          address of v3 source
00003470  00000010                                 2407+         DC    A(16)               result length
00003474  000034C0                                 2408+REA61    DC    A(RE61)             result address
00003478  00000000 00000000                        2409+         DS    FD                  gap
00003480  00000000 00000000                        2410+V1O61    DS    XL16                V1 output
00003488  00000000 00000000
00003490  00000000 00000000                        2411+         DS    FD                  gap
                                                   2412+*
00003498                                           2413+X61      DS    0F
00003498  E310 5010 0014                 00000010  2414+         LGF   R1,V2ADDR           load v2 source
0000349E  E761 0000 0806                 00000000  2415+         VL    v22,0(R1)           use v22 to test decoder
000034A4  E310 5014 0014                 00000014  2416+         LGF   R1,V3ADDR           load v3 source
000034AA  E771 0000 0806                 00000000  2417+         VL    v23,0(R1)           use v23 to test decoder
000034B0  E766 7000 3EA3                           2418+         VMH   V22,V22,V23,3        test instruction (dest is a source)
000034B6  E760 5028 080E                 00003480  2419+         VST   V22,V1O61            save v1 output
000034BC  07FB                                     2420+         BR    R11                 return
000034C0                                           2421+RE61     DC    0F                  xl16 expected result
000034C0                                           2422+         DROP  R5
000034C0  FFFFFF01 0309101C                        2423          DC    XL16'FFFFFF010309101C 0024558DB838C862'   result
000034C8  0024558D B838C862
000034D0  FF020304 05060750                        2424          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000034D8  090A0B0C 0D0E0F7F
000034E0  00010102 02030328                        2425          DC    XL16'0001010202030328 0405053C0607073F'   v3
000034E8  0405053C 0607073F
                                                   2426
                                                   2427          VRR_C VMH,3
000034F0                                           2428+         DS    0FD
000034F0                      000034F0             2429+         USING *,R5                base for test data and test routine
000034F0  00003530                                 2430+T62      DC    A(X62)              address of test routine
000034F4  003E                                     2431+         DC    H'62'               test number
000034F6  00                                       2432+         DC    X'00'
000034F7  03                                       2433+         DC    HL1'3'              m4
000034F8  E5D4C840 40404040                        2434+         DC    CL8'VMH'            instruction name
00003500  00003568                                 2435+         DC    A(RE62+16)          address of v2 source
00003504  00003578                                 2436+         DC    A(RE62+32)          address of v3 source
00003508  00000010                                 2437+         DC    A(16)               result length
0000350C  00003558                                 2438+REA62    DC    A(RE62)             result address
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003510  00000000 00000000                        2439+          DS    FD                 gap
00003518  00000000 00000000                        2440+V1O62     DS    XL16               V1 output
00003520  00000000 00000000
00003528  00000000 00000000                        2441+          DS    FD                 gap
                                                   2442+*
00003530                                           2443+X62       DS    0F
00003530  E310 5010 0014                 00000010  2444+          LGF   R1,V2ADDR          load v2 source
00003536  E761 0000 0806                 00000000  2445+          VL    v22,0(R1)          use v22 to test decoder
0000353C  E310 5014 0014                 00000014  2446+          LGF   R1,V3ADDR          load v3 source
00003542  E771 0000 0806                 00000000  2447+          VL    v23,0(R1)          use v23 to test decoder
00003548  E766 7000 3EA3                           2448+          VMH   V22,V22,V23,3       test instruction (dest is a source)
0000354E  E760 5028 080E                 00003518  2449+          VST   V22,V1O62           save v1 output
00003554  07FB                                     2450+          BR    R11                return
00003558                                           2451+RE62      DC    0F                 xl16 expected result
00003558                                           2452+          DROP  R5
00003558  FFFFFFFF FFFFFFFF                        2453           DC    XL16'FFFFFFFFFFFFFFFF 0009131EA8C3DFFE'   result
00003560  0009131E A8C3DFFE
00003568  FF020304 05060750                        2454           DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00003570  090A0B0C 0D0E0F7F
00003578  00000000 0000000A                        2455           DC    XL16'000000000000000A 0101010F0101010F'   v3
00003580  0101010F 0101010F
                                                   2456
                                                   2457 * Quadword
                                                   2458           VRR_C VMH,4
00003588                                           2459+          DS    0FD
00003588                       00003588            2460+          USING *,R5               base for test data and test routine
00003588  000035C8                                 2461+T63       DC    A(X63)             address of test routine
0000358C  003F                                     2462+          DC    H'63'              test number
0000358E  00                                       2463+          DC    X'00'
0000358F  04                                       2464+          DC    HL1'4'             m4
00003590  E5D4C840 40404040                        2465+          DC    CL8'VMH'           instruction name
00003598  00003600                                 2466+          DC    A(RE63+16)         address of v2 source
0000359C  00003610                                 2467+          DC    A(RE63+32)         address of v3 source
000035A0  00000010                                 2468+          DC    A(16)              result length
000035A4  000035F0                                 2469+REA63     DC    A(RE63)            result address
000035A8  00000000 00000000                        2470+          DS    FD                 gap
000035B0  00000000 00000000                        2471+V1O63     DS    XL16               V1 output
000035B8  00000000 00000000
000035C0  00000000 00000000                        2472+          DS    FD                 gap
                                                   2473+*
000035C8                                           2474+X63       DS    0F
000035C8  E310 5010 0014                 00000010  2475+          LGF   R1,V2ADDR          load v2 source
000035CE  E761 0000 0806                 00000000  2476+          VL    v22,0(R1)          use v22 to test decoder
000035D4  E310 5014 0014                 00000014  2477+          LGF   R1,V3ADDR          load v3 source
000035DA  E771 0000 0806                 00000000  2478+          VL    v23,0(R1)          use v23 to test decoder
000035E0  E766 7000 4EA3                           2479+          VMH   V22,V22,V23,4       test instruction (dest is a source)
000035E6  E760 5028 080E                 000035B0  2480+          VST   V22,V1O63           save v1 output
000035EC  07FB                                     2481+          BR    R11                return
000035F0                                           2482+RE63      DC    0F                 xl16 expected result
000035F0                                           2483+          DROP  R5
000035F0  31000000 00000000                        2484           DC    XL16'31000000 00000000 00000000 00000000'   result
000035F8  00000000 00000000
00003600  70000000 00000000                        2485           DC    XL16'70000000 00000000 00000000 00000000'   v2
00003608  00000000 00000000
00003610  70000000 00000000                        2486           DC    XL16'70000000 00000000 00000000 00000000'   v3
00003618  00000000 00000000
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   2487
                                                   2488          VRR_C VMH,4
00003620                                           2489+         DS    0FD
00003620                     00003620              2490+         USING *,R5              base for test data and test routine
00003620  00003660                                 2491+T64      DC    A(X64)            address of test routine
00003624  0040                                     2492+         DC    H'64'             test number
00003626  00                                       2493+         DC    X'00'
00003627  04                                       2494+         DC    HL1'4'            m4
00003628  E5D4C840 40404040                        2495+         DC    CL8'VMH'          instruction name
00003630  00003698                                 2496+         DC    A(RE64+16)        address of v2 source
00003634  000036A8                                 2497+         DC    A(RE64+32)        address of v3 source
00003638  00000010                                 2498+         DC    A(16)             result length
0000363C  00003688                                 2499+REA64    DC    A(RE64)           result address
00003640  00000000 00000000                        2500+         DS    FD                gap
00003648  00000000 00000000                        2501+V1O64    DS    XL16              V1 output
00003650  00000000 00000000
00003658  00000000 00000000                        2502+         DS    FD                gap
                                                   2503+*
00003660                                           2504+X64      DS    0F
00003660  E310 5010 0014                 00000010  2505+         LGF   R1,V2ADDR         load v2 source
00003666  E761 0000 0806                 00000000  2506+         VL    v22,0(R1)         use v22 to test decoder
0000366C  E310 5014 0014                 00000014  2507+         LGF   R1,V3ADDR         load v3 source
00003672  E771 0000 0806                 00000000  2508+         VL    v23,0(R1)         use v23 to test decoder
00003678  E766 7000 4EA3                           2509+         VMH   V22,V22,V23,4      test instruction (dest is a source)
0000367E  E760 5028 080E                 00003648  2510+         VST   V22,V1O64          save v1 output
00003684  07FB                                     2511+         BR    R11               return
00003688                                           2512+RE64     DC    0F                xl16 expected result
00003688                                           2513+         DROP  R5
00003688  3100D200 E1000000                        2514          DC    XL16'3100D200 E1000000 00000000 00000000'   result
00003690  00000000 00000000
00003698  7000F000 00000000                        2515          DC    XL16'7000F000 00000000 00000000 00000000'   v2
000036A0  00000000 00000000
000036A8  7000F000 00000000                        2516          DC    XL16'7000F000 00000000 00000000 00000000'   v3
000036B0  00000000 00000000
                                                   2517
                                                   2518          VRR_C VMH,4
000036B8                                           2519+         DS    0FD
000036B8                     000036B8              2520+         USING *,R5              base for test data and test routine
000036B8  000036F8                                 2521+T65      DC    A(X65)            address of test routine
000036BC  0041                                     2522+         DC    H'65'             test number
000036BE  00                                       2523+         DC    X'00'
000036BF  04                                       2524+         DC    HL1'4'            m4
000036C0  E5D4C840 40404040                        2525+         DC    CL8'VMH'          instruction name
000036C8  00003730                                 2526+         DC    A(RE65+16)        address of v2 source
000036CC  00003740                                 2527+         DC    A(RE65+32)        address of v3 source
000036D0  00000010                                 2528+         DC    A(16)             result length
000036D4  00003720                                 2529+REA65    DC    A(RE65)           result address
000036D8  00000000 00000000                        2530+         DS    FD                gap
000036E0  00000000 00000000                        2531+V1O65    DS    XL16              V1 output
000036E8  00000000 00000000
000036F0  00000000 00000000                        2532+         DS    FD                gap
                                                   2533+*
000036F8                                           2534+X65      DS    0F
000036F8  E310 5010 0014                 00000010  2535+         LGF   R1,V2ADDR         load v2 source
000036FE  E761 0000 0806                 00000000  2536+         VL    v22,0(R1)         use v22 to test decoder
00003704  E310 5014 0014                 00000014  2537+         LGF   R1,V3ADDR         load v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000370A  E771 0000 0806                00000000  2538+         VL    v23,0(R1)         use v23 to test decoder
00003710  E766 7000 4EA3                          2539+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003716  E760 5028 080E                000036E0  2540+         VST   V22,V1O65          save v1 output
0000371C  07FB                                    2541+         BR    R11               return
00003720                                          2542+RE65     DC    0F                xl16 expected result
00003720                                          2543+         DROP  R5
00003720  3100D201 4A00E100                       2544          DC    XL16'3100D201 4A00E100 00000000 00000000'   result
00003728  00000000 00000000
00003730  7000F000 F0000000                       2545          DC    XL16'7000F000 F0000000 00000000 00000000'   v2
00003738  00000000 00000000
00003740  7000F000 00000000                       2546          DC    XL16'7000F000 00000000 00000000 00000000'   v3
00003748  00000000 00000000
                                                  2547
                                                  2548          VRR_C VMH,4
00003750                                          2549+         DS    0FD
00003750                        00003750          2550+         USING *,R5              base for test data and test routine
00003750  00003790                                2551+T66      DC    A(X66)            address of test routine
00003754  0042                                    2552+         DC    H'66'             test number
00003756  00                                      2553+         DC    X'00'
00003757  04                                      2554+         DC    HL1'4'            m4
00003758  E5D4C840 40404040                       2555+         DC    CL8'VMH'          instruction name
00003760  000037C8                                2556+         DC    A(RE66+16)        address of v2 source
00003764  000037D8                                2557+         DC    A(RE66+32)        address of v3 source
00003768  00000010                                2558+         DC    A(16)             result length
0000376C  000037B8                                2559+REA66    DC    A(RE66)           result address
00003770  00000000 00000000                       2560+         DS    FD                gap
00003778  00000000 00000000                       2561+V1O66    DS    XL16              V1 output
00003780  00000000 00000000
00003788  00000000 00000000                       2562+         DS    FD                gap
                                                  2563+*
00003790                                          2564+X66      DS    0F
00003790  E310 5010 0014                00000010  2565+         LGF   R1,V2ADDR         load v2 source
00003796  E761 0000 0806                00000000  2566+         VL    v22,0(R1)         use v22 to test decoder
0000379C  E310 5014 0014                00000014  2567+         LGF   R1,V3ADDR         load v3 source
000037A2  E771 0000 0806                00000000  2568+         VL    v23,0(R1)         use v23 to test decoder
000037A8  E766 7000 4EA3                          2569+         VMH   V22,V22,V23,4      test instruction (dest is a source)
000037AE  E760 5028 080E                00003778  2570+         VST   V22,V1O66          save v1 output
000037B4  07FB                                    2571+         BR    R11               return
000037B8                                          2572+RE66     DC    0F                xl16 expected result
000037B8                                          2573+         DROP  R5
000037B8  3100D201 4A00E100                       2574          DC    XL16'3100D201 4A00E100 6900E100 E1000000'   result
000037C0  6900E100 E1000000
000037C8  7000F000 F0000000                       2575          DC    XL16'7000F000 F0000000 00000000 00000000'   v2
000037D0  00000000 00000000
000037D8  7000F000 00000000                       2576          DC    XL16'7000F000 00000000 F0000000 00000000'   v3
000037E0  F0000000 00000000
                                                  2577
                                                  2578          VRR_C VMH,4
000037E8                                          2579+         DS    0FD
000037E8                        000037E8          2580+         USING *,R5              base for test data and test routine
000037E8  00003828                                2581+T67      DC    A(X67)            address of test routine
000037EC  0043                                    2582+         DC    H'67'             test number
000037EE  00                                      2583+         DC    X'00'
000037EF  04                                      2584+         DC    HL1'4'            m4
000037F0  E5D4C840 40404040                       2585+         DC    CL8'VMH'          instruction name
000037F8  00003860                                2586+         DC    A(RE67+16)        address of v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000037FC  00003870                                2587+         DC    A(RE67+32)        address of v3 source
00003800  00000010                                2588+         DC    A(16)             result length
00003804  00003850                                2589+REA67    DC    A(RE67)           result address
00003808  00000000 00000000                       2590+         DS    FD                gap
00003810  00000000 00000000                       2591+V1O67    DS    XL16              V1 output
00003818  00000000 00000000
00003820  00000000 00000000                       2592+         DS    FD                gap
                                                  2593+*
00003828                                          2594+X67      DS    0F
00003828  E310 5010 0014                00000010  2595+         LGF   R1,V2ADDR         load v2 source
0000382E  E761 0000 0806                00000000  2596+         VL    v22,0(R1)         use v22 to test decoder
00003834  E310 5014 0014                00000014  2597+         LGF   R1,V3ADDR         load v3 source
0000383A  E771 0000 0806                00000000  2598+         VL    v23,0(R1)         use v23 to test decoder
00003840  E766 7000 4EA3                          2599+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003846  E760 5028 080E                00003810  2600+         VST   V22,V1O67          save v1 output
0000384C  07FB                                    2601+         BR    R11               return
00003850                                          2602+RE67     DC    0F                xl16 expected result
00003850                                          2603+         DROP  R5
00003850  00000000 80000000                       2604          DC    XL16'00000000 80000000 80000000 80000000'   result
00003858  80000000 80000000
00003860  7FFFFFFF FFFFFFFF                       2605          DC    XL16'7FFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF'   v2
00003868  FFFFFFFF FFFFFFFF
00003870  00000001 00000001                       2606          DC    XL16'00000001 00000001 00000001 00000001'   v3
00003878  00000001 00000001
                                                  2607
                                                  2608          VRR_C VMH,4
00003880                                          2609+         DS    0FD
00003880                        00003880          2610+         USING *,R5              base for test data and test routine
00003880  000038C0                                2611+T68      DC    A(X68)            address of test routine
00003884  0044                                    2612+         DC    H'68'             test number
00003886  00                                      2613+         DC    X'00'
00003887  04                                      2614+         DC    HL1'4'            m4
00003888  E5D4C840 40404040                       2615+         DC    CL8'VMH'          instruction name
00003890  000038F8                                2616+         DC    A(RE68+16)        address of v2 source
00003894  00003908                                2617+         DC    A(RE68+32)        address of v3 source
00003898  00000010                                2618+         DC    A(16)             result length
0000389C  000038E8                                2619+REA68    DC    A(RE68)           result address
000038A0  00000000 00000000                       2620+         DS    FD                gap
000038A8  00000000 00000000                       2621+V1O68    DS    XL16              V1 output
000038B0  00000000 00000000
000038B8  00000000 00000000                       2622+         DS    FD                gap
                                                  2623+*
000038C0                                          2624+X68      DS    0F
000038C0  E310 5010 0014                00000010  2625+         LGF   R1,V2ADDR         load v2 source
000038C6  E761 0000 0806                00000000  2626+         VL    v22,0(R1)         use v22 to test decoder
000038CC  E310 5014 0014                00000014  2627+         LGF   R1,V3ADDR         load v3 source
000038D2  E771 0000 0806                00000000  2628+         VL    v23,0(R1)         use v23 to test decoder
000038D8  E766 7000 4EA3                          2629+         VMH   V22,V22,V23,4      test instruction (dest is a source)
000038DE  E760 5028 080E                000038A8  2630+         VST   V22,V1O68          save v1 output
000038E4  07FB                                    2631+         BR    R11               return
000038E8                                          2632+RE68     DC    0F                xl16 expected result
000038E8                                          2633+         DROP  R5
000038E8  3FFFFFFF 00019000                       2634          DC    XL16'3FFFFFFF 00019000 FFFCE03A EFEEEE89'   result
000038F0  FFFCE03A EFEEEE89
000038F8  7FFFFFFF 00019000                       2635          DC    XL16'7FFFFFFF 00019000 00000038 EEEEEEFA'   v2
00003900  00000038 EEEEEEFA
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003908  7FFFFFFF 00019000                        2636          DC    XL16'7FFFFFFF 00019000 00000038 0EEEEEFA'   v3
00003910  00000038 0EEEEEFA
                                                   2637
                                                   2638          VRR_C VMH,4
00003918                                           2639+         DS    0FD
00003918                      00003918             2640+         USING *,R5              base for test data and test routine
00003918  00003958                                 2641+T69      DC    A(X69)            address of test routine
0000391C  0045                                     2642+         DC    H'69'             test number
0000391E  00                                       2643+         DC    X'00'
0000391F  04                                       2644+         DC    HL1'4'            m4
00003920  E5D4C840 40404040                        2645+         DC    CL8'VMH'          instruction name
00003928  00003990                                 2646+         DC    A(RE69+16)        address of v2 source
0000392C  000039A0                                 2647+         DC    A(RE69+32)        address of v3 source
00003930  00000010                                 2648+         DC    A(16)             result length
00003934  00003980                                 2649+REA69    DC    A(RE69)           result address
00003938  00000000 00000000                        2650+         DS    FD                gap
00003940  00000000 00000000                        2651+V1O69    DS    XL16              V1 output
00003948  00000000 00000000
00003950  00000000 00000000                        2652+         DS    FD                gap
                                                   2653+*
00003958                                           2654+X69      DS    0F
00003958  E310 5010 0014                00000010   2655+         LGF   R1,V2ADDR         load v2 source
0000395E  E761 0000 0806                00000000   2656+         VL    v22,0(R1)         use v22 to test decoder
00003964  E310 5014 0014                00000014   2657+         LGF   R1,V3ADDR         load v3 source
0000396A  E771 0000 0806                00000000   2658+         VL    v23,0(R1)         use v23 to test decoder
00003970  E766 7000 4EA3                           2659+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003976  E760 5028 080E                00003940   2660+         VST   V22,V1O69          save v1 output
0000397C  07FB                                     2661+         BR    R11               return
00003980                                           2662+RE69     DC    0F                xl16 expected result
00003980                                           2663+         DROP  R5
00003980  00000000 00000000                        2664          DC    XL16'00000000 00000000 FFFCE002 70FFFF8F'   result
00003988  FFFCE002 70FFFF8F
00003990  FFFFFFFF 00019000                        2665          DC    XL16'FFFFFFFF 00019000 00000038 EEEEEEFA'   v2
00003998  00000038 EEEEEEFA
000039A0  FFFFFFFF 00019000                        2666          DC    XL16'FFFFFFFF 00019000 00000038 0EEEEEFA'   v3
000039A8  00000038 0EEEEEFA
                                                   2667
                                                   2668          VRR_C VMH,4
000039B0                                           2669+         DS    0FD
000039B0                      000039B0             2670+         USING *,R5              base for test data and test routine
000039B0  000039F0                                 2671+T70      DC    A(X70)            address of test routine
000039B4  0046                                     2672+         DC    H'70'             test number
000039B6  00                                       2673+         DC    X'00'
000039B7  04                                       2674+         DC    HL1'4'            m4
000039B8  E5D4C840 40404040                        2675+         DC    CL8'VMH'          instruction name
000039C0  00003A28                                 2676+         DC    A(RE70+16)        address of v2 source
000039C4  00003A38                                 2677+         DC    A(RE70+32)        address of v3 source
000039C8  00000010                                 2678+         DC    A(16)             result length
000039CC  00003A18                                 2679+REA70    DC    A(RE70)           result address
000039D0  00000000 00000000                        2680+         DS    FD                gap
000039D8  00000000 00000000                        2681+V1O70    DS    XL16              V1 output
000039E0  00000000 00000000
000039E8  00000000 00000000                        2682+         DS    FD                gap
                                                   2683+*
000039F0                                           2684+X70      DS    0F
000039F0  E310 5010 0014                00000010   2685+         LGF   R1,V2ADDR         load v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000039F6  E761 0000 0806                00000000  2686+         VL    v22,0(R1)         use v22 to test decoder
000039FC  E310 5014 0014                00000014  2687+         LGF   R1,V3ADDR         load v3 source
00003A02  E771 0000 0806                00000000  2688+         VL    v23,0(R1)         use v23 to test decoder
00003A08  E766 7000 4EA3                          2689+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003A0E  E760 5028 080E                000039D8  2690+         VST   V22,V1O70          save v1 output
00003A14  07FB                                    2691+         BR    R11               return
00003A18                                          2692+RE70     DC    0F                xl16 expected result
00003A18                                          2693+         DROP  R5
00003A18  FFFF0004 0C192C46                       2694          DC    XL16'FFFF0004 0C192C46 69B57B4B BDEC6504'   result
00003A20  69B57B4B BDEC6504
00003A28  FF020304 05060750                       2695          DC    XL16'FF020304 05060750 090A0B0C 0D0E0F7F'   v2
00003A30  090A0B0C 0D0E0F7F
00003A38  01020304 05060750                       2696          DC    XL16'01020304 05060750 090A0B78 0D0E0F7F'   v3
00003A40  090A0B78 0D0E0F7F
                                                  2697
                                                  2698          VRR_C VMH,4
00003A48                                          2699+         DS    0FD
00003A48                        00003A48          2700+         USING *,R5              base for test data and test routine
00003A48  00003A88                                2701+T71      DC    A(X71)            address of test routine
00003A4C  0047                                    2702+         DC    H'71'             test number
00003A4E  00                                      2703+         DC    X'00'
00003A4F  04                                      2704+         DC    HL1'4'            m4
00003A50  E5D4C840 40404040                       2705+         DC    CL8'VMH'          instruction name
00003A58  00003AC0                                2706+         DC    A(RE71+16)        address of v2 source
00003A5C  00003AD0                                2707+         DC    A(RE71+32)        address of v3 source
00003A60  00000010                                2708+         DC    A(16)             result length
00003A64  00003AB0                                2709+REA71    DC    A(RE71)           result address
00003A68  00000000 00000000                       2710+         DS    FD                gap
00003A70  00000000 00000000                       2711+V1O71    DS    XL16              V1 output
00003A78  00000000 00000000
00003A80  00000000 00000000                       2712+         DS    FD                gap
                                                  2713+*
00003A88                                          2714+X71      DS    0F
00003A88  E310 5010 0014                00000010  2715+         LGF   R1,V2ADDR         load v2 source
00003A8E  E761 0000 0806                00000000  2716+         VL    v22,0(R1)         use v22 to test decoder
00003A94  E310 5014 0014                00000014  2717+         LGF   R1,V3ADDR         load v3 source
00003A9A  E771 0000 0806                00000000  2718+         VL    v23,0(R1)         use v23 to test decoder
00003AA0  E766 7000 4EA3                          2719+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003AA6  E760 5028 080E                00003A70  2720+         VST   V22,V1O71          save v1 output
00003AAC  07FB                                    2721+         BR    R11               return
00003AB0                                          2722+RE71     DC    0F                xl16 expected result
00003AB0                                          2723+         DROP  R5
00003AB0  FFFFFF01 0309101C                       2724          DC    XL16'FFFFFF01 0309101C 06CF0A94 A5DE7262'   result
00003AB8  06CF0A94 A5DE7262
00003AC0  FF020304 05060750                       2725          DC    XL16'FF020304 05060750 090A0B0C 0D0E0F7F'   v2
00003AC8  090A0B0C 0D0E0F7F
00003AD0  00010102 02030328                       2726          DC    XL16'00010102 02030328 0405053C 0607073F'   v3
00003AD8  0405053C 0607073F
                                                  2727
                                                  2728          VRR_C VMH,4
00003AE0                                          2729+         DS    0FD
00003AE0                        00003AE0          2730+         USING *,R5              base for test data and test routine
00003AE0  00003B20                                2731+T72      DC    A(X72)            address of test routine
00003AE4  0048                                    2732+         DC    H'72'             test number
00003AE6  00                                      2733+         DC    X'00'
00003AE7  04                                      2734+         DC    HL1'4'            m4
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003AE8  E5D4C840 40404040                        2735+         DC    CL8'VMH'          instruction name
00003AF0  00003B58                                 2736+         DC    A(RE72+16)        address of v2 source
00003AF4  00003B68                                 2737+         DC    A(RE72+32)        address of v3 source
00003AF8  00000010                                 2738+         DC    A(16)             result length
00003AFC  00003B48                                 2739+REA72    DC    A(RE72)           result address
00003B00  00000000 00000000                        2740+         DS    FD                gap
00003B08  00000000 00000000                        2741+V1O72    DS    XL16              V1 output
00003B10  00000000 00000000
00003B18  00000000 00000000                        2742+         DS    FD                gap
                                                   2743+*
00003B20                                           2744+X72      DS    0F
00003B20  E310 5010 0014                 00000010  2745+         LGF   R1,V2ADDR         load v2 source
00003B26  E761 0000 0806                 00000000  2746+         VL    v22,0(R1)         use v22 to test decoder
00003B2C  E310 5014 0014                 00000014  2747+         LGF   R1,V3ADDR         load v3 source
00003B32  E771 0000 0806                 00000000  2748+         VL    v23,0(R1)         use v23 to test decoder
00003B38  E766 7000 4EA3                           2749+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003B3E  E760 5028 080E                 00003B08  2750+         VST   V22,V1O72          save v1 output
00003B44  07FB                                     2751+         BR    R11               return
00003B48                                           2752+RE72     DC    0F                xl16 expected result
00003B48                                           2753+         DROP  R5
00003B48  FFFFFFFF FFFFFFFF                        2754          DC    XL16'FFFFFFFF FFFFFFFF F6131F2C 2C658672'   result
00003B50  F6131F2C 2C658672
00003B58  FF020304 05060750                        2755          DC    XL16'FF020304 05060750 090A0B0C 0D0E0F7F'   v2
00003B60  090A0B0C 0D0E0F7F
00003B68  00000000 0000000A                        2756          DC    XL16'00000000 0000000A 0101010F 0101010F'   v3
00003B70  0101010F 0101010F
                                                   2757
                                                   2758          VRR_C VMH,4
00003B78                                           2759+         DS    0FD
00003B78                         00003B78          2760+         USING *,R5              base for test data and test routine
00003B78  00003BB8                                 2761+T73      DC    A(X73)            address of test routine
00003B7C  0049                                     2762+         DC    H'73'             test number
00003B7E  00                                       2763+         DC    X'00'
00003B7F  04                                       2764+         DC    HL1'4'            m4
00003B80  E5D4C840 40404040                        2765+         DC    CL8'VMH'          instruction name
00003B88  00003BF0                                 2766+         DC    A(RE73+16)        address of v2 source
00003B8C  00003C00                                 2767+         DC    A(RE73+32)        address of v3 source
00003B90  00000010                                 2768+         DC    A(16)             result length
00003B94  00003BE0                                 2769+REA73    DC    A(RE73)           result address
00003B98  00000000 00000000                        2770+         DS    FD                gap
00003BA0  00000000 00000000                        2771+V1O73    DS    XL16              V1 output
00003BA8  00000000 00000000
00003BB0  00000000 00000000                        2772+         DS    FD                gap
                                                   2773+*
00003BB8                                           2774+X73      DS    0F
00003BB8  E310 5010 0014                 00000010  2775+         LGF   R1,V2ADDR         load v2 source
00003BBE  E761 0000 0806                 00000000  2776+         VL    v22,0(R1)         use v22 to test decoder
00003BC4  E310 5014 0014                 00000014  2777+         LGF   R1,V3ADDR         load v3 source
00003BCA  E771 0000 0806                 00000000  2778+         VL    v23,0(R1)         use v23 to test decoder
00003BD0  E766 7000 4EA3                           2779+         VMH   V22,V22,V23,4      test instruction (dest is a source)
00003BD6  E760 5028 080E                 00003BA0  2780+         VST   V22,V1O73          save v1 output
00003BDC  07FB                                     2781+         BR    R11               return
00003BE0                                           2782+RE73     DC    0F                xl16 expected result
00003BE0                                           2783+         DROP  R5
00003BE0  F6146364 177E9A6B                        2784          DC    XL16'F6146364 177E9A6B F4342CDF 4C755AFE'   result
00003BE8  F4342CDF 4C755AFE
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003BF0  50515253 54555657                        2785          DC    XL16'50515253 54555657 58595A5B 5C5D5E5F'   v2
00003BF8  58595A5B 5C5D5E5F
00003C00  E0616263 64656667                        2786          DC    XL16'E0616263 64656667 68696A6B 6C6D6E6F'   v3
00003C08  68696A6B 6C6D6E6F
                                                   2787
                                                   2788 *-----------------------------------------------------------------
                                                   2789 *  VMLE   - Vector Multiply Logical Even
                                                   2790 *-----------------------------------------------------------------
                                                   2791 * Byte
                                                   2792          VRR_C VMLE,0
00003C10                                           2793+         DS    0FD
00003C10                           00003C10        2794+         USING *,R5              base for test data and test routine
00003C10  00003C50                                 2795+T74      DC    A(X74)            address of test routine
00003C14  004A                                     2796+         DC    H'74'             test number
00003C16  00                                       2797+         DC    X'00'
00003C17  00                                       2798+         DC    HL1'0'            m4
00003C18  E5D4D3C5 40404040                        2799+         DC    CL8'VMLE'         instruction name
00003C20  00003C88                                 2800+         DC    A(RE74+16)        address of v2 source
00003C24  00003C98                                 2801+         DC    A(RE74+32)        address of v3 source
00003C28  00000010                                 2802+         DC    A(16)             result length
00003C2C  00003C78                                 2803+REA74    DC    A(RE74)           result address
00003C30  00000000 00000000                        2804+         DS    FD                gap
00003C38  00000000 00000000                        2805+V1O74    DS    XL16              V1 output
00003C40  00000000 00000000
00003C48  00000000 00000000                        2806+         DS    FD                gap
                                                   2807+*
00003C50                                           2808+X74      DS    0F
00003C50  E310 5010 0014                00000010   2809+         LGF   R1,V2ADDR         load v2 source
00003C56  E761 0000 0806                00000000   2810+         VL    v22,0(R1)         use v22 to test decoder
00003C5C  E310 5014 0014                00000014   2811+         LGF   R1,V3ADDR         load v3 source
00003C62  E771 0000 0806                00000000   2812+         VL    v23,0(R1)         use v23 to test decoder
00003C68  E766 7000 0EA4                           2813+         VMLE  V22,V22,V23,0      test instruction (dest is a source)
00003C6E  E760 5028 080E                00003C38   2814+         VST   V22,V1O74          save v1 output
00003C74  07FB                                     2815+         BR    R11               return
00003C78                                           2816+RE74     DC    0F                xl16 expected result
00003C78                                           2817+         DROP  R5
00003C78  FE010000 00000000                        2818          DC    XL16'FE01000000000000 0C40000000000000'   result
00003C80  0C400000 00000000
00003C88  FF000000 00000019                        2819          DC    XL16'FF00000000000019 38000000000000FA'   v2
00003C90  38000000 000000FA
00003C98  FF000000 00000019                        2820          DC    XL16'FF00000000000019 38000000000000FA'   v3
00003CA0  38000000 000000FA
                                                   2821
                                                   2822          VRR_C VMLE,0
00003CA8                                           2823+         DS    0FD
00003CA8                           00003CA8        2824+         USING *,R5              base for test data and test routine
00003CA8  00003CE8                                 2825+T75      DC    A(X75)            address of test routine
00003CAC  004B                                     2826+         DC    H'75'             test number
00003CAE  00                                       2827+         DC    X'00'
00003CAF  00                                       2828+         DC    HL1'0'            m4
00003CB0  E5D4D3C5 40404040                        2829+         DC    CL8'VMLE'         instruction name
00003CB8  00003D20                                 2830+         DC    A(RE75+16)        address of v2 source
00003CBC  00003D30                                 2831+         DC    A(RE75+32)        address of v3 source
00003CC0  00000010                                 2832+         DC    A(16)             result length
00003CC4  00003D10                                 2833+REA75    DC    A(RE75)           result address
00003CC8  00000000 00000000                        2834+         DS    FD                gap
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003CD0  00000000 00000000                        2835+V1O75    DS    XL16              V1 output
00003CD8  00000000 00000000
00003CE0  00000000 00000000                        2836+         DS    FD                gap
                                                   2837+*
00003CE8                                           2838+X75      DS    0F
00003CE8  E310 5010 0014                 00000010  2839+         LGF   R1,V2ADDR         load v2 source
00003CEE  E761 0000 0806                 00000000  2840+         VL    v22,0(R1)         use v22 to test decoder
00003CF4  E310 5014 0014                 00000014  2841+         LGF   R1,V3ADDR         load v3 source
00003CFA  E771 0000 0806                 00000000  2842+         VL    v23,0(R1)         use v23 to test decoder
00003D00  E766 7000 0EA4                           2843+         VMLE  V22,V22,V23,0      test instruction (dest is a source)
00003D06  E760 5028 080E                 00003CD0  2844+         VST   V22,V1O75          save v1 output
00003D0C  07FB                                     2845+         BR    R11               return
00003D10                                           2846+RE75     DC    0F                xl16 expected result
00003D10                                           2847+         DROP  R5
00003D10  FE010009 00190031                        2848          DC    XL16'FE01000900190031 00510079009C00D2'   result
00003D18  00510079 009C00D2
00003D20  FF020304 05060750                        2849          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003D28  090A0B78 0C0D0EFD
00003D30  FF020304 05060750                        2850          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00003D38  090A0B78 0D0E0FFD
                                                   2851
                                                   2852          VRR_C VMLE,0
00003D40                                           2853+         DS    0FD
00003D40                         00003D40          2854+         USING *,R5              base for test data and test routine
00003D40  00003D80                                 2855+T76      DC    A(X76)            address of test routine
00003D44  004C                                     2856+         DC    H'76'             test number
00003D46  00                                       2857+         DC    X'00'
00003D47  00                                       2858+         DC    HL1'0'            m4
00003D48  E5D4D3C5 40404040                        2859+         DC    CL8'VMLE'         instruction name
00003D50  00003DB8                                 2860+         DC    A(RE76+16)        address of v2 source
00003D54  00003DC8                                 2861+         DC    A(RE76+32)        address of v3 source
00003D58  00000010                                 2862+         DC    A(16)             result length
00003D5C  00003DA8                                 2863+REA76    DC    A(RE76)           result address
00003D60  00000000 00000000                        2864+         DS    FD                gap
00003D68  00000000 00000000                        2865+V1O76    DS    XL16              V1 output
00003D70  00000000 00000000
00003D78  00000000 00000000                        2866+         DS    FD                gap
                                                   2867+*
00003D80                                           2868+X76      DS    0F
00003D80  E310 5010 0014                 00000010  2869+         LGF   R1,V2ADDR         load v2 source
00003D86  E761 0000 0806                 00000000  2870+         VL    v22,0(R1)         use v22 to test decoder
00003D8C  E310 5014 0014                 00000014  2871+         LGF   R1,V3ADDR         load v3 source
00003D92  E771 0000 0806                 00000000  2872+         VL    v23,0(R1)         use v23 to test decoder
00003D98  E766 7000 0EA4                           2873+         VMLE  V22,V22,V23,0      test instruction (dest is a source)
00003D9E  E760 5028 080E                 00003D68  2874+         VST   V22,V1O76          save v1 output
00003DA4  07FB                                     2875+         BR    R11               return
00003DA8                                           2876+RE76     DC    0F                xl16 expected result
00003DA8                                           2877+         DROP  R5
00003DA8  FE010003 000A0015                        2878          DC    XL16'FE010003000A0015 0024003700480062'   result
00003DB0  00240037 00480062
00003DB8  FF020304 05060750                        2879          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003DC0  090A0B78 0C0D0EFD
00003DC8  FF010102 02030328                        2880          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00003DD0  0405053C 060707FE
                                                   2881
                                                   2882          VRR_C VMLE,0
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003DD8                                           2883+         DS    0FD
00003DD8                     00003DD8              2884+         USING *,R5              base for test data and test routine
00003DD8  00003E18                                 2885+T77      DC    A(X77)            address of test routine
00003DDC  004D                                     2886+         DC    H'77'             test number
00003DDE  00                                       2887+         DC    X'00'
00003DDF  00                                       2888+         DC    HL1'0'            m4
00003DE0  E5D4D3C5 40404040                        2889+         DC    CL8'VMLE'         instruction name
00003DE8  00003E50                                 2890+         DC    A(RE77+16)        address of v2 source
00003DEC  00003E60                                 2891+         DC    A(RE77+32)        address of v3 source
00003DF0  00000010                                 2892+         DC    A(16)             result length
00003DF4  00003E40                                 2893+REA77    DC    A(RE77)           result address
00003DF8  00000000 00000000                        2894+         DS    FD                gap
00003E00  00000000 00000000                        2895+V1O77    DS    XL16              V1 output
00003E08  00000000 00000000
00003E10  00000000 00000000                        2896+         DS    FD                gap
                                                   2897+*
00003E18                                           2898+X77      DS    0F
00003E18  E310 5010 0014                 00000010  2899+         LGF   R1,V2ADDR         load v2 source
00003E1E  E761 0000 0806                 00000000  2900+         VL    v22,0(R1)         use v22 to test decoder
00003E24  E310 5014 0014                 00000014  2901+         LGF   R1,V3ADDR         load v3 source
00003E2A  E771 0000 0806                 00000000  2902+         VL    v23,0(R1)         use v23 to test decoder
00003E30  E766 7000 0EA4                           2903+         VMLE  V22,V22,V23,0      test instruction (dest is a source)
00003E36  E760 5028 080E                 00003E00  2904+         VST   V22,V1O77          save v1 output
00003E3C  07FB                                     2905+         BR    R11               return
00003E40                                           2906+RE77     DC    0F                xl16 expected result
00003E40                                           2907+         DROP  R5
00003E40  FE010000 00000000                        2908          DC    XL16'FE01000000000000 0009000B000C000E'   result
00003E48  0009000B 000C000E
00003E50  FF020304 05060750                        2909          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003E58  090A0B78 0C0D0EFD
00003E60  FF000000 0000000A                        2910          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00003E68  0101010F 010101FF
                                                   2911
                                                   2912 * Halfword
                                                   2913          VRR_C VMLE,1
00003E70                                           2914+         DS    0FD
00003E70                     00003E70              2915+         USING *,R5              base for test data and test routine
00003E70  00003EB0                                 2916+T78      DC    A(X78)            address of test routine
00003E74  004E                                     2917+         DC    H'78'             test number
00003E76  00                                       2918+         DC    X'00'
00003E77  01                                       2919+         DC    HL1'1'            m4
00003E78  E5D4D3C5 40404040                        2920+         DC    CL8'VMLE'         instruction name
00003E80  00003EE8                                 2921+         DC    A(RE78+16)        address of v2 source
00003E84  00003EF8                                 2922+         DC    A(RE78+32)        address of v3 source
00003E88  00000010                                 2923+         DC    A(16)             result length
00003E8C  00003ED8                                 2924+REA78    DC    A(RE78)           result address
00003E90  00000000 00000000                        2925+         DS    FD                gap
00003E98  00000000 00000000                        2926+V1O78    DS    XL16              V1 output
00003EA0  00000000 00000000
00003EA8  00000000 00000000                        2927+         DS    FD                gap
                                                   2928+*
00003EB0                                           2929+X78      DS    0F
00003EB0  E310 5010 0014                 00000010  2930+         LGF   R1,V2ADDR         load v2 source
00003EB6  E761 0000 0806                 00000000  2931+         VL    v22,0(R1)         use v22 to test decoder
00003EBC  E310 5014 0014                 00000014  2932+         LGF   R1,V3ADDR         load v3 source
00003EC2  E771 0000 0806                 00000000  2933+         VL    v23,0(R1)         use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003EC8  E766 7000 1EA4                           2934+         VMLE  V22,V22,V23,1      test instruction (dest is a source)
00003ECE  E760 5028 080E                 00003E98  2935+         VST   V22,V1O78          save v1 output
00003ED4  07FB                                     2936+         BR    R11               return
00003ED8                                           2937+RE78     DC    0F                xl16 expected result
00003ED8                                           2938+         DROP  R5
00003ED8  FFFE0001 00000000                        2939          DC    XL16'FFFE000100000000 00000C4008000000'   result
00003EE0  00000C40 08000000
00003EE8  FFFF0000 00000019                        2940          DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00003EF0  00380000 1000EEFA
00003EF8  FFFF0000 00000019                        2941          DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00003F00  00380003 8000EEFA
                                                   2942
                                                   2943          VRR_C VMLE,1
00003F08                                           2944+         DS    0FD
00003F08                       00003F08            2945+         USING *,R5              base for test data and test routine
00003F08  00003F48                                 2946+T79      DC    A(X79)            address of test routine
00003F0C  004F                                     2947+         DC    H'79'             test number
00003F0E  00                                       2948+         DC    X'00'
00003F0F  01                                       2949+         DC    HL1'1'            m4
00003F10  E5D4D3C5 40404040                        2950+         DC    CL8'VMLE'         instruction name
00003F18  00003F80                                 2951+         DC    A(RE79+16)        address of v2 source
00003F1C  00003F90                                 2952+         DC    A(RE79+32)        address of v3 source
00003F20  00000010                                 2953+         DC    A(16)             result length
00003F24  00003F70                                 2954+REA79    DC    A(RE79)           result address
00003F28  00000000 00000000                        2955+         DS    FD                gap
00003F30  00000000 00000000                        2956+V1O79    DS    XL16              V1 output
00003F38  00000000 00000000
00003F40  00000000 00000000                        2957+         DS    FD                gap
                                                   2958+*
00003F48                                           2959+X79      DS    0F
00003F48  E310 5010 0014                 00000010  2960+         LGF   R1,V2ADDR         load v2 source
00003F4E  E761 0000 0806                 00000000  2961+         VL    v22,0(R1)         use v22 to test decoder
00003F54  E310 5014 0014                 00000014  2962+         LGF   R1,V3ADDR         load v3 source
00003F5A  E771 0000 0806                 00000000  2963+         VL    v23,0(R1)         use v23 to test decoder
00003F60  E766 7000 1EA4                           2964+         VMLE  V22,V22,V23,1      test instruction (dest is a source)
00003F66  E760 5028 080E                 00003F30  2965+         VST   V22,V1O79          save v1 output
00003F6C  07FB                                     2966+         BR    R11               return
00003F70                                           2967+RE79     DC    0F                xl16 expected result
00003F70                                           2968+         DROP  R5
00003F70  FE04FC04 00193C24                        2969          DC    XL16'FE04FC0400193C24 0051B464009D51B6'   result
00003F78  0051B464 009D51B6
00003F80  FF020304 05060750                        2970          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00003F88  090A0B78 0C0D0EFD
00003F90  FF020304 05060750                        2971          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00003F98  090A0B78 0D0E0FFD
                                                   2972
                                                   2973          VRR_C VMLE,1
00003FA0                                           2974+         DS    0FD
00003FA0                       00003FA0            2975+         USING *,R5              base for test data and test routine
00003FA0  00003FE0                                 2976+T80      DC    A(X80)            address of test routine
00003FA4  0050                                     2977+         DC    H'80'             test number
00003FA6  00                                       2978+         DC    X'00'
00003FA7  01                                       2979+         DC    HL1'1'            m4
00003FA8  E5D4D3C5 40404040                        2980+         DC    CL8'VMLE'         instruction name
00003FB0  00004018                                 2981+         DC    A(RE80+16)        address of v2 source
00003FB4  00004028                                 2982+         DC    A(RE80+32)        address of v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00003FB8  00000010                                 2983+         DC    A(16)              result length
00003FBC  00004008                                 2984+REA80    DC    A(RE80)            result address
00003FC0  00000000 00000000                        2985+         DS    FD                 gap
00003FC8  00000000 00000000                        2986+V1O80    DS    XL16               V1 output
00003FD0  00000000 00000000
00003FD8  00000000 00000000                        2987+         DS    FD                 gap
                                                   2988+*
00003FE0                                           2989+X80      DS    0F
00003FE0  E310 5010 0014                 00000010  2990+         LGF   R1,V2ADDR          load v2 source
00003FE6  E761 0000 0806                 00000000  2991+         VL    v22,0(R1)          use v22 to test decoder
00003FEC  E310 5014 0014                 00000014  2992+         LGF   R1,V3ADDR          load v3 source
00003FF2  E771 0000 0806                 00000000  2993+         VL    v23,0(R1)          use v23 to test decoder
00003FF8  E766 7000 1EA4                           2994+         VMLE  V22,V22,V23,1       test instruction (dest is a source)
00003FFE  E760 5028 080E                 00003FC8  2995+         VST   V22,V1O80           save v1 output
00004004  07FB                                     2996+         BR    R11                return
00004008                                           2997+RE80     DC    0F                 xl16 expected result
00004008                                           2998+         DROP  R5
00004008  FE03FD02 000A1B12                        2999          DC    XL16'FE03FD02000A1B12 002455320048A25B'   result
00004010  00245532 0048A25B
00004018  FF020304 05060750                        3000          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004020  090A0B78 0C0D0EFD
00004028  FF010102 02030328                        3001          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00004030  0405053C 060707FE
                                                   3002
                                                   3003          VRR_C VMLE,1
00004038                                           3004+         DS    0FD
00004038                 00004038                  3005+         USING *,R5               base for test data and test routine
00004038  00004078                                 3006+T81      DC    A(X81)             address of test routine
0000403C  0051                                     3007+         DC    H'81'              test number
0000403E  00                                       3008+         DC    X'00'
0000403F  01                                       3009+         DC    HL1'1'             m4
00004040  E5D4D3C5 40404040                        3010+         DC    CL8'VMLE'          instruction name
00004048  000040B0                                 3011+         DC    A(RE81+16)         address of v2 source
0000404C  000040C0                                 3012+         DC    A(RE81+32)         address of v3 source
00004050  00000010                                 3013+         DC    A(16)              result length
00004054  000040A0                                 3014+REA81    DC    A(RE81)            result address
00004058  00000000 00000000                        3015+         DS    FD                 gap
00004060  00000000 00000000                        3016+V1O81    DS    XL16               V1 output
00004068  00000000 00000000
00004070  00000000 00000000                        3017+         DS    FD                 gap
                                                   3018+*
00004078                                           3019+X81      DS    0F
00004078  E310 5010 0014                 00000010  3020+         LGF   R1,V2ADDR          load v2 source
0000407E  E761 0000 0806                 00000000  3021+         VL    v22,0(R1)          use v22 to test decoder
00004084  E310 5014 0014                 00000014  3022+         LGF   R1,V3ADDR          load v3 source
0000408A  E771 0000 0806                 00000000  3023+         VL    v23,0(R1)          use v23 to test decoder
00004090  E766 7000 1EA4                           3024+         VMLE  V22,V22,V23,1       test instruction (dest is a source)
00004096  E760 5028 080E                 00004060  3025+         VST   V22,V1O81           save v1 output
0000409C  07FB                                     3026+         BR    R11                return
000040A0                                           3027+RE81     DC    0F                 xl16 expected result
000040A0                                           3028+         DROP  R5
000040A0  FE02FE00 00000000                        3029          DC    XL16'FE02FE0000000000 0009130A000C190D'   result
000040A8  0009130A 000C190D
000040B0  FF020304 05060750                        3030          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000040B8  090A0B78 0C0D0EFD
000040C0  FF000000 0000000A                        3031          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000040C8  0101010F 010101FF
                                                  3032
                                                  3033 * Word
                                                  3034          VRR_C VMLE,2
000040D0                                          3035+         DS    0FD
000040D0                      000040D0            3036+         USING *,R5              base for test data and test routine
000040D0  00004110                                3037+T82      DC    A(X82)            address of test routine
000040D4  0052                                    3038+         DC    H'82'             test number
000040D6  00                                      3039+         DC    X'00'
000040D7  02                                      3040+         DC    HL1'2'            m4
000040D8  E5D4D3C5 40404040                       3041+         DC    CL8'VMLE'         instruction name
000040E0  00004148                                3042+         DC    A(RE82+16)        address of v2 source
000040E4  00004158                                3043+         DC    A(RE82+32)        address of v3 source
000040E8  00000010                                3044+         DC    A(16)             result length
000040EC  00004138                                3045+REA82    DC    A(RE82)           result address
000040F0  00000000 00000000                       3046+         DS    FD                gap
000040F8  00000000 00000000                       3047+V1O82    DS    XL16              V1 output
00004100  00000000 00000000
00004108  00000000 00000000                       3048+         DS    FD                gap
                                                  3049+*
00004110                                          3050+X82      DS    0F
00004110  E310 5010 0014                 00000010 3051+         LGF   R1,V2ADDR         load v2 source
00004116  E761 0000 0806                 00000000 3052+         VL    v22,0(R1)         use v22 to test decoder
0000411C  E310 5014 0014                 00000014 3053+         LGF   R1,V3ADDR         load v3 source
00004122  E771 0000 0806                 00000000 3054+         VL    v23,0(R1)         use v23 to test decoder
00004128  E766 7000 2EA4                          3055+         VMLE  V22,V22,V23,2      test instruction (dest is a source)
0000412E  E760 5028 080E                 000040F8 3056+         VST   V22,V1O82          save v1 output
00004134  07FB                                    3057+         BR    R11               return
00004138                                          3058+RE82     DC    0F                xl16 expected result
00004138                                          3059+         DROP  R5
00004138  FFFFFFFE 00000001                       3060          DC    XL16'FFFFFFFE00000001 0000000000000C40'   result
00004140  00000000 00000C40
00004148  FFFFFFFF 00019000                       3061          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00004150  00000038 EEEEEEFA
00004158  FFFFFFFF 00019000                       3062          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00004160  00000038 0EEEEEFA
                                                  3063
                                                  3064          VRR_C VMLE,2
00004168                                          3065+         DS    0FD
00004168                      00004168            3066+         USING *,R5              base for test data and test routine
00004168  000041A8                                3067+T83      DC    A(X83)            address of test routine
0000416C  0053                                    3068+         DC    H'83'             test number
0000416E  00                                      3069+         DC    X'00'
0000416F  02                                      3070+         DC    HL1'2'            m4
00004170  E5D4D3C5 40404040                       3071+         DC    CL8'VMLE'         instruction name
00004178  000041E0                                3072+         DC    A(RE83+16)        address of v2 source
0000417C  000041F0                                3073+         DC    A(RE83+32)        address of v3 source
00004180  00000010                                3074+         DC    A(16)             result length
00004184  000041D0                                3075+REA83    DC    A(RE83)           result address
00004188  00000000 00000000                       3076+         DS    FD                gap
00004190  00000000 00000000                       3077+V1O83    DS    XL16              V1 output
00004198  00000000 00000000
000041A0  00000000 00000000                       3078+         DS    FD                gap
                                                  3079+*
000041A8                                          3080+X83      DS    0F
000041A8  E310 5010 0014                 00000010 3081+         LGF   R1,V2ADDR         load v2 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

000041AE  E761 0000 0806                00000000  3082+         VL    v22,0(R1)         use v22 to test decoder
000041B4  E310 5014 0014                00000014  3083+         LGF   R1,V3ADDR         load v3 source
000041BA  E771 0000 0806                00000000  3084+         VL    v23,0(R1)         use v23 to test decoder
000041C0  E766 7000 2EA4                          3085+         VMLE  V22,V22,V23,2      test instruction (dest is a source)
000041C6  E760 5028 080E                00004190  3086+         VST   V22,V1O83          save v1 output
000041CC  07FB                                    3087+         BR    R11               return
000041D0                                          3088+RE83     DC    0F                xl16 expected result
000041D0                                          3089+         DROP  R5
000041D0  FE050206 04191810                       3090          DC    XL16'FE05020604191810 0051B52F85A6B1A0'   result
000041D8  0051B52F 85A6B1A0
000041E0  FF020304 05060750                       3091          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000041E8  090A0B0C 0D0E0F7F
000041F0  FF020304 05060750                       3092          DC    XL16'FF02030405060750 090A0B780D0E0F7F'   v3
000041F8  090A0B78 0D0E0F7F
                                                  3093
                                                  3094          VRR_C VMLE,2
00004200                                          3095+         DS    0FD
00004200                        00004200          3096+         USING *,R5              base for test data and test routine
00004200  00004240                                3097+T84      DC    A(X84)            address of test routine
00004204  0054                                    3098+         DC    H'84'             test number
00004206  00                                      3099+         DC    X'00'
00004207  02                                      3100+         DC    HL1'2'            m4
00004208  E5D4D3C5 40404040                       3101+         DC    CL8'VMLE'         instruction name
00004210  00004278                                3102+         DC    A(RE84+16)        address of v2 source
00004214  00004288                                3103+         DC    A(RE84+32)        address of v3 source
00004218  00000010                                3104+         DC    A(16)             result length
0000421C  00004268                                3105+REA84    DC    A(RE84)           result address
00004220  00000000 00000000                       3106+         DS    FD                gap
00004228  00000000 00000000                       3107+V1O84    DS    XL16              V1 output
00004230  00000000 00000000
00004238  00000000 00000000                       3108+         DS    FD                gap
                                                  3109+*
00004240                                          3110+X84      DS    0F
00004240  E310 5010 0014                00000010  3111+         LGF   R1,V2ADDR         load v2 source
00004246  E761 0000 0806                00000000  3112+         VL    v22,0(R1)         use v22 to test decoder
0000424C  E310 5014 0014                00000014  3113+         LGF   R1,V3ADDR         load v3 source
00004252  E771 0000 0806                00000000  3114+         VL    v23,0(R1)         use v23 to test decoder
00004258  E766 7000 2EA4                          3115+         VMLE  V22,V22,V23,2      test instruction (dest is a source)
0000425E  E760 5028 080E                00004228  3116+         VST   V22,V1O84          save v1 output
00004264  07FB                                    3117+         BR    R11               return
00004268                                          3118+RE84     DC    0F                xl16 expected result
00004268                                          3119+         DROP  R5
00004268  FE040103 FF0B0A08                       3120          DC    XL16'FE040103FF0B0A08 0024558DB7CDD2D0'   result
00004270  0024558D B7CDD2D0
00004278  FF020304 05060750                       3121          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004280  090A0B0C 0D0E0F7F
00004288  FF010102 02030328                       3122          DC    XL16'FF01010202030328 0405053C0607073F'   v3
00004290  0405053C 0607073F
                                                  3123
                                                  3124          VRR_C VMLE,2
00004298                                          3125+         DS    0FD
00004298                        00004298          3126+         USING *,R5              base for test data and test routine
00004298  000042D8                                3127+T85      DC    A(X85)            address of test routine
0000429C  0055                                    3128+         DC    H'85'             test number
0000429E  00                                      3129+         DC    X'00'
0000429F  02                                      3130+         DC    HL1'2'            m4
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000042A0  E5D4D3C5 40404040                        3131+         DC    CL8'VMLE'         instruction name
000042A8  00004310                                 3132+         DC    A(RE85+16)        address of v2 source
000042AC  00004320                                 3133+         DC    A(RE85+32)        address of v3 source
000042B0  00000010                                 3134+         DC    A(16)             result length
000042B4  00004300                                 3135+REA85    DC    A(RE85)           result address
000042B8  00000000 00000000                        3136+         DS    FD                gap
000042C0  00000000 00000000                        3137+V1O85    DS    XL16              V1 output
000042C8  00000000 00000000
000042D0  00000000 00000000                        3138+         DS    FD                gap
                                                   3139+*
000042D8                                           3140+X85      DS    0F
000042D8  E310 5010 0014                 00000010  3141+         LGF   R1,V2ADDR         load v2 source
000042DE  E761 0000 0806                 00000000  3142+         VL    v22,0(R1)         use v22 to test decoder
000042E4  E310 5014 0014                 00000014  3143+         LGF   R1,V3ADDR         load v3 source
000042EA  E771 0000 0806                 00000000  3144+         VL    v23,0(R1)         use v23 to test decoder
000042F0  E766 7000 2EA4                           3145+         VMLE  V22,V22,V23,2      test instruction (dest is a source)
000042F6  E760 5028 080E                 000042C0  3146+         VST   V22,V1O85          save v1 output
000042FC  07FB                                     3147+         BR    R11               return
00004300                                           3148+RE85     DC    0F                xl16 expected result
00004300                                           3149+         DROP  R5
00004300  FE030100 FC000000                        3150          DC    XL16'FE030100FC000000 0009131EA8ADB1B4'   result
00004308  0009131E A8ADB1B4
00004310  FF020304 05060750                        3151          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004318  090A0B0C 0D0E0F7F
00004320  FF000000 0000000A                        3152          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
00004328  0101010F 0101010F
                                                   3153
                                                   3154 * Doubleword
                                                   3155          VRR_C VMLE,3
00004330                                           3156+         DS    0FD
00004330                         00004330          3157+         USING *,R5              base for test data and test routine
00004330  00004370                                 3158+T86      DC    A(X86)            address of test routine
00004334  0056                                     3159+         DC    H'86'             test number
00004336  00                                       3160+         DC    X'00'
00004337  03                                       3161+         DC    HL1'3'            m4
00004338  E5D4D3C5 40404040                        3162+         DC    CL8'VMLE'         instruction name
00004340  000043A8                                 3163+         DC    A(RE86+16)        address of v2 source
00004344  000043B8                                 3164+         DC    A(RE86+32)        address of v3 source
00004348  00000010                                 3165+         DC    A(16)             result length
0000434C  00004398                                 3166+REA86    DC    A(RE86)           result address
00004350  00000000 00000000                        3167+         DS    FD                gap
00004358  00000000 00000000                        3168+V1O86    DS    XL16              V1 output
00004360  00000000 00000000
00004368  00000000 00000000                        3169+         DS    FD                gap
                                                   3170+*
00004370                                           3171+X86      DS    0F
00004370  E310 5010 0014                 00000010  3172+         LGF   R1,V2ADDR         load v2 source
00004376  E761 0000 0806                 00000000  3173+         VL    v22,0(R1)         use v22 to test decoder
0000437C  E310 5014 0014                 00000014  3174+         LGF   R1,V3ADDR         load v3 source
00004382  E771 0000 0806                 00000000  3175+         VL    v23,0(R1)         use v23 to test decoder
00004388  E766 7000 3EA4                           3176+         VMLE  V22,V22,V23,3      test instruction (dest is a source)
0000438E  E760 5028 080E                 00004358  3177+         VST   V22,V1O86          save v1 output
00004394  07FB                                     3178+         BR    R11               return
00004398                                           3179+RE86     DC    0F                xl16 expected result
00004398                                           3180+         DROP  R5
00004398  FFFFFFFE 00032000                        3181          DC    XL16'FFFFFFFE00032000 FFFCE00271000000'   result
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000043A0  FFFCE002 71000000
000043A8  FFFFFFFF 00019000                         3182          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000043B0  00000038 EEEEEEFA
000043B8  FFFFFFFF 00019000                         3183          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
000043C0  00000038 0EEEEEFA
                                                    3184
                                                    3185          VRR_C VMLE,3
000043C8                                            3186+         DS    0FD
000043C8                      000043C8              3187+         USING *,R5              base for test data and test routine
000043C8  00004408                                  3188+T87      DC    A(X87)            address of test routine
000043CC  0057                                      3189+         DC    H'87'             test number
000043CE  00                                        3190+         DC    X'00'
000043CF  03                                        3191+         DC    HL1'3'            m4
000043D0  E5D4D3C5 40404040                         3192+         DC    CL8'VMLE'         instruction name
000043D8  00004440                                  3193+         DC    A(RE87+16)        address of v2 source
000043DC  00004450                                  3194+         DC    A(RE87+32)        address of v3 source
000043E0  00000010                                  3195+         DC    A(16)             result length
000043E4  00004430                                  3196+REA87    DC    A(RE87)           result address
000043E8  00000000 00000000                         3197+         DS    FD                gap
000043F0  00000000 00000000                         3198+V1O87    DS    XL16              V1 output
000043F8  00000000 00000000
00004400  00000000 00000000                         3199+         DS    FD                gap
                                                    3200+*
00004408                                            3201+X87      DS    0F
00004408  E310 5010 0014                00000010    3202+         LGF   R1,V2ADDR         load v2 source
0000440E  E761 0000 0806                00000000    3203+         VL    v22,0(R1)         use v22 to test decoder
00004414  E310 5014 0014                00000014    3204+         LGF   R1,V3ADDR         load v3 source
0000441A  E771 0000 0806                00000000    3205+         VL    v23,0(R1)         use v23 to test decoder
00004420  E766 7000 3EA4                            3206+         VMLE  V22,V22,V23,3      test instruction (dest is a source)
00004426  E760 5028 080E                000043F0    3207+         VST   V22,V1O87          save v1 output
0000442C  07FB                                      3208+         BR    R11               return
00004430                                            3209+RE87     DC    0F                xl16 expected result
00004430                                            3210+         DROP  R5
00004430  01010308 111F3396                         3211          DC    XL16'01010308111F3396 69B556ED77F57900'   result
00004438  69B556ED 77F57900
00004440  FF020304 05060750                         3212          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004448  090A0B0C 0D0E0F7F
00004450  01020304 05060750                         3213          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00004458  090A0B78 0D0E0F7F
                                                    3214
                                                    3215          VRR_C VMLE,3
00004460                                            3216+         DS    0FD
00004460                      00004460              3217+         USING *,R5              base for test data and test routine
00004460  000044A0                                  3218+T88      DC    A(X88)            address of test routine
00004464  0058                                      3219+         DC    H'88'             test number
00004466  00                                        3220+         DC    X'00'
00004467  03                                        3221+         DC    HL1'3'            m4
00004468  E5D4D3C5 40404040                         3222+         DC    CL8'VMLE'         instruction name
00004470  000044D8                                  3223+         DC    A(RE88+16)        address of v2 source
00004474  000044E8                                  3224+         DC    A(RE88+32)        address of v3 source
00004478  00000010                                  3225+         DC    A(16)             result length
0000447C  000044C8                                  3226+REA88    DC    A(RE88)           result address
00004480  00000000 00000000                         3227+         DS    FD                gap
00004488  00000000 00000000                         3228+V1O88    DS    XL16              V1 output
00004490  00000000 00000000
00004498  00000000 00000000                         3229+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3230+*
000044A0                                           3231+X88      DS    0F
000044A0  E310 5010 0014                 00000010  3232+         LGF   R1,V2ADDR         load v2 source
000044A6  E761 0000 0806                 00000000  3233+         VL    v22,0(R1)         use v22 to test decoder
000044AC  E310 5014 0014                 00000014  3234+         LGF   R1,V3ADDR         load v3 source
000044B2  E771 0000 0806                 00000000  3235+         VL    v23,0(R1)         use v23 to test decoder
000044B8  E766 7000 3EA4                           3236+         VMLE  V22,V22,V23,3      test instruction (dest is a source)
000044BE  E760 5028 080E                 00004488  3237+         VST   V22,V1O88          save v1 output
000044C4  07FB                                     3238+         BR    R11               return
000044C8                                           3239+RE88     DC    0F                xl16 expected result
000044C8                                           3240+         DROP  R5
000044C8  00010003 050C1344                        3241          DC    XL16'00010003050C1344 06D2FE7090F71480'   result
000044D0  06D2FE70 90F71480
000044D8  FF020304 05060750                        3242          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000044E0  090A0B0C 0D0E0F7F
000044E8  00010102 02030328                        3243          DC    XL16'0001010202030328 0405053C0607073F'   v3
000044F0  0405053C 0607073F
                                                   3244
                                                   3245          VRR_C VMLE,3
000044F8                                           3246+         DS    0FD
000044F8                         000044F8          3247+         USING *,R5              base for test data and test routine
000044F8  00004538                                 3248+T89      DC    A(X89)            address of test routine
000044FC  0059                                     3249+         DC    H'89'             test number
000044FE  00                                       3250+         DC    X'00'
000044FF  03                                       3251+         DC    HL1'3'            m4
00004500  E5D4D3C5 40404040                        3252+         DC    CL8'VMLE'         instruction name
00004508  00004570                                 3253+         DC    A(RE89+16)        address of v2 source
0000450C  00004580                                 3254+         DC    A(RE89+32)        address of v3 source
00004510  00000010                                 3255+         DC    A(16)             result length
00004514  00004560                                 3256+REA89    DC    A(RE89)           result address
00004518  00000000 00000000                        3257+         DS    FD                gap
00004520  00000000 00000000                        3258+V1O89    DS    XL16              V1 output
00004528  00000000 00000000
00004530  00000000 00000000                        3259+         DS    FD                gap
                                                   3260+*
00004538                                           3261+X89      DS    0F
00004538  E310 5010 0014                 00000010  3262+         LGF   R1,V2ADDR         load v2 source
0000453E  E761 0000 0806                 00000000  3263+         VL    v22,0(R1)         use v22 to test decoder
00004544  E310 5014 0014                 00000014  3264+         LGF   R1,V3ADDR         load v3 source
0000454A  E771 0000 0806                 00000000  3265+         VL    v23,0(R1)         use v23 to test decoder
00004550  E766 7000 3EA4                           3266+         VMLE  V22,V22,V23,3      test instruction (dest is a source)
00004556  E760 5028 080E                 00004520  3267+         VST   V22,V1O89          save v1 output
0000455C  07FB                                     3268+         BR    R11               return
00004560                                           3269+RE89     DC    0F                xl16 expected result
00004560                                           3270+         DROP  R5
00004560  00000000 00000009                        3271          DC    XL16'0000000000000009 F6141E28323C4920'   result
00004568  F6141E28 323C4920
00004570  FF020304 05060750                        3272          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004578  090A0B0C 0D0E0F7F
00004580  00000000 0000000A                        3273          DC    XL16'000000000000000A 0101010F0101010F'   v3
00004588  0101010F 0101010F
                                                   3274
                                                   3275          VRR_C VMLE,3
00004590                                           3276+         DS    0FD
00004590                         00004590          3277+         USING *,R5              base for test data and test routine
00004590  000045D0                                 3278+T90      DC    A(X90)            address of test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004594  005A                                     3279+         DC    H'90'              test number
00004596  00                                       3280+         DC    X'00'
00004597  03                                       3281+         DC    HL1'3'             m4
00004598  E5D4D3C5 40404040                        3282+         DC    CL8'VMLE'          instruction name
000045A0  00004608                                 3283+         DC    A(RE90+16)         address of v2 source
000045A4  00004618                                 3284+         DC    A(RE90+32)         address of v3 source
000045A8  00000010                                 3285+         DC    A(16)              result length
000045AC  000045F8                                 3286+REA90    DC    A(RE90)            result address
000045B0  00000000 00000000                        3287+         DS    FD                 gap
000045B8  00000000 00000000                        3288+V1O90    DS    XL16               V1 output
000045C0  00000000 00000000
000045C8  00000000 00000000                        3289+         DS    FD                 gap
                                                   3290+*
000045D0                                           3291+X90      DS    0F
000045D0  E310 5010 0014                 00000010  3292+         LGF   R1,V2ADDR          load v2 source
000045D6  E761 0000 0806                 00000000  3293+         VL    v22,0(R1)          use v22 to test decoder
000045DC  E310 5014 0014                 00000014  3294+         LGF   R1,V3ADDR          load v3 source
000045E2  E771 0000 0806                 00000000  3295+         VL    v23,0(R1)          use v23 to test decoder
000045E8  E766 7000 3EA4                           3296+         VMLE  V22,V22,V23,3       test instruction (dest is a source)
000045EE  E760 5028 080E                 000045B8  3297+         VST   V22,V1O90           save v1 output
000045F4  07FB                                     3298+         BR    R11                return
000045F8                                           3299+RE90     DC    0F                 xl16 expected result
000045F8                                           3300+         DROP  R5
000045F8  0009131E A8C3DFFE                        3301          DC    XL16'0009131EA8C3DFFE 091C345060616771'   result
00004600  091C3450 60616771
00004608  090A0B0C 0D0E0F7F                        3302          DC    XL16'090A0B0C0D0E0F7F FF02030405060750'   v2
00004610  FF020304 05060750
00004618  0101010F 0101010F                        3303          DC    XL16'0101010F0101010F 000000000000000A'   v3
00004620  00000000 0000000A
                                                   3304
                                                   3305 *-------------------------------------------------------------------
                                                   3306 *  VMLO   - Vector Multiply Logical Odd
                                                   3307 *-------------------------------------------------------------------
                                                   3308 * Byte
                                                   3309          VRR_C VMLO,0
00004628                                           3310+         DS    0FD
00004628                         00004628          3311+         USING *,R5               base for test data and test routine
00004628  00004668                                 3312+T91      DC    A(X91)             address of test routine
0000462C  005B                                     3313+         DC    H'91'              test number
0000462E  00                                       3314+         DC    X'00'
0000462F  00                                       3315+         DC    HL1'0'             m4
00004630  E5D4D3D6 40404040                        3316+         DC    CL8'VMLO'          instruction name
00004638  000046A0                                 3317+         DC    A(RE91+16)         address of v2 source
0000463C  000046B0                                 3318+         DC    A(RE91+32)         address of v3 source
00004640  00000010                                 3319+         DC    A(16)              result length
00004644  00004690                                 3320+REA91    DC    A(RE91)            result address
00004648  00000000 00000000                        3321+         DS    FD                 gap
00004650  00000000 00000000                        3322+V1O91    DS    XL16               V1 output
00004658  00000000 00000000
00004660  00000000 00000000                        3323+         DS    FD                 gap
                                                   3324+*
00004668                                           3325+X91      DS    0F
00004668  E310 5010 0014                 00000010  3326+         LGF   R1,V2ADDR          load v2 source
0000466E  E761 0000 0806                 00000000  3327+         VL    v22,0(R1)          use v22 to test decoder
00004674  E310 5014 0014                 00000014  3328+         LGF   R1,V3ADDR          load v3 source
0000467A  E771 0000 0806                 00000000  3329+         VL    v23,0(R1)          use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004680  E766 7000 0EA5                           3330+         VMLO  V22,V22,V23,0      test instruction (dest is a source)
00004686  E760 5028 080E                 00004650  3331+         VST   V22,V1O91          save v1 output
0000468C  07FB                                     3332+         BR    R11               return
00004690                                           3333+RE91     DC    0F                xl16 expected result
00004690                                           3334+         DROP  R5
00004690  00000000 00000271                        3335          DC    XL16'0000000000000271 000000000000F424'   result
00004698  00000000 0000F424
000046A0  FF000000 00000019                        3336          DC    XL16'FF00000000000019 38000000000000FA'   v2
000046A8  38000000 000000FA
000046B0  FF000000 00000019                        3337          DC    XL16'FF00000000000019 38000000000000FA'   v3
000046B8  38000000 000000FA
                                                   3338
                                                   3339          VRR_C VMLO,0
000046C0                                           3340+         DS    0FD
000046C0                      000046C0             3341+         USING *,R5              base for test data and test routine
000046C0  00004700                                 3342+T92      DC    A(X92)            address of test routine
000046C4  005C                                     3343+         DC    H'92'             test number
000046C6  00                                       3344+         DC    X'00'
000046C7  00                                       3345+         DC    HL1'0'            m4
000046C8  E5D4D3D6 40404040                        3346+         DC    CL8'VMLO'         instruction name
000046D0  00004738                                 3347+         DC    A(RE92+16)        address of v2 source
000046D4  00004748                                 3348+         DC    A(RE92+32)        address of v3 source
000046D8  00000010                                 3349+         DC    A(16)             result length
000046DC  00004728                                 3350+REA92    DC    A(RE92)           result address
000046E0  00000000 00000000                        3351+         DS    FD                gap
000046E8  00000000 00000000                        3352+V1O92    DS    XL16              V1 output
000046F0  00000000 00000000
000046F8  00000000 00000000                        3353+         DS    FD                gap
                                                   3354+*
00004700                                           3355+X92      DS    0F
00004700  E310 5010 0014                 00000010  3356+         LGF   R1,V2ADDR         load v2 source
00004706  E761 0000 0806                 00000000  3357+         VL    v22,0(R1)         use v22 to test decoder
0000470C  E310 5014 0014                 00000014  3358+         LGF   R1,V3ADDR         load v3 source
00004712  E771 0000 0806                 00000000  3359+         VL    v23,0(R1)         use v23 to test decoder
00004718  E766 7000 0EA5                           3360+         VMLO  V22,V22,V23,0      test instruction (dest is a source)
0000471E  E760 5028 080E                 000046E8  3361+         VST   V22,V1O92          save v1 output
00004724  07FB                                     3362+         BR    R11               return
00004728                                           3363+RE92     DC    0F                xl16 expected result
00004728                                           3364+         DROP  R5
00004728  00040010 00241900                        3365          DC    XL16'0004001000241900 0064384000B6FA09'   result
00004730  00643840 00B6FA09
00004738  FF020304 05060750                        3366          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004740  090A0B78 0C0D0EFD
00004748  FF020304 05060750                        3367          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00004750  090A0B78 0D0E0FFD
                                                   3368
                                                   3369          VRR_C VMLO,0
00004758                                           3370+         DS    0FD
00004758                      00004758             3371+         USING *,R5              base for test data and test routine
00004758  00004798                                 3372+T93      DC    A(X93)            address of test routine
0000475C  005D                                     3373+         DC    H'93'             test number
0000475E  00                                       3374+         DC    X'00'
0000475F  00                                       3375+         DC    HL1'0'            m4
00004760  E5D4D3D6 40404040                        3376+         DC    CL8'VMLO'         instruction name
00004768  000047D0                                 3377+         DC    A(RE93+16)        address of v2 source
0000476C  000047E0                                 3378+         DC    A(RE93+32)        address of v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004770  00000010                                 3379+         DC    A(16)              result length
00004774  000047C0                                 3380+REA93    DC    A(RE93)            result address
00004778  00000000 00000000                        3381+         DS    FD                 gap
00004780  00000000 00000000                        3382+V1O93    DS    XL16               V1 output
00004788  00000000 00000000
00004790  00000000 00000000                        3383+         DS    FD                 gap
                                                   3384+*
00004798                                           3385+X93      DS    0F
00004798  E310 5010 0014                 00000010  3386+         LGF   R1,V2ADDR          load v2 source
0000479E  E761 0000 0806                 00000000  3387+         VL    v22,0(R1)          use v22 to test decoder
000047A4  E310 5014 0014                 00000014  3388+         LGF   R1,V3ADDR          load v3 source
000047AA  E771 0000 0806                 00000000  3389+         VL    v23,0(R1)          use v23 to test decoder
000047B0  E766 7000 0EA5                           3390+         VMLO  V22,V22,V23,0       test instruction (dest is a source)
000047B6  E760 5028 080E                 00004780  3391+         VST   V22,V1O93           save v1 output
000047BC  07FB                                     3392+         BR    R11                return
000047C0                                           3393+RE93     DC    0F                 xl16 expected result
000047C0                                           3394+         DROP  R5
000047C0  00020008 00120C80                        3395          DC    XL16'0002000800120C80 00321C20005BFB06'   result
000047C8  00321C20 005BFB06
000047D0  FF020304 05060750                        3396          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000047D8  090A0B78 0C0D0EFD
000047E0  FF010102 02030328                        3397          DC    XL16'FF01010202030328 0405053C060707FE'   v3
000047E8  0405053C 060707FE
                                                   3398
                                                   3399          VRR_C VMLO,0
000047F0                                           3400+         DS    0FD
000047F0                 000047F0                  3401+         USING *,R5               base for test data and test routine
000047F0  00004830                                 3402+T94      DC    A(X94)             address of test routine
000047F4  005E                                     3403+         DC    H'94'              test number
000047F6  00                                       3404+         DC    X'00'
000047F7  00                                       3405+         DC    HL1'0'             m4
000047F8  E5D4D3D6 40404040                        3406+         DC    CL8'VMLO'          instruction name
00004800  00004868                                 3407+         DC    A(RE94+16)         address of v2 source
00004804  00004878                                 3408+         DC    A(RE94+32)         address of v3 source
00004808  00000010                                 3409+         DC    A(16)              result length
0000480C  00004858                                 3410+REA94    DC    A(RE94)            result address
00004810  00000000 00000000                        3411+         DS    FD                 gap
00004818  00000000 00000000                        3412+V1O94    DS    XL16               V1 output
00004820  00000000 00000000
00004828  00000000 00000000                        3413+         DS    FD                 gap
                                                   3414+*
00004830                                           3415+X94      DS    0F
00004830  E310 5010 0014                 00000010  3416+         LGF   R1,V2ADDR          load v2 source
00004836  E761 0000 0806                 00000000  3417+         VL    v22,0(R1)          use v22 to test decoder
0000483C  E310 5014 0014                 00000014  3418+         LGF   R1,V3ADDR          load v3 source
00004842  E771 0000 0806                 00000000  3419+         VL    v23,0(R1)          use v23 to test decoder
00004848  E766 7000 0EA5                           3420+         VMLO  V22,V22,V23,0       test instruction (dest is a source)
0000484E  E760 5028 080E                 00004818  3421+         VST   V22,V1O94           save v1 output
00004854  07FB                                     3422+         BR    R11                return
00004858                                           3423+RE94     DC    0F                 xl16 expected result
00004858                                           3424+         DROP  R5
00004858  00000000 00000320                        3425          DC    XL16'0000000000000320 000A0708000DFC03'   result
00004860  000A0708 000DFC03
00004868  FF020304 05060750                        3426          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004870  090A0B78 0C0D0EFD
00004878  FF000000 0000000A                        3427          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004880  0101010F 010101FF
                                                  3428
                                                  3429 * Halfword
                                                  3430          VRR_C VMLO,1
00004888                                          3431+         DS    0FD
00004888                      00004888            3432+         USING *,R5              base for test data and test routine
00004888  000048C8                                3433+T95      DC    A(X95)            address of test routine
0000488C  005F                                    3434+         DC    H'95'             test number
0000488E  00                                      3435+         DC    X'00'
0000488F  01                                      3436+         DC    HL1'1'            m4
00004890  E5D4D3D6 40404040                       3437+         DC    CL8'VMLO'         instruction name
00004898  00004900                                3438+         DC    A(RE95+16)        address of v2 source
0000489C  00004910                                3439+         DC    A(RE95+32)        address of v3 source
000048A0  00000010                                3440+         DC    A(16)             result length
000048A4  000048F0                                3441+REA95    DC    A(RE95)           result address
000048A8  00000000 00000000                       3442+         DS    FD                gap
000048B0  00000000 00000000                       3443+V1O95    DS    XL16              V1 output
000048B8  00000000 00000000
000048C0  00000000 00000000                       3444+         DS    FD                gap
                                                  3445+*
000048C8                                          3446+X95      DS    0F
000048C8  E310 5010 0014                00000010  3447+         LGF   R1,V2ADDR         load v2 source
000048CE  E761 0000 0806                00000000  3448+         VL    v22,0(R1)         use v22 to test decoder
000048D4  E310 5014 0014                00000014  3449+         LGF   R1,V3ADDR         load v3 source
000048DA  E771 0000 0806                00000000  3450+         VL    v23,0(R1)         use v23 to test decoder
000048E0  E766 7000 1EA5                          3451+         VMLO  V22,V22,V23,1      test instruction (dest is a source)
000048E6  E760 5028 080E                000048B0  3452+         VST   V22,V1O95          save v1 output
000048EC  07FB                                    3453+         BR    R11               return
000048F0                                          3454+RE95     DC    0F                xl16 expected result
000048F0                                          3455+         DROP  R5
000048F0  00000000 00000271                       3456          DC    XL16'0000000000000271 00000000DF15CC24'   result
000048F8  00000000 DF15CC24
00004900  FFFF0000 00000019                       3457          DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00004908  00380000 1000EEFA
00004910  FFFF0000 00000019                       3458          DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00004918  00380003 8000EEFA
                                                  3459
                                                  3460          VRR_C VMLO,1
00004920                                          3461+         DS    0FD
00004920                      00004920            3462+         USING *,R5              base for test data and test routine
00004920  00004960                                3463+T96      DC    A(X96)            address of test routine
00004924  0060                                    3464+         DC    H'96'             test number
00004926  00                                      3465+         DC    X'00'
00004927  01                                      3466+         DC    HL1'1'            m4
00004928  E5D4D3D6 40404040                       3467+         DC    CL8'VMLO'         instruction name
00004930  00004998                                3468+         DC    A(RE96+16)        address of v2 source
00004934  000049A8                                3469+         DC    A(RE96+32)        address of v3 source
00004938  00000010                                3470+         DC    A(16)             result length
0000493C  00004988                                3471+REA96    DC    A(RE96)           result address
00004940  00000000 00000000                       3472+         DS    FD                gap
00004948  00000000 00000000                       3473+V1O96    DS    XL16              V1 output
00004950  00000000 00000000
00004958  00000000 00000000                       3474+         DS    FD                gap
                                                  3475+*
00004960                                          3476+X96      DS    0F
00004960  E310 5010 0014                00000010  3477+         LGF   R1,V2ADDR         load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00004966  E761 0000 0806                00000000  3478+         VL    v22,0(R1)         use v22 to test decoder
0000496C  E310 5014 0014                00000014  3479+         LGF   R1,V3ADDR         load v3 source
00004972  E771 0000 0806                00000000  3480+         VL    v23,0(R1)         use v23 to test decoder
00004978  E766 7000 1EA5                          3481+         VMLO  V22,V22,V23,1      test instruction (dest is a source)
0000497E  E760 5028 080E                00004948  3482+         VST   V22,V1O96          save v1 output
00004984  07FB                                    3483+         BR    R11               return
00004988                                          3484+RE96     DC    0F                xl16 expected result
00004988                                          3485+         DROP  R5
00004988  00091810 00357900                       3486          DC    XL16'0009181000357900 0083884000EFA309'   result
00004990  00838840 00EFA309
00004998  FF020304 05060750                       3487          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000049A0  090A0B78 0C0D0EFD
000049A8  FF020304 05060750                       3488          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000049B0  090A0B78 0D0E0FFD
                                                  3489
                                                  3490          VRR_C VMLO,1
000049B8                                          3491+         DS    0FD
000049B8                        000049B8          3492+         USING *,R5              base for test data and test routine
000049B8  000049F8                                3493+T97      DC    A(X97)            address of test routine
000049BC  0061                                    3494+         DC    H'97'             test number
000049BE  00                                      3495+         DC    X'00'
000049BF  01                                      3496+         DC    HL1'1'            m4
000049C0  E5D4D3D6 40404040                       3497+         DC    CL8'VMLO'         instruction name
000049C8  00004A30                                3498+         DC    A(RE97+16)        address of v2 source
000049CC  00004A40                                3499+         DC    A(RE97+32)        address of v3 source
000049D0  00000010                                3500+         DC    A(16)             result length
000049D4  00004A20                                3501+REA97    DC    A(RE97)           result address
000049D8  00000000 00000000                       3502+         DS    FD                gap
000049E0  00000000 00000000                       3503+V1O97    DS    XL16              V1 output
000049E8  00000000 00000000
000049F0  00000000 00000000                       3504+         DS    FD                gap
                                                  3505+*
000049F8                                          3506+X97      DS    0F
000049F8  E310 5010 0014                00000010  3507+         LGF   R1,V2ADDR         load v2 source
000049FE  E761 0000 0806                00000000  3508+         VL    v22,0(R1)         use v22 to test decoder
00004A04  E310 5014 0014                00000014  3509+         LGF   R1,V3ADDR         load v3 source
00004A0A  E771 0000 0806                00000000  3510+         VL    v23,0(R1)         use v23 to test decoder
00004A10  E766 7000 1EA5                          3511+         VMLO  V22,V22,V23,1      test instruction (dest is a source)
00004A16  E760 5028 080E                000049E0  3512+         VST   V22,V1O97          save v1 output
00004A1C  07FB                                    3513+         BR    R11               return
00004A20                                          3514+RE97     DC    0F                xl16 expected result
00004A20                                          3515+         DROP  R5
00004A20  00030A08 00171480                       3516          DC    XL16'00030A0800171480 003C08200077CA06'   result
00004A28  003C0820 0077CA06
00004A30  FF020304 05060750                       3517          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004A38  090A0B78 0C0D0EFD
00004A40  FF010102 02030328                       3518          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00004A48  0405053C 060707FE
                                                  3519
                                                  3520          VRR_C VMLO,1
00004A50                                          3521+         DS    0FD
00004A50                        00004A50          3522+         USING *,R5              base for test data and test routine
00004A50  00004A90                                3523+T98      DC    A(X98)            address of test routine
00004A54  0062                                    3524+         DC    H'98'             test number
00004A56  00                                      3525+         DC    X'00'
00004A57  01                                      3526+         DC    HL1'1'            m4
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004A58  E5D4D3D6 40404040                        3527+         DC    CL8'VMLO'         instruction name
00004A60  00004AC8                                 3528+         DC    A(RE98+16)        address of v2 source
00004A64  00004AD8                                 3529+         DC    A(RE98+32)        address of v3 source
00004A68  00000010                                 3530+         DC    A(16)             result length
00004A6C  00004AB8                                 3531+REA98    DC    A(RE98)           result address
00004A70  00000000 00000000                        3532+         DS    FD                gap
00004A78  00000000 00000000                        3533+V1O98    DS    XL16              V1 output
00004A80  00000000 00000000
00004A88  00000000 00000000                        3534+         DS    FD                gap
                                                   3535+*
00004A90                                           3536+X98      DS    0F
00004A90  E310 5010 0014                 00000010  3537+         LGF   R1,V2ADDR         load v2 source
00004A96  E761 0000 0806                 00000000  3538+         VL    v22,0(R1)         use v22 to test decoder
00004A9C  E310 5014 0014                 00000014  3539+         LGF   R1,V3ADDR         load v3 source
00004AA2  E771 0000 0806                 00000000  3540+         VL    v23,0(R1)         use v23 to test decoder
00004AA8  E766 7000 1EA5                           3541+         VMLO  V22,V22,V23,1      test instruction (dest is a source)
00004AAE  E760 5028 080E                 00004A78  3542+         VST   V22,V1O98          save v1 output
00004AB4  07FB                                     3543+         BR    R11               return
00004AB8                                           3544+RE98     DC    0F                xl16 expected result
00004AB8                                           3545+         DROP  R5
00004AB8  00000000 00004920                        3546          DC    XL16'0000000000004920 000C2408001DEB03'   result
00004AC0  000C2408 001DEB03
00004AC8  FF020304 05060750                        3547          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00004AD0  090A0B78 0C0D0EFD
00004AD8  FF000000 0000000A                        3548          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00004AE0  0101010F 010101FF
                                                   3549
                                                   3550 * Word
                                                   3551          VRR_C VMLO,2
00004AE8                                           3552+         DS    0FD
00004AE8                      00004AE8             3553+         USING *,R5              base for test data and test routine
00004AE8  00004B28                                 3554+T99      DC    A(X99)            address of test routine
00004AEC  0063                                     3555+         DC    H'99'             test number
00004AEE  00                                       3556+         DC    X'00'
00004AEF  02                                       3557+         DC    HL1'2'            m4
00004AF0  E5D4D3D6 40404040                        3558+         DC    CL8'VMLO'         instruction name
00004AF8  00004B60                                 3559+         DC    A(RE99+16)        address of v2 source
00004AFC  00004B70                                 3560+         DC    A(RE99+32)        address of v3 source
00004B00  00000010                                 3561+         DC    A(16)             result length
00004B04  00004B50                                 3562+REA99    DC    A(RE99)           result address
00004B08  00000000 00000000                        3563+         DS    FD                gap
00004B10  00000000 00000000                        3564+V1O99    DS    XL16              V1 output
00004B18  00000000 00000000
00004B20  00000000 00000000                        3565+         DS    FD                gap
                                                   3566+*
00004B28                                           3567+X99      DS    0F
00004B28  E310 5010 0014                 00000010  3568+         LGF   R1,V2ADDR         load v2 source
00004B2E  E761 0000 0806                 00000000  3569+         VL    v22,0(R1)         use v22 to test decoder
00004B34  E310 5014 0014                 00000014  3570+         LGF   R1,V3ADDR         load v3 source
00004B3A  E771 0000 0806                 00000000  3571+         VL    v23,0(R1)         use v23 to test decoder
00004B40  E766 7000 2EA5                           3572+         VMLO  V22,V22,V23,2      test instruction (dest is a source)
00004B46  E760 5028 080E                 00004B10  3573+         VST   V22,V1O99          save v1 output
00004B4C  07FB                                     3574+         BR    R11               return
00004B50                                           3575+RE99     DC    0F                xl16 expected result
00004B50                                           3576+         DROP  R5
00004B50  00000002 71000000                        3577          DC    XL16'0000000271000000 0DF0123F4FEDCC24'   result
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004B58  0DF0123F 4FEDCC24
00004B60  FFFFFFFF 00019000                         3578          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00004B68  00000038 EEEEEEFA
00004B70  FFFFFFFF 00019000                         3579          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00004B78  00000038 0EEEEEFA
                                                    3580
                                                    3581          VRR_C VMLO,2
00004B80                                            3582+         DS    0FD
00004B80                      00004B80              3583+         USING *,R5              base for test data and test routine
00004B80  00004BC0                                  3584+T100     DC    A(X100)           address of test routine
00004B84  0064                                      3585+         DC    H'100'            test number
00004B86  00                                        3586+         DC    X'00'
00004B87  02                                        3587+         DC    HL1'2'            m4
00004B88  E5D4D3D6 40404040                         3588+         DC    CL8'VMLO'         instruction name
00004B90  00004BF8                                  3589+         DC    A(RE100+16)       address of v2 source
00004B94  00004C08                                  3590+         DC    A(RE100+32)       address of v3 source
00004B98  00000010                                  3591+         DC    A(16)             result length
00004B9C  00004BE8                                  3592+REA100   DC    A(RE100)          result address
00004BA0  00000000 00000000                         3593+         DS    FD                gap
00004BA8  00000000 00000000                         3594+V1O100   DS    XL16              V1 output
00004BB0  00000000 00000000
00004BB8  00000000 00000000                         3595+         DS    FD                gap
                                                    3596+*
00004BC0                                            3597+X100     DS    0F
00004BC0  E310 5010 0014                 00000010   3598+         LGF   R1,V2ADDR         load v2 source
00004BC6  E761 0000 0806                 00000000   3599+         VL    v22,0(R1)         use v22 to test decoder
00004BCC  E310 5014 0014                 00000014   3600+         LGF   R1,V3ADDR         load v3 source
00004BD2  E771 0000 0806                 00000000   3601+         VL    v23,0(R1)         use v23 to test decoder
00004BD8  E766 7000 2EA5                            3602+         VMLO  V22,V22,V23,2      test instruction (dest is a source)
00004BDE  E760 5028 080E                 00004BA8   3603+         VST   V22,V1O100         save v1 output
00004BE4  07FB                                      3604+         BR    R11               return
00004BE8                                            3605+RE100    DC    0F                xl16 expected result
00004BE8                                            3606+         DROP  R5
00004BE8  00193C6D 77F57900                         3607          DC    XL16'00193C6D77F57900 00AA6E5898D42101'   result
00004BF0  00AA6E58 98D42101
00004BF8  FF020304 05060750                         3608          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004C00  090A0B0C 0D0E0F7F
00004C08  FF020304 05060750                         3609          DC    XL16'FF02030405060750 090A0B780D0E0F7F'   v3
00004C10  090A0B78 0D0E0F7F
                                                    3610
                                                    3611          VRR_C VMLO,2
00004C18                                            3612+         DS    0FD
00004C18                      00004C18              3613+         USING *,R5              base for test data and test routine
00004C18  00004C58                                  3614+T101     DC    A(X101)           address of test routine
00004C1C  0065                                      3615+         DC    H'101'            test number
00004C1E  00                                        3616+         DC    X'00'
00004C1F  02                                        3617+         DC    HL1'2'            m4
00004C20  E5D4D3D6 40404040                         3618+         DC    CL8'VMLO'         instruction name
00004C28  00004C90                                  3619+         DC    A(RE101+16)       address of v2 source
00004C2C  00004CA0                                  3620+         DC    A(RE101+32)       address of v3 source
00004C30  00000010                                  3621+         DC    A(16)             result length
00004C34  00004C80                                  3622+REA101   DC    A(RE101)          result address
00004C38  00000000 00000000                         3623+         DS    FD                gap
00004C40  00000000 00000000                         3624+V1O101   DS    XL16              V1 output
00004C48  00000000 00000000
00004C50  00000000 00000000                         3625+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3626+*
00004C58                                           3627+X101     DS    0F
00004C58  E310 5010 0014                 00000010  3628+         LGF   R1,V2ADDR         load v2 source
00004C5E  E761 0000 0806                 00000000  3629+         VL    v22,0(R1)         use v22 to test decoder
00004C64  E310 5014 0014                 00000014  3630+         LGF   R1,V3ADDR         load v3 source
00004C6A  E771 0000 0806                 00000000  3631+         VL    v23,0(R1)         use v23 to test decoder
00004C70  E766 7000 2EA5                           3632+         VMLO  V22,V22,V23,2      test instruction (dest is a source)
00004C76  E760 5028 080E                 00004C40  3633+         VST   V22,V1O101         save v1 output
00004C7C  07FB                                     3634+         BR    R11               return
00004C80                                           3635+RE101    DC    0F                xl16 expected result
00004C80                                           3636+         DROP  R5
00004C80  000A1B30 90F71480                        3637          DC    XL16'000A1B3090F71480 004EB01DFF5B4941'   result
00004C88  004EB01D FF5B4941
00004C90  FF020304 05060750                        3638          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004C98  090A0B0C 0D0E0F7F
00004CA0  FF010102 02030328                        3639          DC    XL16'FF01010202030328 0405053C0607073F'   v3
00004CA8  0405053C 0607073F
                                                   3640
                                                   3641          VRR_C VMLO,2
00004CB0                                           3642+         DS    0FD
00004CB0                         00004CB0          3643+         USING *,R5              base for test data and test routine
00004CB0  00004CF0                                 3644+T102     DC    A(X102)           address of test routine
00004CB4  0066                                     3645+         DC    H'102'            test number
00004CB6  00                                       3646+         DC    X'00'
00004CB7  02                                       3647+         DC    HL1'2'            m4
00004CB8  E5D4D3D6 40404040                        3648+         DC    CL8'VMLO'         instruction name
00004CC0  00004D28                                 3649+         DC    A(RE102+16)       address of v2 source
00004CC4  00004D38                                 3650+         DC    A(RE102+32)       address of v3 source
00004CC8  00000010                                 3651+         DC    A(16)             result length
00004CCC  00004D18                                 3652+REA102   DC    A(RE102)          result address
00004CD0  00000000 00000000                        3653+         DS    FD                gap
00004CD8  00000000 00000000                        3654+V1O102   DS    XL16              V1 output
00004CE0  00000000 00000000
00004CE8  00000000 00000000                        3655+         DS    FD                gap
                                                   3656+*
00004CF0                                           3657+X102     DS    0F
00004CF0  E310 5010 0014                 00000010  3658+         LGF   R1,V2ADDR         load v2 source
00004CF6  E761 0000 0806                 00000000  3659+         VL    v22,0(R1)         use v22 to test decoder
00004CFC  E310 5014 0014                 00000014  3660+         LGF   R1,V3ADDR         load v3 source
00004D02  E771 0000 0806                 00000000  3661+         VL    v23,0(R1)         use v23 to test decoder
00004D08  E766 7000 2EA5                           3662+         VMLO  V22,V22,V23,2      test instruction (dest is a source)
00004D0E  E760 5028 080E                 00004CD8  3663+         VST   V22,V1O102         save v1 output
00004D14  07FB                                     3664+         BR    R11               return
00004D18                                           3665+RE102    DC    0F                xl16 expected result
00004D18                                           3666+         DROP  R5
00004D18  00000000 323C4920                        3667          DC    XL16'00000000323C4920 000D1B2B60616771'   result
00004D20  000D1B2B 60616771
00004D28  FF020304 05060750                        3668          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004D30  090A0B0C 0D0E0F7F
00004D38  FF000000 0000000A                        3669          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
00004D40  0101010F 0101010F
                                                   3670
                                                   3671 * Doubleword
                                                   3672          VRR_C VMLO,3
00004D48                                           3673+         DS    0FD
00004D48                         00004D48          3674+         USING *,R5              base for test data and test routine
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004D48  00004D88                                 3675+T103     DC    A(X103)           address of test routine
00004D4C  0067                                     3676+         DC    H'103'            test number
00004D4E  00                                       3677+         DC    X'00'
00004D4F  03                                       3678+         DC    HL1'3'            m4
00004D50  E5D4D3D6 40404040                        3679+         DC    CL8'VMLO'         instruction name
00004D58  00004DC0                                 3680+         DC    A(RE103+16)       address of v2 source
00004D5C  00004DD0                                 3681+         DC    A(RE103+32)       address of v3 source
00004D60  00000010                                 3682+         DC    A(16)             result length
00004D64  00004DB0                                 3683+REA103   DC    A(RE103)          result address
00004D68  00000000 00000000                        3684+         DS    FD                gap
00004D70  00000000 00000000                        3685+V1O103   DS    XL16              V1 output
00004D78  00000000 00000000
00004D80  00000000 00000000                        3686+         DS    FD                gap
                                                   3687+*
00004D88                                           3688+X103     DS    0F
00004D88  E310 5010 0014                 00000010  3689+         LGF   R1,V2ADDR         load v2 source
00004D8E  E761 0000 0806                 00000000  3690+         VL    v22,0(R1)         use v22 to test decoder
00004D94  E310 5014 0014                 00000014  3691+         LGF   R1,V3ADDR         load v3 source
00004D9A  E771 0000 0806                 00000000  3692+         VL    v23,0(R1)         use v23 to test decoder
00004DA0  E766 7000 3EA5                           3693+         VMLO  V22,V22,V23,3      test instruction (dest is a source)
00004DA6  E760 5028 080E                 00004D70  3694+         VST   V22,V1O103         save v1 output
00004DAC  07FB                                     3695+         BR    R11               return
00004DB0                                           3696+RE103    DC    0F                xl16 expected result
00004DB0                                           3697+         DROP  R5
00004DB0  00000000 00000C77                        3698          DC    XL16'0000000000000C77 96789F9F4FEDCC24'   result
00004DB8  96789F9F 4FEDCC24
00004DC0  FFFFFFFF 00019000                        3699          DC    XL16'FFFFFFFF00019000 00000038EEEEEFA'   v2
00004DC8  00000038 EEEEEEFA
00004DD0  FFFFFFFF 00019000                        3700          DC    XL16'FFFFFFFF00019000 000000380EEEEFA'   v3
00004DD8  00000038 0EEEEEFA
                                                   3701
                                                   3702          VRR_C VMLO,3
00004DE0                                           3703+         DS    0FD
00004DE0                      00004DE0             3704+         USING *,R5              base for test data and test routine
00004DE0  00004E20                                 3705+T104     DC    A(X104)           address of test routine
00004DE4  0068                                     3706+         DC    H'104'            test number
00004DE6  00                                       3707+         DC    X'00'
00004DE7  03                                       3708+         DC    HL1'3'            m4
00004DE8  E5D4D3D6 40404040                        3709+         DC    CL8'VMLO'         instruction name
00004DF0  00004E58                                 3710+         DC    A(RE104+16)       address of v2 source
00004DF4  00004E68                                 3711+         DC    A(RE104+32)       address of v3 source
00004DF8  00000010                                 3712+         DC    A(16)             result length
00004DFC  00004E48                                 3713+REA104   DC    A(RE104)          result address
00004E00  00000000 00000000                        3714+         DS    FD                gap
00004E08  00000000 00000000                        3715+V1O104   DS    XL16              V1 output
00004E10  00000000 00000000
00004E18  00000000 00000000                        3716+         DS    FD                gap
                                                   3717+*
00004E20                                           3718+X104     DS    0F
00004E20  E310 5010 0014                 00000010  3719+         LGF   R1,V2ADDR         load v2 source
00004E26  E761 0000 0806                 00000000  3720+         VL    v22,0(R1)         use v22 to test decoder
00004E2C  E310 5014 0014                 00000014  3721+         LGF   R1,V3ADDR         load v3 source
00004E32  E771 0000 0806                 00000000  3722+         VL    v23,0(R1)         use v23 to test decoder
00004E38  E766 7000 3EA5                           3723+         VMLO  V22,V22,V23,3      test instruction (dest is a source)
00004E3E  E760 5028 080E                 00004E08  3724+         VST   V22,V1O104         save v1 output
00004E44  07FB                                     3725+         BR    R11               return
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004E48                                           3726+RE104    DC    0F                xl16 expected result
00004E48                                           3727+         DROP  R5
00004E48  0051B52F 8692B4F6                        3728          DC    XL16'0051B52F8692B4F6 152B55D498D42101'   result
00004E50  152B55D4 98D42101
00004E58  FF020304 05060750                        3729          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004E60  090A0B0C 0D0E0F7F
00004E68  01020304 05060750                        3730          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00004E70  090A0B78 0D0E0F7F
                                                   3731
                                                   3732          VRR_C VMLO,3
00004E78                                           3733+         DS    0FD
00004E78                      00004E78             3734+         USING *,R5              base for test data and test routine
00004E78  00004EB8                                 3735+T105     DC    A(X105)           address of test routine
00004E7C  0069                                     3736+         DC    H'105'            test number
00004E7E  00                                       3737+         DC    X'00'
00004E7F  03                                       3738+         DC    HL1'3'            m4
00004E80  E5D4D3D6 40404040                        3739+         DC    CL8'VMLO'         instruction name
00004E88  00004EF0                                 3740+         DC    A(RE105+16)       address of v2 source
00004E8C  00004F00                                 3741+         DC    A(RE105+32)       address of v3 source
00004E90  00000010                                 3742+         DC    A(16)             result length
00004E94  00004EE0                                 3743+REA105   DC    A(RE105)          result address
00004E98  00000000 00000000                        3744+         DS    FD                gap
00004EA0  00000000 00000000                        3745+V1O105   DS    XL16              V1 output
00004EA8  00000000 00000000
00004EB0  00000000 00000000                        3746+         DS    FD                gap
                                                   3747+*
00004EB8                                           3748+X105     DS    0F
00004EB8  E310 5010 0014                00000010   3749+         LGF   R1,V2ADDR         load v2 source
00004EBE  E761 0000 0806                00000000   3750+         VL    v22,0(R1)         use v22 to test decoder
00004EC4  E310 5014 0014                00000014   3751+         LGF   R1,V3ADDR         load v3 source
00004ECA  E771 0000 0806                00000000   3752+         VL    v23,0(R1)         use v23 to test decoder
00004ED0  E766 7000 3EA5                           3753+         VMLO  V22,V22,V23,3      test instruction (dest is a source)
00004ED6  E760 5028 080E                00004EA0   3754+         VST   V22,V1O105         save v1 output
00004EDC  07FB                                     3755+         BR    R11               return
00004EE0                                           3756+RE105    DC    0F                xl16 expected result
00004EE0                                           3757+         DROP  R5
00004EE0  0024558D B838C862                        3758          DC    XL16'0024558DB838C862 B47CD8D5FF5B4941'   result
00004EE8  B47CD8D5 FF5B4941
00004EF0  FF020304 05060750                        3759          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004EF8  090A0B0C 0D0E0F7F
00004F00  00010102 02030328                        3760          DC    XL16'0001010202030328 0405053C0607073F'   v3
00004F08  0405053C 0607073F
                                                   3761
                                                   3762          VRR_C VMLO,3
00004F10                                           3763+         DS    0FD
00004F10                      00004F10             3764+         USING *,R5              base for test data and test routine
00004F10  00004F50                                 3765+T106     DC    A(X106)           address of test routine
00004F14  006A                                     3766+         DC    H'106'            test number
00004F16  00                                       3767+         DC    X'00'
00004F17  03                                       3768+         DC    HL1'3'            m4
00004F18  E5D4D3D6 40404040                        3769+         DC    CL8'VMLO'         instruction name
00004F20  00004F88                                 3770+         DC    A(RE106+16)       address of v2 source
00004F24  00004F98                                 3771+         DC    A(RE106+32)       address of v3 source
00004F28  00000010                                 3772+         DC    A(16)             result length
00004F2C  00004F78                                 3773+REA106   DC    A(RE106)          result address
00004F30  00000000 00000000                        3774+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00004F38  00000000 00000000                        3775+V1O106   DS    XL16              V1 output
00004F40  00000000 00000000
00004F48  00000000 00000000                        3776+         DS    FD                gap
                                                   3777+*
00004F50                                           3778+X106     DS    0F
00004F50  E310 5010 0014                 00000010  3779+         LGF   R1,V2ADDR         load v2 source
00004F56  E761 0000 0806                 00000000  3780+         VL    v22,0(R1)         use v22 to test decoder
00004F5C  E310 5014 0014                 00000014  3781+         LGF   R1,V3ADDR         load v3 source
00004F62  E771 0000 0806                 00000000  3782+         VL    v23,0(R1)         use v23 to test decoder
00004F68  E766 7000 3EA5                           3783+         VMLO  V22,V22,V23,3      test instruction (dest is a source)
00004F6E  E760 5028 080E                 00004F38  3784+         VST   V22,V1O106         save v1 output
00004F74  07FB                                     3785+         BR    R11               return
00004F78                                           3786+RE106    DC    0F                xl16 expected result
00004F78                                           3787+         DROP  R5
00004F78  0009131E A8C3DFFE                        3788          DC    XL16'0009131EA8C3DFFE 091C345060616771'   result
00004F80  091C3450 60616771
00004F88  FF020304 05060750                        3789          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00004F90  090A0B0C 0D0E0F7F
00004F98  00000000 0000000A                        3790          DC    XL16'000000000000000A 0101010F0101010F'   v3
00004FA0  0101010F 0101010F
                                                   3791
                                                   3792          VRR_C VMLO,3
00004FA8                                           3793+         DS    0FD
00004FA8                         00004FA8          3794+         USING *,R5              base for test data and test routine
00004FA8  00004FE8                                 3795+T107     DC    A(X107)           address of test routine
00004FAC  006B                                     3796+         DC    H'107'            test number
00004FAE  00                                       3797+         DC    X'00'
00004FAF  03                                       3798+         DC    HL1'3'            m4
00004FB0  E5D4D3D6 40404040                        3799+         DC    CL8'VMLO'         instruction name
00004FB8  00005020                                 3800+         DC    A(RE107+16)       address of v2 source
00004FBC  00005030                                 3801+         DC    A(RE107+32)       address of v3 source
00004FC0  00000010                                 3802+         DC    A(16)             result length
00004FC4  00005010                                 3803+REA107   DC    A(RE107)          result address
00004FC8  00000000 00000000                        3804+         DS    FD                gap
00004FD0  00000000 00000000                        3805+V1O107   DS    XL16              V1 output
00004FD8  00000000 00000000
00004FE0  00000000 00000000                        3806+         DS    FD                gap
                                                   3807+*
00004FE8                                           3808+X107     DS    0F
00004FE8  E310 5010 0014                 00000010  3809+         LGF   R1,V2ADDR         load v2 source
00004FEE  E761 0000 0806                 00000000  3810+         VL    v22,0(R1)         use v22 to test decoder
00004FF4  E310 5014 0014                 00000014  3811+         LGF   R1,V3ADDR         load v3 source
00004FFA  E771 0000 0806                 00000000  3812+         VL    v23,0(R1)         use v23 to test decoder
00005000  E766 7000 3EA5                           3813+         VMLO  V22,V22,V23,3      test instruction (dest is a source)
00005006  E760 5028 080E                 00004FD0  3814+         VST   V22,V1O107         save v1 output
0000500C  07FB                                     3815+         BR    R11               return
00005010                                           3816+RE107    DC    0F                xl16 expected result
00005010                                           3817+         DROP  R5
00005010  00000000 00000009                        3818          DC    XL16'0000000000000009 F6141E28323C4920'   result
00005018  F6141E28 323C4920
00005020  090A0B0C 0D0E0F7F                        3819          DC    XL16'090A0B0C0D0E0F7F FF02030405060750'   v2
00005028  FF020304 05060750
00005030  0101010F 0101010F                        3820          DC    XL16'0101010F0101010F 000000000000000A'   v3
00005038  00000000 0000000A
                                                   3821
                                                   3822 *-----------------------------------------------------------------
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   3823 *  VME    - Vector Multiply Even
                                                   3824 *-----------------------------------------------------------------
                                                   3825 * Byte
                                                   3826          VRR_C VME,0
00005040                                           3827+         DS    0FD
00005040                       00005040            3828+         USING *,R5              base for test data and test routine
00005040  00005080                                 3829+T108     DC    A(X108)           address of test routine
00005044  006C                                     3830+         DC    H'108'            test number
00005046  00                                       3831+         DC    X'00'
00005047  00                                       3832+         DC    HL1'0'            m4
00005048  E5D4C540 40404040                        3833+         DC    CL8'VME'          instruction name
00005050  000050B8                                 3834+         DC    A(RE108+16)       address of v2 source
00005054  000050C8                                 3835+         DC    A(RE108+32)       address of v3 source
00005058  00000010                                 3836+         DC    A(16)             result length
0000505C  000050A8                                 3837+REA108   DC    A(RE108)          result address
00005060  00000000 00000000                        3838+         DS    FD                gap
00005068  00000000 00000000                        3839+V1O108   DS    XL16              V1 output
00005070  00000000 00000000
00005078  00000000 00000000                        3840+         DS    FD                gap
                                                   3841+*
00005080                                           3842+X108     DS    0F
00005080  E310 5010 0014                00000010   3843+         LGF   R1,V2ADDR         load v2 source
00005086  E761 0000 0806                00000000   3844+         VL    v22,0(R1)         use v22 to test decoder
0000508C  E310 5014 0014                00000014   3845+         LGF   R1,V3ADDR         load v3 source
00005092  E771 0000 0806                00000000   3846+         VL    v23,0(R1)         use v23 to test decoder
00005098  E766 7000 0EA6                           3847+         VME   V22,V22,V23,0      test instruction (dest is a source)
0000509E  E760 5028 080E                00005068   3848+         VST   V22,V1O108         save v1 output
000050A4  07FB                                     3849+         BR    R11               return
000050A8                                           3850+RE108    DC    0F                xl16 expected result
000050A8                                           3851+         DROP  R5
000050A8  00010000 00000000                        3852          DC    XL16'0001000000000000 0C40000000000000'   result
000050B0  0C400000 00000000
000050B8  FF000000 00000019                        3853          DC    XL16'FF00000000000019 38000000000000FA'   v2
000050C0  38000000 000000FA
000050C8  FF000000 00000019                        3854          DC    XL16'FF00000000000019 38000000000000FA'   v3
000050D0  38000000 000000FA
                                                   3855
                                                   3856          VRR_C VME,0
000050D8                                           3857+         DS    0FD
000050D8                       000050D8            3858+         USING *,R5              base for test data and test routine
000050D8  00005118                                 3859+T109     DC    A(X109)           address of test routine
000050DC  006D                                     3860+         DC    H'109'            test number
000050DE  00                                       3861+         DC    X'00'
000050DF  00                                       3862+         DC    HL1'0'            m4
000050E0  E5D4C540 40404040                        3863+         DC    CL8'VME'          instruction name
000050E8  00005150                                 3864+         DC    A(RE109+16)       address of v2 source
000050EC  00005160                                 3865+         DC    A(RE109+32)       address of v3 source
000050F0  00000010                                 3866+         DC    A(16)             result length
000050F4  00005140                                 3867+REA109   DC    A(RE109)          result address
000050F8  00000000 00000000                        3868+         DS    FD                gap
00005100  00000000 00000000                        3869+V1O109   DS    XL16              V1 output
00005108  00000000 00000000
00005110  00000000 00000000                        3870+         DS    FD                gap
                                                   3871+*
00005118                                           3872+X109     DS    0F
00005118  E310 5010 0014                00000010   3873+         LGF   R1,V2ADDR         load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

0000511E  E761 0000 0806                00000000  3874+         VL    v22,0(R1)         use v22 to test decoder
00005124  E310 5014 0014                00000014  3875+         LGF   R1,V3ADDR         load v3 source
0000512A  E771 0000 0806                00000000  3876+         VL    v23,0(R1)         use v23 to test decoder
00005130  E766 7000 0EA6                          3877+         VME   V22,V22,V23,0      test instruction (dest is a source)
00005136  E760 5028 080E                00005100  3878+         VST   V22,V1O109         save v1 output
0000513C  07FB                                    3879+         BR    R11               return
00005140                                          3880+RE109    DC    0F                xl16 expected result
00005140                                          3881+         DROP  R5
00005140  00010009 00190031                       3882          DC    XL16'0001000900190031 00510079009C00D2'   result
00005148  00510079 009C00D2
00005150  FF020304 05060750                       3883          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005158  090A0B78 0C0D0EFD
00005160  FF020304 05060750                       3884          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00005168  090A0B78 0D0E0FFD
                                                  3885
                                                  3886          VRR_C VME,0
00005170                                          3887+         DS    0FD
00005170                      00005170            3888+         USING *,R5              base for test data and test routine
00005170  000051B0                                3889+T110     DC    A(X110)           address of test routine
00005174  006E                                    3890+         DC    H'110'            test number
00005176  00                                      3891+         DC    X'00'
00005177  00                                      3892+         DC    HL1'0'            m4
00005178  E5D4C540 40404040                       3893+         DC    CL8'VME'          instruction name
00005180  000051E8                                3894+         DC    A(RE110+16)       address of v2 source
00005184  000051F8                                3895+         DC    A(RE110+32)       address of v3 source
00005188  00000010                                3896+         DC    A(16)             result length
0000518C  000051D8                                3897+REA110   DC    A(RE110)          result address
00005190  00000000 00000000                       3898+         DS    FD                gap
00005198  00000000 00000000                       3899+V1O110   DS    XL16              V1 output
000051A0  00000000 00000000
000051A8  00000000 00000000                       3900+         DS    FD                gap
                                                  3901+*
000051B0                                          3902+X110     DS    0F
000051B0  E310 5010 0014                00000010  3903+         LGF   R1,V2ADDR         load v2 source
000051B6  E761 0000 0806                00000000  3904+         VL    v22,0(R1)         use v22 to test decoder
000051BC  E310 5014 0014                00000014  3905+         LGF   R1,V3ADDR         load v3 source
000051C2  E771 0000 0806                00000000  3906+         VL    v23,0(R1)         use v23 to test decoder
000051C8  E766 7000 0EA6                          3907+         VME   V22,V22,V23,0      test instruction (dest is a source)
000051CE  E760 5028 080E                00005198  3908+         VST   V22,V1O110         save v1 output
000051D4  07FB                                    3909+         BR    R11               return
000051D8                                          3910+RE110    DC    0F                xl16 expected result
000051D8                                          3911+         DROP  R5
000051D8  00010003 000A0015                       3912          DC    XL16'00010003000A0015 0024003700480062'   result
000051E0  00240037 00480062
000051E8  FF020304 05060750                       3913          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000051F0  090A0B78 0C0D0EFD
000051F8  FF010102 02030328                       3914          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00005200  0405053C 060707FE
                                                  3915
                                                  3916          VRR_C VME,0
00005208                                          3917+         DS    0FD
00005208                      00005208            3918+         USING *,R5              base for test data and test routine
00005208  00005248                                3919+T111     DC    A(X111)           address of test routine
0000520C  006F                                    3920+         DC    H'111'            test number
0000520E  00                                      3921+         DC    X'00'
0000520F  00                                      3922+         DC    HL1'0'            m4
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005210  E5D4C540 40404040                        3923+         DC    CL8'VME'          instruction name
00005218  00005280                                 3924+         DC    A(RE111+16)       address of v2 source
0000521C  00005290                                 3925+         DC    A(RE111+32)       address of v3 source
00005220  00000010                                 3926+         DC    A(16)             result length
00005224  00005270                                 3927+REA111   DC    A(RE111)          result address
00005228  00000000 00000000                        3928+         DS    FD                gap
00005230  00000000 00000000                        3929+V1O111   DS    XL16              V1 output
00005238  00000000 00000000
00005240  00000000 00000000                        3930+         DS    FD                gap
                                                   3931+*
00005248                                           3932+X111     DS    0F
00005248  E310 5010 0014                 00000010  3933+         LGF   R1,V2ADDR         load v2 source
0000524E  E761 0000 0806                 00000000  3934+         VL    v22,0(R1)         use v22 to test decoder
00005254  E310 5014 0014                 00000014  3935+         LGF   R1,V3ADDR         load v3 source
0000525A  E771 0000 0806                 00000000  3936+         VL    v23,0(R1)         use v23 to test decoder
00005260  E766 7000 0EA6                           3937+         VME   V22,V22,V23,0      test instruction (dest is a source)
00005266  E760 5028 080E                 00005230  3938+         VST   V22,V1O111         save v1 output
0000526C  07FB                                     3939+         BR    R11               return
00005270                                           3940+RE111    DC    0F                xl16 expected result
00005270                                           3941+         DROP  R5
00005270  00010000 00000000                        3942          DC    XL16'0001000000000000 0009000B000C000E'   result
00005278  0009000B 000C000E
00005280  FF020304 05060750                        3943          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005288  090A0B78 0C0D0EFD
00005290  FF000000 0000000A                        3944          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00005298  0101010F 010101FF
                                                   3945
                                                   3946 * Halfword
                                                   3947          VRR_C VME,1
000052A0                                           3948+         DS    0FD
000052A0                      000052A0             3949+         USING *,R5              base for test data and test routine
000052A0  000052E0                                 3950+T112     DC    A(X112)           address of test routine
000052A4  0070                                     3951+         DC    H'112'            test number
000052A6  00                                       3952+         DC    X'00'
000052A7  01                                       3953+         DC    HL1'1'            m4
000052A8  E5D4C540 40404040                        3954+         DC    CL8'VME'          instruction name
000052B0  00005318                                 3955+         DC    A(RE112+16)       address of v2 source
000052B4  00005328                                 3956+         DC    A(RE112+32)       address of v3 source
000052B8  00000010                                 3957+         DC    A(16)             result length
000052BC  00005308                                 3958+REA112   DC    A(RE112)          result address
000052C0  00000000 00000000                        3959+         DS    FD                gap
000052C8  00000000 00000000                        3960+V1O112   DS    XL16              V1 output
000052D0  00000000 00000000
000052D8  00000000 00000000                        3961+         DS    FD                gap
                                                   3962+*
000052E0                                           3963+X112     DS    0F
000052E0  E310 5010 0014                 00000010  3964+         LGF   R1,V2ADDR         load v2 source
000052E6  E761 0000 0806                 00000000  3965+         VL    v22,0(R1)         use v22 to test decoder
000052EC  E310 5014 0014                 00000014  3966+         LGF   R1,V3ADDR         load v3 source
000052F2  E771 0000 0806                 00000000  3967+         VL    v23,0(R1)         use v23 to test decoder
000052F8  E766 7000 1EA6                           3968+         VME   V22,V22,V23,1      test instruction (dest is a source)
000052FE  E760 5028 080E                 000052C8  3969+         VST   V22,V1O112         save v1 output
00005304  07FB                                     3970+         BR    R11               return
00005308                                           3971+RE112    DC    0F                xl16 expected result
00005308                                           3972+         DROP  R5
00005308  00000001 00000000                        3973          DC    XL16'0000000100000000 00000C40F8000000'   result
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005310  00000C40 F8000000
00005318  FFFF0000 00000019                         3974          DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00005320  00380000 1000EEFA
00005328  FFFF0000 00000019                         3975          DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00005330  00380003 8000EEFA
                                                    3976
                                                    3977          VRR_C VME,1
00005338                                            3978+         DS    0FD
00005338                      00005338              3979+         USING *,R5              base for test data and test routine
00005338  00005378                                  3980+T113     DC    A(X113)           address of test routine
0000533C  0071                                      3981+         DC    H'113'            test number
0000533E  00                                        3982+         DC    X'00'
0000533F  01                                        3983+         DC    HL1'1'            m4
00005340  E5D4C540 40404040                         3984+         DC    CL8'VME'          instruction name
00005348  000053B0                                  3985+         DC    A(RE113+16)       address of v2 source
0000534C  000053C0                                  3986+         DC    A(RE113+32)       address of v3 source
00005350  00000010                                  3987+         DC    A(16)             result length
00005354  000053A0                                  3988+REA113   DC    A(RE113)          result address
00005358  00000000 00000000                         3989+         DS    FD                gap
00005360  00000000 00000000                         3990+V1O113   DS    XL16              V1 output
00005368  00000000 00000000
00005370  00000000 00000000                         3991+         DS    FD                gap
                                                    3992+*
00005378                                            3993+X113     DS    0F
00005378  E310 5010 0014                 00000010   3994+         LGF   R1,V2ADDR         load v2 source
0000537E  E761 0000 0806                 00000000   3995+         VL    v22,0(R1)         use v22 to test decoder
00005384  E310 5014 0014                 00000014   3996+         LGF   R1,V3ADDR         load v3 source
0000538A  E771 0000 0806                 00000000   3997+         VL    v23,0(R1)         use v23 to test decoder
00005390  E766 7000 1EA6                            3998+         VME   V22,V22,V23,1      test instruction (dest is a source)
00005396  E760 5028 080E                 00005360   3999+         VST   V22,V1O113         save v1 output
0000539C  07FB                                      4000+         BR    R11               return
000053A0                                            4001+RE113    DC    0F                xl16 expected result
000053A0                                            4002+         DROP  R5
000053A0  0000FC04 00193C24                         4003          DC    XL16'0000FC0400193C24 0051B464009D51B6'   result
000053A8  0051B464 009D51B6
000053B0  FF020304 05060750                         4004          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000053B8  090A0B78 0C0D0EFD
000053C0  FF020304 05060750                         4005          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
000053C8  090A0B78 0D0E0FFD
                                                    4006
                                                    4007          VRR_C VME,1
000053D0                                            4008+         DS    0FD
000053D0                      000053D0              4009+         USING *,R5              base for test data and test routine
000053D0  00005410                                  4010+T114     DC    A(X114)           address of test routine
000053D4  0072                                      4011+         DC    H'114'            test number
000053D6  00                                        4012+         DC    X'00'
000053D7  01                                        4013+         DC    HL1'1'            m4
000053D8  E5D4C540 40404040                         4014+         DC    CL8'VME'          instruction name
000053E0  00005448                                  4015+         DC    A(RE114+16)       address of v2 source
000053E4  00005458                                  4016+         DC    A(RE114+32)       address of v3 source
000053E8  00000010                                  4017+         DC    A(16)             result length
000053EC  00005438                                  4018+REA114   DC    A(RE114)          result address
000053F0  00000000 00000000                         4019+         DS    FD                gap
000053F8  00000000 00000000                         4020+V1O114   DS    XL16              V1 output
00005400  00000000 00000000
00005408  00000000 00000000                         4021+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   4022+*
00005410                                           4023+X114     DS    0F
00005410  E310 5010 0014                 00000010  4024+         LGF   R1,V2ADDR         load v2 source
00005416  E761 0000 0806                 00000000  4025+         VL    v22,0(R1)         use v22 to test decoder
0000541C  E310 5014 0014                 00000014  4026+         LGF   R1,V3ADDR         load v3 source
00005422  E771 0000 0806                 00000000  4027+         VL    v23,0(R1)         use v23 to test decoder
00005428  E766 7000 1EA6                           4028+         VME   V22,V22,V23,1      test instruction (dest is a source)
0000542E  E760 5028 080E                 000053F8  4029+         VST   V22,V1O114         save v1 output
00005434  07FB                                     4030+         BR    R11               return
00005438                                           4031+RE114    DC    0F                xl16 expected result
00005438                                           4032+         DROP  R5
00005438  0000FD02 000A1B12                        4033          DC    XL16'0000FD02000A1B12 002455320048A25B'   result
00005440  00245532 0048A25B
00005448  FF020304 05060750                        4034          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005450  090A0B78 0C0D0EFD
00005458  FF010102 02030328                        4035          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00005460  0405053C 060707FE
                                                   4036
                                                   4037          VRR_C VME,1
00005468                                           4038+         DS    0FD
00005468                         00005468          4039+         USING *,R5              base for test data and test routine
00005468  000054A8                                 4040+T115     DC    A(X115)           address of test routine
0000546C  0073                                     4041+         DC    H'115'            test number
0000546E  00                                       4042+         DC    X'00'
0000546F  01                                       4043+         DC    HL1'1'            m4
00005470  E5D4C540 40404040                        4044+         DC    CL8'VME'          instruction name
00005478  000054E0                                 4045+         DC    A(RE115+16)       address of v2 source
0000547C  000054F0                                 4046+         DC    A(RE115+32)       address of v3 source
00005480  00000010                                 4047+         DC    A(16)             result length
00005484  000054D0                                 4048+REA115   DC    A(RE115)          result address
00005488  00000000 00000000                        4049+         DS    FD                gap
00005490  00000000 00000000                        4050+V1O115   DS    XL16              V1 output
00005498  00000000 00000000
000054A0  00000000 00000000                        4051+         DS    FD                gap
                                                   4052+*
000054A8                                           4053+X115     DS    0F
000054A8  E310 5010 0014                 00000010  4054+         LGF   R1,V2ADDR         load v2 source
000054AE  E761 0000 0806                 00000000  4055+         VL    v22,0(R1)         use v22 to test decoder
000054B4  E310 5014 0014                 00000014  4056+         LGF   R1,V3ADDR         load v3 source
000054BA  E771 0000 0806                 00000000  4057+         VL    v23,0(R1)         use v23 to test decoder
000054C0  E766 7000 1EA6                           4058+         VME   V22,V22,V23,1      test instruction (dest is a source)
000054C6  E760 5028 080E                 00005490  4059+         VST   V22,V1O115         save v1 output
000054CC  07FB                                     4060+         BR    R11               return
000054D0                                           4061+RE115    DC    0F                xl16 expected result
000054D0                                           4062+         DROP  R5
000054D0  0000FE00 00000000                        4063          DC    XL16'0000FE0000000000 0009130A000C190D'   result
000054D8  0009130A 000C190D
000054E0  FF020304 05060750                        4064          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
000054E8  090A0B78 0C0D0EFD
000054F0  FF000000 0000000A                        4065          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
000054F8  0101010F 010101FF
                                                   4066
                                                   4067 * Word
                                                   4068          VRR_C VME,2
00005500                                           4069+         DS    0FD
00005500                         00005500          4070+         USING *,R5              base for test data and test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005500  00005540                                 4071+T116     DC    A(X116)           address of test routine
00005504  0074                                     4072+         DC    H'116'            test number
00005506  00                                       4073+         DC    X'00'
00005507  02                                       4074+         DC    HL1'2'            m4
00005508  E5D4C540 40404040                        4075+         DC    CL8'VME'          instruction name
00005510  00005578                                 4076+         DC    A(RE116+16)       address of v2 source
00005514  00005588                                 4077+         DC    A(RE116+32)       address of v3 source
00005518  00000010                                 4078+         DC    A(16)             result length
0000551C  00005568                                 4079+REA116   DC    A(RE116)          result address
00005520  00000000 00000000                        4080+         DS    FD                gap
00005528  00000000 00000000                        4081+V1O116   DS    XL16              V1 output
00005530  00000000 00000000
00005538  00000000 00000000                        4082+         DS    FD                gap
                                                   4083+*
00005540                                           4084+X116     DS    0F
00005540  E310 5010 0014                 00000010  4085+         LGF   R1,V2ADDR         load v2 source
00005546  E761 0000 0806                 00000000  4086+         VL    v22,0(R1)         use v22 to test decoder
0000554C  E310 5014 0014                 00000014  4087+         LGF   R1,V3ADDR         load v3 source
00005552  E771 0000 0806                 00000000  4088+         VL    v23,0(R1)         use v23 to test decoder
00005558  E766 7000 2EA6                           4089+         VME   V22,V22,V23,2      test instruction (dest is a source)
0000555E  E760 5028 080E                 00005528  4090+         VST   V22,V1O116         save v1 output
00005564  07FB                                     4091+         BR    R11               return
00005568                                           4092+RE116    DC    0F                xl16 expected result
00005568                                           4093+         DROP  R5
00005568  00000000 00000001                        4094          DC    XL16'0000000000000001 0000000000000C40'   result
00005570  00000000 00000C40
00005578  FFFFFFFF 00019000                        4095          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00005580  00000038 EEEEEEFA
00005588  FFFFFFFF 00019000                        4096          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00005590  00000038 0EEEEEFA
                                                   4097
                                                   4098          VRR_C VME,2
00005598                                           4099+         DS    0FD
00005598                      00005598             4100+         USING *,R5              base for test data and test routine
00005598  000055D8                                 4101+T117     DC    A(X117)           address of test routine
0000559C  0075                                     4102+         DC    H'117'            test number
0000559E  00                                       4103+         DC    X'00'
0000559F  02                                       4104+         DC    HL1'2'            m4
000055A0  E5D4C540 40404040                        4105+         DC    CL8'VME'          instruction name
000055A8  00005610                                 4106+         DC    A(RE117+16)       address of v2 source
000055AC  00005620                                 4107+         DC    A(RE117+32)       address of v3 source
000055B0  00000010                                 4108+         DC    A(16)             result length
000055B4  00005600                                 4109+REA117   DC    A(RE117)          result address
000055B8  00000000 00000000                        4110+         DS    FD                gap
000055C0  00000000 00000000                        4111+V1O117   DS    XL16              V1 output
000055C8  00000000 00000000
000055D0  00000000 00000000                        4112+         DS    FD                gap
                                                   4113+*
000055D8                                           4114+X117     DS    0F
000055D8  E310 5010 0014                 00000010  4115+         LGF   R1,V2ADDR         load v2 source
000055DE  E761 0000 0806                 00000000  4116+         VL    v22,0(R1)         use v22 to test decoder
000055E4  E310 5014 0014                 00000014  4117+         LGF   R1,V3ADDR         load v3 source
000055EA  E771 0000 0806                 00000000  4118+         VL    v23,0(R1)         use v23 to test decoder
000055F0  E766 7000 2EA6                           4119+         VME   V22,V22,V23,2      test instruction (dest is a source)
000055F6  E760 5028 080E                 000055C0  4120+         VST   V22,V1O117         save v1 output
000055FC  07FB                                     4121+         BR    R11               return
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005600                                           4122+RE117    DC    0F                xl16 expected result
00005600                                           4123+         DROP  R5
00005600  FFFF0004 0C191810                        4124          DC    XL16'FFFF00040C191810 0051B52F85A6B1A0'   result
00005608  0051B52F 85A6B1A0
00005610  FF020304 05060750                        4125          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00005618  090A0B0C 0D0E0F7F
00005620  01020304 05060750                        4126          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00005628  090A0B78 0D0E0F7F
                                                   4127
                                                   4128          VRR_C VME,2
00005630                                           4129+         DS    0FD
00005630                      00005630             4130+         USING *,R5              base for test data and test routine
00005630  00005670                                 4131+T118     DC    A(X118)           address of test routine
00005634  0076                                     4132+         DC    H'118'            test number
00005636  00                                       4133+         DC    X'00'
00005637  02                                       4134+         DC    HL1'2'            m4
00005638  E5D4C540 40404040                        4135+         DC    CL8'VME'          instruction name
00005640  000056A8                                 4136+         DC    A(RE118+16)       address of v2 source
00005644  000056B8                                 4137+         DC    A(RE118+32)       address of v3 source
00005648  00000010                                 4138+         DC    A(16)             result length
0000564C  00005698                                 4139+REA118   DC    A(RE118)          result address
00005650  00000000 00000000                        4140+         DS    FD                gap
00005658  00000000 00000000                        4141+V1O118   DS    XL16              V1 output
00005660  00000000 00000000
00005668  00000000 00000000                        4142+         DS    FD                gap
                                                   4143+*
00005670                                           4144+X118     DS    0F
00005670  E310 5010 0014                00000010   4145+         LGF   R1,V2ADDR         load v2 source
00005676  E761 0000 0806                00000000   4146+         VL    v22,0(R1)         use v22 to test decoder
0000567C  E310 5014 0014                00000014   4147+         LGF   R1,V3ADDR         load v3 source
00005682  E771 0000 0806                00000000   4148+         VL    v23,0(R1)         use v23 to test decoder
00005688  E766 7000 2EA6                           4149+         VME   V22,V22,V23,2      test instruction (dest is a source)
0000568E  E760 5028 080E                00005658   4150+         VST   V22,V1O118         save v1 output
00005694  07FB                                     4151+         BR    R11               return
00005698                                           4152+RE118    DC    0F                xl16 expected result
00005698                                           4153+         DROP  R5
00005698  FFFFFF01 030B0A08                        4154          DC    XL16'FFFFFF01030B0A08 0024558DB7CDD2D0'   result
000056A0  0024558D B7CDD2D0
000056A8  FF020304 05060750                        4155          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000056B0  090A0B0C 0D0E0F7F
000056B8  00010102 02030328                        4156          DC    XL16'0001010202030328 0405053C0607073F'   v3
000056C0  0405053C 0607073F
                                                   4157
                                                   4158          VRR_C VME,2
000056C8                                           4159+         DS    0FD
000056C8                      000056C8             4160+         USING *,R5              base for test data and test routine
000056C8  00005708                                 4161+T119     DC    A(X119)           address of test routine
000056CC  0077                                     4162+         DC    H'119'            test number
000056CE  00                                       4163+         DC    X'00'
000056CF  02                                       4164+         DC    HL1'2'            m4
000056D0  E5D4C540 40404040                        4165+         DC    CL8'VME'          instruction name
000056D8  00005740                                 4166+         DC    A(RE119+16)       address of v2 source
000056DC  00005750                                 4167+         DC    A(RE119+32)       address of v3 source
000056E0  00000010                                 4168+         DC    A(16)             result length
000056E4  00005730                                 4169+REA119   DC    A(RE119)          result address
000056E8  00000000 00000000                        4170+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000056F0  00000000 00000000                        4171+V1O119   DS    XL16              V1 output
000056F8  00000000 00000000
00005700  00000000 00000000                        4172+         DS    FD                gap
                                                   4173+*
00005708                                           4174+X119     DS    0F
00005708  E310 5010 0014                 00000010  4175+         LGF   R1,V2ADDR         load v2 source
0000570E  E761 0000 0806                 00000000  4176+         VL    v22,0(R1)         use v22 to test decoder
00005714  E310 5014 0014                 00000014  4177+         LGF   R1,V3ADDR         load v3 source
0000571A  E771 0000 0806                 00000000  4178+         VL    v23,0(R1)         use v23 to test decoder
00005720  E766 7000 2EA6                           4179+         VME   V22,V22,V23,2      test instruction (dest is a source)
00005726  E760 5028 080E                 000056F0  4180+         VST   V22,V1O119         save v1 output
0000572C  07FB                                     4181+         BR    R11               return
00005730                                           4182+RE119    DC    0F                xl16 expected result
00005730                                           4183+         DROP  R5
00005730  00000000 00000000                        4184          DC    XL16'0000000000000000 0009131EA8ADB1B4'   result
00005738  0009131E A8ADB1B4
00005740  FF020304 05060750                        4185          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00005748  090A0B0C 0D0E0F7F
00005750  00000000 0000000A                        4186          DC    XL16'000000000000000A 0101010F0101010F'   v3
00005758  0101010F 0101010F
                                                   4187
                                                   4188 * Doubleword
                                                   4189          VRR_C VME,3
00005760                                           4190+         DS    0FD
00005760                         00005760          4191+         USING *,R5              base for test data and test routine
00005760  000057A0                                 4192+T120     DC    A(X120)           address of test routine
00005764  0078                                     4193+         DC    H'120'            test number
00005766  00                                       4194+         DC    X'00'
00005767  03                                       4195+         DC    HL1'3'            m4
00005768  E5D4C540 40404040                        4196+         DC    CL8'VME'          instruction name
00005770  000057D8                                 4197+         DC    A(RE120+16)       address of v2 source
00005774  000057E8                                 4198+         DC    A(RE120+32)       address of v3 source
00005778  00000010                                 4199+         DC    A(16)             result length
0000577C  000057C8                                 4200+REA120   DC    A(RE120)          result address
00005780  00000000 00000000                        4201+         DS    FD                gap
00005788  00000000 00000000                        4202+V1O120   DS    XL16              V1 output
00005790  00000000 00000000
00005798  00000000 00000000                        4203+         DS    FD                gap
                                                   4204+*
000057A0                                           4205+X120     DS    0F
000057A0  E310 5010 0014                 00000010  4206+         LGF   R1,V2ADDR         load v2 source
000057A6  E761 0000 0806                 00000000  4207+         VL    v22,0(R1)         use v22 to test decoder
000057AC  E310 5014 0014                 00000014  4208+         LGF   R1,V3ADDR         load v3 source
000057B2  E771 0000 0806                 00000000  4209+         VL    v23,0(R1)         use v23 to test decoder
000057B8  E766 7000 3EA6                           4210+         VME   V22,V22,V23,3      test instruction (dest is a source)
000057BE  E760 5028 080E                 00005788  4211+         VST   V22,V1O120         save v1 output
000057C4  07FB                                     4212+         BR    R11               return
000057C8                                           4213+RE120    DC    0F                xl16 expected result
000057C8                                           4214+         DROP  R5
000057C8  00000000 00000000                        4215          DC    XL16'0000000000000000 FFFCE00271000000'   result
000057D0  FFFCE002 71000000
000057D8  FFFFFFFF 00019000                        4216          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000057E0  00000038 EEEEEEFA
000057E8  FFFFFFFF 00019000                        4217          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
000057F0  00000038 0EEEEEFA
                                                   4218
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   4219          VRR_C VME,3
000057F8                                           4220+         DS    0FD
000057F8                     000057F8              4221+         USING *,R5              base for test data and test routine
000057F8  00005838                                 4222+T121     DC    A(X121)           address of test routine
000057FC  0079                                     4223+         DC    H'121'            test number
000057FE  00                                       4224+         DC    X'00'
000057FF  03                                       4225+         DC    HL1'3'            m4
00005800  E5D4C540 40404040                        4226+         DC    CL8'VME'          instruction name
00005808  00005870                                 4227+         DC    A(RE121+16)       address of v2 source
0000580C  00005880                                 4228+         DC    A(RE121+32)       address of v3 source
00005810  00000010                                 4229+         DC    A(16)             result length
00005814  00005860                                 4230+REA121   DC    A(RE121)          result address
00005818  00000000 00000000                        4231+         DS    FD                gap
00005820  00000000 00000000                        4232+V1O121   DS    XL16              V1 output
00005828  00000000 00000000
00005830  00000000 00000000                        4233+         DS    FD                gap
                                                   4234+*
00005838                                           4235+X121     DS    0F
00005838  E310 5010 0014                00000010   4236+         LGF   R1,V2ADDR         load v2 source
0000583E  E761 0000 0806                00000000   4237+         VL    v22,0(R1)         use v22 to test decoder
00005844  E310 5014 0014                00000014   4238+         LGF   R1,V3ADDR         load v3 source
0000584A  E771 0000 0806                00000000   4239+         VL    v23,0(R1)         use v23 to test decoder
00005850  E766 7000 3EA6                           4240+         VME   V22,V22,V23,3      test instruction (dest is a source)
00005856  E760 5028 080E                00005820   4241+         VST   V22,V1O121         save v1 output
0000585C  07FB                                     4242+         BR    R11               return
00005860                                           4243+RE121    DC    0F                xl16 expected result
00005860                                           4244+         DROP  R5
00005860  FFFF0004 0C192C46                        4245          DC    XL16'FFFF00040C192C46 69B556ED77F57900'   result
00005868  69B556ED 77F57900
00005870  FF020304 05060750                        4246          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00005878  090A0B0C 0D0E0F7F
00005880  01020304 05060750                        4247          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
00005888  090A0B78 0D0E0F7F
                                                   4248
                                                   4249          VRR_C VME,3
00005890                                           4250+         DS    0FD
00005890                     00005890              4251+         USING *,R5              base for test data and test routine
00005890  000058D0                                 4252+T122     DC    A(X122)           address of test routine
00005894  007A                                     4253+         DC    H'122'            test number
00005896  00                                       4254+         DC    X'00'
00005897  03                                       4255+         DC    HL1'3'            m4
00005898  E5D4C540 40404040                        4256+         DC    CL8'VME'          instruction name
000058A0  00005908                                 4257+         DC    A(RE122+16)       address of v2 source
000058A4  00005918                                 4258+         DC    A(RE122+32)       address of v3 source
000058A8  00000010                                 4259+         DC    A(16)             result length
000058AC  000058F8                                 4260+REA122   DC    A(RE122)          result address
000058B0  00000000 00000000                        4261+         DS    FD                gap
000058B8  00000000 00000000                        4262+V1O122   DS    XL16              V1 output
000058C0  00000000 00000000
000058C8  00000000 00000000                        4263+         DS    FD                gap
                                                   4264+*
000058D0                                           4265+X122     DS    0F
000058D0  E310 5010 0014                00000010   4266+         LGF   R1,V2ADDR         load v2 source
000058D6  E761 0000 0806                00000000   4267+         VL    v22,0(R1)         use v22 to test decoder
000058DC  E310 5014 0014                00000014   4268+         LGF   R1,V3ADDR         load v3 source
000058E2  E771 0000 0806                00000000   4269+         VL    v23,0(R1)         use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000058E8  E766 7000 3EA6                           4270+         VME   V22,V22,V23,3      test instruction (dest is a source)
000058EE  E760 5028 080E                 000058B8  4271+         VST   V22,V1O122         save v1 output
000058F4  07FB                                     4272+         BR    R11               return
000058F8                                           4273+RE122    DC    0F                xl16 expected result
000058F8                                           4274+         DROP  R5
000058F8  FFFFFF01 0309101C                        4275          DC    XL16'FFFFFF010309101C 06D2FE7090F71480'   result
00005900  06D2FE70 90F71480
00005908  FF020304 05060750                        4276          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00005910  090A0B0C 0D0E0F7F
00005918  00010102 02030328                        4277          DC    XL16'0001010202030328 0405053C0607073F'   v3
00005920  0405053C 0607073F
                                                   4278
                                                   4279          VRR_C VME,3
00005928                                           4280+         DS    0FD
00005928                       00005928            4281+         USING *,R5              base for test data and test routine
00005928  00005968                                 4282+T123     DC    A(X123)           address of test routine
0000592C  007B                                     4283+         DC    H'123'            test number
0000592E  00                                       4284+         DC    X'00'
0000592F  03                                       4285+         DC    HL1'3'            m4
00005930  E5D4C540 40404040                        4286+         DC    CL8'VME'          instruction name
00005938  000059A0                                 4287+         DC    A(RE123+16)       address of v2 source
0000593C  000059B0                                 4288+         DC    A(RE123+32)       address of v3 source
00005940  00000010                                 4289+         DC    A(16)             result length
00005944  00005990                                 4290+REA123   DC    A(RE123)          result address
00005948  00000000 00000000                        4291+         DS    FD                gap
00005950  00000000 00000000                        4292+V1O123   DS    XL16              V1 output
00005958  00000000 00000000
00005960  00000000 00000000                        4293+         DS    FD                gap
                                                   4294+*
00005968                                           4295+X123     DS    0F
00005968  E310 5010 0014                 00000010  4296+         LGF   R1,V2ADDR         load v2 source
0000596E  E761 0000 0806                 00000000  4297+         VL    v22,0(R1)         use v22 to test decoder
00005974  E310 5014 0014                 00000014  4298+         LGF   R1,V3ADDR         load v3 source
0000597A  E771 0000 0806                 00000000  4299+         VL    v23,0(R1)         use v23 to test decoder
00005980  E766 7000 3EA6                           4300+         VME   V22,V22,V23,3      test instruction (dest is a source)
00005986  E760 5028 080E                 00005950  4301+         VST   V22,V1O123         save v1 output
0000598C  07FB                                     4302+         BR    R11               return
00005990                                           4303+RE123    DC    0F                xl16 expected result
00005990                                           4304+         DROP  R5
00005990  FFFFFFFF FFFFFFFF                        4305          DC    XL16'FFFFFFFFFFFFFFFF F6141E28323C4920'   result
00005998  F6141E28 323C4920
000059A0  FF020304 05060750                        4306          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000059A8  090A0B0C 0D0E0F7F
000059B0  00000000 0000000A                        4307          DC    XL16'000000000000000A 0101010F0101010F'   v3
000059B8  0101010F 0101010F
                                                   4308
                                                   4309          VRR_C VME,3
000059C0                                           4310+         DS    0FD
000059C0                       000059C0            4311+         USING *,R5              base for test data and test routine
000059C0  00005A00                                 4312+T124     DC    A(X124)           address of test routine
000059C4  007C                                     4313+         DC    H'124'            test number
000059C6  00                                       4314+         DC    X'00'
000059C7  03                                       4315+         DC    HL1'3'            m4
000059C8  E5D4C540 40404040                        4316+         DC    CL8'VME'          instruction name
000059D0  00005A38                                 4317+         DC    A(RE124+16)       address of v2 source
000059D4  00005A48                                 4318+         DC    A(RE124+32)       address of v3 source
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000059D8  00000010                                 4319+         DC    A(16)              result length
000059DC  00005A28                                 4320+REA124   DC    A(RE124)           result address
000059E0  00000000 00000000                        4321+         DS    FD                 gap
000059E8  00000000 00000000                        4322+V1O124   DS    XL16               V1 output
000059F0  00000000 00000000
000059F8  00000000 00000000                        4323+         DS    FD                 gap
                                                   4324+*
00005A00                                           4325+X124     DS    0F
00005A00  E310 5010 0014                 00000010  4326+         LGF   R1,V2ADDR          load v2 source
00005A06  E761 0000 0806                 00000000  4327+         VL    v22,0(R1)          use v22 to test decoder
00005A0C  E310 5014 0014                 00000014  4328+         LGF   R1,V3ADDR          load v3 source
00005A12  E771 0000 0806                 00000000  4329+         VL    v23,0(R1)          use v23 to test decoder
00005A18  E766 7000 3EA6                           4330+         VME   V22,V22,V23,3       test instruction (dest is a source)
00005A1E  E760 5028 080E                 000059E8  4331+         VST   V22,V1O124          save v1 output
00005A24  07FB                                     4332+         BR    R11                return
00005A28                                           4333+RE124    DC    0F                 xl16 expected result
00005A28                                           4334+         DROP  R5
00005A28  0009131E A8C3DFFE                        4335          DC    XL16'0009131EA8C3DFFE 091C345060616771'   result
00005A30  091C3450 60616771
00005A38  090A0B0C 0D0E0F7F                        4336          DC    XL16'090A0B0C0D0E0F7F FF02030405060750'   v2
00005A40  FF020304 05060750
00005A48  0101010F 0101010F                        4337          DC    XL16'0101010F0101010F 000000000000000A'   v3
00005A50  00000000 0000000A
                                                   4338
                                                   4339 *-------------------------------------------------------------------
                                                   4340 *  VMO    - Vector Multiply Odd
                                                   4341 *-------------------------------------------------------------------
                                                   4342 * Byte
                                                   4343          VRR_C VMO,0
00005A58                                           4344+         DS    0FD
00005A58                      00005A58             4345+         USING *,R5               base for test data and test routine
00005A58  00005A98                                 4346+T125     DC    A(X125)            address of test routine
00005A5C  007D                                     4347+         DC    H'125'             test number
00005A5E  00                                       4348+         DC    X'00'
00005A5F  00                                       4349+         DC    HL1'0'             m4
00005A60  E5D4D640 40404040                        4350+         DC    CL8'VMO'           instruction name
00005A68  00005AD0                                 4351+         DC    A(RE125+16)        address of v2 source
00005A6C  00005AE0                                 4352+         DC    A(RE125+32)        address of v3 source
00005A70  00000010                                 4353+         DC    A(16)              result length
00005A74  00005AC0                                 4354+REA125   DC    A(RE125)           result address
00005A78  00000000 00000000                        4355+         DS    FD                 gap
00005A80  00000000 00000000                        4356+V1O125   DS    XL16               V1 output
00005A88  00000000 00000000
00005A90  00000000 00000000                        4357+         DS    FD                 gap
                                                   4358+*
00005A98                                           4359+X125     DS    0F
00005A98  E310 5010 0014                 00000010  4360+         LGF   R1,V2ADDR          load v2 source
00005A9E  E761 0000 0806                 00000000  4361+         VL    v22,0(R1)          use v22 to test decoder
00005AA4  E310 5014 0014                 00000014  4362+         LGF   R1,V3ADDR          load v3 source
00005AAA  E771 0000 0806                 00000000  4363+         VL    v23,0(R1)          use v23 to test decoder
00005AB0  E766 7000 0EA7                           4364+         VMO   V22,V22,V23,0       test instruction (dest is a source)
00005AB6  E760 5028 080E                 00005A80  4365+         VST   V22,V1O125          save v1 output
00005ABC  07FB                                     4366+         BR    R11                return
00005AC0                                           4367+RE125    DC    0F                 xl16 expected result
00005AC0                                           4368+         DROP  R5
00005AC0  00000000 00000271                        4369          DC    XL16'0000000000000271 0000000000000024'   result
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005AC8  00000000 00000024
00005AD0  FF000000 00000019                         4370          DC    XL16'FF00000000000019 38000000000000FA'   v2
00005AD8  38000000 000000FA
00005AE0  FF000000 00000019                         4371          DC    XL16'FF00000000000019 38000000000000FA'   v3
00005AE8  38000000 000000FA
                                                    4372
                                                    4373          VRR_C VMO,0
00005AF0                                            4374+         DS    0FD
00005AF0                      00005AF0              4375+         USING *,R5              base for test data and test routine
00005AF0  00005B30                                  4376+T126     DC    A(X126)           address of test routine
00005AF4  007E                                      4377+         DC    H'126'            test number
00005AF6  00                                        4378+         DC    X'00'
00005AF7  00                                        4379+         DC    HL1'0'            m4
00005AF8  E5D4D640 40404040                         4380+         DC    CL8'VMO'          instruction name
00005B00  00005B68                                  4381+         DC    A(RE126+16)       address of v2 source
00005B04  00005B78                                  4382+         DC    A(RE126+32)       address of v3 source
00005B08  00000010                                  4383+         DC    A(16)             result length
00005B0C  00005B58                                  4384+REA126   DC    A(RE126)          result address
00005B10  00000000 00000000                         4385+         DS    FD                gap
00005B18  00000000 00000000                         4386+V1O126   DS    XL16              V1 output
00005B20  00000000 00000000
00005B28  00000000 00000000                         4387+         DS    FD                gap
                                                    4388+*
00005B30                                            4389+X126     DS    0F
00005B30  E310 5010 0014                00000010    4390+         LGF   R1,V2ADDR         load v2 source
00005B36  E761 0000 0806                00000000    4391+         VL    v22,0(R1)         use v22 to test decoder
00005B3C  E310 5014 0014                00000014    4392+         LGF   R1,V3ADDR         load v3 source
00005B42  E771 0000 0806                00000000    4393+         VL    v23,0(R1)         use v23 to test decoder
00005B48  E766 7000 0EA7                            4394+         VMO   V22,V22,V23,0      test instruction (dest is a source)
00005B4E  E760 5028 080E                00005B18    4395+         VST   V22,V1O126         save v1 output
00005B54  07FB                                      4396+         BR    R11               return
00005B58                                            4397+RE126    DC    0F                xl16 expected result
00005B58                                            4398+         DROP  R5
00005B58  00040010 00241900                         4399          DC    XL16'0004001000241900 0064384000B60009'   result
00005B60  00643840 00B60009
00005B68  FF020304 05060750                         4400          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005B70  090A0B78 0C0D0EFD
00005B78  FF020304 05060750                         4401          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00005B80  090A0B78 0D0E0FFD
                                                    4402
                                                    4403          VRR_C VMO,0
00005B88                                            4404+         DS    0FD
00005B88                      00005B88              4405+         USING *,R5              base for test data and test routine
00005B88  00005BC8                                  4406+T127     DC    A(X127)           address of test routine
00005B8C  007F                                      4407+         DC    H'127'            test number
00005B8E  00                                        4408+         DC    X'00'
00005B8F  00                                        4409+         DC    HL1'0'            m4
00005B90  E5D4D640 40404040                         4410+         DC    CL8'VMO'          instruction name
00005B98  00005C00                                  4411+         DC    A(RE127+16)       address of v2 source
00005B9C  00005C10                                  4412+         DC    A(RE127+32)       address of v3 source
00005BA0  00000010                                  4413+         DC    A(16)             result length
00005BA4  00005BF0                                  4414+REA127   DC    A(RE127)          result address
00005BA8  00000000 00000000                         4415+         DS    FD                gap
00005BB0  00000000 00000000                         4416+V1O127   DS    XL16              V1 output
00005BB8  00000000 00000000
00005BC0  00000000 00000000                         4417+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   4418+*
00005BC8                                           4419+X127     DS    0F
00005BC8  E310 5010 0014                 00000010  4420+         LGF   R1,V2ADDR         load v2 source
00005BCE  E761 0000 0806                 00000000  4421+         VL    v22,0(R1)         use v22 to test decoder
00005BD4  E310 5014 0014                 00000014  4422+         LGF   R1,V3ADDR         load v3 source
00005BDA  E771 0000 0806                 00000000  4423+         VL    v23,0(R1)         use v23 to test decoder
00005BE0  E766 7000 0EA7                           4424+         VMO   V22,V22,V23,0      test instruction (dest is a source)
00005BE6  E760 5028 080E                 00005BB0  4425+         VST   V22,V1O127         save v1 output
00005BEC  07FB                                     4426+         BR    R11               return
00005BF0                                           4427+RE127    DC    0F                xl16 expected result
00005BF0                                           4428+         DROP  R5
00005BF0  00020008 00120C80                        4429          DC    XL16'0002000800120C80 00321C20005B0006'   result
00005BF8  00321C20 005B0006
00005C00  FF020304 05060750                        4430          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005C08  090A0B78 0C0D0EFD
00005C10  FF010102 02030328                        4431          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00005C18  0405053C 060707FE
                                                   4432
                                                   4433          VRR_C VMO,0
00005C20                                           4434+         DS    0FD
00005C20                      00005C20             4435+         USING *,R5              base for test data and test routine
00005C20  00005C60                                 4436+T128     DC    A(X128)           address of test routine
00005C24  0080                                     4437+         DC    H'128'            test number
00005C26  00                                       4438+         DC    X'00'
00005C27  00                                       4439+         DC    HL1'0'            m4
00005C28  E5D4D640 40404040                        4440+         DC    CL8'VMO'          instruction name
00005C30  00005C98                                 4441+         DC    A(RE128+16)       address of v2 source
00005C34  00005CA8                                 4442+         DC    A(RE128+32)       address of v3 source
00005C38  00000010                                 4443+         DC    A(16)             result length
00005C3C  00005C88                                 4444+REA128   DC    A(RE128)          result address
00005C40  00000000 00000000                        4445+         DS    FD                gap
00005C48  00000000 00000000                        4446+V1O128   DS    XL16              V1 output
00005C50  00000000 00000000
00005C58  00000000 00000000                        4447+         DS    FD                gap
                                                   4448+*
00005C60                                           4449+X128     DS    0F
00005C60  E310 5010 0014                 00000010  4450+         LGF   R1,V2ADDR         load v2 source
00005C66  E761 0000 0806                 00000000  4451+         VL    v22,0(R1)         use v22 to test decoder
00005C6C  E310 5014 0014                 00000014  4452+         LGF   R1,V3ADDR         load v3 source
00005C72  E771 0000 0806                 00000000  4453+         VL    v23,0(R1)         use v23 to test decoder
00005C78  E766 7000 0EA7                           4454+         VMO   V22,V22,V23,0      test instruction (dest is a source)
00005C7E  E760 5028 080E                 00005C48  4455+         VST   V22,V1O128         save v1 output
00005C84  07FB                                     4456+         BR    R11               return
00005C88                                           4457+RE128    DC    0F                xl16 expected result
00005C88                                           4458+         DROP  R5
00005C88  00000000 00000320                        4459          DC    XL16'0000000000000320 000A0708000D0003'   result
00005C90  000A0708 000D0003
00005C98  FF020304 05060750                        4460          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005CA0  090A0B78 0C0D0EFD
00005CA8  FF000000 0000000A                        4461          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00005CB0  0101010F 010101FF
                                                   4462
                                                   4463 * Halfword
                                                   4464          VRR_C VMO,1
00005CB8                                           4465+         DS    0FD
00005CB8                      00005CB8             4466+         USING *,R5              base for test data and test routine
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005CB8  00005CF8                                 4467+T129     DC    A(X129)           address of test routine
00005CBC  0081                                     4468+         DC    H'129'            test number
00005CBE  00                                       4469+         DC    X'00'
00005CBF  01                                       4470+         DC    HL1'1'            m4
00005CC0  E5D4D640 40404040                        4471+         DC    CL8'VMO'          instruction name
00005CC8  00005D30                                 4472+         DC    A(RE129+16)       address of v2 source
00005CCC  00005D40                                 4473+         DC    A(RE129+32)       address of v3 source
00005CD0  00000010                                 4474+         DC    A(16)             result length
00005CD4  00005D20                                 4475+REA129   DC    A(RE129)          result address
00005CD8  00000000 00000000                        4476+         DS    FD                gap
00005CE0  00000000 00000000                        4477+V1O129   DS    XL16              V1 output
00005CE8  00000000 00000000
00005CF0  00000000 00000000                        4478+         DS    FD                gap
                                                   4479+*
00005CF8                                           4480+X129     DS    0F
00005CF8  E310 5010 0014                00000010   4481+         LGF   R1,V2ADDR         load v2 source
00005CFE  E761 0000 0806                00000000   4482+         VL    v22,0(R1)         use v22 to test decoder
00005D04  E310 5014 0014                00000014   4483+         LGF   R1,V3ADDR         load v3 source
00005D0A  E771 0000 0806                00000000   4484+         VL    v23,0(R1)         use v23 to test decoder
00005D10  E766 7000 1EA7                           4485+         VMO   V22,V22,V23,1      test instruction (dest is a source)
00005D16  E760 5028 080E                00005CE0   4486+         VST   V22,V1O129         save v1 output
00005D1C  07FB                                     4487+         BR    R11               return
00005D20                                           4488+RE129    DC    0F                xl16 expected result
00005D20                                           4489+         DROP  R5
00005D20  00000000 00000271                        4490          DC    XL16'0000000000000271 000000000121CC24'   result
00005D28  00000000 0121CC24
00005D30  FFFF0000 00000019                        4491          DC    XL16'FFFF000000000019 003800001000EEFA'   v2
00005D38  00380000 1000EEFA
00005D40  FFFF0000 00000019                        4492          DC    XL16'FFFF000000000019 003800038000EEFA'   v3
00005D48  00380003 8000EEFA
                                                   4493
                                                   4494          VRR_C VMO,1
00005D50                                           4495+         DS    0FD
00005D50                        00005D50           4496+         USING *,R5              base for test data and test routine
00005D50  00005D90                                 4497+T130     DC    A(X130)           address of test routine
00005D54  0082                                     4498+         DC    H'130'            test number
00005D56  00                                       4499+         DC    X'00'
00005D57  01                                       4500+         DC    HL1'1'            m4
00005D58  E5D4D640 40404040                        4501+         DC    CL8'VMO'          instruction name
00005D60  00005DC8                                 4502+         DC    A(RE130+16)       address of v2 source
00005D64  00005DD8                                 4503+         DC    A(RE130+32)       address of v3 source
00005D68  00000010                                 4504+         DC    A(16)             result length
00005D6C  00005DB8                                 4505+REA130   DC    A(RE130)          result address
00005D70  00000000 00000000                        4506+         DS    FD                gap
00005D78  00000000 00000000                        4507+V1O130   DS    XL16              V1 output
00005D80  00000000 00000000
00005D88  00000000 00000000                        4508+         DS    FD                gap
                                                   4509+*
00005D90                                           4510+X130     DS    0F
00005D90  E310 5010 0014                00000010   4511+         LGF   R1,V2ADDR         load v2 source
00005D96  E761 0000 0806                00000000   4512+         VL    v22,0(R1)         use v22 to test decoder
00005D9C  E310 5014 0014                00000014   4513+         LGF   R1,V3ADDR         load v3 source
00005DA2  E771 0000 0806                00000000   4514+         VL    v23,0(R1)         use v23 to test decoder
00005DA8  E766 7000 1EA7                           4515+         VMO   V22,V22,V23,1      test instruction (dest is a source)
00005DAE  E760 5028 080E                00005D78   4516+         VST   V22,V1O130         save v1 output
00005DB4  07FB                                     4517+         BR    R11               return
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005DB8                                           4518+RE130    DC    0F                xl16 expected result
00005DB8                                           4519+         DROP  R5
00005DB8  00091810 00357900                        4520          DC    XL16'0009181000357900 0083884000EFA309'   result
00005DC0  00838840 00EFA309
00005DC8  FF020304 05060750                        4521          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005DD0  090A0B78 0C0D0EFD
00005DD8  FF020304 05060750                        4522          DC    XL16'FF02030405060750 090A0B780D0E0FFD'   v3
00005DE0  090A0B78 0D0E0FFD
                                                   4523
                                                   4524          VRR_C VMO,1
00005DE8                                           4525+         DS    0FD
00005DE8                      00005DE8             4526+         USING *,R5              base for test data and test routine
00005DE8  00005E28                                 4527+T131     DC    A(X131)           address of test routine
00005DEC  0083                                     4528+         DC    H'131'            test number
00005DEE  00                                       4529+         DC    X'00'
00005DEF  01                                       4530+         DC    HL1'1'            m4
00005DF0  E5D4D640 40404040                        4531+         DC    CL8'VMO'          instruction name
00005DF8  00005E60                                 4532+         DC    A(RE131+16)       address of v2 source
00005DFC  00005E70                                 4533+         DC    A(RE131+32)       address of v3 source
00005E00  00000010                                 4534+         DC    A(16)             result length
00005E04  00005E50                                 4535+REA131   DC    A(RE131)          result address
00005E08  00000000 00000000                        4536+         DS    FD                gap
00005E10  00000000 00000000                        4537+V1O131   DS    XL16              V1 output
00005E18  00000000 00000000
00005E20  00000000 00000000                        4538+         DS    FD                gap
                                                   4539+*
00005E28                                           4540+X131     DS    0F
00005E28  E310 5010 0014                00000010   4541+         LGF   R1,V2ADDR         load v2 source
00005E2E  E761 0000 0806                00000000   4542+         VL    v22,0(R1)         use v22 to test decoder
00005E34  E310 5014 0014                00000014   4543+         LGF   R1,V3ADDR         load v3 source
00005E3A  E771 0000 0806                00000000   4544+         VL    v23,0(R1)         use v23 to test decoder
00005E40  E766 7000 1EA7                           4545+         VMO   V22,V22,V23,1      test instruction (dest is a source)
00005E46  E760 5028 080E                00005E10   4546+         VST   V22,V1O131         save v1 output
00005E4C  07FB                                     4547+         BR    R11               return
00005E50                                           4548+RE131    DC    0F                xl16 expected result
00005E50                                           4549+         DROP  R5
00005E50  00030A08 00171480                        4550          DC    XL16'00030A0800171480 003C08200077CA06'   result
00005E58  003C0820 0077CA06
00005E60  FF020304 05060750                        4551          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005E68  090A0B78 0C0D0EFD
00005E70  FF010102 02030328                        4552          DC    XL16'FF01010202030328 0405053C060707FE'   v3
00005E78  0405053C 060707FE
                                                   4553
                                                   4554          VRR_C VMO,1
00005E80                                           4555+         DS    0FD
00005E80                      00005E80             4556+         USING *,R5              base for test data and test routine
00005E80  00005EC0                                 4557+T132     DC    A(X132)           address of test routine
00005E84  0084                                     4558+         DC    H'132'            test number
00005E86  00                                       4559+         DC    X'00'
00005E87  01                                       4560+         DC    HL1'1'            m4
00005E88  E5D4D640 40404040                        4561+         DC    CL8'VMO'          instruction name
00005E90  00005EF8                                 4562+         DC    A(RE132+16)       address of v2 source
00005E94  00005F08                                 4563+         DC    A(RE132+32)       address of v3 source
00005E98  00000010                                 4564+         DC    A(16)             result length
00005E9C  00005EE8                                 4565+REA132   DC    A(RE132)          result address
00005EA0  00000000 00000000                        4566+         DS    FD                gap
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00005EA8  00000000 00000000                        4567+V1O132   DS    XL16              V1 output
00005EB0  00000000 00000000
00005EB8  00000000 00000000                        4568+         DS    FD                gap
                                                   4569+*
00005EC0                                           4570+X132     DS    0F
00005EC0  E310 5010 0014                 00000010  4571+         LGF   R1,V2ADDR         load v2 source
00005EC6  E761 0000 0806                 00000000  4572+         VL    v22,0(R1)         use v22 to test decoder
00005ECC  E310 5014 0014                 00000014  4573+         LGF   R1,V3ADDR         load v3 source
00005ED2  E771 0000 0806                 00000000  4574+         VL    v23,0(R1)         use v23 to test decoder
00005ED8  E766 7000 1EA7                           4575+         VMO   V22,V22,V23,1      test instruction (dest is a source)
00005EDE  E760 5028 080E                 00005EA8  4576+         VST   V22,V1O132         save v1 output
00005EE4  07FB                                     4577+         BR    R11               return
00005EE8                                           4578+RE132    DC    0F                xl16 expected result
00005EE8                                           4579+         DROP  R5
00005EE8  00000000 00004920                        4580          DC    XL16'0000000000004920 000C2408001DEB03'   result
00005EF0  000C2408 001DEB03
00005EF8  FF020304 05060750                        4581          DC    XL16'FF02030405060750 090A0B780C0D0EFD'   v2
00005F00  090A0B78 0C0D0EFD
00005F08  FF000000 0000000A                        4582          DC    XL16'FF0000000000000A 0101010F010101FF'   v3
00005F10  0101010F 010101FF
                                                   4583
                                                   4584 * Word
                                                   4585          VRR_C VMO,2
00005F18                                           4586+         DS    0FD
00005F18                         00005F18          4587+         USING *,R5              base for test data and test routine
00005F18  00005F58                                 4588+T133     DC    A(X133)           address of test routine
00005F1C  0085                                     4589+         DC    H'133'            test number
00005F1E  00                                       4590+         DC    X'00'
00005F1F  02                                       4591+         DC    HL1'2'            m4
00005F20  E5D4D640 40404040                        4592+         DC    CL8'VMO'          instruction name
00005F28  00005F90                                 4593+         DC    A(RE133+16)       address of v2 source
00005F2C  00005FA0                                 4594+         DC    A(RE133+32)       address of v3 source
00005F30  00000010                                 4595+         DC    A(16)             result length
00005F34  00005F80                                 4596+REA133   DC    A(RE133)          result address
00005F38  00000000 00000000                        4597+         DS    FD                gap
00005F40  00000000 00000000                        4598+V1O133   DS    XL16              V1 output
00005F48  00000000 00000000
00005F50  00000000 00000000                        4599+         DS    FD                gap
                                                   4600+*
00005F58                                           4601+X133     DS    0F
00005F58  E310 5010 0014                 00000010  4602+         LGF   R1,V2ADDR         load v2 source
00005F5E  E761 0000 0806                 00000000  4603+         VL    v22,0(R1)         use v22 to test decoder
00005F64  E310 5014 0014                 00000014  4604+         LGF   R1,V3ADDR         load v3 source
00005F6A  E771 0000 0806                 00000000  4605+         VL    v23,0(R1)         use v23 to test decoder
00005F70  E766 7000 2EA7                           4606+         VMO   V22,V22,V23,2      test instruction (dest is a source)
00005F76  E760 5028 080E                 00005F40  4607+         VST   V22,V1O133         save v1 output
00005F7C  07FB                                     4608+         BR    R11               return
00005F80                                           4609+RE133    DC    0F                xl16 expected result
00005F80                                           4610+         DROP  R5
00005F80  00000002 71000000                        4611          DC    XL16'0000000271000000 FF0123454FEDCC24'   result
00005F88  FF012345 4FEDCC24
00005F90  FFFFFFFF 00019000                        4612          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
00005F98  00000038 EEEEEEFA
00005FA0  FFFFFFFF 00019000                        4613          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00005FA8  00000038 0EEEEEFA
                                                   4614
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   4615          VRR_C VMO,2
00005FB0                                           4616+         DS    0FD
00005FB0                     00005FB0              4617+         USING *,R5              base for test data and test routine
00005FB0  00005FF0                                 4618+T134     DC    A(X134)           address of test routine
00005FB4  0086                                     4619+         DC    H'134'            test number
00005FB6  00                                       4620+         DC    X'00'
00005FB7  02                                       4621+         DC    HL1'2'            m4
00005FB8  E5D4D640 40404040                        4622+         DC    CL8'VMO'          instruction name
00005FC0  00006028                                 4623+         DC    A(RE134+16)       address of v2 source
00005FC4  00006038                                 4624+         DC    A(RE134+32)       address of v3 source
00005FC8  00000010                                 4625+         DC    A(16)             result length
00005FCC  00006018                                 4626+REA134   DC    A(RE134)          result address
00005FD0  00000000 00000000                        4627+         DS    FD                gap
00005FD8  00000000 00000000                        4628+V1O134   DS    XL16              V1 output
00005FE0  00000000 00000000
00005FE8  00000000 00000000                        4629+         DS    FD                gap
                                                   4630+*
00005FF0                                           4631+X134     DS    0F
00005FF0  E310 5010 0014                00000010   4632+         LGF   R1,V2ADDR         load v2 source
00005FF6  E761 0000 0806                00000000   4633+         VL    v22,0(R1)         use v22 to test decoder
00005FFC  E310 5014 0014                00000014   4634+         LGF   R1,V3ADDR         load v3 source
00006002  E771 0000 0806                00000000   4635+         VL    v23,0(R1)         use v23 to test decoder
00006008  E766 7000 2EA7                           4636+         VMO   V22,V22,V23,2      test instruction (dest is a source)
0000600E  E760 5028 080E                00005FD8   4637+         VST   V22,V1O134         save v1 output
00006014  07FB                                     4638+         BR    R11               return
00006018                                           4639+RE134    DC    0F                xl16 expected result
00006018                                           4640+         DROP  R5
00006018  00193C6D 77F57900                        4641          DC    XL16'00193C6D77F57900 00AA6E5898D42101'   result
00006020  00AA6E58 98D42101
00006028  FF020304 05060750                        4642          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00006030  090A0B0C 0D0E0F7F
00006038  FF020304 05060750                        4643          DC    XL16'FF02030405060750 090A0B780D0E0F7F'   v3
00006040  090A0B78 0D0E0F7F
                                                   4644
                                                   4645          VRR_C VMO,2
00006048                                           4646+         DS    0FD
00006048                     00006048              4647+         USING *,R5              base for test data and test routine
00006048  00006088                                 4648+T135     DC    A(X135)           address of test routine
0000604C  0087                                     4649+         DC    H'135'            test number
0000604E  00                                       4650+         DC    X'00'
0000604F  02                                       4651+         DC    HL1'2'            m4
00006050  E5D4D640 40404040                        4652+         DC    CL8'VMO'          instruction name
00006058  000060C0                                 4653+         DC    A(RE135+16)       address of v2 source
0000605C  000060D0                                 4654+         DC    A(RE135+32)       address of v3 source
00006060  00000010                                 4655+         DC    A(16)             result length
00006064  000060B0                                 4656+REA135   DC    A(RE135)          result address
00006068  00000000 00000000                        4657+         DS    FD                gap
00006070  00000000 00000000                        4658+V1O135   DS    XL16              V1 output
00006078  00000000 00000000
00006080  00000000 00000000                        4659+         DS    FD                gap
                                                   4660+*
00006088                                           4661+X135     DS    0F
00006088  E310 5010 0014                00000010   4662+         LGF   R1,V2ADDR         load v2 source
0000608E  E761 0000 0806                00000000   4663+         VL    v22,0(R1)         use v22 to test decoder
00006094  E310 5014 0014                00000014   4664+         LGF   R1,V3ADDR         load v3 source
0000609A  E771 0000 0806                00000000   4665+         VL    v23,0(R1)         use v23 to test decoder
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

000060A0  E766 7000 2EA7                          4666+         VMO   V22,V22,V23,2      test instruction (dest is a source)
000060A6  E760 5028 080E                00006070  4667+         VST   V22,V1O135         save v1 output
000060AC  07FB                                    4668+         BR    R11               return
000060B0                                          4669+RE135    DC    0F                xl16 expected result
000060B0                                          4670+         DROP  R5
000060B0  000A1B30 90F71480                       4671          DC    XL16'000A1B3090F71480 004EB01DFF5B4941'   result
000060B8  004EB01D FF5B4941
000060C0  FF020304 05060750                       4672          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000060C8  090A0B0C 0D0E0F7F
000060D0  FF010102 02030328                       4673          DC    XL16'FF01010202030328 0405053C0607073F'   v3
000060D8  0405053C 0607073F
                                                  4674
                                                  4675          VRR_C VMO,2
000060E0                                          4676+         DS    0FD
000060E0                      000060E0            4677+         USING *,R5              base for test data and test routine
000060E0  00006120                                4678+T136     DC    A(X136)           address of test routine
000060E4  0088                                    4679+         DC    H'136'            test number
000060E6  00                                      4680+         DC    X'00'
000060E7  02                                      4681+         DC    HL1'2'            m4
000060E8  E5D4D640 40404040                       4682+         DC    CL8'VMO'          instruction name
000060F0  00006158                                4683+         DC    A(RE136+16)       address of v2 source
000060F4  00006168                                4684+         DC    A(RE136+32)       address of v3 source
000060F8  00000010                                4685+         DC    A(16)             result length
000060FC  00006148                                4686+REA136   DC    A(RE136)          result address
00006100  00000000 00000000                       4687+         DS    FD                gap
00006108  00000000 00000000                       4688+V1O136   DS    XL16              V1 output
00006110  00000000 00000000
00006118  00000000 00000000                       4689+         DS    FD                gap
                                                  4690+*
00006120                                          4691+X136     DS    0F
00006120  E310 5010 0014                00000010  4692+         LGF   R1,V2ADDR         load v2 source
00006126  E761 0000 0806                00000000  4693+         VL    v22,0(R1)         use v22 to test decoder
0000612C  E310 5014 0014                00000014  4694+         LGF   R1,V3ADDR         load v3 source
00006132  E771 0000 0806                00000000  4695+         VL    v23,0(R1)         use v23 to test decoder
00006138  E766 7000 2EA7                          4696+         VMO   V22,V22,V23,2      test instruction (dest is a source)
0000613E  E760 5028 080E                00006108  4697+         VST   V22,V1O136         save v1 output
00006144  07FB                                    4698+         BR    R11               return
00006148                                          4699+RE136    DC    0F                xl16 expected result
00006148                                          4700+         DROP  R5
00006148  00000000 323C4920                       4701          DC    XL16'00000000323C4920 000D1B2B60616771'   result
00006150  000D1B2B 60616771
00006158  FF020304 05060750                       4702          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00006160  090A0B0C 0D0E0F7F
00006168  FF000000 0000000A                       4703          DC    XL16'FF0000000000000A 0101010F0101010F'   v3
00006170  0101010F 0101010F
                                                  4704
                                                  4705 * Doubleword
                                                  4706          VRR_C VMO,3
00006178                                          4707+         DS    0FD
00006178                      00006178            4708+         USING *,R5              base for test data and test routine
00006178  000061B8                                4709+T137     DC    A(X137)           address of test routine
0000617C  0089                                    4710+         DC    H'137'            test number
0000617E  00                                      4711+         DC    X'00'
0000617F  03                                      4712+         DC    HL1'3'            m4
00006180  E5D4D640 40404040                       4713+         DC    CL8'VMO'          instruction name
00006188  000061F0                                4714+         DC    A(RE137+16)       address of v2 source
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

0000618C  00006200                                 4715+         DC    A(RE137+32)       address of v3 source
00006190  00000010                                 4716+         DC    A(16)             result length
00006194  000061E0                                 4717+REA137   DC    A(RE137)          result address
00006198  00000000 00000000                        4718+         DS    FD                gap
000061A0  00000000 00000000                        4719+V1O137   DS    XL16              V1 output
000061A8  00000000 00000000
000061B0  00000000 00000000                        4720+         DS    FD                gap
                                                   4721+*
000061B8                                           4722+X137     DS    0F
000061B8  E310 5010 0014                 00000010  4723+         LGF   R1,V2ADDR         load v2 source
000061BE  E761 0000 0806                 00000000  4724+         VL    v22,0(R1)         use v22 to test decoder
000061C4  E310 5014 0014                 00000014  4725+         LGF   R1,V3ADDR         load v3 source
000061CA  E771 0000 0806                 00000000  4726+         VL    v23,0(R1)         use v23 to test decoder
000061D0  E766 7000 3EA7                           4727+         VMO   V22,V22,V23,3      test instruction (dest is a source)
000061D6  E760 5028 080E                 000061A0  4728+         VST   V22,V1O137         save v1 output
000061DC  07FB                                     4729+         BR    R11               return
000061E0                                           4730+RE137    DC    0F                xl16 expected result
000061E0                                           4731+         DROP  R5
000061E0  00000000 00000C77                        4732          DC    XL16'0000000000000C77 96789F9F4FEDCC24'   result
000061E8  96789F9F 4FEDCC24
000061F0  FFFFFFFF 00019000                        4733          DC    XL16'FFFFFFFF00019000 00000038EEEEEEFA'   v2
000061F8  00000038 EEEEEEFA
00006200  FFFFFFFF 00019000                        4734          DC    XL16'FFFFFFFF00019000 000000380EEEEEFA'   v3
00006208  00000038 0EEEEEFA
                                                   4735
                                                   4736          VRR_C VMO,3
00006210                                           4737+         DS    0FD
00006210                         00006210          4738+         USING *,R5              base for test data and test routine
00006210  00006250                                 4739+T138     DC    A(X138)           address of test routine
00006214  008A                                     4740+         DC    H'138'            test number
00006216  00                                       4741+         DC    X'00'
00006217  03                                       4742+         DC    HL1'3'            m4
00006218  E5D4D640 40404040                        4743+         DC    CL8'VMO'          instruction name
00006220  00006288                                 4744+         DC    A(RE138+16)       address of v2 source
00006224  00006298                                 4745+         DC    A(RE138+32)       address of v3 source
00006228  00000010                                 4746+         DC    A(16)             result length
0000622C  00006278                                 4747+REA138   DC    A(RE138)          result address
00006230  00000000 00000000                        4748+         DS    FD                gap
00006238  00000000 00000000                        4749+V1O138   DS    XL16              V1 output
00006240  00000000 00000000
00006248  00000000 00000000                        4750+         DS    FD                gap
                                                   4751+*
00006250                                           4752+X138     DS    0F
00006250  E310 5010 0014                 00000010  4753+         LGF   R1,V2ADDR         load v2 source
00006256  E761 0000 0806                 00000000  4754+         VL    v22,0(R1)         use v22 to test decoder
0000625C  E310 5014 0014                 00000014  4755+         LGF   R1,V3ADDR         load v3 source
00006262  E771 0000 0806                 00000000  4756+         VL    v23,0(R1)         use v23 to test decoder
00006268  E766 7000 3EA7                           4757+         VMO   V22,V22,V23,3      test instruction (dest is a source)
0000626E  E760 5028 080E                 00006238  4758+         VST   V22,V1O138         save v1 output
00006274  07FB                                     4759+         BR    R11               return
00006278                                           4760+RE138    DC    0F                xl16 expected result
00006278                                           4761+         DROP  R5
00006278  0051B52F 8692B4F6                        4762          DC    XL16'0051B52F8692B4F6 152B55D498D42101'   result
00006280  152B55D4 98D42101
00006288  FF020304 05060750                        4763          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00006290  090A0B0C 0D0E0F7F
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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00006298  01020304 05060750                        4764          DC    XL16'0102030405060750 090A0B780D0E0F7F'   v3
000062A0  090A0B78 0D0E0F7F
                                                   4765
                                                   4766          VRR_C VMO,3
000062A8                                           4767+         DS    0FD
000062A8                      000062A8             4768+         USING *,R5              base for test data and test routine
000062A8  000062E8                                 4769+T139     DC    A(X139)           address of test routine
000062AC  008B                                     4770+         DC    H'139'            test number
000062AE  00                                       4771+         DC    X'00'
000062AF  03                                       4772+         DC    HL1'3'            m4
000062B0  E5D4D640 40404040                        4773+         DC    CL8'VMO'          instruction name
000062B8  00006320                                 4774+         DC    A(RE139+16)       address of v2 source
000062BC  00006330                                 4775+         DC    A(RE139+32)       address of v3 source
000062C0  00000010                                 4776+         DC    A(16)             result length
000062C4  00006310                                 4777+REA139   DC    A(RE139)          result address
000062C8  00000000 00000000                        4778+         DS    FD                gap
000062D0  00000000 00000000                        4779+V1O139   DS    XL16              V1 output
000062D8  00000000 00000000
000062E0  00000000 00000000                        4780+         DS    FD                gap
                                                   4781+*
000062E8                                           4782+X139     DS    0F
000062E8  E310 5010 0014                00000010   4783+         LGF   R1,V2ADDR         load v2 source
000062EE  E761 0000 0806                00000000   4784+         VL    v22,0(R1)         use v22 to test decoder
000062F4  E310 5014 0014                00000014   4785+         LGF   R1,V3ADDR         load v3 source
000062FA  E771 0000 0806                00000000   4786+         VL    v23,0(R1)         use v23 to test decoder
00006300  E766 7000 3EA7                           4787+         VMO   V22,V22,V23,3      test instruction (dest is a source)
00006306  E760 5028 080E                000062D0   4788+         VST   V22,V1O139         save v1 output
0000630C  07FB                                     4789+         BR    R11               return
00006310                                           4790+RE139    DC    0F                xl16 expected result
00006310                                           4791+         DROP  R5
00006310  0024558D B838C862                        4792          DC    XL16'0024558DB838C862 B47CD8D5FF5B4941'   result
00006318  B47CD8D5 FF5B4941
00006320  FF020304 05060750                        4793          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
00006328  090A0B0C 0D0E0F7F
00006330  00010102 02030328                        4794          DC    XL16'0001010202030328 0405053C0607073F'   v3
00006338  0405053C 0607073F
                                                   4795
                                                   4796          VRR_C VMO,3
00006340                                           4797+         DS    0FD
00006340                      00006340             4798+         USING *,R5              base for test data and test routine
00006340  00006380                                 4799+T140     DC    A(X140)           address of test routine
00006344  008C                                     4800+         DC    H'140'            test number
00006346  00                                       4801+         DC    X'00'
00006347  03                                       4802+         DC    HL1'3'            m4
00006348  E5D4D640 40404040                        4803+         DC    CL8'VMO'          instruction name
00006350  000063B8                                 4804+         DC    A(RE140+16)       address of v2 source
00006354  000063C8                                 4805+         DC    A(RE140+32)       address of v3 source
00006358  00000010                                 4806+         DC    A(16)             result length
0000635C  000063A8                                 4807+REA140   DC    A(RE140)          result address
00006360  00000000 00000000                        4808+         DS    FD                gap
00006368  00000000 00000000                        4809+V1O140   DS    XL16              V1 output
00006370  00000000 00000000
00006378  00000000 00000000                        4810+         DS    FD                gap
                                                   4811+*
00006380                                           4812+X140     DS    0F
00006380  E310 5010 0014                00000010   4813+         LGF   R1,V2ADDR         load v2 source
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2    STMT

00006386  E761 0000 0806                00000000  4814+         VL    v22,0(R1)          use v22 to test decoder
0000638C  E310 5014 0014                00000014  4815+         LGF   R1,V3ADDR          load v3 source
00006392  E771 0000 0806                00000000  4816+         VL    v23,0(R1)          use v23 to test decoder
00006398  E766 7000 3EA7                          4817+         VMO   V22,V22,V23,3       test instruction (dest is a source)
0000639E  E760 5028 080E                00006368  4818+         VST   V22,V1O140          save v1 output
000063A4  07FB                                    4819+         BR    R11                return
000063A8                                          4820+RE140    DC    0F                 xl16 expected result
000063A8                                          4821+         DROP  R5
000063A8  0009131E A8C3DFFE                       4822          DC    XL16'0009131EA8C3DFFE 091C345060616771'   result
000063B0  091C3450 60616771
000063B8  FF020304 05060750                       4823          DC    XL16'FF02030405060750 090A0B0C0D0E0F7F'   v2
000063C0  090A0B0C 0D0E0F7F
000063C8  00000000 0000000A                       4824          DC    XL16'000000000000000A 0101010F0101010F'   v3
000063D0  0101010F 0101010F
                                                  4825
                                                  4826          VRR_C VMO,3
000063D8                                          4827+         DS    0FD
000063D8                        000063D8          4828+         USING *,R5               base for test data and test routine
000063D8  00006418                                4829+T141     DC    A(X141)            address of test routine
000063DC  008D                                    4830+         DC    H'141'             test number
000063DE  00                                      4831+         DC    X'00'
000063DF  03                                      4832+         DC    HL1'3'             m4
000063E0  E5D4D640 40404040                       4833+         DC    CL8'VMO'           instruction name
000063E8  00006450                                4834+         DC    A(RE141+16)        address of v2 source
000063EC  00006460                                4835+         DC    A(RE141+32)        address of v3 source
000063F0  00000010                                4836+         DC    A(16)              result length
000063F4  00006440                                4837+REA141   DC    A(RE141)           result address
000063F8  00000000 00000000                       4838+         DS    FD                 gap
00006400  00000000 00000000                       4839+V1O141   DS    XL16               V1 output
00006408  00000000 00000000
00006410  00000000 00000000                       4840+         DS    FD                 gap
                                                  4841+*
00006418                                          4842+X141     DS    0F
00006418  E310 5010 0014                00000010  4843+         LGF   R1,V2ADDR          load v2 source
0000641E  E761 0000 0806                00000000  4844+         VL    v22,0(R1)          use v22 to test decoder
00006424  E310 5014 0014                00000014  4845+         LGF   R1,V3ADDR          load v3 source
0000642A  E771 0000 0806                00000000  4846+         VL    v23,0(R1)          use v23 to test decoder
00006430  E766 7000 3EA7                          4847+         VMO   V22,V22,V23,3       test instruction (dest is a source)
00006436  E760 5028 080E                00006400  4848+         VST   V22,V1O141          save v1 output
0000643C  07FB                                    4849+         BR    R11                return
00006440                                          4850+RE141    DC    0F                 xl16 expected result
00006440                                          4851+         DROP  R5
00006440  FFFFFFFF FFFFFFFF                       4852          DC    XL16'FFFFFFFFFFFFFFFF F6141E28323C4920'   result
00006448  F6141E28 323C4920
00006450  090A0B0C 0D0E0F7F                       4853          DC    XL16'090A0B0C0D0E0F7F FF02030405060750'   v2
00006458  FF020304 05060750
00006460  0101010F 0101010F                       4854          DC    XL16'0101010F0101010F 000000000000000A'   v3
00006468  00000000 0000000A
                                                  4855
                                                  4856
00006470  00000000                                4857          DC    F'0'     END OF TABLE
00006474  00000000                                4858          DC    F'0'
                                                  4859 *
                                                  4860 * table of pointers to individual load test
                                                  4861 *
00006478                                          4862 E7TESTS  DS    0F
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                                   4863          PTTABLE
00006478                                           4864+TTABLE   DS    0F
00006478  000010B8                                 4865+         DC    A(T1)
0000647C  00001150                                 4866+         DC    A(T2)
00006480  000011E8                                 4867+         DC    A(T3)
00006484  00001280                                 4868+         DC    A(T4)
00006488  00001318                                 4869+         DC    A(T5)
0000648C  000013B0                                 4870+         DC    A(T6)
00006490  00001448                                 4871+         DC    A(T7)
00006494  000014E0                                 4872+         DC    A(T8)
00006498  00001578                                 4873+         DC    A(T9)
0000649C  00001610                                 4874+         DC    A(T10)
000064A0  000016A8                                 4875+         DC    A(T11)
000064A4  00001740                                 4876+         DC    A(T12)
000064A8  000017D8                                 4877+         DC    A(T13)
000064AC  00001870                                 4878+         DC    A(T14)
000064B0  00001908                                 4879+         DC    A(T15)
000064B4  000019A0                                 4880+         DC    A(T16)
000064B8  00001A38                                 4881+         DC    A(T17)
000064BC  00001AD0                                 4882+         DC    A(T18)
000064C0  00001B68                                 4883+         DC    A(T19)
000064C4  00001C00                                 4884+         DC    A(T20)
000064C8  00001C98                                 4885+         DC    A(T21)
000064CC  00001D30                                 4886+         DC    A(T22)
000064D0  00001DC8                                 4887+         DC    A(T23)
000064D4  00001E60                                 4888+         DC    A(T24)
000064D8  00001EF8                                 4889+         DC    A(T25)
000064DC  00001F90                                 4890+         DC    A(T26)
000064E0  00002028                                 4891+         DC    A(T27)
000064E4  000020C0                                 4892+         DC    A(T28)
000064E8  00002158                                 4893+         DC    A(T29)
000064EC  000021F0                                 4894+         DC    A(T30)
000064F0  00002288                                 4895+         DC    A(T31)
000064F4  00002320                                 4896+         DC    A(T32)
000064F8  000023B8                                 4897+         DC    A(T33)
000064FC  00002450                                 4898+         DC    A(T34)
00006500  000024E8                                 4899+         DC    A(T35)
00006504  00002580                                 4900+         DC    A(T36)
00006508  00002618                                 4901+         DC    A(T37)
0000650C  000026B0                                 4902+         DC    A(T38)
00006510  00002748                                 4903+         DC    A(T39)
00006514  000027E0                                 4904+         DC    A(T40)
00006518  00002878                                 4905+         DC    A(T41)
0000651C  00002910                                 4906+         DC    A(T42)
00006520  000029A8                                 4907+         DC    A(T43)
00006524  00002A40                                 4908+         DC    A(T44)
00006528  00002AD8                                 4909+         DC    A(T45)
0000652C  00002B70                                 4910+         DC    A(T46)
00006530  00002C08                                 4911+         DC    A(T47)
00006534  00002CA0                                 4912+         DC    A(T48)
00006538  00002D38                                 4913+         DC    A(T49)
0000653C  00002DD0                                 4914+         DC    A(T50)
00006540  00002E68                                 4915+         DC    A(T51)
00006544  00002F00                                 4916+         DC    A(T52)
00006548  00002F98                                 4917+         DC    A(T53)
0000654C  00003030                                 4918+         DC    A(T54)
```

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  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00006550  000030C8                                4919+         DC    A(T55)
00006554  00003160                                4920+         DC    A(T56)
00006558  000031F8                                4921+         DC    A(T57)
0000655C  00003290                                4922+         DC    A(T58)
00006560  00003328                                4923+         DC    A(T59)
00006564  000033C0                                4924+         DC    A(T60)
00006568  00003458                                4925+         DC    A(T61)
0000656C  000034F0                                4926+         DC    A(T62)
00006570  00003588                                4927+         DC    A(T63)
00006574  00003620                                4928+         DC    A(T64)
00006578  000036B8                                4929+         DC    A(T65)
0000657C  00003750                                4930+         DC    A(T66)
00006580  000037E8                                4931+         DC    A(T67)
00006584  00003880                                4932+         DC    A(T68)
00006588  00003918                                4933+         DC    A(T69)
0000658C  000039B0                                4934+         DC    A(T70)
00006590  00003A48                                4935+         DC    A(T71)
00006594  00003AE0                                4936+         DC    A(T72)
00006598  00003B78                                4937+         DC    A(T73)
0000659C  00003C10                                4938+         DC    A(T74)
000065A0  00003CA8                                4939+         DC    A(T75)
000065A4  00003D40                                4940+         DC    A(T76)
000065A8  00003DD8                                4941+         DC    A(T77)
000065AC  00003E70                                4942+         DC    A(T78)
000065B0  00003F08                                4943+         DC    A(T79)
000065B4  00003FA0                                4944+         DC    A(T80)
000065B8  00004038                                4945+         DC    A(T81)
000065BC  000040D0                                4946+         DC    A(T82)
000065C0  00004168                                4947+         DC    A(T83)
000065C4  00004200                                4948+         DC    A(T84)
000065C8  00004298                                4949+         DC    A(T85)
000065CC  00004330                                4950+         DC    A(T86)
000065D0  000043C8                                4951+         DC    A(T87)
000065D4  00004460                                4952+         DC    A(T88)
000065D8  000044F8                                4953+         DC    A(T89)
000065DC  00004590                                4954+         DC    A(T90)
000065E0  00004628                                4955+         DC    A(T91)
000065E4  000046C0                                4956+         DC    A(T92)
000065E8  00004758                                4957+         DC    A(T93)
000065EC  000047F0                                4958+         DC    A(T94)
000065F0  00004888                                4959+         DC    A(T95)
000065F4  00004920                                4960+         DC    A(T96)
000065F8  000049B8                                4961+         DC    A(T97)
000065FC  00004A50                                4962+         DC    A(T98)
00006600  00004AE8                                4963+         DC    A(T99)
00006604  00004B80                                4964+         DC    A(T100)
00006608  00004C18                                4965+         DC    A(T101)
0000660C  00004CB0                                4966+         DC    A(T102)
00006610  00004D48                                4967+         DC    A(T103)
00006614  00004DE0                                4968+         DC    A(T104)
00006618  00004E78                                4969+         DC    A(T105)
0000661C  00004F10                                4970+         DC    A(T106)
00006620  00004FA8                                4971+         DC    A(T107)
00006624  00005040                                4972+         DC    A(T108)
00006628  000050D8                                4973+         DC    A(T109)
0000662C  00005170                                4974+         DC    A(T110)
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

00006630  00005208                                 4975+          DC    A(T111)
00006634  000052A0                                 4976+          DC    A(T112)
00006638  00005338                                 4977+          DC    A(T113)
0000663C  000053D0                                 4978+          DC    A(T114)
00006640  00005468                                 4979+          DC    A(T115)
00006644  00005500                                 4980+          DC    A(T116)
00006648  00005598                                 4981+          DC    A(T117)
0000664C  00005630                                 4982+          DC    A(T118)
00006650  000056C8                                 4983+          DC    A(T119)
00006654  00005760                                 4984+          DC    A(T120)
00006658  000057F8                                 4985+          DC    A(T121)
0000665C  00005890                                 4986+          DC    A(T122)
00006660  00005928                                 4987+          DC    A(T123)
00006664  000059C0                                 4988+          DC    A(T124)
00006668  00005A58                                 4989+          DC    A(T125)
0000666C  00005AF0                                 4990+          DC    A(T126)
00006670  00005B88                                 4991+          DC    A(T127)
00006674  00005C20                                 4992+          DC    A(T128)
00006678  00005CB8                                 4993+          DC    A(T129)
0000667C  00005D50                                 4994+          DC    A(T130)
00006680  00005DE8                                 4995+          DC    A(T131)
00006684  00005E80                                 4996+          DC    A(T132)
00006688  00005F18                                 4997+          DC    A(T133)
0000668C  00005FB0                                 4998+          DC    A(T134)
00006690  00006048                                 4999+          DC    A(T135)
00006694  000060E0                                 5000+          DC    A(T136)
00006698  00006178                                 5001+          DC    A(T137)
0000669C  00006210                                 5002+          DC    A(T138)
000066A0  000062A8                                 5003+          DC    A(T139)
000066A4  00006340                                 5004+          DC    A(T140)
000066A8  000063D8                                 5005+          DC    A(T141)
                                                   5006+*
000066AC  00000000                                 5007+          DC    A(0)              END OF TABLE
000066B0  00000000                                 5008+          DC    A(0)
                                                   5009
000066B4  00000000                                 5010           DC    F'0'     END OF TABLE
000066B8  00000000                                 5011           DC    F'0'
```

```
  LOC        OBJECT CODE       ADDR1     ADDR2     STMT

                                         5013 ************************************************************************
                                         5014 *        Register equates
                                         5015 ************************************************************************


                             00000000  00000001  5017 R0       EQU   0
                             00000001  00000001  5018 R1       EQU   1
                             00000002  00000001  5019 R2       EQU   2
                             00000003  00000001  5020 R3       EQU   3
                             00000004  00000001  5021 R4       EQU   4
                             00000005  00000001  5022 R5       EQU   5
                             00000006  00000001  5023 R6       EQU   6
                             00000007  00000001  5024 R7       EQU   7
                             00000008  00000001  5025 R8       EQU   8
                             00000009  00000001  5026 R9       EQU   9
                             0000000A  00000001  5027 R10      EQU   10
                             0000000B  00000001  5028 R11      EQU   11
                             0000000C  00000001  5029 R12      EQU   12
                             0000000D  00000001  5030 R13      EQU   13
                             0000000E  00000001  5031 R14      EQU   14
                             0000000F  00000001  5032 R15      EQU   15


                                         5034 ************************************************************************
                                         5035 *        Register equates
                                         5036 ************************************************************************


                             00000000  00000001  5038 V0       EQU   0
                             00000001  00000001  5039 V1       EQU   1
                             00000002  00000001  5040 V2       EQU   2
                             00000003  00000001  5041 V3       EQU   3
                             00000004  00000001  5042 V4       EQU   4
                             00000005  00000001  5043 V5       EQU   5
                             00000006  00000001  5044 V6       EQU   6
                             00000007  00000001  5045 V7       EQU   7
                             00000008  00000001  5046 V8       EQU   8
                             00000009  00000001  5047 V9       EQU   9
                             0000000A  00000001  5048 V10      EQU   10
                             0000000B  00000001  5049 V11      EQU   11
                             0000000C  00000001  5050 V12      EQU   12
                             0000000D  00000001  5051 V13      EQU   13
                             0000000E  00000001  5052 V14      EQU   14
                             0000000F  00000001  5053 V15      EQU   15
                             00000010  00000001  5054 V16      EQU   16
                             00000011  00000001  5055 V17      EQU   17
                             00000012  00000001  5056 V18      EQU   18
                             00000013  00000001  5057 V19      EQU   19
                             00000014  00000001  5058 V20      EQU   20
                             00000015  00000001  5059 V21      EQU   21
```

```
  LOC         OBJECT CODE       ADDR1     ADDR2    STMT

                              00000016  00000001  5060 V22      EQU   22
                              00000017  00000001  5061 V23      EQU   23
                              00000018  00000001  5062 V24      EQU   24
                              00000019  00000001  5063 V25      EQU   25
                              0000001A  00000001  5064 V26      EQU   26
                              0000001B  00000001  5065 V27      EQU   27
                              0000001C  00000001  5066 V28      EQU   28
                              0000001D  00000001  5067 V29      EQU   29
                              0000001E  00000001  5068 V30      EQU   30
                              0000001F  00000001  5069 V31      EQU   31
                                                  5070
                                                  5071          END
```

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
BEGIN	I	00000200	2	165	131	161	162	163									
CTLR0	F	0000053C	4	394	175	176	177	178									
DECNUM	C	00001073	16	446	308	310	316	318									
E7TEST	4	00000000	64	460	257												
E7TESTS	F	00006478	4	4862	250												
EDIT	X	00001047	18	441	309	317											
ENDTEST	U	000003CE	1	294	255												
EOJ	I	00000520	4	384	210	243	297										
EOJPSW	D	00000510	8	382	384												
FAILCONT	U	000003BE	1	284													
FAILED	F	00001000	4	423	286	295											
FAILMSG	U	000003BA	1	278	268												
FAILPSW	D	00000528	8	386	388												
FAILTEST	I	00000538	4	388	298												
FB0001	F	00000280	8	194	198	199	201										
FB0002	F	00000330	8	227	231	232	234										
IMAGE	1	00000000	26300	0													
K	U	00000400	1	407	408	409	410										
K64	U	00010000	1	409													
M4	U	00000007	1	464	315												
MB	U	00100000	1	410													
MSG	I	00000458	4	344	209	242	327										
MSGCMD	C	000004A6	9	374	357	358											
MSGMSG	C	000004AF	95	375	351	372	349										
MSGMVC	I	000004A0	6	372	355												
MSGOK	I	0000046E	2	353	350												
MSGRET	I	0000048E	4	368	361	364											
MSGSAVE	F	00000494	4	371	347	368											
NEXTE7	U	00000384	1	252	271	289											
OPNAME	C	00000008	8	466	313												
PAGE	U	00001000	1	408													
PRT3	C	0000105D	18	444	309	310	311	317	318	319							
PRTLINE	C	00001008	16	429	436	326											
PRTLNG	U	0000003F	1	436	325												
PRTM4	C	00001044	2	434	319												
PRTNAME	C	00001033	8	432	313												
PRTNUM	C	00001018	3	430	311												
R0	U	00000000	1	5017	125	175	178	198	200	201	202	207	231	233	234	235	240
					259	260	285	286	324	325	328	344	347	349	351	353	368
R1	U	00000001	1	5018	208	241	266	267	295	296	326	358	372	594	595	596	597
					624	625	626	627	654	655	656	657	684	685	686	687	716
					717	718	719	746	747	748	749	776	777	778	779	806	807
					808	809	837	838	839	840	867	868	869	870	897	898	899
					900	927	928	929	930	958	959	960	961	988	989	990	991
					1018	1019	1020	1021	1048	1049	1050	1051	1079	1080	1081	1082	1109
					1110	1111	1112	1139	1140	1141	1142	1169	1170	1171	1172	1199	1200
					1201	1202	1229	1230	1231	1232	1259	1260	1261	1262	1289	1290	1291
					1292	1319	1320	1321	1322	1349	1350	1351	1352	1383	1384	1385	1386
					1413	1414	1415	1416	1443	1444	1445	1446	1473	1474	1475	1476	1504
					1505	1506	1507	1534	1535	1536	1537	1564	1565	1566	1567	1594	1595
					1596	1597	1625	1626	1627	1628	1655	1656	1657	1658	1685	1686	1687
					1688	1715	1716	1717	1718	1746	1747	1748	1749	1776	1777	1778	1779
					1806	1807	1808	1809	1836	1837	1838	1839	1867	1868	1869	1870	1897
					1898	1899	1900	1927	1928	1929	1930	1957	1958	1959	1960	1991	1992
					1993	1994	2021	2022	2023	2024	2051	2052	2053	2054	2081	2082	2083
					2084	2112	2113	2114	2115	2142	2143	2144	2145	2172	2173	2174	2175

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					2202	2203	2204	2205	2233	2234	2235	2236	2263	2264	2265	2266	2293
					2294	2295	2296	2323	2324	2325	2326	2354	2355	2356	2357	2384	2385
					2386	2387	2414	2415	2416	2417	2444	2445	2446	2447	2475	2476	2477
					2478	2505	2506	2507	2508	2535	2536	2537	2538	2565	2566	2567	2568
					2595	2596	2597	2598	2625	2626	2627	2628	2655	2656	2657	2658	2685
					2686	2687	2688	2715	2716	2717	2718	2745	2746	2747	2748	2775	2776
					2777	2778	2809	2810	2811	2812	2839	2840	2841	2842	2869	2870	2871
					2872	2899	2900	2901	2902	2930	2931	2932	2933	2960	2961	2962	2963
					2990	2991	2992	2993	3020	3021	3022	3023	3051	3052	3053	3054	3081
					3082	3083	3084	3111	3112	3113	3114	3141	3142	3143	3144	3172	3173
					3174	3175	3202	3203	3204	3205	3232	3233	3234	3235	3262	3263	3264
					3265	3292	3293	3294	3295	3326	3327	3328	3329	3356	3357	3358	3359
					3386	3387	3388	3389	3416	3417	3418	3419	3447	3448	3449	3450	3477
					3478	3479	3480	3507	3508	3509	3510	3537	3538	3539	3540	3568	3569
					3570	3571	3598	3599	3600	3601	3628	3629	3630	3631	3658	3659	3660
					3661	3689	3690	3691	3692	3719	3720	3721	3722	3749	3750	3751	3752
					3779	3780	3781	3782	3809	3810	3811	3812	3843	3844	3845	3846	3873
					3874	3875	3876	3903	3904	3905	3906	3933	3934	3935	3936	3964	3965
					3966	3967	3994	3995	3996	3997	4024	4025	4026	4027	4054	4055	4056
					4057	4085	4086	4087	4088	4115	4116	4117	4118	4145	4146	4147	4148
					4175	4176	4177	4178	4206	4207	4208	4209	4236	4237	4238	4239	4266
					4267	4268	4269	4296	4297	4298	4299	4326	4327	4328	4329	4360	4361
					4362	4363	4390	4391	4392	4393	4420	4421	4422	4423	4450	4451	4452
					4453	4481	4482	4483	4484	4511	4512	4513	4514	4541	4542	4543	4544
					4571	4572	4573	4574	4602	4603	4604	4605	4632	4633	4634	4635	4662
					4663	4664	4665	4692	4693	4694	4695	4723	4724	4725	4726	4753	4754
					4755	4756	4783	4784	4785	4786	4813	4814	4815	4816	4843	4844	4845
					4846												
R10	U	0000000A	1	5027	163	172	173										
R11	U	0000000B	1	5028	263	264	600	630	660	690	722	752	782	812	843	873	903
					933	964	994	1024	1054	1085	1115	1145	1175	1205	1235	1265	1295
					1325	1355	1389	1419	1449	1479	1510	1540	1570	1600	1631	1661	1691
					1721	1752	1782	1812	1842	1873	1903	1933	1963	1997	2027	2057	2087
					2118	2148	2178	2208	2239	2269	2299	2329	2360	2390	2420	2450	2481
					2511	2541	2571	2601	2631	2661	2691	2721	2751	2781	2815	2845	2875
					2905	2936	2966	2996	3026	3057	3087	3117	3147	3178	3208	3238	3268
					3298	3332	3362	3392	3422	3453	3483	3513	3543	3574	3604	3634	3664
					3695	3725	3755	3785	3815	3849	3879	3909	3939	3970	4000	4030	4060
					4091	4121	4151	4181	4212	4242	4272	4302	4332	4366	4396	4426	4456
					4487	4517	4547	4577	4608	4638	4668	4698	4729	4759	4789	4819	4849
R12	U	0000000C	1	5029	250	253	270	288									
R13	U	0000000D	1	5030													
R14	U	0000000E	1	5031													
R15	U	0000000F	1	5032	279	304	331	332									
R2	U	00000002	1	5019	209	242	307	308	315	316	324	327	328	345	347	353	354
					355	357	363	368	369								
R3	U	00000003	1	5020													
R4	U	00000004	1	5021													
R5	U	00000005	1	5022	253	254	257	305	330	579	602	609	632	639	662	669	692
					701	724	731	754	761	784	791	814	822	845	852	875	882
					905	912	935	943	966	973	996	1003	1026	1033	1056	1064	1087
					1094	1117	1124	1147	1154	1177	1184	1207	1214	1237	1244	1267	1274
					1297	1304	1327	1334	1357	1368	1391	1398	1421	1428	1451	1458	1481
					1489	1512	1519	1542	1549	1572	1579	1602	1610	1633	1640	1663	1670
					1693	1700	1723	1731	1754	1761	1784	1791	1814	1821	1844	1852	1875
					1882	1905	1912	1935	1942	1965	1976	1999	2006	2029	2036	2059	2066

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					2089	2097	2120	2127	2150	2157	2180	2187	2210	2218	2241	2248	2271
					2278	2301	2308	2331	2339	2362	2369	2392	2399	2422	2429	2452	2460
					2483	2490	2513	2520	2543	2550	2573	2580	2603	2610	2633	2640	2663
					2670	2693	2700	2723	2730	2753	2760	2783	2794	2817	2824	2847	2854
					2877	2884	2907	2915	2938	2945	2968	2975	2998	3005	3028	3036	3059
					3066	3089	3096	3119	3126	3149	3157	3180	3187	3210	3217	3240	3247
					3270	3277	3300	3311	3334	3341	3364	3371	3394	3401	3424	3432	3455
					3462	3485	3492	3515	3522	3545	3553	3576	3583	3606	3613	3636	3643
					3666	3674	3697	3704	3727	3734	3757	3764	3787	3794	3817	3828	3851
					3858	3881	3888	3911	3918	3941	3949	3972	3979	4002	4009	4032	4039
					4062	4070	4093	4100	4123	4130	4153	4160	4183	4191	4214	4221	4244
					4251	4274	4281	4304	4311	4334	4345	4368	4375	4398	4405	4428	4435
					4458	4466	4489	4496	4519	4526	4549	4556	4579	4587	4610	4617	4640
					4647	4670	4677	4700	4708	4731	4738	4761	4768	4791	4798	4821	4828
					4851												
R6	U	00000006	1	5023													
R7	U	00000007	1	5024													
R8	U	00000008	1	5025	161	165	166	167	169								
R9	U	00000009	1	5026	162	169	170	172									
RE1	F	00001120	4	601	585	586	588										
RE10	F	00001678	4	874	858	859	861										
RE100	F	00004BE8	4	3605	3589	3590	3592										
RE101	F	00004C80	4	3635	3619	3620	3622										
RE102	F	00004D18	4	3665	3649	3650	3652										
RE103	F	00004DB0	4	3696	3680	3681	3683										
RE104	F	00004E48	4	3726	3710	3711	3713										
RE105	F	00004EE0	4	3756	3740	3741	3743										
RE106	F	00004F78	4	3786	3770	3771	3773										
RE107	F	00005010	4	3816	3800	3801	3803										
RE108	F	000050A8	4	3850	3834	3835	3837										
RE109	F	00005140	4	3880	3864	3865	3867										
RE11	F	00001710	4	904	888	889	891										
RE110	F	000051D8	4	3910	3894	3895	3897										
RE111	F	00005270	4	3940	3924	3925	3927										
RE112	F	00005308	4	3971	3955	3956	3958										
RE113	F	000053A0	4	4001	3985	3986	3988										
RE114	F	00005438	4	4031	4015	4016	4018										
RE115	F	000054D0	4	4061	4045	4046	4048										
RE116	F	00005568	4	4092	4076	4077	4079										
RE117	F	00005600	4	4122	4106	4107	4109										
RE118	F	00005698	4	4152	4136	4137	4139										
RE119	F	00005730	4	4182	4166	4167	4169										
RE12	F	000017A8	4	934	918	919	921										
RE120	F	000057C8	4	4213	4197	4198	4200										
RE121	F	00005860	4	4243	4227	4228	4230										
RE122	F	000058F8	4	4273	4257	4258	4260										
RE123	F	00005990	4	4303	4287	4288	4290										
RE124	F	00005A28	4	4333	4317	4318	4320										
RE125	F	00005AC0	4	4367	4351	4352	4354										
RE126	F	00005B58	4	4397	4381	4382	4384										
RE127	F	00005BF0	4	4427	4411	4412	4414										
RE128	F	00005C88	4	4457	4441	4442	4444										
RE129	F	00005D20	4	4488	4472	4473	4475										
RE13	F	00001840	4	965	949	950	952										
RE130	F	00005DB8	4	4518	4502	4503	4505										
RE131	F	00005E50	4	4548	4532	4533	4535										

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE132	F	00005EE8	4	4578	4562	4563	4565
RE133	F	00005F80	4	4609	4593	4594	4596
RE134	F	00006018	4	4639	4623	4624	4626
RE135	F	000060B0	4	4669	4653	4654	4656
RE136	F	00006148	4	4699	4683	4684	4686
RE137	F	000061E0	4	4730	4714	4715	4717
RE138	F	00006278	4	4760	4744	4745	4747
RE139	F	00006310	4	4790	4774	4775	4777
RE14	F	000018D8	4	995	979	980	982
RE140	F	000063A8	4	4820	4804	4805	4807
RE141	F	00006440	4	4850	4834	4835	4837
RE15	F	00001970	4	1025	1009	1010	1012
RE16	F	00001A08	4	1055	1039	1040	1042
RE17	F	00001AA0	4	1086	1070	1071	1073
RE18	F	00001B38	4	1116	1100	1101	1103
RE19	F	00001BD0	4	1146	1130	1131	1133
RE2	F	000011B8	4	631	615	616	618
RE20	F	00001C68	4	1176	1160	1161	1163
RE21	F	00001D00	4	1206	1190	1191	1193
RE22	F	00001D98	4	1236	1220	1221	1223
RE23	F	00001E30	4	1266	1250	1251	1253
RE24	F	00001EC8	4	1296	1280	1281	1283
RE25	F	00001F60	4	1326	1310	1311	1313
RE26	F	00001FF8	4	1356	1340	1341	1343
RE27	F	00002090	4	1390	1374	1375	1377
RE28	F	00002128	4	1420	1404	1405	1407
RE29	F	000021C0	4	1450	1434	1435	1437
RE3	F	00001250	4	661	645	646	648
RE30	F	00002258	4	1480	1464	1465	1467
RE31	F	000022F0	4	1511	1495	1496	1498
RE32	F	00002388	4	1541	1525	1526	1528
RE33	F	00002420	4	1571	1555	1556	1558
RE34	F	000024B8	4	1601	1585	1586	1588
RE35	F	00002550	4	1632	1616	1617	1619
RE36	F	000025E8	4	1662	1646	1647	1649
RE37	F	00002680	4	1692	1676	1677	1679
RE38	F	00002718	4	1722	1706	1707	1709
RE39	F	000027B0	4	1753	1737	1738	1740
RE4	F	000012E8	4	691	675	676	678
RE40	F	00002848	4	1783	1767	1768	1770
RE41	F	000028E0	4	1813	1797	1798	1800
RE42	F	00002978	4	1843	1827	1828	1830
RE43	F	00002A10	4	1874	1858	1859	1861
RE44	F	00002AA8	4	1904	1888	1889	1891
RE45	F	00002B40	4	1934	1918	1919	1921
RE46	F	00002BD8	4	1964	1948	1949	1951
RE47	F	00002C70	4	1998	1982	1983	1985
RE48	F	00002D08	4	2028	2012	2013	2015
RE49	F	00002DA0	4	2058	2042	2043	2045
RE5	F	00001380	4	723	707	708	710
RE50	F	00002E38	4	2088	2072	2073	2075
RE51	F	00002ED0	4	2119	2103	2104	2106
RE52	F	00002F68	4	2149	2133	2134	2136
RE53	F	00003000	4	2179	2163	2164	2166
RE54	F	00003098	4	2209	2193	2194	2196
RE55	F	00003130	4	2240	2224	2225	2227

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES		
RE56	F	000031C8	4	2270	2254	2255	2257
RE57	F	00003260	4	2300	2284	2285	2287
RE58	F	000032F8	4	2330	2314	2315	2317
RE59	F	00003390	4	2361	2345	2346	2348
RE6	F	00001418	4	753	737	738	740
RE60	F	00003428	4	2391	2375	2376	2378
RE61	F	000034C0	4	2421	2405	2406	2408
RE62	F	00003558	4	2451	2435	2436	2438
RE63	F	000035F0	4	2482	2466	2467	2469
RE64	F	00003688	4	2512	2496	2497	2499
RE65	F	00003720	4	2542	2526	2527	2529
RE66	F	000037B8	4	2572	2556	2557	2559
RE67	F	00003850	4	2602	2586	2587	2589
RE68	F	000038E8	4	2632	2616	2617	2619
RE69	F	00003980	4	2662	2646	2647	2649
RE7	F	000014B0	4	783	767	768	770
RE70	F	00003A18	4	2692	2676	2677	2679
RE71	F	00003AB0	4	2722	2706	2707	2709
RE72	F	00003B48	4	2752	2736	2737	2739
RE73	F	00003BE0	4	2782	2766	2767	2769
RE74	F	00003C78	4	2816	2800	2801	2803
RE75	F	00003D10	4	2846	2830	2831	2833
RE76	F	00003DA8	4	2876	2860	2861	2863
RE77	F	00003E40	4	2906	2890	2891	2893
RE78	F	00003ED8	4	2937	2921	2922	2924
RE79	F	00003F70	4	2967	2951	2952	2954
RE8	F	00001548	4	813	797	798	800
RE80	F	00004008	4	2997	2981	2982	2984
RE81	F	000040A0	4	3027	3011	3012	3014
RE82	F	00004138	4	3058	3042	3043	3045
RE83	F	000041D0	4	3088	3072	3073	3075
RE84	F	00004268	4	3118	3102	3103	3105
RE85	F	00004300	4	3148	3132	3133	3135
RE86	F	00004398	4	3179	3163	3164	3166
RE87	F	00004430	4	3209	3193	3194	3196
RE88	F	000044C8	4	3239	3223	3224	3226
RE89	F	00004560	4	3269	3253	3254	3256
RE9	F	000015E0	4	844	828	829	831
RE90	F	000045F8	4	3299	3283	3284	3286
RE91	F	00004690	4	3333	3317	3318	3320
RE92	F	00004728	4	3363	3347	3348	3350
RE93	F	000047C0	4	3393	3377	3378	3380
RE94	F	00004858	4	3423	3407	3408	3410
RE95	F	000048F0	4	3454	3438	3439	3441
RE96	F	00004988	4	3484	3468	3469	3471
RE97	F	00004A20	4	3514	3498	3499	3501
RE98	F	00004AB8	4	3544	3528	3529	3531
RE99	F	00004B50	4	3575	3559	3560	3562
REA1	A	000010D4	4	588			
REA10	A	0000162C	4	861			
REA100	A	00004B9C	4	3592			
REA101	A	00004C34	4	3622			
REA102	A	00004CCC	4	3652			
REA103	A	00004D64	4	3683			
REA104	A	00004DFC	4	3713			
REA105	A	00004E94	4	3743			

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA106	A	00004F2C	4	3773	
REA107	A	00004FC4	4	3803	
REA108	A	0000505C	4	3837	
REA109	A	000050F4	4	3867	
REA11	A	000016C4	4	891	
REA110	A	0000518C	4	3897	
REA111	A	00005224	4	3927	
REA112	A	000052BC	4	3958	
REA113	A	00005354	4	3988	
REA114	A	000053EC	4	4018	
REA115	A	00005484	4	4048	
REA116	A	0000551C	4	4079	
REA117	A	000055B4	4	4109	
REA118	A	0000564C	4	4139	
REA119	A	000056E4	4	4169	
REA12	A	0000175C	4	921	
REA120	A	0000577C	4	4200	
REA121	A	00005814	4	4230	
REA122	A	000058AC	4	4260	
REA123	A	00005944	4	4290	
REA124	A	000059DC	4	4320	
REA125	A	00005A74	4	4354	
REA126	A	00005B0C	4	4384	
REA127	A	00005BA4	4	4414	
REA128	A	00005C3C	4	4444	
REA129	A	00005CD4	4	4475	
REA13	A	000017F4	4	952	
REA130	A	00005D6C	4	4505	
REA131	A	00005E04	4	4535	
REA132	A	00005E9C	4	4565	
REA133	A	00005F34	4	4596	
REA134	A	00005FCC	4	4626	
REA135	A	00006064	4	4656	
REA136	A	000060FC	4	4686	
REA137	A	00006194	4	4717	
REA138	A	0000622C	4	4747	
REA139	A	000062C4	4	4777	
REA14	A	0000188C	4	982	
REA140	A	0000635C	4	4807	
REA141	A	000063F4	4	4837	
REA15	A	00001924	4	1012	
REA16	A	000019BC	4	1042	
REA17	A	00001A54	4	1073	
REA18	A	00001AEC	4	1103	
REA19	A	00001B84	4	1133	
REA2	A	0000116C	4	618	
REA20	A	00001C1C	4	1163	
REA21	A	00001CB4	4	1193	
REA22	A	00001D4C	4	1223	
REA23	A	00001DE4	4	1253	
REA24	A	00001E7C	4	1283	
REA25	A	00001F14	4	1313	
REA26	A	00001FAC	4	1343	
REA27	A	00002044	4	1377	
REA28	A	000020DC	4	1407	
REA29	A	00002174	4	1437	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA3	A	00001204	4	648	
REA30	A	0000220C	4	1467	
REA31	A	000022A4	4	1498	
REA32	A	0000233C	4	1528	
REA33	A	000023D4	4	1558	
REA34	A	0000246C	4	1588	
REA35	A	00002504	4	1619	
REA36	A	0000259C	4	1649	
REA37	A	00002634	4	1679	
REA38	A	000026CC	4	1709	
REA39	A	00002764	4	1740	
REA4	A	0000129C	4	678	
REA40	A	000027FC	4	1770	
REA41	A	00002894	4	1800	
REA42	A	0000292C	4	1830	
REA43	A	000029C4	4	1861	
REA44	A	00002A5C	4	1891	
REA45	A	00002AF4	4	1921	
REA46	A	00002B8C	4	1951	
REA47	A	00002C24	4	1985	
REA48	A	00002CBC	4	2015	
REA49	A	00002D54	4	2045	
REA5	A	00001334	4	710	
REA50	A	00002DEC	4	2075	
REA51	A	00002E84	4	2106	
REA52	A	00002F1C	4	2136	
REA53	A	00002FB4	4	2166	
REA54	A	0000304C	4	2196	
REA55	A	000030E4	4	2227	
REA56	A	0000317C	4	2257	
REA57	A	00003214	4	2287	
REA58	A	000032AC	4	2317	
REA59	A	00003344	4	2348	
REA6	A	000013CC	4	740	
REA60	A	000033DC	4	2378	
REA61	A	00003474	4	2408	
REA62	A	0000350C	4	2438	
REA63	A	000035A4	4	2469	
REA64	A	0000363C	4	2499	
REA65	A	000036D4	4	2529	
REA66	A	0000376C	4	2559	
REA67	A	00003804	4	2589	
REA68	A	0000389C	4	2619	
REA69	A	00003934	4	2649	
REA7	A	00001464	4	770	
REA70	A	000039CC	4	2679	
REA71	A	00003A64	4	2709	
REA72	A	00003AFC	4	2739	
REA73	A	00003B94	4	2769	
REA74	A	00003C2C	4	2803	
REA75	A	00003CC4	4	2833	
REA76	A	00003D5C	4	2863	
REA77	A	00003DF4	4	2893	
REA78	A	00003E8C	4	2924	
REA79	A	00003F24	4	2954	
REA8	A	000014FC	4	800	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA80	A	00003FBC	4	2984		
REA81	A	00004054	4	3014		
REA82	A	000040EC	4	3045		
REA83	A	00004184	4	3075		
REA84	A	0000421C	4	3105		
REA85	A	000042B4	4	3135		
REA86	A	0000434C	4	3166		
REA87	A	000043E4	4	3196		
REA88	A	0000447C	4	3226		
REA89	A	00004514	4	3256		
REA9	A	00001594	4	831		
REA90	A	000045AC	4	3286		
REA91	A	00004644	4	3320		
REA92	A	000046DC	4	3350		
REA93	A	00004774	4	3380		
REA94	A	0000480C	4	3410		
REA95	A	000048A4	4	3441		
REA96	A	0000493C	4	3471		
REA97	A	000049D4	4	3501		
REA98	A	00004A6C	4	3531		
REA99	A	00004B04	4	3562		
READDR	A	0000001C	4	470	266	
REG2LOW	U	000000DD	1	413		
REG2PATT	U	AABBCCDD	1	412		
RELEN	A	00000018	4	469		
RPTDWSAV	D	00000448	8	337	324	328
RPTERROR	I	000003DC	4	304	279	
RPTSAVE	F	00000440	4	334	304	331
RPTSVR5	F	00000444	4	335	305	330
SKL0001	U	0000004E	1	191	207	
SKL0002	U	0000004E	1	224	240	
SKT0001	C	0000022A	20	188	191	208
SKT0002	C	000002D4	20	221	224	241
SVOLDPSW	U	00000140	0	127		
T1	A	000010B8	4	580	4865	
T10	A	00001610	4	853	4874	
T100	A	00004B80	4	3584	4964	
T101	A	00004C18	4	3614	4965	
T102	A	00004CB0	4	3644	4966	
T103	A	00004D48	4	3675	4967	
T104	A	00004DE0	4	3705	4968	
T105	A	00004E78	4	3735	4969	
T106	A	00004F10	4	3765	4970	
T107	A	00004FA8	4	3795	4971	
T108	A	00005040	4	3829	4972	
T109	A	000050D8	4	3859	4973	
T11	A	000016A8	4	883	4875	
T110	A	00005170	4	3889	4974	
T111	A	00005208	4	3919	4975	
T112	A	000052A0	4	3950	4976	
T113	A	00005338	4	3980	4977	
T114	A	000053D0	4	4010	4978	
T115	A	00005468	4	4040	4979	
T116	A	00005500	4	4071	4980	
T117	A	00005598	4	4101	4981	
T118	A	00005630	4	4131	4982	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T119	A	000056C8	4	4161	4983
T12	A	00001740	4	913	4876
T120	A	00005760	4	4192	4984
T121	A	000057F8	4	4222	4985
T122	A	00005890	4	4252	4986
T123	A	00005928	4	4282	4987
T124	A	000059C0	4	4312	4988
T125	A	00005A58	4	4346	4989
T126	A	00005AF0	4	4376	4990
T127	A	00005B88	4	4406	4991
T128	A	00005C20	4	4436	4992
T129	A	00005CB8	4	4467	4993
T13	A	000017D8	4	944	4877
T130	A	00005D50	4	4497	4994
T131	A	00005DE8	4	4527	4995
T132	A	00005E80	4	4557	4996
T133	A	00005F18	4	4588	4997
T134	A	00005FB0	4	4618	4998
T135	A	00006048	4	4648	4999
T136	A	000060E0	4	4678	5000
T137	A	00006178	4	4709	5001
T138	A	00006210	4	4739	5002
T139	A	000062A8	4	4769	5003
T14	A	00001870	4	974	4878
T140	A	00006340	4	4799	5004
T141	A	000063D8	4	4829	5005
T15	A	00001908	4	1004	4879
T16	A	000019A0	4	1034	4880
T17	A	00001A38	4	1065	4881
T18	A	00001AD0	4	1095	4882
T19	A	00001B68	4	1125	4883
T2	A	00001150	4	610	4866
T20	A	00001C00	4	1155	4884
T21	A	00001C98	4	1185	4885
T22	A	00001D30	4	1215	4886
T23	A	00001DC8	4	1245	4887
T24	A	00001E60	4	1275	4888
T25	A	00001EF8	4	1305	4889
T26	A	00001F90	4	1335	4890
T27	A	00002028	4	1369	4891
T28	A	000020C0	4	1399	4892
T29	A	00002158	4	1429	4893
T3	A	000011E8	4	640	4867
T30	A	000021F0	4	1459	4894
T31	A	00002288	4	1490	4895
T32	A	00002320	4	1520	4896
T33	A	000023B8	4	1550	4897
T34	A	00002450	4	1580	4898
T35	A	000024E8	4	1611	4899
T36	A	00002580	4	1641	4900
T37	A	00002618	4	1671	4901
T38	A	000026B0	4	1701	4902
T39	A	00002748	4	1732	4903
T4	A	00001280	4	670	4868
T40	A	000027E0	4	1762	4904
T41	A	00002878	4	1792	4905

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T42	A	00002910	4	1822	4906
T43	A	000029A8	4	1853	4907
T44	A	00002A40	4	1883	4908
T45	A	00002AD8	4	1913	4909
T46	A	00002B70	4	1943	4910
T47	A	00002C08	4	1977	4911
T48	A	00002CA0	4	2007	4912
T49	A	00002D38	4	2037	4913
T5	A	00001318	4	702	4869
T50	A	00002DD0	4	2067	4914
T51	A	00002E68	4	2098	4915
T52	A	00002F00	4	2128	4916
T53	A	00002F98	4	2158	4917
T54	A	00003030	4	2188	4918
T55	A	000030C8	4	2219	4919
T56	A	00003160	4	2249	4920
T57	A	000031F8	4	2279	4921
T58	A	00003290	4	2309	4922
T59	A	00003328	4	2340	4923
T6	A	000013B0	4	732	4870
T60	A	000033C0	4	2370	4924
T61	A	00003458	4	2400	4925
T62	A	000034F0	4	2430	4926
T63	A	00003588	4	2461	4927
T64	A	00003620	4	2491	4928
T65	A	000036B8	4	2521	4929
T66	A	00003750	4	2551	4930
T67	A	000037E8	4	2581	4931
T68	A	00003880	4	2611	4932
T69	A	00003918	4	2641	4933
T7	A	00001448	4	762	4871
T70	A	000039B0	4	2671	4934
T71	A	00003A48	4	2701	4935
T72	A	00003AE0	4	2731	4936
T73	A	00003B78	4	2761	4937
T74	A	00003C10	4	2795	4938
T75	A	00003CA8	4	2825	4939
T76	A	00003D40	4	2855	4940
T77	A	00003DD8	4	2885	4941
T78	A	00003E70	4	2916	4942
T79	A	00003F08	4	2946	4943
T8	A	000014E0	4	792	4872
T80	A	00003FA0	4	2976	4944
T81	A	00004038	4	3006	4945
T82	A	000040D0	4	3037	4946
T83	A	00004168	4	3067	4947
T84	A	00004200	4	3097	4948
T85	A	00004298	4	3127	4949
T86	A	00004330	4	3158	4950
T87	A	000043C8	4	3188	4951
T88	A	00004460	4	3218	4952
T89	A	000044F8	4	3248	4953
T9	A	00001578	4	823	4873
T90	A	00004590	4	3278	4954
T91	A	00004628	4	3312	4955
T92	A	000046C0	4	3342	4956

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
T93	A	00004758	4	3372	4957	
T94	A	000047F0	4	3402	4958	
T95	A	00004888	4	3433	4959	
T96	A	00004920	4	3463	4960	
T97	A	000049B8	4	3493	4961	
T98	A	00004A50	4	3523	4962	
T99	A	00004AE8	4	3554	4963	
TESTING	F	00001004	4	424	260	
TNUM	H	00000004	2	462	259	307
TSUB	A	00000000	4	461	263	
TTABLE	F	00006478	4	4864		
V0	U	00000000	1	5038		
V1	U	00000001	1	5039	262	
V10	U	0000000A	1	5048		
V11	U	0000000B	1	5049		
V12	U	0000000C	1	5050		
V13	U	0000000D	1	5051		
V14	U	0000000E	1	5052		
V15	U	0000000F	1	5053		
V16	U	00000010	1	5054		
V17	U	00000011	1	5055		
V18	U	00000012	1	5056		
V19	U	00000013	1	5057		
V1FUDGE	X	00001094	16	453	262	
V1O1	X	000010E0	16	590	599	
V1O10	X	00001638	16	863	872	
V1O100	X	00004BA8	16	3594	3603	
V1O101	X	00004C40	16	3624	3633	
V1O102	X	00004CD8	16	3654	3663	
V1O103	X	00004D70	16	3685	3694	
V1O104	X	00004E08	16	3715	3724	
V1O105	X	00004EA0	16	3745	3754	
V1O106	X	00004F38	16	3775	3784	
V1O107	X	00004FD0	16	3805	3814	
V1O108	X	00005068	16	3839	3848	
V1O109	X	00005100	16	3869	3878	
V1O11	X	000016D0	16	893	902	
V1O110	X	00005198	16	3899	3908	
V1O111	X	00005230	16	3929	3938	
V1O112	X	000052C8	16	3960	3969	
V1O113	X	00005360	16	3990	3999	
V1O114	X	000053F8	16	4020	4029	
V1O115	X	00005490	16	4050	4059	
V1O116	X	00005528	16	4081	4090	
V1O117	X	000055C0	16	4111	4120	
V1O118	X	00005658	16	4141	4150	
V1O119	X	000056F0	16	4171	4180	
V1O12	X	00001768	16	923	932	
V1O120	X	00005788	16	4202	4211	
V1O121	X	00005820	16	4232	4241	
V1O122	X	000058B8	16	4262	4271	
V1O123	X	00005950	16	4292	4301	
V1O124	X	000059E8	16	4322	4331	
V1O125	X	00005A80	16	4356	4365	
V1O126	X	00005B18	16	4386	4395	
V1O127	X	00005BB0	16	4416	4425	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1O128	X	00005C48	16	4446	4455
V1O129	X	00005CE0	16	4477	4486
V1O13	X	00001800	16	954	963
V1O130	X	00005D78	16	4507	4516
V1O131	X	00005E10	16	4537	4546
V1O132	X	00005EA8	16	4567	4576
V1O133	X	00005F40	16	4598	4607
V1O134	X	00005FD8	16	4628	4637
V1O135	X	00006070	16	4658	4667
V1O136	X	00006108	16	4688	4697
V1O137	X	000061A0	16	4719	4728
V1O138	X	00006238	16	4749	4758
V1O139	X	000062D0	16	4779	4788
V1O14	X	00001898	16	984	993
V1O140	X	00006368	16	4809	4818
V1O141	X	00006400	16	4839	4848
V1O15	X	00001930	16	1014	1023
V1O16	X	000019C8	16	1044	1053
V1O17	X	00001A60	16	1075	1084
V1O18	X	00001AF8	16	1105	1114
V1O19	X	00001B90	16	1135	1144
V1O2	X	00001178	16	620	629
V1O20	X	00001C28	16	1165	1174
V1O21	X	00001CC0	16	1195	1204
V1O22	X	00001D58	16	1225	1234
V1O23	X	00001DF0	16	1255	1264
V1O24	X	00001E88	16	1285	1294
V1O25	X	00001F20	16	1315	1324
V1O26	X	00001FB8	16	1345	1354
V1O27	X	00002050	16	1379	1388
V1O28	X	000020E8	16	1409	1418
V1O29	X	00002180	16	1439	1448
V1O3	X	00001210	16	650	659
V1O30	X	00002218	16	1469	1478
V1O31	X	000022B0	16	1500	1509
V1O32	X	00002348	16	1530	1539
V1O33	X	000023E0	16	1560	1569
V1O34	X	00002478	16	1590	1599
V1O35	X	00002510	16	1621	1630
V1O36	X	000025A8	16	1651	1660
V1O37	X	00002640	16	1681	1690
V1O38	X	000026D8	16	1711	1720
V1O39	X	00002770	16	1742	1751
V1O4	X	000012A8	16	680	689
V1O40	X	00002808	16	1772	1781
V1O41	X	000028A0	16	1802	1811
V1O42	X	00002938	16	1832	1841
V1O43	X	000029D0	16	1863	1872
V1O44	X	00002A68	16	1893	1902
V1O45	X	00002B00	16	1923	1932
V1O46	X	00002B98	16	1953	1962
V1O47	X	00002C30	16	1987	1996
V1O48	X	00002CC8	16	2017	2026
V1O49	X	00002D60	16	2047	2056
V1O5	X	00001340	16	712	721
V1O50	X	00002DF8	16	2077	2086

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V1051	X	00002E90	16	2108	2117
V1052	X	00002F28	16	2138	2147
V1053	X	00002FC0	16	2168	2177
V1054	X	00003058	16	2198	2207
V1055	X	000030F0	16	2229	2238
V1056	X	00003188	16	2259	2268
V1057	X	00003220	16	2289	2298
V1058	X	000032B8	16	2319	2328
V1059	X	00003350	16	2350	2359
V106	X	000013D8	16	742	751
V1060	X	000033E8	16	2380	2389
V1061	X	00003480	16	2410	2419
V1062	X	00003518	16	2440	2449
V1063	X	000035B0	16	2471	2480
V1064	X	00003648	16	2501	2510
V1065	X	000036E0	16	2531	2540
V1066	X	00003778	16	2561	2570
V1067	X	00003810	16	2591	2600
V1068	X	000038A8	16	2621	2630
V1069	X	00003940	16	2651	2660
V107	X	00001470	16	772	781
V1070	X	000039D8	16	2681	2690
V1071	X	00003A70	16	2711	2720
V1072	X	00003B08	16	2741	2750
V1073	X	00003BA0	16	2771	2780
V1074	X	00003C38	16	2805	2814
V1075	X	00003CD0	16	2835	2844
V1076	X	00003D68	16	2865	2874
V1077	X	00003E00	16	2895	2904
V1078	X	00003E98	16	2926	2935
V1079	X	00003F30	16	2956	2965
V108	X	00001508	16	802	811
V1080	X	00003FC8	16	2986	2995
V1081	X	00004060	16	3016	3025
V1082	X	000040F8	16	3047	3056
V1083	X	00004190	16	3077	3086
V1084	X	00004228	16	3107	3116
V1085	X	000042C0	16	3137	3146
V1086	X	00004358	16	3168	3177
V1087	X	000043F0	16	3198	3207
V1088	X	00004488	16	3228	3237
V1089	X	00004520	16	3258	3267
V109	X	000015A0	16	833	842
V1090	X	000045B8	16	3288	3297
V1091	X	00004650	16	3322	3331
V1092	X	000046E8	16	3352	3361
V1093	X	00004780	16	3382	3391
V1094	X	00004818	16	3412	3421
V1095	X	000048B0	16	3443	3452
V1096	X	00004948	16	3473	3482
V1097	X	000049E0	16	3503	3512
V1098	X	00004A78	16	3533	3542
V1099	X	00004B10	16	3564	3573
V1OUTPUT	X	00000028	16	472	267
V2	U	00000002	1	5040	
V20	U	00000014	1	5058	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V21	U	00000015	1	5059													
V22	U	00000016	1	5060	595	598	599	625	628	629	655	658	659	685	688	689	717
					720	721	747	750	751	777	780	781	807	810	811	838	841
					842	868	871	872	898	901	902	928	931	932	959	962	963
					989	992	993	1019	1022	1023	1049	1052	1053	1080	1083	1084	1110
					1113	1114	1140	1143	1144	1170	1173	1174	1200	1203	1204	1230	1233
					1234	1260	1263	1264	1290	1293	1294	1320	1323	1324	1350	1353	1354
					1384	1387	1388	1414	1417	1418	1444	1447	1448	1474	1477	1478	1505
					1508	1509	1535	1538	1539	1565	1568	1569	1595	1598	1599	1626	1629
					1630	1656	1659	1660	1686	1689	1690	1716	1719	1720	1747	1750	1751
					1777	1780	1781	1807	1810	1811	1837	1840	1841	1868	1871	1872	1898
					1901	1902	1928	1931	1932	1958	1961	1962	1992	1995	1996	2022	2025
					2026	2052	2055	2056	2082	2085	2086	2113	2116	2117	2143	2146	2147
					2173	2176	2177	2203	2206	2207	2234	2237	2238	2264	2267	2268	2294
					2297	2298	2324	2327	2328	2355	2358	2359	2385	2388	2389	2415	2418
					2419	2445	2448	2449	2476	2479	2480	2506	2509	2510	2536	2539	2540
					2566	2569	2570	2596	2599	2600	2626	2629	2630	2656	2659	2660	2686
					2689	2690	2716	2719	2720	2746	2749	2750	2776	2779	2780	2810	2813
					2814	2840	2843	2844	2870	2873	2874	2900	2903	2904	2931	2934	2935
					2961	2964	2965	2991	2994	2995	3021	3024	3025	3052	3055	3056	3082
					3085	3086	3112	3115	3116	3142	3145	3146	3173	3176	3177	3203	3206
					3207	3233	3236	3237	3263	3266	3267	3293	3296	3297	3327	3330	3331
					3357	3360	3361	3387	3390	3391	3417	3420	3421	3448	3451	3452	3478
					3481	3482	3508	3511	3512	3538	3541	3542	3569	3572	3573	3599	3602
					3603	3629	3632	3633	3659	3662	3663	3690	3693	3694	3720	3723	3724
					3750	3753	3754	3780	3783	3784	3810	3813	3814	3844	3847	3848	3874
					3877	3878	3904	3907	3908	3934	3937	3938	3965	3968	3969	3995	3998
					3999	4025	4028	4029	4055	4058	4059	4086	4089	4090	4116	4119	4120
					4146	4149	4150	4176	4179	4180	4207	4210	4211	4237	4240	4241	4267
					4270	4271	4297	4300	4301	4327	4330	4331	4361	4364	4365	4391	4394
					4395	4421	4424	4425	4451	4454	4455	4482	4485	4486	4512	4515	4516
					4542	4545	4546	4572	4575	4576	4603	4606	4607	4633	4636	4637	4663
					4666	4667	4693	4696	4697	4724	4727	4728	4754	4757	4758	4784	4787
					4788	4814	4817	4818	4844	4847	4848						
V23	U	00000017	1	5061	597	598	627	628	657	658	687	688	719	720	749	750	779
					780	809	810	840	841	870	871	900	901	930	931	961	962
					991	992	1021	1022	1051	1052	1082	1083	1112	1113	1142	1143	1172
					1173	1202	1203	1232	1233	1262	1263	1292	1293	1322	1323	1352	1353
					1386	1387	1416	1417	1446	1447	1476	1477	1507	1508	1537	1538	1567
					1568	1597	1598	1628	1629	1658	1659	1688	1689	1718	1719	1749	1750
					1779	1780	1809	1810	1839	1840	1870	1871	1900	1901	1930	1931	1960
					1961	1994	1995	2024	2025	2054	2055	2084	2085	2115	2116	2145	2146
					2175	2176	2205	2206	2236	2237	2266	2267	2296	2297	2326	2327	2357
					2358	2387	2388	2417	2418	2447	2448	2478	2479	2508	2509	2538	2539
					2568	2569	2598	2599	2628	2629	2658	2659	2688	2689	2718	2719	2748
					2749	2778	2779	2812	2813	2842	2843	2872	2873	2902	2903	2933	2934
					2963	2964	2993	2994	3023	3024	3054	3055	3084	3085	3114	3115	3144
					3145	3175	3176	3205	3206	3235	3236	3265	3266	3295	3296	3329	3330
					3359	3360	3389	3390	3419	3420	3450	3451	3480	3481	3510	3511	3540
					3541	3571	3572	3601	3602	3631	3632	3661	3662	3692	3693	3722	3723
					3752	3753	3782	3783	3812	3813	3846	3847	3876	3877	3906	3907	3936
					3937	3967	3968	3997	3998	4027	4028	4057	4058	4088	4089	4118	4119
					4148	4149	4178	4179	4209	4210	4239	4240	4269	4270	4299	4300	4329
					4330	4363	4364	4393	4394	4423	4424	4453	4454	4484	4485	4514	4515
					4544	4545	4574	4575	4605	4606	4635	4636	4665	4666	4695	4696	4726
					4727	4756	4757	4786	4787	4816	4817	4846	4847				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V24	U	00000018	1	5062													
V25	U	00000019	1	5063													
V26	U	0000001A	1	5064													
V27	U	0000001B	1	5065													
V28	U	0000001C	1	5066													
V29	U	0000001D	1	5067													
V2ADDR	A	00000010	4	467	594	624	654	684	716	746	776	806	837	867	897	927	958
					988	1018	1048	1079	1109	1139	1169	1199	1229	1259	1289	1319	1349
					1383	1413	1443	1473	1504	1534	1564	1594	1625	1655	1685	1715	1746
					1776	1806	1836	1867	1897	1927	1957	1991	2021	2051	2081	2112	2142
					2172	2202	2233	2263	2293	2323	2354	2384	2414	2444	2475	2505	2535
					2565	2595	2625	2655	2685	2715	2745	2775	2809	2839	2869	2899	2930
					2960	2990	3020	3051	3081	3111	3141	3172	3202	3232	3262	3292	3326
					3356	3386	3416	3447	3477	3507	3537	3568	3598	3628	3658	3689	3719
					3749	3779	3809	3843	3873	3903	3933	3964	3994	4024	4054	4085	4115
					4145	4175	4206	4236	4266	4296	4326	4360	4390	4420	4450	4481	4511
					4541	4571	4602	4632	4662	4692	4723	4753	4783	4813	4843		
V3	U	00000003	1	5041													
V30	U	0000001E	1	5068													
V31	U	0000001F	1	5069													
V3ADDR	A	00000014	4	468	596	626	656	686	718	748	778	808	839	869	899	929	960
					990	1020	1050	1081	1111	1141	1171	1201	1231	1261	1291	1321	1351
					1385	1415	1445	1475	1506	1536	1566	1596	1627	1657	1687	1717	1748
					1778	1808	1838	1869	1899	1929	1959	1993	2023	2053	2083	2114	2144
					2174	2204	2235	2265	2295	2325	2356	2386	2416	2446	2477	2507	2537
					2567	2597	2627	2657	2687	2717	2747	2777	2811	2841	2871	2901	2932
					2962	2992	3022	3053	3083	3113	3143	3174	3204	3234	3264	3294	3328
					3358	3388	3418	3449	3479	3509	3539	3570	3600	3630	3660	3691	3721
					3751	3781	3811	3845	3875	3905	3935	3966	3996	4026	4056	4087	4117
					4147	4177	4208	4238	4268	4298	4328	4362	4392	4422	4452	4483	4513
					4543	4573	4604	4634	4664	4694	4725	4755	4785	4815	4845		
V4	U	00000004	1	5042													
V5	U	00000005	1	5043													
V6	U	00000006	1	5044													
V7	U	00000007	1	5045													
V8	U	00000008	1	5046													
V9	U	00000009	1	5047													
X0001	U	000002A8	1	197	185	198											
X0002	U	00000358	1	230	218	231											
X1	F	000010F8	4	593	580												
X10	F	00001650	4	866	853												
X100	F	00004BC0	4	3597	3584												
X101	F	00004C58	4	3627	3614												
X102	F	00004CF0	4	3657	3644												
X103	F	00004D88	4	3688	3675												
X104	F	00004E20	4	3718	3705												
X105	F	00004EB8	4	3748	3735												
X106	F	00004F50	4	3778	3765												
X107	F	00004FE8	4	3808	3795												
X108	F	00005080	4	3842	3829												
X109	F	00005118	4	3872	3859												
X11	F	000016E8	4	896	883												
X110	F	000051B0	4	3902	3889												
X111	F	00005248	4	3932	3919												
X112	F	000052E0	4	3963	3950												
X113	F	00005378	4	3993	3980												

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X114	F	00005410	4	4023	4010
X115	F	000054A8	4	4053	4040
X116	F	00005540	4	4084	4071
X117	F	000055D8	4	4114	4101
X118	F	00005670	4	4144	4131
X119	F	00005708	4	4174	4161
X12	F	00001780	4	926	913
X120	F	000057A0	4	4205	4192
X121	F	00005838	4	4235	4222
X122	F	000058D0	4	4265	4252
X123	F	00005968	4	4295	4282
X124	F	00005A00	4	4325	4312
X125	F	00005A98	4	4359	4346
X126	F	00005B30	4	4389	4376
X127	F	00005BC8	4	4419	4406
X128	F	00005C60	4	4449	4436
X129	F	00005CF8	4	4480	4467
X13	F	00001818	4	957	944
X130	F	00005D90	4	4510	4497
X131	F	00005E28	4	4540	4527
X132	F	00005EC0	4	4570	4557
X133	F	00005F58	4	4601	4588
X134	F	00005FF0	4	4631	4618
X135	F	00006088	4	4661	4648
X136	F	00006120	4	4691	4678
X137	F	000061B8	4	4722	4709
X138	F	00006250	4	4752	4739
X139	F	000062E8	4	4782	4769
X14	F	000018B0	4	987	974
X140	F	00006380	4	4812	4799
X141	F	00006418	4	4842	4829
X15	F	00001948	4	1017	1004
X16	F	000019E0	4	1047	1034
X17	F	00001A78	4	1078	1065
X18	F	00001B10	4	1108	1095
X19	F	00001BA8	4	1138	1125
X2	F	00001190	4	623	610
X20	F	00001C40	4	1168	1155
X21	F	00001CD8	4	1198	1185
X22	F	00001D70	4	1228	1215
X23	F	00001E08	4	1258	1245
X24	F	00001EA0	4	1288	1275
X25	F	00001F38	4	1318	1305
X26	F	00001FD0	4	1348	1335
X27	F	00002068	4	1382	1369
X28	F	00002100	4	1412	1399
X29	F	00002198	4	1442	1429
X3	F	00001228	4	653	640
X30	F	00002230	4	1472	1459
X31	F	000022C8	4	1503	1490
X32	F	00002360	4	1533	1520
X33	F	000023F8	4	1563	1550
X34	F	00002490	4	1593	1580
X35	F	00002528	4	1624	1611
X36	F	000025C0	4	1654	1641
X37	F	00002658	4	1684	1671

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X38	F	000026F0	4	1714	1701
X39	F	00002788	4	1745	1732
X4	F	000012C0	4	683	670
X40	F	00002820	4	1775	1762
X41	F	000028B8	4	1805	1792
X42	F	00002950	4	1835	1822
X43	F	000029E8	4	1866	1853
X44	F	00002A80	4	1896	1883
X45	F	00002B18	4	1926	1913
X46	F	00002BB0	4	1956	1943
X47	F	00002C48	4	1990	1977
X48	F	00002CE0	4	2020	2007
X49	F	00002D78	4	2050	2037
X5	F	00001358	4	715	702
X50	F	00002E10	4	2080	2067
X51	F	00002EA8	4	2111	2098
X52	F	00002F40	4	2141	2128
X53	F	00002FD8	4	2171	2158
X54	F	00003070	4	2201	2188
X55	F	00003108	4	2232	2219
X56	F	000031A0	4	2262	2249
X57	F	00003238	4	2292	2279
X58	F	000032D0	4	2322	2309
X59	F	00003368	4	2353	2340
X6	F	000013F0	4	745	732
X60	F	00003400	4	2383	2370
X61	F	00003498	4	2413	2400
X62	F	00003530	4	2443	2430
X63	F	000035C8	4	2474	2461
X64	F	00003660	4	2504	2491
X65	F	000036F8	4	2534	2521
X66	F	00003790	4	2564	2551
X67	F	00003828	4	2594	2581
X68	F	000038C0	4	2624	2611
X69	F	00003958	4	2654	2641
X7	F	00001488	4	775	762
X70	F	000039F0	4	2684	2671
X71	F	00003A88	4	2714	2701
X72	F	00003B20	4	2744	2731
X73	F	00003BB8	4	2774	2761
X74	F	00003C50	4	2808	2795
X75	F	00003CE8	4	2838	2825
X76	F	00003D80	4	2868	2855
X77	F	00003E18	4	2898	2885
X78	F	00003EB0	4	2929	2916
X79	F	00003F48	4	2959	2946
X8	F	00001520	4	805	792
X80	F	00003FE0	4	2989	2976
X81	F	00004078	4	3019	3006
X82	F	00004110	4	3050	3037
X83	F	000041A8	4	3080	3067
X84	F	00004240	4	3110	3097
X85	F	000042D8	4	3140	3127
X86	F	00004370	4	3171	3158
X87	F	00004408	4	3201	3188
X88	F	000044A0	4	3231	3218

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES					
X89	F	00004538	4	3261	3248					
X9	F	000015B8	4	836	823					
X90	F	000045D0	4	3291	3278					
X91	F	00004668	4	3325	3312					
X92	F	00004700	4	3355	3342					
X93	F	00004798	4	3385	3372					
X94	F	00004830	4	3415	3402					
X95	F	000048C8	4	3446	3433					
X96	F	00004960	4	3476	3463					
X97	F	000049F8	4	3506	3493					
X98	F	00004A90	4	3536	3523					
X99	F	00004B28	4	3567	3554					
XC0001	U	000002D0	1	211	203					
XC0002	U	00000380	1	244	236					
ZVE7TST	J	00000000	26300	124	127	129	133	137	422	125
=A(E7TESTS)	A	0000054C	4	400	250					
=AL2(L'MSGMSG)	R	00000556	2	403	349					
=F'1'	F	00000550	4	401	285					
=F'2'	F	00000548	4	399	235					
=F'64'	F	00000544	4	398	202					
=H'0'	H	00000554	2	402	344					

```
 MACRO   DEFN  REFERENCES

FCHECK     77    184    217
PTTABLE   536   4863
VRR_C     491    577    607    637    667    699    729    759    789    820    850    880    910    941    971   1001   1031   1062
                1092   1122   1152   1182   1212   1242   1272   1302   1332   1366   1396   1426   1456   1487   1517   1547   1577
                1608   1638   1668   1698   1729   1759   1789   1819   1850   1880   1910   1940   1974   2004   2034   2064   2095
                2125   2155   2185   2216   2246   2276   2306   2337   2367   2397   2427   2458   2488   2518   2548   2578   2608
                2638   2668   2698   2728   2758   2792   2822   2852   2882   2913   2943   2973   3003   3034   3064   3094   3124
                3155   3185   3215   3245   3275   3309   3339   3369   3399   3430   3460   3490   3520   3551   3581   3611   3641
                3672   3702   3732   3762   3792   3826   3856   3886   3916   3947   3977   4007   4037   4068   4098   4128   4158
                4189   4219   4249   4279   4309   4343   4373   4403   4433   4464   4494   4524   4554   4585   4615   4645   4675
                4706   4736   4766   4796   4826
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   DESC     SYMBOL   SIZE     POS        ADDR

Entry: 0

Image      IMAGE    26300  0000-66BB  0000-66BB
  Region            26300  0000-66BB  0000-66BB
    CSECT  ZVE7TST  26300  0000-66BB  0000-66BB
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   STMT                        FILE NAME
1     /devstor/sharedvfp/tests/zvector-e7-09-multiply.asm

** NO ERRORS FOUND **
```