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PAGE 1 - TITLE
PAGE 2 - Block Diagram
PAGE 3 - FPGA Power
PAGE 4 - JTAG, Clocking
PAGE 5 - DDR4 SDRAM
PAGE 6 - BANK 4, Transceivers
PAGE 7 - BANK 2
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Revision History
0.1 - 17.12.2020
SHEET 4 - Changed net names acording to transceivers;
1.0 - 02 Jun 2022
SHEET 3 - Changed DA1 from EN63A0QA to MYMGK1R820FRSR
SHEET 4 - Added Green, Red User LEDs in 0201 package
- 13 Jun 2022
SHEET 2 - Added Block Diagram

PCB NOTE: DDR4 chips on page 5
must accept single and dual die chips,
Chip max dimensions is 14x10.5mm

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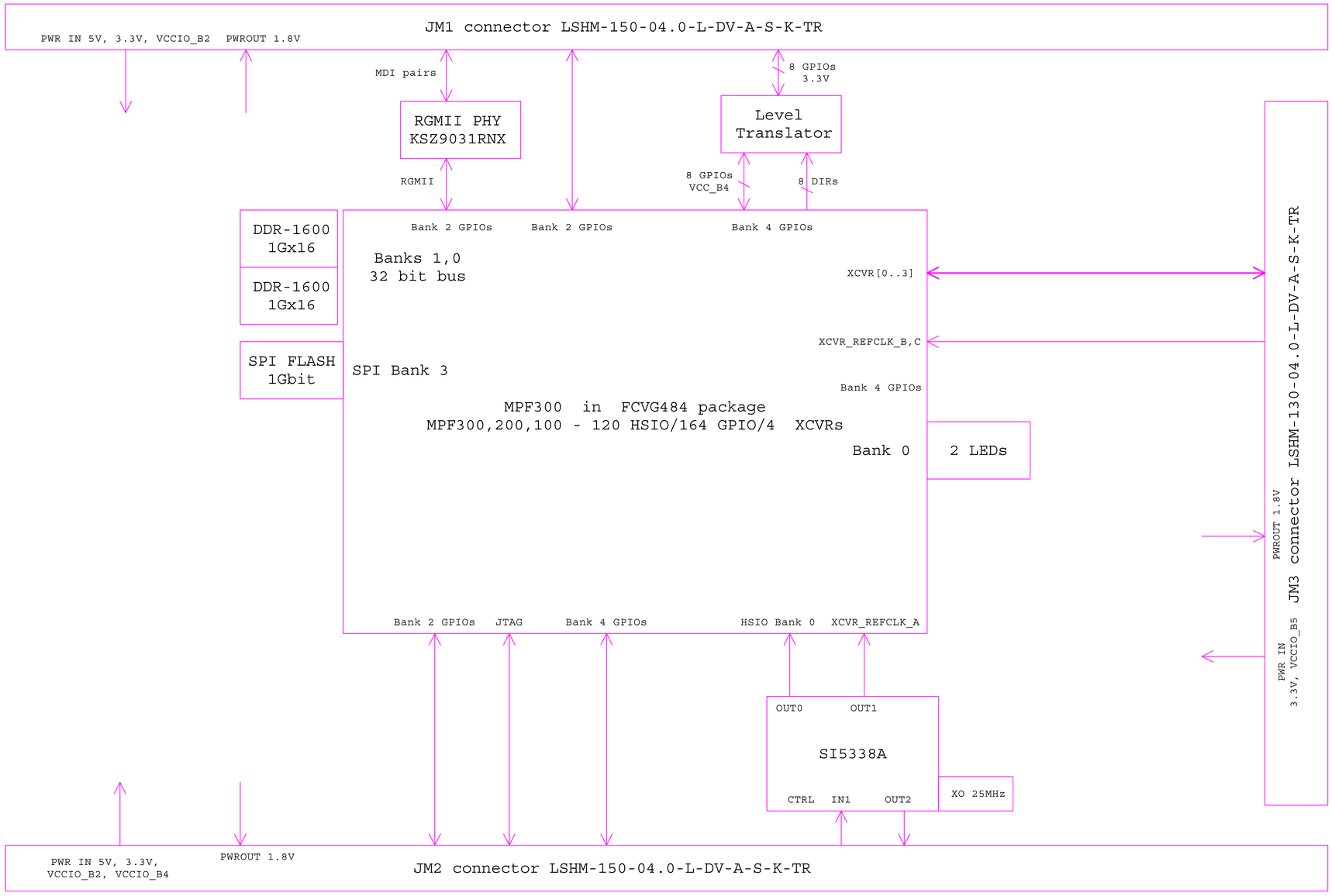
Block Diagram



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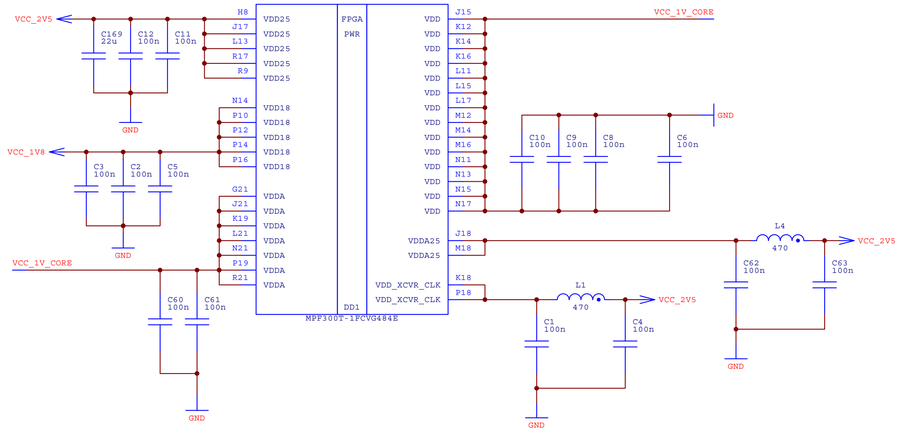
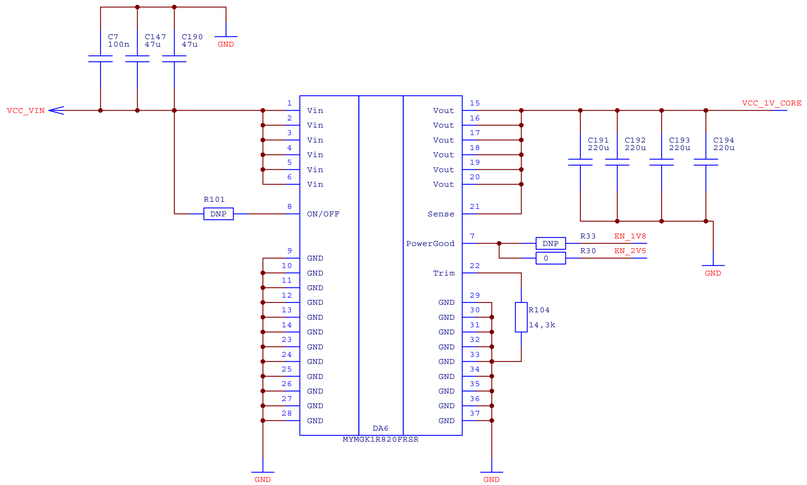
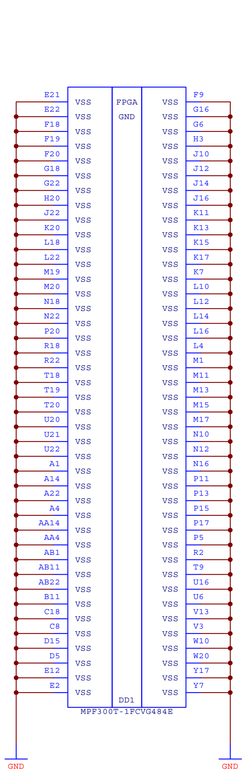
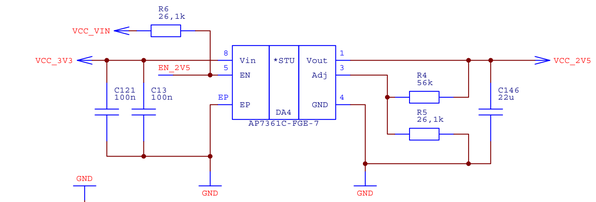
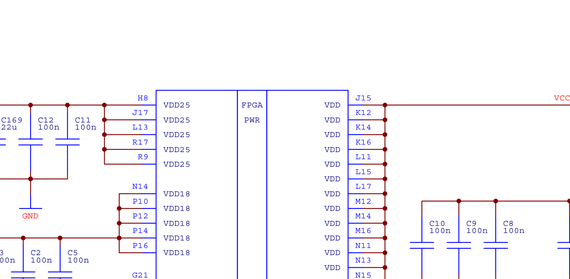
FPGA Power

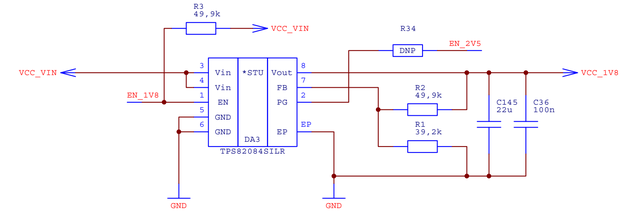


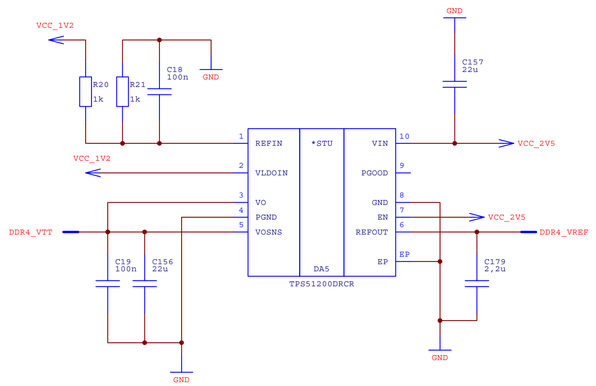












Power Sequence per ERRATA

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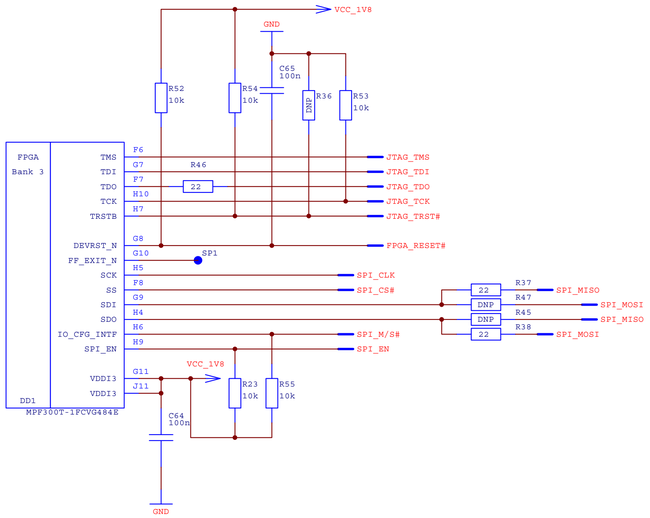
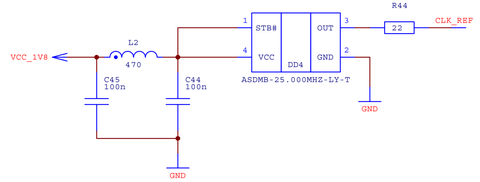
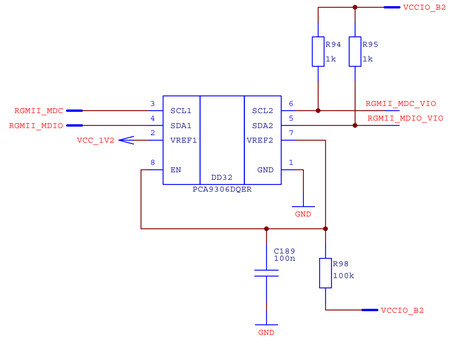
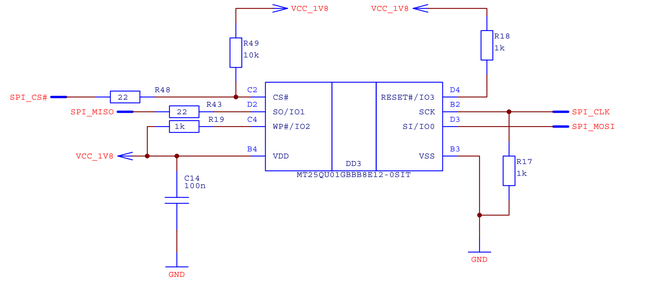
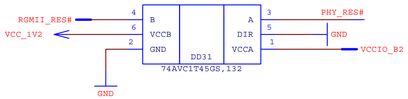
JTAG, Clocking

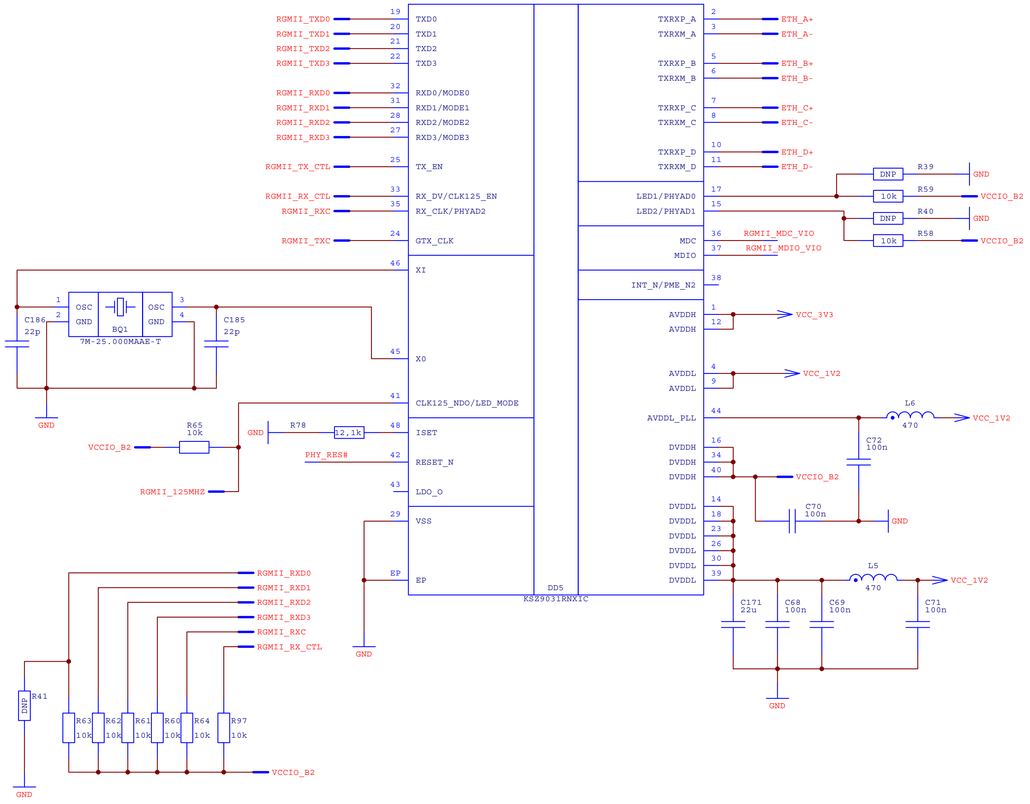


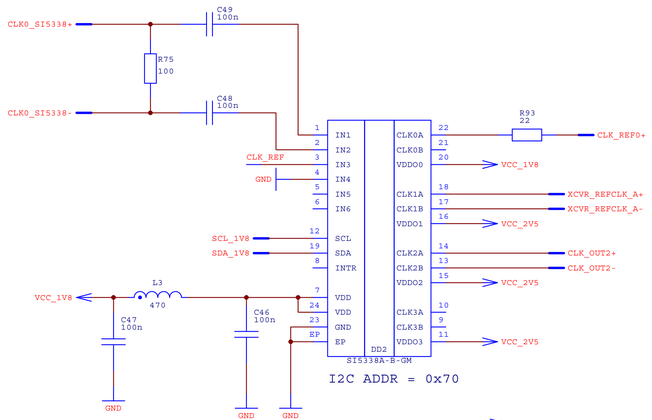


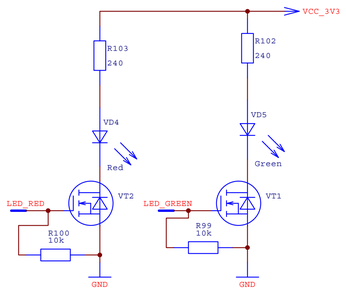












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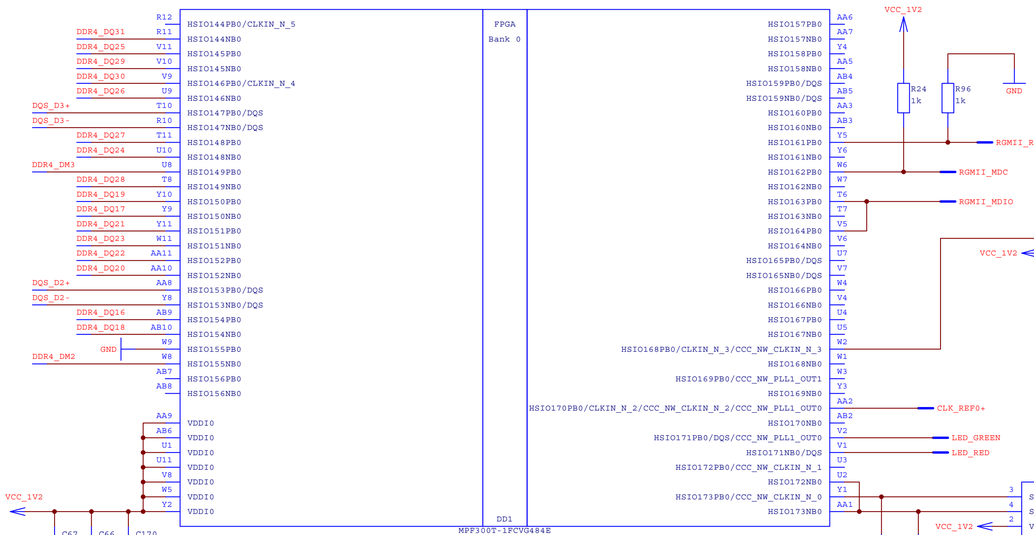
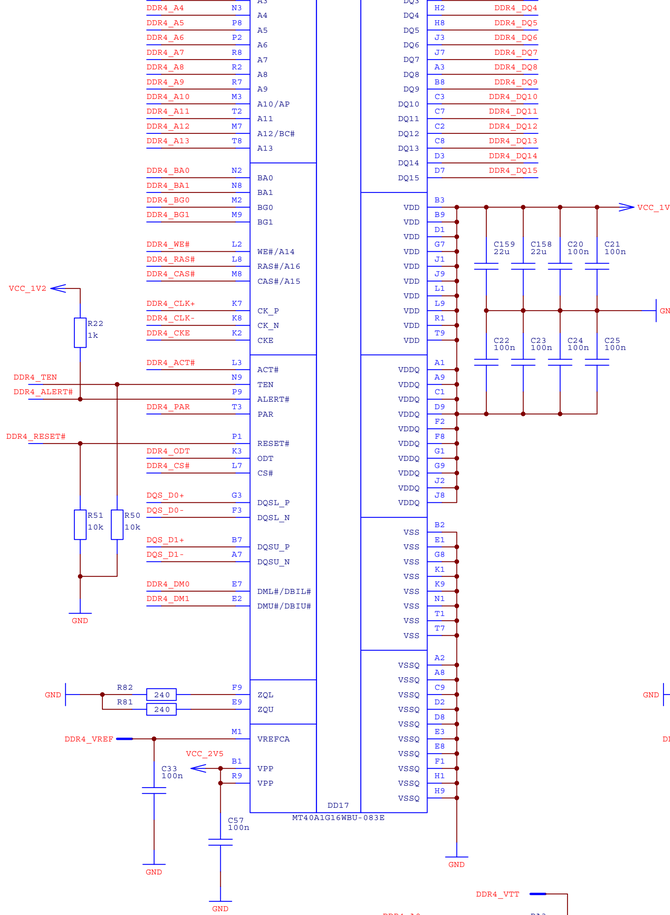
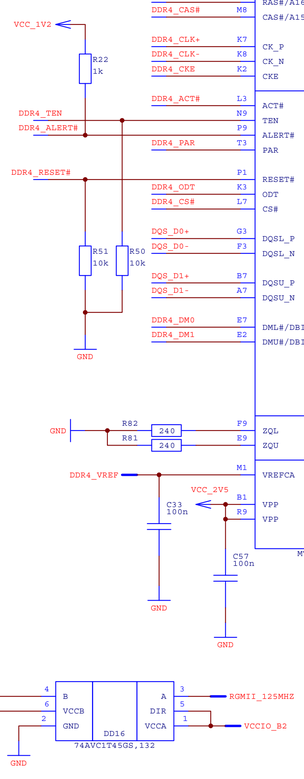
DDR4 SDRAM

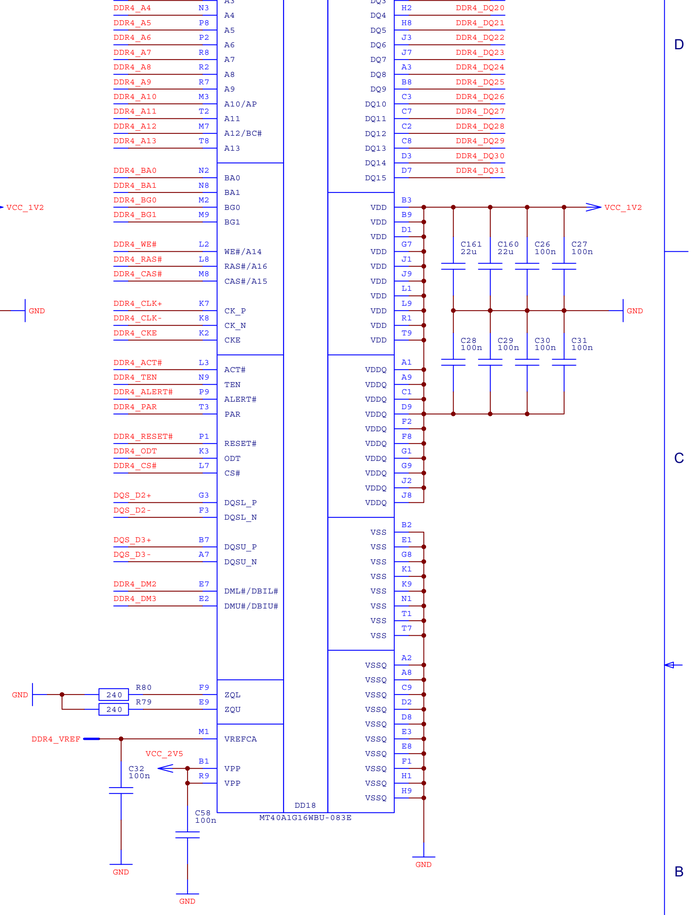
DO NOT SWAP DDR4

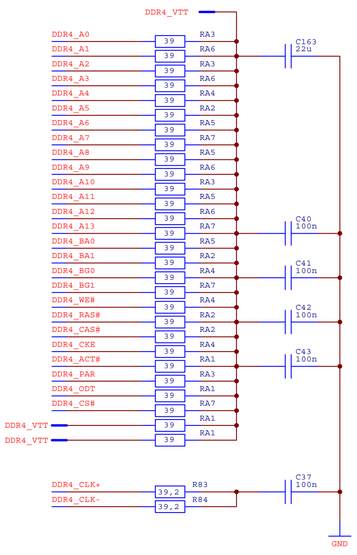


DO NOT SWAP DDR4









SEE NOTE on TITLE PAGE

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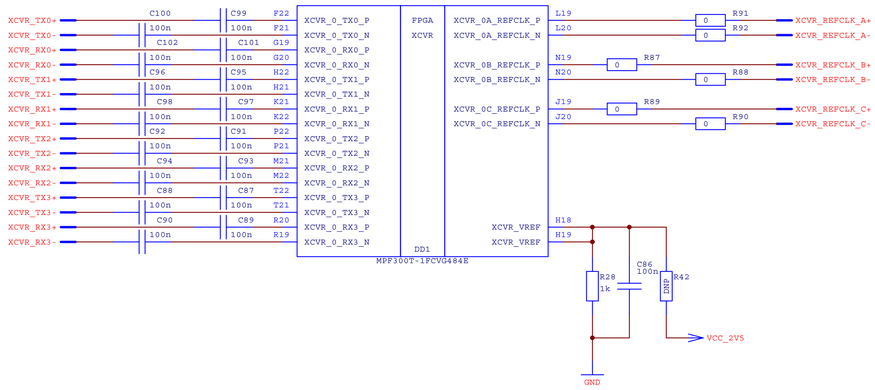
BANK 4, Transceivers



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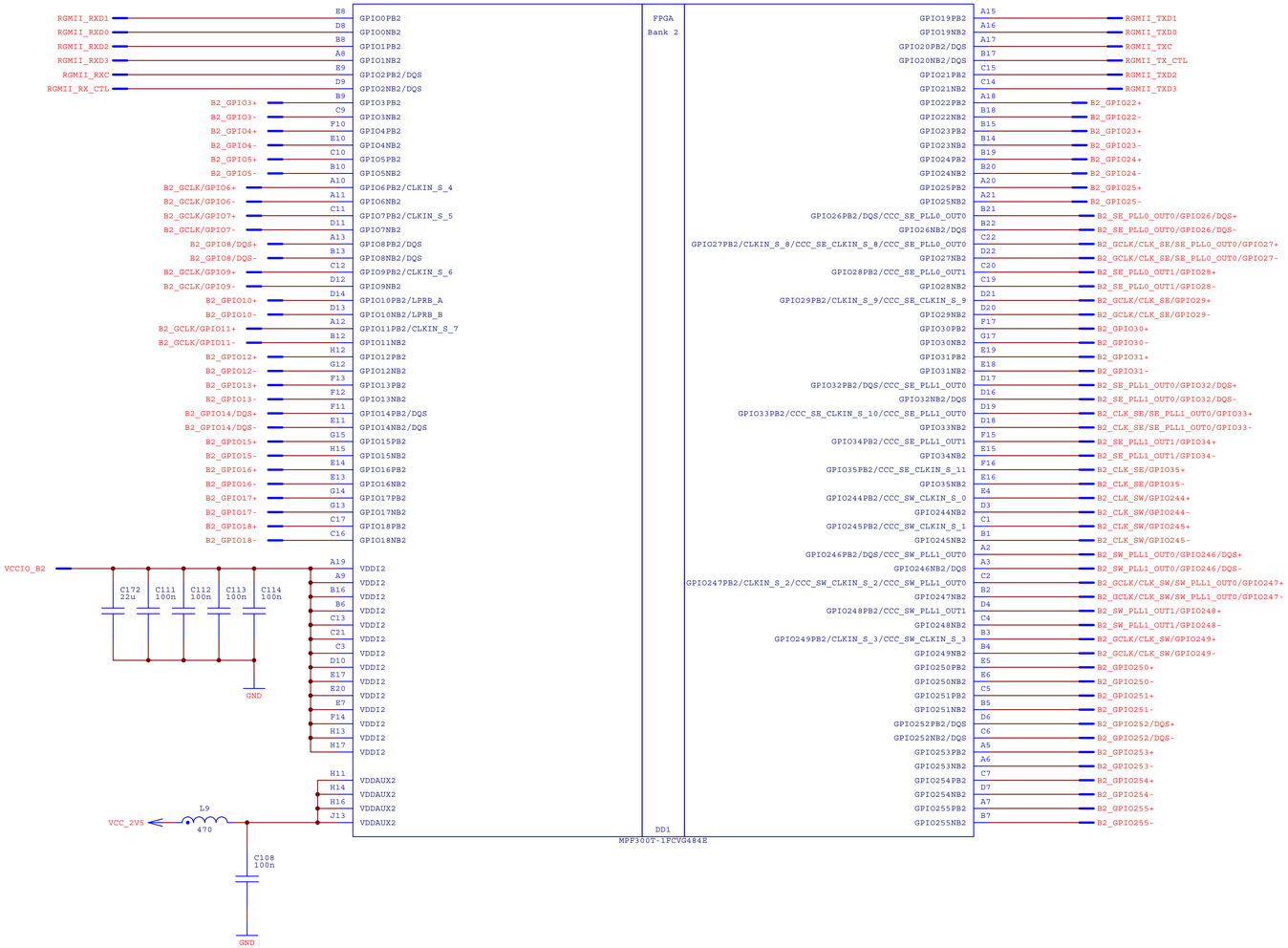
BANK 2



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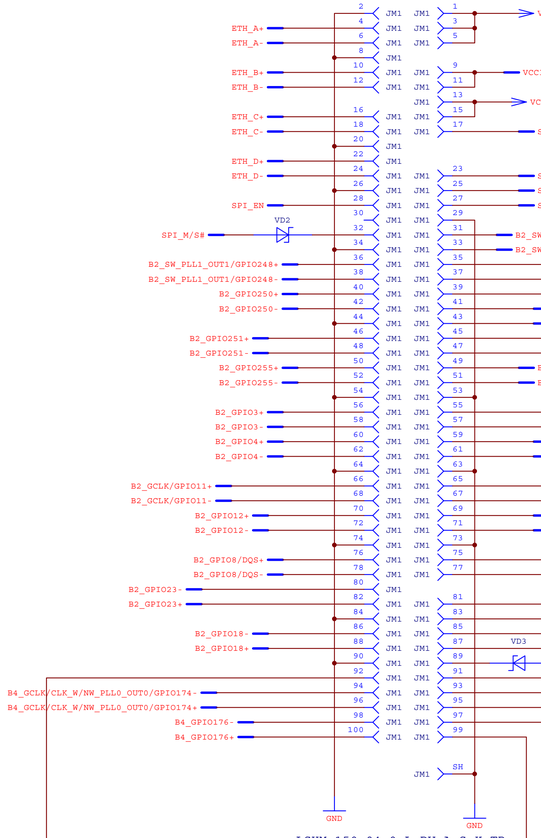
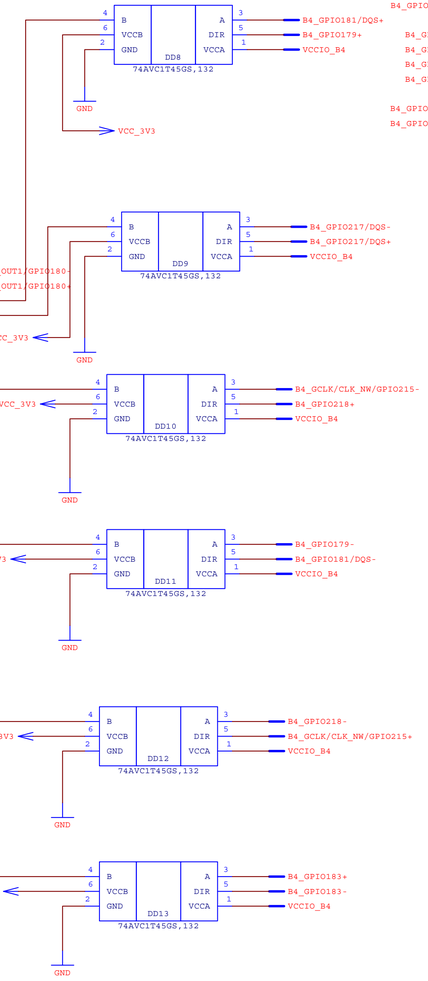
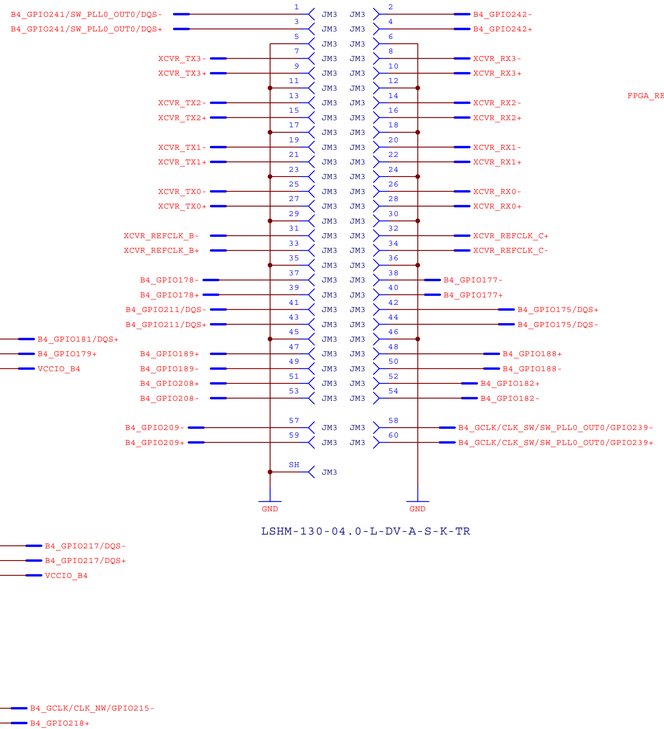
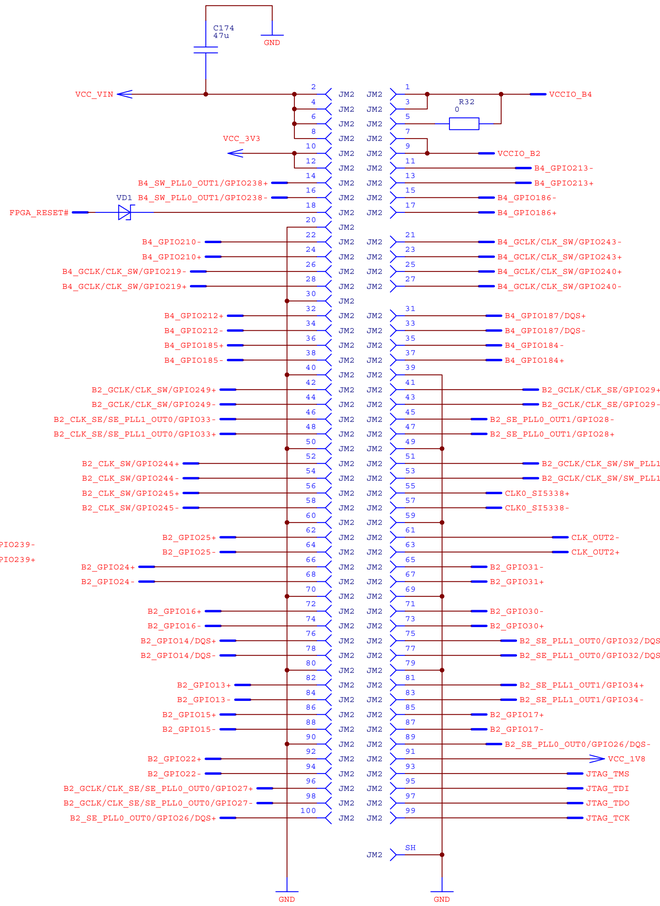
Connectors









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