Analog Circuit Design

UE21EC251A

Project Report

Schmitt Trigger Comparator

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Sem 3, F Sec

Aim:

To design and simulate Schmitt Trigger circuit (Comparator) using LTSpice

Components used:

- 3 CMOS-n transistors
- 3 PMOS-n transistors
- Independent voltage source (sinusoidal of 500kHz)
- Threshold DC voltage source Vdd

Theory:

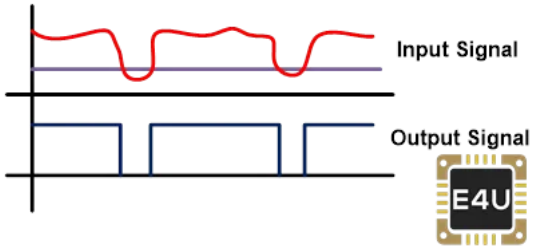
A **Comparator** is a device that compares two voltages or currents. The output is the signal which is the larger of the two. Assuming inputs positive voltage V_+ and negative voltage V_-, the output is usually

$$V_o = \begin{cases} 1, & \text{if } V_+ > V_-, \\ 0, & \text{if } V_+ < V_-. \end{cases}$$

A **Schmitt Trigger** is a comparator circuit with hysteresis implemented by applying positive feedback to the non-inverting input of a comparator or differential amplifier

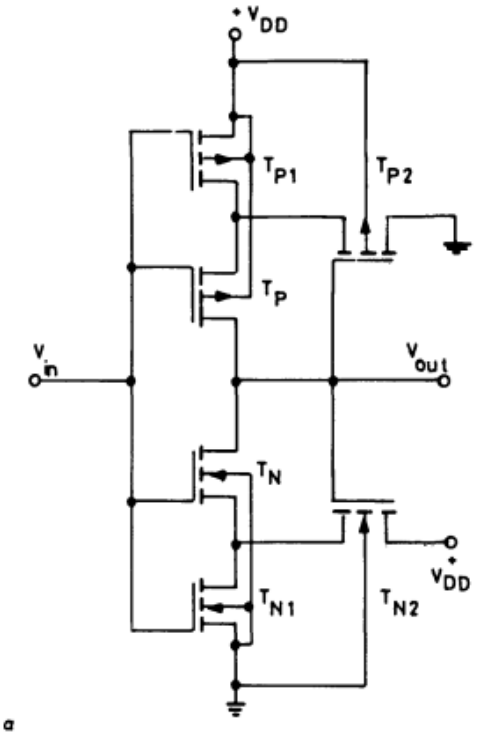
Why Schmitt trigger?

The normal comparator contains only one threshold signal. And it compares the threshold signal with an input signal. But, if the input signal has noise, it may affect the output signal.

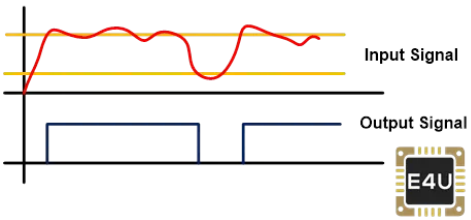


Hence the usual comparators are not protected from noise.

The Schmitt trigger gives proper results even if the input signal is noisy. The “trigger” in the name “Schmitt Trigger” comes from the fact that the output retains its value until the input varies sufficiently to “trigger” a change.



It uses two threshold voltages; one is the upper threshold voltage (VUT) and the second is lower threshold voltage (VLT).



Assuming initial input is 0, V_{out}=0. The feedback loop biases the PMOS transistors M1 and M2 in the conductive mode while M3 is off. The input signal effectively connects to an inverter consisting of two PMOS transistors in parallel (M2 and M1) as a pull-up network, and a single NMOS transistor (M6) in the pull-down chain. This modifies the transistor ratio which moves the switching threshold up.

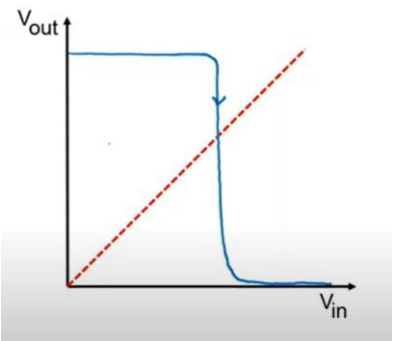
How does switching threshold move up?

The HIGH Vout activates M6 acting as feedback, and the value is transferred to Vx which changes the kn/kp ratio.

$$\frac{k_n}{k_p} = \frac{W_n/L_n}{W_p/L_p}$$

This speeds up the transition and produces a clean output signal with steep slopes. The stronger PMOS transistor network shifts the characteristics towards right.

Ratio = $k_{M6}/(k_{M1}+k_{M2})$

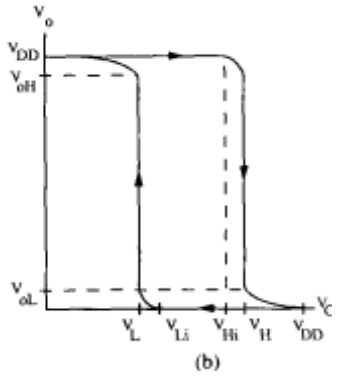


Similar behavior can be observed for the high-to-low transition. In this case, the pull-down network initially consists of M4 and M5 in parallel, while the pull-up network is formed by M3. This reduces the value of the switching threshold to VM-.

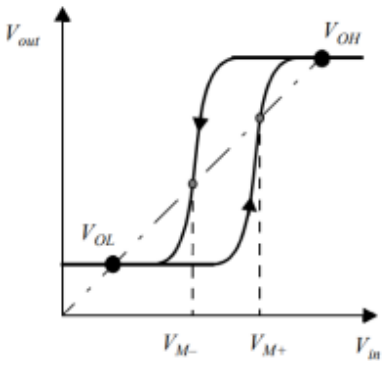
The switching down:

The Gnd value is transferred through M3 to Vy and makes for a stronger pull-down network. The transfer characteristics now shifts towards left.

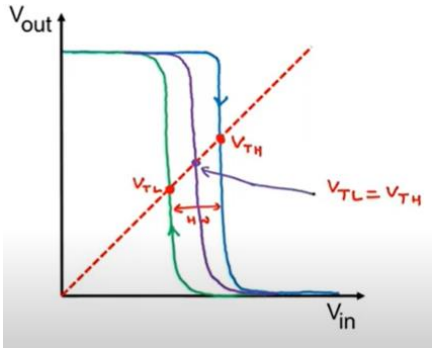
Ratio= $(k_{M4}+k_{M5})/k_{M3}$



Vm+ and Vm- are the upper threshold and lower voltages respectively. (VUT and VLT). Hysteresis width = V_{M+} - V_{M-}.



On attempting to bring $V_{M+}=V_{M-}$, we should get the characteristics as:



Use of positive feedback mechanism:

- If the threshold voltages VUT and VLT are more than input noise voltage Vin, it
- eliminates the false output transition.
- Adding noise immunity by introducing the hysteresis effect. Noise excursions smaller than hysteresis width will not cause an undesired reversal in output state.

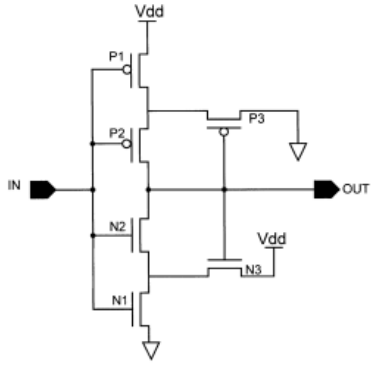
Hysteresis characteristics:

- When the input is below a different (lower) chosen threshold, the output is low,
- when the input is between the two levels the output retains its value.
- Brings about a delayed action

This dual threshold action is called hysteresis and implies that the Schmitt trigger possesses memory and can act as a bistable multivibrator (latch or flip-flop).

V_{M+} and V_{M-}:

Consider Vout=Vdd, Vin=0 -> Vdd
Nearby VM+, M1 and M3 are in saturation region. Using reference:



Consider $V_{out} = V_{dd}$, $V_{in} = 0 \rightarrow V_{dd}$.

At the nearby point of V_{TH}, Transistors **M1** and **M3** are in saturation regions

$$\frac{k_1}{2}(V_{in} - V_{Th,n})^2 = \frac{k_3}{2}(V_{dd} - V_x - V_{Th,n})^2$$

The node voltage $V_x \downarrow$ if $V_{in} \uparrow$

As $V_x = V_{in} - V_{Th,n}$, transistor **M2 = ON**, $V_{out} \rightarrow 0$.
Substituting V_{in} with V_{TH} and solve for V_{TH}

$$V_{TH} = \frac{V_{dd} + V_{Th,n} \times \sqrt{\frac{k_1}{k_3}}}{1 + \sqrt{\frac{k_1}{k_3}}}$$

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Consider $V_{out} = 0$, $V_{in} = V_{dd} \rightarrow 0$.

At the nearby point of V_{TL}, Transistors **M4** and **M6** are in saturation regions

$$\frac{k_4}{2}(V_{dd} - V_{in} - |V_{Th,p}|)^2 = \frac{k_6}{2}(V_y - |V_{Th,p}|)^2$$

The node voltage $V_y \uparrow$ if $V_{in} \downarrow$

As $V_y = V_{in} + |V_{Th,p}|$, transistor **M5 = ON**, $V_{out} \rightarrow V_{dd}$.
Substituting V_{in} with V_{TL} and solve for V_{TL}

$$V_{TL} = \frac{\sqrt{\frac{k_4}{k_6}}(V_{dd} - |V_{Th,p}|)}{1 + \sqrt{\frac{k_4}{k_6}}}$$

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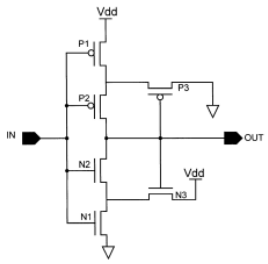
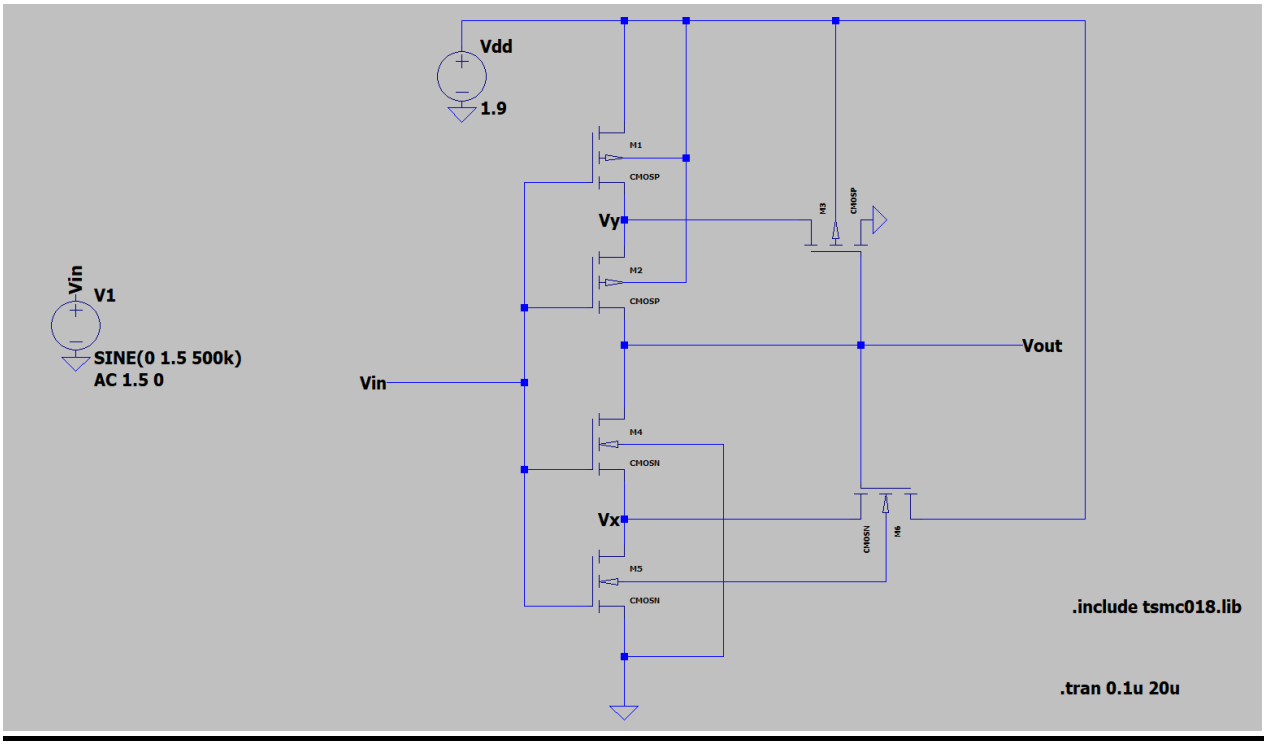
Design:

A conventional Schmitt trigger circuit is basically composed of two sub-sections, section1 and section 2, where section 1 represents the PMOS circuitry consisting of three CMOS-p transistors. This is the ‘pull-up’ P-subcircuit responsible for generation of the lower threshold switching voltage VL. The bottom three CMOS-n transistors make up the ‘pull-down’ N-subcircuit responsible for generation of the upper threshold switching voltage VH.

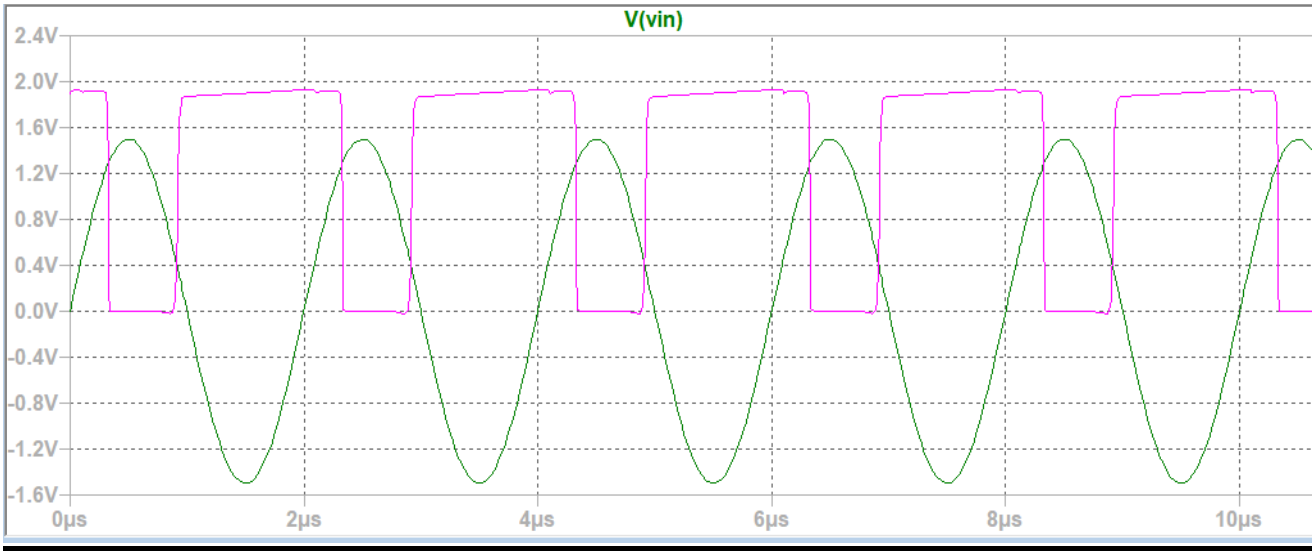


When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal to VDD). During this condition, both P1 and P2 are on (because Vgs < |Vtp| source voltage and gate voltage is equal). Therefore, the output voltage is pull to VDD. When the input increases to Vdd, N1 and N2 is turned on. Thus the output voltage is pull down to GND.

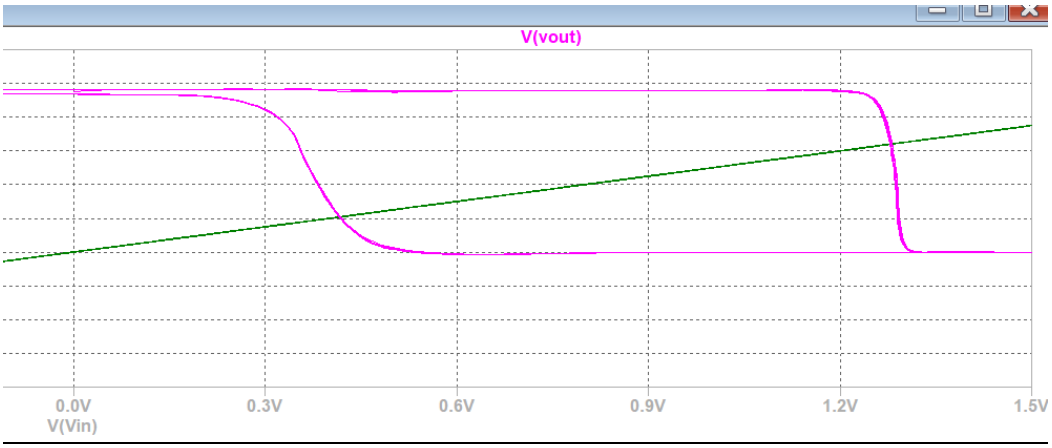


Actual Waveform:

Transient Analysis: Vin=1.5V, 500kHz, Vdd=1.9V



Hysteresis waveform:



Vm+=1.293V, Vm-=0.42 V; Hysteresis width =0.455 V

Conclusion:

The output waveform swings between 0 and Vdd value as a square waveform, thus responding to the slow changing sinusoidal waveform into a fast transitional square waveform.

Applications: implementing relaxation oscillators, removing noise from digital circuits, in switching power supplies as well as function generators.

References:

- Digital Integrated Circuits, A Design Perspective, by Jan M. Rabaey
- https://en.wikipedia.org/wiki/Schmitt_trigger
- https://components101.com/articles/schmitt-trigger-introduction-working-applications
- https://www.electrical4u.com/schmitt-trigger/