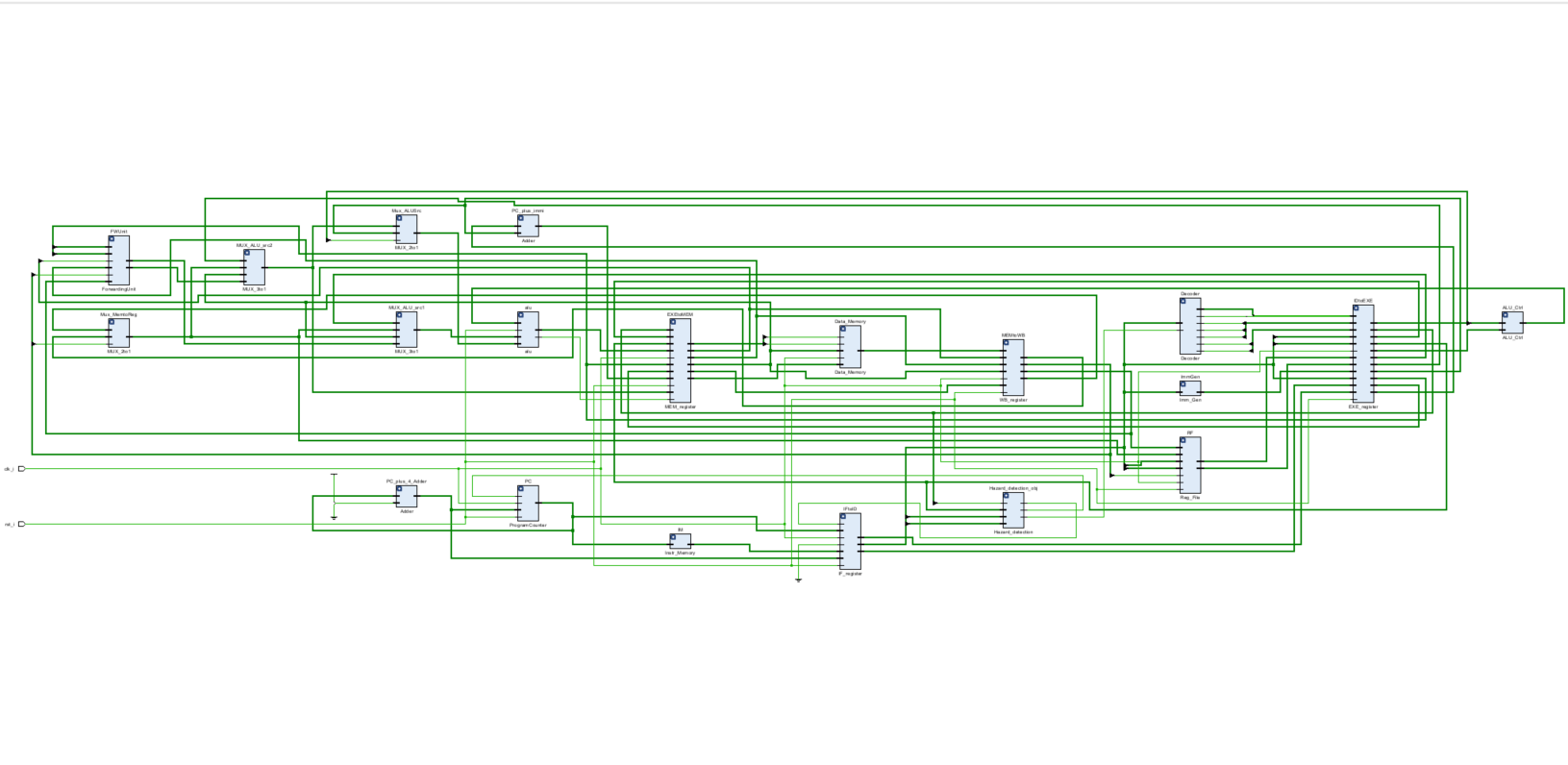
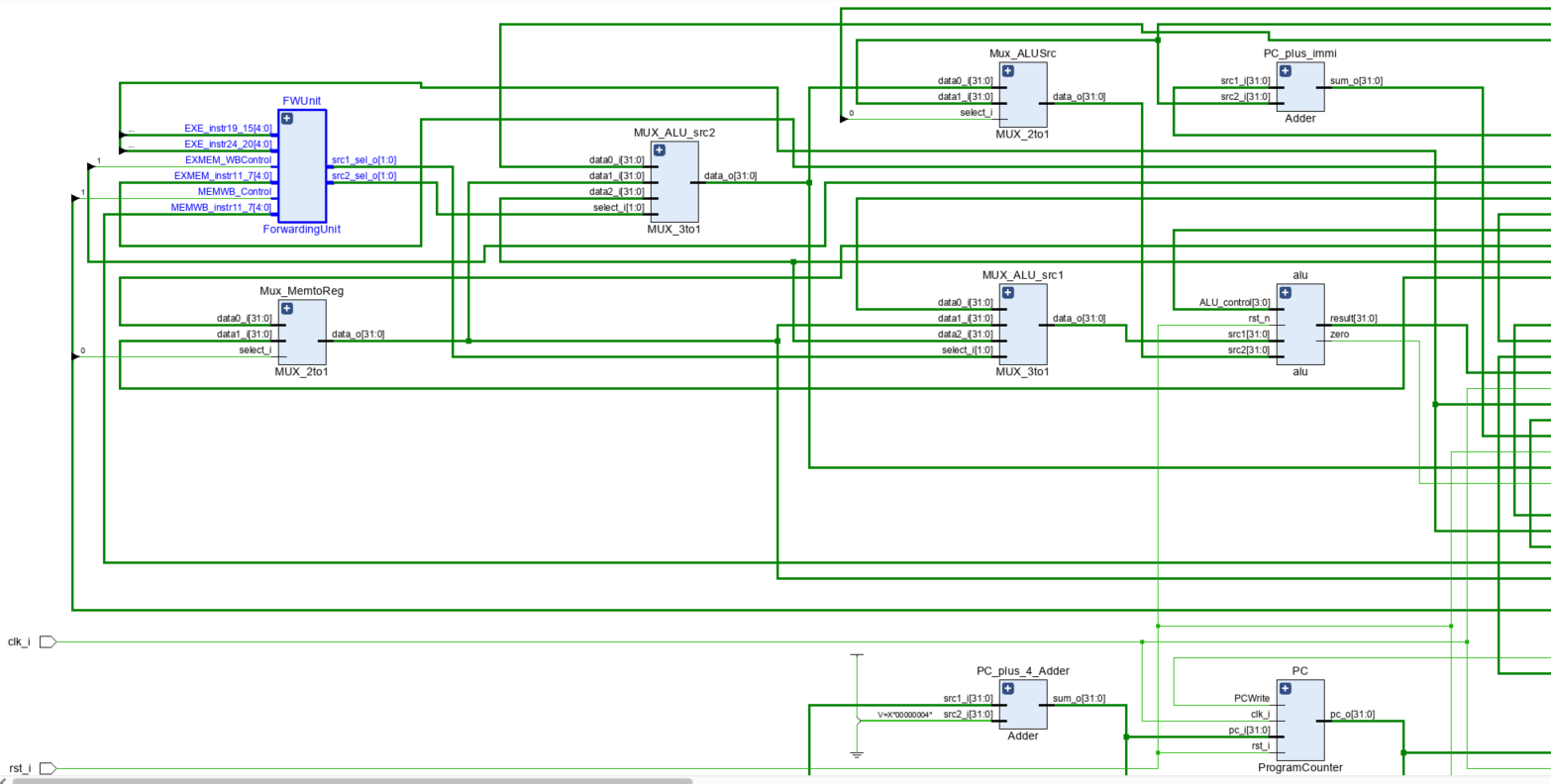
**Computer Organization**

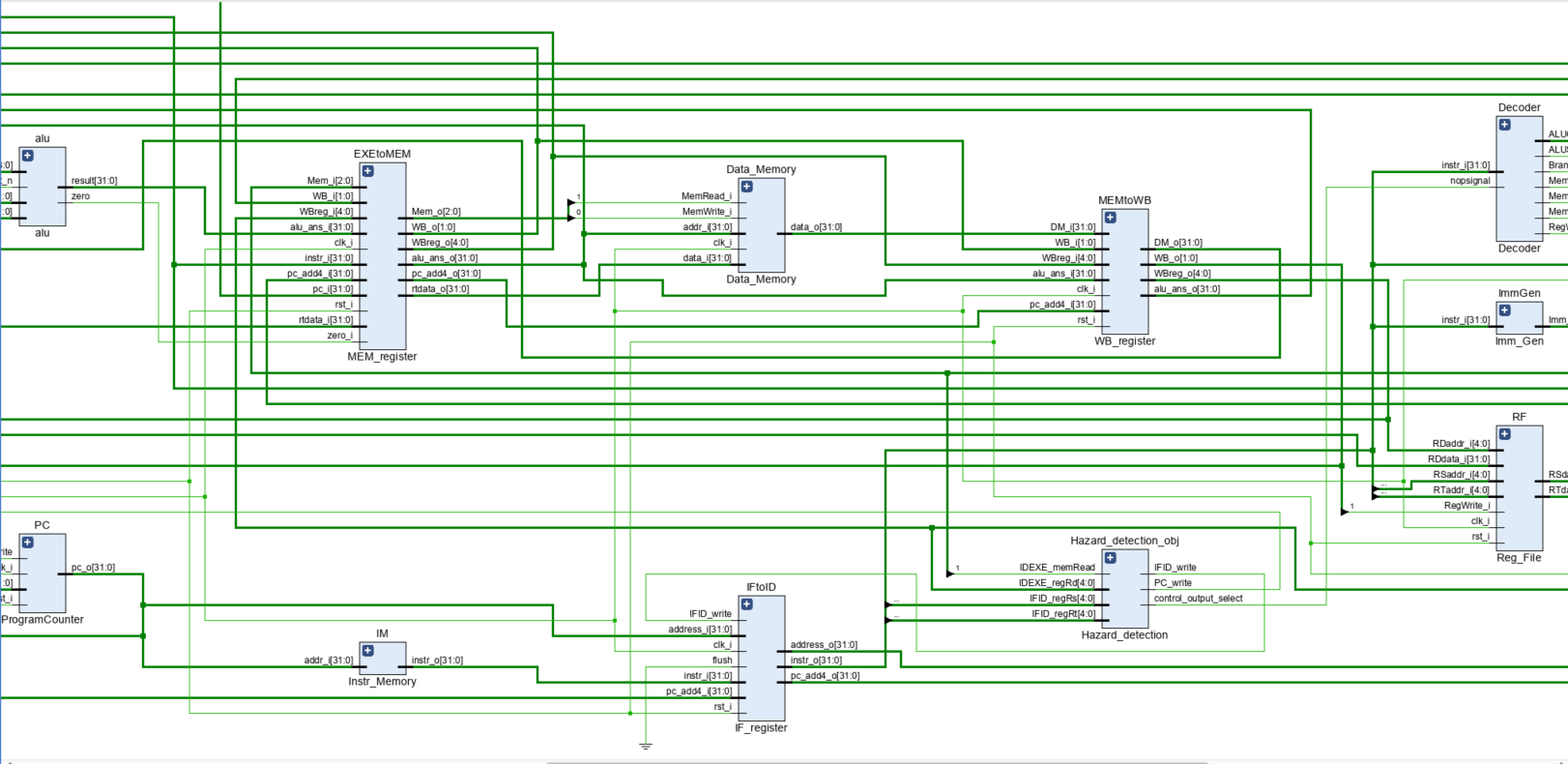
**Architecture diagram:**

****

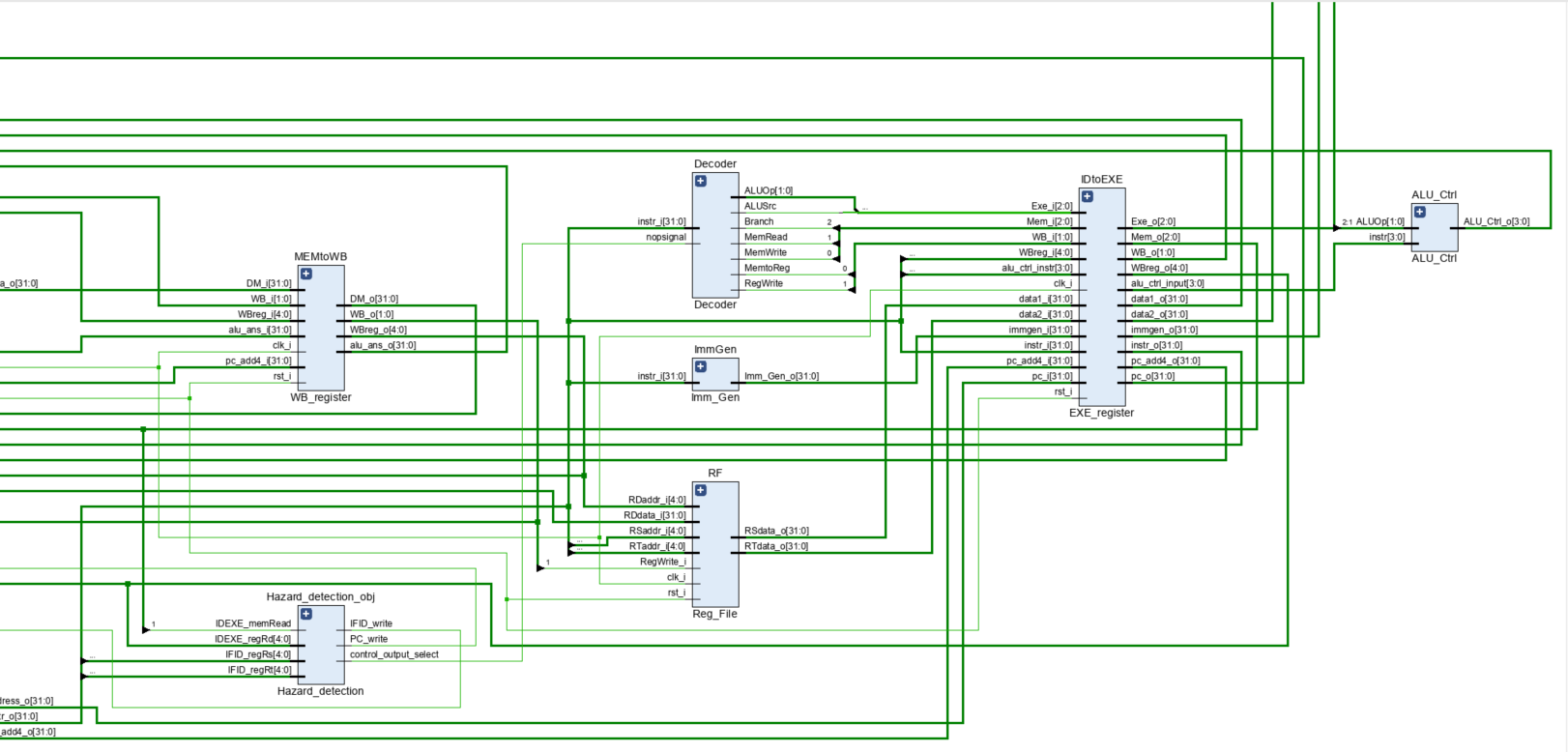
**左半**

****

**中間:**

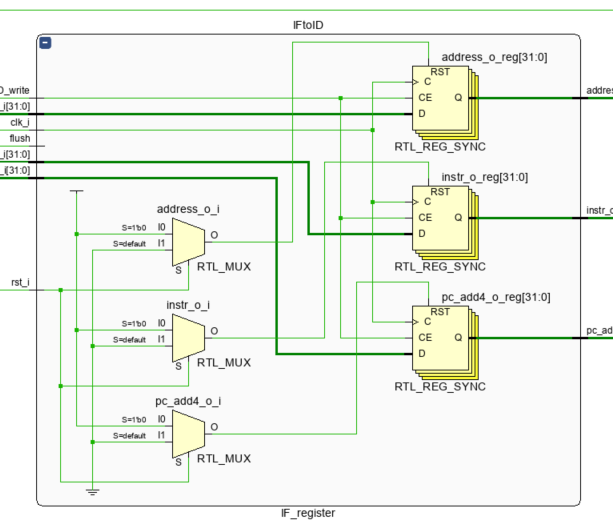
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**右半**

****

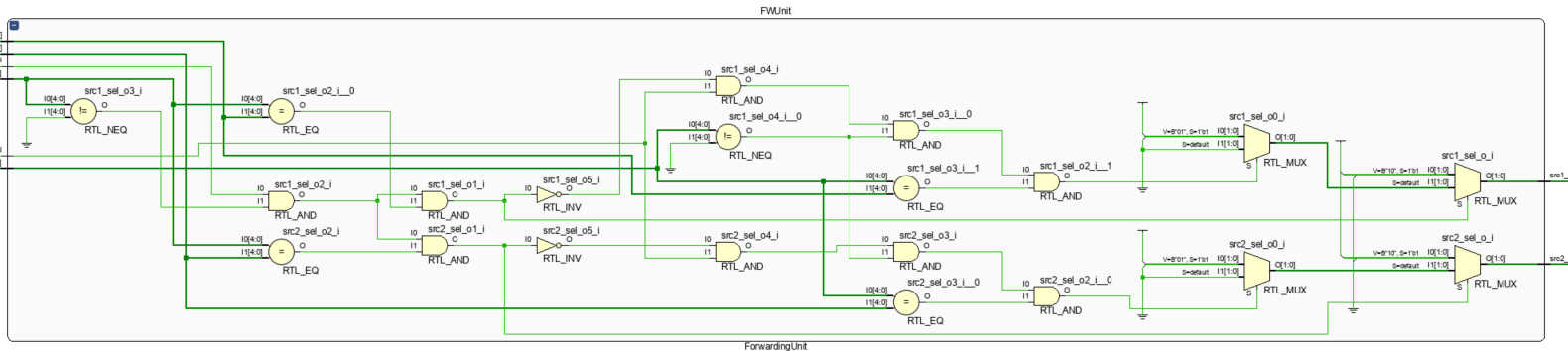
**Detailed description of the implementation:**

**Pipeline register:**

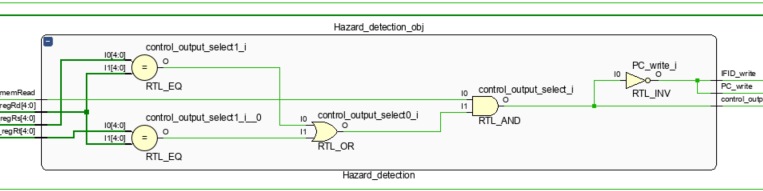
****

**其他三個類似。**

**Forwarding Unit:**

****

**Hazard detecting unit:**

****

**其他基本是同之前的lab ><**

**Implementation results:**

**得到如上的結果 & datapath**

**Problems encountered and solutions:**

**有些aluop和想的不同，debug 很久才找到問題。另外在接線時由於線路太多，導致頭腦當機接線接到很混亂，後來在我們和和花時間，一點一點的除完了錯。**

**Lesson learnt (if any):**

**No**

**Comment:**

**這次作業是目前做起來最完整，也是最累的XD**