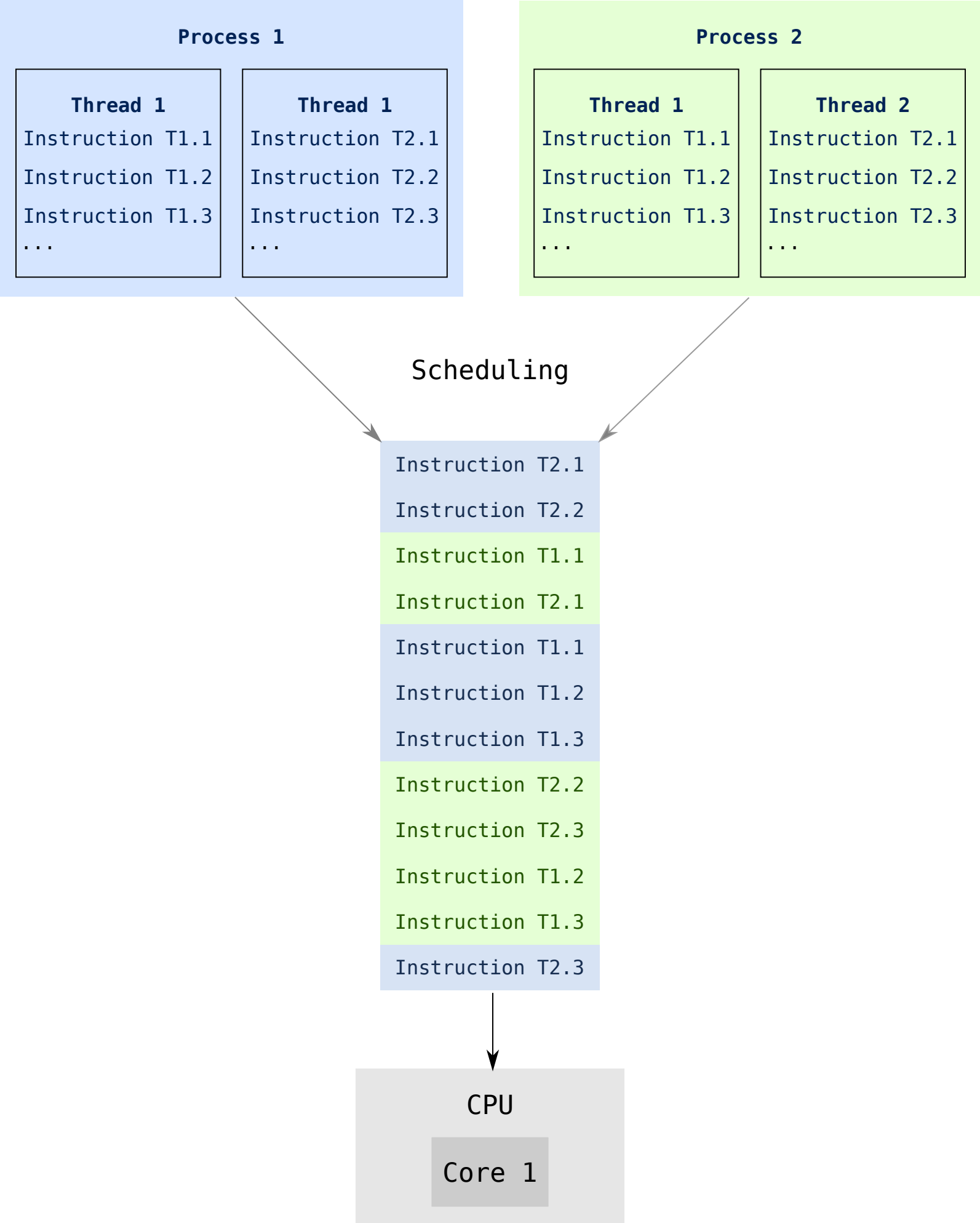
Process 1
Thread 1
Instruction T1.1
Instruction T1.2
Instruction T1.3
...
Thread 1
Instruction T2.1
Instruction T2.2
Instruction T2.3
...
Process 2
Thread 1
Instruction T1.1
Instruction T1.2
Instruction T1.3
...
Thread 2
Instruction T2.1
Instruction T2.2
Instruction T2.3
...
Scheduling
Instruction T2.1
Instruction T2.2
Instruction T1.1
Instruction T2.1
Instruction T1.1
Instruction T1.2
Instruction T1.3
Instruction T2.2
Instruction T2.3
Instruction T1.2
Instruction T1.3
Instruction T2.3
CPU
Core 1