SENAI

Processadores Embarcados

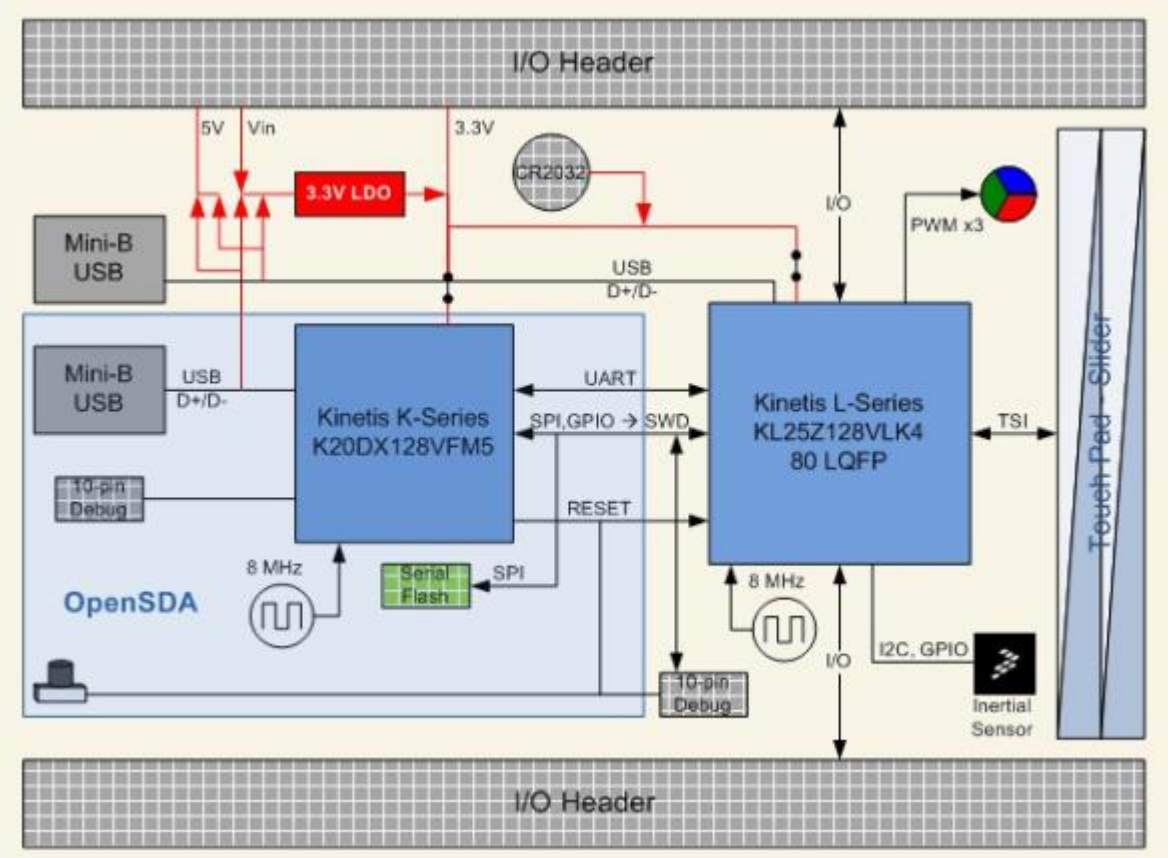
GPIO MCU

ARM Cortex M0+

Profº Fernando Simplicio

Processadores Embarcados

- **FRDM-KL25Z**



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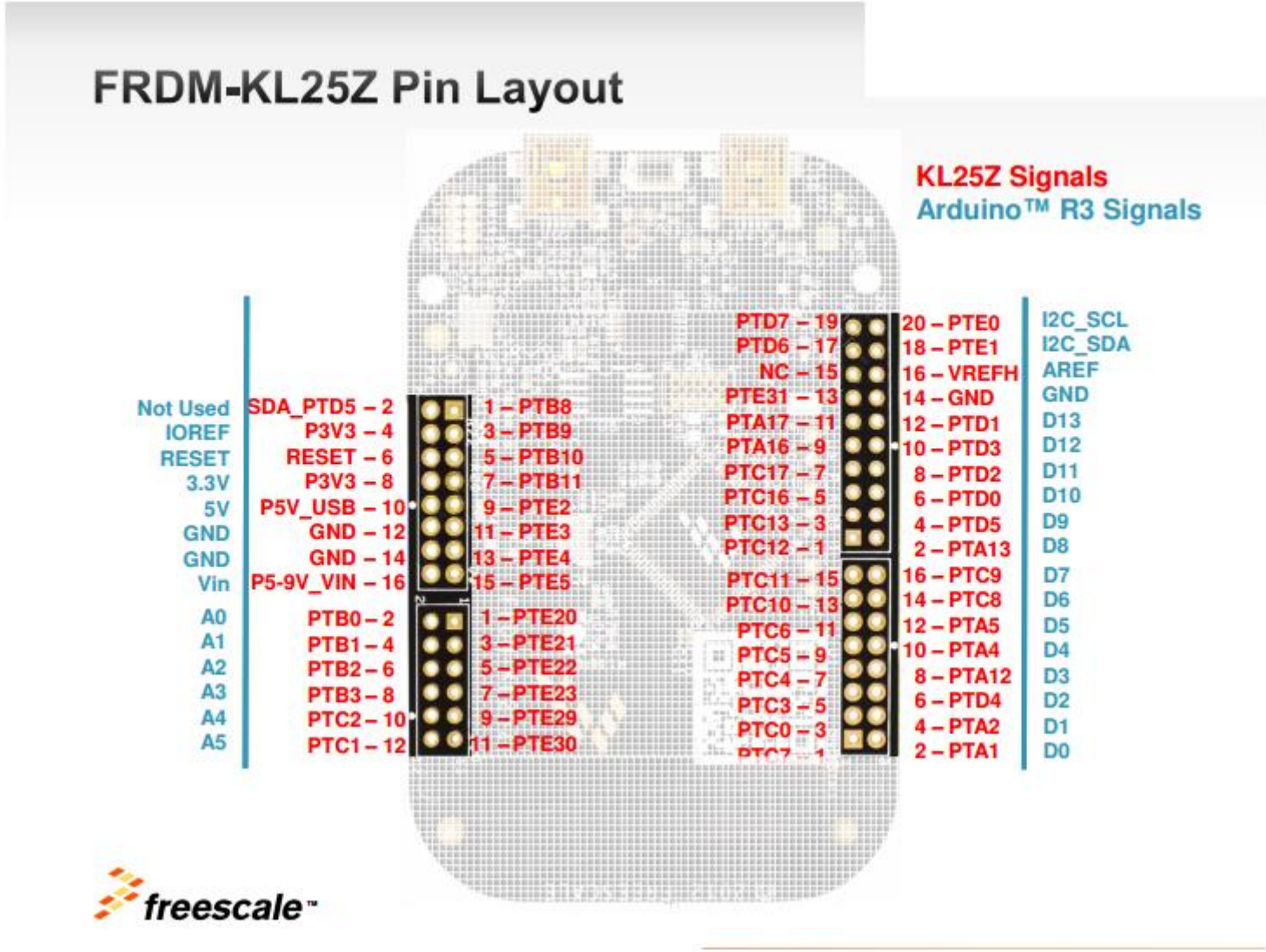

Processadores Embarcados

GPIOs (General-Purpose Input/Output)

- Representam os periféricos para leitura e escrita de dados para interfaceamento com dispositivos.
- Nos MCUs Kinetis cada porta possui 32 pinos [31:0].
- Cada porta é conectada ao MCU através de um barramento, possibilitando a comunicação do MCU com módulos de menor desempenho.

Chip signal name	Module signal name	Description	I/O
PTA[31:0][1]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0][1]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[31:0][1]	PORTC31–PORTC0	General-purpose input/output	I/O
PTD[31:0][1]	PORTD31–PORTD0	General-purpose input/output	I/O
PTE[31:0][1]	PORTE31–PORTE0	General-purpose input/output	I/O

Registradores do periférico GPIO.

- **Cada porta possui um conjunto de registradores para controle dos pinos.**

1. **Port Data Direction Register (GPIOx_PDDR) – configura entrada ou saída**
2. **Port Data Output Register (GPIOx_PDOR) – configura o nível lógico do pino**
3. **Port Set Output Register (GPIOx_PSOR) – nível lógico 1 para setar o pino**
4. **Port Clear Output Register(GPIOx_PCOR) – nível lógico 1 para zerar o pino**
5. **Port Toggle Output Register (GPIOx_PTOR) – nível lógico 1 para inverter o**
6. **nível lógico presente no pino**
7. **Port Data Input Register (GPIOx_PDIR) – registro para leitura da porta**

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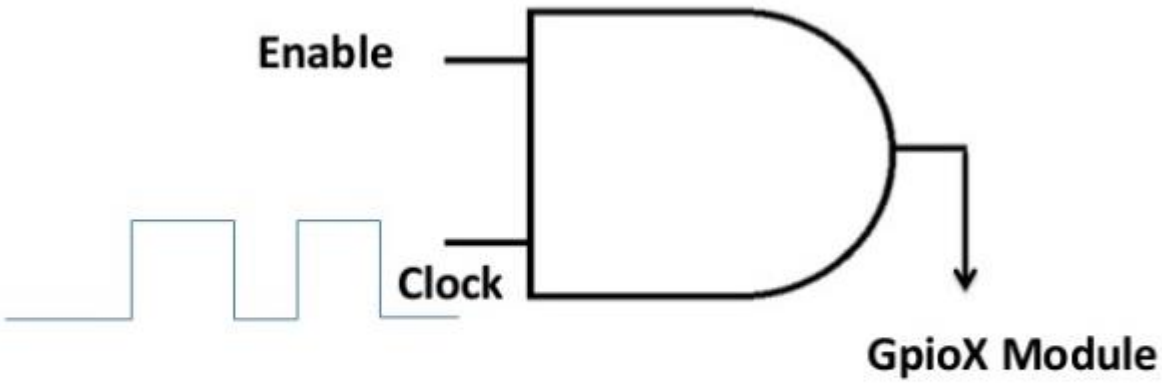
Mapa de memória da PORTA.

- **Cada porta possui um conjunto de registradores para controle dos pinos.**

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
400F_F000	Port Data Output Register (GPIOA_PDOR)	32	R/W	0_0000 _0000h	55.2.1/1745
400F_F004	Port Set Output Register (GPIOA_PSOR)	32	W (always reads 0)	0_0000 _0000h	55.2.2/1746
400F_F008	Port Clear Output Register (GPIOA_PCOR)	32	W (always reads 0)	0_0000 _0000h	55.2.3/1746
400F_F00C	Port Toggle Output Register (GPIOA_PTOR)	32	W (always reads 0)	0_0000 _0000h	55.2.4/1747
400F_F010	Port Data Input Register (GPIOA_PDIR)	32	R	0_0000 _0000h	55.2.5/1747
400F_F014	Port Data Direction Register (GPIOA_PDDR)	32	R/W	0_0000 _0000h	55.2.6/1748

Registrador do GPIO – ativação do clock.

1-First We Must deliver clock to GpioX Module



Warning : IF you try to read or write in any Register in GpioX Module without deliver Clock ,you will cause **bus fault Exception**

Registrador do GPIO – ativação do clock.

Na configuração padrão os clocks de áreas específicas que não estão em uso são desativados, reduzindo o consumo dinâmico necessário.

Para utilizar um periférico particular ou recurso o usuário precisa ativar esse clock para recurso individualmente:

12.2.9 System Clock Gating Control Register 5 (SIM_SCGC5)

Address: 4004_7000h base + 1038h offset = 4004_8038h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0												0	0		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0		PORTE	PORTD	PORTC	PORTB	PORTA	1		0	TSI	0			0	LPTMR
W																
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

Pin Control Register n (PORTx_PCRn) - MUX

Multiplexação dos recursos: interrupção, DMA, multiplexador dos pinos, capacidade de corrente (Drive Strength Enable), saída com dreno aberto (Open Drain Enable), filtro dos pinos de entrada, velocidade (*Slew Rate Enable*), pull up, pull down, etc..

Address: Base address + 0h offset + (4d × i), where i=0d to 31d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0							ISF	0				IRQC			
W								w1c								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0					MUX			0	DSE	0	PFE	0	SRE	PE	PS
W																
Reset	0	0	0	0	0	x*	x*	x*	0	x*	0	x*	0	x*	x*	x*

* Notes:
- x = Undefined at reset.

Pin Control Register n (PORTx_PCRn)

PORTx_PCR*n* field descriptions (continued)

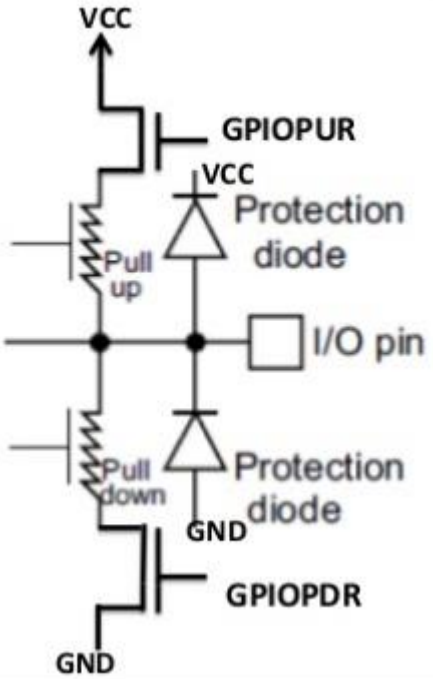
Field	Description
23–20 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
19–16 IRQC	Interrupt Configuration This field is read only for pins that do not support interrupt generation. The pin interrupt configuration is valid in all digital pin muxing modes. The corresponding pin is configured to generate interrupt/DMA request as follows: 0000 Interrupt/DMA request disabled. 0001 DMA request on rising edge. 0010 DMA request on falling edge. 0011 DMA request on either edge. 1000 Interrupt when logic zero. 1001 Interrupt on rising edge. 1010 Interrupt on falling edge. 1011 Interrupt on either edge. 1100 Interrupt when logic one. Others Reserved.

Pin Control Register n (PORTx_PCRn)

10–8 MUX	Pin Mux Control Not all pins support all pin muxing slots. Unimplemented pin muxing slots are reserved and may result in configuring the pin for a different pin muxing slot. The corresponding pin is configured in the following pin muxing slot as follows: 000 Pin disabled (analog). 001 Alternative 1 (GPIO). 010 Alternative 2 (chip-specific). 011 Alternative 3 (chip-specific). 100 Alternative 4 (chip-specific). 101 Alternative 5 (chip-specific). 110 Alternative 6 (chip-specific). 111 Alternative 7 (chip-specific).
7 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
6 DSE	Drive Strength Enable This bit is read only for pins that do not support a configurable drive strength. Drive strength configuration is valid in all digital pin muxing modes. 0 Low drive strength is configured on the corresponding pin, if pin is configured as a digital output. 1 High drive strength is configured on the corresponding pin, if pin is configured as a digital output.

Pin Control Register n (PORTx_PCRn)

2 SRE	Slew Rate Enable This bit is read only for pins that do not support a configurable slew rate. Slew rate configuration is valid in all digital pin muxing modes. 0 Fast slew rate is configured on the corresponding pin, if the pin is configured as a digital output. 1 Slow slew rate is configured on the corresponding pin, if the pin is configured as a digital output.
1 PE	Pull Enable This bit is read only for pins that do not support a configurable pull resistor. Refer to the Chapter of Signal Multiplexing and Signal Descriptions for the pins that support a configurable pull resistor. Pull configuration is valid in all digital pin muxing modes. 0 Internal pullup or pulldown resistor is not enabled on the corresponding pin. 1 Internal pullup or pulldown resistor is enabled on the corresponding pin, if the pin is configured as a digital input.
0 PS	Pull Select This bit is read only for pins that do not support a configurable pull resistor direction. Pull configuration is valid in all digital pin muxing modes. 0 Internal pulldown resistor is enabled on the corresponding pin, if the corresponding Port Pull Enable field is set. 1 Internal pullup resistor is enabled on the corresponding pin, if the corresponding Port Pull Enable field is set.



Registrador de Direção Input/Output (GPIOx_PDDR)

Seta ou reseta um determinado GPIO ou a porta completa.

41.2.6 Port Data Direction Register (GPIOx_PDDR)

The PDDR configures the individual port pins for input or output.

Address: Base address + 14h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PDD																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PDDR field descriptions

Field	Description
31–0 PDD	Port Data Direction Configures individual port pins for input or output. 0 Pin is configured as general-purpose input, for the GPIO function. 1 Pin is configured as general-purpose output, for the GPIO function.

Seta as GPIOs (GPIOx_PSOR)

41.2.2 Port Set Output Register (GPIOx_PSOR)

This register configures whether to set the fields of the PDOR.

Address: Base address + 4h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W	PTSO																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PSOR field descriptions

Field	Description
31–0 PTSO	Port Set Output Writing to this register will update the contents of the corresponding bit in the PDOR as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is set to logic 1.

Reseta as GPIOs (GPIOx_PCOR)

41.2.3 Port Clear Output Register (GPIOx_PCOR)

This register configures whether to clear the fields of PDOR.

Address: Base address + 8h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W	PTCO																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PCOR field descriptions

Field	Description
31–0 PTCO	Port Clear Output Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is cleared to logic 0.

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Info:

Como você percebeu existe dois registradores responsáveis em setar e resetar um GPIO. Portanto não é utilizado o método READ-MODIFY-WRITE como encontrado em muitos outros MCUs.

Inverte o estado lógido das GPIOs (GPIOx_PTOR)

41.2.4 Port Toggle Output Register (GPIOx_PTOR)

Address: Base address + Ch offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																															
W	PTTO																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PTOR field descriptions

Field	Description
31–0 PTTO	Port Toggle Output Writing to this register will update the contents of the corresponding bit in the PDOR as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is set to the inverse of its existing logic state.

Leitura da GPIO (GPIOx_PDIR)

41.2.5 Port Data Input Register (GPIOx_PDIR)

Address: Base address + 10h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	PDI																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_PDIR field descriptions

Field	Description
31–0 PDI	Port Data Input Reads 0 at the unimplemented pins for a particular device. Pins that are not configured for a digital function read 0. If the Port Control and Interrupt module is disabled, then the corresponding bit in PDIR does not update. 0 Pin logic level is logic 0, or is not configured for use by digital function. 1 Pin logic level is logic 1.

Exemplo:

```
//HABILITA O CLOCK NAS PORTAS D, C e A.
SIM_SCGC5 |= SIM_SCGC5_PORTD_MASK | SIM_SCGC5_PORTC_MASK | SIM_SCGC5_PORTA_MASK;

//PINOS COMO DIGITAIS (BARRAMENTO)
PORTC_PCR9 =  PORT_PCR_MUX(1) | PORT_PCR_DSE_MASK | PORT_PCR_PE_MASK | PORT_PCR_PS_MASK; //d7
PORTC_PCR8 =  PORT_PCR_MUX(1) | PORT_PCR_DSE_MASK | PORT_PCR_PE_MASK | PORT_PCR_PS_MASK; //d6
PORTA_PCR5 =  PORT_PCR_MUX(1) | PORT_PCR_DSE_MASK | PORT_PCR_PE_MASK | PORT_PCR_PS_MASK; //d5
PORTA_PCR4 =  PORT_PCR_MUX(1) | PORT_PCR_DSE_MASK | PORT_PCR_PE_MASK | PORT_PCR_PS_MASK; //d4
PORTA_PCR13 = PORT_PCR_MUX(1) | PORT_PCR_DSE_MASK | PORT_PCR_PE_MASK | PORT_PCR_PS_MASK;  //rs
PORTD_PCR5  = PORT_PCR_MUX(1) | PORT_PCR_DSE_MASK | PORT_PCR_PE_MASK | PORT_PCR_PS_MASK;  //en

//PINOS COMO SAIDA
GPIOC_PDDR |= (1<<9)  | (1<<8);
GPIOA_PDDR |= (1<<13) | (1<<5) | (1<<4);  //PT13=RS  PTD5 = EN
GPIOD_PDDR |= (1<<5);

//PINOS RESETADOS
GPIOC_PCOR = (1<<9)  | (1<<8);
GPIOA_PCOR = (1<<13) | (1<<5) | (1<<4);
GPIOD_PCOR = (1<<5);
```

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Exemplo:

```
GPIOA_PDDR &= ~(1 << 19);  // Configuração da chave SW1
GPIOE_PDDR &= ~(1 << 26);  // Configuração da chave SW2
If ((GPIOA_PDIR & (1 << 19) == 0) || (GPIOE_PDIR & (1 << 26) == 0))
{

}
```

Dicas:

Port Data Output Register (GPIOx_PDOR) - If you write ***GPIOB_PDOR |= (1 << 18);*** you will get a high level on the pin PTB18, If you write ***GPIOB_PDOR &= ~(1 << 18);*** you will get a low level on the pin PTB18.

Port Set Output Register (GPIOx_PSOR) - If you write ***GPIOB_PSOR |= (1 << 18);*** you will get a high level on the pin PTB18, If you write ***GPIOB_PSOR &= ~(1 << 18);*** anything will happen.

Port Clear Output Register (GPIOx_PCOR) - If you write ***GPIOB_PCOR |= (1 << 18);*** you will get a low level on the pin PTB18, If you write ***GPIOB_PCOR &= ~(1 << 18);*** anything will happen.

Port Toggle Output Register (GPIOx_PTOR) - If you write ***GPIOB_PTOR |= (1 << 18);*** you will get a opposite level you have on the pin PTB18, If you write ***GPIOB_PTOR &= ~(1 << 18);*** anything will happen.

Processadores Embarcados

Primeiro Programa:

```
#include <MKL25Z4.h>
void delay(int time)
{
  for(int i; i < time; ++i){}
}
int main(void)
{

        SystemInit();
        SIM_SCGC5 |= SIM_SCGC5_PORTB_MASK;
        PORTB_PCR18 = PORT_PCR_MUX(1) |
                      PORT_PCR_DSE_MASK |
                      PORT_PCR_PE_MASK  |
                      PORT_PCR_PS_MASK;
        //Configura como saída.
        GPIOB_PDDR |= (1<<18);

        //Seta o pino;
        GPIOB_PSOR |= (1<<18);

  for (;;) {
        GPIOB_PSOR |= (1<<18);  //liga
        delay(100000);
        GPIOB_PCOR |=  (1<<18);  //desliga
        delay(100000);

  }
}
```