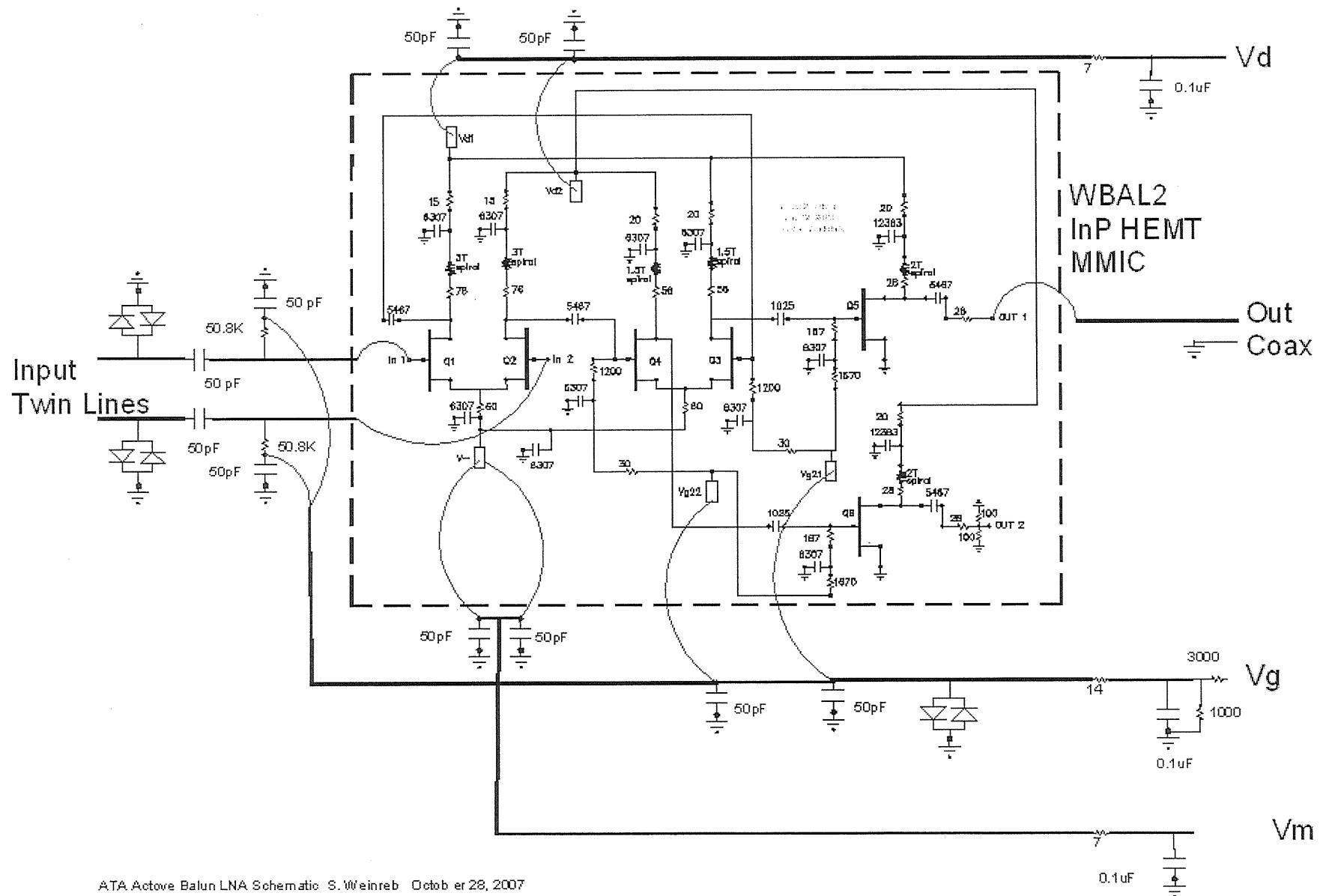


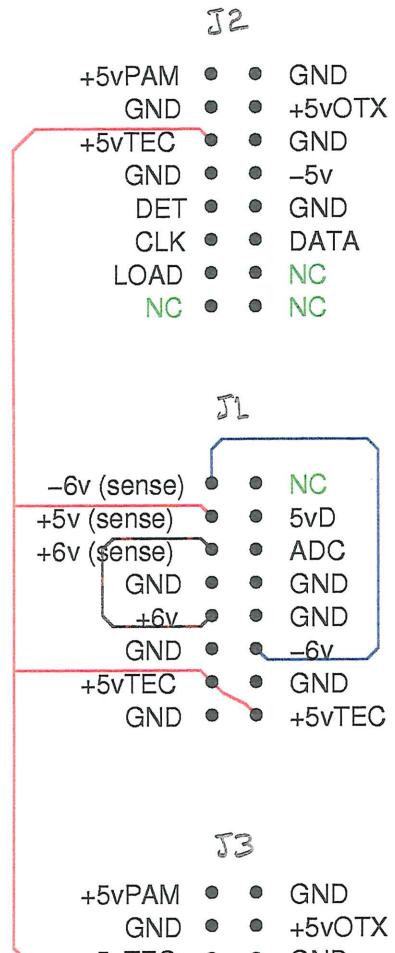
Current ATA LNA 2011



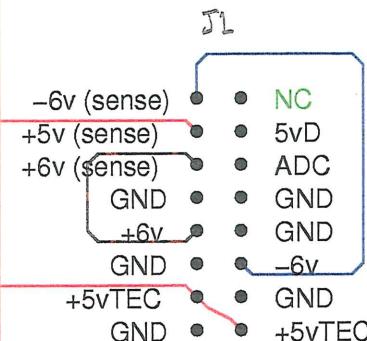
ATA Actove Balun LNA Schematic S. Weinreb October 28, 2007

PAX Controller – Connectors (1)

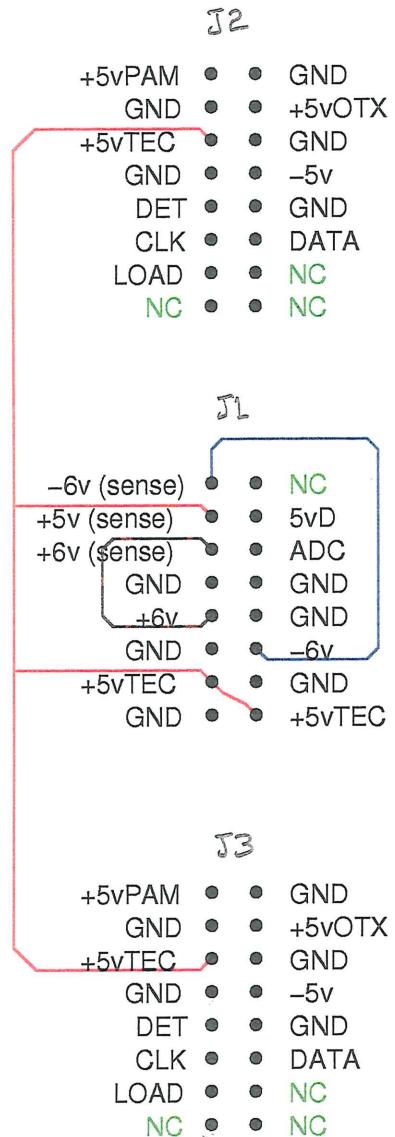
X Pol. PAM



Power (from rim box)



Y Pol. PAM

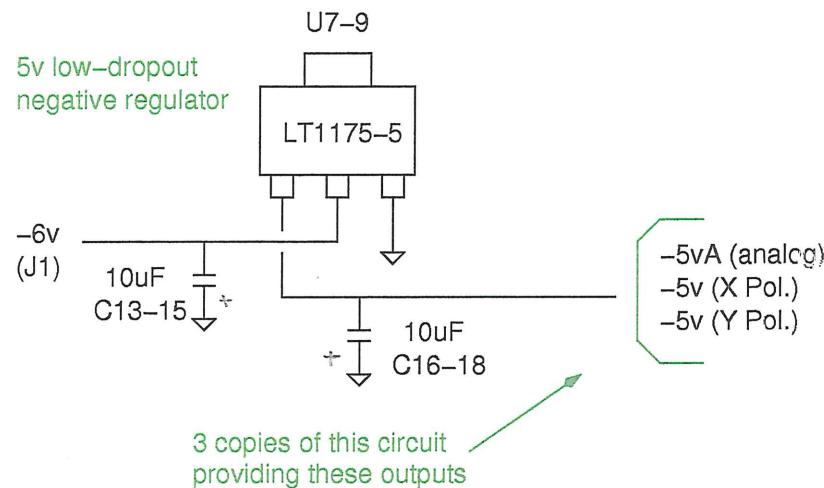
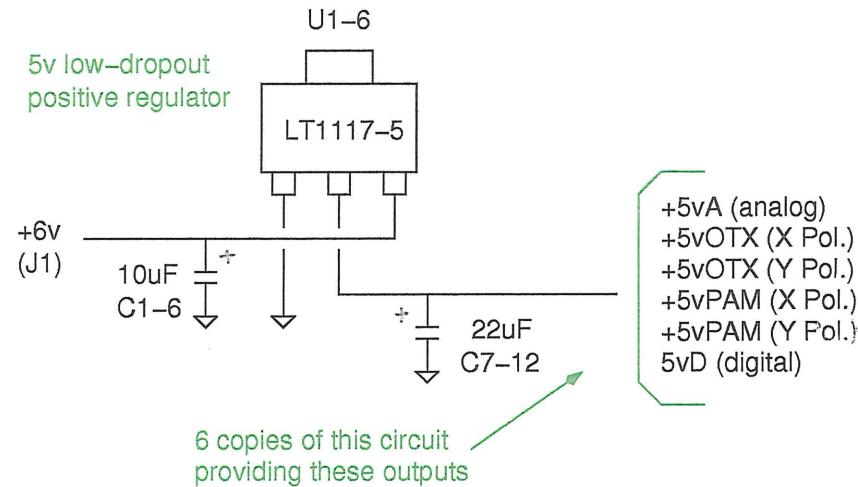


NA bias (to feed)

J4

GND	●	●	VmY
VdY	●	●	GND
GND	●	●	GND
NC	●	●	VgY
NC	●	●	NC
VgX	●	●	NC
GND	●	●	GND
GND	●	●	VmX
VdX	●	●	NC
NC	●	●	NC

PAX Controller – Regulators (2)

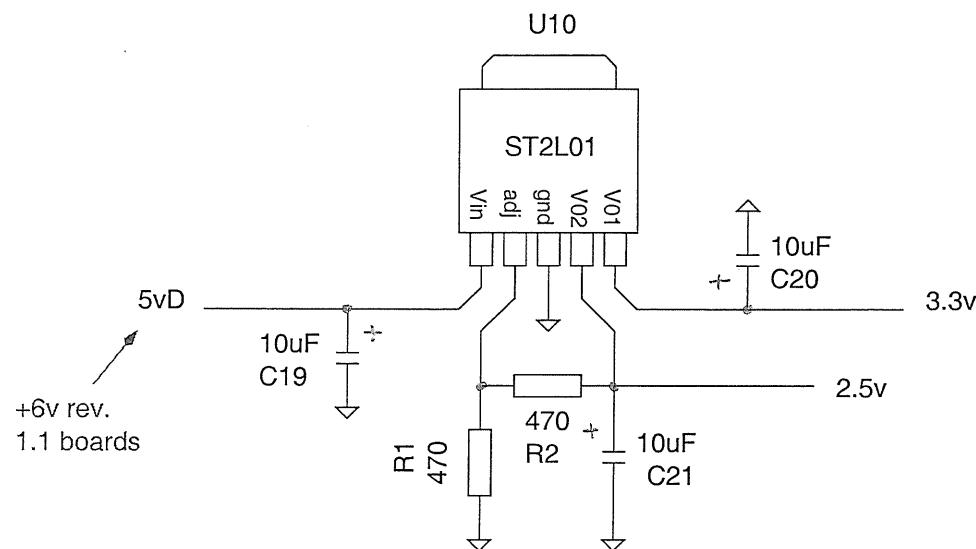


U9
C18

PAX Controller – Microcontroller Regulator (3)

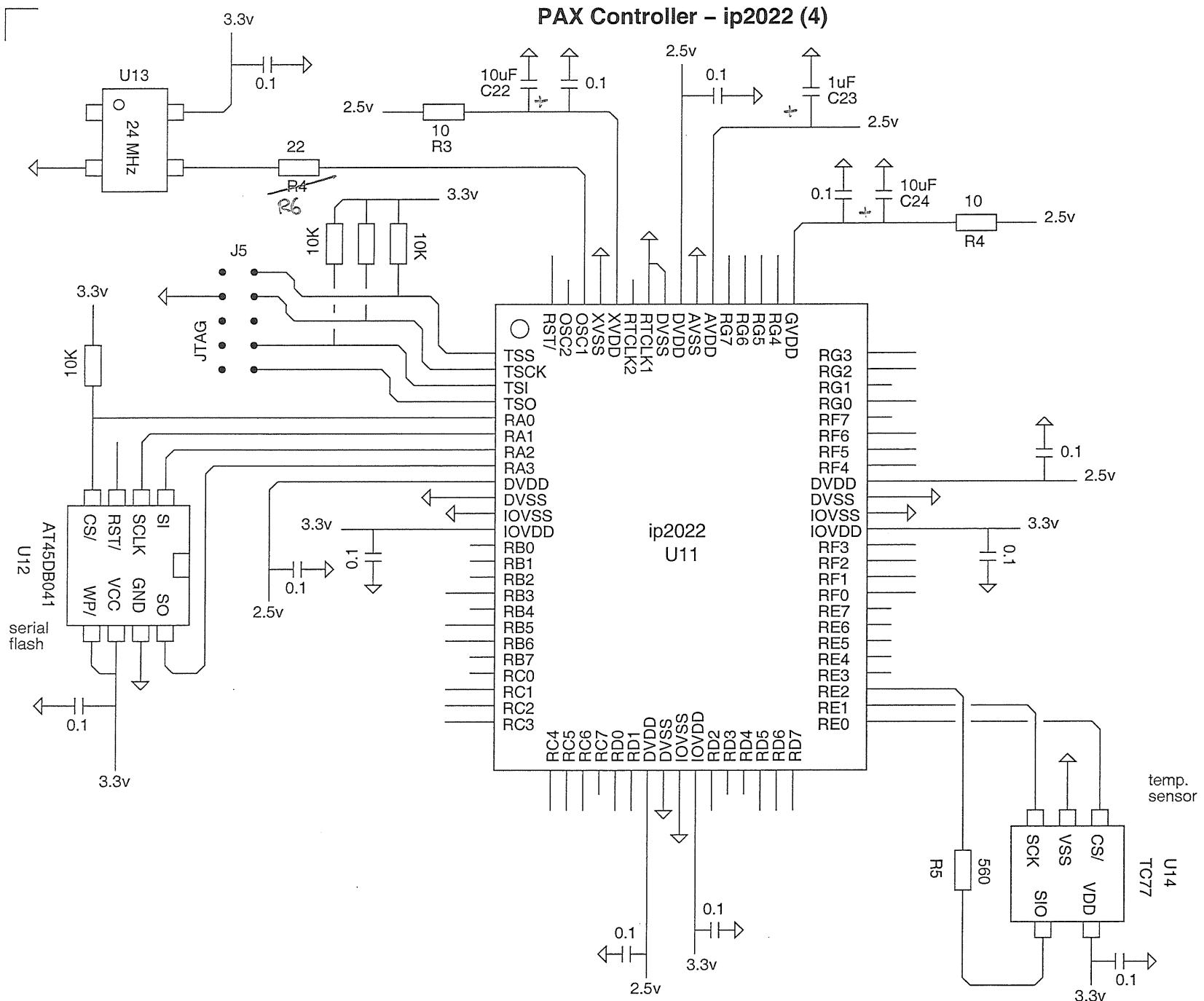
U9
C18

✓

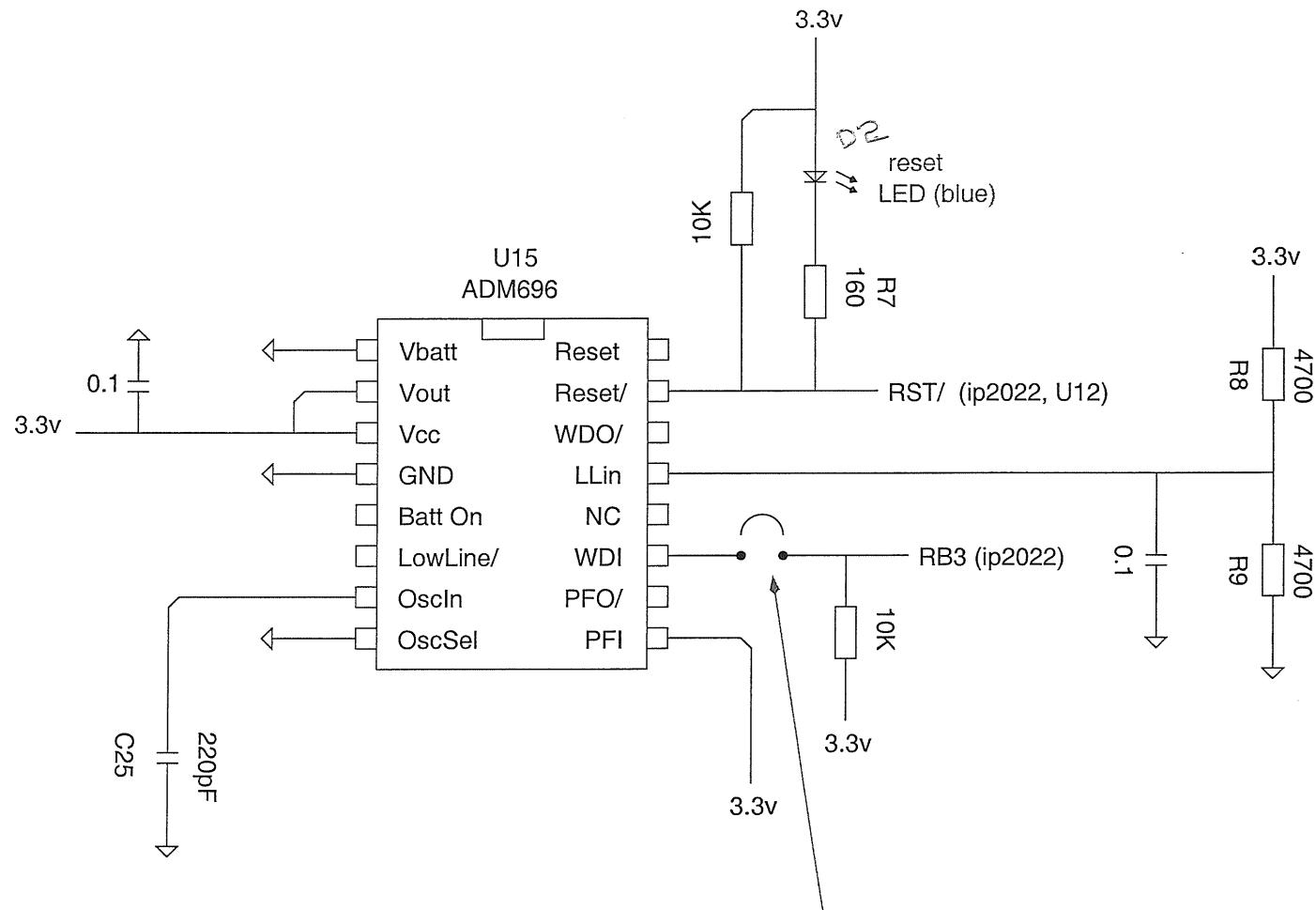


U10
C21
R2

PAX Controller - ip2022 (4)



PAX Controller – Watchdog (5)

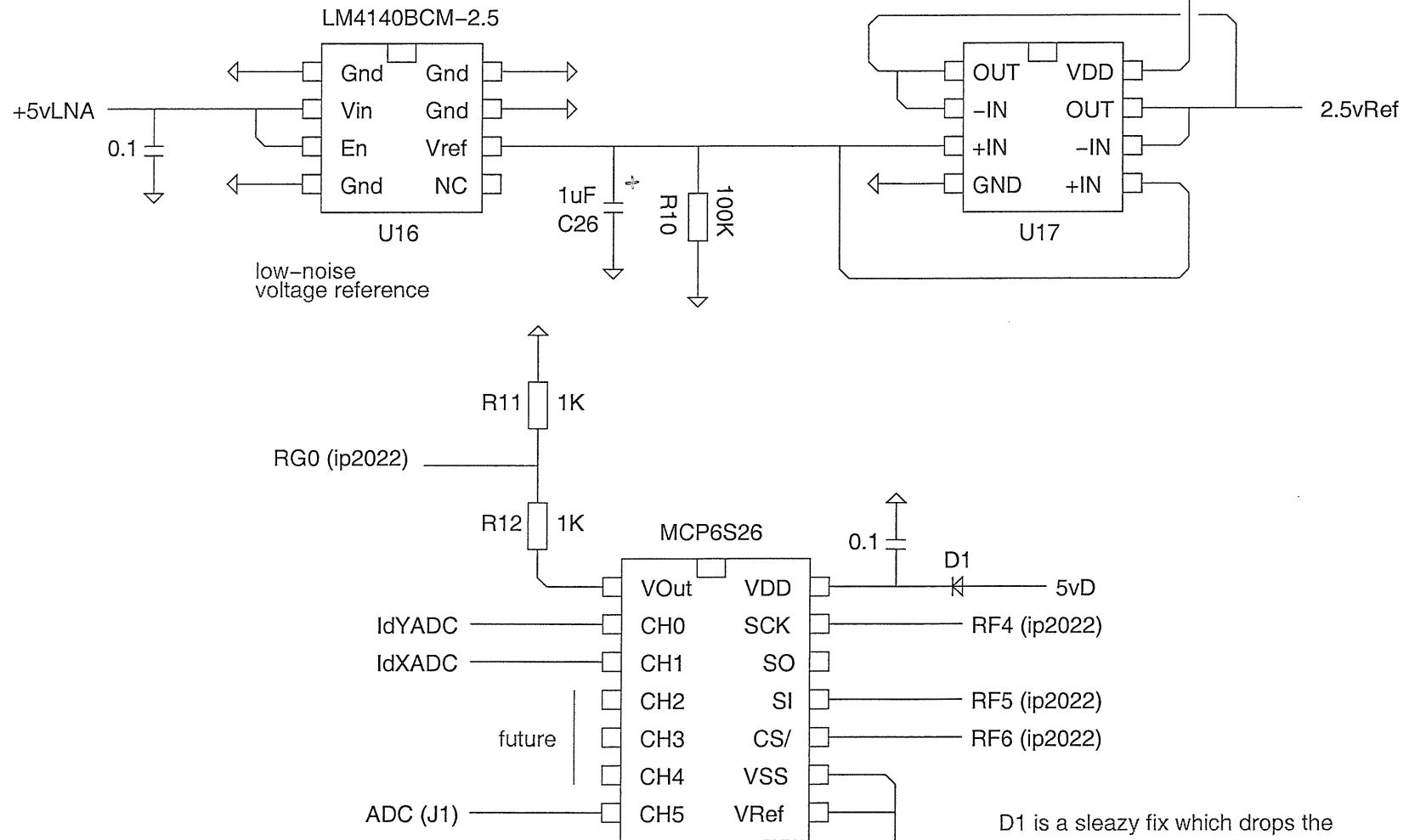


watchdog timeout = $400\text{ms} \times C(\text{pF}) / 47$

remove jumper to disable watchdog
when programming ip2022 via JTAG

✓
U15
C25
R9
D2

PAX Controller – Reference, ADC Multiplexer (6)

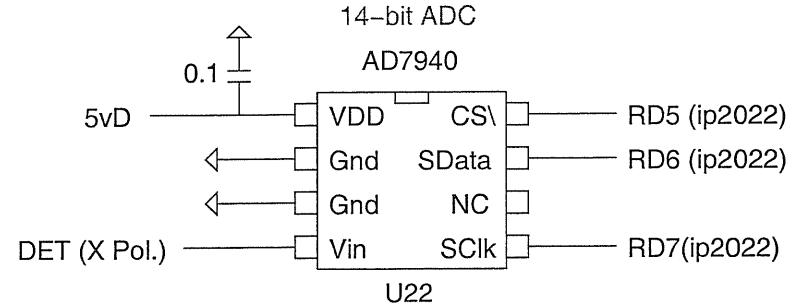
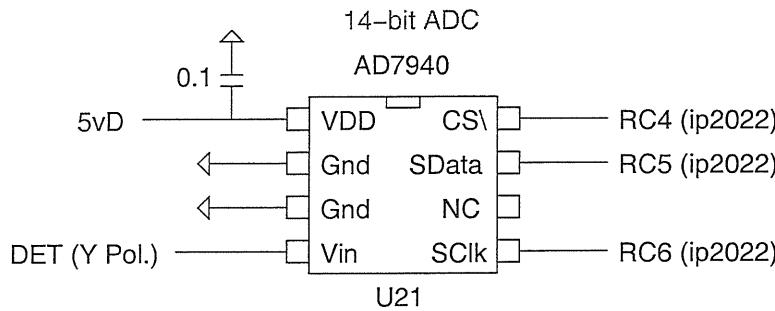
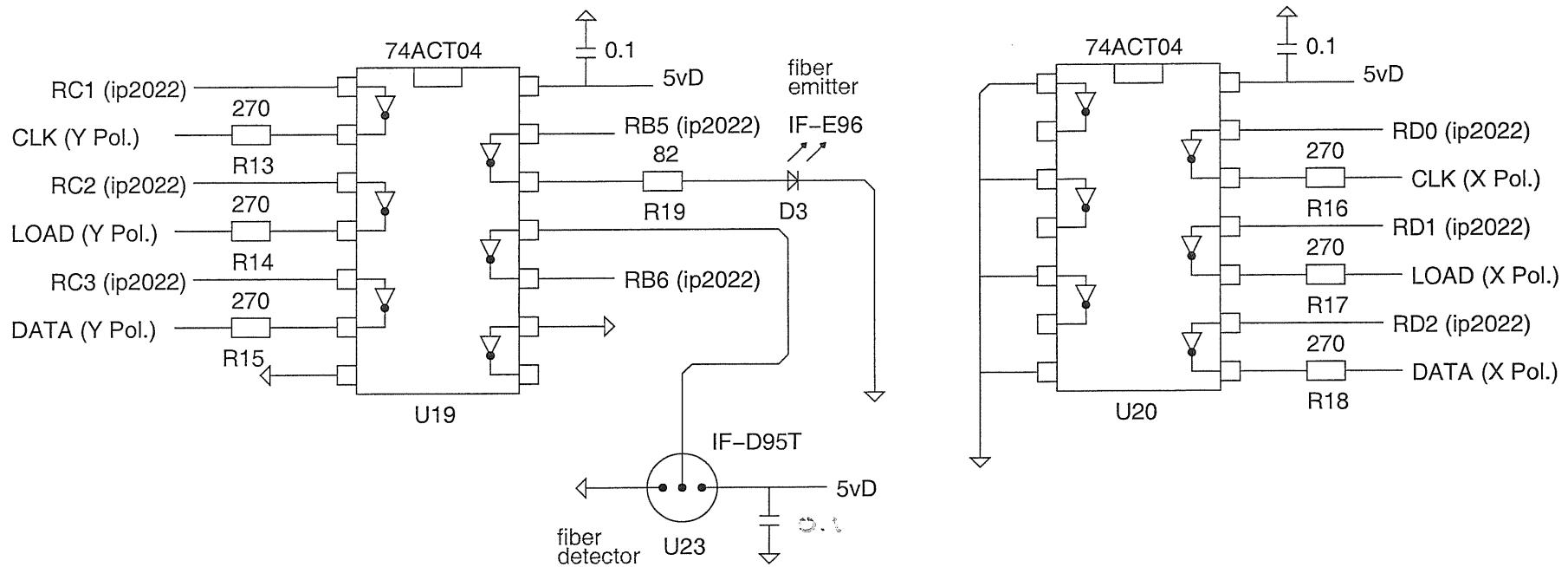


D1 is a sleazy fix which drops the MCP6S26 CMOS input voltage thresholds to be safely within range of the ip2022 3.3v CMOS outputs

U18
C26
R12
D2

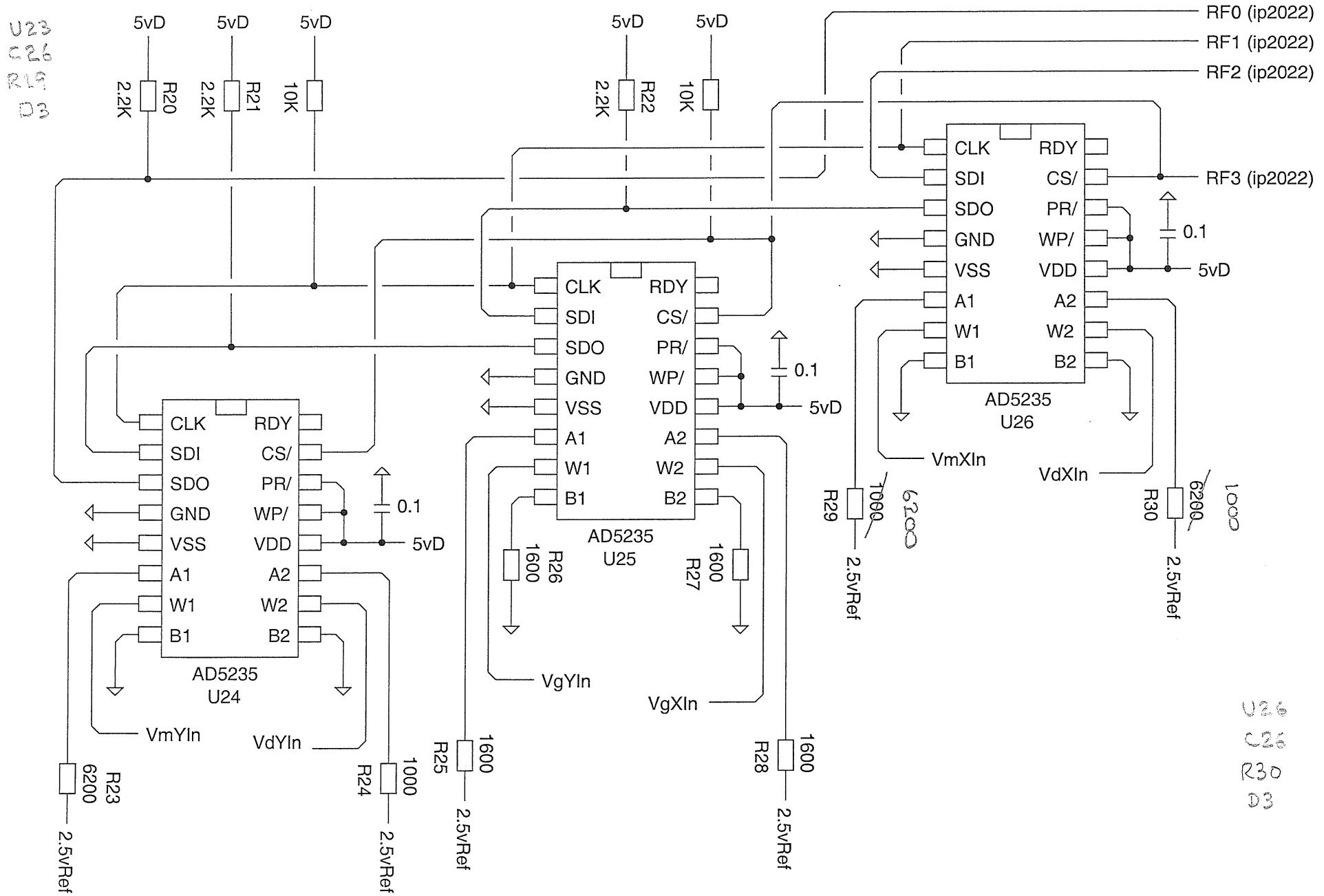
U18
C26
R12
D2

PAX Controller – Buffers, Detector ADCs (7)



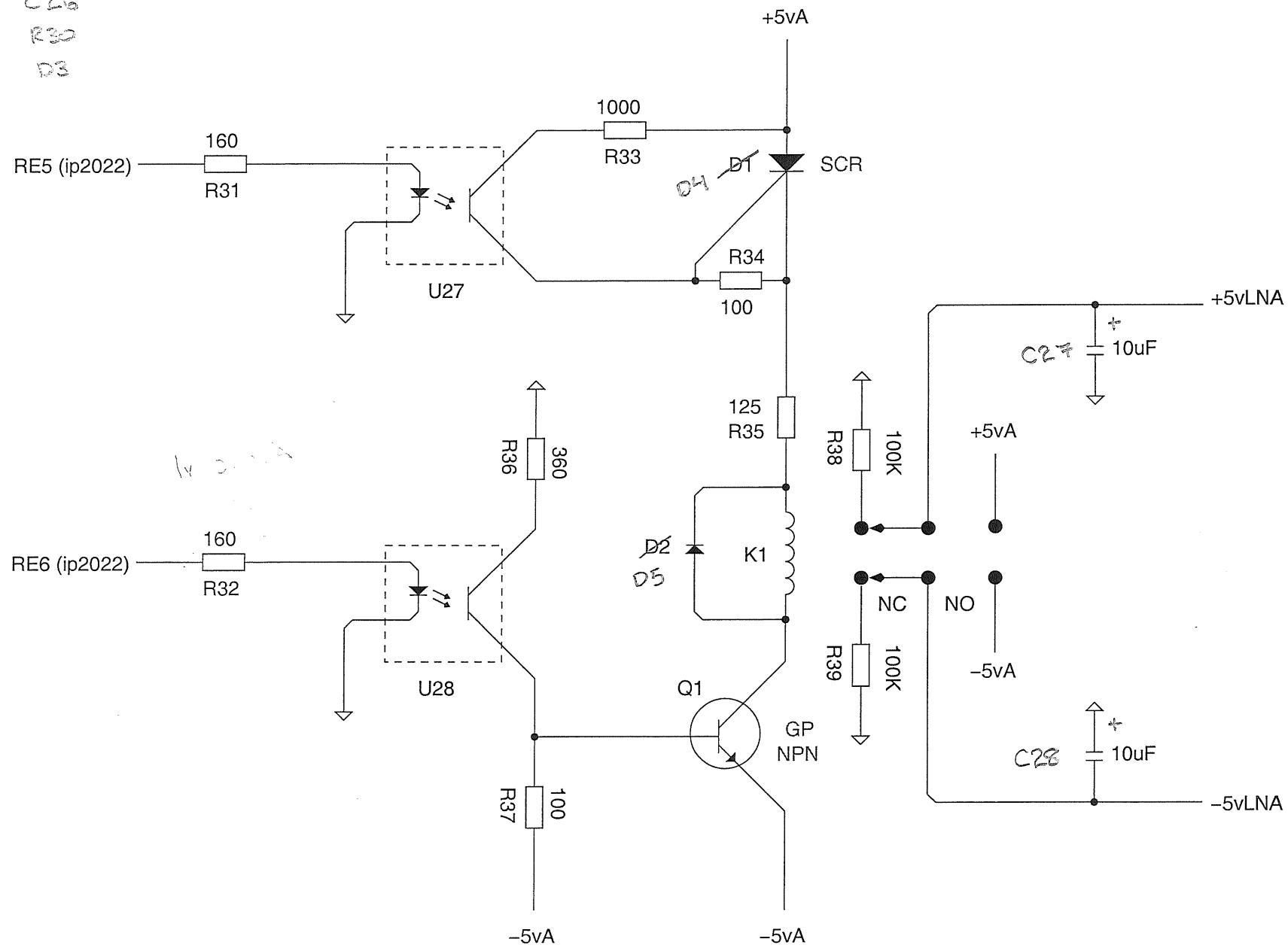
U23
C26
R12
D3

PAX Controller – Digital Potentiometers (8)



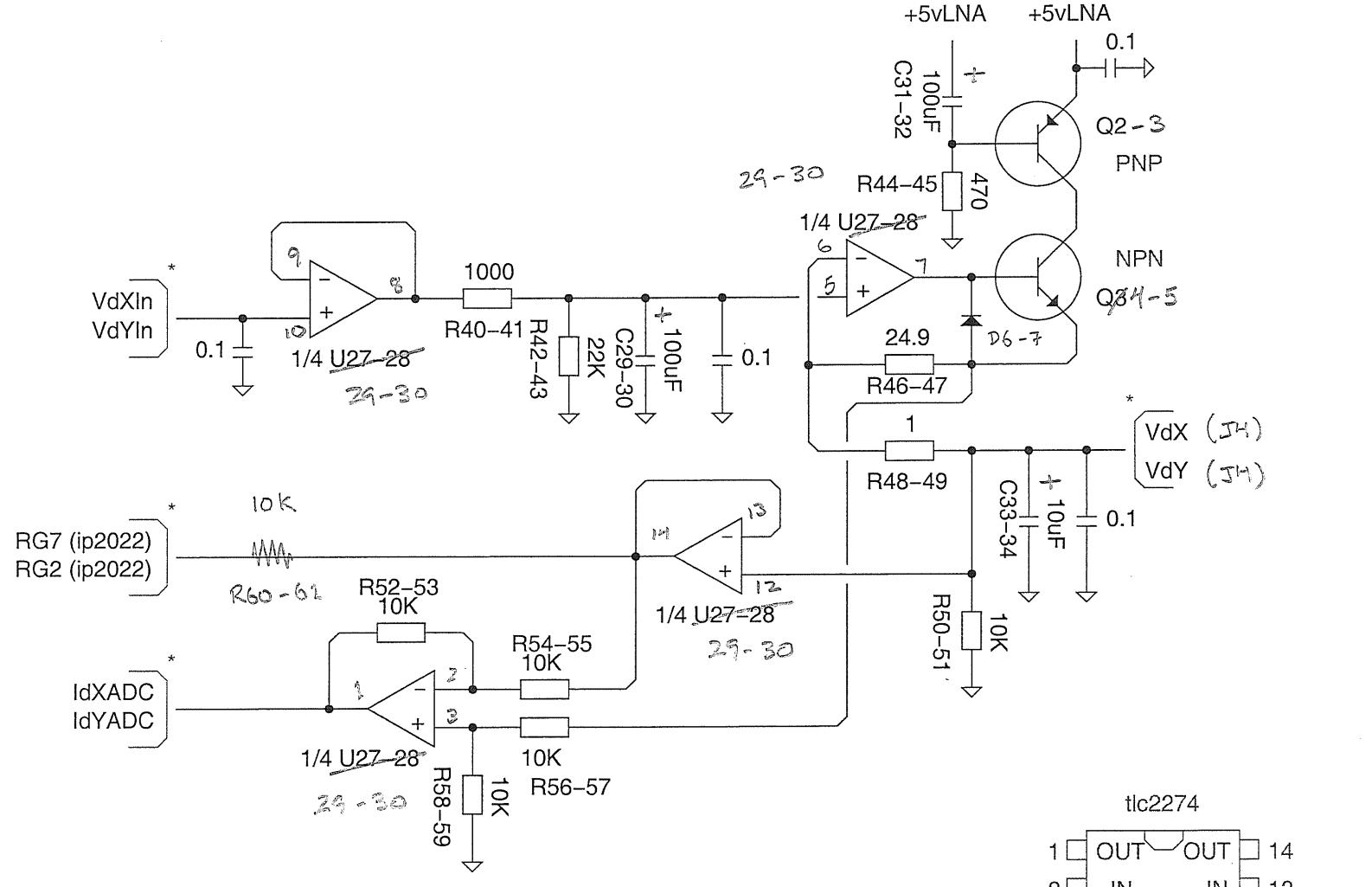
PAX Controller – LNA Bias Latch (9)

U26
C26
R32
D3

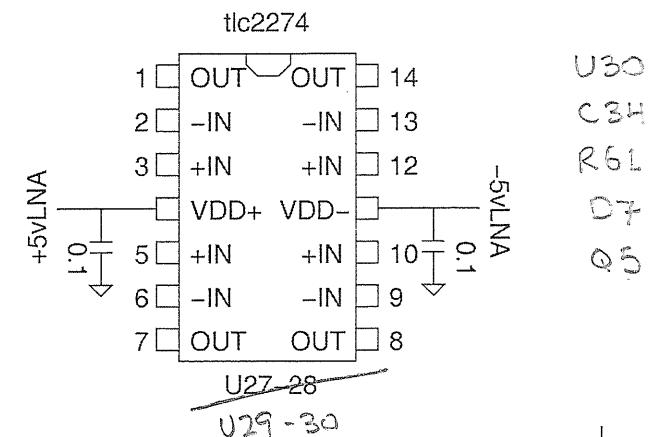


U28
C28
R39
D5
Q1

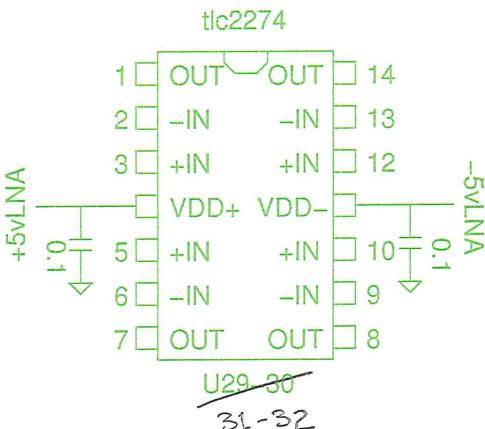
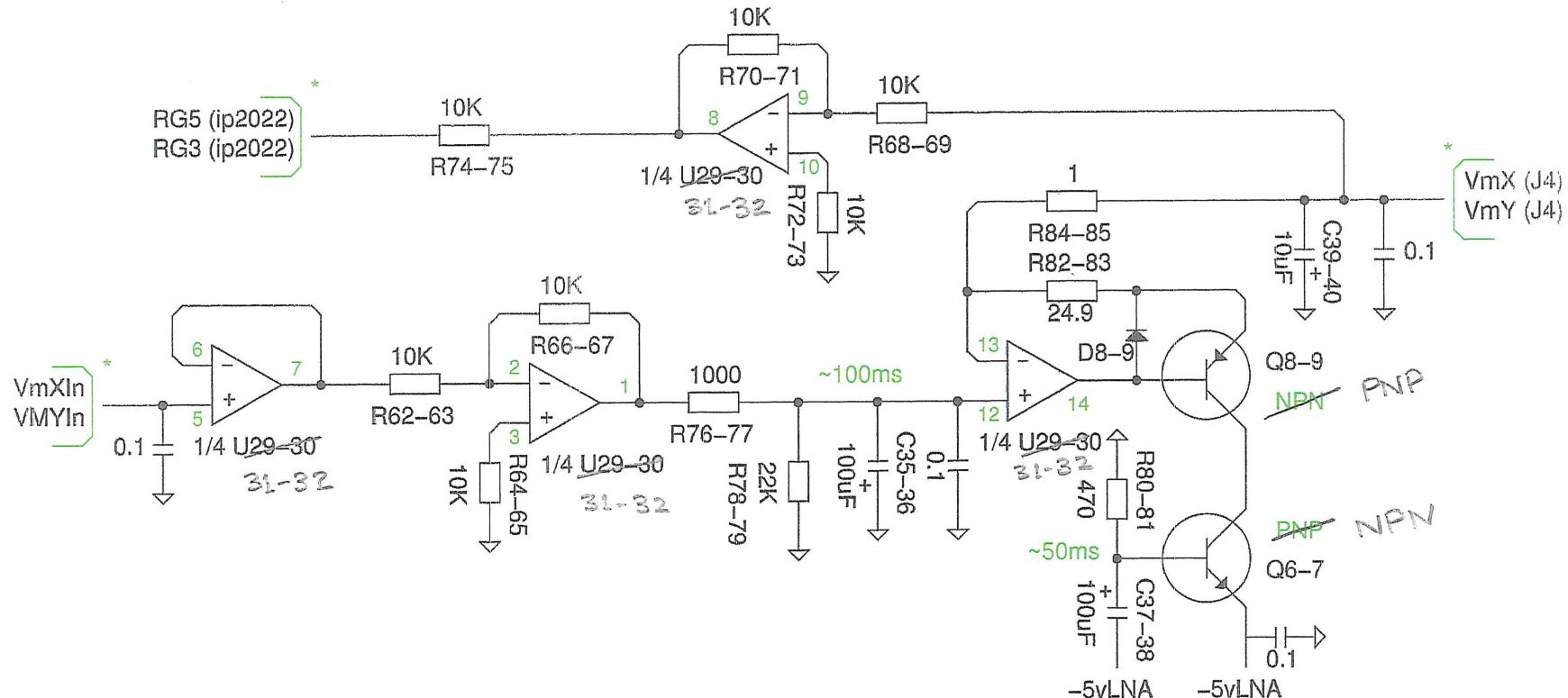
PAX Controller – Vd LNA Bias (10)



* two copies of this circuit



PAX Controller – Vm LNA Bias (11)

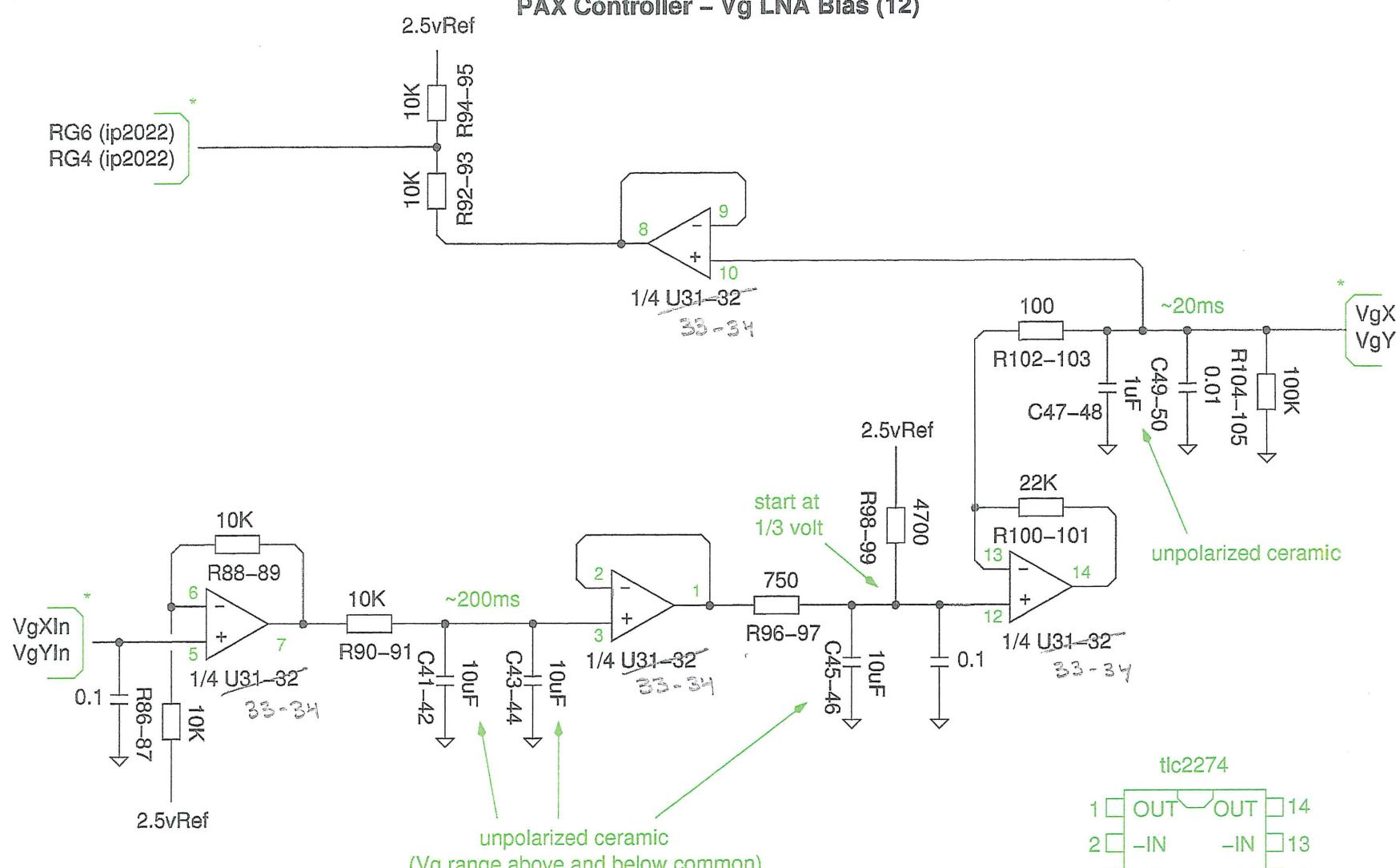


* two copies of this circuit: one for each polarization (multiple inputs and outputs shown)

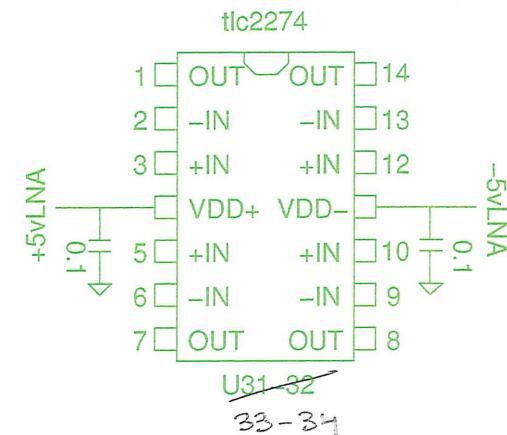
Note: this is a negative supply; therefore, tantalum capacitor polarity must be oriented positive with respect to ground.

U32
CHO
R85
D9
Q9

PAX Controller - Vg LNA Bias (12)



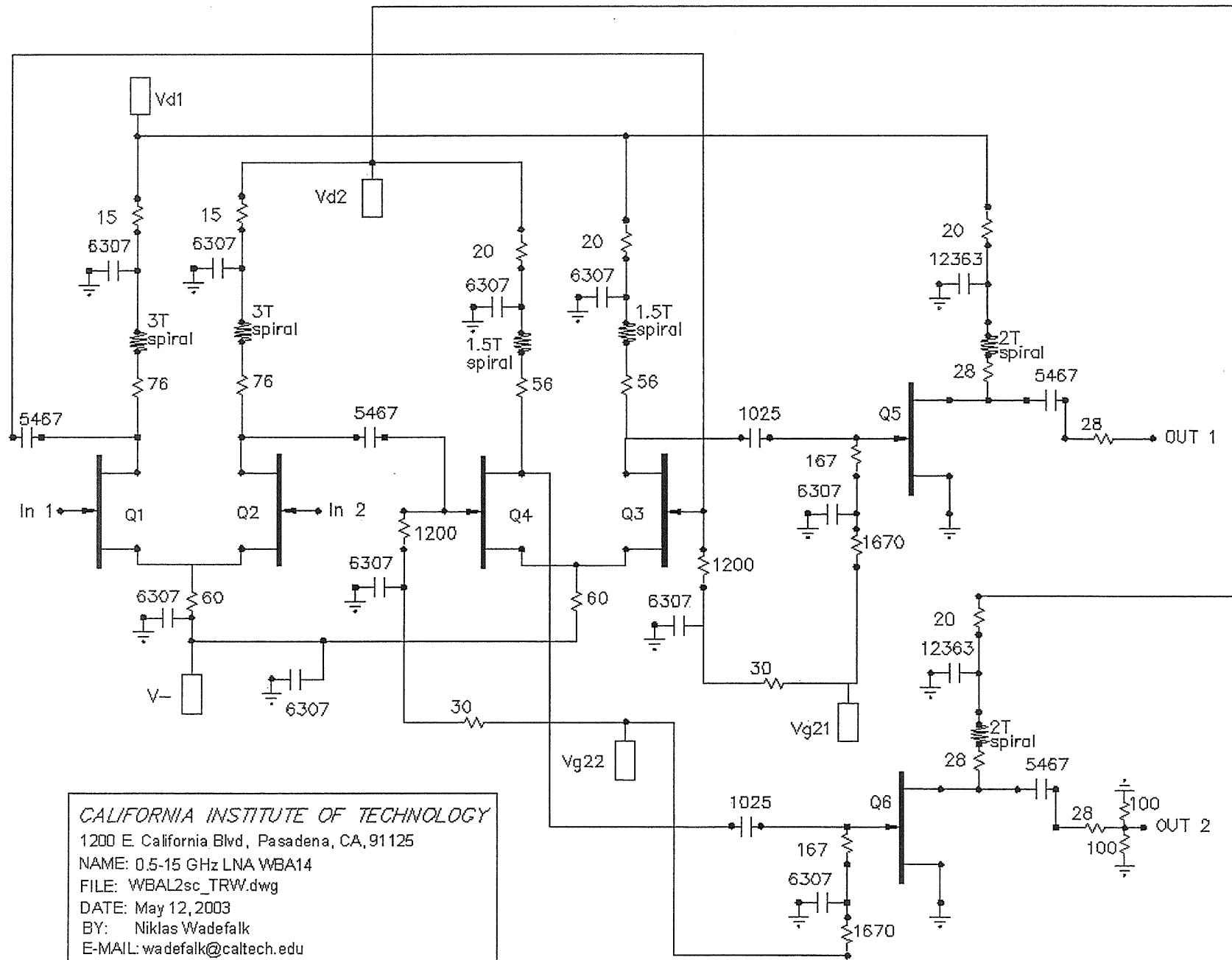
* two copies of this circuit: one for each polarization (multiple inputs and outputs shown)

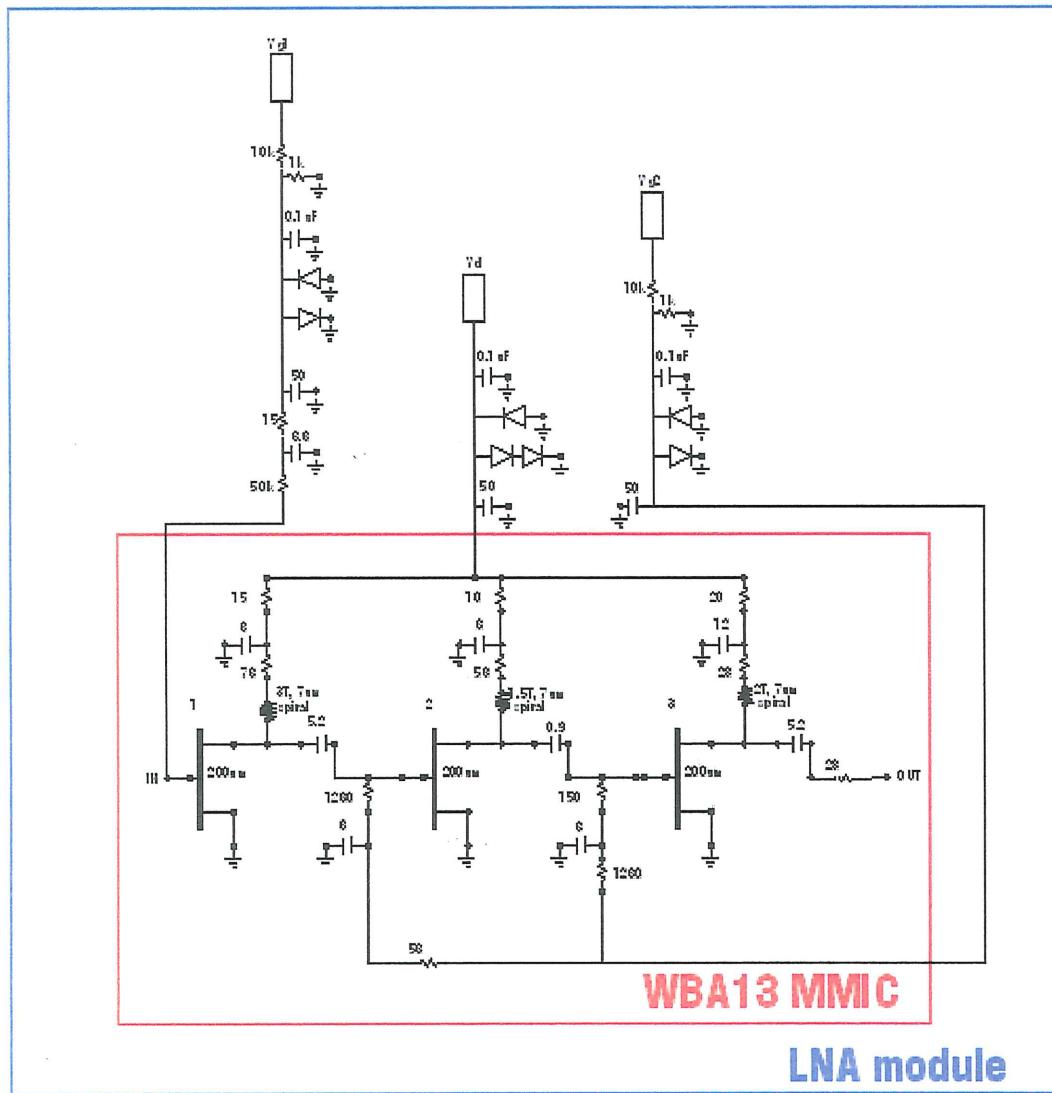


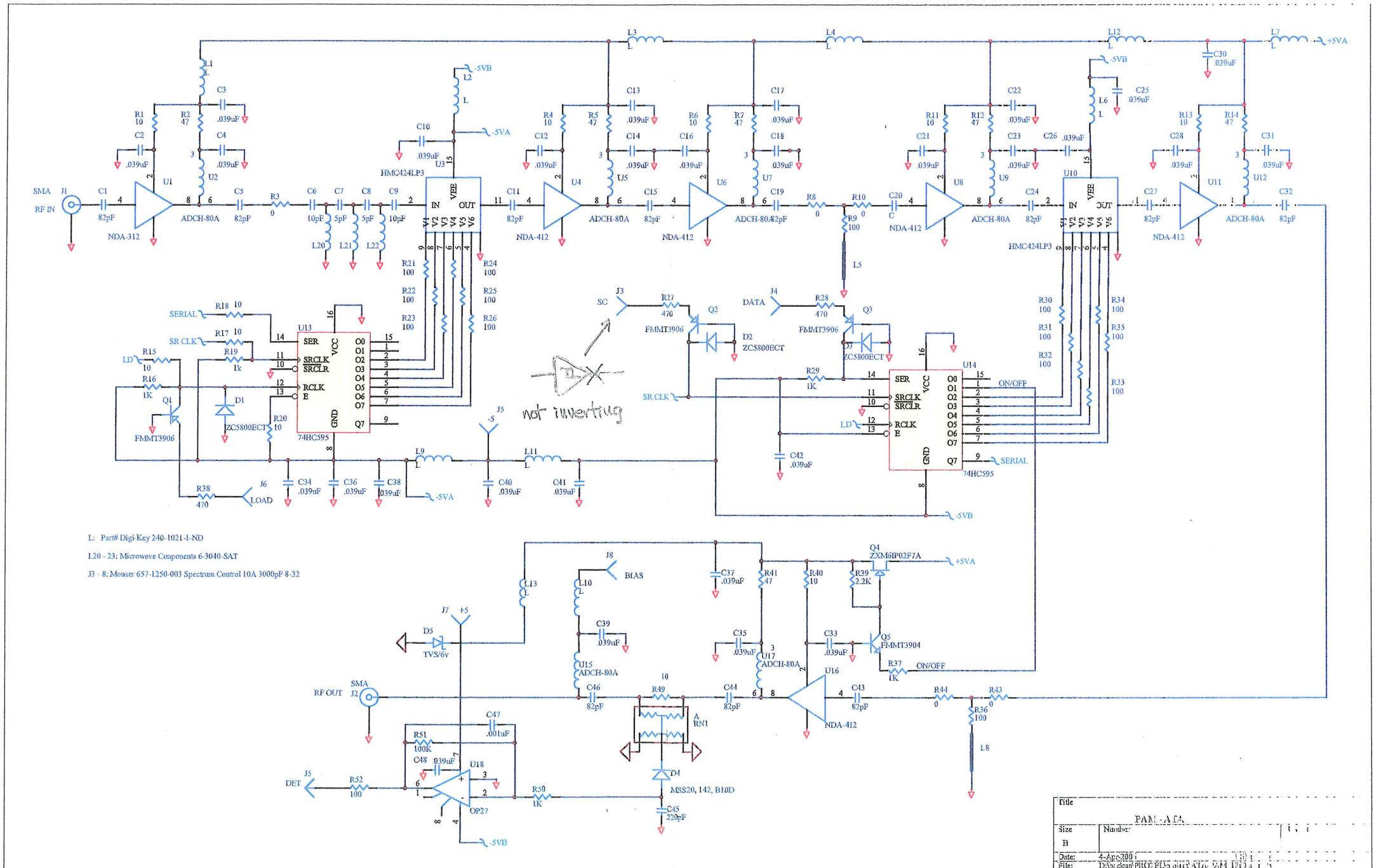
PAX Controller – Component List (13)

C1–6, C13–22, C24,							
C27, C28, C33–34, C39–40	10uF	tantalum capacitor, SMD, 10–20v	R42–43, R78–79, R100–101	22K ohm	1/8W resistor, 0805 SMD		
C7–12	22uF	tantalum capacitor, SMD, 10–20v	R46–47, R82–83	24.9 ohm	1/2W resistor, SMD		
C23, C26	1uF	tantalum capacitor, SMD, 10–20v	R48–49, R84–85	1 ohm	1/2W resistor, SMD		
C25	220pF	ceramic capacitor, SMD, 10–50v	R50–61, R62–75, R86–95	10K ohm	1/8W resistor, 0805 SMD		
C29–32, C35–38	100uF	tantalum capacitor, SMD, 10–20v	R96–97	750 ohm	1/8W resistor, 0805 SMD		
C41–46	10uF	ceramic capacitor, SMD, 10–50v					
C47–48	1uF	ceramic capacitor, SMD, 10–50v					
C49–50	0.01uF	ceramic capacitor, SMD, 10–50v					
D1, D6–9		GP silicon rectifier, SOT–23	U1–6	LT1117–5	low-dropout positive 5v regulator, SOT–223		
D2	blue	LED, 0805 SMD	U7–9	LT1175–5	low-dropout negative 5v regulator, SOT–223		
D3	IF-E96	fiber optic emitter, plastic 1000um	U10	ST2L01	dual 3.3v and adj. output positive regulator		
D4	(MCR08BT1)	SCR, 0.8A, SOT–223	U11	ip2022–PQ80	Ubicom microcontroller		
D5		GP silicon rectifier, 1A, SMA	U12	AT45DB041	Atmel serial flash, 8–SOIC		
J1–3		2x8 100mil header	U13	24MHz	oscillator, 3.3v (CB3LV–3C–24M0000–T)		
J4		2x10 100mil header	U14	TC77	Microchip digital temp. sensor, SOT–23–5		
J5		2x5 100mil header	U15	ADM696	Analog Devices watchdog, 16–SOIC		
K1		5v DPDT PCB relay	U16	LM4140BCM–2.5	2.5v voltage reference, 8–SOIC		
Q1	(MJD31C)	GP silicon NPN transistor, TO–252	U17	tlc2272	dual low-noise operational amplifier, 8–SOIC		
Q2–3, Q8–9	(MMBT2907ALT1)	GP silicon PNP transistor, SOT–23	U18	MCP6S26	Microchip prog. gain mux amp, 14–SOIC		
Q4–5, Q6–7	(MMBT4401LT1)	GP silicon NPN transistor, SOT–23	U19–20	74ACT04	hex TTL to CMOS inverter, 14–SOIC		
R1–2, R44–45, R80–81	470 ohm	1/8W resistor, 0805 SMD	U21–22	AD7940	Analog Devices 14-bit ADC, 8–MSOP		
R3–4	10 ohm	1/8W resistor, 0805 SMD	U23	IF-D95T	fiber optic detector, plastic 1000um		
R5	560 ohm	1/8W resistor, 0805 SMD	U24–26	AD5235	1024-step digital pot., 16–TSSOP		
R6	22 ohm	1/8W resistor, 0805 SMD	U27–28	(NTE3098)	LED to NPN transistor optoisolator		
R7, R31–32	160 ohm	1/8W resistor, 0805 SMD	U29–34	tlc2274	quad low-noise operational amplifier, 14–SOIC		
R8–9, R98–99	4.7K ohm	1/8W resistor, 0805 SMD					
R10, R38–39, R104–105	100K ohm	1/8W resistor, 0805 SMD					
R11–12, R24, R30, R33,							
R40–41, R76–77	1K ohm	1/8W resistor, 0805 SMD					
R13–18	270 ohm	1/8W resistor, 0805 SMD					
R19	82 ohm	1/8W resistor, 0805 SMD					
R20–22	2.2K ohm	1/8W resistor, 0805 SMD					
R23, R29	6.2K ohm	1/8W resistor, 0805 SMD					
R25–28	1.6K ohm	1/8W resistor, 0805 SMD					
R34, R37, R102–103	100 ohm	1/8W resistor, 0805 SMD					
R35	125 ohm	1/2W resistor, SMD					
R36	360 ohm	1/8W resistor, 0805 SMD					

Throughout the schematics are shown unnamed 0.1uF ceramic decoupling capacitors and 10K ohm 1/8W 0805 pull-up resistors.



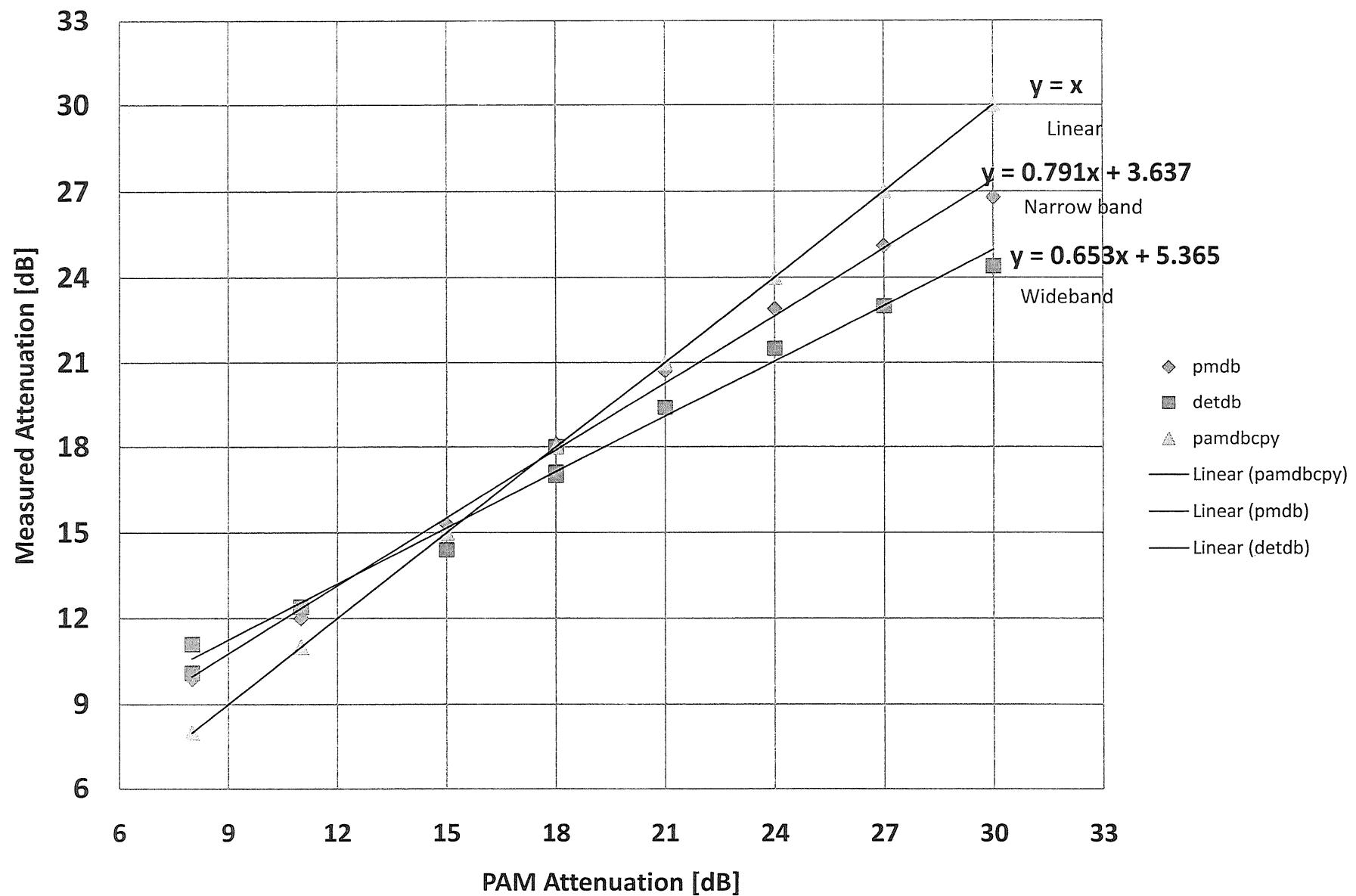


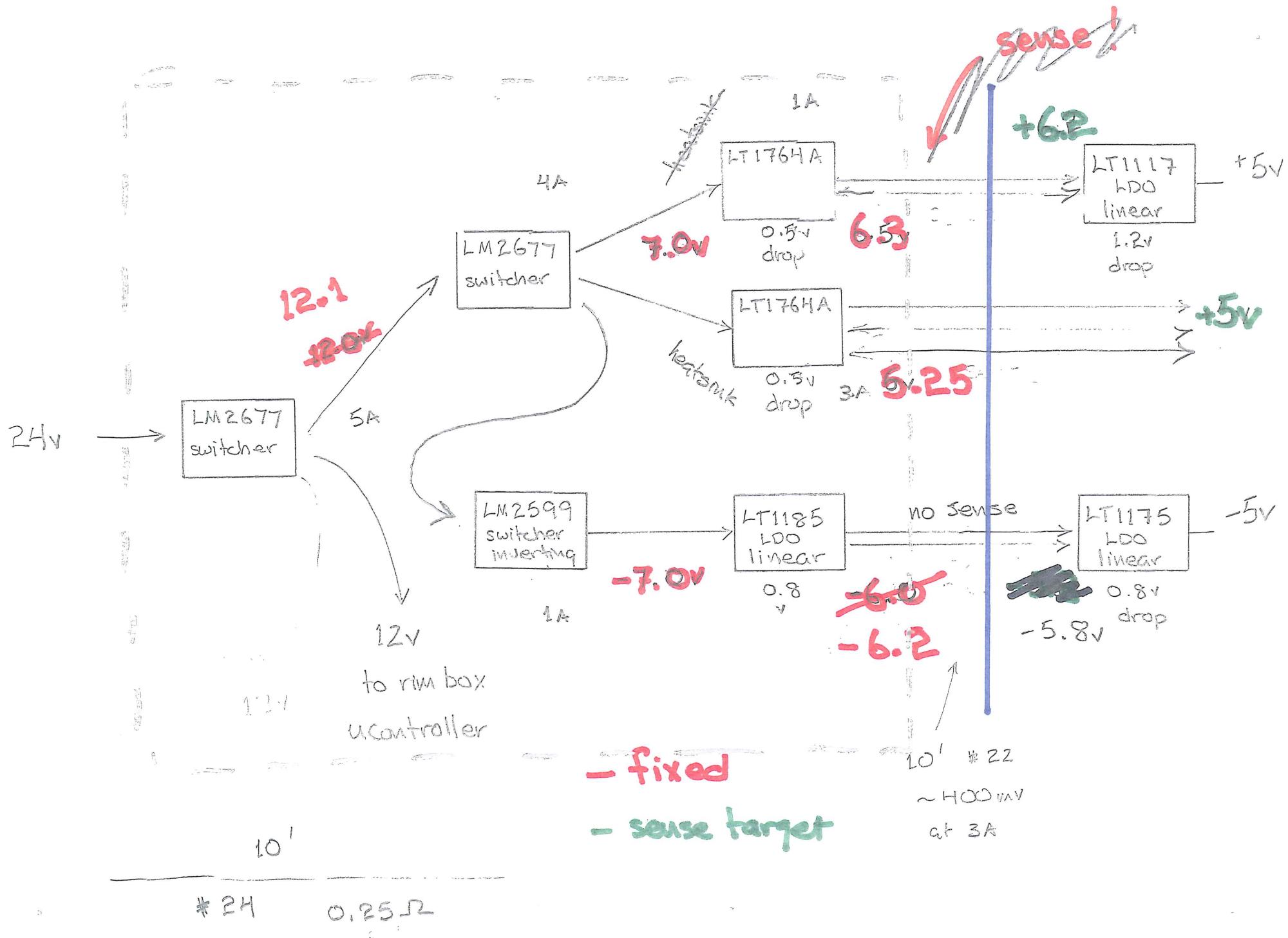


Rob, Something not shown on the schematic (and we found more recent one with the new detector, which is attached) at the serial clock (SC, ahead of R27) is a Schmitt Trigger:
 SN741VC1G17
 Single Schmitt-Trigger Buffer

Dave

3h Power Detector (non-)Linearity





1 PAX interface

Figure 1.1 below shows the front-panel of the PAX (which actually faces away from the feed) and the tables below give the pin-outs for the two filtered D-connectors.

Y-pol fiber cut

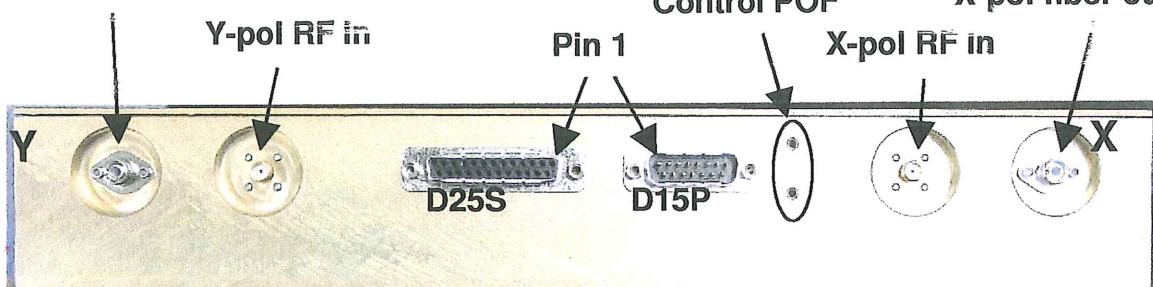


Figure 1.1: Annotated picture of the “front-panel” of the PAX box.

D25S – powers LNA’s from PAX control board. Connects to dewar.

D15P – powers PAX from rim power box (and temperature input). Connects to bottom of PAX case.

*Pin-out D25S

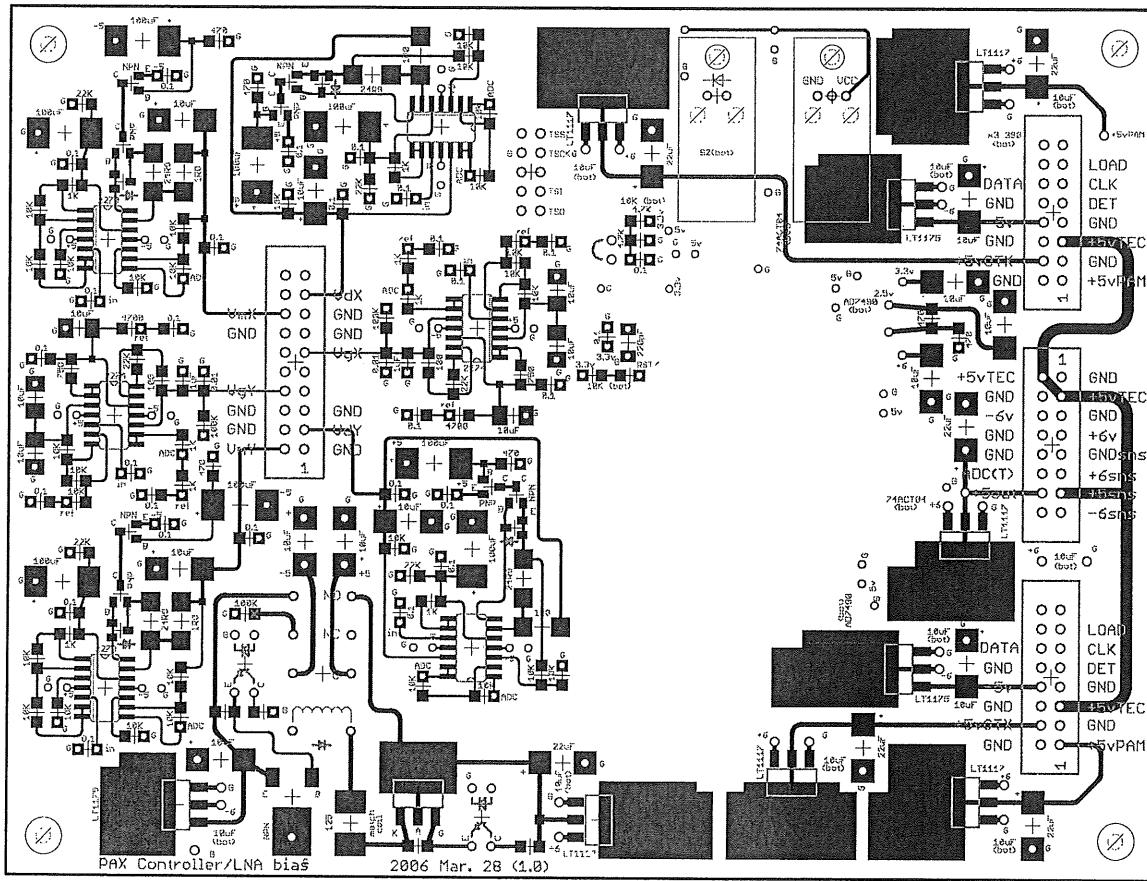
1	GND
2	Vdrain Y
3	GND
4	Future
5	Future
6	Vgate X
7	GND
8	GND
9	Vdrain X
10	NC
11	Future
12	NC
13	NC
14	Vminus Y
15	GND
16	GND
17	Vgate Y
18	Future
19	Future
20	GND
21	Vminus X
22	NC
23	Future
24	NC

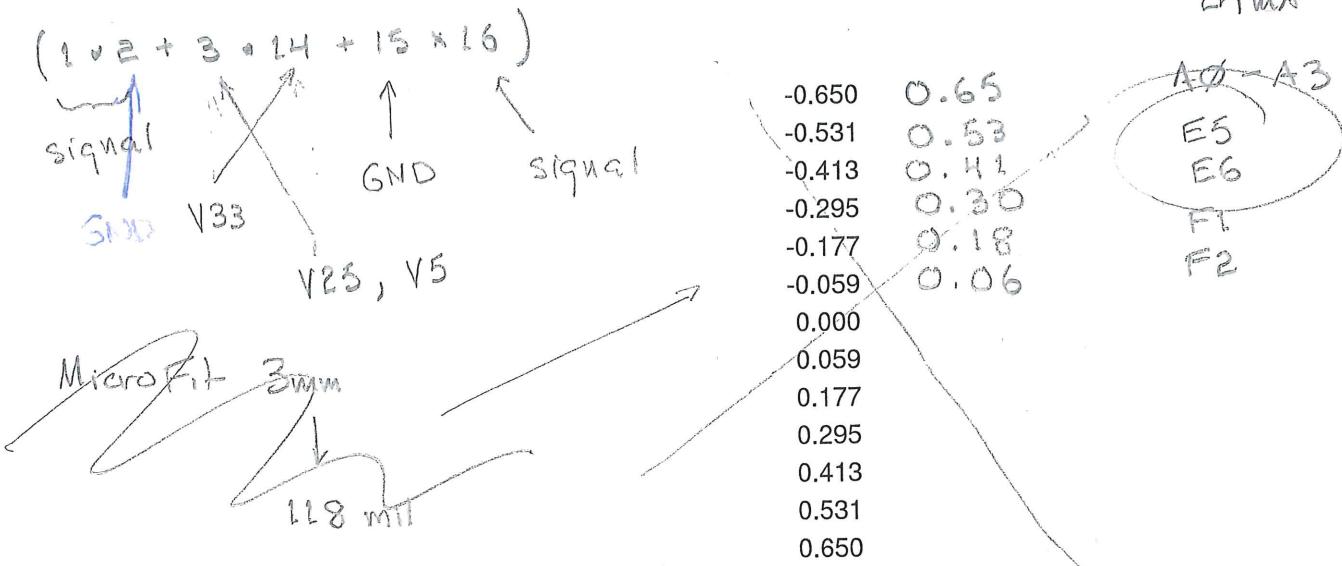
*Pin-out D15P

1	GND
2	+5 (OTXTEC)
3	GND
4	+6 (OTXlaser/PAM)
5	GNDsense
6	+6sense
7	+5sense
8	-5sense
9	+5 (OTXTEC)
10	GND
11	-5 (OTX/PAM)
12	GND
13	GND
14	T
15	+5 V out to T

See also section

~~- 6 (OTX /PAM)~~

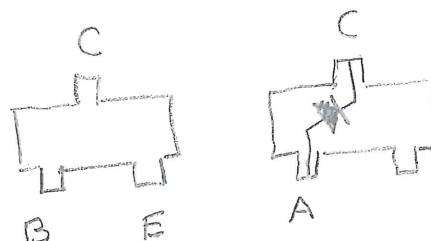
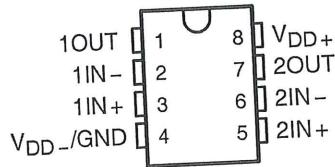




0.3 - 0.043327

0.18

TLC2272
D, JG, P, OR PW PACKAGE
(TOP VIEW)



TLC2274
D, J, N, PW, OR W PACKAGE
(TOP VIEW)

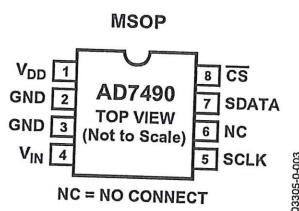
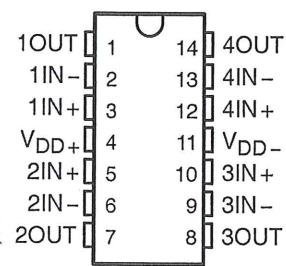
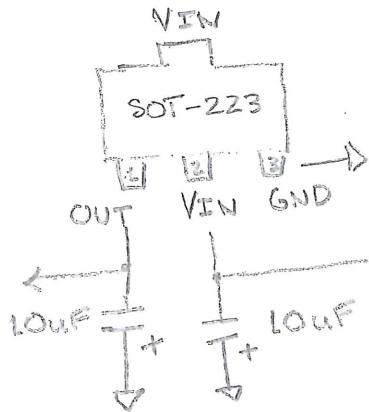


Figure 4. MSOP Pin Configuration

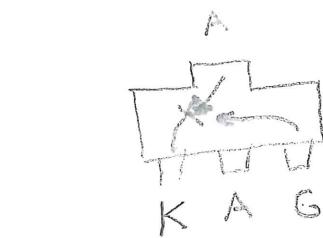


1 signal (analog)

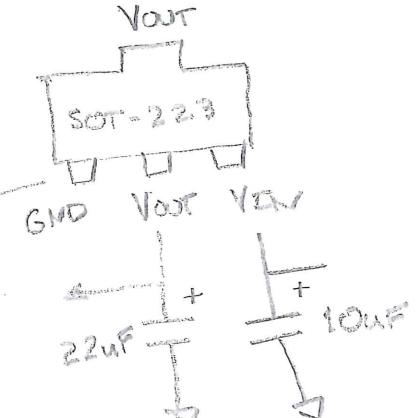
2 signal

3	V _{P6} +6	V _{P5} +5	V _S +5	V _{2.5} +5	V ₅ +5	V ₂₅
14	V _{M6} -6	V _{M5} -5	V _{3.3} +5	V ₃₃	V ₃₃	REF25
15	N	N				
	ground	ground				

26 signal (digital)



LT1117
(pos. 5V)



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

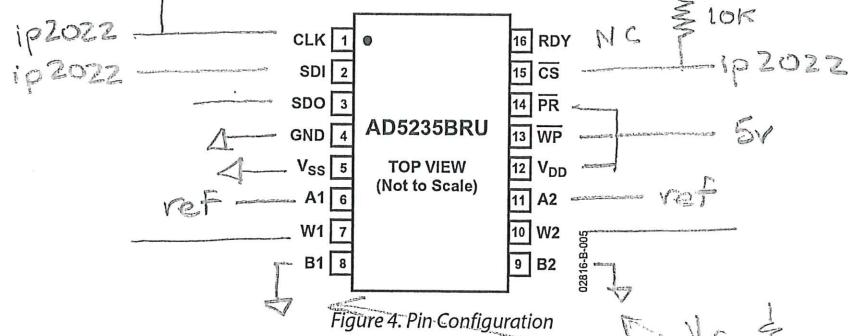
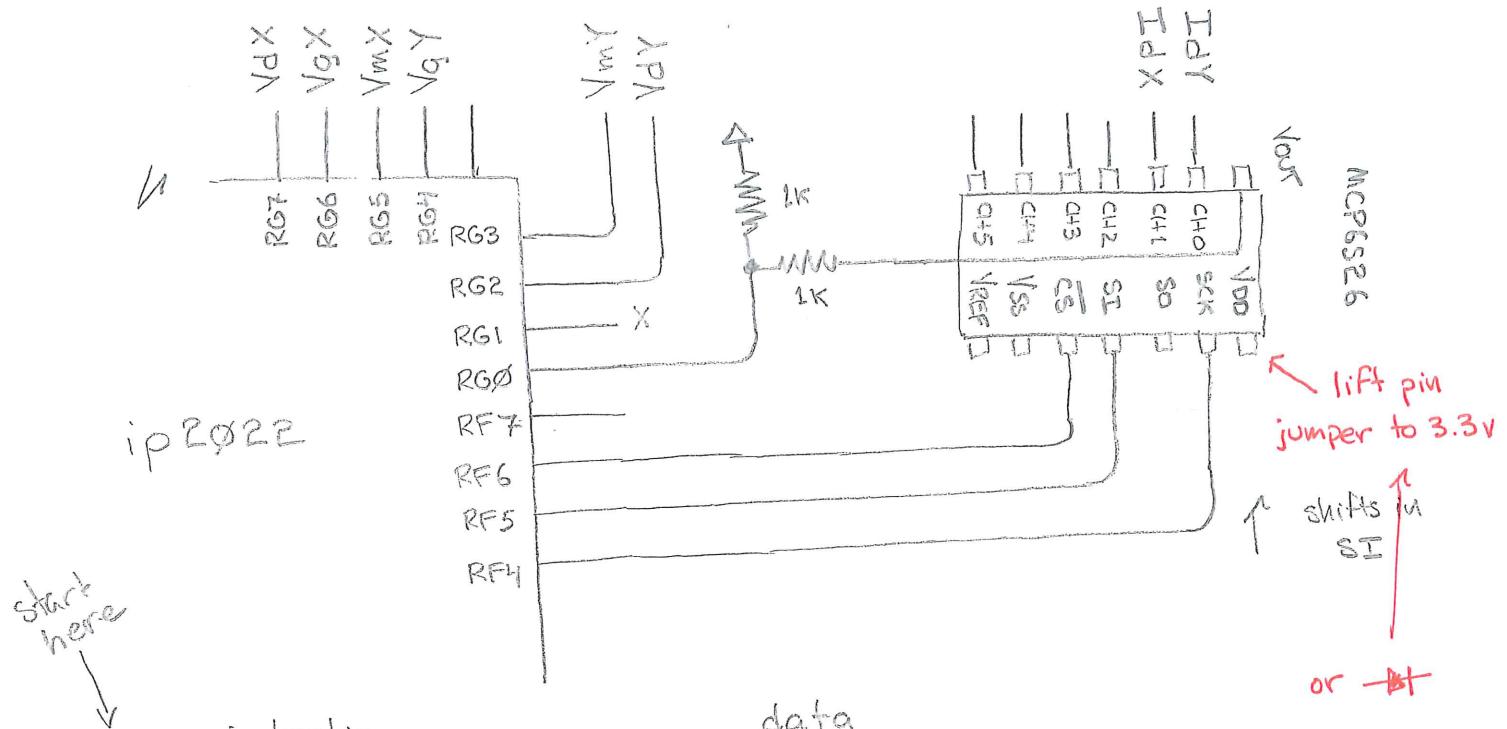


Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Input Register Clock. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input. Shifts in one bit at a time on positive clock CLK edges. MSB loads first.
3	SDO	Serial Data Output. Serves readback and daisy-chain functions. Commands 9 and 10 activate the SDO output for the readback function, delayed by 24 or 25 clock pulses, depending on the clock polarity before and after the data-word (see Figure 2, Figure 3, and Table 7). In other commands, the SDO shifts out the previously loaded SDI bit pattern, delayed by 24 or 25 clock pulses depending on the clock polarity (see Figure 2 and Figure 3). This previously shifted-out SDI can be used for daisy-chaining multiple devices. Whenever SDO is used, a pull-up resistor in the range of 1 kΩ to 10 kΩ is needed.
4	GND	Ground Pin, Logic Ground Reference.
5	V _{ss}	Negative Supply. Connect to 0 V for single-supply applications. If V _{ss} is used in dual supply, it must be able to sink 35 mA for 30 ms when storing data to EEMEM.
6	A1	Terminal A of RDAC1.
7	W1	Wiper terminal of RDAC1. ADDR(RDAC1) = 0x0.
8	B1	Terminal B of RDAC1.
9	B2	Terminal B of RDAC2.
10	W2	Wiper terminal of RDAC2. ADDR(RDAC2) = 0x1.
11	A2	Terminal A of RDAC2.
12	V _{DD}	Positive Power Supply.
13	WP	Optional Write Protect. When active low, <u>WP</u> prevents any changes to the present contents, except <u>PR</u> strobe. CMD_1 and COMD_8 refresh the RDAC register from EEMEM. Execute a NOP instruction before returning to <u>WP</u> high. Tie <u>WP</u> to V _{DD} , if not used.
14	PR	Optional Hardware Override Preset. Refreshes the scratchpad register with current contents of the EEMEM register. Factory default loads midscale 512 ₁₀ until EEMEM is loaded with a new value by the user. <u>PR</u> is activated at the logic high transition. Tie <u>PR</u> to V _{DD} , if not used.
15	CS	Serial Register Chip Select Active Low. Serial register operation takes place when <u>CS</u> returns to logic high.
16	RDY	Ready. Active-high open-drain output. Identifies completion of Instructions 2, 3, 8, 9, 10, and <u>PR</u> .



instruction
8b data
8b | 8b



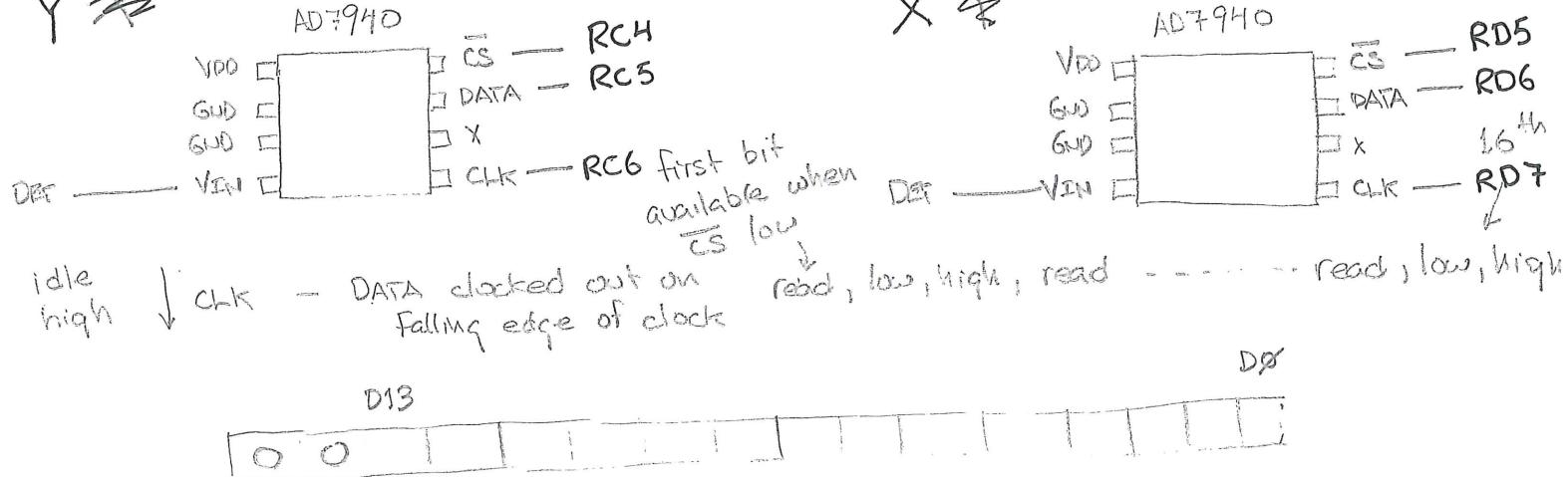
0 1 0	A0	X	X	X	X	X	0 0 0	CH0
							0 0 1	CH1
							0 1 0	CH2
							0 1 1	CH3
							1 0 0	CH4
							1 0 1	CH5
							1 1 0	
							1 1 1	

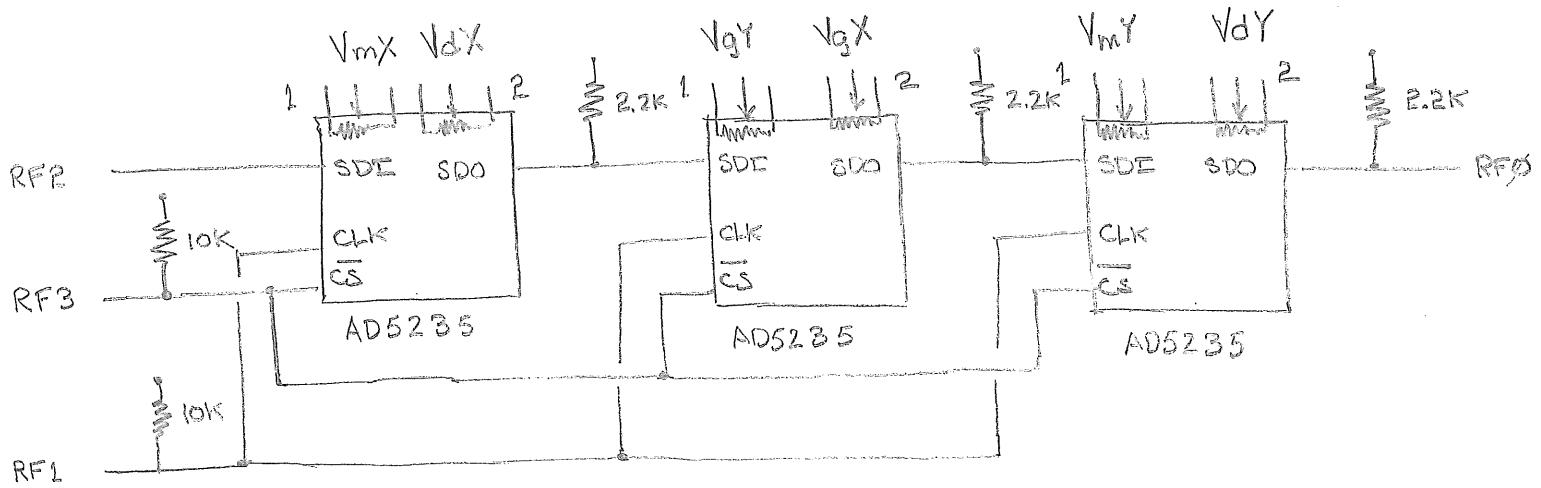
$$0.7 \cdot H.H =$$

3.1

high threshold

Y





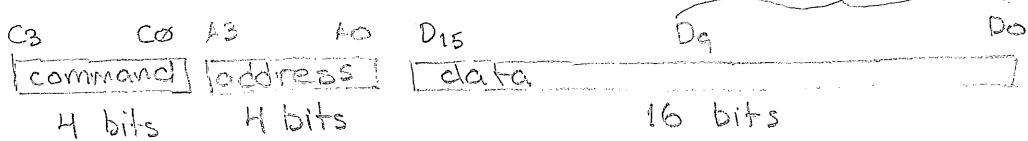
CLK ↑ shifts in SDI

SDI MSB first

CS active low, operation takes place when CS returns high

0000 - RDAC1

0001 - RDAC2



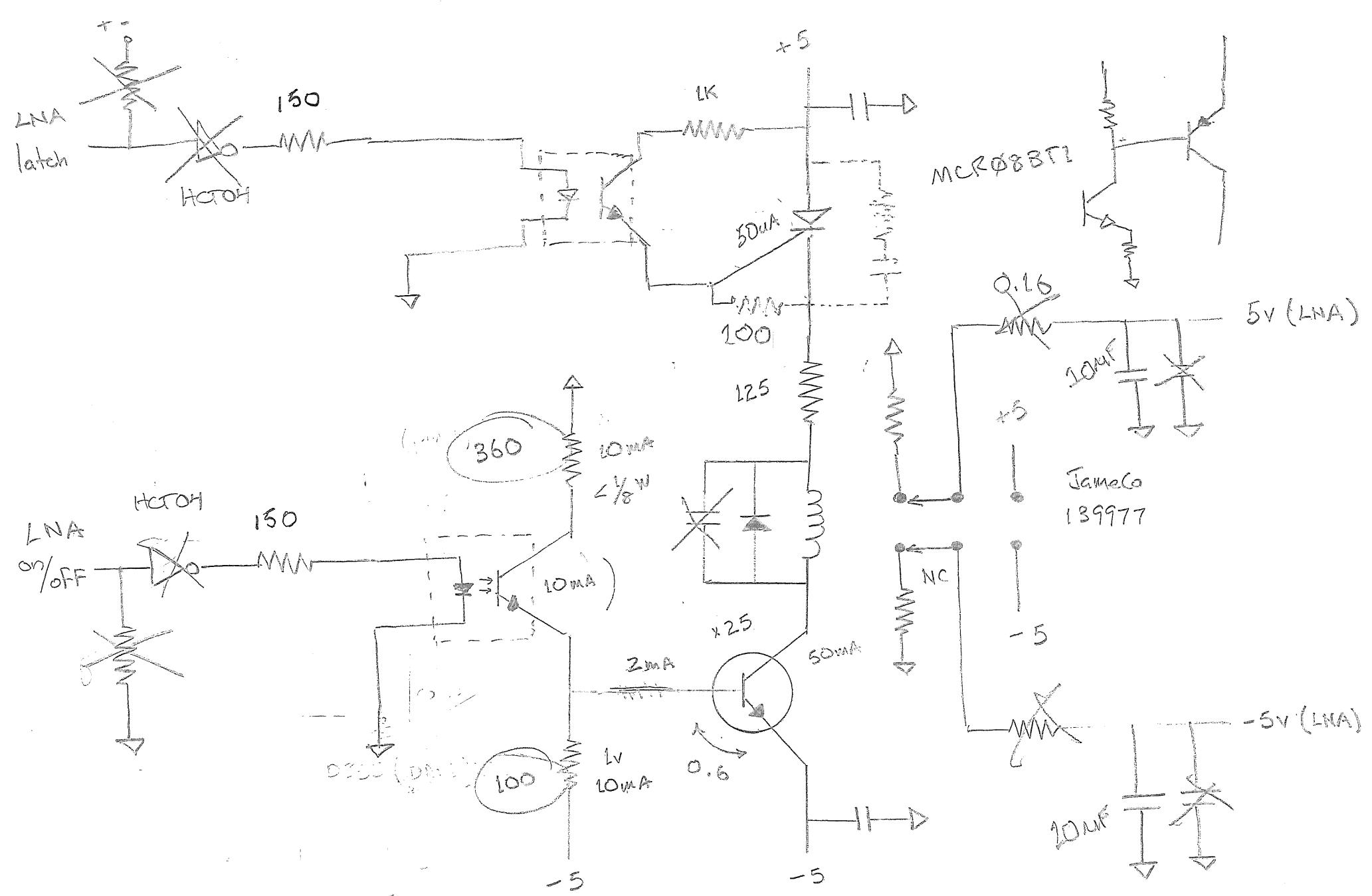
1011 - write data
to RDAC

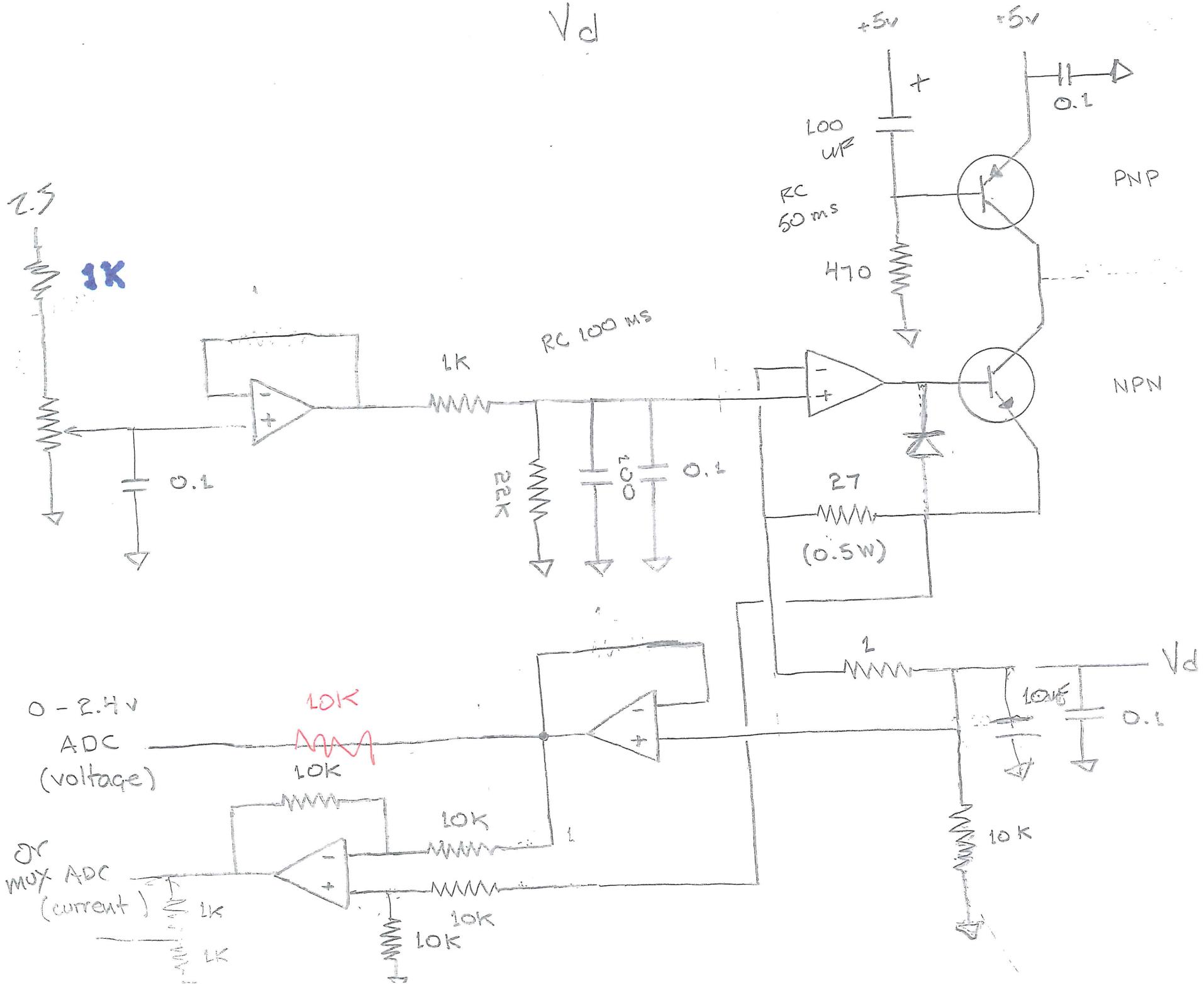
0000 - NOP

0010 - store RDAC to EEPROM

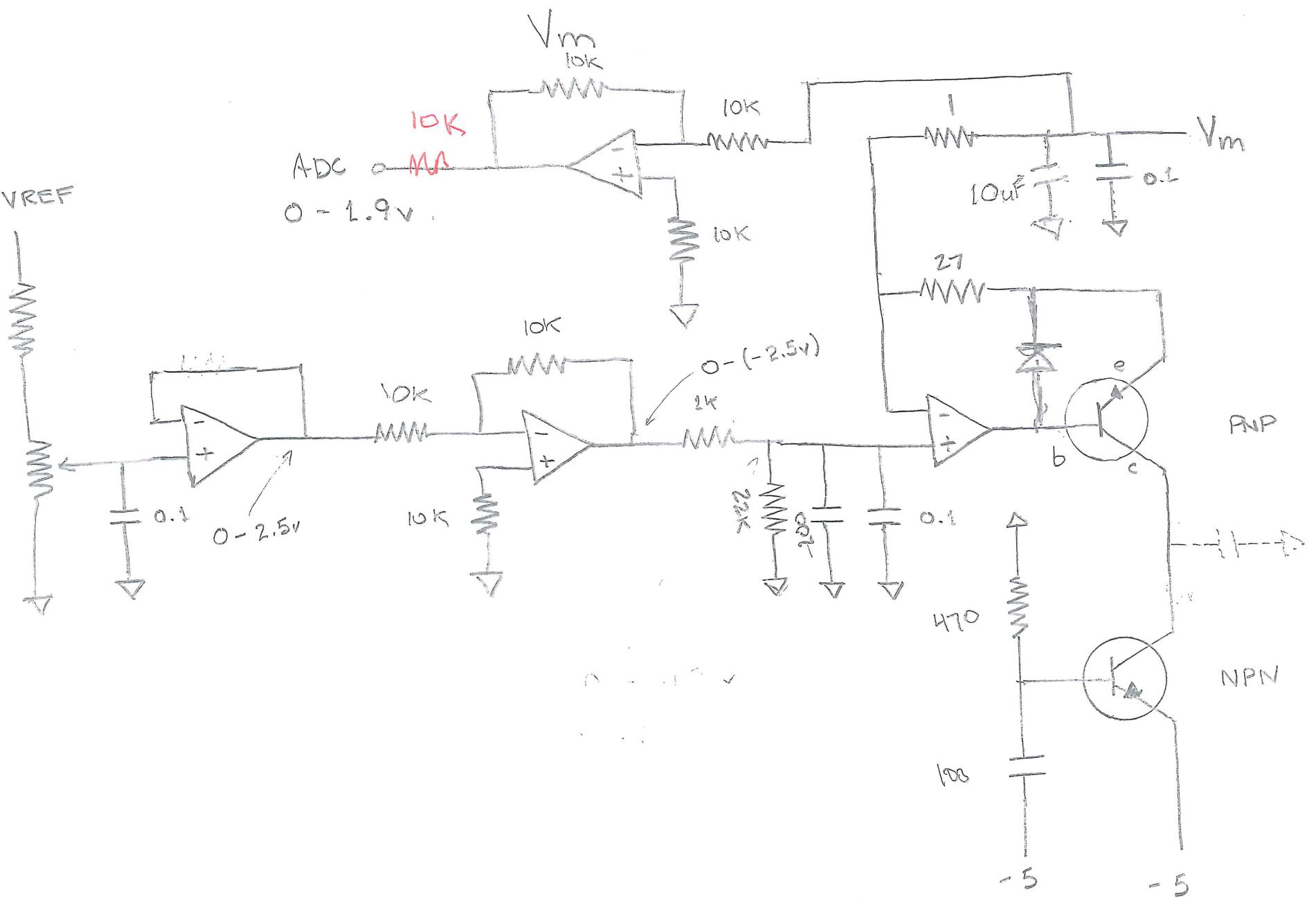
25 ms

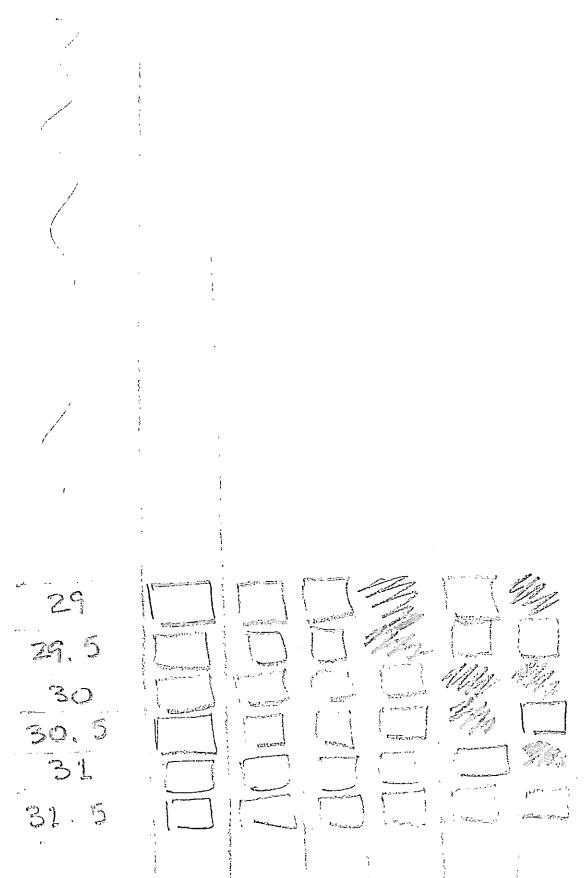
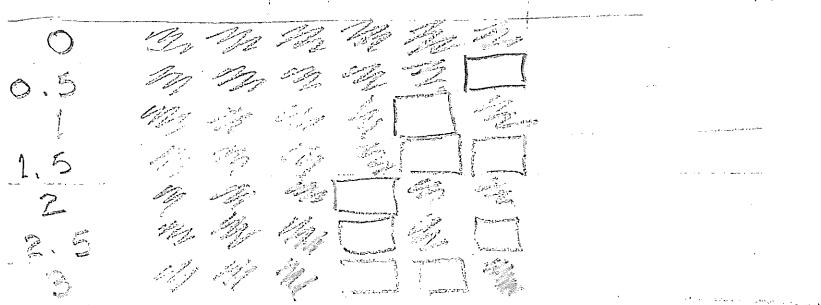
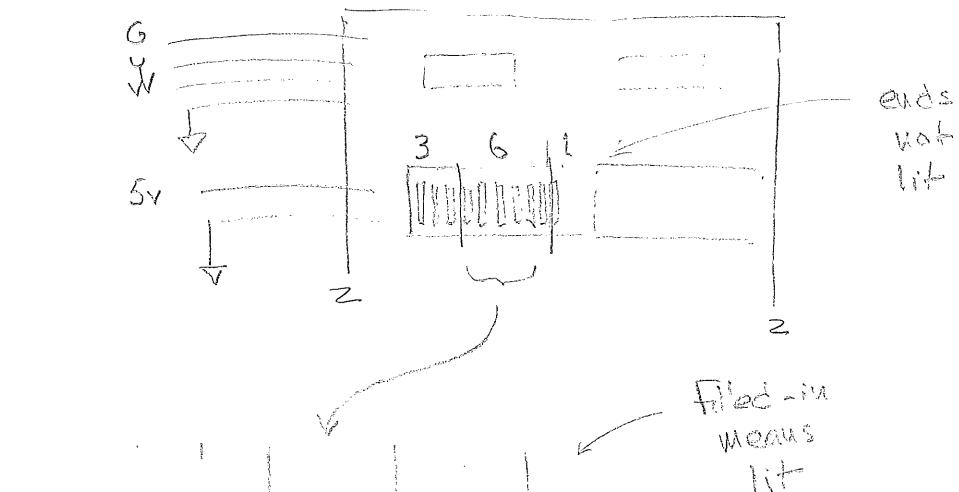
read
inc or dec
until target
voltage reached



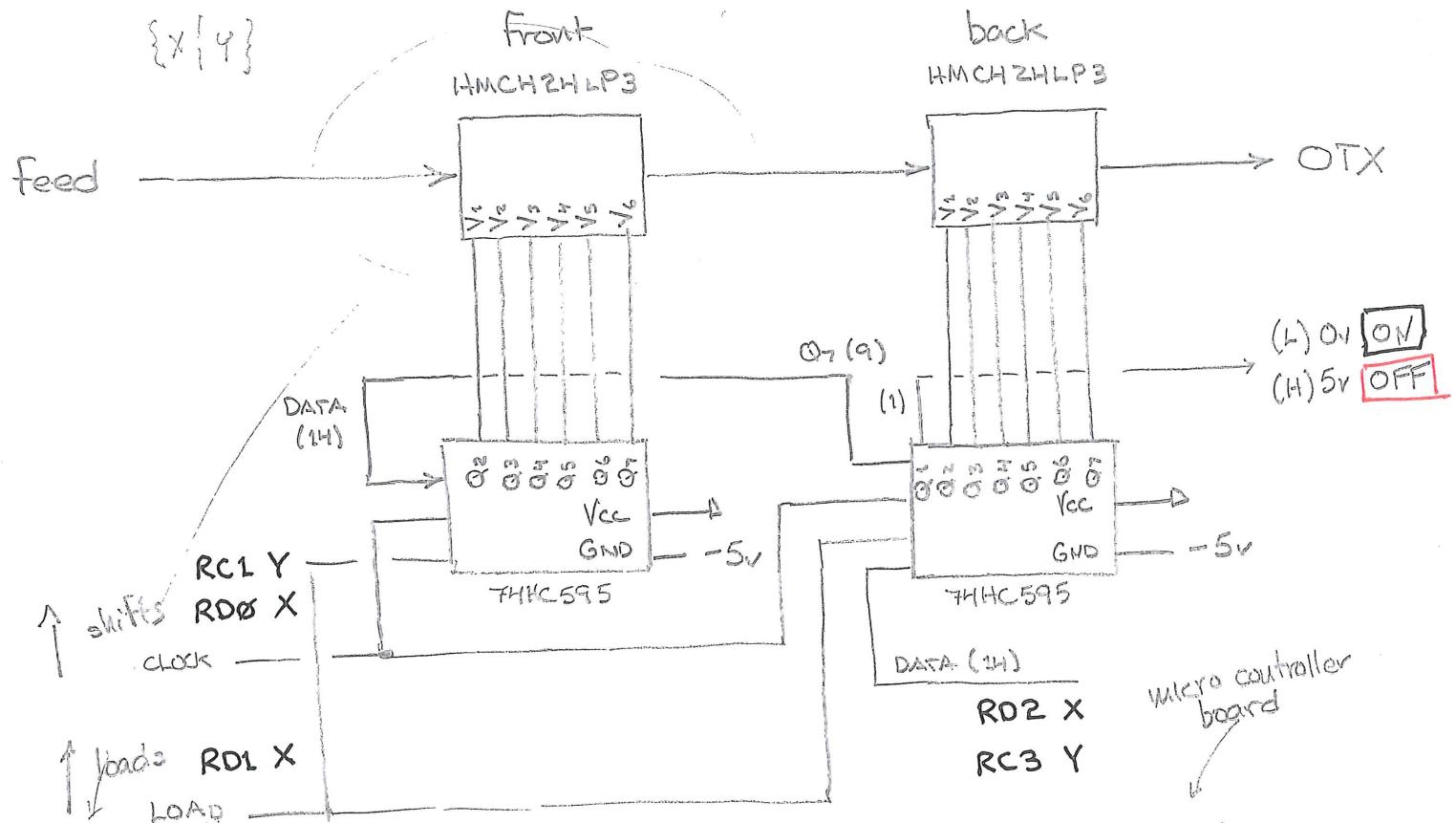


2.5VREF





setpam [{on|off}] [back-atten front-atten]



(L) low 0v RC2 Y
(H) high -5v

1st →
dark →

(L) -5v ↔ (L) 0v
(H) 0v ↔ (H) 5v

$V_1 \quad V_2 \quad V_3 \quad V_4 \quad V_5 \quad V_6$

L	L	L	L	L	L	0dB
L	L	L	L	L	H	0.5 dB
L	L	L	H	H	L	1 dB

$Q_2 \quad Q_3 \quad Q_4 \quad Q_5 \quad Q_6 \quad Q_7$

<input checked="" type="checkbox"/>					
<input checked="" type="checkbox"/>					
<input checked="" type="checkbox"/>					

LOAD

DATA

CLK

microcontroller board

PAM

PNP

$V_1 \quad V_2 \quad V_3 \quad V_4 \quad V_5 \quad V_6$

H	L	L	L	L	L	16dB
H	H	H	H	H	H	31.5 dB

<input checked="" type="checkbox"/>					
<input checked="" type="checkbox"/>					
<input checked="" type="checkbox"/>					

from perspective of ip2021 pms:

while idle set DATA, CLK, LD high

do 16 times

set DATA bit

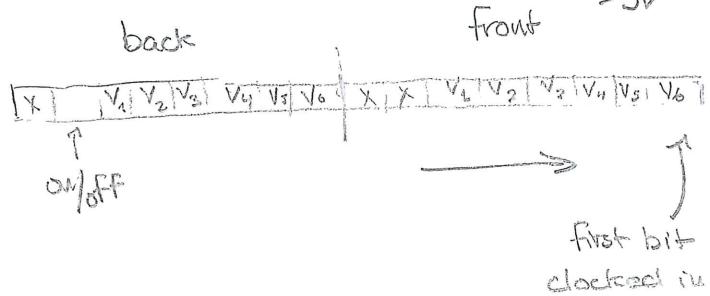
set CLK low

set CLK high

end

set LOAD low

set LOAD high



first bit clocked in

**Notes on the Active Balun Power Supply Taken from E-mails from
Niklas and Sandy.**

DRD
April 5, 2005

The active balun LNA (ABLNA) design requires 3 supply voltages (V_d , V_g , V_m) as well as, operationally, one current (I_d) monitor per amplifier . Typical values based on Niklas's April visit to Minex, are:

Active balun bias @300K

V_d	2.00V	Supply
I_d	100mA	Monitor
V_g	varies	Supply
I_g	varies	
V_m	-1.70V	Supply
I_m	53mA	

Active balun bias @50K

V_d	1.40V	Supply
I_d	55mA	Monitor
V_g	varies	Supply
I_g	varies	
V_m	-1.00V	Supply
I_m	32mA	

Pinch-off test:

- 1) Connect the power supply to +/-5V.
- 2) Set V_d and V_m to 0.0V using the trim pots.
- 3) Connect the LNA.
- 4) Set $V_d=0.05V$
- 5) Adjust V_g until I_d becomes 0mA (scaling of the monitoring point is 25mA/V). The ABLNAs have 4.3:1 voltage dividers on the gate, whereas the other LNAs had 10:1. V_g must not be greater than +/-3V, which should not be possible with this supply.
- 6) Set all voltages to 0V
- 7) Disconnect LNA

Power-up:

- 1) Connect the power supply to +/-5V.
- 2) Set V_{d1} and V_m to 0.0V using the trim pots.
- 3) Connect the LNA.
- 4) Set V_d to nominal value.
- 5) Set V_m to nominal value.
- 6) Set V_g to give nominal I_d .

Power-down:

- 1) Set V_m to 0V
- 2) Set V_d to 0V
- 3) Disconnect LNA.
- 4) Disconnect +/-5V

Below is the dual-amplifier power supply unit fabricated at Caltech. The supply voltages on the input D9 connector are +5V/-5V and GND. The marked ports are for monitoring. The ABLNA schematic is shown on the following page

Niklas:

300K:

- 1) Bring Vg to about 0.5V
- 2) Set Vd to 2.00V
- 3) Set Vm to -1.70V
- 4) Adjust Vg until Id=100mA

60K:

- 1) Bring Vg to about 0.5V
- 2) Set Vd to 1.40V
- 3) Set Vm to -1.00V
- 4) Adjust Vg until Id=50mA

Safe levels for the transistors are:

Vds<2V

-?<Vgs<0.7V

Vdg<2V

The question is how does this translate to safe voltage levels at the DC-pads (Vd, Vm, Vg).

I have a feeling that the start-up procedure can be simplified, and might even be unimportant, but this has to be checked. At room temperature Vdm=3.7V which is higher than the breakdown. These transistors can not pinch-off large Vds because of the short channel, so there will be a drain current flowing even when Vg=0V, which will cause a voltage drop in the drain and source resistors. Have a look at the attached IV, and schematic. I have noticed that the short channel effect is not as strong at cryogenic temperatures, which might be bad in this case.

I will have to measure IV of a transistor at 50K, and also check how it behaves at negative Vds before giving you a better answer. For now, stick to the safe procedure.

Hamdi:

Here is the procedure I was using (at Room Temperature) :

1. Connect ground + Vd +Vg
2. Connect Vm (Turn it ON)
3. Bring Vg to 0.5V
4. Bring Vd to 1V
5. Bring down Vm to -1V
6. Increase Vd to 2V
7. Decrease Vm to -1.7V
8. Adjust Vg to get about 100mA Id

The procedure but at 60K :

1. Bring Vg to 0.5V
2. Bring Vd to 1V
3. Bring down Vm to -1V
4. Increase Vd to 1.4V
5. Adjust Vg to get about 60mA Id (it varies from 40mA to 60mA to

get the minimum noise)

Subject: Re: PAX power

From: David DeBoer <ddeboer@seti.org>

Date: Fri, 03 Mar 2006 15:33:00 -0800

To: Robert Ackermann <robackrman@aol.com>

Hi Rob, Thanks for the reply -- I've been in a board meeting all day. I'll relabel that pin. The cable is about 10' long and is #24 shielded twisted pairs. Thanks, Dave

Robert Ackermann wrote:

Hi Dave,

This pinout looks good to me; however, please change label for pin 5 GND to "GNDsense." This ground will not carry significant current so that the voltage drop of the other common power supply grounds can be tracked.

Do you know approximately the length of the wires from the rim box to the PAX and has the gauge been selected?

Please make sure to note in the specification that the +5v (pin 15) comes from the PAX board, not the rim box. There will be 6 to 8 ADCs on the PAX board in addition to the special ADCs for the power detector. That is plenty, correct?

-Rob

>Hi Rob, I'm trying to resolve the issue with the PAX power
>wiring that you noticed and wanted to verify the scheme.

>The proper pinout for the input 15 pin should be?

```
>1  GND
>2  +5  OTXTEC
>3  GND
>4  +6  OTXlaser/PAM
>5  GND
>6  +6sense
>7  +5sense
>8  -5sense
>9  +5  OTXTEC
>10  GND
>11  -5  OTX/PAM
>12  GND
>--these three below would be for the possibility of bringing
>in a LM35 temperature sensor onto the PAX controller
>board, if you are set for it
>13  GND
>14  T
>15  +5

>Thanks,
>Dave
```

Subject: [ATAuser] Re: PAM power detector
From: "Gerald R. Harp" <gharp@seti.org>
Date: Tue, 28 Jun 2005 07:06:14 -0700
To: Robert Ackermann <robackrman@aol.com>
CC: ATA User <atauser@seti.org>

Just a reminder that we thought the power detector should be supported by an ADC with 14-16 bits. I can't quite remember the calculation, but I bet Mike does. The calibration source gives a signal of about 1 K, whereas the sky down to 500 MHz might be ~100 K. If we want amplitude calibration to 1%, then we need 10^4 dynamic range.

Or something like that,

Gerry

Hi Dave, It has been a while since I have heard anything about the PAM power detector. Has that been worked out? If so, where can I get info on its voltage output range and rough calibration? -Rob

--

=====
G. R. Harp, Ph.D. 2035 Landings Dr.
Sr. SW Scientist Mountain View, CA 94043
Allen Telescope Array (650)960-4576
SETI Institute
=====

ATAuser mailing list
ATAuser@seti.org
<http://mailman.seti.org/listinfo/atauser>

Subject: PAM detector

From: David DeBoer <ddeboer@seti.org>

Date: Tue, 28 Feb 2006 12:54:07 -0800

To: Robert Ackermann <robackrman@aol.com>

The PAM power detector is nominally centered at 2.5V ± 2V. Never below 0V and never above 5V.

In addition, I still have not received, although I have asked previously two or three times, the output voltage range for the PAM power detector. If this information is not immediately available, perhaps you can verify that it will never go negative?

Subject: Re: PAX card

From: Dave DeBoer <ddeboer@seti.org>

Date: Mon, 19 Dec 2005 21:19:21 -0800 (PST)

To: Robert Ackermann <robackrman@aol.com>

CC: "Gerald R. Harp" <gsharp@seti.org>, Jeff Kaufman <jeff@hcro.berkeley.edu>, Edward Fields <efields@uclink.berkeley.edu>

The laser TEC is wired separately -- we just have to bring it to the PAX, which we can do. We probably want a terminal block on the board to handle all of the input wires, and split them out from there (including the new rim-regulated flavors).

The laser (+5) draws $170\text{mA} \times 2 = 340\text{mA}$
laser TEC (+5) $532\text{mA} \times 2 = 1064\text{mA}$
otx general (-5) $200\text{mA} \times 2 = 400\text{mA}$

I'm actually not quite sure what the PAX ±5 draws. I've reattached the document. Rob -- you'll need another sense pair, won't you?

Thanks,
Dave

On Mon, 19 Dec 2005, Robert Ackermann wrote:

Thanks Rob, interesting idea. The regulation was there because of the thermal stability, which is primarily important for the LNA. The PAM and OTX should have stable power supplies as well, any variation in gain due to drift is indistinguishable from the signal of interest, which, as you know, is extraordinarily weak. Any idea how much variation we could see on the +5V (it doesn't matter on the -5V so much)?

OK, so we can move -5v regulation into the rim box with a sense wire return from the PAX.

I've cc'd Ed as well. Another idea would be to regulate □5 as you suggest, but also send +6V to a single regulator (maybe 2?) in the PAX for the +5 PAM and +5 laser (but not laser TEC)? You'd have to make another voltage flavor however, but now the important things are regulated within the PAX and the other things that draw most of the current (OTX TEC) are not.

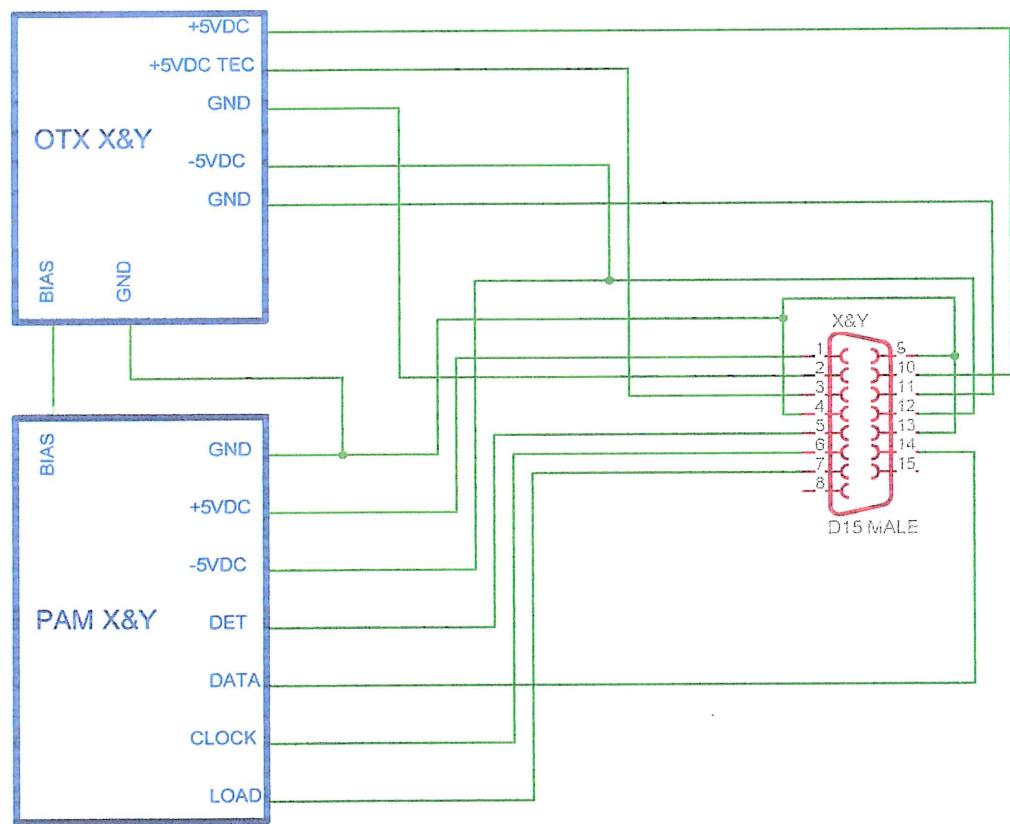
Is the laser TEC supply separate from the +5 laser supply? I don't remember that but that is probably just because that is how it is wired. Ed? I would like to pursue this too because it would move regulation of the large load to the rim box.

If we can't work this out through e-mail soon, perhaps we should have a meeting to spec this so I can get going on the rim box power supply and the PAX card. Also, we will change your pinout diagram (Dave) for PAX 15-pin D-sub connector.

-Rob

PAX Front Panel.doc

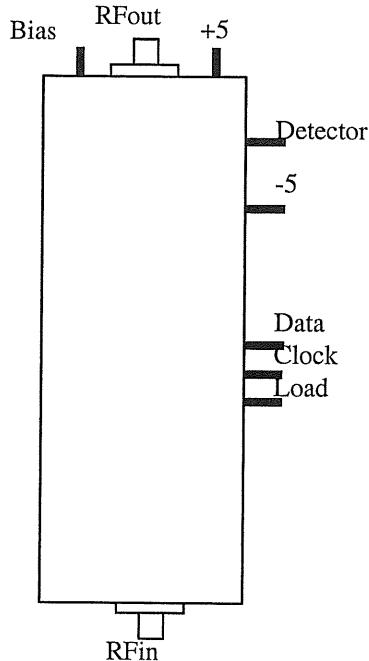
Content-Type: APPLICATION/octet-stream
Content-Encoding: BASE64



PAX Wiring

David DeBoer
June 6, 2003

PAM (all pins internal)



Bias	- brown wire from OTX + GND
+5	- red wire to pin _____ + GND
Det	- white to pin _____ + GND
-5	- blue wire to pin _____
Data	- white wire to pin _____
Clock	- yellow wire to pin _____
Load	- green wire to pin _____

OTX pairs (all pins internal, Black is ground)

- Brown/black – to PAM (bias wire)
Yellow/black – +5 from pin _____
Red/black – +5 from pin _____
Blue/black – -5 from pin _____
-

PIC

+5

Current power supply – January 2003 (Black is ground)

From external pins:

- White/black – -12 from pins 1/6
Orange/black – +6 from pins 2/7, 3/8, 4/9
-

To internal pins:

- Yellow/black – +5 to pin _____ (see yellow/black under OTX)
Red/black – +5 to pin _____ (see red/black under OTX)

Blue/black - -5 to pin _____ (see blue/black under OTX)

Wiring I'd want

To PAM

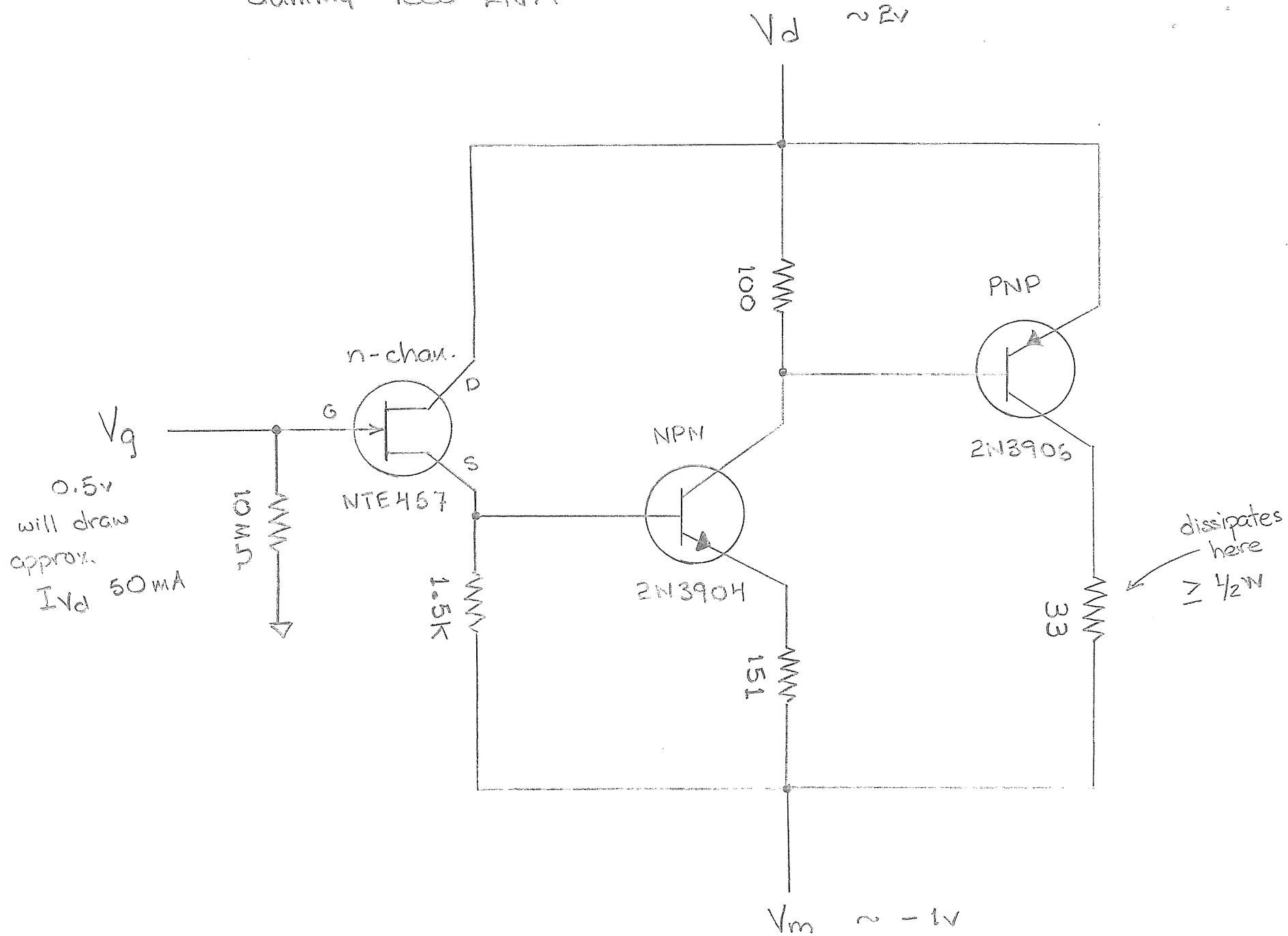
2 ×	1	Data	2
2 ×	2	Clock	2
2 ×	3	Load	2
1 ×	4	+5	1
1 ×	5	GND	1
1 ×	6	-5	1
0 ×	7	GND	0
2 ×	8	Detector	2
2 ×	9	GND	2

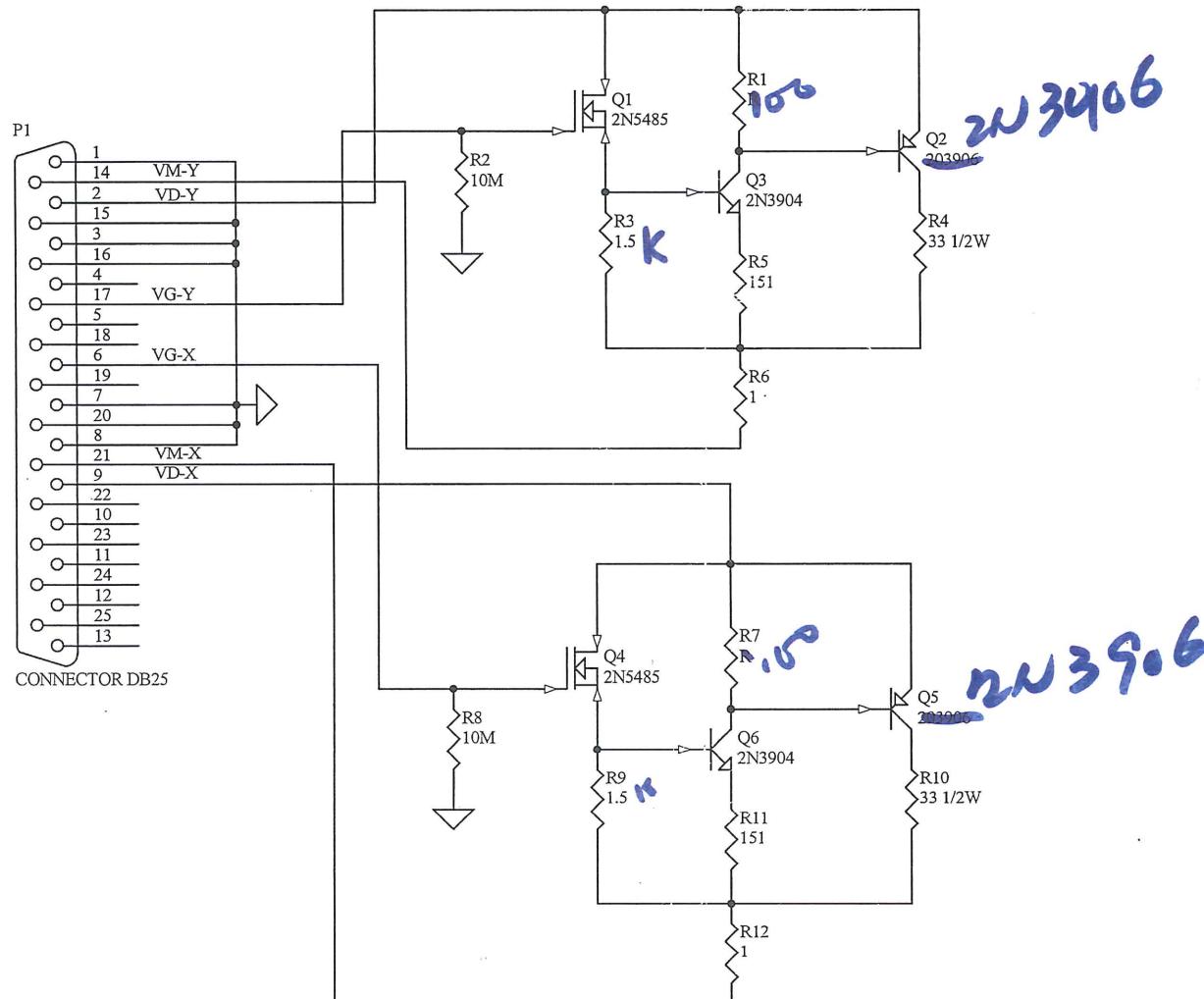
To OTX

1 ×	1	+5 TEC	1
1 ×	2	GND	1
1 ×	3	+5 laser	1
1 ×	4	GND	1
0 ×	5	-5	0
0 ×	6	GND	0

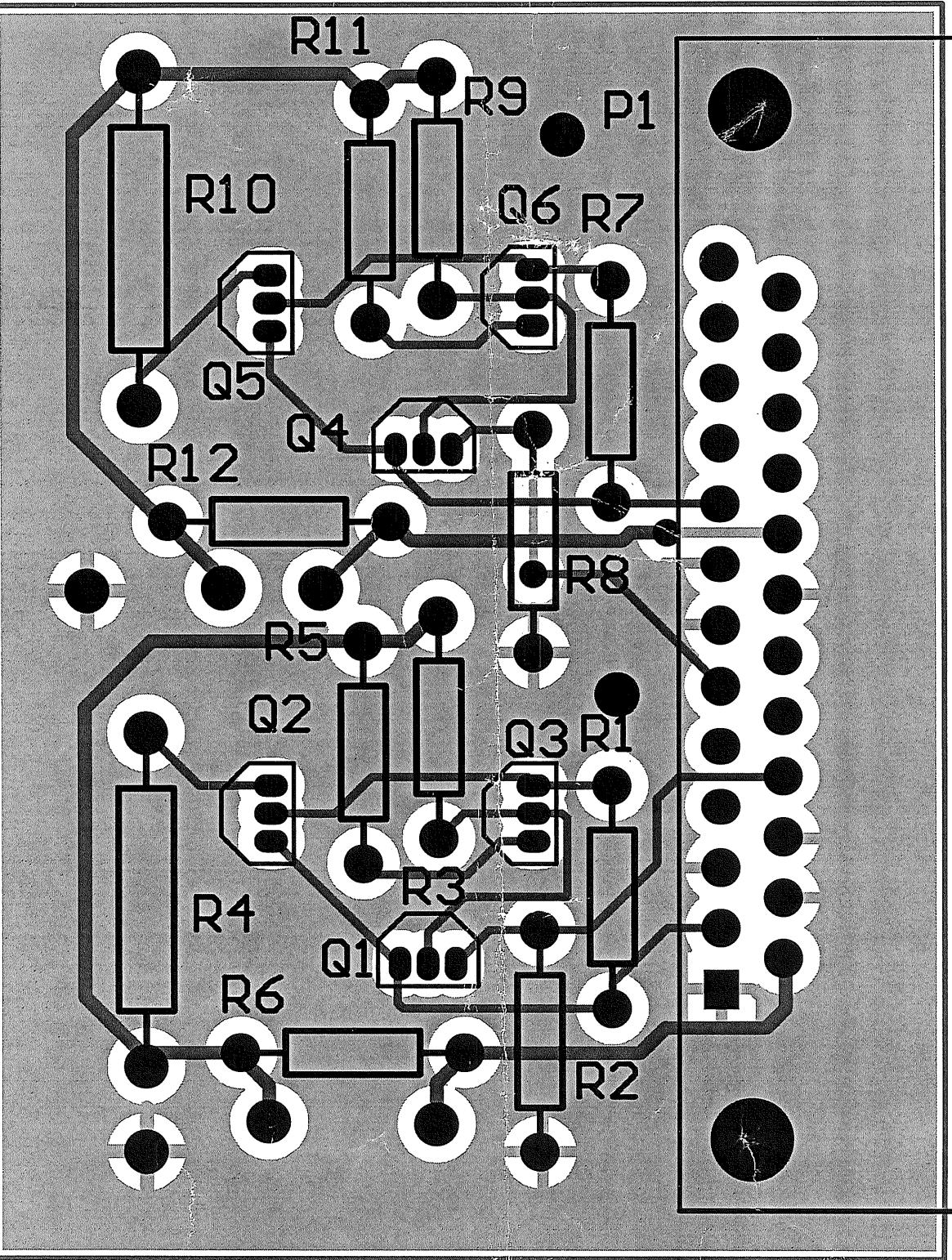
To Output

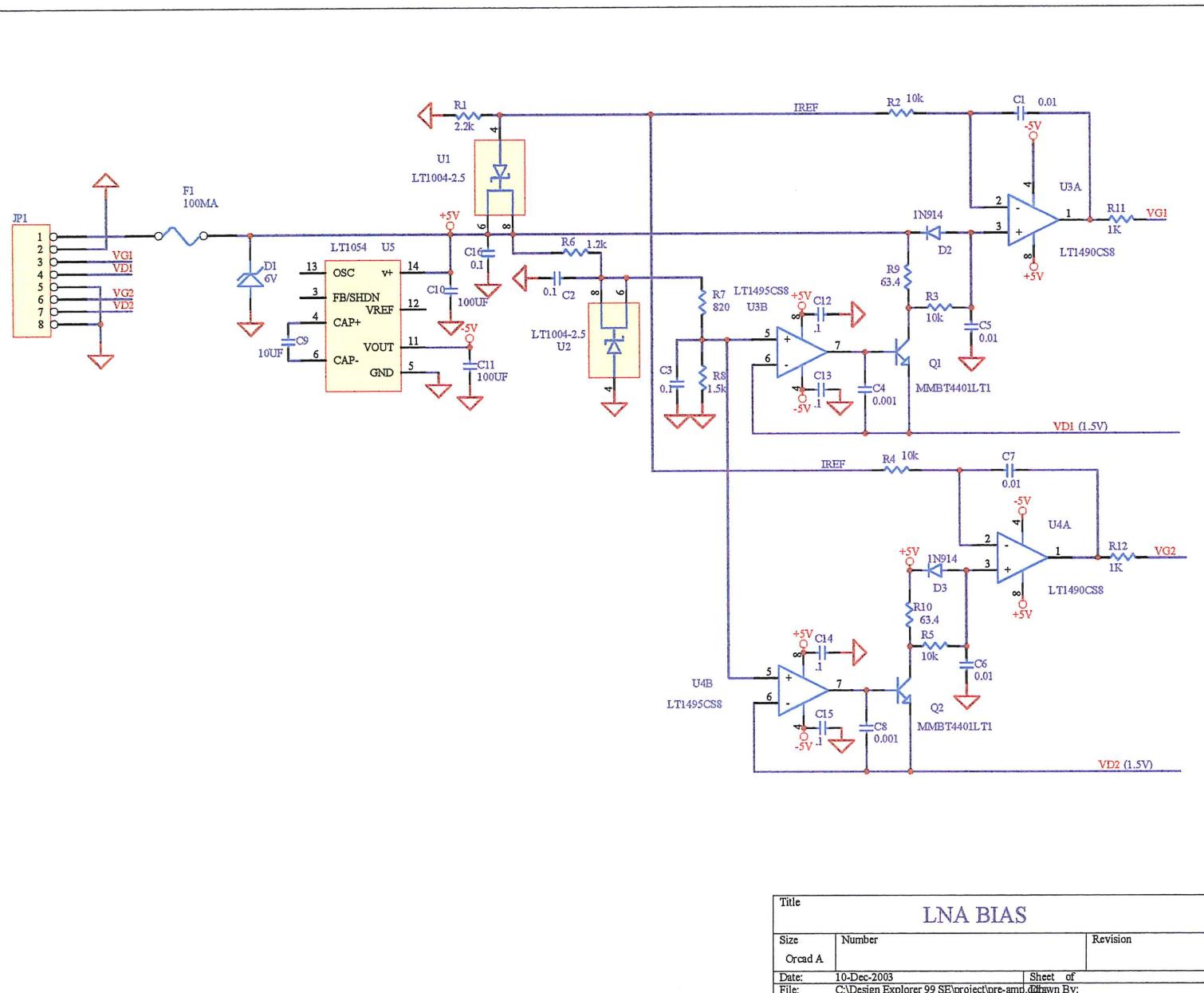
"dummy" feed LNA





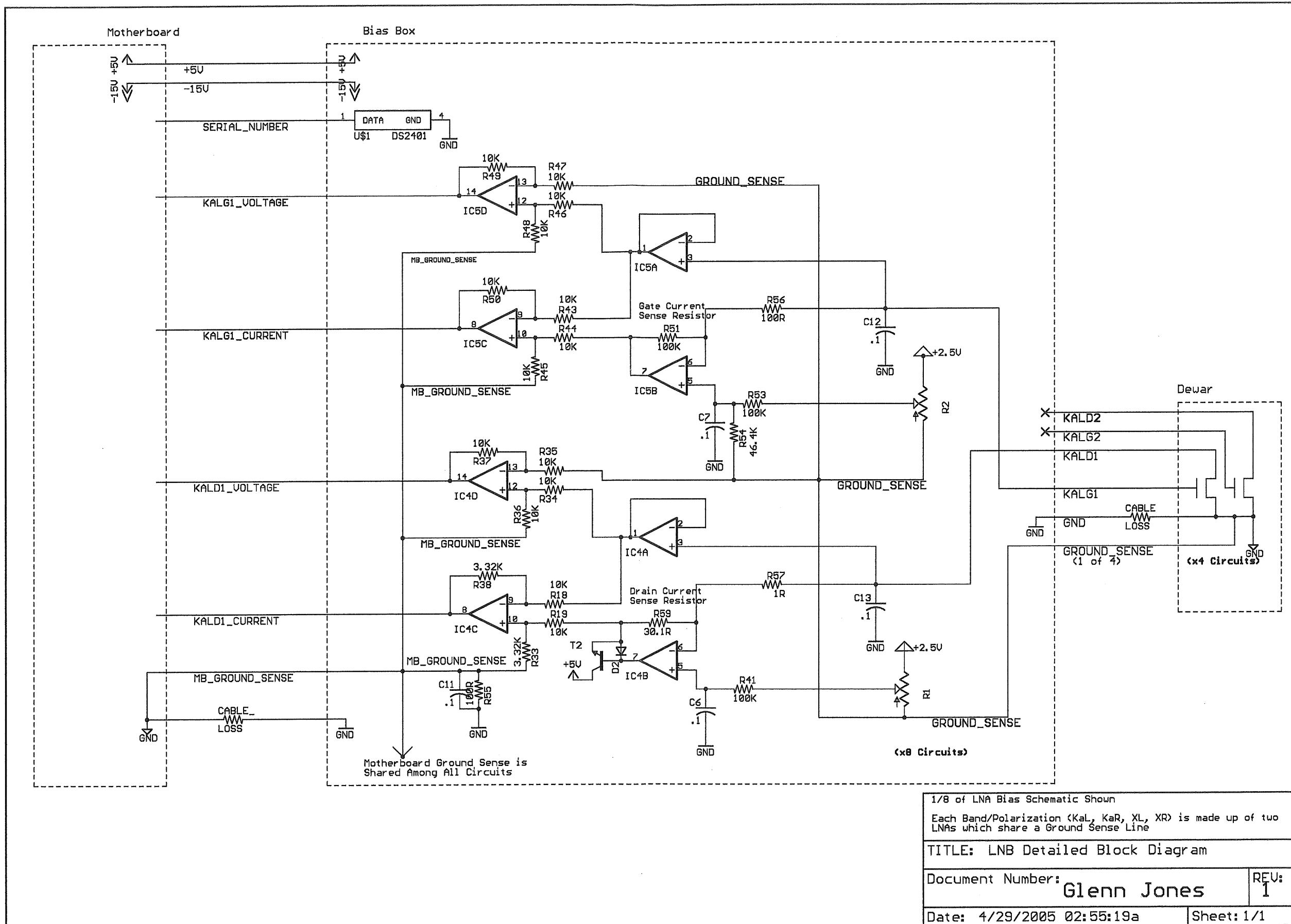
Title "DUMMY" FEED LNA		
Size A	Number 1030	Revision
Date: 4/28/2006	Sheet of	
File: F:\WorkFiles\pcbwork\1030.SchDoc		Drawn By:





Title LNA BIAS		
Size Orcad A	Number	Revision
Date: 10-Dec-2003		Sheet of
File: C:\Design Explorer 99 SE\project\pre-amp.dwg		drawn By:

20

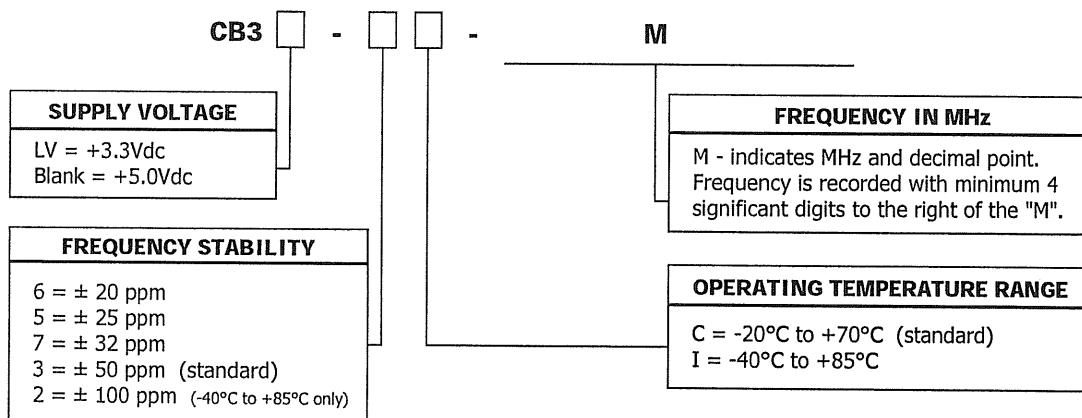


FEATURES

- Standard 7.5x5mm Surface Mount Footprint
- CMOS/TTL Compatible
- Frequency Range 1.5 – 160 MHz
- Frequency Stability, ± 50 ppm Standard
(± 25 ppm and ± 20 ppm available)
- +3.3Vdc or +5.0Vdc Operation
- Operating Temperature to -40°C to $+85^{\circ}\text{C}$
- Output Enable Standard
- Tape & Reel Packaging
- RoHS Compliant

DESCRIPTION

The CB3/CB3LV is a ceramic packaged Clock oscillator offering reduced size and enhanced stability. The small size means it is perfect for any application. The enhanced stability means it is the perfect choice for today's communications applications that require tight frequency control.

**ORDERING INFORMATION**

Example Part Number: CB3LV-3C-32M7680 or CB3-3I-32M7680

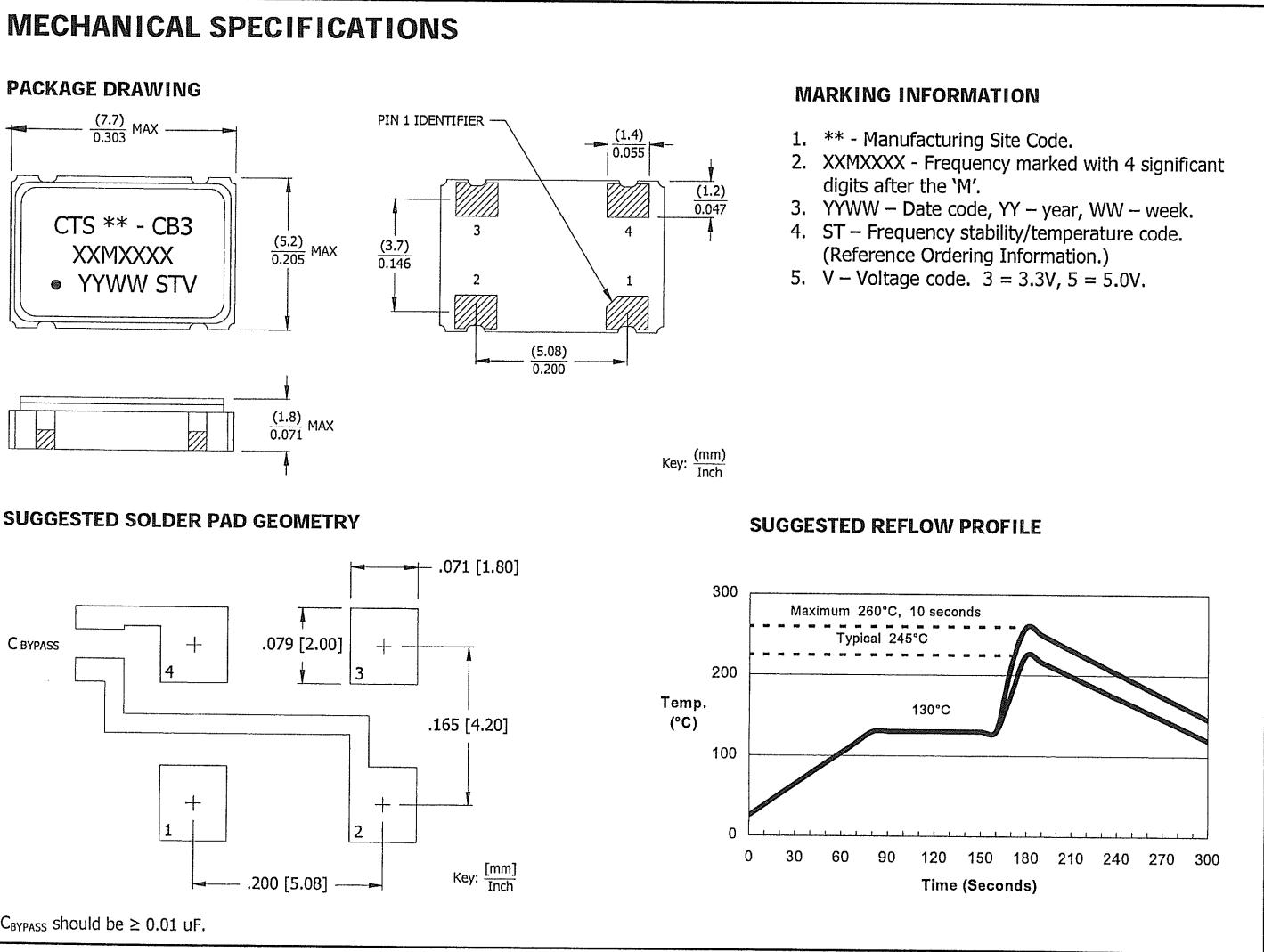
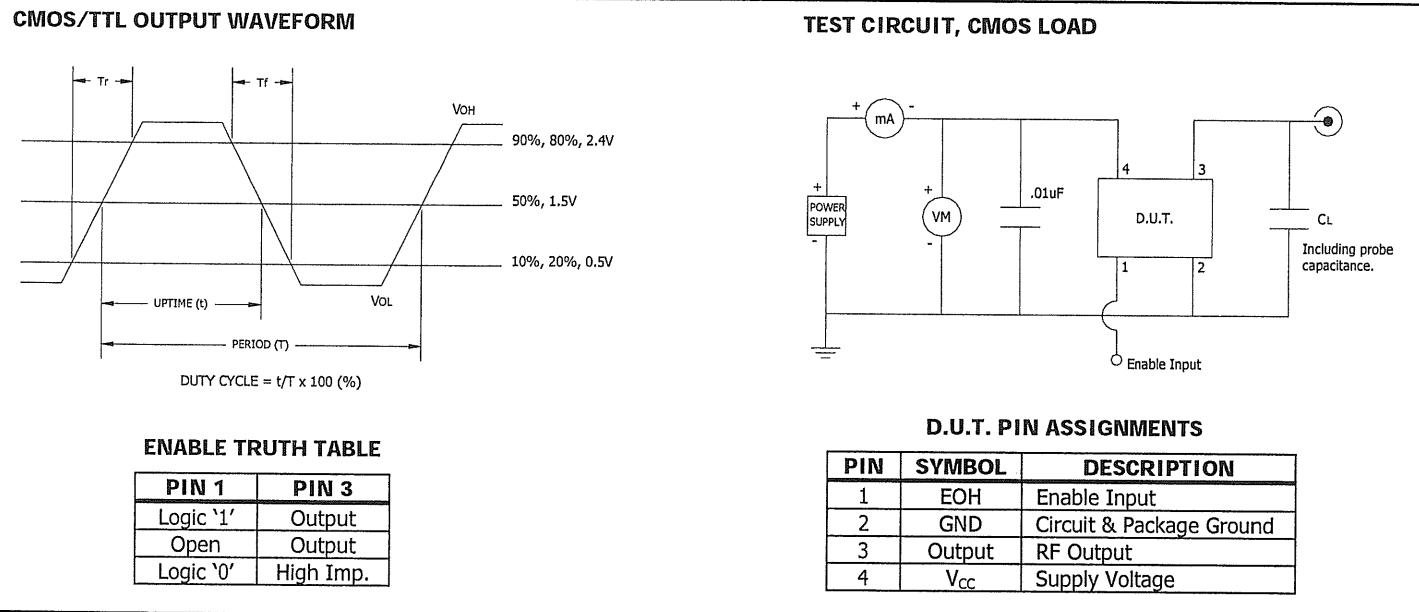
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Maximums	Maximum Supply Voltage	V _{CC}	-	-0.5	-	V
	Storage Temperature	T _{STG}	-	-55	-	°C
	Frequency Range	f ₀	-	1.5	-	MHz
	Frequency Stability (See Note 1 and Ordering Information)	Δf/f ₀	-	-	20,25,32, 50 or 100	± ppm
	Operating Temperature Commercial	T _A	-	-20	-	°C
	Industrial		-40	25	70	
	Supply Voltage CB3	V _{CC}	± 10 %	4.5	5.0	V
	CB3LV			3.0	3.3	5.5
	Supply Current CB3	I _{CC}	1.5 MHz to 20 MHz C _L =50pF	-	10	25
			20.1 MHz to 80 MHz C _L =50pF	-	30	50
Electrical and Waveform Parameters			80.1 MHz to 160 MHz C _L =15pF	-	40	100
	CB3LV		1.5 MHz to 20 MHz C _L =15pF	-	7	12
			20.1 MHz to 80 MHz C _L =15pF	-	20	40
			80.1 MHz to 160 MHz C _L =15pF	-	30	60
	Output Load	C _L	1.5 MHz to 50 MHz 50.1 MHz to 80 MHz 80.1 MHz to 160 MHz	-	-	pF
				-	-	50
				-	-	30
				-	-	15
	Output Voltage Levels Logic '1' Level	V _{OH}	CMOS Load 10 TTL LOAD	V _{CC} - 0.5V V _{CC} - 0.6V	-	-
	Logic '0' Level	V _{OL}	CMOS or TTL Load	-	-	0.4
Output Current Logic '1' Level	I _{OH}	V _{OH} = 3.9V/2.2V	V _{CC} = 4.5V/3.0V	-	-	-16/-8
	I _{OL}	V _{OL} = 0.4V	V _{CC} = 4.5V/3.0V	-	-	+16/+8
	Output Duty Cycle	SYM	@ 50% Level	45	-	%
	Rise and Fall Time CB3	T _R , T _F	@ 10% - 90% Levels 1.5 MHz to 20 MHz C _L =50pF	-	8	10
			20.1 MHz to 80 MHz C _L =50pF	-	4	8
			80.1 MHz to 160 MHz C _L =15pF	-	2.5	5
	CB3LV		1.5 MHz to 20 MHz C _L =15pF	-	6	8
			20.1 MHz to 80 MHz C _L =15pF	-	3	4
			80.1 MHz to 160 MHz C _L =15pF	-	1.5	3
	Start Up Time	T _S	Application of V _{CC}	-	-	ms
Enable Function (See Note 2)	V _{IH}	Pin 1 Logic '1', Output Enabled	2	-	-	V
	V _{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.8	
	Enable Time CB3	T _{PLZ}	Pin 1 Logic '1'	-	-	ns
	CB3LV			-	-	ms
Phase Jitter	t _{jms}	Bandwidth 12 KHz - 20 MHz	-	< 1	-	ps RMS

Notes:

1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and first year aging at an average operating temperature of +40 °C.

2. Reference CTS Application Note 014-0002-0.



Single-Ended, Rail-to-Rail I/O, Low Gain PGA

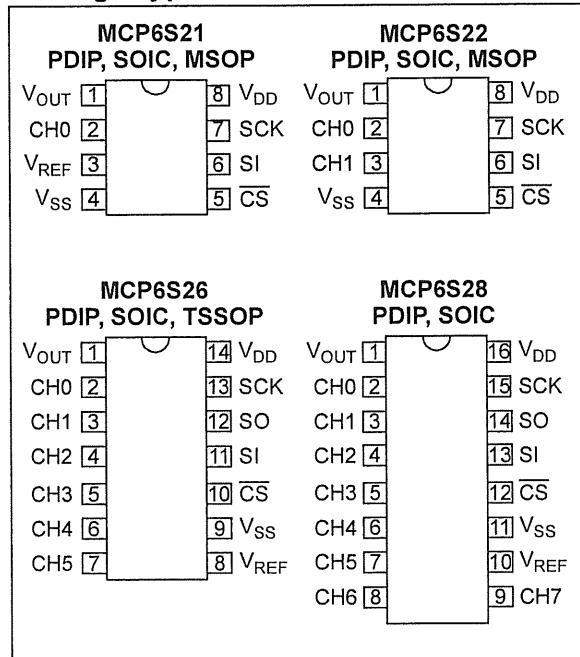
Features

- Multiplexed Inputs: 1, 2, 6 or 8 channels
- 8 Gain Selections:
 - +1, +2, +4, +5, +8, +10, +16 or +32 V/V
- Serial Peripheral Interface (SPI™)
- Rail-to-Rail Input and Output
- Low Gain Error: $\pm 1\%$ (max)
- Low Offset: $\pm 275 \mu V$ (max)
- High Bandwidth: 2 to 12 MHz (typ)
- Low Noise: 10 nV/V/Hz @ 10 kHz (typ)
- Low Supply Current: 1.0 mA (typ)
- Single Supply: 2.5V to 5.5V

Typical Applications

- A/D Converter Driver
- Multiplexed Analog Applications
- Data Acquisition
- Industrial Instrumentation
- Test Equipment
- Medical Instrumentation

Package Types

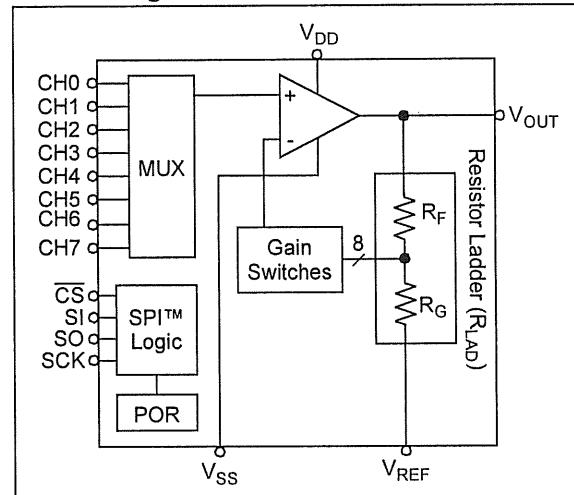


Description

The Microchip Technology Inc. MCP6S21/2/6/8 are analog Programmable Gain Amplifiers (PGA). They can be configured for gains from +1 V/V to +32 V/V and the input multiplexer can select one of up to eight channels through an SPI port. The serial interface can also put the PGA into shutdown to conserve power. These PGAs are optimized for high speed, low offset voltage and single-supply operation with rail-to-rail input and output capability. These specifications support single supply applications needing flexible performance or multiple inputs.

The one channel MCP6S21 and the two channel MCP6S22 are available in 8-pin PDIP, SOIC and MSOP packages. The six channel MCP6S26 is available in 14-pin PDIP, SOIC and TSSOP packages. The eight channel MCP6S28 is available in 16-pin PDIP and SOIC packages. All parts are fully specified from -40°C to +85°C.

Block Diagram



Ultra-low-noise low-dropout regulator achieves $6\text{-nV}/\sqrt{\text{Hz}}$ noise floor

Ken Yang, Maxim Integrated Products Inc, Sunnyvale, CA



Many low-dropout-voltage regulators see service in electronic systems, but relatively few are designed for low-noise operation. (For example,

Maxim's MAX8887 achieves a noise voltage of approximately $42\text{ }\mu\text{V}$ rms. However, certain applications, such as ultra-low-noise instrumentation oscil-

lators, demand even lower levels of power-supply noise. To reach this level, the circuit in Figure 1 combines low-noise components and extra filtering to achieve an output noise floor of only $6\text{ nV}/\sqrt{\text{Hz}}$.

Voltage reference IC_1 , a Maxim MAX6126, features low output noise. Lowpass filter $R_1\text{-}C_1$ further reduces this noise by attenuating noise frequencies

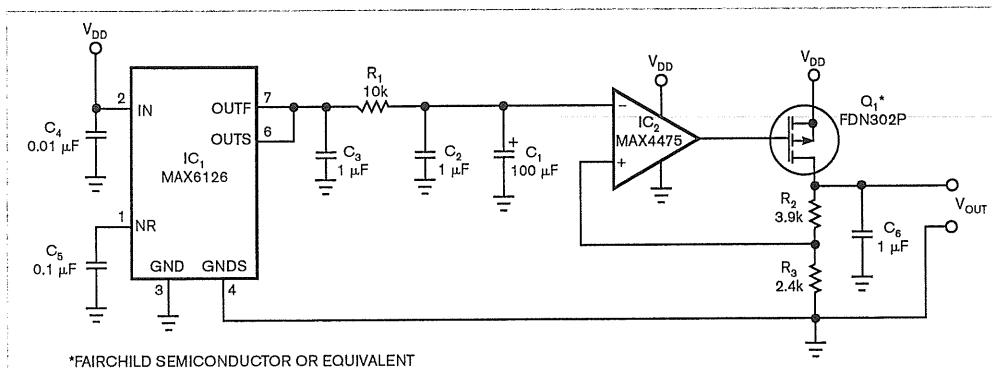


Figure 1 This low-dropout-voltage regulator features a noise floor of only $6 \text{ nV}/\sqrt{\text{Hz}}$, making it an ideal power source for low-noise oscillators.

above IC_1 's 0.16-Hz cutoff frequency. The filtered reference voltage drives the inverting terminal of error amplifier IC_2 , a Maxim MAX4475, which regulates the output voltage by means of Q_1 , a P-channel power FET source follower. Feedback resistors R_2 and R_3 determine the output voltage as follows: $R_2 = R_3[(V_{\text{OUT}}/2.048\text{V}) - 1]$.

The simplified noise-analysis diagram illustrates the components' noise contributions (Figure 2). Lowpass filter R_1 -

C_1 attenuates high-frequency noise on the voltage reference's output. The op amp's noise current, $0.5 \text{ fA}/\sqrt{\text{Hz}}$, is negligible with respect to its voltage noise, $4.5 \text{ nV}/\sqrt{\text{Hz}}$. The reference-noise source adds to the op-amp voltage noise because they effectively connect in series. The MOSFET's noise contribution appears at Q_1 's input.

The noise at IC_2 's inverting terminal equals the noise at its noninverting terminal:

$$V_{\text{N_REF}}H(f) + V_{\text{N_OPAMP}} = V_{\text{N_OUT}}\left(\frac{R_3}{R_2 + R_3}\right),$$

and

$$V_{\text{N_OUT}} = \left(V_{\text{N_REF}}H(f) + V_{\text{N_OPAMP}}\right)\left(\frac{R_2 + R_3}{R_3}\right),$$

dropout circuit's output noise comprises only the op amp's noise multiplied by the closed-loop gain. The feedback loop suppresses $V_{\text{N_FET}}$, the MOSFET's noise contribution, which therefore can't contribute to the output noise. For frequencies within the loop's bandwidth, the low-dropout circuit also rejects ripple and noise voltages that the power supply introduces.

Figure 3 shows a plot of noise density versus frequency for the circuit of Figure 1, which exhibits a noise floor of about $6 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz. For comparison, the plot shows the noise-measurement instrument's noise floor and a typical low-dropout circuit's much higher noise density—for example, $500 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz for the MAX8887 low-noise, low-dropout circuit. EDN

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You can post a comment to any of these Design Ideas by visiting their online versions and clicking on Feedback Loop.

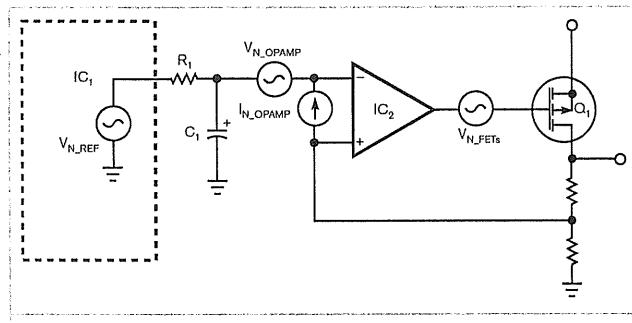


Figure 2 This simplified version of Figure 1 highlights noise sources for analysis.

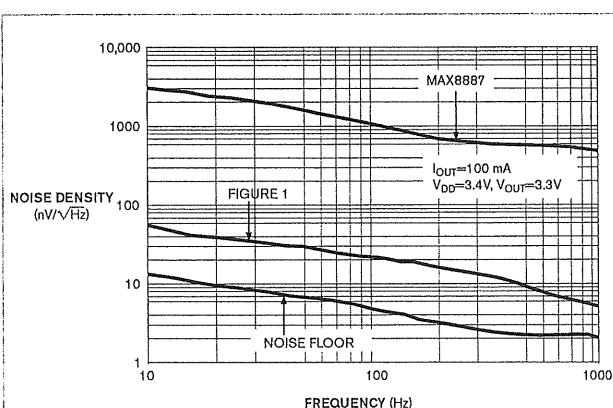


Figure 3 A noise-density-versus-frequency plot for the low-dropout circuit in Figure 1 is 38 dB lower than that of a conventional low-noise, low-dropout-voltage regulator—in this case, a Maxim MAX8887.

Noise testing of the active and passive baluns for the ATA

N. Wadefalk and S. Weinreb

September 7, 2004

The ATA Low Noise Amplifier is connected to the feed with a quartz balun [1,2]. The balun converts the balanced signal from the feed to an unbalanced signal, which allows us to use a conventional single-ended LNA. This report describes noise testing of the quartz balun connected to the single-ended LNA (WBA13). The result is compared with similar tests of an active balun (WBAL2). Gain and noise have been tested for both these cases using a 200 ohm Variable Temperature Load (VTL) at 300, 77 and 12 Kelvin physical temperature. The result of two different baluns is also compared; one made on very low loss fused quartz, and the other on high thermal conductivity crystal quartz.

1. The test set-up

To be able to measure the noise of the balun and LNA we must inject a noise signal on the input of the DUT. Since the input is balanced and of a non-standard impedance, no commercial noise sources are available. To overcome this problem we had to design our own noise generator. This noise source is a 200 ohm thin film resistor on a 12*7.5 mm crystal quartz substrate (Fig 1). There are ultrasonically drilled holes through the substrate for a 200 ohm twin lead line to be connected to the resistor. The other end of the twin lead line goes to the DUT. For room temperature measurements, this resistor can be dipped in liquid nitrogen to change its temperature (noise power). At cryogenic temperatures however,

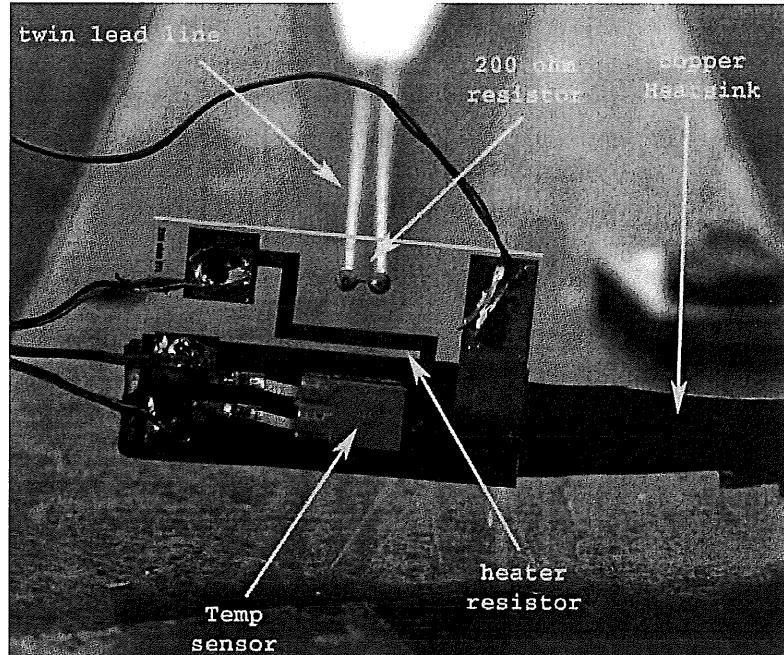


Fig 1. The 200 ohm VTL.

the temperature has to be changed by other means, and therefore there's also a heater resistor and a pad for a temperature sensor on the substrate. At low temperatures the thermal conductivity of crystal quartz is very high, which should make the temperature distribution along the substrate very uniform; i.e the sensor should measure the actual temperature of the 200 ohm resistor, even though it is not mounted on the resistor itself.

The VTL circuit was processed on 5 and 20 mil thick crystal quartz. The part of the twin lead line that goes through the substrate will have much lower characteristic impedance than the nominal 200 ohms, and therefore it is important to keep the substrate as thin as possible. This mismatch should give a ripple

in the measurement result as the impedance presented to the DUT varies around its nominal value. Simulations show that this ripple will be small even with the 20 mil substrate, and since it is more robust than the 5 mil one, all measurements in this report were done using the thicker substrate, except the room temperature measurements which used a special circuit with only the 200 ohm resistor on a 5 mils substrate. Figure 2 shows the VTL circuit connected to a 200 ohm, 2" long twin lead line followed by the balun and the LNA. The twin lead line consists of two 0.014" diameter silver plated stainless steel tubes.

2. Measurement results

The measurements were done at 300, 77 and 12 K physical temperature. The 12 K experiments were done in a large cryobox equipped with a CTI 350 cryocooler, while the 77 K measurements took place in a small Infrared Labs liquid nitrogen dewar. The 12 K dewar has a radiation shield with a temperature of 90 K, and the 77 K dewar has a 77 K radiation shield. However, where the balun sits in the 77 K dewar, there is an opening in the radiation shield and therefore it will "see" the 300 K walls surrounding it. Since the ATA dewar has a radiation shield that is at the same temperature as the balun, a copper foil enclosure were built for the balun to simulate the situation in the ATA dewar. Figure 3 shows the measurement set-up with this enclosure.

The active balun MMIC was mounted on a small copper plate together with the necessary external components (input matching network, biasing components, etc). The fact that there is no cover over the MMIC makes it sensitive to where it is located in the dewars. If it is surrounded by metal, feedback from output to input via a waveguide mode can cause gain peaks and in worst case oscillations. Normally high gain MMICs are mounted in a narrow cut-off cavity to avoid such problems, but as a first test the flat copper plate is sufficient (Fig 7). The result at 300, 77 and 12 K are presented in Fig 4-6 respectively, and the bias settings in Table 1. The graphs also include simulation results for the LNAs. This curve applies to both the single-ended LNA and the active balun, since theoretically they should have the same noise.

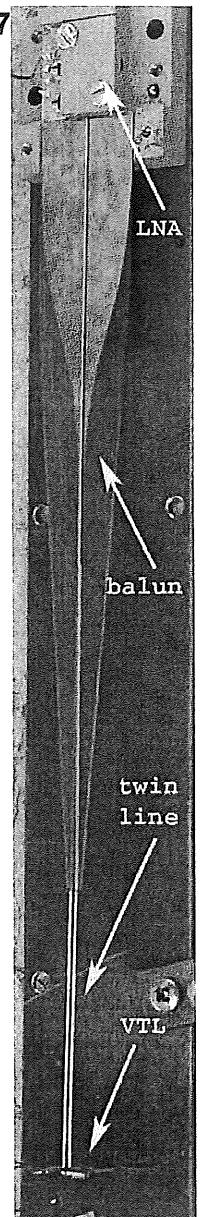


Fig 2. Test set-up with VTL, balun and LNA

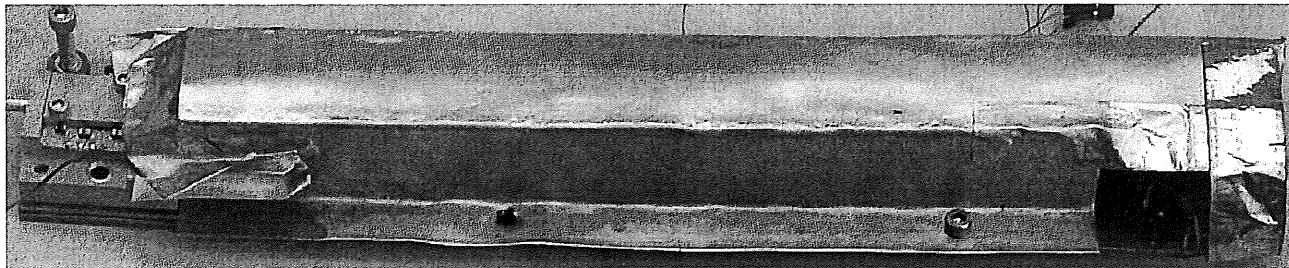


Fig 3. Same test set-up as in Fig 2, but with the shield.

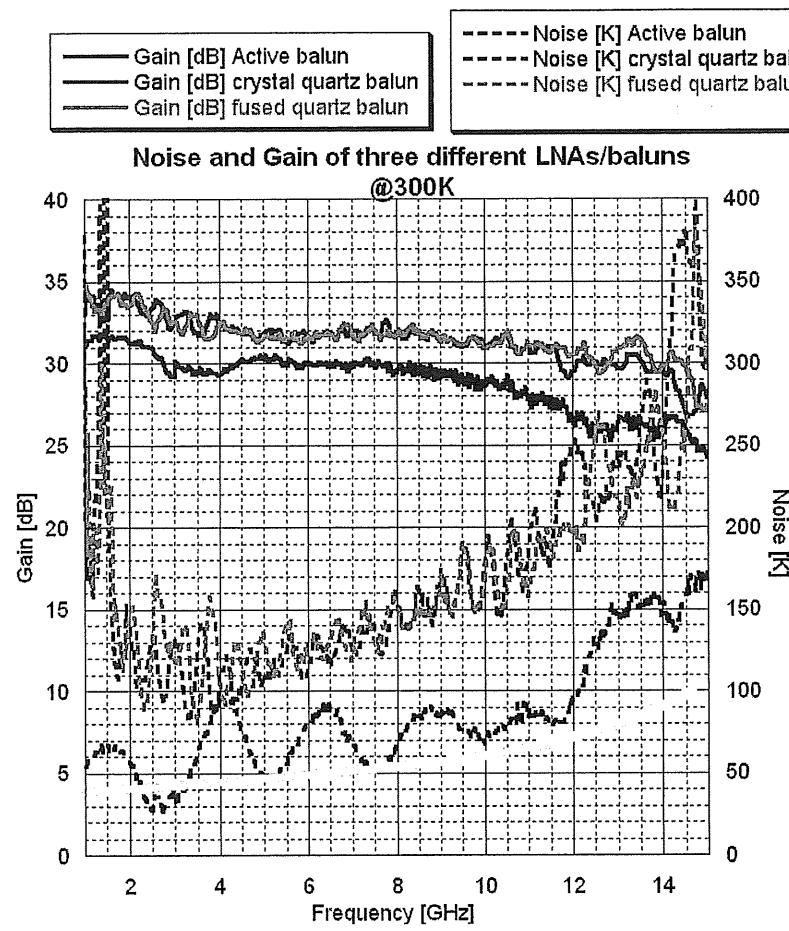


Fig 4. Test result at 300 K

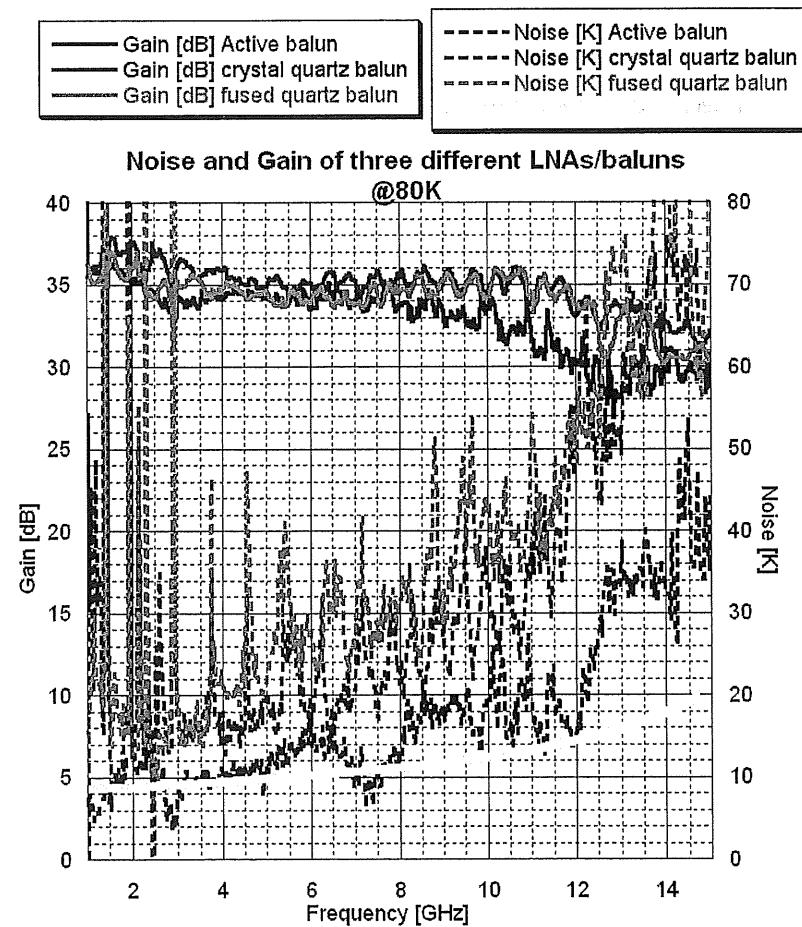


Fig 5. Test result at 80K

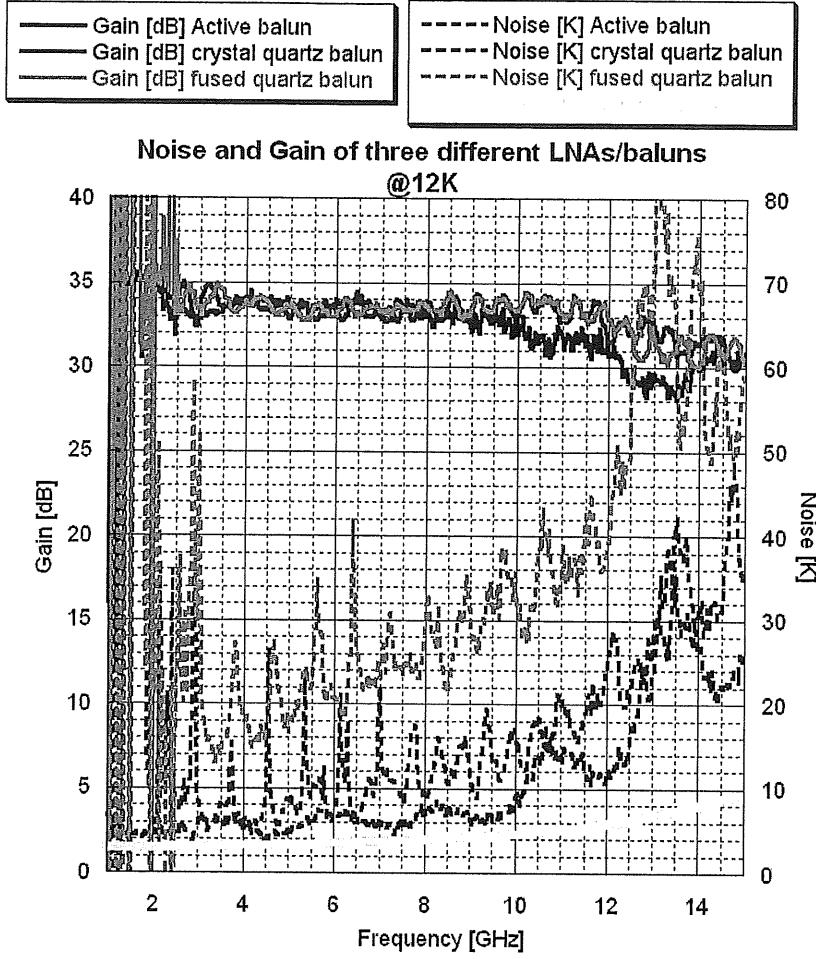


Fig 6. Test result at 12 K

All measurements are referenced to the 200 ohm resistor side of the twin lead line, i.e no compensation was done for losses in the 2" long line. One important piece of information is missing in the three noise graphs, namely the measured noise of the single-ended LNA. Unfortunately, for the moment we have no way of measuring this LNA, which has a 100 ohm microstrip input, at cryogenic temperature; however it has been measured at room temperature with very good agreement with simulations. Further, a coaxial 50 ohm module using the same MMIC has been measured at all three temperatures with equally good agreement with simulations. We believe that the maximum error of the simulated performance indicated in Fig 4-6 is less than 30% for WBA13.

	Vd [V]	Id [mA]	Vg [V]	V- [V]	I- [mA]	Pdc [mW]
Active balun @300K	1.80	100	0.132	-1.50	-50	255
Active balun @77K	1.60	74	0.155	-1.20	-40	166
Active balun @12K	1.40	64	0.180	-0.85	-31	116
Single ended LNA @300K	1.80	50	-0.077	n/a	n/a	90
Single ended LNA @77K	1.50	40	+0.082	n/a	n/a	60
Single ended LNA @12K	1.20	20	+0.025	n/a	n/a	24

Table 1. Bias conditions of the two LNAs at 300,77 and 12 K.

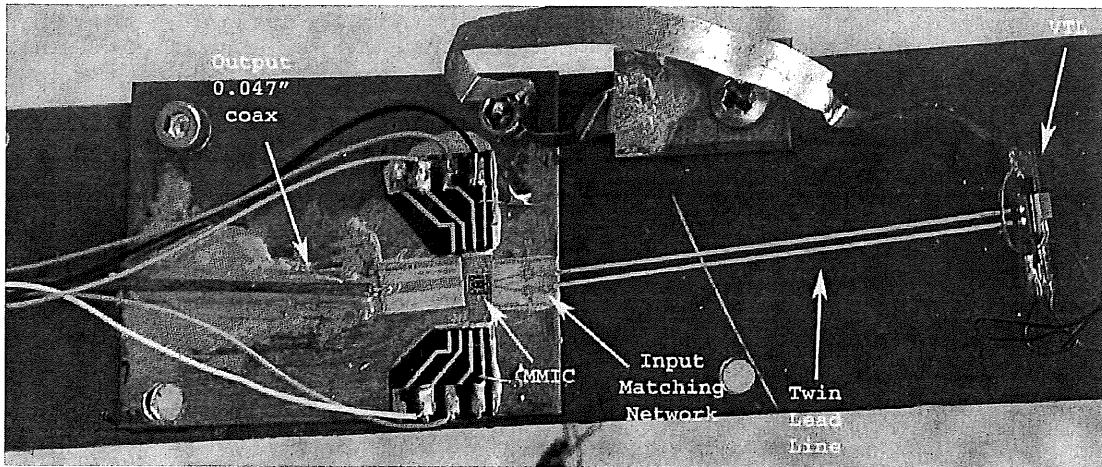


Fig 7. Close-up of the active balun on a copper plate

3. Discussion

The room temperature measurements were done without the copper shield and with ground as far away as practically possible. As can be seen in Fig 4, there's a large ripple in the noise of both the active and passive baluns. The period of 2.5 GHz for the active balun ripple, suggests a separation between two discontinuities of about 60 mm in air, which is approximately the distance between the 200 ohm source and the input of the MMIC. The 600 MHz period ripple of the passive balun is what we would expect if the reflections occurred at the 200 ohm resistor and the input of the LNA, under the condition that the signal travels in the twin lead line and then the intended way in the quartz substrate. The average effective dielectric constant of the balun is about 2.6 and the length about 125 mm. The cause of this ripple is unknown. Measurements of the return loss, looking into the balun's unbalanced end with the 200 ohm VTL connected to the balanced side, show better than 15 dB across the entire band. This is with good agreement with simulations. The amplifiers should be very well matched on the input for frequencies higher than 4 GHz. If the ripple in noise was caused by a mismatch we would expect to see a large ripple in the gain as well. Figure 4 shows a very smooth gain curve, at least for the active balun.

One of the concerns with the passive balun is the possible excitation of even modes when located in a grounded enclosure [3]. This mode will be badly matched at the ends of the copper shield and will therefore form a resonant cavity. As can be seen in figure 5-6, sharp peaks in noise appear on top of the ripple we saw in the room temperature measurements. The peaks appear at the same frequencies with and without the shield, but they are sharper and larger in magnitude with the shield. Without the shield, the balun will still be enclosed in a grounded cavity, but the distance to the top cover of the 90 K shield is about 100 mm compared to about 10 mm with the copper shield on. It is also worth noting that the sharp peaks can not easily be distinguished in the gain curves, which suggests that a simple transmission measurement through a balun might not reveal the problem. The situation in the ATA dewar is quite different since the narrow end of the radiation shield is open which allows a possible even mode to

radiate. The copper shield used in these measurements is closed in both ends and the even mode will be badly matched in both ends.

If the increase in measured noise caused by adding the balun between the LNA and the 200 ohm source, is considered to be of thermal nature, the loss of the balun can be calculated using Equation 1.

$$L_b = \frac{T_{tot} + T_b}{T_b + T_{LNA}}$$

Eq 1. Expression for balun loss, where L_b =loss of balun, T_{tot} = total measured noise temperature, T_b =physical temperature of balun, T_{LNA} =noise temperature of LNA

Figure 8 shows the result of Equation 1 applied to Figure 4-6. Since we have no noise measurements of the single-ended LNA except for at room temperature, the simulated noise of the LNA was used. The physical temperature of the balun was measured by gluing a Lakeshore silicon diode temperature sensor to the tip of the balun using cyanoacrylate. The temperature of the LNA side of the balun was measured by screwing a sensor to the LNA body. Cyanoacrylate has low thermal conductivity but also low viscosity, so a very thin layer can be applied and therefore the temperature gradient should be very small. The average balun temperature was used in Equation 1.

The loss of the balun at room temperature is mostly due to the finite conductivity of the conductor metal, and the loss of 1 dB at 11 GHz is close to what we would expect. At cryogenic temperatures the conductivity of the top gold layer should increase by a factor of about 8 at 77K and up to several thousand at 12 K and therefore we would expect a large decrease in balun loss. As can be seen in figure 8, the balun loss seems to be quite constant down to 77K and at lower temperatures it even increases. At low temperatures, especially below 70K, the conductivity of metals is very dependent on their purity. To check for this, the DC-resistance of the top trace of the balun was measured at 300K and with the balun immersed in liquid nitrogen. The result is presented in Table 2 together with a reference measurement of a 100 ohm line on Duroid 6002, with 17 μm copper and 5 μm electroplated gold.

	@300 K	@77 K	@12 K
Temperature of crystal quartz balun base	300 K	79.50 K	13.35 K
Temperature of crystal quartz balun tip	300 K	85.50 K	16.65 K
Temperature of fused quartz balun base	300 K	79.30 K	13.35 K
Temperature of fused quartz balun tip	300 K	120 K	69.50 K
Resistance of crystal quartz top trace	2.36 Ω	0.49 Ω	-
Resistance of fused quartz top trace	3.68 Ω	1.07 Ω	-
Resistance of a 100 ohm line on 20 mil Duroid 6002	44 m Ω	5.8 m Ω	-

Table 2. Measurement results of the two baluns related to thermal and electrical conductivity.

The metal stack-up of the crystal quartz balun starting from the bottom layer is 0.1 μm Ti, 2.5 μm Cu, 1 μm Ni and 0.5 μm Au. The fused quartz balun has only Au on Ti of unknown thicknesses. The DC-measurement of the crystal quartz balun does not say much about its microwave loss, because of its multilayer structure. The fused quartz balun only has one layer of high conductivity metal and it should

therefore be safe to say that the change in conductivity between 300 and 77K in Table 2 is in the gold layer. It drops with a factor of 3.4 which should be compared with the theoretical value of 8. This indicates that the gold is not of high purity. Processing the substrates at very high temperatures can make the underlying metal to diffuse into the gold. The gold on both baluns looks very shiny which is not typical for pure gold. The crystal quartz balun used in these experiments even has areas where the top metal is nickel colored. It is not likely that poor metallization alone explains the higher-than-expected noise. This poses the question whether the measurements are correct or not. There's no easy way to check the accuracy of this completely new type of noise measurement system. The fact that the measurements of the active balun is quite close to simulations is a strong indication that the noise measurement system is working and that it gives results that are close to the truth. Repeatability was very good and therefore the noise system should be an accurate tool to compare the different cases. Future measurements will give us more experience with the system and then we will be able to tell more about the absolute accuracy.

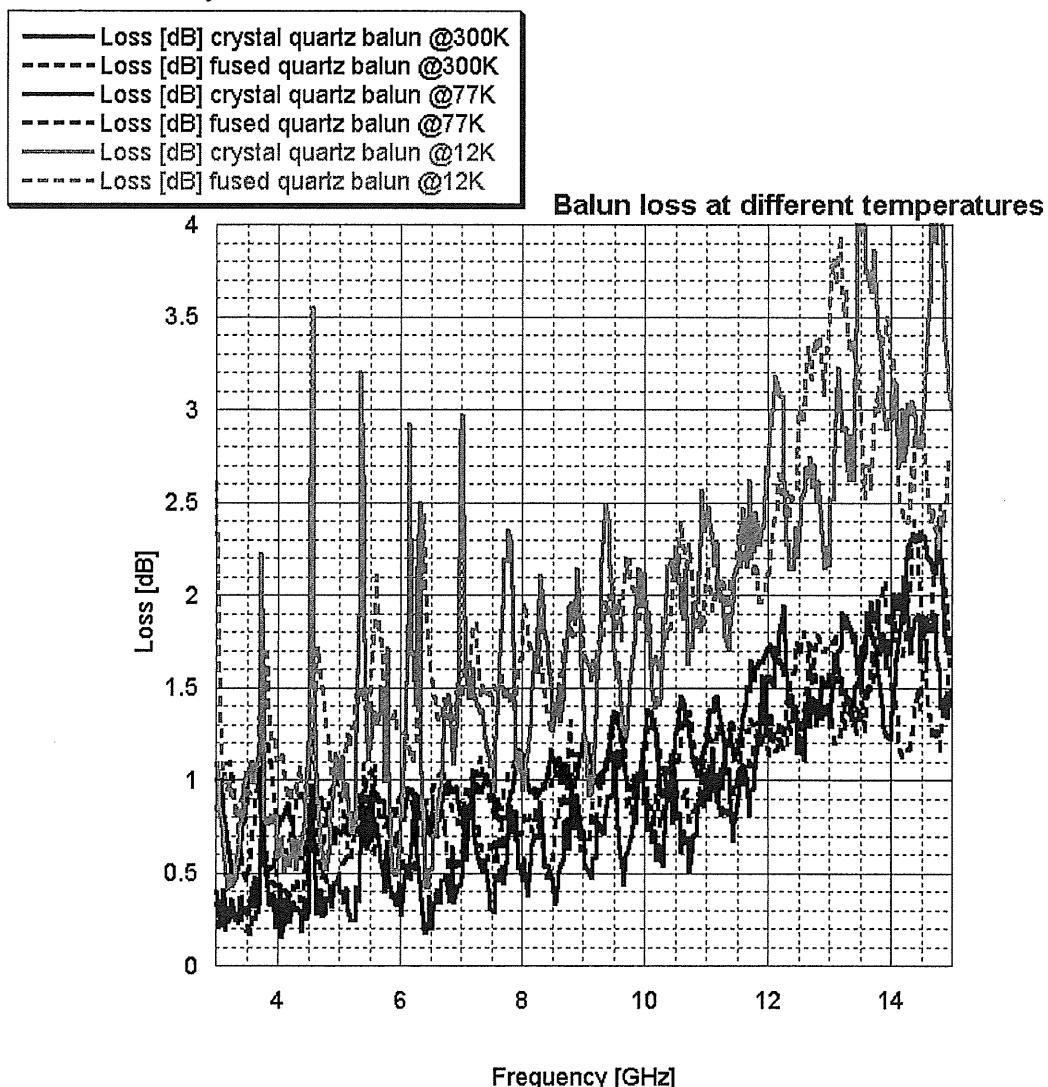


Fig 8. Calculated balun loss at different temperatures

4. Conclusions

The noise and gain of a crystal and a fused quartz balun connected to the single-ended ATA LNA (WBA13) was measured at 300, 77 and 12 K physical temperature, using a new type of differential noise measurement system. The measured noise at 300K agrees well with simulations, but at 77 and 12K it is considerably higher than expected. The reason for this seems to be excessive loss in the baluns, and in the fused quartz case, also the fact that it does not cool down all the way to the tip. DC measurements of the top trace resistance indicate that the excessive balun loss can partly be explained by an impure gold top layer.

Measurements at room temperature show a large periodic ripple in the noise. The period of 600 MHz suggests discontinuities at the LNA and the 200 ohm source, and a signal traveling through the twin lead line and then the intended way through the quartz substrate. The reason for this ripple is unknown.

With the copper foil shield around the balun, sharp peaks appear in the noise at certain frequencies. Also without the shield these peaks appear when the baluns are located inside the 12 or 77K dewar. The reason for these peaks is even mode excitation and is discussed in [3]. It is suggested that the measurements in this report are repeated with a conical ATA shield around the balun to check if the peaks remain or not.

The measurements of the active balun show pretty good agreement with simulations at all three temperatures. The noise has the same ripple as with the passive baluns, suggesting standing waves between the LNA and the 200 ohm source. The reason for this ripple needs to be investigated. The active balun also needs a proper module to make it less sensitive to unwanted feedback when placed in a metal enclosure, and for possible future testing in an ATA feed.

References:

- [1] G. Engargiola, "Tapered Microstrip Balun for ATA Feed Development", ATA memo 35
- [2] G. Engargiola , "Tapered microstrip balun for integrating a low noise amplifier with a nonplanar log periodic antenna", Review of Scientific Instrument, VOLUME 74, NUMBER 12, December 2003
- [3] W.J. Welch, "Generation of Unwanted EM Modes in the ATA Feed Dewar", ATA memo 56