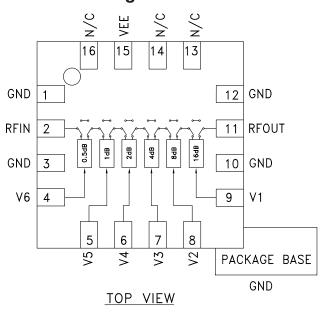


Typical Applications

The HMC424LP3 is ideal for:

- Basestation Infrastructure
- Fiber Optics & Broadband Telecom
- Microwave & VSAT Radios
- Military & Space
- Test Instrumentation

Functional Diagram



Features

0.5 dB LSB Steps to 31.5 dB
Single Control Line Per Bit
+/- 0.5 dB Typical Bit Error
9mm² Leadless SMT Plastic Package

General Description

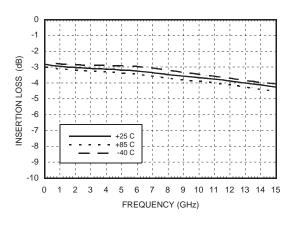
The HMC424LP3 is a broadband 6-bit GaAs IC digital attenuator in a low cost leadless surface mount package. Covering DC to 13 GHz, the insertion loss is less then 4 dB typical. The attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent at \pm 0.5 dB typical step error with an IIP3 of +32 dBm. Six control voltage inputs, toggled between 0 and -5V, are used to select each attenuation state. A single Vee bias of -5V allows operation at frequencies down to DC.

Electrical Specifications, $T_A = +25^{\circ} \text{ C}$, With Vee = -5V & VCTL= 0/-5V

Parameter		Frequency (GHz)	Min.	Тур.	Max.	Units
Insertion Loss		DC - 4.0 GHz 4.0 - 8.0 GHz 8.0 - 13.0 GHz		3.1 3.5 4.0	3.8 4.0 4.6	dB dB dB
Attenuation Range		DC - 13.0 GHz		31.5		dB
Return Loss (RF1 & RF2, All Atten. States)		DC - 13.0 GHz	9	12		dB
Attenuation Accuracy: (Referenced to Insertion Loss)	0.5 - 15.5 dB States 16 - 31.5 dB States	DC - 13.0 GHz DC - 13.0 GHz	± 0.3 + 3% of Atten. Setting Max ± 0.3 + 5% of Atten. Setting Max		dB dB	
Input Power for 0.1 dB Compression		1.0 - 13.0 Ghz		22		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	REF State All Other States	1.0 - 13.0 Ghz		46 32		dBm dBm
Switching Characteristics		DC - 13.0 GHz				
tRISE, tFALL (10/90% RF) tON/tOFF (50% CTL to 10/90% RF)				30 50		ns ns

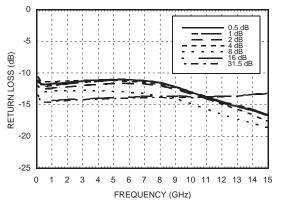


Insertion Loss



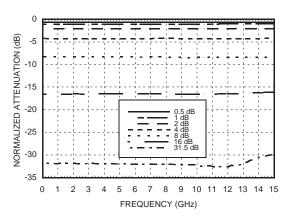
Return Loss RF1, RF2



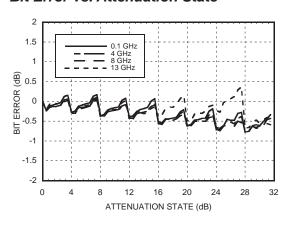


Normalized Attenuation

(Only Major States are Shown)

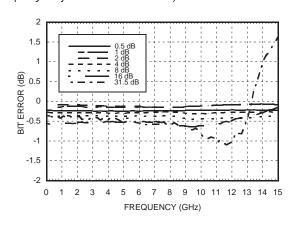


Bit Error vs. Attenuation State



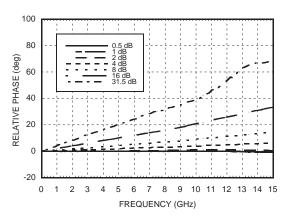
Bit Error vs. Frequency

(Only Major States are Shown)



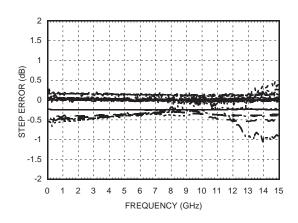
Relative Phase vs. Frequency

(Only Major States are Shown)





Worst Case Step Error Between Successive Attenuation States



Bias Voltage & Current

Vee Range= -5.0 Vdc ± 10%		
Vee (VDC)	lee (Typ.) (mA)	lee (Max.) (mA)
-5.0	2	4

Control Voltage

State	Bias Condition
Low	0 to -3V @ 70 μA Typ.
High	-5 to -4.2V @ 5 μA Typ.

Truth Table

Control Voltage Input					Attenuation		
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	V6 0.5 dB	State RF - RF2	
Low	Low	Low	Low	Low	Low	Reference I.L.	
Low	Low	Low	Low	Low	High	0.5 dB	
Low	Low	Low	Low	High	Low	1 dB	
Low	Low	Low	High	Low	Low	2 dB	
Low	Low	High	Low	Low	Low	4 dB	
Low	High	Low	Low	Low	Low	8 dB	
High	Low	Low	Low	Low	Low	16 dB	
High	High	High	High	High	High	31.5 dB	

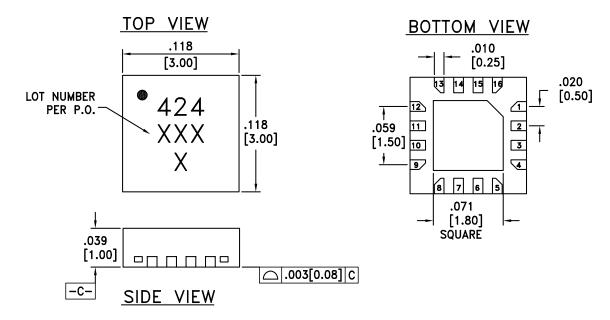
Any Combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.



Absolute Maximum Ratings

Control Voltage (V1 to V5)	Vee - 0.5 Vdc
Bias Voltage (Vee)	-7.0 Vdc
Storage Temperature	-65 to + 150 deg C
Operating Temperature	-55 to +85 deg C
RF Input Power (0.5 - 13.0 GHz)	+25 dBm

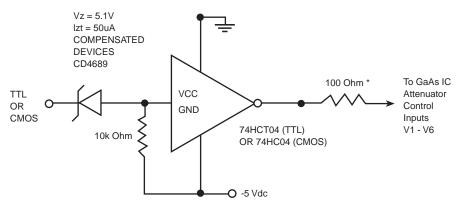
Pin Locations & Outline Drawing



- 1. MATERIAL: PLASTIC
- 2. PLATING: GOLD OVER NICKEL
- 3. ALL DIMENSIONS IN INCHES (MILLIMETERS)
- 4. ALL TOLERANCES ARE ±0.005 (±0.13)
- 5. ALL GROUNDS MUST BE SOLDERED TO THE PCB RF GROUND
- 6. INDICATES PIN 1
- 7. GROUND PAD



Suggested Driver Circuit (One Circuit Required Per Bit Control Input)



Simple driver using inexpensive standard logic ICs provides fast switching using minimum DC current.

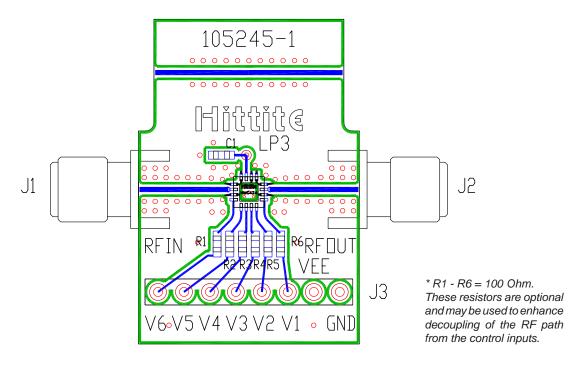
* Recommended value to suppress unwanted RF signals at V1 -V6 control lines.

Pad Description

Pad Number	Function	Description	Interface Schematic
1, 3, 10, 12	GND	Package bottom has an exposed metal paddle that must also be connected to RF ground.	0
2, 11	RFIN, RFOUT	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.	
4, 5, 6, 7, 8, 9	V1 - V6	See truth table and control voltage table.	100K
13, 14, 16	NC	This pin should be connected to PCB RF ground to maximize performance	<u> </u>
15	VEE	Supply Voltage -5V ± 10%	0 3pF ≥ 2K



HMC424LP3 Evaluation PCB



The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation Circuit Board Layout Design Details

Item	Description	
J1 - J2	PC Mount SMA Connector	
J3	8 Pin DC Connector	
C1	0.01 μF Capacitor, 0603 Pkg.	
R1 - R6	100 Ohm Resistor, 0603 Pkg.	
U1	HMC424LP3 Digital Attenuator	
PCB*	105245 Evaluation PCB	
* Circuit Board Material: Rogers 4350		