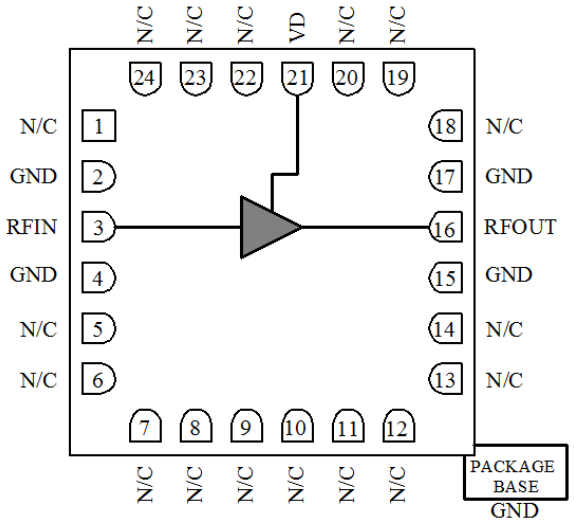
Features

- Single Biasing Voltage (Self Biased)
- Frequency: 0.05-20GHz
- Small Signal Gain: 23dBTypical
- Gain Flatness: ±1.5dB Typical
- Noise Figure:2.3dB Typical
- P1dB: 12dBm Typical
- Power Supply: +5V@57mA
- Input/Output: 50Ω
- Package Size : 4 x 4 x 0.87mm

Functional Block Diagram



Typical Applications

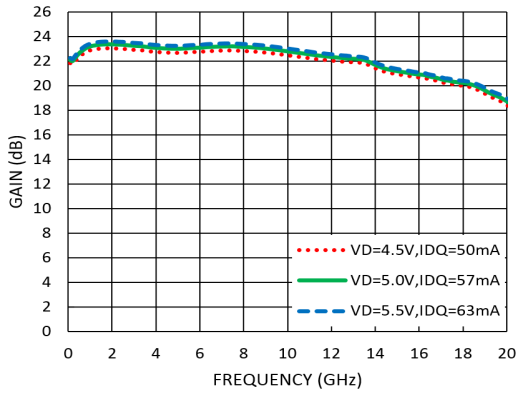
- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

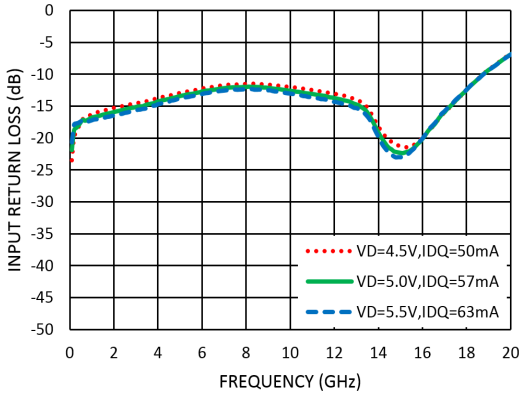
Electrical Specifications

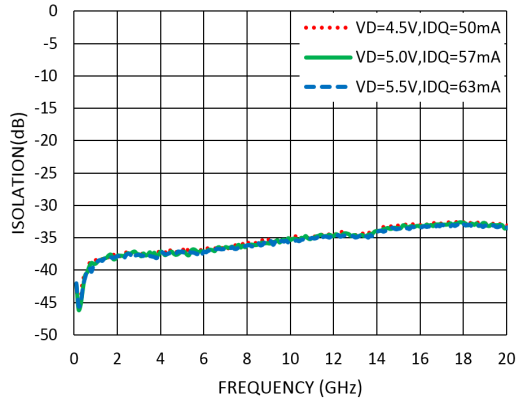
TA = +25°C, VD = +5V, IDD = 57mA Typical

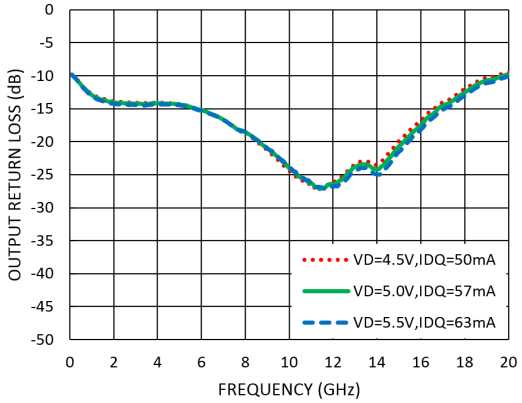
Parameters	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency	0.05		12	12		20	GHz
Small Signal Gain	20	23		18	20		dB
Gain Flatness		±1.0			±1.5		dB
Noise Figure		2.2			2.4		dB
P1dB - Output 1dB Compression	10	12		10	12		dBm
Psat - Saturated Output Power		14			13.5		dBm
OIP3 - Output Third Order Intercept		23			24		dBm
Input Return Loss		-13			-13		dB
Output Return Loss		-15			-15		dB

Measurement Plots: S-parameters

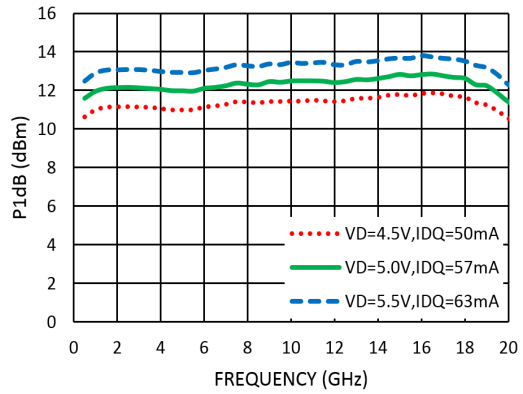




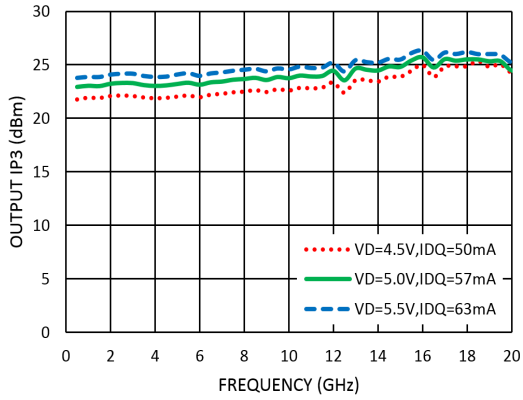




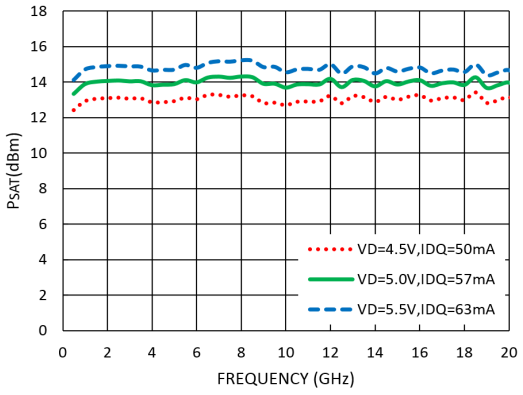
Measurement Plots: P1dB



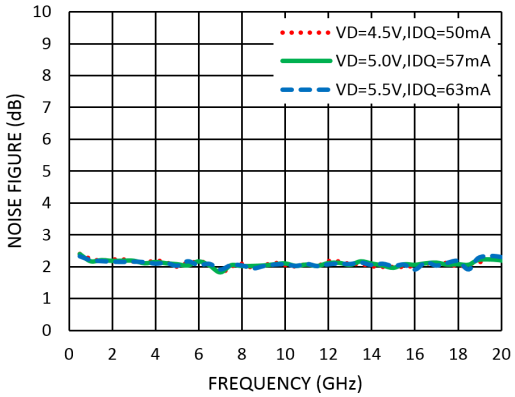
Measurement Plots: OIP3



Measurement Plots: PSAT



Measurement Plots: Noise Figure



Absolute Maximum Ratings

Drain Bias Voltage (VD)	+6V
RF Input Power (RFIN)	+18dBm
Channel Temperature	175°C
Continuous Pdiss (T = 85 °C) (derate 4.7mW/°C above 85 °C)	0.42W
Thermal Resistance (channel to die bottom)	50°C/W
Operating Temperature	-55°C to +85 °C
Storage Temperature	-65°C to +150 °C

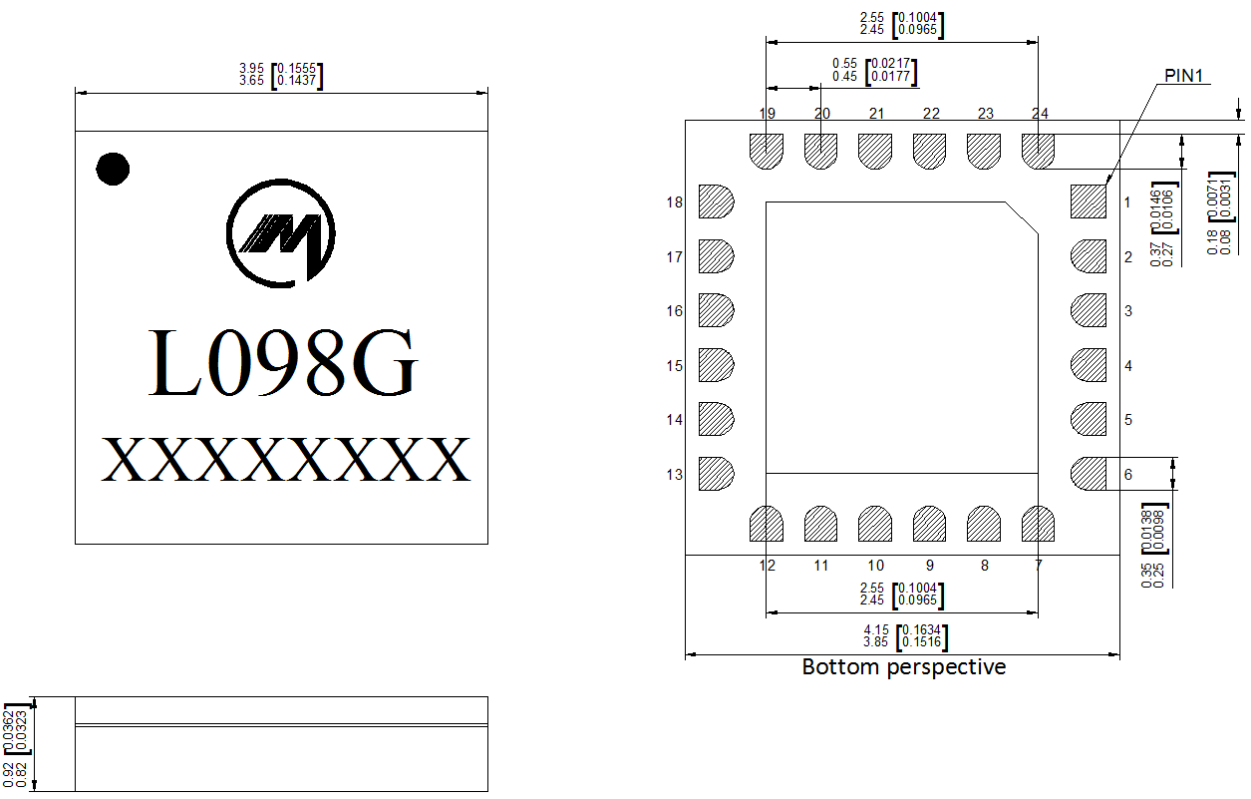
Typical Supply Current vs. VD

VD (V)	IDD (mA)
+4.5	50
+5.0	57
+5.5	63

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing:

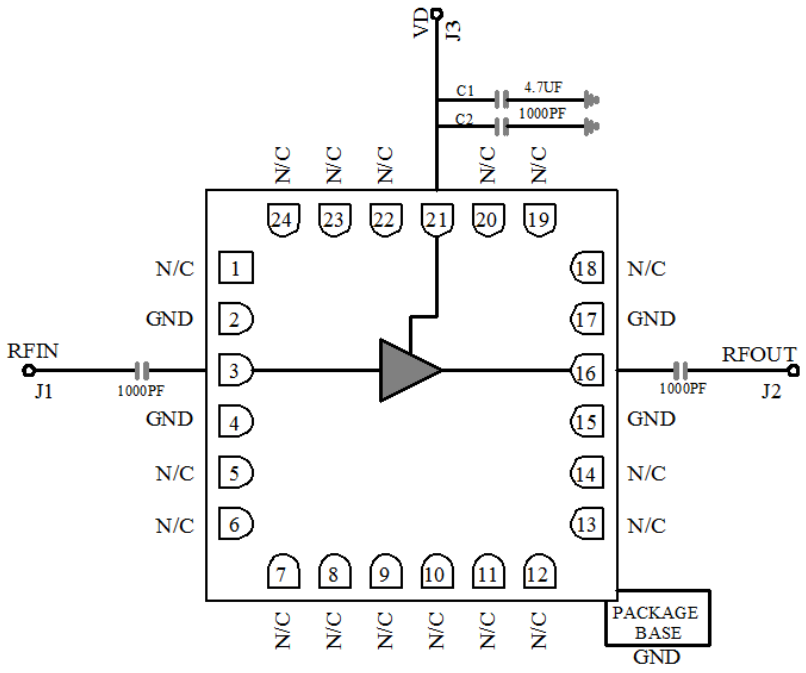
All Dimensions in mm[inches]



Notes:

1. Package body material : Alumina.
2. Lead and ground paddle plating: Gold flash over nickel.
3. Dimensions are in millimeters(inches).
4. Lead spacing tolerance is non-cumulative.

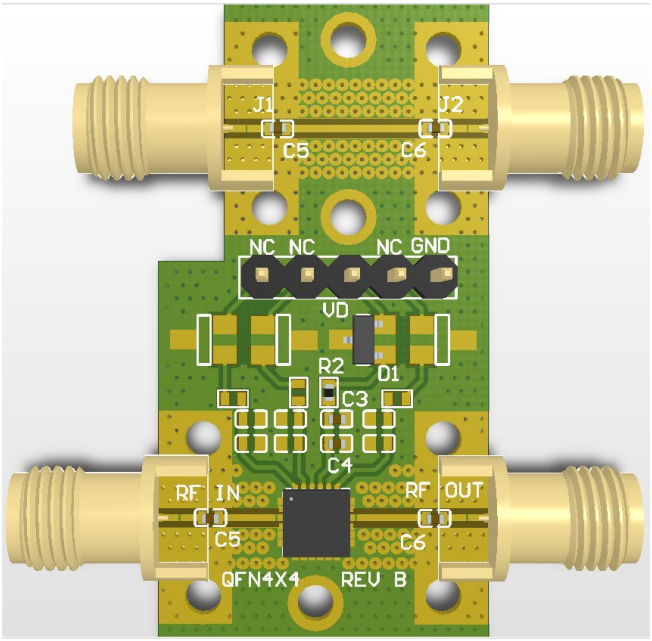
Assembly Drawing

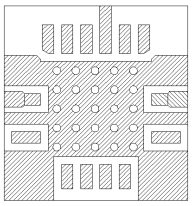


Pin Descriptions

No	Function	Description
1,5,6,7,8,9,10,11,12,13, 14,18,19,20,22,23,24	NC	No connection. These pins may be connected to RF ground. Performance will not be affected.
3	RF IN	Signal input terminal, connected to 50Ω circuit; blocking capacitor required.
16	RF OUT	Signal output terminal, connected to 50Ω circuit; blocking capacitor required.
21	VD	Connect to external 1000pf and 4.7uf bypass capacitors.
2,4,15,17	GND	These pins & exposed ground paddle must be connected to RF/DC ground
25	GND	Package bottom must be connected to RF/DC ground

Evaluation Board Layout Assembly and Mounting Pattern





Mounting Detail

Top dielectric material is ROGERS 4003C, 0.008 inch thickness with 0.5 oz copper.

The pad pattern shown above has been developed and tested for optimized assembly at Miller. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008~0.01 in. diameter drill, filled with copper plating.

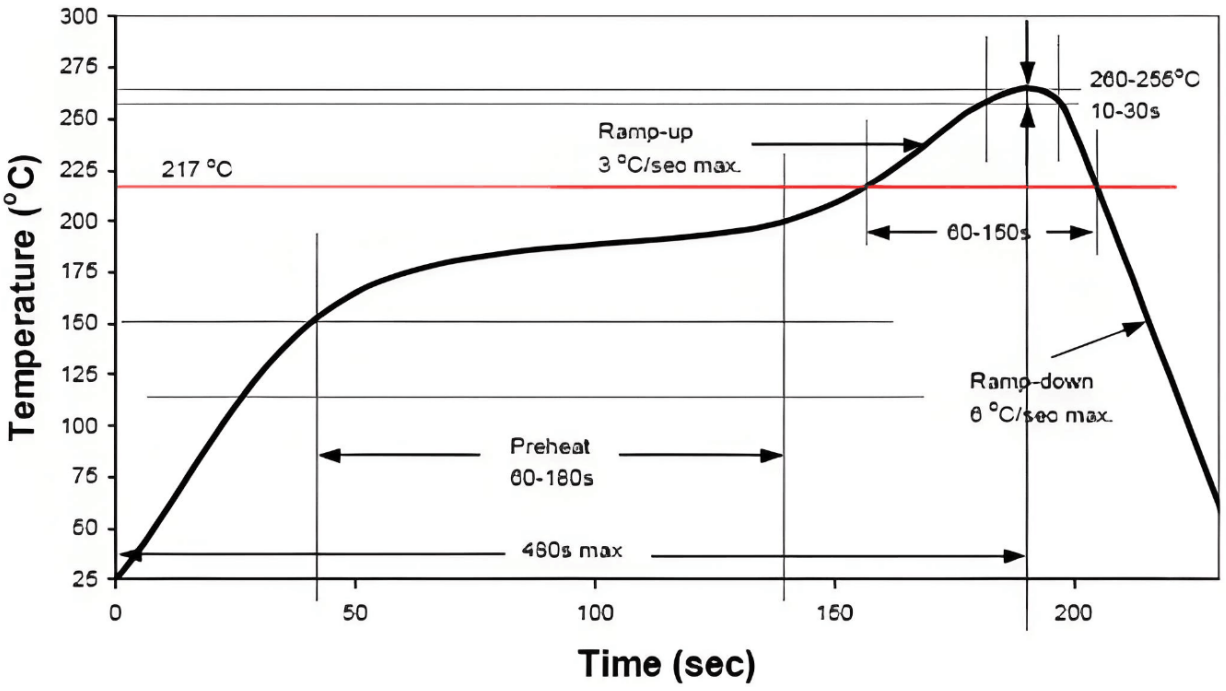
Bill of Materials

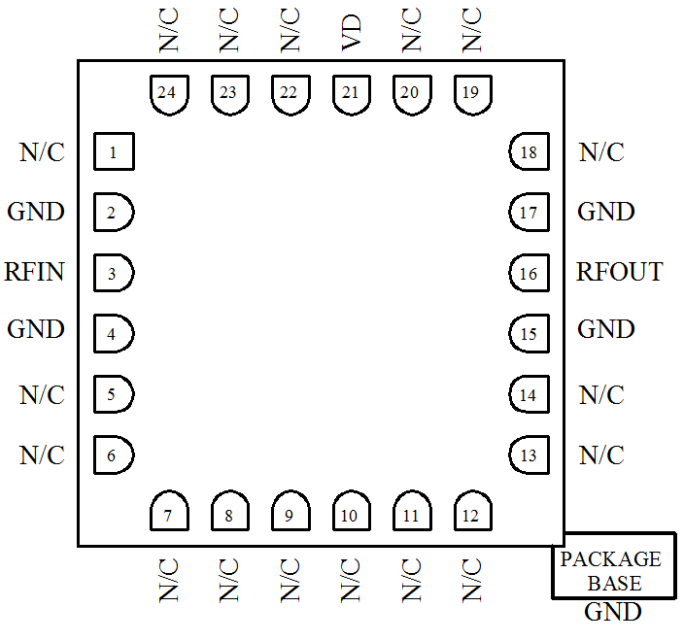
Reference Des.	Value	Description	Manuf.
C3	4.7uF	Cap, 0402, +10V, ±10 %, X5R	Various
C4	100pF	Cap, 0402, +50V, ±5%, X7R	Various
C5,C6	1000pF	Cap, 0402, +50V, ±10%, X7R	Various
R2	0.01 Ω	Res, 0402,0.06W	Various
D1	6.8V	Diode,SOT23,ESD	Various

Solderability

1. Compatible with lead-free soldering process with 260℃ peak reflow temperature.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile





Biasing and Operation

Turn ON procedure:

1. Connect GND to RF and dc ground.
2. Apply positive drain voltage VD and set to +5.0 V .
3. Apply RF signal.

Turn OFF procedure:

1. Turn off the RF signal.
2. Turn off the positive drain voltage VD.