Analog Output Interface Preliminary Design

Larry R. D'Addario

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1. Requirements

We require an assembly that will accept a complex digital sample stream corresponding to a phased-array sum from the ATA and convert it to analog form for further processing. The assembly should be a direct plug-in replacement for a "Back End Transmitter" (BET) module of the ATA, and therefore it should be implemented on a single 6U×160 mm printed circuit board with a backplane interface identical to that of the BET. It should process all four of the sample streams (for the four beams generated from one baseband channel) that appear on the backplane. The analog outputs should appear at baseband on coaxial connectors on the front panel of the new module, with nominal source impedance of 50 ohms.

The samples are fixed-point complex numbers with real and imaginary parts of 16b each, sampled at 104.16 MHz. They represent a Nyquist band that extends from −52.08 MHz to +52.08 MHz. At the backplane, the samples are time-multiplexed by 4 to a clock rate of 416.64 MHz, and appear as (4 beams)×(real+imag)×(16b/4 mux) = 32 LVDS signals.

The module operates in only one mode, producing whatever analog signals correspond to the backplane's digital signals. Therefore it needs no control inputs and produces no other outputs, other than the control and monitor signals needed to support its internal design. A simple control and monitoring interface, for technical purposes only, is anticipated.

2. Architectures

2.1 Sideband Separation and Nyquist-Rate DACs

The most straightforward architecture for each beam is shown in Figure 1. Here the complex sample stream is digitally transformed to two real sample streams containing the upper sideband (positive frequencies) and lower sideband (negative frequencies), respectively. Then each real stream is presented to a digital-to-analog converter, resulting in a piecewise-constant current signal. Lowpass filters cutting off at the Nyquist frequency (52 MHz) then reconstruct the desired waveform.

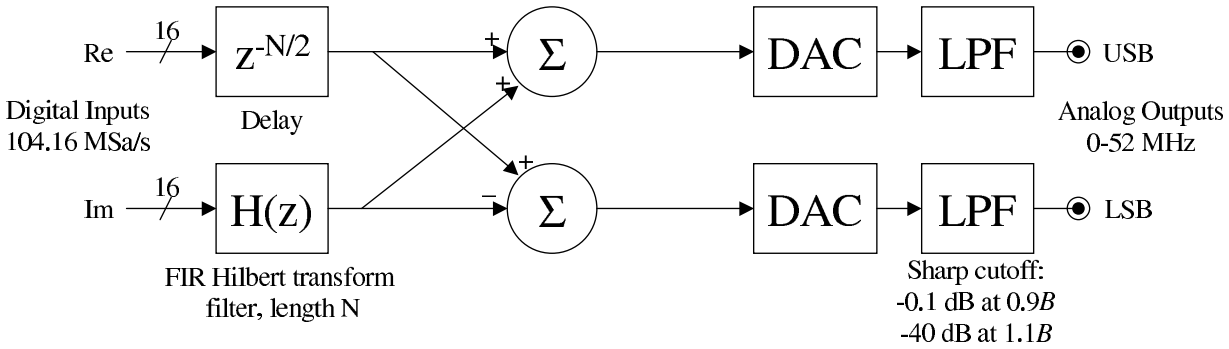

Figure 1: Architecture based on digital sideband separation with Nyquist-rate digital-to-analog conversion.

The sideband separation process consists mainly of an FIR filter approximating a Hilbert transform applied to the imaginary input. It shifts the phase of all frequencies in the Nyquist band by $\pi/2$, and introduces a fixed delay. The real input is then delayed by the same amount, then the two results are added to produce the USB signal and subtracted to produce the LSB signal.

With finite complexity, this arrangement produces outputs containing imperfections. These include the following.

- The DACs nominally produce a constant output during each clock period, corresponding to the digital value of the sample at the beginning of that period. This is equivalent to applying a filter having a boxcar impulse response, or a frequency response of $\sin(\pi f/f_s)/(\pi f/f_s)$ for sampling rate f_s, resulting in a gain of −3.9 dB at the Nyquist band edge $f = f_s/2$. This is considered acceptable in the SETI

application, since it can be accounted for in later processing and since it should not significantly affect the signal-to-noise ratio. If it were a problem, a compensating digital filter could be implemented ahead of each DAC.

- The FIR approximation of the Hilbert transform filter has an ideal phase response, but its amplitude response cannot be flat over the entire Nyquist band. This results in imperfect image rejection when its output is combined with the real part. For a given filter length, weights can be optimized to maximize the image rejection over a given portion of the band. For example, a 33-tap filter achieves 27 dB minimum rejection over the inner 90% of the band (from $.05 f_s/2$ to $0.95 f_s/2$. The image rejection vs. frequency for this filter (with infinite-precision arithmetic) is plotted in Figure 2. (Implementation of this filter at the Nyquist clock rate requires only 8 multipliers because the weights are odd-symmetric and all even-numbered weights are zero.)

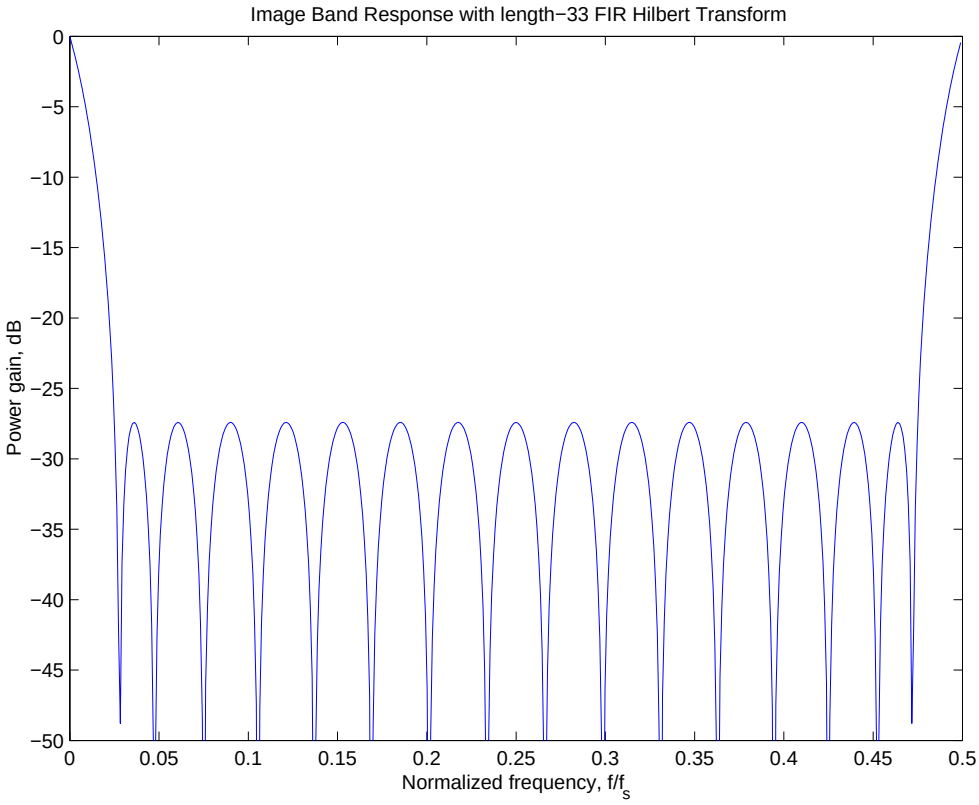

Figure 2: Image sideband response of a digital sideband separator based on a length-33 FIR approximation of a Hilbert transform filter.

- The lowpass reconstruction filters should ideally have boxcar frequency responses, but in practice they have finite rolloff rates. This causes a combination of extra attenuation at the upper end of the passband and leakage of energy from the stopband (which contains an aliased version of the signal) into the passband, and the filter is generally designed as a compromise between these effects. A fairly complex filter (about 13 poles) is needed to keep contamination of the lower 90% of the band below −40 dB. The filter can also cause additional imperfections, such as passband ripple and a complicated phase response. The filter response is subject to fabrication tolerances and variation with temperature.

2.2 Sideband Separation and Interpolation

The above architecture can be improved if some higher-speed processing and higher-speed ADCs are available, as shown in Figure 3. Here the sideband separation circuitry is the same as before, operating at the Nyquist rate, but the USB and LSB signals are each interpolated to a higher sampling rate prior to the ADCs. The ADCs must then operate at the higher rate. Interpolation is accomplished by FIR lowpass

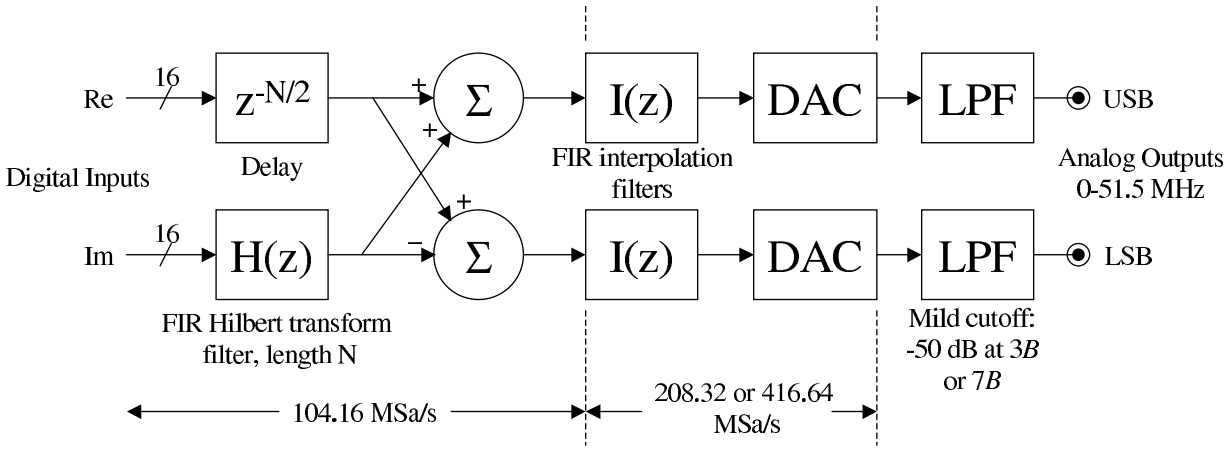

Figure 3: Architecture based on digital sideband separation followed by interpolation, with high-speed digital-to-analog conversion.

filters operating at the higher clock rate. The filters can be designed to provide very sharp cutoff and linear phase, without concern for variations in manufacture or with environmental conditions.

The result is that the analog reconstruction filters can be substantially simpler and their effects on the final outputs can be smaller. For example, with 4x interpolation (to sampling rate 416.64 MHz) alias contamination due to the analog filter can be kept below −40 dB for the entire Nyquist band by a filter whose −40 dB point is at 7 times its −0.5 dB point. On the other hand, alias contamination from the finite rolloff of the digital interpolation filter also occurs.

In addition, the sinc rolloff of the faster DACs has much less affect on the passband. With 4× interpolation, the gain loss at the band edge is only −0.22 dB.

This architecture is made practical by the availability of DAC ICs that are not only sufficiently fast, but that include the interpolation filters and clock frequency multiplication. Such devices are now available from at least two manufacturers at reasonable prices.[1]

2.3 Interpolation and Up-Conversion

A rather different architecture is shown in Figure 4. Here the real and imaginary inputs are immediately interpolated to a higher sampling rate (at least 2× Nyquist), and then digitally translated upward in frequency by $B/2$, where B is the two-sided Nyquist bandwidth of the signal. This moves both the LSB and USB to positive frequencies, allowing both to be included in a single real signal. The up-conversion can be understood as consisting of complex multiplication by $e^{j\pi Bt}$ and taking the real part of the result, which is equivalent to multiplying the real part of the input by $\cos \pi Bt$ and the imaginary part by $\sin \pi Bt$ and subtacting. The one sample stream is then converted to analog by a high-speed DAC and analog reconstruction filter.

The signal processing for this scheme is illustrated in Figure 5 for the case of 4× interpolation. The interpolation process is similar to that described in section 2.2, except that here it is applied to the real and imaginary parts of the input rather than to the separated USB and LSB signals. The image responses then become well separated from the desired signal. After upconversion, the images remain separated provided that the interpolation factor is greater than 2. Here the nearest image begins at $3B$, making it possible to use a slow-rolloff analog reconstruction filter.

This arrangement requires most of the digital circuitry to operate at a sampling rate faster than the input, but it eliminates the need for the Hilbert transform filter. This means that the errors of that filter are avoided, and there is no significant image contamination between sidebands, not even near the sideband edges. The useful part of the band is thus larger. With 4× interpolation, the DAC rolloff at B is −0.91 dB.

Again, this is made practical by the availablity of commercial ICs that include the interpolation filters, upconversion, and DAC all operating at the requisite speed.

[1] Texas Instruments and Analog Devices each have 16b dual interpolating ADCs that operate to 400 or 500 MHz for $40 to $50 each in small quantities.

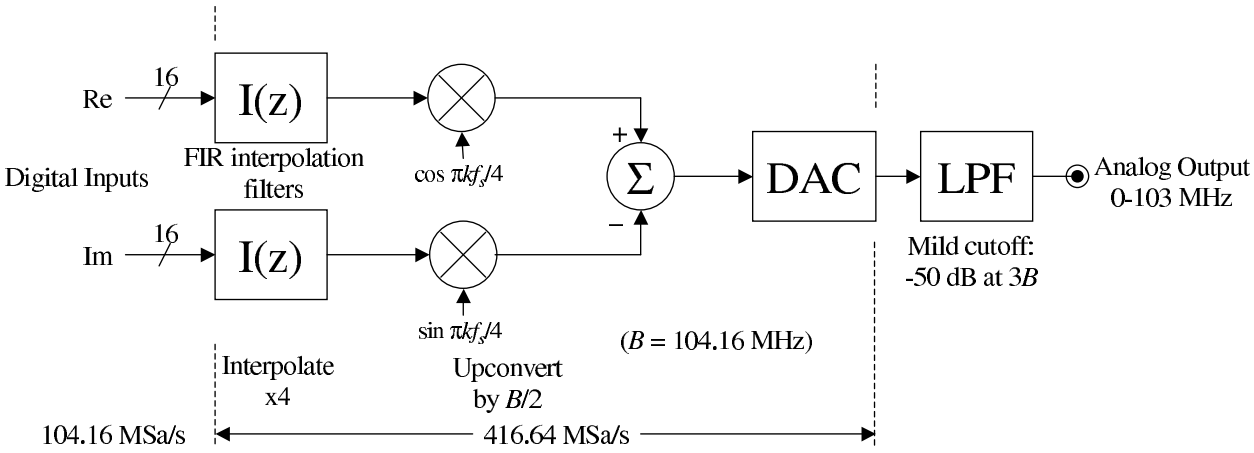

Figure 4: Architecture based on interpolation followed by digital upconversion and high-speed digital-to-analog conversion.

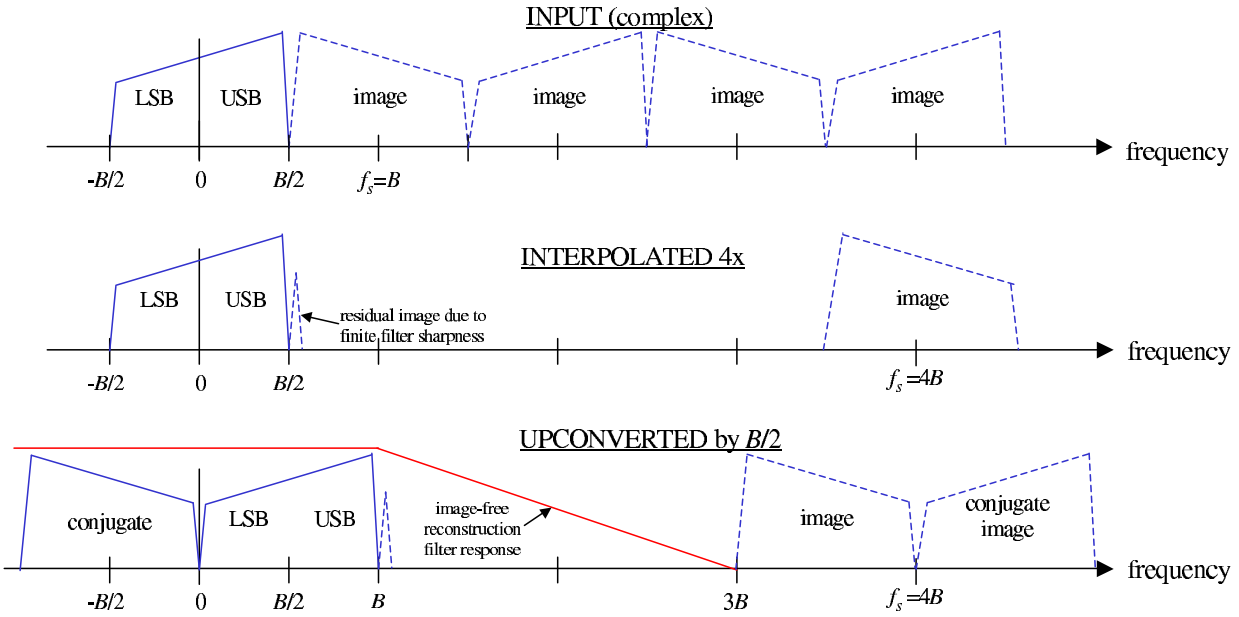

Figure 5: Illustration of signal processing for methods involving interpolation. Top: Spectrum of complex input signal, where negative frequencies (LSB) contain independent information. Sampling rate f_s is equal to the total bandwidth B. Middle: Result of $4\times$ interpolation, to a sampling rate $f_s = 4B$. The image response is now well separated from the desired signal. Bottom: Result of digital upconversion by $B/2$. Taking the real part of the result causes negative frequency components to be complex conjugates of their positive counterparts. Image frequencies remain well separated, enabling D-to-A conversion to use a simple reconstruction filter.

3. Description of Selected Design

Based on the discussion in the preceeding section, the interpolate-and-upconvert architecture is recommended. Figure 6 is a block diagram of the proposed physical design, based on use of the Analog Devices AD9786 integrated circuit [1]. This choice provides the best performance. A disadvantage is that the component costs are higher than for the architecture of section 2.1 and Fig. 1; 200 MHz DACs are available for less than $10 each. On the other hand, the IC costs are still low, and the total cost of the assembly is likely to be dominated by that of the PC board, connectors, assembly, and testing. In addition, considerable development work is avoided by accomplishing most of the signal processing in off-the-shelf parts. This

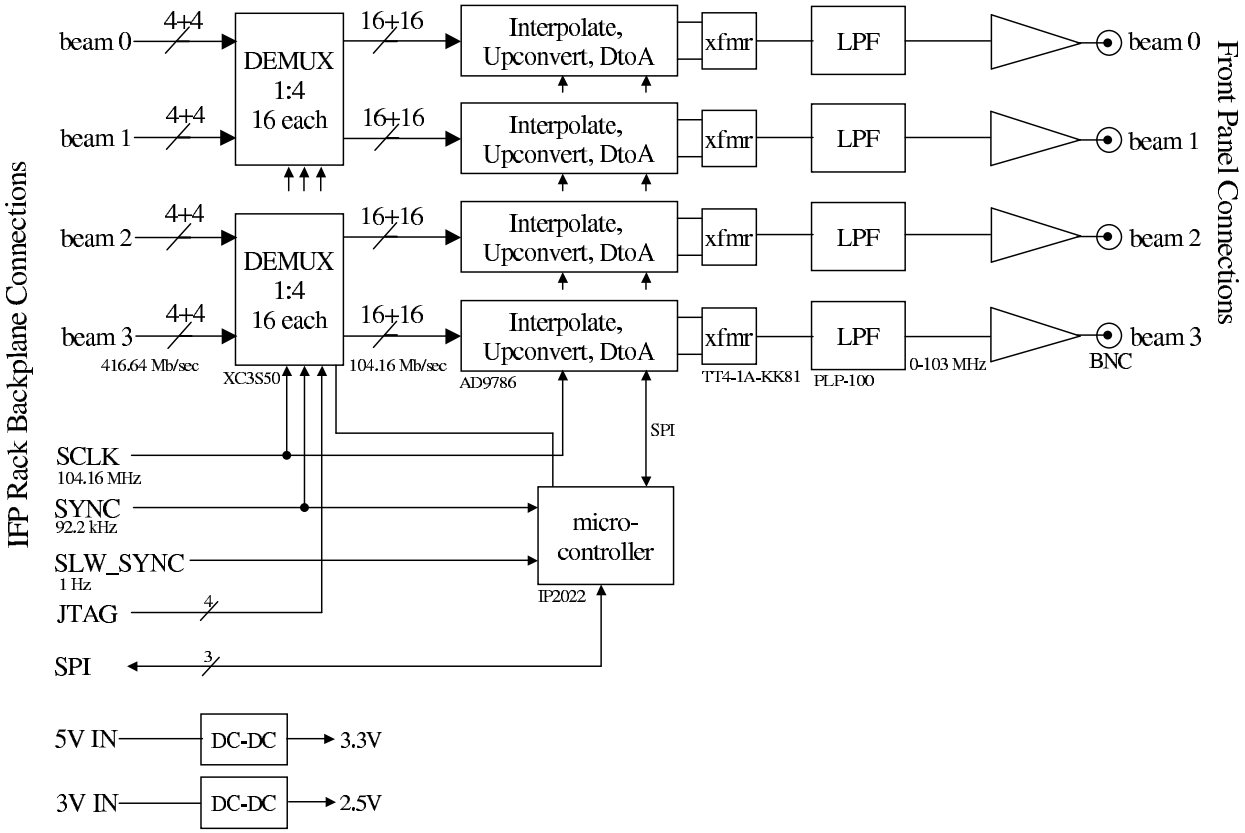

Figure 6: Block diagram of the proposed design.

should be understood in the light of the fact that not many of these assemblies are needed for the ATA — at most 8 of them, one for each baseband channel, plus spares.

Because of the requirement that the assembly be a direct plug-in replacement for the BET, all backplane signals are identical to those on the BET module. These include the signal streams for all beams; clock signals; serial communication with the monitor/control system via an SPI interface; JTAG port for logic programming; and power (+3V and +5V).

The signal streams must first be de-multiplexed to a clock rate equal to the sample rate (from 416.64 MHz to 104.16 MHz), and converted from diffferential to single-ended signalling. Thus, 32 identical 1:4 demultiplexers are required. Very little logic is needed, so it is hard to justify use of an advanced FPGA, but due to the large number of I/O connections and the high speed, the Xilinx Spartan-3 FPGA family is the preliminary choice. It is most economical to split this into two ICs, with half of the demultiplexers in each, so as to use the smallest chip of the family and an inexpensive package type (PQFP). However, the detailed design will include a search for a still more economical solution, perhaps based on CPLDs.

The main signal processing is accomplished by four AD9786s, with one for each beam's signal. When properly configured via its serial control port, each provides all of the digital processing shown in Figures 4 and 5. The device is capable of internal clock rates and DAC conversion rates up to 500 MHz, along with rates up to 200 Mb/sec on the input pins.

The interpolation function uses FIR lowpass filters of fixed design, where the tap weights are given on the data sheet [1]. Interpolation by 4× is done by two half-band filters in cascade; the overall response is plotted in Figure 7. The stopband rejection generally exceeds 70 dB and the passband is extremely flat, but the rolloff is not a sharp as might be desired. It is 20 dB down at 10% above the desired band edge at $B_1 = f_s/8$, and 60 dB down at 20% above. In this region between B_1 and $B_1 + \epsilon$, the signal represented

will be an image of that between B_1 and $B_1 - \epsilon$, but due to the high sampling rate this representation is accurate; there is no distortion of the region below B_1 (see Fig. 5). Such distortion can occur if the output of the assembly is later undersampled.

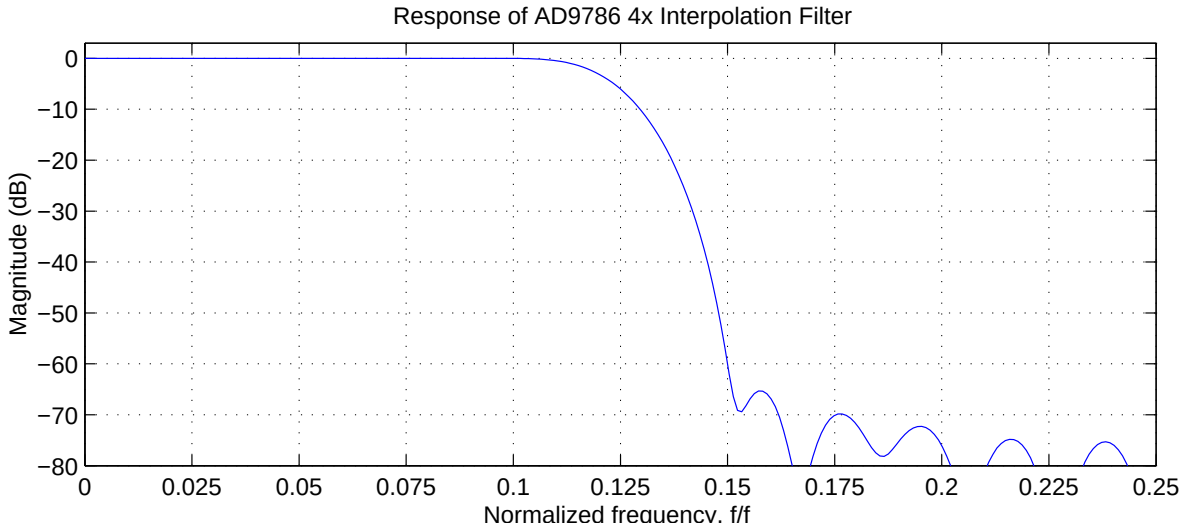

Figure 7: Response of the 4x interpolation filter in the AD9786.

The DAC output of the AD9786 consists of a pair of differential current sources. These are converted to single-ended form with a broadband transformer and then delivered to the reconstruction lowpass filter. As noted earlier, this can be a simple filter with slow rolloff. An inexpensive stock filter from Mini Circuits (Model PLP-100, −1 dB at 98 MHz and −40 dB at 189 MHz) is probably adequate. However, for maximum passband flatness, a Butterworth response filter is recommended; several manufacturers (e.g., TTE) offer inexpensive custom filters in the same package at the PLP-100. A 5-pole ideal Butterworth filter will have more than 60 dB attenuation at 3 times the −1 dB frequency.

Finally, a small buffer amplifier is provided at each analog output so as to provide a high drive level, good impedance match, and good isolation. Without the amplifier, output levels should be around 2 mW into 50 ohms. Amplified outputs around 30 mW (+15 dBm) can easily be provided.

The control interface uses a Ubicom IP2022 microcontroller, identical to that used in the BET and IF Processor modules. It is much more powerful than needed here, but this allows re-use of software written for the other devices. Its main purpose is to put the AD9786 chips into the proper configuration for the desired signal processing, but it can also support internal test functions as discussed below. It communicates with higher level computers via an SPI port identical to that on the BET. A JTAG port for programming the FPGAs (or CPLDs) is also provided; again, this is identical to the BET.

Three system clock signals are delivered via the backplane. The 104.16 MHz main clock (SCLK) is distributed to the demultiplexers (FPGAs) and the signal processing DACs; in each chip, it is internally multiplied to 416.64 MHz. The slower clocks (SYNC and SLW_SYNC) are used primarily by the microcontroller.

Power on the backplane is available at 5.0V and 3.0V. These are converted on the board to the voltages needed by the chips. The AD9786s require 3.3V and 2.5V. Details of the on-board converters can be copied from existing designs.

Besides the components shown in Figure 6, various small ICs and passive components will be required. Line receivers and drivers are needed for the interface signals and clocks. External memory is probably needed for the microcontroller.

3.1 Optional Additional Features

Although the arrangement of Figure 6 satisfies all the requirements, various additional features may be usefully added at low cost. Some of them are described briefly here.

- *Ethernet Port.* The microcontroller supports an ethernet connection, and such a connection is provided on the BET and IFP boards. The system application for it is uncertain, but it is easy to provide.
- *Test Signal Generation.* The de-multiplexer chips will have considerable spare logic, especially if FPGAs are used. Then can be designed to replace the input sample streams by test signals of various types, including sinusoids and pseudo-random noise, in order to facilitate debugging and troubleshooting. This can be commanded via the microcontroller.
- *Loop-back Self Test.* By adding a fast analog to digital converter on the board, a self-testing capability can be implemented. Analog switches can be used to connect any of the outputs to the ADC, and a block of its samples can be buffered and then slowly read by the microcontroller. The results can be analyzed to verify proper operation of the board when it is generating test signals, or to do broader system tests when sample streams from the telescope are being processed.

3.2 Availability of Components and Alternatives

The design described here is based on the Analog Devices AD9786 interpolating DAC. This IC is new, and is not yet in production. It can be purchased as part of an evaluation board, and is expected to go into production in the first quarter of 2004 [2]. Pricing is not yet available, but based on competing devices it is expected to be around $50 in small quantities. However, alternatives are immediately available that allow implementation of the same architecture.

The Texas Instuments DAC5686 provides very similar functionality and speed (dual 16b inputs, 500 MHz DAC rate, up to 16x interpolation). It has more capabilities than we need, and includes two high speed output DACs, one of which would not be used in our application. It has some disadvantages with respect to clock synchronization compared to the AD9786. The small-quantity price is $46.75.

The AD9777 ($40) and the TI DAC5674 ($21) are also interpolating DACs with adequate functionality for our application, but they are specified only to 400 MHz DAC rate. Most likely they would operate at our slightly faster rate, but this is not guaranteed. The DAC5674 also has less digital resolution at 14b.

REFERENCES

[1] Analog Devices, Inc., "16-bit, 200-500 MSPS TxDAC+ with 2x/4x/8x interpolation and signal processing: Preliminary technical data." AD9786 preliminary data sheet, rev PrC, dated 8/27/2003.

[2] Gerry Spring, Analog Devices High Speed Converters division, private communication (email of 2004-Jan-16).