RF MICRO·DEVICES

NDA-412

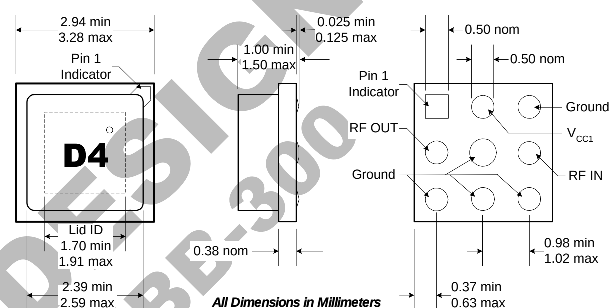
InGaP/GaAs HBT MMIC DISTRIBUTED AMPLIFIER DC TO 11GHz

Typical Applications

- Narrow and Broadband Commercial and Military Radio Designs
- Linear and Saturated Amplifiers
- Gain Stage or Driver Amplifiers for MW Radio/Optical Designs

Product Description

The NDA-412 InGaP/GaAs HBT MMIC distributed amplifier is a low-cost, high-performance solution for high frequency RF, microwave, or optical amplification needs. This 50Ω matched distributed amplifier is based on a reliable HBT proprietary MMIC design, providing unsurpassed performance for small-signal applications. Designed with an external bias resistor, the NDA-412 provides flexibility and stability. In addition, the NDA-410-D chip was designed with an additional ground via to enable low junction temperature operation. NDA-series distributed amplifiers provide design flexibility by incorporating AGC functionality into their designs.



Notes:
1. Solder pads are coplanar to within ±0.025 mm.
2. Lid will be centered relative to frontside metallization with a tolerance of ±0.13 mm.
3. Mark to include two characters and dot to reference pin 1.

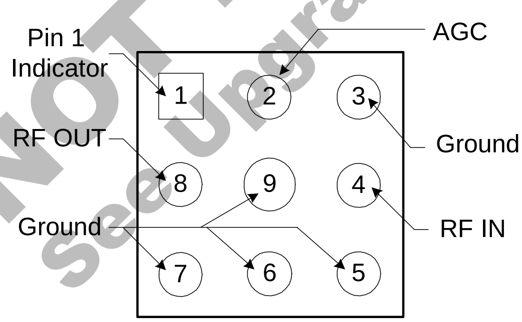
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☑ InGaP/HBT
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaN HEMT
- ☐ GaAs MESFET
- ☐ Si CMOS
- ☐ SiGe Bi-CMOS

Package Style: MPGA, Bowtie, 3x3, Ceramic

Features

- Reliable, Low-Cost HBT Design
- 12.0dB Gain, +14.6dBm P1dB@2GHz
- High P1dB of +14.0dBm@6.0GHz and +13.0dBm@11.0GHz
- Fixed Gain or AGC Operation
- 50Ω I/O Matched for High Freq. Use



Functional Block Diagram

Ordering Information

NDA-412	InGaP/GaAs HBT MMIC Distributed Amplifier DC to 11GHz

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Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+15	dBm
Power Dissipation	300	mW
Device Current, I_{CC1}	42	mA
Device Current, I_{CC2}	42	mA
Output Device Voltage, V_{C2}	3.5	V
Junction Temperature, Tj	200	°C
Operating Temperature	-45 to +85	°C
Storage Temperature	-65 to +150	°C

Exceeding any one or a combination of these limits may cause permanent damage.

Caution! ESD sensitive device.

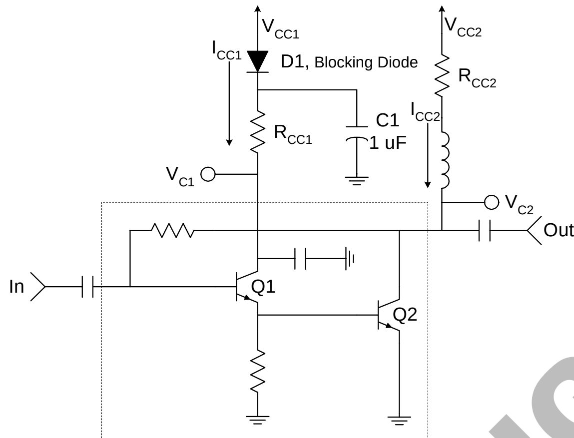
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC1}=+10V, V_{CC2}=+10V, V_{C1}=+4.7V, V_{C2}=+2.98V, I_{CC1}=29mA, I_{CC2}=36mA, Z_0=50Ω, T_A=+25°C
Small Signal Power Gain, S21	12.0	13.0		dB	f=0.1GHz to 4.0GHz
		12.0		dB	f=4.0GHz to 6.0GHz
		13.0		dB	f=6.0GHz to 8.0GHz
	11.0	14.0		dB	f=8.0GHz to 11.0GHz
Input and Output VSWR		1.25			f=0.1GHz to 4.0GHz
		2.10			f=4.0GHz to 8.0GHz
		3.50			f=8.0GHz to 11.0GHz
Bandwidth, BW		12.5		GHz	BW3 (3dB)
Output Power @ 1dB Compression		14.6		dBm	f=2.0GHz
		14.0		dBm	f=6.0GHz
		13.0		dBm	f=11.0GHz
Noise Figure, NF		5.0		dB	f=2.0GHz
Third Order Intercept, IP3		+24.0		dBm	f=2.0GHz
Reverse Isolation, S12		-16.0		dB	f=0.1GHz to 11.0GHz
Output Device Voltage, V_{C2}	2.70	2.98	3.20	V	
AGC Control Voltage, V_{C1}		4.7		V	
Gain Temperature Coefficient, $\delta G_T/\delta T$		-0.0015		dB/°C	
MTTF versus Temperature @ $P_{TOT,DIS}$=245mW					
Case Temperature		85		°C	
Junction Temperature		144		°C	
MTTF		>1,000,000		hours	
Thermal Resistance					
θ_{JC}		242		°C/W	$\frac{J_T - T_{CASE}}{V_D \cdot I_{CC}} = \theta_{JC}(°C/Watt)$

Suggested Voltage Supply: $V_{CC1} \geq 4.7V$, $V_{CC2} \geq 5.0V$

Pin	Function	Description	Interface Schematic
1	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
2	VCC1	AGC bias pin. Biasing is accomplished with an external series resistor to V_{CC1}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{CC1} - V_{DEVICE1})}{I_{CC1}}$$ Care should also be taken in the resistor selection to ensure that the current into the part never exceeds maximum datasheet operating (mA) over the planned operating temperature. This means that a resistor between the supply and this pin is always required, even if a supply near 5.0V is available, to provide DC feedback to prevent thermal runaway. Alternatively, a constant current supply circuit may be implemented. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
3	GND	Same as pin 1.	
4	RF IN	RF input pin. This pin is NOT internally DC blocked. A DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. DC coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.	
5	GND	Same as pin 1.	
6	GND	Same as pin 1.	
7	GND	Same as pin 1.	
8	RF OUT AND VCC2	RF output and bias pin. Biasing is accomplished with an external series resistor and choke inductor to V_{CC2}. The resistor is selected to set the DC current into this pin to a desired level. The resistor value is determined by the following equation: $$R = \frac{(V_{CC2} - V_{DEVICE2})}{I_{CC2}}$$ Care should also be taken in the resistor selection to ensure that the current into the part never exceeds maximum datasheet operating current (mA) over the planned operating temperature. This means that a resistor between the supply and this pin is always required, even if a supply near 5.0V is available, to provide DC feedback to prevent thermal runaway. Alternatively, a constant current supply circuit may be implemented. Because DC is present on this pin, a DC blocking capacitor, suitable for the frequency of operation, should be used in most applications. The supply side of the bias network should also be well bypassed.	
9	GND	Same as pin 1.	

Typical Bias Configuration

Application notes related to biasing circuit, device footprint, and thermal considerations are available on request.



Simplified Schematic of Distributed Amplifier

Bias Resistor Selection
R_{CC1}: For $4.7V<V_{CC1}<5.0V$ $R_{CC1}=0\Omega$ For $5.0V<V_{CC1}<10.0V$ $R_{CC1}=V_{CC1}-4.7/0.029\Omega$
R_{CC2}: For $5.0V<V_{CC2}<10.0V$ $R_{CC1}=V_{CC2}-2.98/0.036\Omega$

Typical Bias Parameters for $V_{CC1}=V_{CC2}=10V$:							
V_{CC1} (V)	V_{CC2} (V)	I_{CC1} (mA)	V_{C1} (V)	R_{CC1} (Ω)	I_{CC2} (mA)	V_{C2} (V)	R_{CC2} (Ω)
10	10	29	4.75	180	36	2.98	195

Application Notes

Die Attach

The die attach process mechanically attaches the die to the circuit substrate. In addition, it electrically connects the ground to the trace on which the chip is mounted, and establishes the thermal path by which heat can leave the chip.

Wire Bonding

Electrical connections to the chip are made through wire bonds. Either wedge or ball bonding methods are acceptable practices for wire bonding.

Assembly Procedure

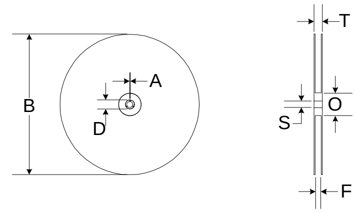
Epoxy or eutectic die attach are both acceptable attachment methods. Top and bottom metallization are gold. Conductive silver-filled epoxies are recommended. This procedure involves the use of epoxy to form a joint between the backside gold of the chip and the metallized area of the substrate. A 150°C cure for 1 hour is necessary. Recommended epoxy is Ablebond 84-1LMI from Ablestik.

Bonding Temperature (Wedge or Ball)

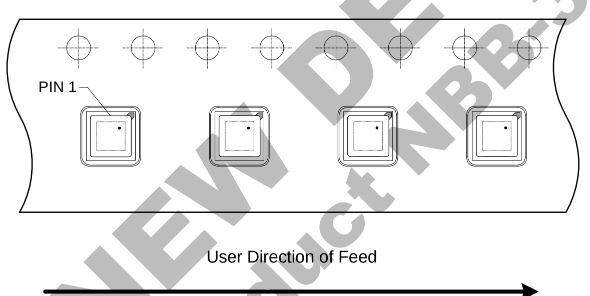
It is recommended that the heater block temperature be set to 160°C±10°C.

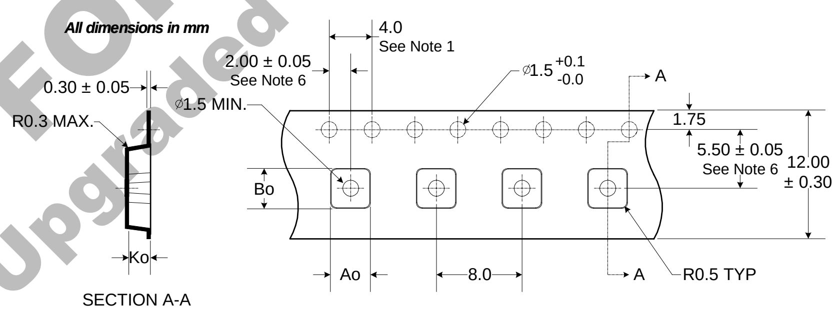
Tape and Reel Dimensions

All Dimensions in Millimeters



330 mm (13") REEL			Micro-X, MPGA	
	ITEMS	SYMBOL	SIZE (mm)	SIZE (inches)
FLANGE	Diameter	B	330 +0.25/-4.0	13.0 +0.079/-0.158
	Thickness	T	18.4 MAX	0.724 MAX
	Space Between Flange	F	12.4 +2.0	0.488 +0.08
HUB	Outer Diameter	O	102.0 REF	4.0 REF
	Spindle Hole Diameter	S	13.0 +0.5/-0.2	0.512 +0.020/-0.008
	Key Slit Width	A	1.5 MIN	0.059 MIN
	Key Slit Diameter	D	20.2 MIN	0.795 MIN

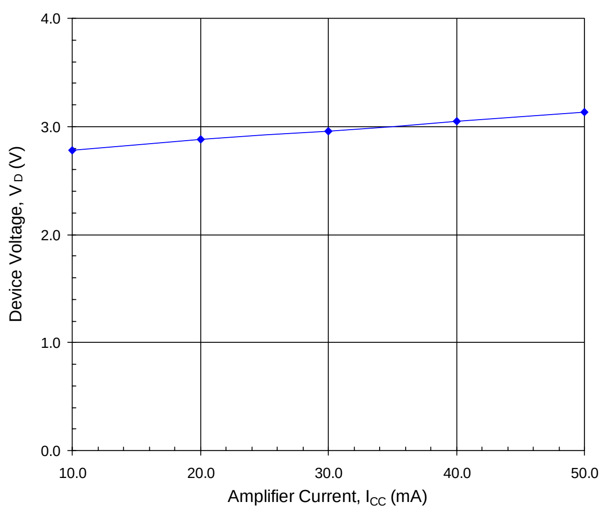




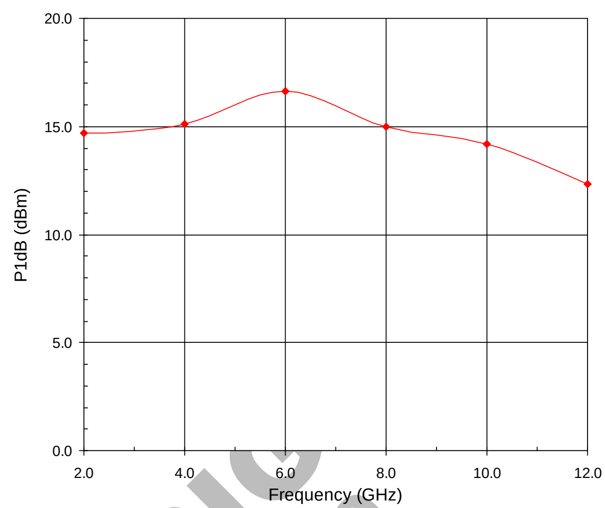
NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm.
3. Material: PS+C
4. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 3.6 MM
Bo = 3.6 MM
Ko = 1.7 MM

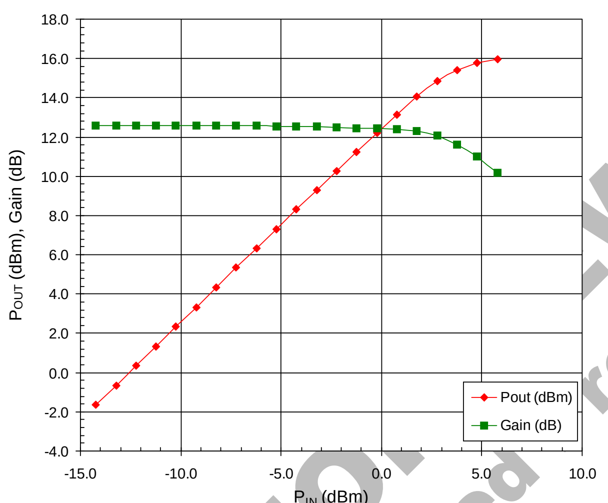
Device Voltage versus Amplifier Current



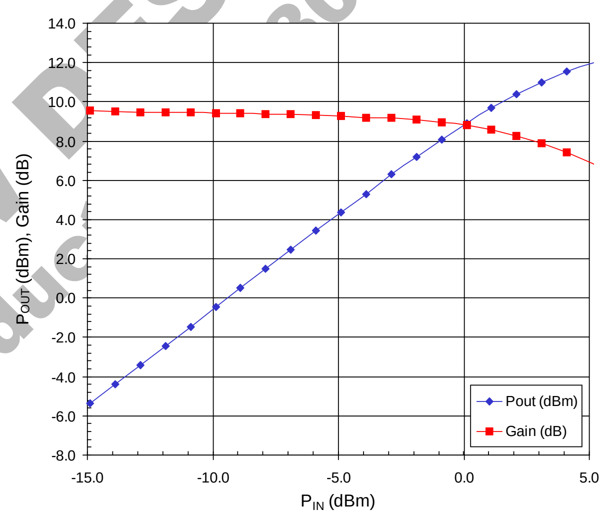
P1dB versus Frequency at 25°C



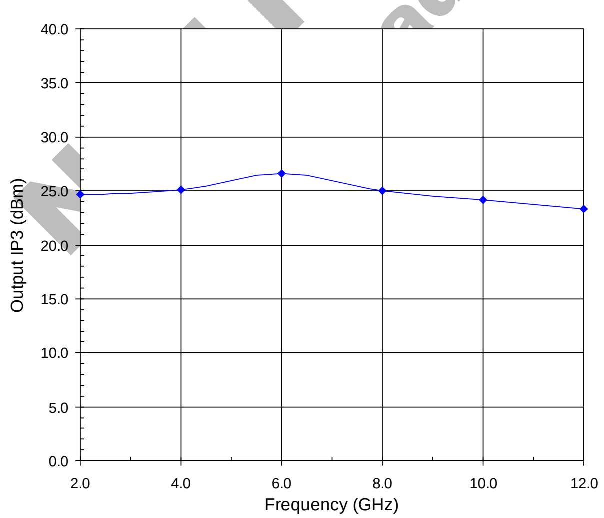
P_{OUT}/Gain versus P_{IN} at 6 GHz



P_{OUT}/Gain versus P_{IN} at 14 GHz



Third Order Intercept versus Frequency at 25°C



Note: The s-parameter gain results shown below include device performance as well as evaluation board and connector loss variations. The insertion losses of the evaluation board and connectors are as follows:

1GHz to 4GHz=-0.06dB
5GHz to 9GHz=-0.22dB
10GHz to 14GHz=-0.50dB
15GHz to 20GHz=-1.08dB