

# **Course Introduction**

# Instructional Support

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- **Teaching mode:** concurrent classroom and online (Feishu)
- **Office Hours:** W 4:00 – 6:00pm / Th 10:00am – noon, in office or on Feishu, or by appointment
- **TAs:**
  - Mr. SHI Xiaotian, [sxt813@sjtu.edu.cn](mailto:sxt813@sjtu.edu.cn)
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- **Recitation:** TBD
- **TA Office Hours:** TBD

# What will be taught?

- Assembly language
- How computers execute programs?
- What's the correspondence between different levels of languages: C/C++, assembly, and machine language?
- How to design a processor as a digital system?
- What are the difficulties and tricks in the design of a CPU? How to resolve? How to improve?
- How memory works as part of a computer, and how is it organized?
- How processor, memory, and I/O devices work together as a computer?

# What Are You Expected to Do?

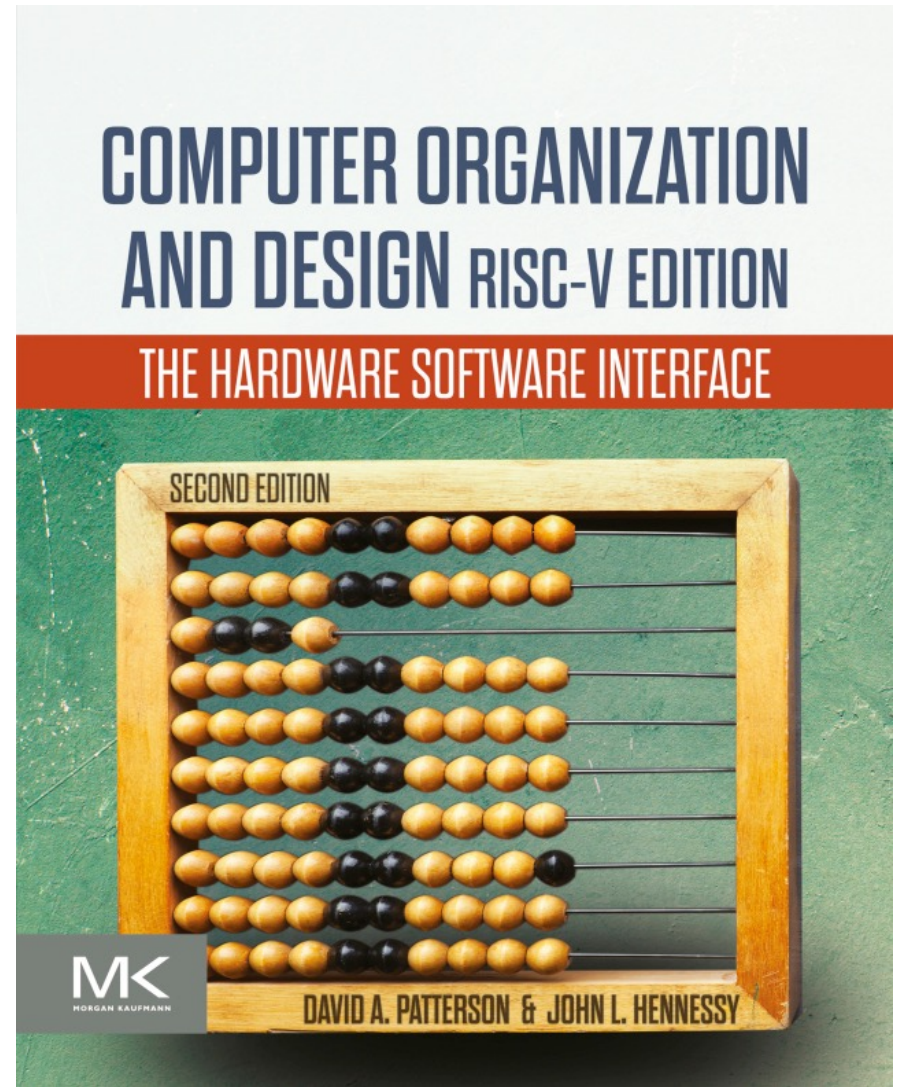
- Write an assembly language program, translate the program into binary code, and trace execution of the program.
- Model a processor using hardware description languages (HDLs).
- Be able to identify and resolve potential data and control hazards in the Instruction Set Architecture (ISA)
- Understand memory hierarchy including cache, main memory, hard disk, and how data is stored, understand memory hits and misses
- Understand the memory mapped I/O concept and how I/O devices interface to the CPU
- Be able to use library and internet resources for literature search to learn contemporary issues, technologies, and future development trends in computing

# Textbook

David Patterson and John Hennessy

*Computer Organization  
and Design RISC-V Edition,*  
2<sup>nd</sup> edition

Morgan Kaufmann, 2020,  
ISBN-10: 0128203315  
ISBN-13: 978-0128203316



# Tentative Schedule

Week	Date	Topics	Labs
1	9/14	Course Introduction, introduction to computer	
	9/16	RISC-V assembly: operations and operands	
2	9/21	<b>No Class (National Holiday)</b>	Lab 1 (Assembly)
	9/23	RISC-V assembly: function and function call	
3	9/28	RISC-V assembly: function and function call	Lab 2 (Assembly Functions)
	9/30	RISC-V assembly: instruction encoding	
4	10/5	<b>No Class (National Holiday)</b>	
	10/7	<b>No Class (National Holiday)</b>	
5	10/12	CPU: single cycle processor	Preparation for Literature Review Project
	10/14	CPU: pipelined processor	
6	10/19	CPU: pipelined processor	Lab 3 (Single Cycle Processor)
	10/21	CPU: data hazards	
7	10/26	CPU: data hazards	Lab 4 (Pipelined Processor)
	10/28	CPU: data hazards	
8	11/2	<b>Midterm Exam</b>	
	11/4	CPU: control hazards	
9	11/9	CPU: control hazards	Lab 5 (Taking Care of Hazards)
	11/11	Memory: cache	
10	11/16	Memory: cache	
	11/18	Memory: cache	
11	11/23	Memory: cache	Lab 6 (Cache)
	11/25	Memory: virtual memory	
12	11/30	Memory: virtual memory	Lab 7 (Everything for Memory)
	12/2	Memory: virtual memory	
13	12/7	I/Os and interfaces	
	12/9	Discussion & Review	
14	TBD	<b>Final Exam</b>	

# Course Policies

## ■ Honor Code:

- Honor Code of the Joint Institute
- *Addendum to the Honor Code for Online Teaching.*

## ■ Test:

- Test procedure will be announced prior to the tests. Anyone violating the test procedure will be given an 'F' for the test.

## ■ Attendance:

- Strongly encouraged for better understanding of difficult concepts and student engagement during class time

## ■ Participation:

- Active participation is highly expected for all students. This involves:
  - Participation in interactive activities during the lecture time
  - Active involvement in labs
  - Proper assistance to other students in group studying
  - Contributions to the Q&A on Piazza, etc.

# Course Policies

## ■ Individual Assignments:

- Homework, some labs, literature review project
- OK to discuss course topics and help each other understand the project/homework requirements better
- NOT OK for duplicated submission

## ■ Group Assignments:

- Some labs are team efforts
- Teams of 3 students, grouped randomly
- Group now, study together through the semester

## ■ Submission:

- Electronic submission on Canvas before deadline



# Assessment Methods

- **Homework:**

- About 8 homework assignments

- **Examination:**

- Two online or paper-based examinations.
- The typical types of exam problems include conceptual understanding, computation, procedural development, short answer, analysis and design, and etc.

- **Laboratory:**

- 7 labs
- Labs 1-3 are individual work
- Labs 4-7 are team work

# Assessment Methods

## ■ Literature Review Project:

- Choose an interesting area, search literatures to review, write a review report

## ■ Participation and Etiquette:

- Classroom interaction with the instructor and other students
- effective contribution on Piazza
- active participation in team-based labs.
- Vandalism, spam messages, verbal and other forms of abuse, violation of English-only policies and disturbance of the learning experience of other students are not permitted

# Grading Policy

Participation & Etiquette	5%
Midterm Exam	20%
Final Exam	20%
Lab */**	40%
Literature Review Project *	5%
Homework *	10%
<b>Total</b>	<b>100%</b>

\*Individual assignments

\*\*Group assignments

Note: final letter grades may be curved