JOINT INSTITUTE
交大密西根学院

Ve370 Introduction to Computer Organization

Homework 4

楊毅文 519370910053

Assigned: October 21, 2021

Due: 2:00pm on October 28, 2021

Submit a PDF file on Canvas

1. (15 points) Given this instruction:
   `lw x5, -4(x2)`

   As the instruction goes through the pipeline, what will be stored in the pipeline registers:
   // Instruction = 11111111100 00010 010 00101 0000011

   IF: what's in PC
   The address of the instruction `lw`

   ID: what's in IF/ID
   The address of the instruction `lw`, the instruction

   EX: what's in ID/EX?
   The address of the instruction `lw`, read data of `x2`, read data (not used), immediate number = `-4`, sign bit = 1, funct3 = 010, rd = 00101, control signals (Branch = 0, MemRead = 1, MemtoReg = 1, ALUop = 00, MemWrite = 0, ALUsrc = 1, RegWrite = 1)

   MEM: what's in EX/MEM
   The address of the instruction `lw` + immediate number * 2, Zero = 0, ALU result = (`x2 - 4`) , read data 2 (not used), rd = 00101, control signals (Branch = 0, MemRead = 1, MemtoReg = 1, MemWrite = 0, RegWrite = 1)

   WB: what's in MEM/WB?
   Read data from memory with address (`x2 - 4`), ALU result = (`x2 - 4`), rd = 00101, control signals (MemtoReg = 1, RegWrite = 1)

2. (20 points) Assume that individual stages of the RISC-V pipelined datapath have the following latencies:

IF	ID	EX	MEM	WB
250 ps	350 ps	150 ps	300 ps	200 ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	Load	Store
45%	20%	20%	15%

(1) What is the clock cycle time? (2 points)
T_{cc} = 350 ps
(2) What is the execution time of a sw instruction in the pipelined processor? (3 points)
$T_{sw} = 5T_{cc}$ = 1750 ps
(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor? (5 points)
ID stage should be split, then T_{cc} = 300 ps
(4) Using the processor to run a program of 1,000 instructions, what is the total execution time? What is the CPI? (10 points)

$$\text{CPI} = \frac{1000 + 4}{1000} = 1.004$$

$$T_{total} = \text{IC} \times \text{CPI} \times T_{cc} = 1000 \times 1.004 \times 350 = 351400 \text{ ps}$$

3. (10 points) Assume that x11 is initialized to 11 and x12 is initialized to 22. Suppose you executed the code below on a pipelined processor that does not handle data hazards at all.

```
L1: addi x11, x12, 5
L2: add x13, x12, x11
L3: addi x14, x11, 15
```

(1) Indicate data dependencies, if any, in above instruction sequence. (which register between which instructions) (5 points)
`x12` between `L1` and `L2`;
`x11` between `L1` and `L2`, `L2` and `L3`.
(2) What would the final values of registers x13 and x14 be? (5 points)
`x13` = 33, `x14` = 26

4. (30 points) Given the following instructions:

```
L1: sw  x18,-12(x8)
L2: lw  x3,8(x18)
L3: add x6,x3,x3
L4: or  x8,x9,x6
```

a) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)
hazards: `x3` between `L2` and `L3`, `x6` between `L3` and `L4`, 12 cycles

```
L1: sw  x18,-12(x8)
L2: lw  x3,8(x18)
NOP
NOP
L3: add x6,x3,x3
NOP
NOP
L4: or  x8,x9,x6
```

b) Assume there is ALU-ALU forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)
hazards: `x3` between `L2` and `L3`, 10 cycles

```
L1: sw  x18,-12(x8)
L2: lw  x3,8(x18)
NOP
NOP
L3: add x6,x3,x3
L4: or  x8,x9,x6
```

c) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them. How many clock cycles will it take to execute the instructions? (10 points)
hazards: `x3` between `L2` and `L3`, 9 cycles

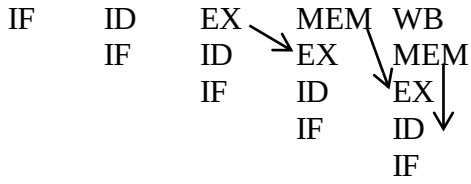
```
L1: sw  x18,-12(x8)
L2: lw  x3,8(x18)
NOP
L3: add x6,x3,x3
L4: or  x8,x9,x6
```

5. (25 points) Given this assembly instruction sequence executed by the pipelined processor:

```
sub x6, x2, x1
lw  x3, 8(x6)
lw  x2, 0(x6)
or  x3, x5, x3
sw  x3, 0(x5)
```

a) If the processor has forwarding, but we forgot to implement the hazard detection unit, what happens when this code executes? (5 points)
The code will run correctly, since the hazards are already solved by forwarding and no need for extra stall.

b) If there is forwarding, for the first five cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units. (10 points)



First five cycles:					PCWrite	IF/IDWrite	Control	ALU_1	ALU_2
IF	ID	EX	MEM	WB	1	1	1	00	00
	IF	ID	EX	MEM	1	1	1	10	00
		IF	ID	EX	1	1	1	01	00
			IF	ID	1	1	1	00	01
				IF	1	1	1	00	10

c) If there is no forwarding, what new inputs and output signals do we need for the hazard detection unit? Using this instruction sequence as an example, explain why each signal is needed. (10 points)
New inputs: EX/MEM.RegisterRd, MEM/WB.RegisterRd, EX/MEM.RegWrite, MEM/WB.RegWrite.
New outputs: None.
EX/MEM.RegisterRd, EX/MEM.RegWrite are used to detect EX hazard, such as `x3` between `L4` and `L5`; MEM/WB.RegisterRd, MEM/WB.RegWrite are used to detect MEM hazard, such as `x6` between `L1` and `L3`.