JOINT INSTITUTE
交大密西根学院

Ve370 Introduction to Computer Organization

Homework 3

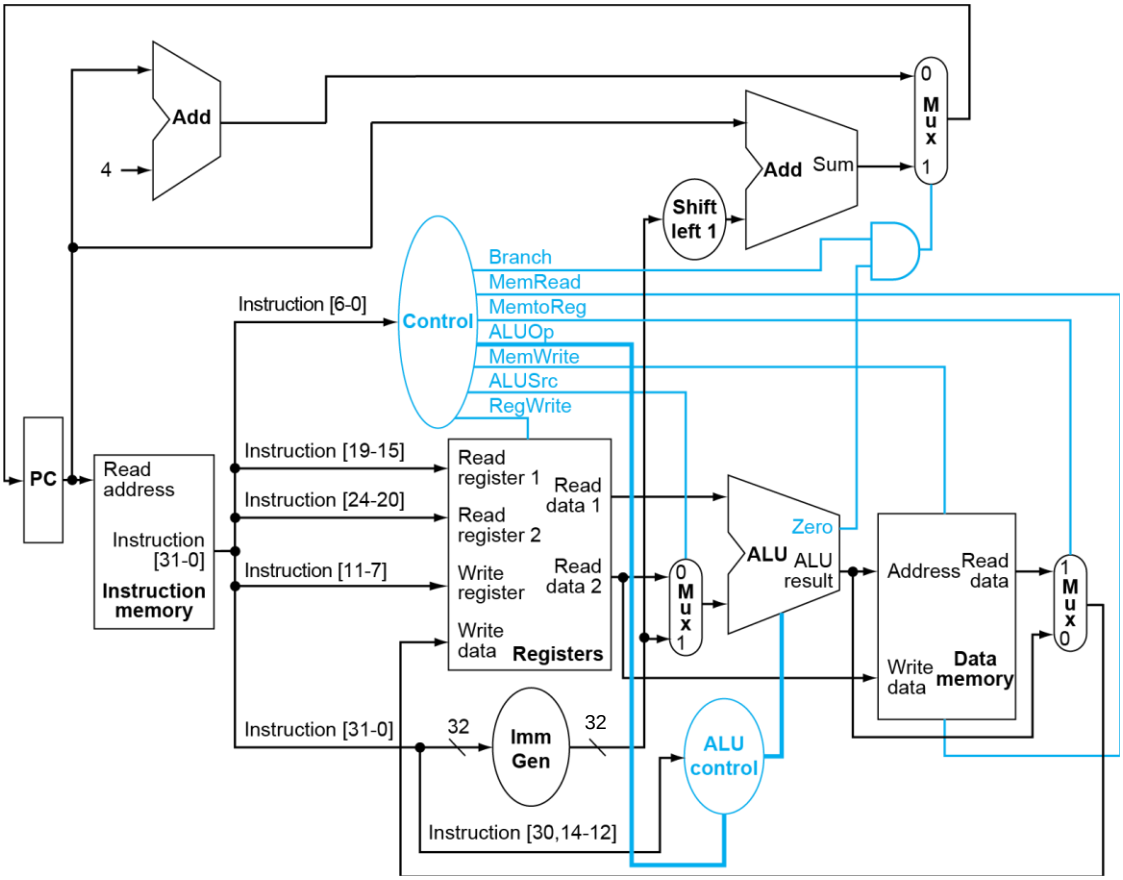
楊毅文 519370910053

Assigned: October 12, 2021

Due: 2:00pm on October 19, 2021

Submit a PDF file on Canvas

All questions refer to the following figure.



1. (30 points) Given RISC-V assembly instruction sequence:

```
       bne x22, x23, Else
       add x19, x20, x21
       beq x0,x0,Exit
Else:  lw x19, 0(x20)
Exit:  …
```

Assuming the memory location of the first instruction (`bne`) is 0x1000F400, what are the values of the following control signals for each of the instructions?

Ctrl Signals / Instruction	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUSrc	RegWrite	Zero	ImmGen Output
`add`	0	0	0	10	0	0	1	0	X
`beq`	1	0	0	01	0	0	0	1	0000000000000000 0000000000000100
`lw`	0	1	1	00	0	1	1	0	0000000000000000 0000000000000000

2. (10 points) Given following assembly instruction:
`and rd, rs1, rs2`

   (1) Which resources (blocks) perform a useful function for this instruction? (3 points)
   PC, Instruction memory, registers, ALU.
   (2) Which resources (blocks) produce no output for this instruction? Which resources produce output that is not used? (7 points)
   Data memory produces no output.
   ImmGen produces output that is not used.

3. (10 points) Consider the following instruction mix:

R-type	**I-type (non-lw)**	**Load**	**Store**	**Branch**	**Jump**
24%	28%	25%	10%	11%	2%

   (1) What fraction of all instructions use data memory? (3 points)
   35%
   (2) What fraction of all instructions use instruction memory? (2 points)
   100%
   (3) What fraction of all instructions use the sign extend? (5 points)
   76%

4. (10 points) When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get “broken” and always read a logical 0. This is often called a “stuck-at-0” fault.
   (1) Which instructions fail to operate correctly if the MemToReg wire is stuck at 0? (5 points)
   Load instructions as `lw`.
   (2) Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0? (5 points)
   I-type and S-type.

5. (30 points) Problems in this exercise assume that the logic blocks used to implement a processor’s datapath have the following latencies:

I-Mem / D-Mem	Register File	Mux	ALU	Adder	Single gate	Register Read	Register Setup	Sign extend	Control
250 ps	150 ps	25 ps	200 ps	150 ps	5 ps	30 ps	20 ps	50 ps	50 ps

In above table, "Register Read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register Setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

(1) What is the latency of an R-type instruction (i.e., how long must the clock period be to ensure that this instruction works correctly)? (5 points)
Critical path is PC→I Mem→Register File→Mux→ALU→Mux→Register File.
20+30+250+150+25+200+25+150=850 ps

(2) What is the latency of lw? (5 points)
Critical path is PC→I Mem→Register File→Mux→ALU→D Mem→Mux→Register File.
20+30+250+150+25+200+250+25+150=1100 ps

(3) What is the latency of sw? (5 points)
Critical path is PC→I Mem→Register File→Mux→ALU→D Mem.
20+30+250+150+25+200+250=925 ps

(4) What is the latency of beq? (5 points)
Critical path is PC→I Mem→Register File→Mux→ALU→And gate→Mux.
20+30+250+150+25+200+5+25=705 ps

(5) What is the latency of an arithmetic, logical, or shift I-type (non-load) instruction? (5 points)
Critical path is PC→I Mem→Register File→Mux→ALU→Mux→Register File.
20+30+250+150+25+200+25+150=850 ps

(6) What is the minimum clock period for this CPU? (5 points)
The maximum latency of all instructions is 1140 ps, so the minimum clock period should be 1100 ps.

6. (10 points) Modify the single-cycle processor datapath to add a proposed new assembly instruction:

```
ss rs1, rs2, immediate  #Store Sum
```

Operation: Mem[Reg[rs1]]=Reg[rs2]+immediate

The new instruction will look like S-type, while the assembler should take rs1 in the rs2 position and rs2 in the rs1 position; For all other instructions, SaveSum signal will be zero to remain their functions.

Ctrl Signals / Instruction	SaveSum	Branch	MemRead	MemtoReg	ALUOp	MemWrite	ALUSrc	RegWrite
ss	1	0	0	0	00	1	1	0

imm[11:5]	rs2	rs1	funct3	imm[4:0]	opcode
7 bits	5 bits	5 bits	3 bits	5 bits	7 bits