JOINT INSTITUTE
交大密西根学院

Ve370 Introduction to Computer Organization

Homework 8

Assigned: November 30, 2021

Due: 2:00pm on December 7, 2021

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1. (20 points) Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows parameters for a two-level cache memory.

	Size	Miss Rate	Hit Time
L1	16 KB	7.3%	1.18 ns
L2	1 MB	1.5%	5.34 ns

(1) What is the AMAT for the computer? (10 points)

Answer:

AMAT = L1 hit time + L1 miss rate * L1 miss penalty + L2 miss rate * memory access time

= 1.18 + 7.3% * 98.5% * 5.34 + 7.3% * 1.5% * 70 = 1.18 + 0.384 + 0.077 = 1.641 ns

(2) Assuming the L1 hit time determines the cycle times and a base CPI is 1.0 without any memory stalls, what is the total CPI? (10 points)

Answer: assuming only data cache is considered

L1 miss penalty = 5.34/1.18 = 5 cycles

L2 miss penalty = 70/1.18 = 60 cycles

Total CPI = base CPI + 36% * (7.3% * 98.5% * 5 + 7.3% * 1.5% * 60) = 1.15

2. (30 points) In this exercise, we will examine how replacement policies impact miss rate. Assume a 2-way set associative cache with 4 blocks. Following table gives addresses for memory access.

(1) Assuming an LRU replacement policy, how many hits does this address sequence exhibit? (10 points)

Answer:

There are 2 sets in the cache. All following block addresses map to set 1

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1	M				1	
3	M				1	3
5	M	1			5	3
1	M	3			5	1
3	M	5			3	1
1	H				3	1
3	H				3	1
5	M	1			3	5
3	H				3	5

3 hits.

(2) Assuming an MRU (most recently used) replacement policy, how many hits does this address sequence exhibit? (10 points)

Answer:

There are 2 sets in the cache. All following block addresses map to set 1

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1	M				1	
3	M				1	3
5	M	3			1	5
1	H				1	5
3	M	1			3	5
1	M	3			1	5
3	M	1			3	5
5	H				3	5
3	H				3	5

3 hits.

(3) Simulate a random replacement policy by flipping a coin. For example, “heads” means to evict the first block in a set and “tails” means to evict the second block in a set. How many hits does this address sequence exhibit? Note: you should flip the coin yourself, not by computer. (10 points)

Answer:

No standard solution to this problem because of the randomly picked block. Something like this:

Block Address of memory	Hit/Miss	Evicted Block	Contents of Cache			
			Set 0		Set 1	
1	M				1	
3	M				1	3
5	M	1			5	3
1	M	3			5	1
3	M	1			5	3
1	M	5			1	3
3	H				1	3
5	M	1			5	3
3	H				5	3

3. (50 points) Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. The following is a stream of virtual byte addresses used to access memory. Virtual addresses (in decimal): 12648, 45419, 46824, 16975, 40004, 12707, 52236
Assume 4 KB pages, a 4-entry fully associative TLB, and LRU replacement. If pages must be brought in from disk, increment to the next largest page number.

TLB:

Valid	Tag	Physical Page Number
1	11	12
1	7	4
1	3	6
0	4	9

Page Table:

Valid	Physical Page Number
1	5
0	Disk
0	Disk
1	6
1	9
1	11
0	Disk
1	4
0	Disk
0	Disk
1	3
1	12

(1) Given the virtual address stream, and the initial TLB and page table states shown above, show the final state of the system. Also list for each reference if it is a hit in the TLB, a hit in the page table, or a page fault. (15 points)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">VPN</th><th rowspan="2">Page Fault</th><th rowspan="2">TLB hit?</th><th colspan="3">TLB</th></tr>
<tr><th>Decimal</th><th>Hex</th><th>Valid</th><th>Tag</th><th>PPN</th></tr>
<tr><td rowspan="4">12648</td><td rowspan="4">0x3168</td><td rowspan="4">3</td><td rowspan="4">N</td><td rowspan="4">Y</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>0</td><td>4</td><td>9</td></tr>
<tr><td rowspan="4">45419</td><td rowspan="4">0xB16B</td><td rowspan="4">B(11)</td><td rowspan="4">N</td><td rowspan="4">Y</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>0</td><td>4</td><td>9</td></tr>
<tr><td rowspan="4">46824</td><td rowspan="4">0xB6E8</td><td rowspan="4">B(11)</td><td rowspan="4">N</td><td rowspan="4">Y</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>0</td><td>4</td><td>9</td></tr>
<tr><td rowspan="4">16975</td><td rowspan="4">0x424F</td><td rowspan="4">4</td><td rowspan="4">N</td><td rowspan="4">N</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>1</td><td>4</td><td>9</td></tr>
<tr><td rowspan="4">40004</td><td rowspan="4">0x9C44</td><td rowspan="4">9</td><td rowspan="4">Y</td><td rowspan="4">N</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>9</td><td>13</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>1</td><td>4</td><td>9</td></tr>
<tr><td rowspan="4">12707</td><td rowspan="4">0x31A3</td><td rowspan="4">3</td><td rowspan="4">N</td><td rowspan="4">Y</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>9</td><td>13</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>1</td><td>4</td><td>9</td></tr>
<tr><td rowspan="4">52236</td><td rowspan="4">0xCC0C</td><td rowspan="4">C(12)</td><td rowspan="4">Y</td><td rowspan="4">N</td><td>1</td><td>12</td><td>14</td></tr>
<tr><td>1</td><td>9</td><td>13</td></tr>
<tr><td>1</td><td>3</td><td>6</td></tr>
<tr><td>1</td><td>4</td><td>9</td></tr>
</table>

Page Table:

Index	Valid	Physical Page Number
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9

5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	1	13
10	1	3
11(B)	1	12
12(C)	1	14

(2) Repeat question (1), but this time use 16 KB pages instead of 4 KB pages. (15 points)

Address		VPN	Page Fault	TLB hit?	TLB		
Decimal	Hex				Valid	Tag	PPN
12648	0x3168	0	N	N	1	11	12
					1	7	4
					1	3	6
					1	0	5
45419	0xB16B	2	Y	N	1	2	13
					1	7	4
					1	3	6
					1	0	5
46824	0xB6E8	2	N	Y	1	2	13
					1	7	4
					1	3	6
					1	0	5
16975	0x424F	1	Y	N	1	2	13
					1	1	14
					1	3	6
					1	0	5
40004	0x9C44	2	N	Y	1	2	13
					1	1	14
					1	3	6
					1	0	5
12707	0x31A3	0	N	Y	1	2	13
					1	1	14
					1	3	6
					1	0	5
52236	0xCC0C	3	N	Y	1	2	13
					1	1	14
					1	3	6
					1	0	5

Page Table

Index	Valid	Physical Page Number
0	1	5
1	1	14
2	1	13
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
10	1	3
11	1	12

(3) What would be some of the advantages and disadvantages of having a larger page size? (5 points)

Answer:

A larger page size may reduce the page fault rate but can lead to lower utilization of the physical memory. Large page size also increases page fault penalty.

(4) Show the final contents of the TLB if it is 2-way set associative. (15 points)

Answer: 4KB page size, 12 bits of page offset, 1 bit for set index, 3 bits of tag

<table>
<tr><th colspan="2">Address</th><th rowspan="2">VPN</th><th rowspan="2">Set Index</th><th rowspan="2">Tag</th><th rowspan="2">Page Fault</th><th rowspan="2">TLB hit?</th><th colspan="4">TLB</th></tr>
<tr><th>Decimal</th><th>Hex</th><th>Index</th><th>Valid</th><th>Tag</th><th>PPN</th></tr>
<tr><td rowspan="4">12648</td><td rowspan="4">0x3168</td><td rowspan="4">3
0011</td><td rowspan="4">1</td><td rowspan="4">001(1)</td><td rowspan="4">N</td><td rowspan="4">N</td><td rowspan="2">0</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>3</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>6</td></tr>
<tr><td rowspan="4">45419</td><td rowspan="4">0xB16B</td><td rowspan="4">B(11)
1011</td><td rowspan="4">1</td><td rowspan="4">101(5)</td><td rowspan="4">N</td><td rowspan="4">N</td><td rowspan="2">0</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>5</td><td>12</td></tr>
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<tr><td rowspan="4">46824</td><td rowspan="4">0xB6E8</td><td rowspan="4">B(11)
1011</td><td rowspan="4">1</td><td rowspan="4">101(5)</td><td rowspan="4">N</td><td rowspan="4">Y</td><td rowspan="2">0</td><td>1</td><td>11</td><td>12</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>5</td><td>12</td></tr>
<tr><td>1</td><td>1</td><td>6</td></tr>
<tr><td rowspan="4">16975</td><td rowspan="4">0x424F</td><td rowspan="4">4
0100</td><td rowspan="4">0</td><td rowspan="4">010(2)</td><td rowspan="4">N</td><td rowspan="4">N</td><td rowspan="2">0</td><td>1</td><td>2</td><td>9</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>5</td><td>12</td></tr>
<tr><td>1</td><td>1</td><td>6</td></tr>
<tr><td rowspan="4">40004</td><td rowspan="4">0x9C44</td><td rowspan="4">9
1001</td><td rowspan="4">1</td><td rowspan="4">100(4)</td><td rowspan="4">Y</td><td rowspan="4">N</td><td rowspan="2">0</td><td>1</td><td>2</td><td>9</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>5</td><td>12</td></tr>
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0011</td><td rowspan="4">1</td><td rowspan="4">001(1)</td><td rowspan="4">N</td><td rowspan="4">N</td><td rowspan="2">0</td><td>1</td><td>2</td><td>9</td></tr>
<tr><td>1</td><td>7</td><td>4</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>4</td><td>13</td></tr>
<tr><td rowspan="4">52236</td><td rowspan="4">0xCC0C</td><td rowspan="4">C(12)
1100</td><td rowspan="4">0</td><td rowspan="4">110(6)</td><td rowspan="4">Y</td><td rowspan="4">N</td><td rowspan="2">0</td><td>1</td><td>2</td><td>9</td></tr>
<tr><td>1</td><td>6</td><td>14</td></tr>
<tr><td rowspan="2">1</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>1</td><td>4</td><td>13</td></tr>
</table>

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0	1	5
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5	1	11
6	0	Disk

7	1	4
8	0	Disk
9	0	13
10	1	3
11	1	12
12	1	14