# Ve370 Introduction to Computer Organization

Homework 2

楊毅文 519370910053

# Assigned: September 30, 2021

**Due: 2:00pm on October 12, 2021 Submit a PDF file on Canvas**

1. (5 points) Following memory location has address 0x0F000000 and content 0x15C78933.

0 1 2 3

0x0F000000

|  |  |  |  |
| --- | --- | --- | --- |
| 33 | 89 | C7 | 15 |

Write RISC-V assembly instructions to load the byte C7 as a signed number into register x20, then show the content of x20 after the operations.

1. (10 points) The RISC-V assembly program below computes the factorial of a given input n (n!). The integer input is passed through register x12, and the result is returned in register x10. In the assembly code below, there are a few errors. Correct the errors.

FACT: addi sp, sp, 8 sw x1, 4(sp) sw x12, 0(sp)

add x18, x0, x12 addi x5, x0, 2 bge x12, x5, L1 mul x10, x18, x10 addi sp, sp, -8 jalr x0, 0(x1)

L1: addi x12, x12, -1 jal x1, FACT

addi x10, x0, 1 lw x12, 4(sp) lw x1, 0(sp) addi sp, sp, -8 jalr x0, 0(x1)

1. (10 points) Consider a proposed new instruction named rpt. This instruction combines a loop’s condition check and counter decrement into a single instruction. For example,

rpt x29, loop

would do the following:

if (x29 > 0) { x29=x29−1;

goto loop;

}

* 1. (5 points) If this instruction were to be added to the RISC-V instruction set, what is the most appropriate instruction format?
  2. (5 points) What is the shortest sequence of RISC-V instructions that performs the same operation?

1. (7 points) Given a 32-bit RISC-V machine instruction:

1111 1111 0110 1010 0001 1010 1110 0011

* 1. (6 points) What does the assembly instruction do?
  2. (1 point) What type of instruction is it?

1. (6 points) Given RISC-V assembly instruction:

lw x21, -32(sp)

* 1. (5 points) What is the corresponding binary representation?
  2. (1 point) What type of instruction is it?

1. (12 points) If the RISC-V processor is modified to have 128 registers rather than 32 registers:
   1. (4 points) show the bit fields of an R-type format instruction assuming opcode and func fields are not changed.
   2. (4 points) What would happen to the I-type instruction if we want to keep the total number of bits for an instruction unchanged?
   3. (4 points) What is the impact on the range of addresses for a beq instruction? Assume all instructions remain 32 bits long and the size of opcode and func fields don’t change.
2. (15 points) Convert the following assembly code fragment into machine code, assuming the memory location of the first instruction (LOOP) is 0x1000F400

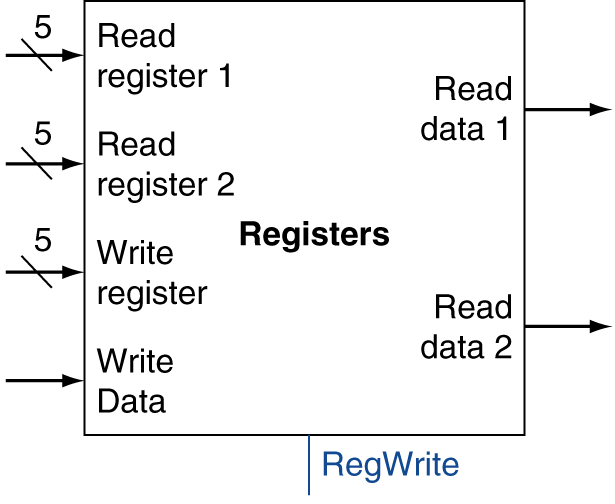
LOOP: blt x0, x5, ELSE

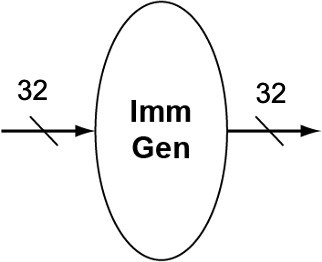
jal x0, DONE ELSE: addi x5, x5, -1

addiu x25, x25, 2 jal x0, LOOP

DONE: …

1. (15 points) Model the Register File component shown below in Verilog HDL. Show source code and screen shots of simulation results.



1. (20 points) Model the following Immediate Generator component in Verilog HDL. Show source code, and simulation results of one instruction for each type involving immediate numbers.