CyberSecurity Club at San Francisco State University

Initial Design Document

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Abstract

This research focuses on designing and implementing a secure MISC device that will be built to adhere to the standards of the functional and security requirements. Our design will aim to withstand all attack scenarios presented by the MITRE documentation, as well as provide a new approach to embedded system programming with the popular and recent memory-safe Rust programming language.

1. Introduction

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2. Functional Requirements

We plan to meet the functional requirements by doing x, y, and z.

3. Security Requirements

3.1. Security Requirement 1

Security Requirement 1 (**SR1**) requires us to ensure the Application Processor will not boot unless expected components are present and valid. Our plan for this involves a two-pronged approach which uses public/private key encryption and a secure cryptographic nonce.

During the build process, we will generate a public/private key pair. The public key will be flashed onto the components, and the private key will be stored in the application processor. Additionally, a random seed will be generated using /dev/urandom and stored in the application processor. This seed will be used by the components and the application processor to generate and validate cryptographic nonces.

The components will use the public key to encrypt the nonce along with their own unique identifier and send it back to the application processor over I2C bus. The application processor will use the private key to decrypt the nonce and verify that it matches the original nonce. If the nonces match, the application processor will know that the components are valid and will continue with boot. If no message is received, or the nonces do not match, the application processor will not boot.

3.2. Security Requirement 2

Security Requirement 2 (**SR2**) requires us to ensure that the components will not boot until commanded to do so by an Application Processor that has validated the integrity of the system. Our plan to meet this requirement is much the same as the plan for Security Requirement 1, but in reverse.

During the build process, a random seed will be burned onto the firmware as delineated in SR1. In addition, each component will receive a public/private key pair similar to the AP's. This key will be used to encrypt messages before transmitting them over the I2C bus, as well as to verify digital signatures.

After the application processor verifies the message sent by the components as delineated in SR1, it will return an acknowledgement, encrypted with the component's public key. Upon receipt of this acknowledgement, the component will use its private key to decrypt the message and validate its digital signature. From there, the nonce will be checked against the random key generator. If the message is not present, the digital signature is invalid, or the nonce verification fails, the component will immediately halt the boot process. Conversely, if all checks pass - suggesting the AP successfully validated the components - the component will proceed with the boot sequence.

References

[1] S. Scholes, Discuss. Faraday Soc. No. 50 (1970) 222.

[2] O.V. Mazurin and E.A. Porai-Koshits (eds.),

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