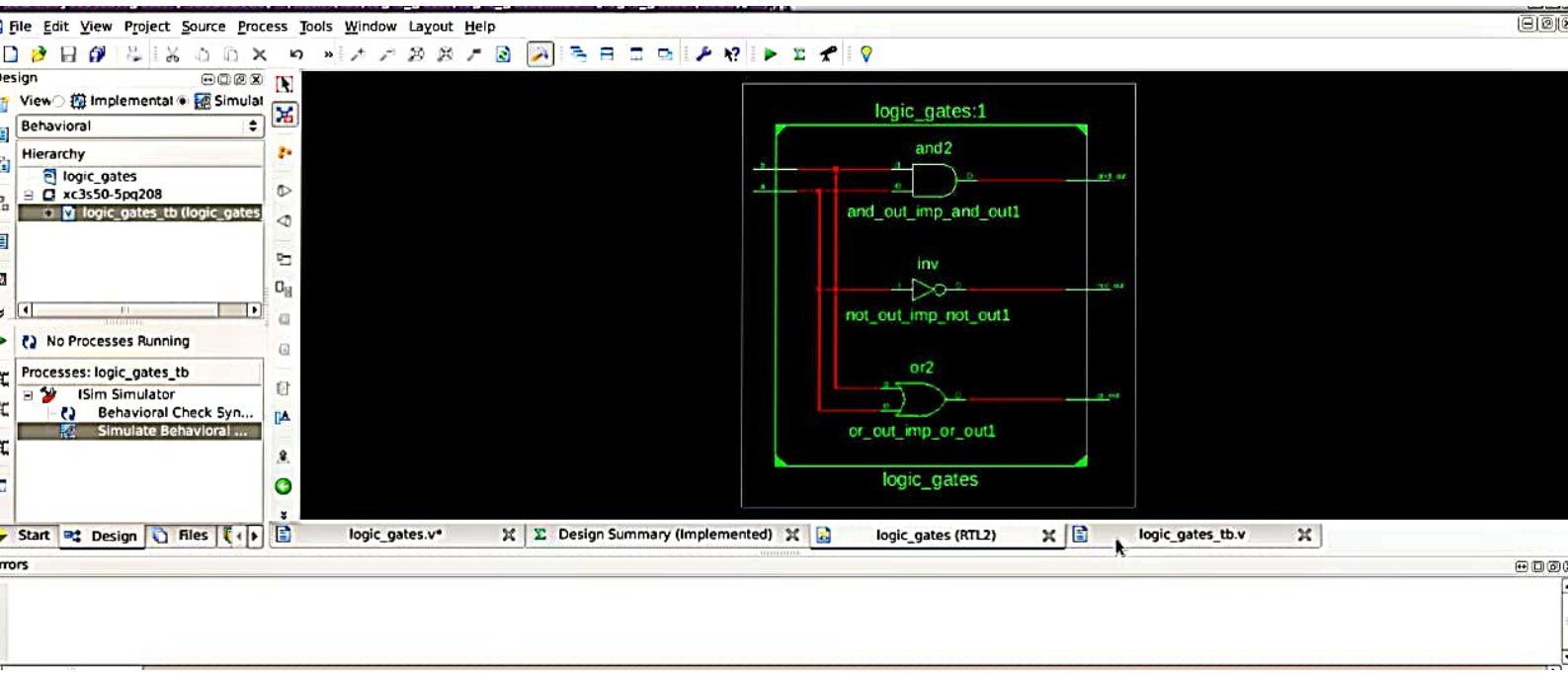
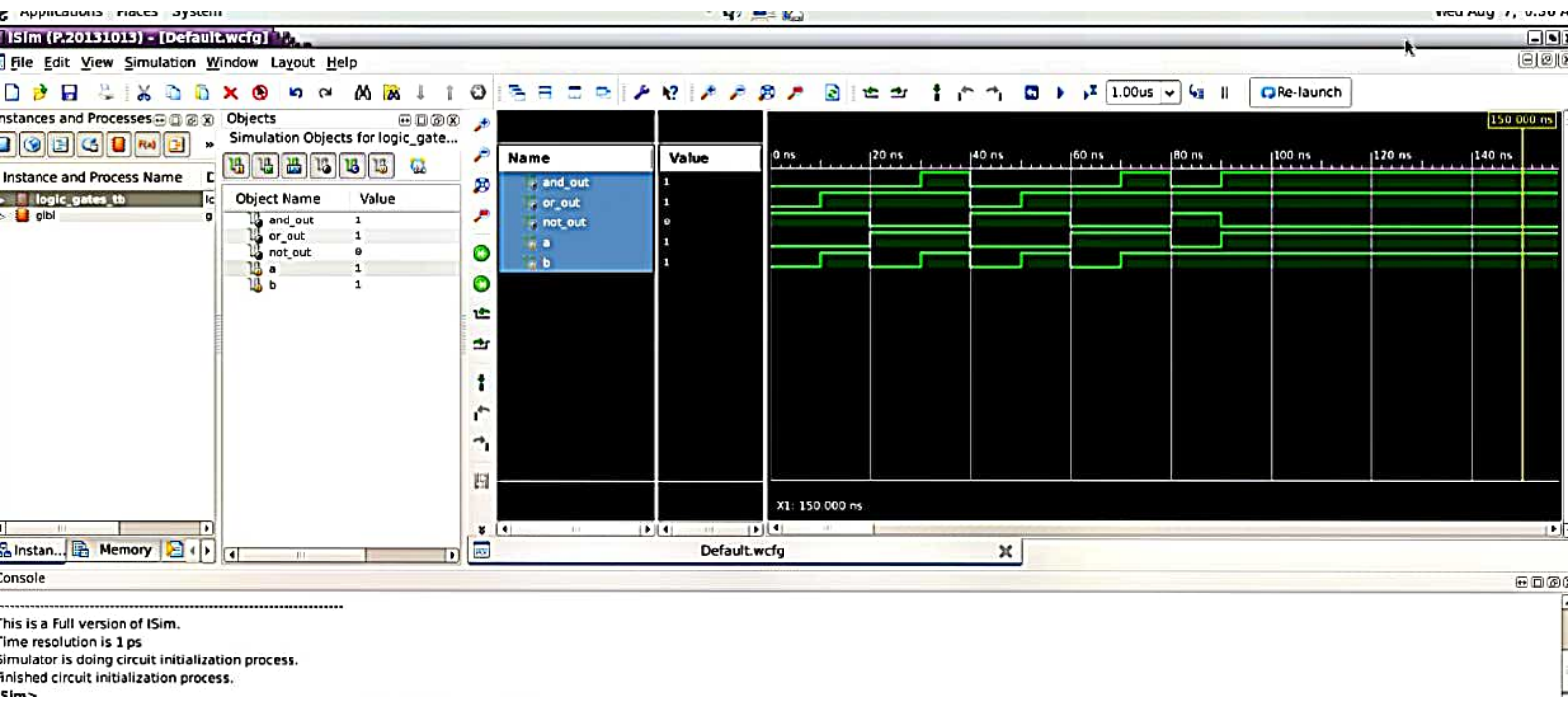
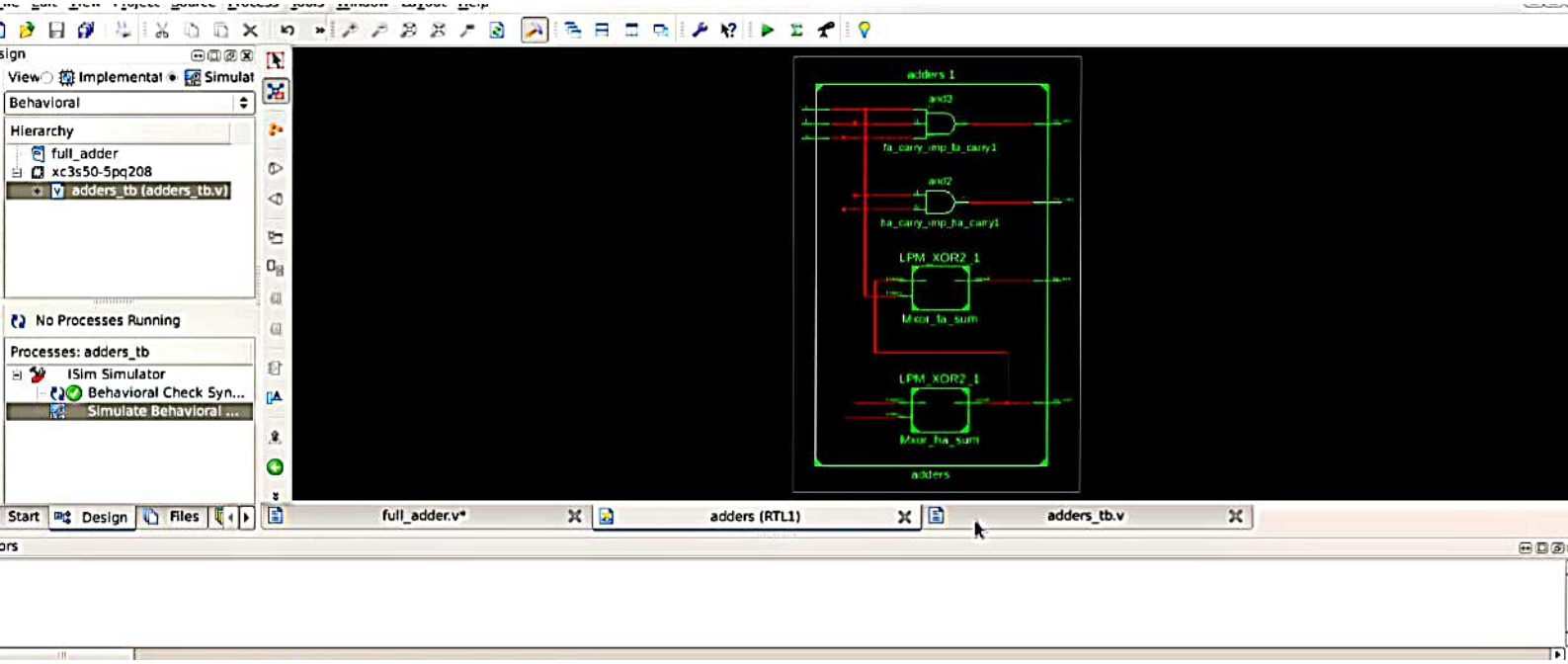
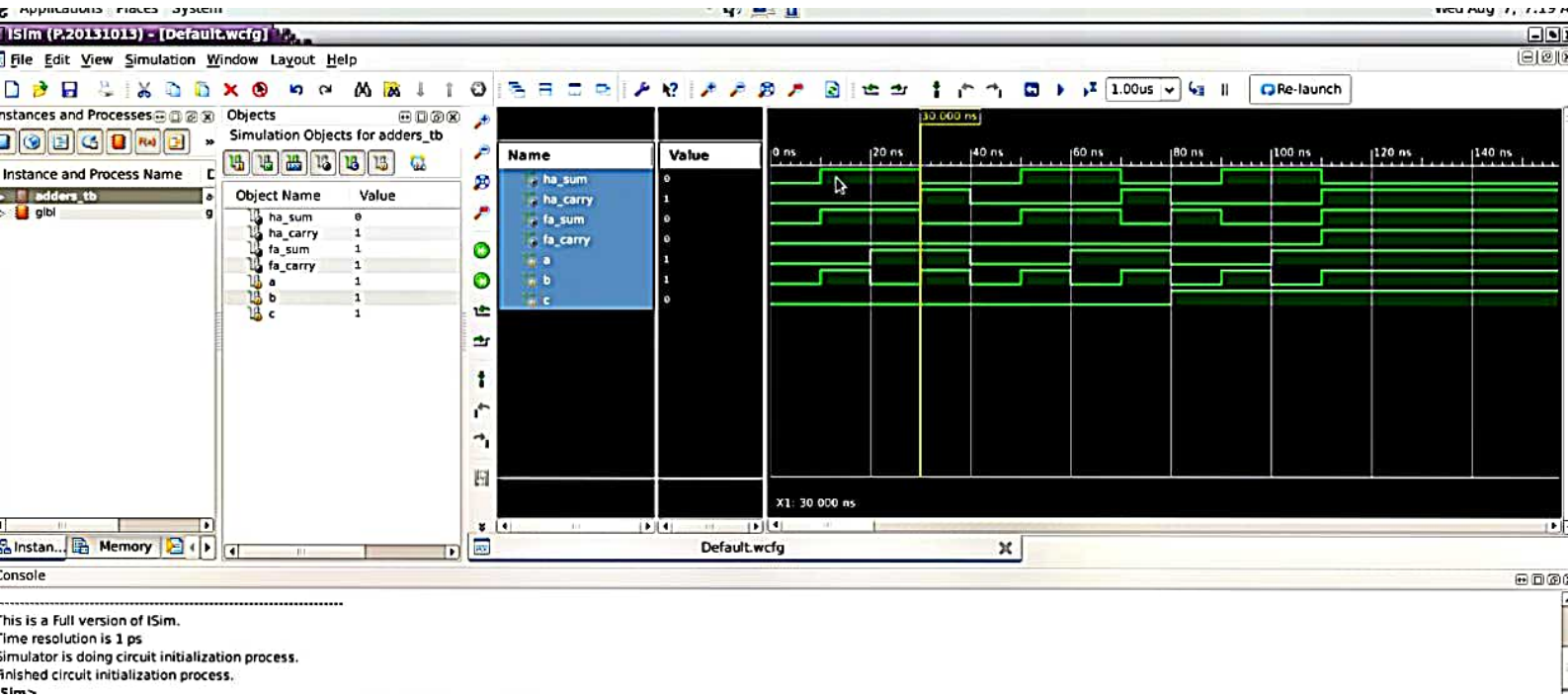
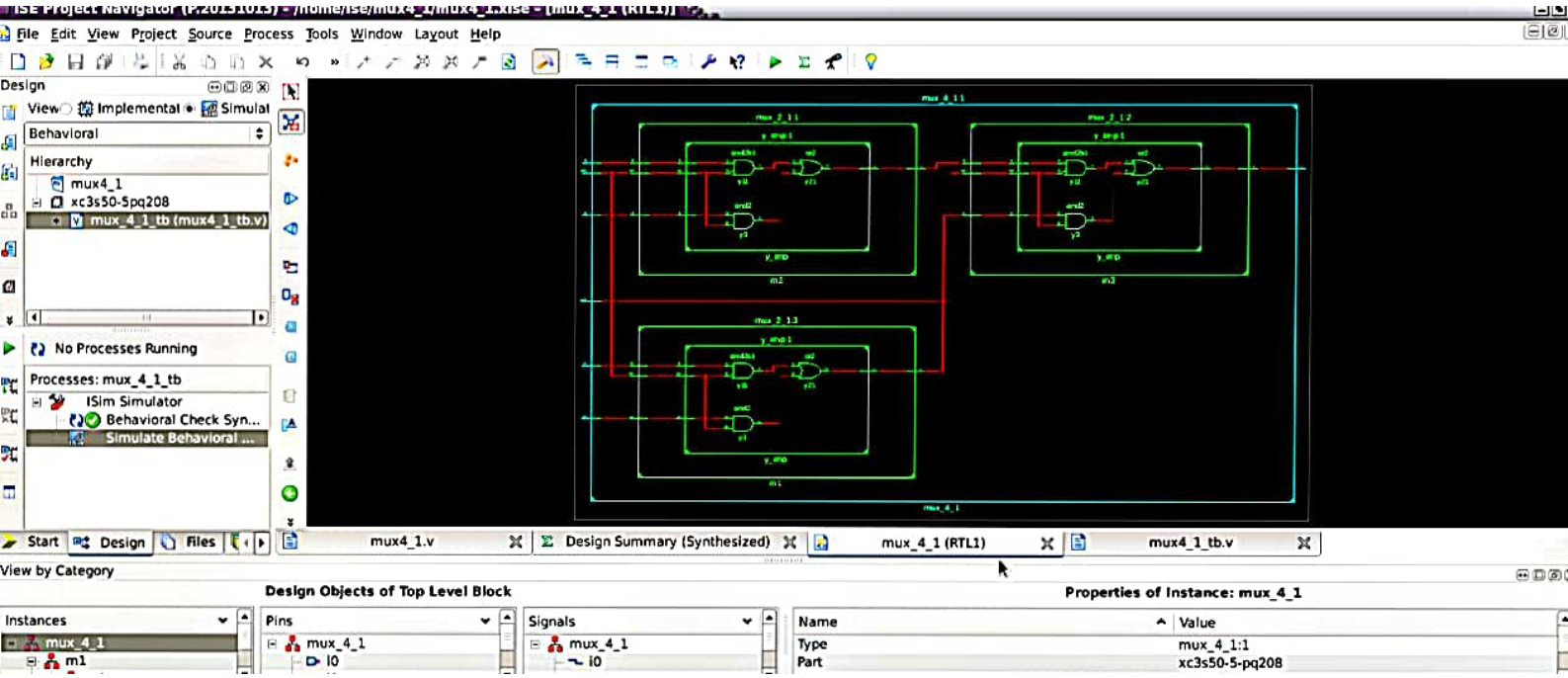
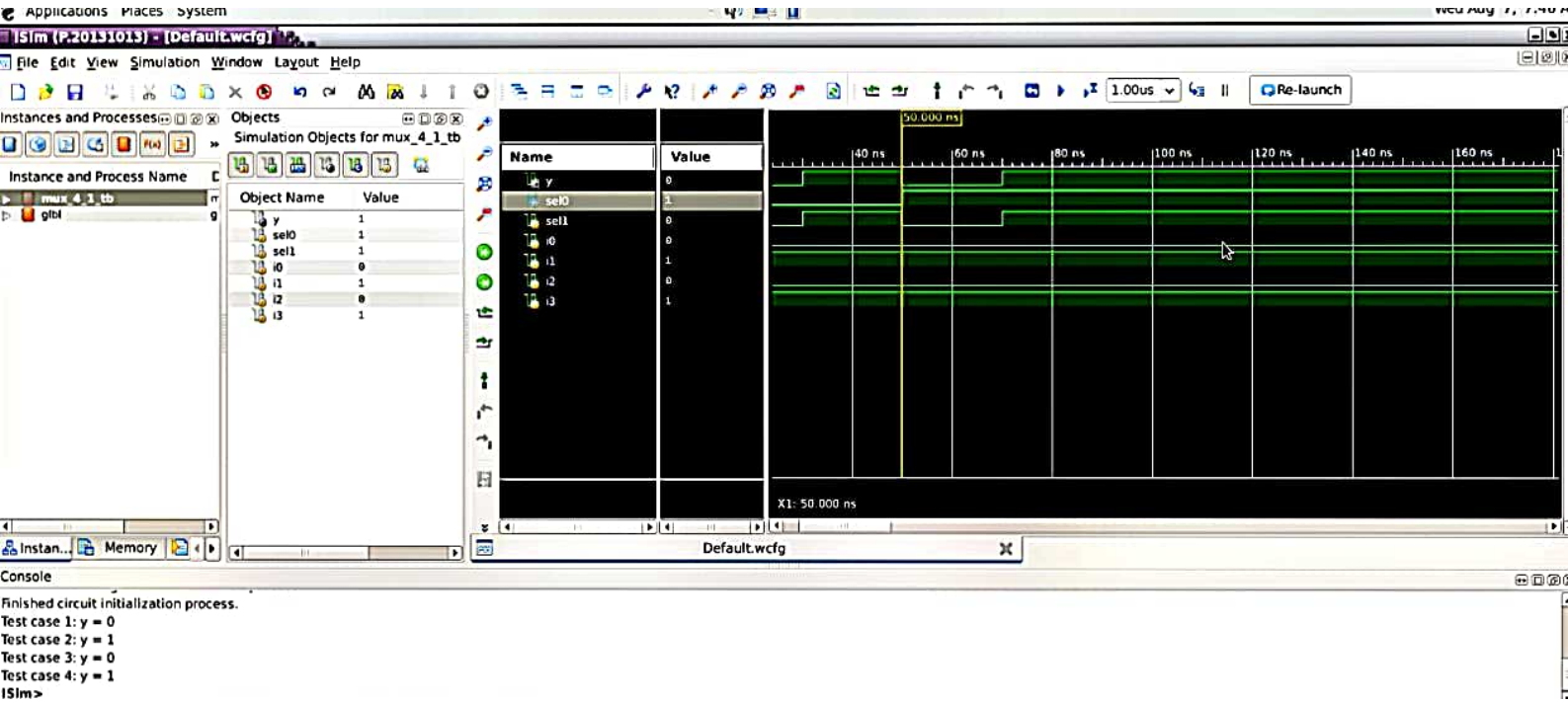

File Edit View Project Source Process Tools Window Layout Help
View Implemental Simulat
Behavioral
Hierarchy
logic_gates
xc3s50-5pq208
logic_gates_tb (logic_gates
No Processes Running
Processes: logic_gates_tb
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start
Design
Files
logic_gates:1
and2
and_out_imp_and_out1
inv
not_out_imp_not_out1
or2
or_out_imp_or_out1
logic_gates
logic_gates.v*
Design Summary (Implemented)
logic_gates (RTL2)
logic_gates_tb.v
rrors

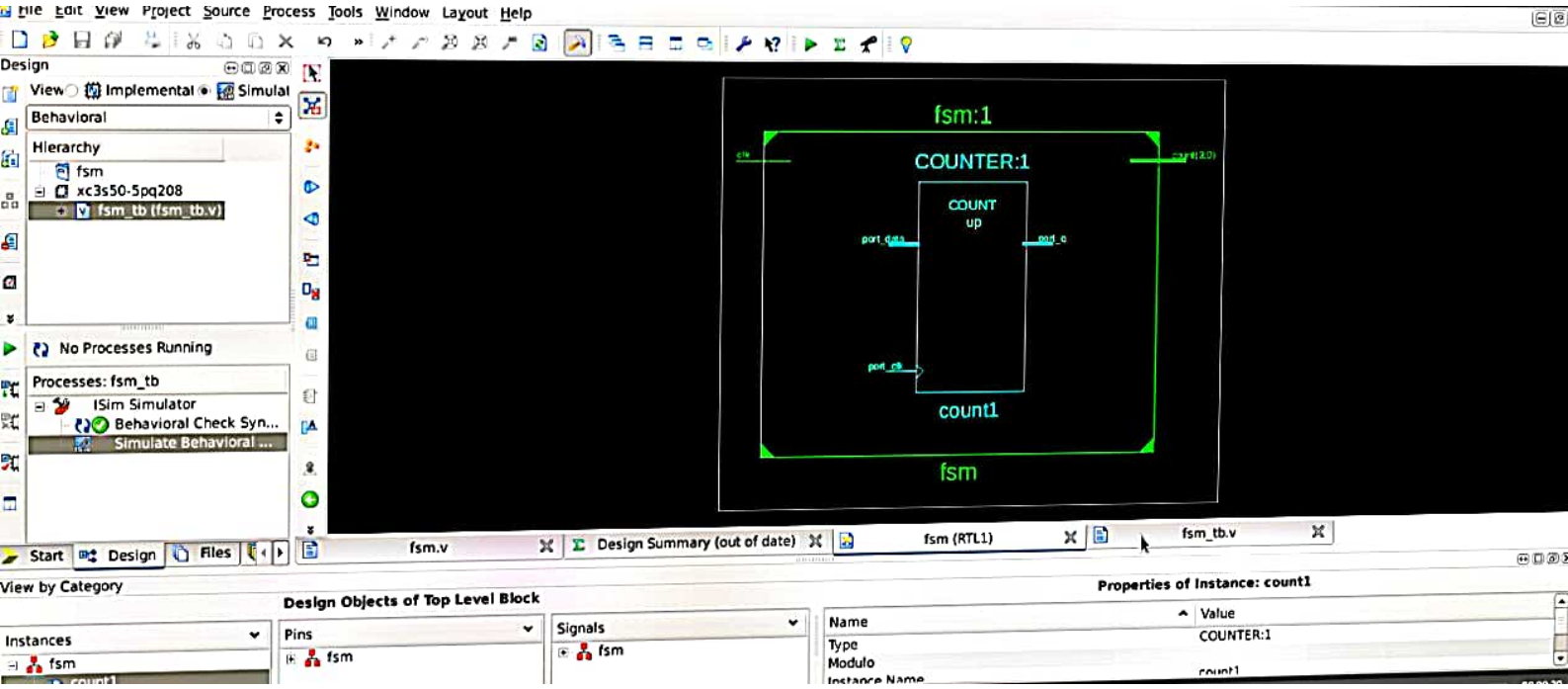

ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
logic_gates_tb
glbl
Objects
Simulation Objects for logic_gate...
Object Name
Value
and_out 1
or_out 1
not_out 0
a 1
b 1
Name
Value
and_out
or_out
not_out
a
b
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
150.000 ns
X1: 150.000 ns
Default.wcfg
Memory
Console
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.

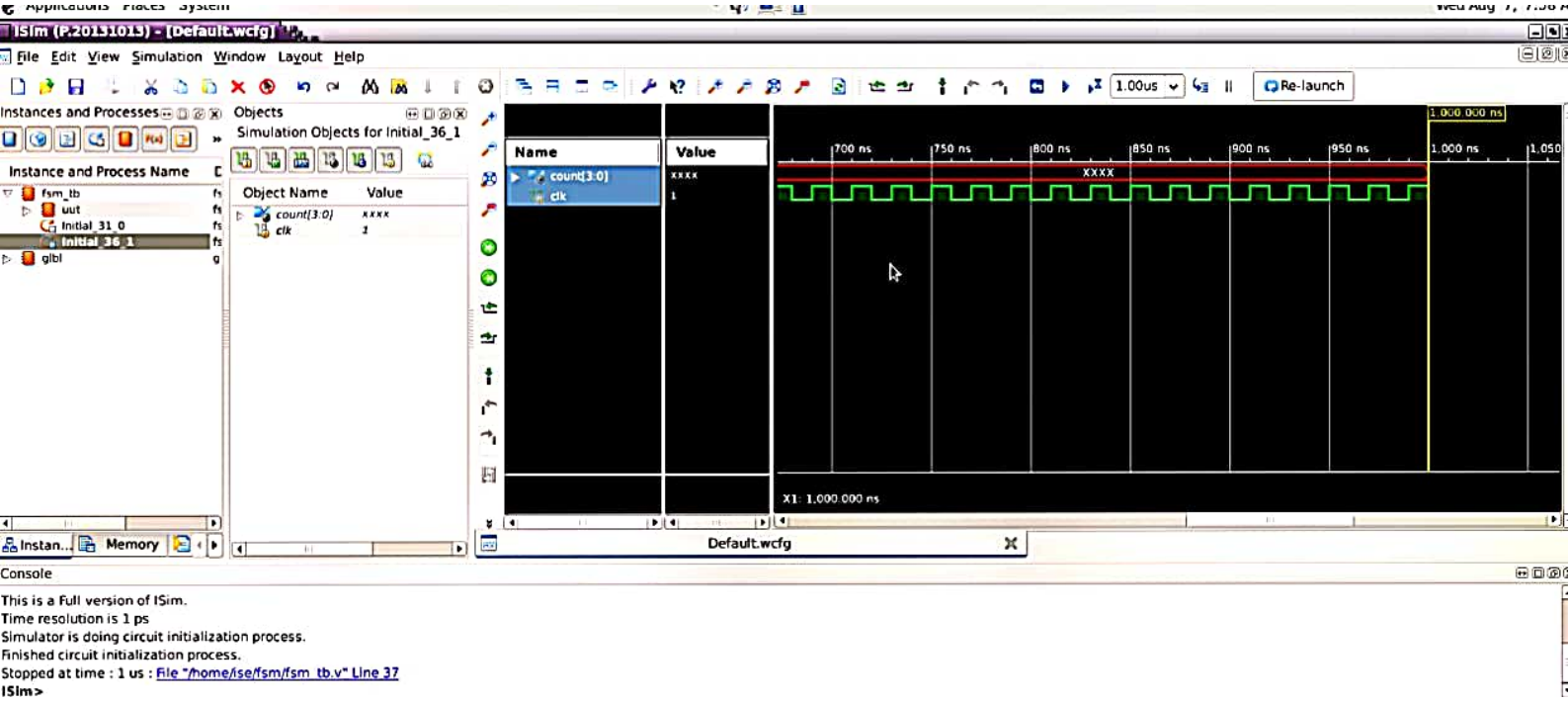

sign
View
Implemental
Simulat
Behavioral
Hierarchy
full_adder
xc3s50-5pq208
adders_tb (adders_tb.v)
No Processes Running
Processes: adders_tb
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start
Design
Files
adders 1
and2
ha_carry_imp_ha_carry1
and2
ha_carry_imp_ha_carry1
LPM_XOR2_1
Mxor_fa_sum
LPM_XOR2_1
Mxor_ha_sum
adders
full_adder.v*
adders (RTL1)
adders_tb.v


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
adders_tb
glbl
Objects
Simulation Objects for adders_tb
Object Name
Value
ha_sum 0
ha_carry 1
fa_sum 1
fa_carry 1
a 1
b 1
c 1
Name
Value
ha_sum
ha_carry
fa_sum
fa_carry
a
b
c
30 000 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
X1: 30 000 ns
Memory
Default.wcfg
Console
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.


File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Behavioral
Hierarchy
mux4_1
xc3s50-5pq208
mux_4_1_tb (mux4_1_tb.v)
No Processes Running
Processes: mux_4_1_tb
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start
Design
Files
mux4_1.v
Design Summary (Synthesized)
mux_4_1 (RTL1)
mux4_1_tb.v
View by Category
Design Objects of Top Level Block
Properties of Instance: mux_4_1
Instances
mux_4_1
m1
Pins
mux_4_1
I0
Signals
mux_4_1
i0
Name
Value
Type
mux_4_1:1
Part
xc3s50-5-pq208


Applications Places System
ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
Instances and Processes
Instance and Process Name
mux_4_1_tb
glbl
Objects
Simulation Objects for mux_4_1_tb
Object Name
Value
y 1
sel0 1
sel1 1
i0 0
i1 1
i2 0
i3 1
Name
Value
y 0
sel0 1
sel1 0
i0 0
i1 1
i2 0
i3 1
50.000 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
X1: 50.000 ns
Instan...
Memory
Default.wcfg
Console
Finished circuit initialization process.
Test case 1: y = 0
Test case 2: y = 1
Test case 3: y = 0
Test case 4: y = 1
ISim>


File Edit View Project Source Process Tools Window Layout Help
Design
View: Implemental Simulat
Behavioral
Hierarchy
fsm
xc3s50-5pq208
fsm_tb (fsm_tb.v)
No Processes Running
Processes: fsm_tb
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
Start
Design
Files
fsm:1
COUNTER:1
COUNT
up
count1
fsm
fsm.v
Design Summary (out of date)
fsm (RTL1)
fsm_tb.v
View by Category
Design Objects of Top Level Block
Properties of Instance: count1
Instances
Pins
Signals
Name
Value
Type
COUNTER:1
Modulo


ISim (P.20131013) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
fsm_tb
uut
Initial_31_0
Initial_36_1
glbl
Objects
Simulation Objects for Initial_36_1
Object Name
Value
count[3:0]
clk
Name
Value
700 ns
750 ns
800 ns
850 ns
900 ns
950 ns
1.000 ns
1.050
XXXX
X1: 1,000.000 ns
Default.wcfg
Memory
Console
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Stopped at time : 1 us : File "/home/ise/fsm/fsm_tb.v" Line 37
ISim>