Experiment No.02

Name of the Experiment: Realization of Basic gates using Universal Gates.

Objective:

To construct NOT, AND, OR, Exclusive OR (EX-OR), Exclusive NOR (EX-NOR) logic gates using only NAND gates.

To construct NOT, AND, OR, Exclusive OR (EX-OR), Exclusive NOR (EX-NOR) logic gates using only NOR gates.

Components required:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	NAND GATE 2 I/P	IC 7400	1
2.	NOR GATE 2 I/P	IC 7402	1
3.	IC TRAINER KIT		1
4.	PATCH CORD		

(A) NAND AS A UNIVERSAL GATE:

THEORY:

NAND gate is actually a combination of two logic gates: AND gate followed by NOT gate. So its output is complement of the output of an AND gate. This gate can have minimum two inputs, output is always one. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR, NOR. So this gate is also called universal gate.

1. NAND gate as NOT gate:

A NOT produces complement of the input. It can have only one input, tie the inputs of a NAND gate together. Now it will work as a NOT gate. Its output is

$$Y = (A.A)' = (A)'$$

2. NAND gates as AND gate:

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

$$Y = ((A.B)')' = (A.B)$$

3. NAND gates as OR gate:

From De Morgan's theorems: (A.B)' = A' + B'. Similarly, (A'.B')' = A'' + B'' = A+ B.

So, give the inverted inputs to a NAND gate, obtain OR operation at output.

4. NAND gates as EX-OR gate:

The output of a two input EX-OR gate is given by: Y = A'B + AB'. EX-OR gate can be implemented using four NAND gates as follows.

Gate No.	Inputs	Output
1	A, B	(AB)'
2	A, (AB)'	(A (AB)')'
3	(AB)', B	(B (AB)')' A'B +
4	(A (AB)')', (B (AB)')'	AB'

Now the output from gate no. 4 is the overall output of the configuration.

Y = ((A (AB)')' (B (AB)')')'

= (A (AB)')'' + (B (AB)')''

= (A (AB)') + (B (AB)')

= (A (A' + B)') + (B (A' + B'))

= (AA' + AB') + (BA' + BB')

= (0+AB'+BA'+0)

= AB' + BA'

So, Y = AB' + A'B

5. NAND gates as EX-NOR gate

EX-NOR gate is actually EX-OR gate followed by NOT gate. So give the output of EX-OR gate to a NOT gate, overall output is that of an EX-NOR gate.

Y = AB+ A'B'

PROCEDURE:

(i) Verify the gates and connect the NAND gates as per logic diagrams (A) for any of the logic functions to be realized.

(ii) Connect Pin-14 of all ICs to +5V and Pin-7 to ground.

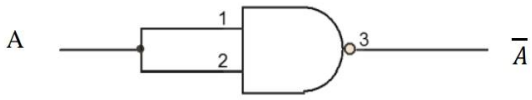
(iii) Feed the logic 0 (0V) or 1(5V) in different combinations at the inputs A & B according to truth table.

(iv) Observe and note down the output readings for Y for different combinations of inputs and verify the truth table for input/output combination

(v) Repeat the process for all logic functions/gates.

Logic diagrams (A) observations table (A)

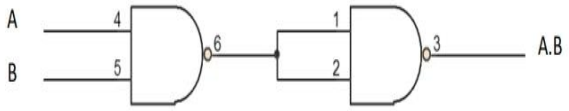
1. *NAND gate as NOT gate:*



A	Y
0	1
1	0

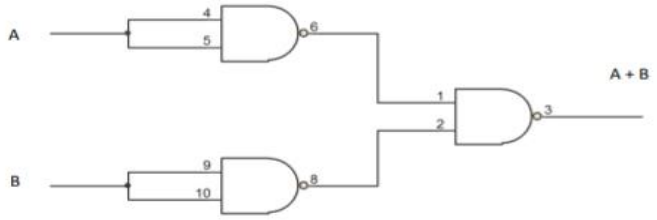
2. *NAND gates as AND gate:*

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



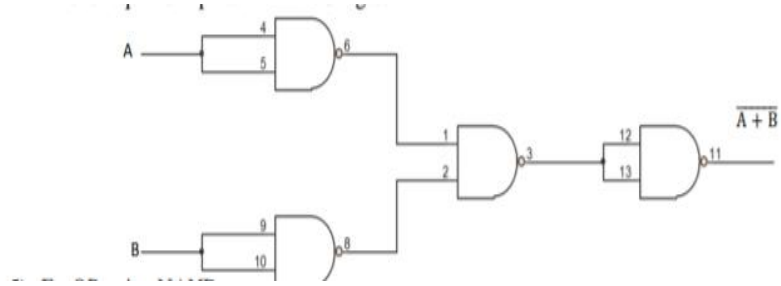
3. NAND gates as OR gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



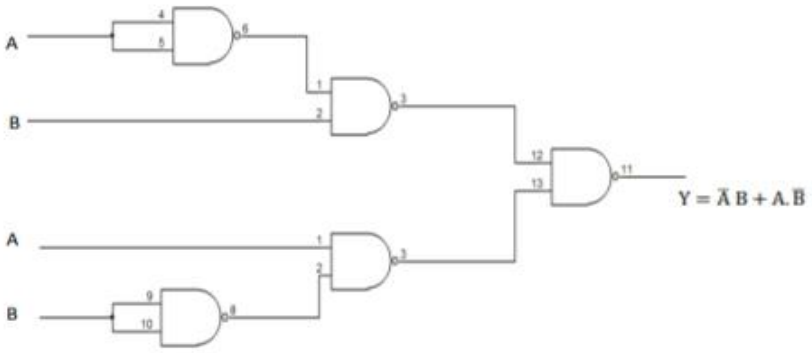
4. NAND gates as EX-OR gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



5. NAND gates as EX-NOR gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



(B) NOR AS A UNIVERSAL GATE:
THEORY:

NOR gate is actually a combination of two logic gates: OR gate followed by NOT gate. So its output is complement of the output of an OR gate. This gate can have minimum two inputs, output is always one. By using only NOR gates, we can realize all logic functions: AND, OR, NOT, X-OR, X-NOR , NAND. So this gate is also called universal gate.

1. NOR gate as NOT gate:

A NOT produces complement of the input. It can have only one input, tie the inputs of a NOR gate together. Now it will work as a NOT gate. Its output is

Y = (A+A)' = (A)'

2. NOR gates as OR gate:

A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

Y = ((A+B)')'= (A+B)

3. NOR gates as AND gate:

From De Morgan's theorems: (A+B)' = A'. B'. Similarly, (A'+B')' = A''. B'' = A .B So, give the inverted inputs to a NOR gate, obtain AND operation at output.

4. NOR gates as EX-NOR gate:

The output of a two input EX-NOR gate is given by: Y = AB + A'B'. EX-NOR gate can be implemented using four NOR gates as follows.

Gate No.	Inputs	Output
1	A, B	(A + B)’
2	A, (A + B)’	(A +(A+B)’)’
3	(A + B)’, B	(B + (A+B)’)’
4	(A + (A + B)’)’, (B + (A+B)’)’	AB + A’B’

Now the output from gate no. 4 is the overall output of the configuration.

Y =((A + (A+B)’)’ (B +(A+B)’)’)’
= (A+(A+B)’)’’.(B+(A+B)’)’’
= (A+(A+B)’).(B+(A+B)’)
= (A+A’B’).(B+A’B’)
= (A + A’).(A + B’).(B+A’)(B+B’)
= 1.(A+B’).(B+A’).1
= (A+B’).(B+A’)
= A.(B + A’) +B’.(B+A’)
= AB + AA’ +B’B+B’A’
= AB+0+0+B’A’
= AB + B’A’

So Y = AB + A’B’

5. NOR gates as EX-OR gate

EX-OR gate is actually EX-NOR gate followed by NOT gate. So give the output of EX-NOR gate to a NOT gate, overall output is that of an EX-OR gate.

Y = A’B+ AB’

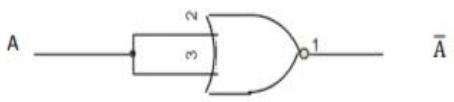
PROCEDURE:

(i) Verify the gates and connect the NOR gates as per logic diagrams (B) for any of the logic functions to be realized.
(ii) Connect Pin-14 of all ICs to +5V and Pin-7 to ground.
(iii) Feed the logic 0 (0V) or 1(5V) in different combinations at the inputs A & B according to truth table.
(iv) Observe and note down the output readings for Y for different combinations of inputs and verify the truth table for input/output combination
(v) Repeat the process for all logic functions/gates

LOGIC DIAGRAMS (B):

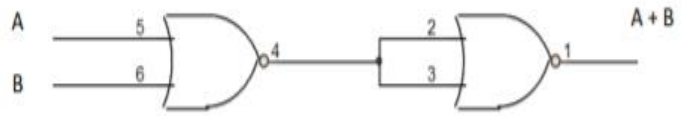
1. NOR gate as NOT gate:

A	Y
0	1
1	0



2. NOR gates as OR gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



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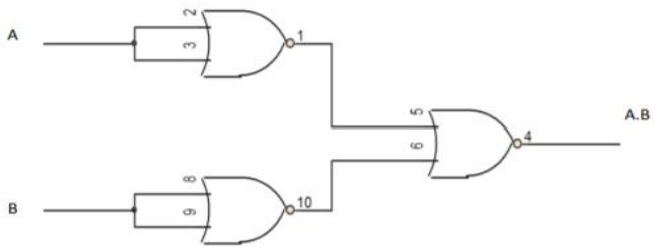
3. NOR gates as AND gate:

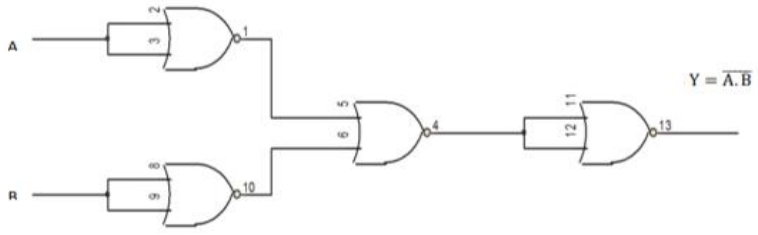
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



4. NOR gates as EX-NOR gate:

A	B	Y
0	0	0
0	1	1
1	0	1

1	1	0



5. NOR gates as EX-OR gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

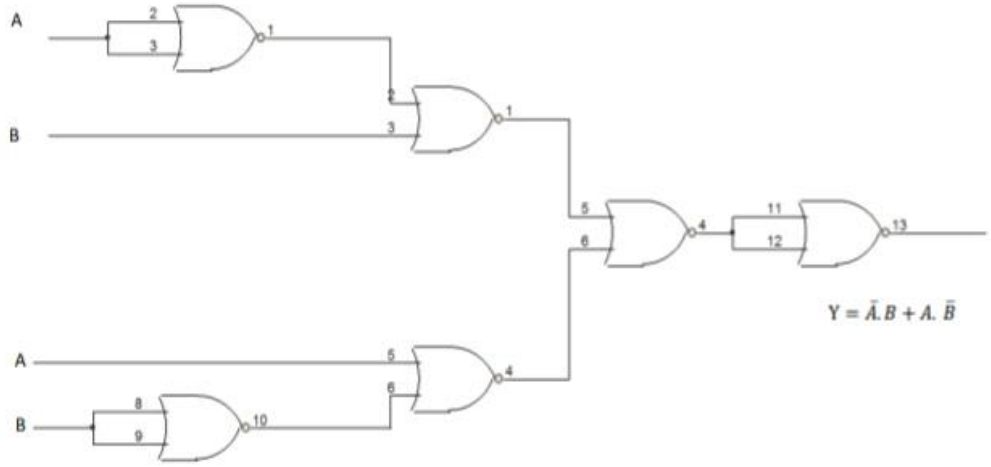
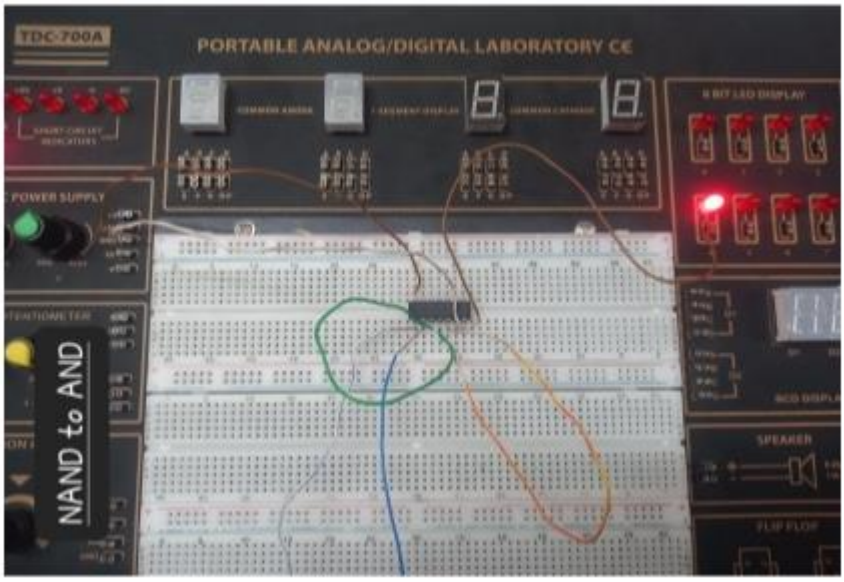
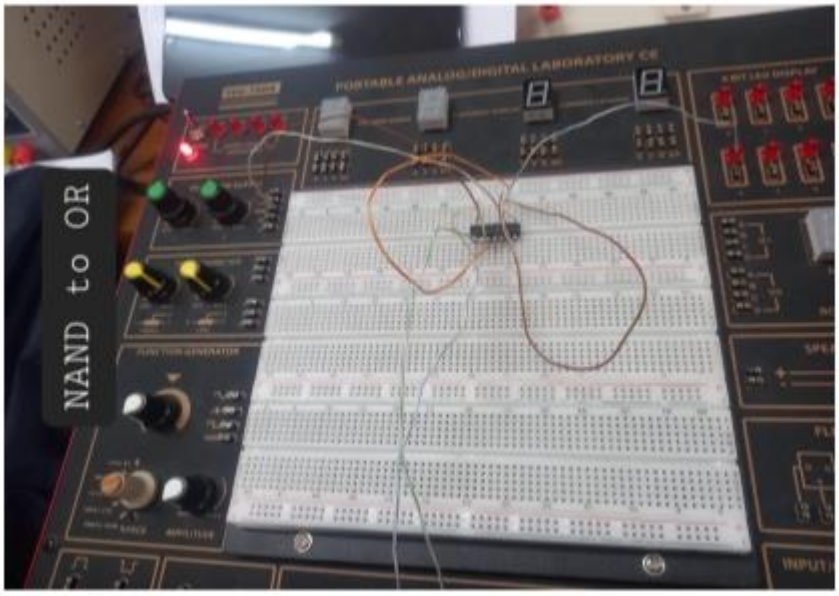


DIAGRAM:





Result:

We used IC and connecting wires to implement the connections in the bread board . In this experiment we used IC7400 for connection . After connecting the wires with the IC perfectly we got the accurate result.in the IC we connected the 7 no pin with the ground and 14 no. pin

for input voltage .While implementing there were some errors due to wrong wire connection and some fault in the breadboard.

Conclusion:

All the gates are realized using NAND and NOR gates and truth table are verified.