**Experiment No. 05**

**Name of the experiment**: Parity generator and Checker.

**Objective:** To design and verify the truth table of a three-bit odd parity generator and checker.

**COMPONENTS REQUIRED:**

IC Trainer kit, IC 7400 x2, IC 7486 x1

**THEORY:**

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1’s either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker. In even parity the added parity bit will make the total number of 1’s an even amount and in odd parity the added parity bit will make the total number of 1’s an odd amount. In a three-bit odd parity generator the three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit. The parity checker circuit checks for possible errors in the transmission. Since the information was transmitted with odd parity the four bits received must have an odd number of 1’s. An error occurs during the transmission if the four bits received have an even number of 1’s, indicating that one bit has changed during transmission. The output of the parity checker is denoted by PEC (parity error check) and it will be equal to 1 if an error occurs, i.e., if the four bits received has an even number of 1’s. The parity bit is only for checking errors not for correction.

**TRUTH TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
| **INPUTS**  (Three bit messages) | | | **OUTPUT**  (Odd Parity bit) |
| **A** | **B** | **C** | **P** |
| **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **0** |

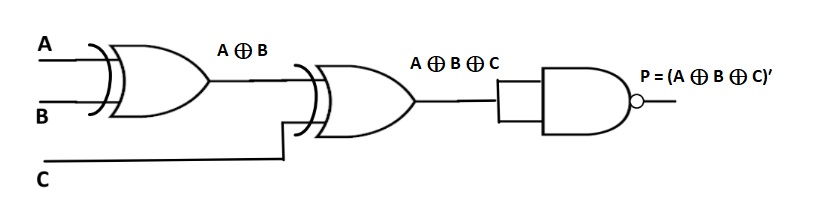
From the truth table the expression for the output parity bit is, P (A, B, C) = Σ m (0, 3, 5, 6)

Also written as,

**P=A’B’C’+A’BC+AB’C+ABC’**

**P = (A ⊕ B ⊕ C)′**

**CIRCUIT DIAGRAM:** Odd Parity Generator



**ODD Parity Checker:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **INPUTS**  (Four bit message Received) | | | | **OUTPUT**  (Parity error Check) |
| **A** | **B** | **C** | **P** | **X** |
| **0** | **0** | **0** | **0** | **1** |
| **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** |
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| **1** | **0** | **0** | **1** | **1** |
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| **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |

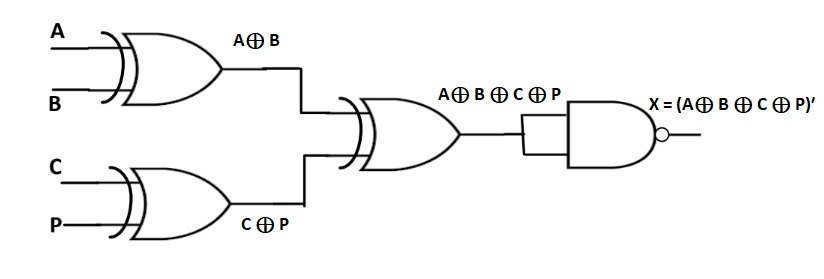
From the truth table the expression for the output parity checker bit is,

**X (A, B, C,P) = Σ (0, 3, 5, 6, 9, 10 ,12, 15 )**

The above expression is reduced as,

**X = (A⊕ B ⊕ C ⊕ P)′**

**CIRCUIT DIAGRAM:** Odd Parity Checker



**Procedure:**

1. You established the necessary connections according to circuit diagrams.
2. For all integrated circuits (ICs) involved, you grounded the 7th pin and supplied +5V to the 14th pin.
3. You applied inputs to the circuits and verified the truth table for both the Parity generator and checker circuits.

**Discussion:**

1. You successfully generated parity and verified it using your teacher's guidance.
2. Your teacher verified the output of your experiment, indicating that the results were accurate and valid.
3. You found the experiment to be exciting and noted that it provided a valuable learning experience.
4. You mentioned that you learned how to generate parity and check for parity errors during the experiment.

Overall, it's clear that the experiment was both educational and engaging, allowing you to gain practical experience in the field of parity generation and error checking. This hands-on experience can be valuable in understanding how these concepts work in real-world applications.