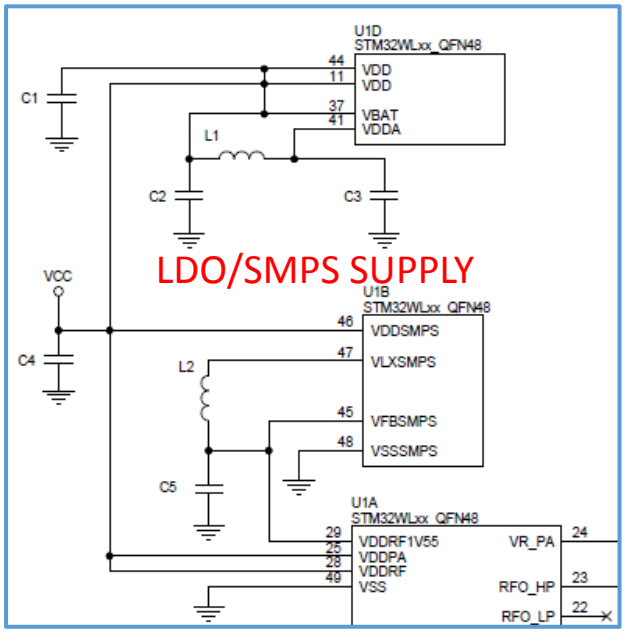
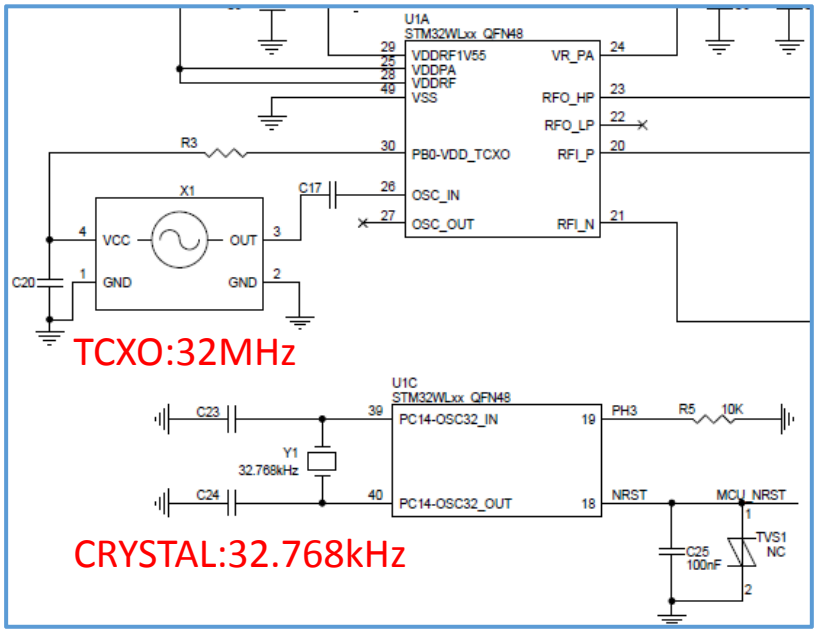
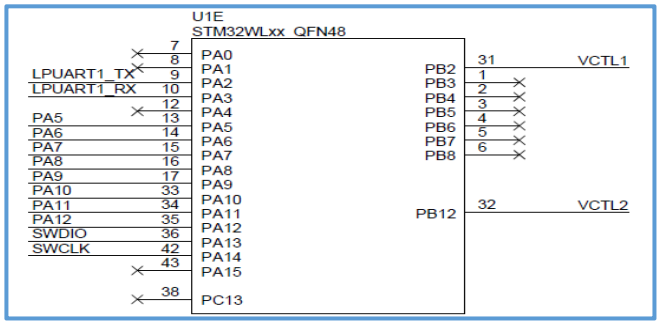
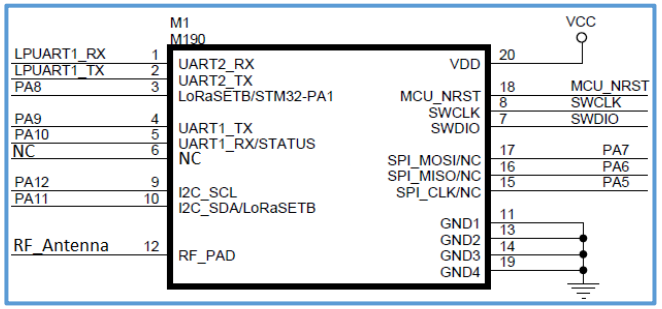
M190/5 Module Development Guide —Hardware

Hardware Design Schematic



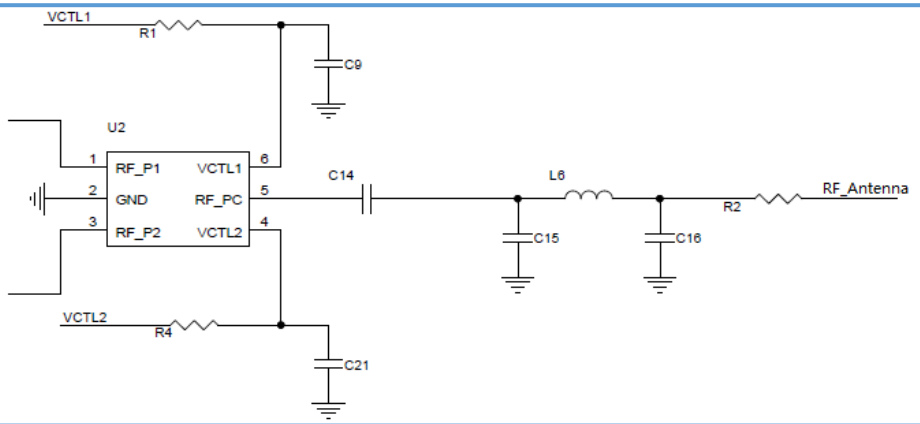






SPDT Switch Truth Table

VCTL1 (Pin 6)	VCTL2 (Pin 4)	INPUT to OUTPUT1 Path	INPUT to OUTPUT2 Path
1	0	Isolation	Insertion loss
0	1	Insertion loss	Isolation



Pin Function Description(Module vs MCU)

M190/5 Pin Number	MCU(STM32WLE5C B/C U6) Pin			
	Numb	Name	Alternate functions	Additional functions
1	10	PA3	TIM2_CH4, I2S2_MCK, USART2_RX, LPUART1_RX, CM4_EVENTOUT	-
2	9	PA2	LSCO, TIM2_CH3, USART2_TX, LPUART1_TX, COMP2_OUT, DEBUG_PWR_LDORDY, CM4_EVENTOUT	LSCO
3	16	PA8	MCO, TIM1_CH1, SPI2_SCK/I2S2_CK, USART1_CK, LPTIM2_OUT, CM4_EVENTOUT	-
4	17	PA9	TIM1_CH2, SPI2_NSS/I2S2_WS, I2C1_SCL, SPI2_SCK/I2S2_CK, USART1_TX, CM4_EVENTOUT	
5	33	PA10	RTC_REFIN, TIM1_CH3, I2C1_SDA, SPI2_MOSI/I2S2_SD, USART1_RX, DEBUG_RF_HSE32RDY, TIM17_BKIN, CM4_EVENTOUT	COMP1_INM, COMP2_INM, DAC_OUT1, ADC_IN6
6	-			
7	36	PA13	JTMS-SWDIO, I2C2_SMBA, IR_OUT, CM4_EVENTOUT	ADC_IN9
8	42	PA14	JTCK-SWCLK, LPTIM1_OUT, I2C1_SMBA, CM4_EVENTOUT	ADC_IN10
9	35	PA12	TIM1_ETR, LPTIM3_IN1, I2C2_SCL, SPI1_MOSI, RF_BUSY, USART1_RTS, CM4_EVENTOUT	ADC_IN8

M190 Pin Number	MCU(STM32WLE5C B/C U6) Pin			
	Number	Name	Alternate functions	Additional functions
10	34	PA11	TIM1_CH4, TIM1_BKIN2, LPTIM3_ETR, I2C2_SDA, SPI1_MISO, USART1_CTS, DEBUG_RF_NRESET, CM4_EVENTOUT	COMP1_INM, COMP2_INM, ADC_IN7
11	48/49	VSSSMPS/VSS	-	-
12	-			
13	48/49	VSSSMPS/VSS	-	-
14	48/49	VSSSMPS/VSS	-	-
15	13	PA5	TIM2_CH1, TIM2_ETR, SPI2_MISO, SPI1_SCK, DEBUG_SUBGHZSPI_ SCKOUT, LPTIM2_ETR, CM4_EVENTOUT	-
16	14	PA6	TIM1_BKIN, I2C2_SMBA, SPI1_MISO, LPUART1_CTS, DEBUG_SUBGHZSPI_ MISOOUT, TIM16_CH1, CM4_EVENTOUT	-
17	15	PA7	TIM1_CH1N, I2C3_SCL, SPI1_MOSI, COMP2_OUT, DEBUG_SUBGHZSPI_ MOSIOUT, TIM17_CH1, CM4_EVENTOUT	-
18	18	NRST	-	-
19	48/49	VSSSMPS/VSS	-	-
20	11/25/ 28/37/44	VDD/VDDPA/ VDDRF/VBAT/VDD	-	-

M190 use STM32WLE5CBU6
M195 use STM32WLE5CCU6

Electrical characteristics

Item	Conditions	Min	Typ	Max	Unit
Operating Voltage	All Band	2.0	3.3	3.6	V
Supply Current	TX , +22dBm	-	120	-	mA
	TX , +17dBm	-	78	-	mA
	RX	-	9	-	mA
	Standby (Class C)	-	8	-	mA
	Sleep (Class A)	1.1	1.5	1.8	μA
Operating Frequency Band	Low Band	430	-	510	MHz
	High Band	862	-	932	MHz
Operating Temperature		-40	-	85	℃
Working Humidity	No-condensation	10%	-	90%	RH
Transmission characteristics	LoRa Mode， Carrier Output， PA_BOOST ON,25±2℃				
MAX. Output Power	_	21.0	21.6	22.0	dBm
Second Harmonic			-40	-	dBm
Receive Characteristics	PER = 1% ， CR = 4/5 ， CRC ON ， Preamble Length = 12 ， Packet Length = 10				
Receive Sensitivity	SF12 ， 125kHz	-	-139	-	dBm
Frequency Characteristics	Frequency Stability: ±2ppm@-40℃~85℃				

RF_TX/RX Specifications

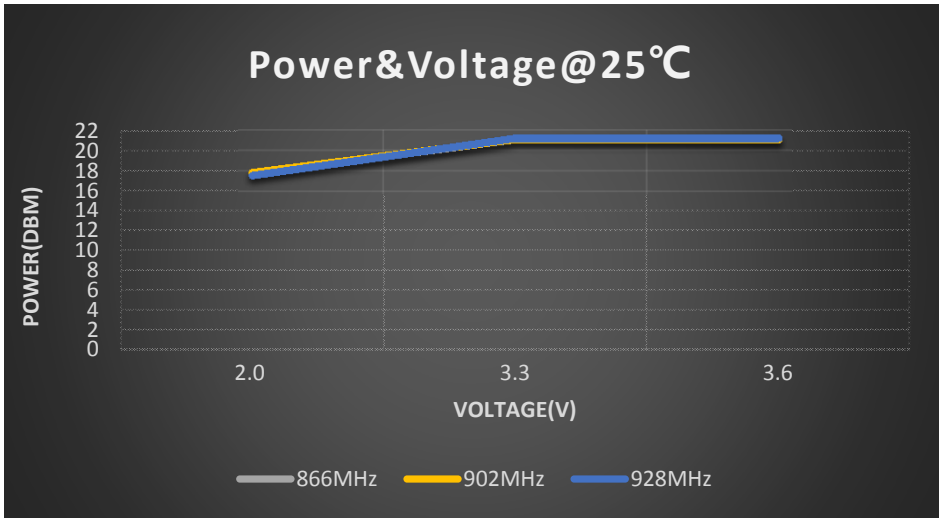
Sub-GHz radio transmit high output power

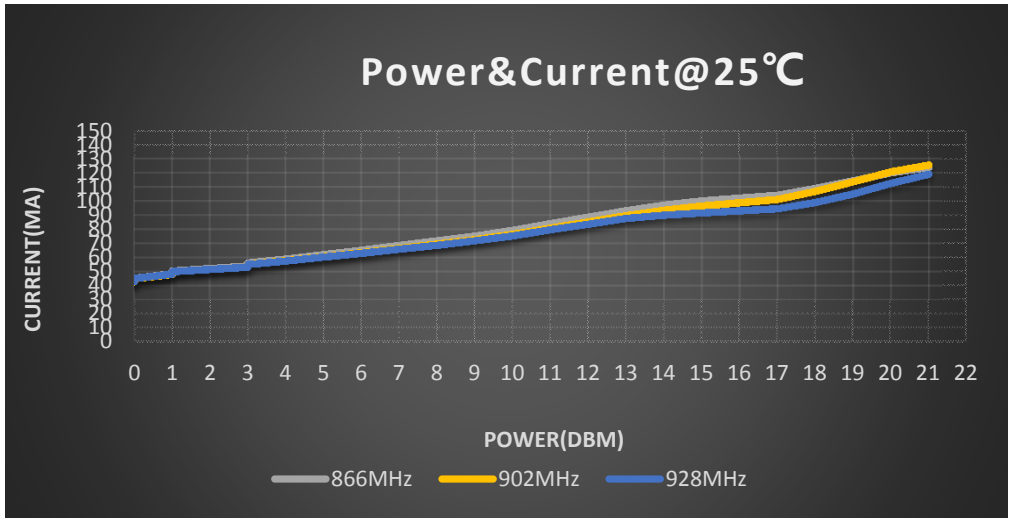
V_{DDPA} supply (V)	Transmit output power (dBm)
3.3	+ 22
2.7	+ 20
2.4	+ 19
1.8	+ 16

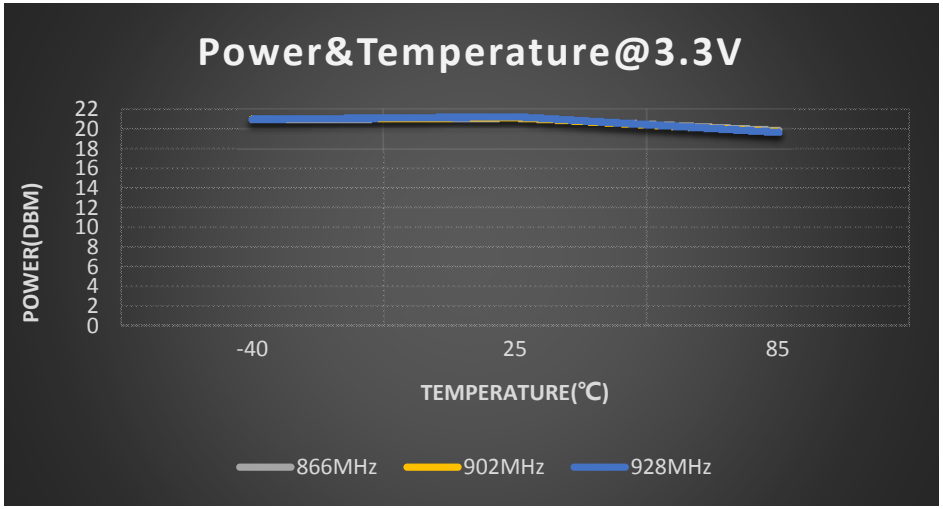
Sub-GHz radio receive mode specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
RXS_LB	Sensitivity LoRa, RX boosted gain, split RF paths for RX and Tx, RF switch insertion loss excluded	BW = 125 kHz, SF = 7	-	–125	-	dBm
		BW = 125 kHz, SF = 12	-	–138	-	
		BW = 250 kHz, SF = 7	-	–122	-	
		BW = 250 kHz, SF = 12	-	–135	-	
		BW = 500 kHz, SF = 7	-	–118	-	
		BW = 500 kHz, SF = 12	-	–130	-	

Transmit Test Data



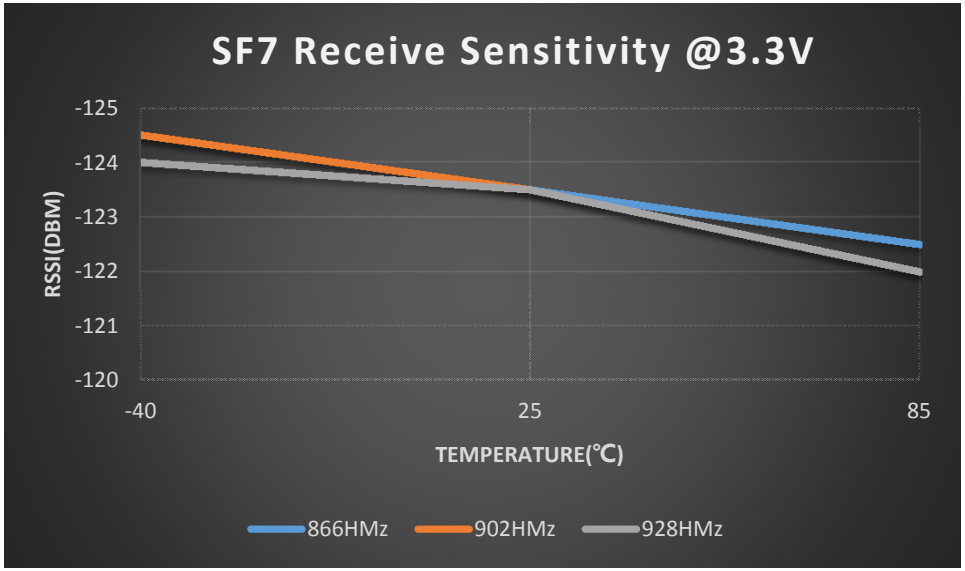


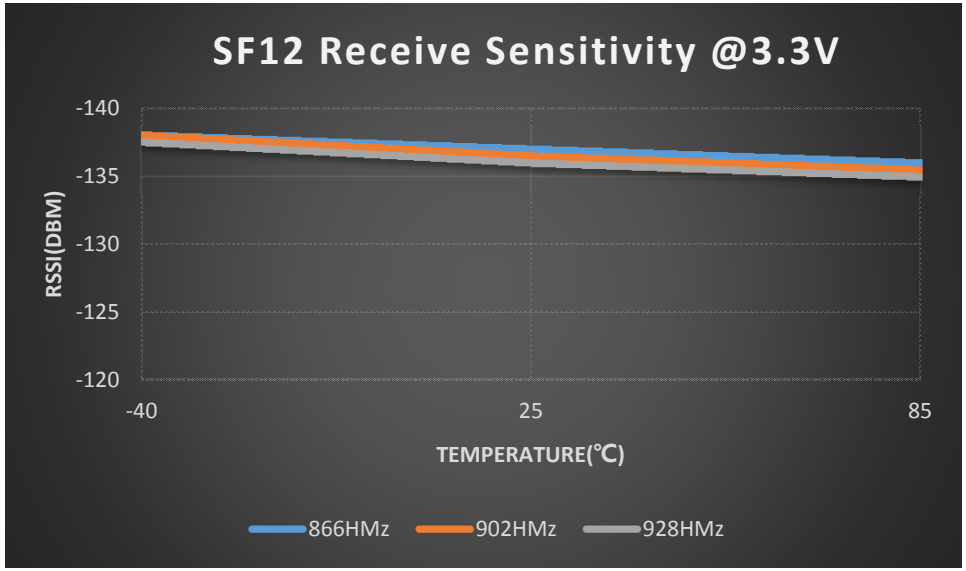


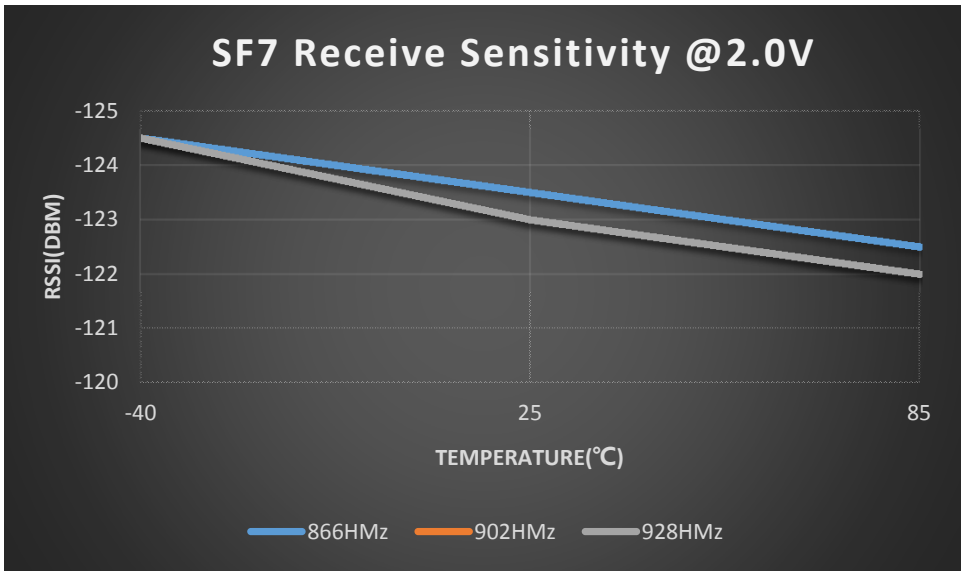
Conducted Spurious Emission

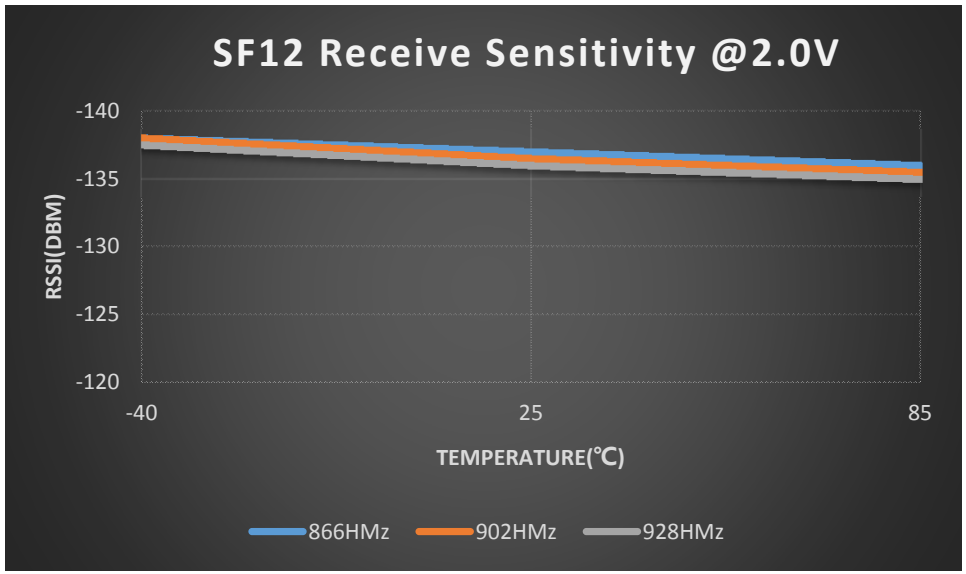
Operating conditions:3.3V, 25℃, 22dBm						
Frequency	866MHz		902MHz		928MHz	
Harmonic	2nd	3nd	2nd	3nd	2nd	3nd
1#(dBm)	-40.81	-50.18	-43.28	-48.55	-41.43	-48.05
Margin(dB)	10.81	20.18	13.28	18.55	11.43	18.05
2#(dBm)	-40.75	-50.62	-43.25	-48.47	-41.78	-49.01
Margin(dB)	10.75	20.62	13.25	18.47	11.78	19.01

Receive Sensitivity Test Data



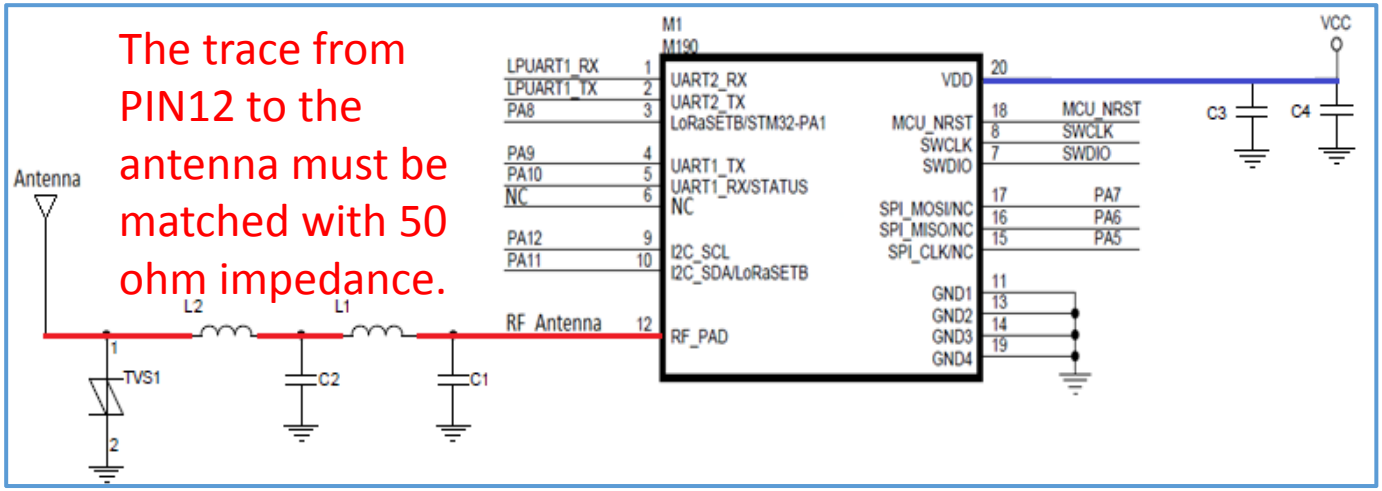






Hardware Design Reference

The trace from PIN12 to the antenna must be matched with 50 ohm impedance.



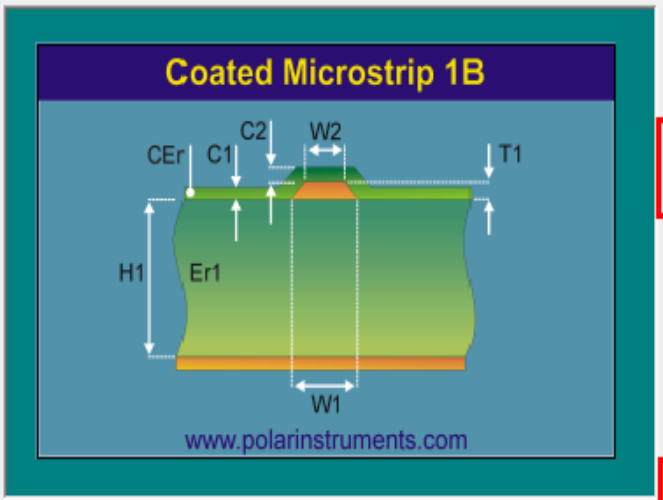
The power supply capacity of the burst current is not less than 150mA.

If it is powered by a capacity battery, please add a super capacitor.

The safe power supply voltage range is 2.0~3.6V.

You can use Polar Si9000 to simulate and calculate the trace width, which is related to the PCB dielectric(Er1), trace thickness(T1) and the distance(H1) between the adjacent layer GND .

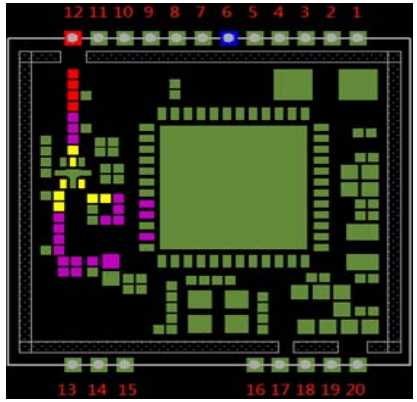
And add more ground holes on both sides of the trace.

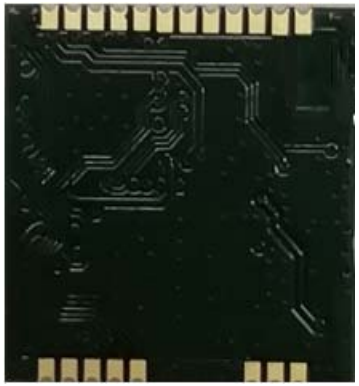


				Tolerance	Minimum	Maximum	
Substrate 1 Height	H1	3.6500	+/-	0.0000	3.6500	3.6500	Calculate
Substrate 1 Dielectric	Er1	3.8500	+/-	0.0000	3.8500	3.8500	Calculate
Lower Trace Width	W1	6.8221	+/-	0.0000	6.8221	6.8221	
Upper Trace Width	W2	5.8221	+/-	0.0000	5.8221	5.8221	Calculate
Trace Thickness	T1	0.6900	+/-	0.0000	0.6900	0.6900	Calculate
Coating Above Substrate	C1	0.8000	+/-	0.0000	0.8000	0.8000	
Coating Above Trace	C2	0.5000	+/-	0.0000	0.5000	0.5000	
Coating Dielectric	CEr	3.3000	+/-	0.0000	3.3000	3.3000	
Impedance	Zo	50.00			0.00	0.00	Calculate

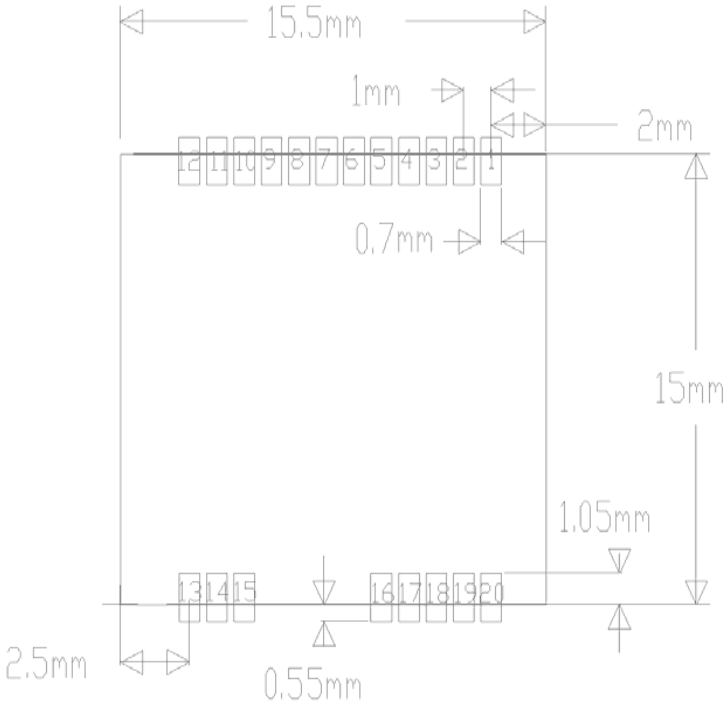
Structure and Package

1mm Pitch Htamp Hole Pads

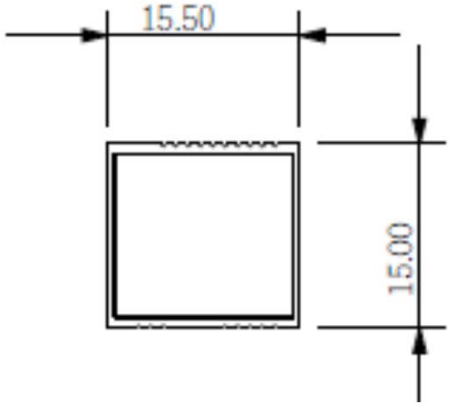


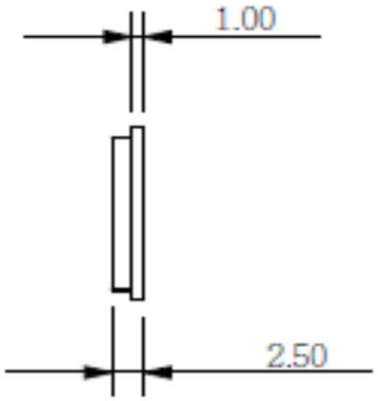


Package



Structure Size





Thank you!