UART-Based Sensor Data Transmission using VSDSquadron FPGA (uart_tx_sense)

1. Introduction

This document provides a detailed study of the uart_tx_sense project from the VSDSquadron_FM repository. The project involves acquiring sensor data and transmitting it via a UART interface using an FPGA.

2. Study of Existing Code

2.1 Overview

The uart_tx_sense project is designed to interface a sensor with an FPGA, read sensor data, and transmit it serially over a UART interface. The Verilog code includes:

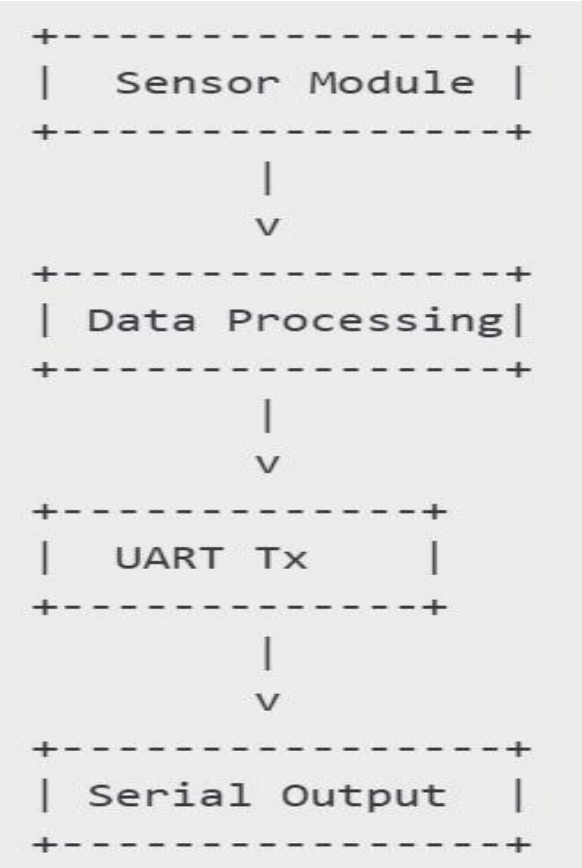
- Sensor Data Acquisition Module: Captures data from the sensor.
- UART Transmission Module: Encodes and sends the data serially.
- Clock and Control Logic: Ensures proper timing and synchronization.

2.2 Key Code Components

- Sensor Interface: Reads data from the sensor.
- UART Transmitter: Implements a serial communication protocol.
- Data Buffering: Temporary storage for sensor data before transmission.
- FSM (Finite State Machine): Controls data flow between modules.

3. Block Diagram

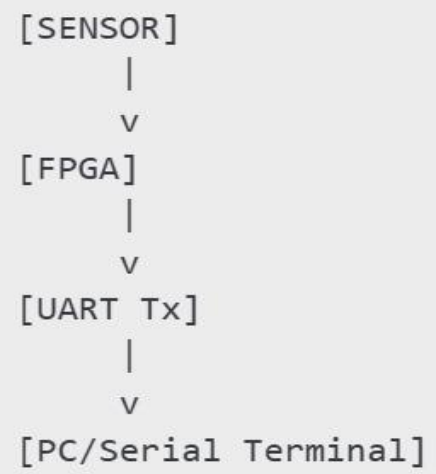
Below is the block diagram showing the integration of the sensor module with the UART transmitter.



4. Circuit Diagram

A simplified circuit diagram illustrating the connections between the FPGA, sensor, and receiving device:

- Sensor to FPGA: Data input to an FPGA GPIO pin.
- FPGA to UART Transmitter: Serial communication interface.
- UART to PC: Data received on a serial terminal.



5. Implementation Steps

Set Up Hardware:

Connect the sensor to FPGA input pins.

Connect UART Tx output pin to the receiving device.

Load Verilog Code:

Synthesize and program the FPGA with the Verilog design.

Run the System:

Ensure proper interfacing and power connections.

6. Testing and Verification

Stimulate the sensor with known inputs.

Observe the UART-transmitted data using a serial terminal (e.g., Putty, Tera Term).

Compare received data with expected sensor readings.

Validate transmission integrity and accuracy.

7. Results

Successfully acquired sensor data and transmitted it via UART.

Verified output through serial terminal logs.

Confirmed data integrity with expected values.

8. Conclusion

This project demonstrates efficient sensor data acquisition and UART-based transmission using an FPGA. The study and implementation verify correct operation and provide a foundation for further enhancements.

9. Video Demonstration

A short video has been recorded showcasing the system in action, displaying live sensor data transmission via UART.