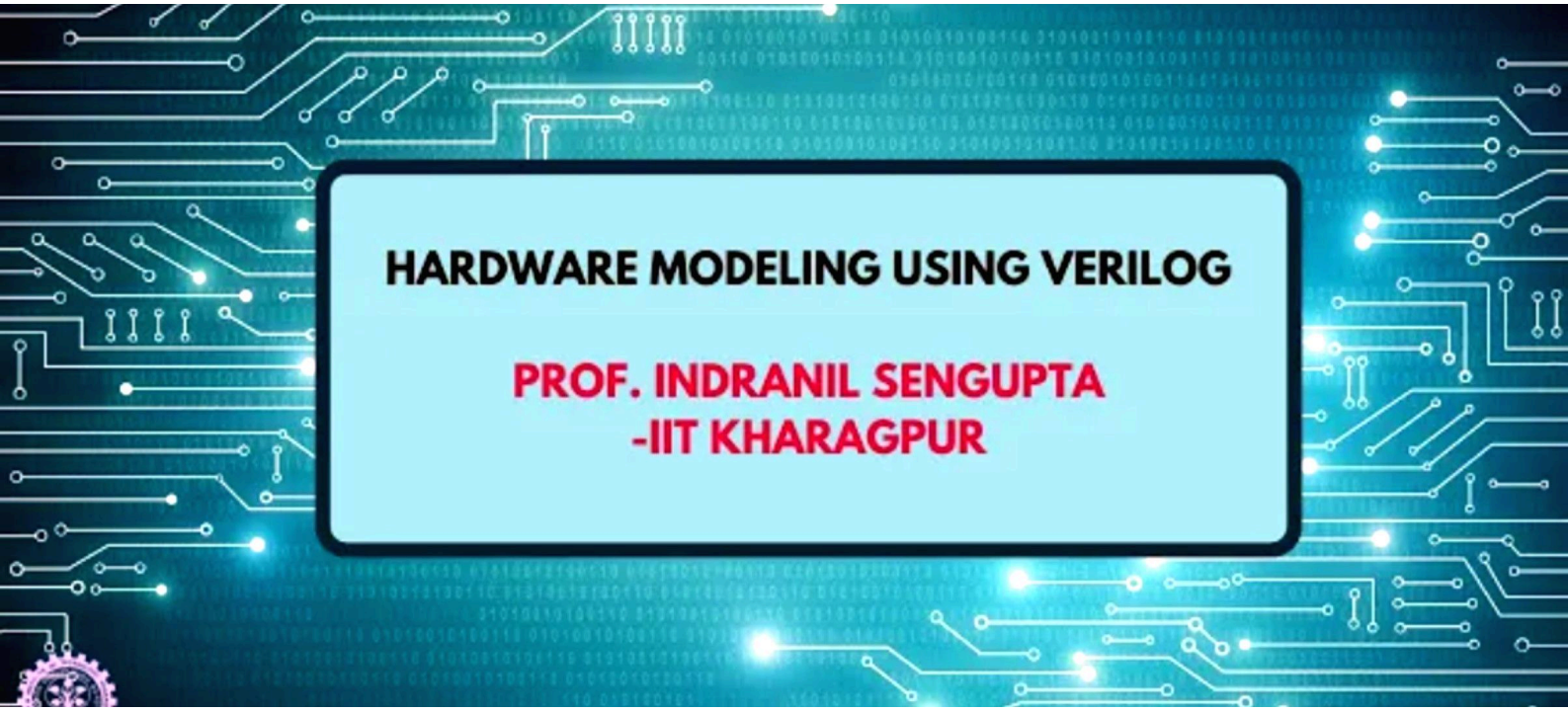
HARDWARE MODELING USING VERILOG
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by

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NPTEL
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2020

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HARDWARE MODELING USING VERILOG [IIIK]

⊙ VLSI DESIGN FLOW

- Standardized design procedure
  - Starting from the design Idea down to the actual implementation.
- Encompasses many steps:
  - Specification
  - Synthesis
  - Simulation
  - layout
  - Testability analysis
  - and many more

- Need to use Computer Aided Design (CAD) tools.
  - Based on Hardware Description language (HDL)
  - HDL's provide formats for representing the output of various design step.
  - A CAD tool transforms its HDL input into a HDL output that Contains more detailed information about the hardware.
    - behavioral level to register transfer level
    - Register transfer level to gate level
    - Gate level to transistor level
    - Transistor level to the layout level.

Notes

⊙ Two Competing HDL's :-

① VERILOG
② VHDL

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- design are created typically using HDLs, which get transformed from one level of abstraction to the next as the design flow progress

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◉ Simplistic View of Design Flow :-

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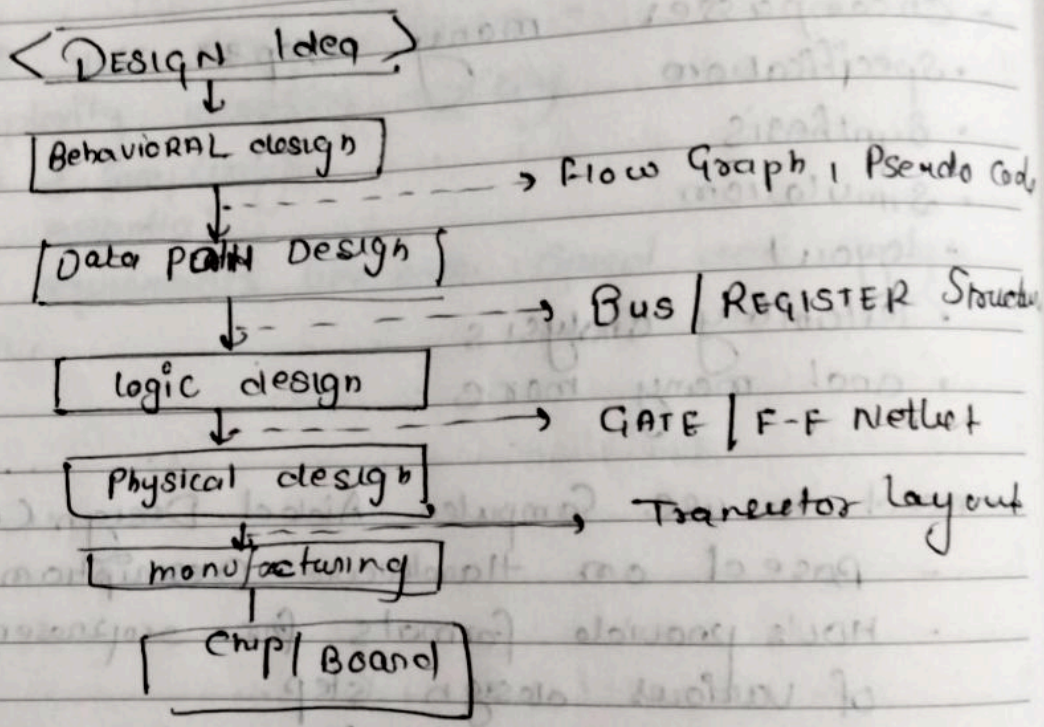

◉ Step in the Design Flow

- BEHAVIORAL DESIGN
- Specify the functionality of the design in terms of its behavior.
- Various way of specifying :
  - Boolean expression or truth table.
  - finite-state machine behaviour (eg : State digram or table
  - in the form of high-level algorithm
- need to be Synthesized into more detailed Specification for hardware realization.

07 Sunday

Notes

⊙ DATA PATH DESIGN :-

- Generate a netlist of register transfer level components like registers, adders, multipliers, multiplexers, decoders etc.
- A netlist is a directed graph, where the vertices indicates components, and the edges indicates interconnections.
- A netlist specification is also referred to as structural design.
- Systematically transformed from one level to the next.

⊙ logic DESIGN :-

- generate a netlist of gates / flip-flops or standard cells.
- A standard cell is a predesigned circuit module (like gates, flip-flops, multiplexer, etc) at the layout level.
- various logic optimization techniques are used to obtain a cost effective design.
- There may be conflicting requirements during optimization:
  - minimum number of gates.
  - minimum num of gate levels (i.e delay)
  - minimum signal transition activities (ie. dynamic power)

Notes ⊙ PHYSICAL DESIGN AND MANUFACTURING

- Generate the final layout that can be sent for fabrication.

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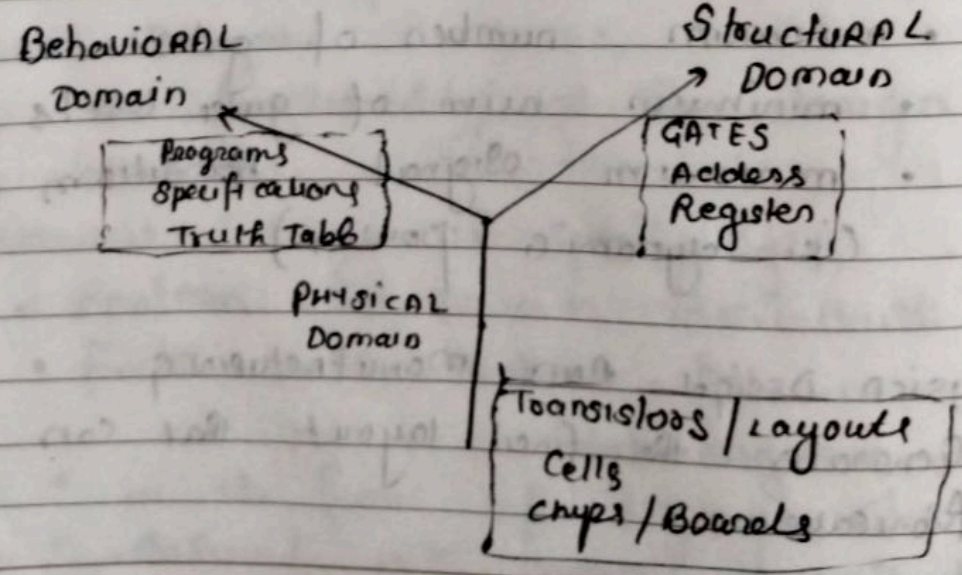
OTHER STEP IN THE DESIGN FLOW

- Simulation for verification
  - At various level: logic level, switch level, circuit level,
- FORMAL VERIFICATION
  - used to verify the design through formal techniques
- TESTABILITY analysis and TEST PATTERN GENERATION
  - required for testing the manufactured devices.

Lecture ② DESIGN REPRESENTATION

- A design can be represented at various levels from three different point of view:
  ① Behavioral
  ② structural
  ③ Physical
- Can be conveniently expressed by Y-diagram.
  ∴ Y diagram means it has shape Y.



Notes

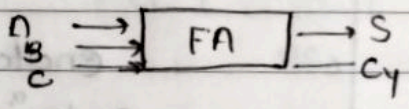
⊙ BEHAVIORAL REPRESENTATION

- Specifies how a particular design should respond to a given set of inputs.
- may be specified by :-
  - Boolean equation
  - Tables of Input and output values
  - Algorithms written in standard HLL like C
  - Algorithms written in special HDL like Verilog or VHDL.

eg;-

Full Adder :-

- two operand input A and B
- a carry input C
- a carry output C_4
- a Sum output S



- expression in terms of Boolean expression;

$$S = A.B'.C' + A'B'C + A'BC' + ABC$$

$$S = A \oplus B \oplus C$$

$$C_4 = AB + AC + BC$$

⊙ Expression in verilog in terms of Boolean expression

```
module Carry (S, C4, A, B, C);   // name module; S, C4, A, B, C: Parameters
    input A, B, C;
    output S, C4;
    assign S = A^B^C;
    assign C4 = (A&B) | (B&C) | (C&A);
endmodule
```

∴ This is like the function in C. Notes

⊙ Express in VERILOG in terms of Truth table (Only C_4 is shown) ;; C_4 → carry

```
primitive Carry (C4, A, B, C);
  input A, B, C;
  output C4;
  table
  //  A  B  C  :  C4
      1  1  ?  :  1;
      1  ?  1  :  1;
      ?  1  1  :  1;
      0  0  ?  :  0;
      0  ?  0  :  0
      ?  0  0  ;  0
  endtable
endprimitive
```

(? means don't care)

∴ when $C_4 = AB + BC + CA$

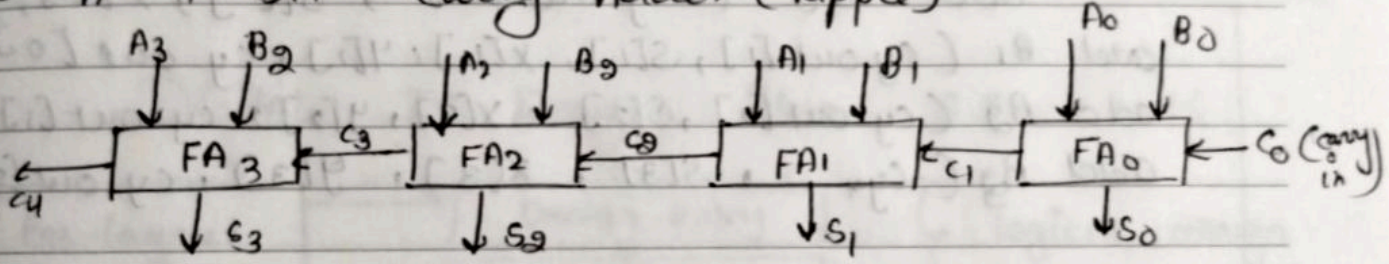
$= \begin{matrix} A & B & C \\ 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{matrix}$ ∴ All other cases $C_4 = 0$

⊙ STRUCTURAL REPRESENTATION :

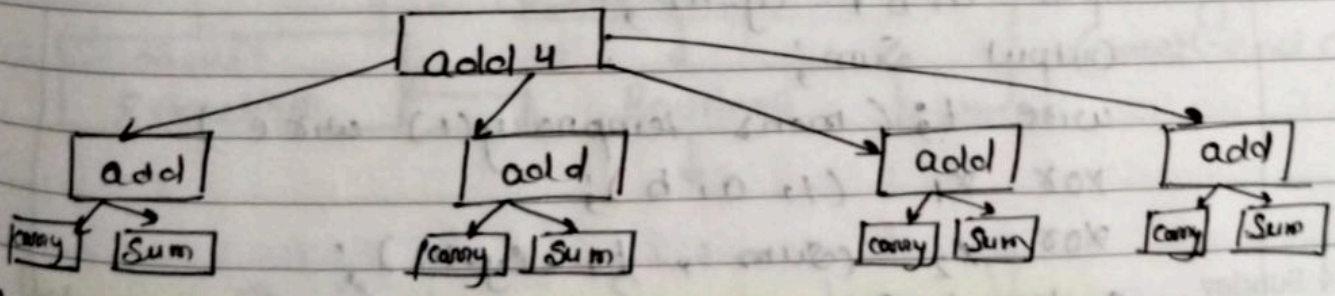
- Specifies how components are interconnected.
- In general, the description is a list of modules and their interconnections.
  - called netlist.
  - Can be specified at various levels.

- At the structural level, the levels of abstraction are:
  - The module (Functional level)
  - The gate level
  - The transistor level
  - Any combination of above
- In each successive level detail in revealed about the implementation.

eg:- A 4-bit Carry-Adder (Ripple)



- Consist of four full adders.
- Each full adder consists of a Sum circuit and a Carry circuit.



Carry = $A \cdot B + B \cdot C + C \cdot A$
Sum = $A \oplus B \oplus C$

⊙ we instantiate Carry and Sum circuits to create a full adder.
- we instantiate four full adders to create the 4 bit adder.

Notes

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→ expression in verilog

```
module add4 ( S, Cy4, Cy_in, X, Y );
  input [3:0] X, Y;
  input Cy_in;
  output [3:0] S;
  output Cy4;
  wire [2:0] Cy_out;

  add B0 ( Cy_out[0], S[0], X[0], Y[0] );
  add B1 ( Cy_out[1], S[1], X[1], Y[1], Cy_out[0] );
  add B2 ( Cy_out[2], S[2], X[2], Y[2], Cy_out[1] );
  add B3 ( Cy4, S[3], X[3], Y[3], Cy_out[2] );

endmodule
```

[3:0] ↓ means 4 bit num

∴

```
module Sum ( Sum, a, b, Cy_in );
  input a, b, Cy_in;
  output Sum;
  wire t; ( means temprary(t) wire )
  xor X1 (t, a, b);
  xor X2 (Sum, t, Cy_in);
endmodule
```

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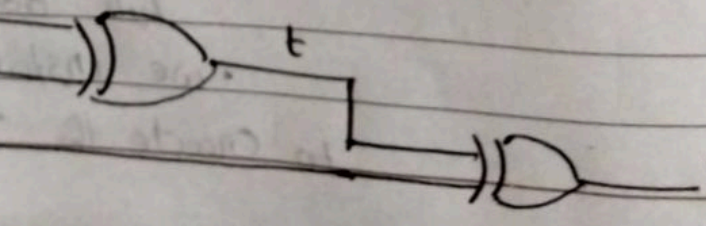
∴ this is structural design

Notes

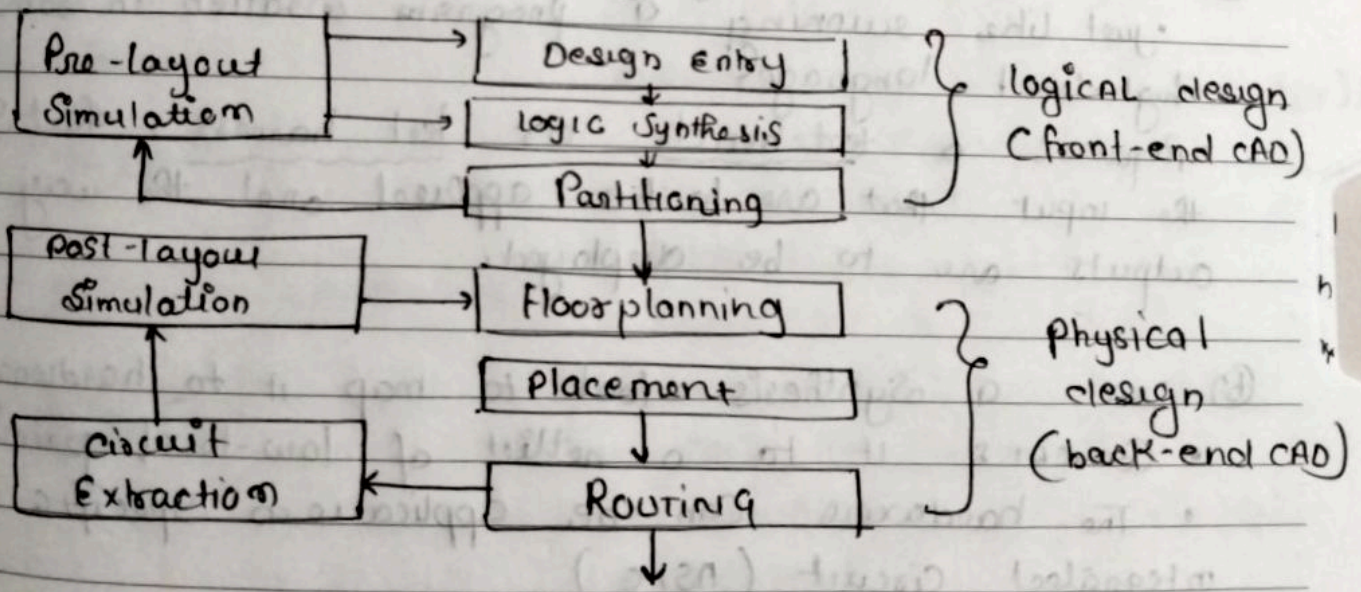
∴ xor X1 (t, a, b) → representation the line



∴ xor X2 (Sum, t, Cy_in

```
module Carry (cy_out, a, b, cy_in);
  input a, b, cy_in;
  output cy_out;
  wire t1, t2, t3;
  and g1 (t1, a, b);
  and g2 (t2, a, c);
  and g3 (t3, b, c);
  or g4 (cy_out, t1, t2, t3);
endmodule
```

DIGITAL IC DESIGN FLOW : A QUICK LOOK



LECTURE ⇒ (3) GETTING STARTED WITH VERILOG

→ WHY DO WE USE VERILOG ?

Notes

- To describe a digital System as a set of modules.
  - each of the module will have an interface to other modules, in addition to its description

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- Two way to Specify a module
  - (a) By Specifying its internal logical structure (called Structural representations).
  - (b) By describing its behavior in a program-like manner (called behavioral representation).
- The modules are interconnected using nets, which allow them to work with each other. (↓ just like wire)

⊙ AFTER SPECIFYING the System in VERILOG, we can do Two things:

(a) Simulate the System and Verify the operation.
- just like, running a program written in some high-level language.
- Requires a test-bench or test harness, that Specify the input that are to be applied and the way the outputs are to be displayed.

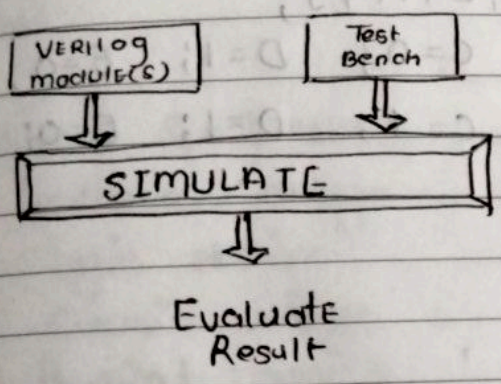
(b) Use a synthesis tool to map it to hardware.
- Converts it to a netlist of low-level primitives.
- The hardware can be application Specific integrated Circuit (ASIC)
- or else, it can be field programmable Gate Array (FPGA).

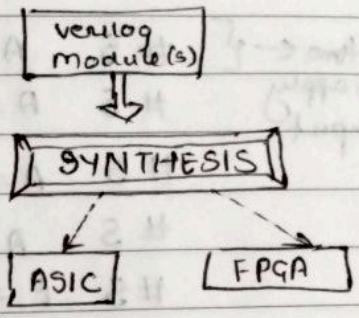
Notes

⊙ Using ASIC as hardware target?
- when high performance & high packing density is required.
- when the manufactured hardware is expected to be used in large numbers (e.g. proces

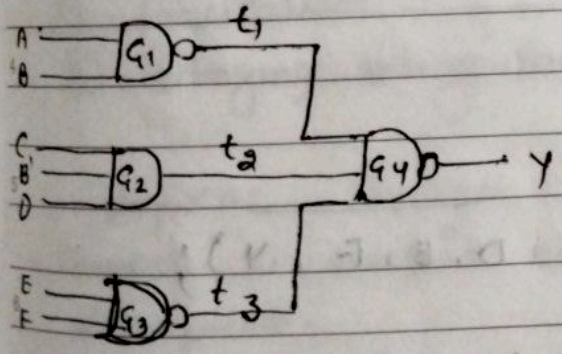
@ using FPGA as hardware target ?

- When Fast turnaround time is required to validate the design.
- The mapping can be done in the laboratory itself with a FPGA kit and associated software.
- There is a tradeoff in performance.





An Example :-




```
module example (A, B, C, D, E, F, Y);
    input A, B, C, D, E, F;
    output Y;
wire t1, t2, t3, Y;
nand #1 g1 (t1, A, B);
and #2 g2 (t2, C, ~B, D);
nor #1 g3 (t3, E, F);
nand #1 g4 (Y, t1, t2, t3);
endmodule
```

we can combine declarations of same type of gate together

```
nand #1 g1 (t1, A, B),
        g4 (Y, t1, t2, t3);
```

Notes

Now we work to TestBench :-

```
module Testbench;
    reg A, B, C, D, E, F; wire Y;
```

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example DUT(A,B,C,D,E,F,Y);

initial
begin $monitor ($time, " A=%b, B=%b, C=%b, D=%b, E=%b, Y=%b"; (like printf) , b= binary
A,B,C,D,E,F,Y);

time ← { #5 A=1; B=0; C=0; D=1; E=0; F=0;
miss 5 apply input #5 A=0; B=0; C=1; D=1; E=0; F=0;
#5 A=1; C=0;
#5 A=1;
#5 F=1;
#5 $finish;
end
endmodule

// Orignal file
file name — example.v

```
module example (A,B,C,D,E,F,Y);
  wire t1,t2,t3,Y;
  nand #1 G1 (t1,A,B)
  and  #2 G2 (t2,C,~B,D);
  nor  #1 G3 (t3,E,F);
  nand #1 G4 (Y,t1,t2,t3);
endmodule
```

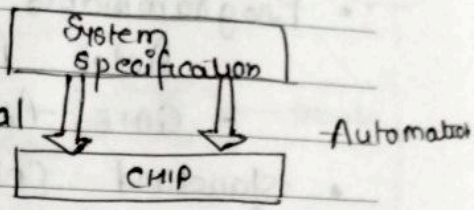
Notes

// $dumpfile ("example.vcd"); (value change dump)
$dumpvars (0, testbench)

Lecture :⇒ ④ VLSI DESIGN STYLES PART - 1

VLSI DESIGN CYCLE

- Large number of devices
- optimization requirements for high performance
- Time-to-market competition
- Cost



① System Specification
② functional design
③ Logic design
④ Circuit design
⑤ Physical design
⑥ Design Verification
⑦ fabrication
⑧ Packaging, testing and debugging.

PHYSICAL DESIGN

- Converts a circuit description in to a geometric description.
  - This description is used for fabrication of the chip.
- Basic steps in the physical design cycle:
  ① Partitioning, floorplaning and placement
  ② Routing
  ③ Static time Analysis
  ④ Signal integrity and crosstalk analysis
  ⑤ Physical Verification and Sign off.

Notes

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Various design Styles

- Programmable logic devices
  - field Programmable Gate Array [FPGA]
  - GATE Array
- standard cell (Semi-Custom Design)
- full-Custom Design

→ which Design Style to use?

- Basically a tradeoff among several design Parameters
  - Hardware Cost
  - Circuit delay
  - Time Required
- optimizing on these Parameters is often Conflicting

⊙ FIELD PROGRAMMABLE GATE ARRAY (FPGA)

- what does FPGA OFFER?

- USER / Field PROGRAMMABILITY.
  - Assay of logic cells Connected via routing channels
  - different types of cells:
    - Special I/O cells:
    - Logic cells (mainly lookup tables (LUT) with associated registers).

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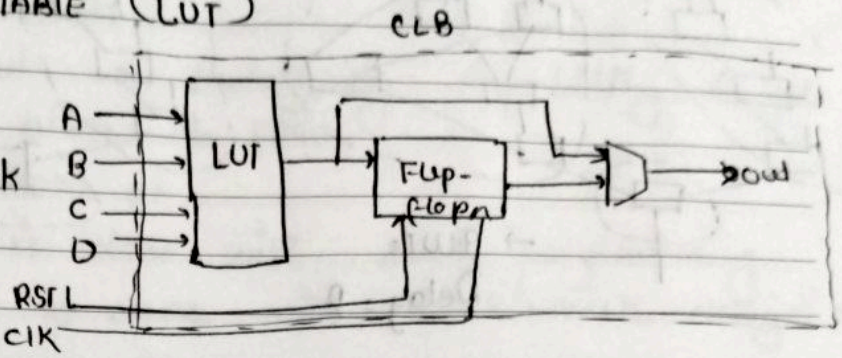
  - Interconnection Between Cells:
    - using SRAM based Switches.
    - using anti-fuse elements.

Notes

Look UP Table (LUT)

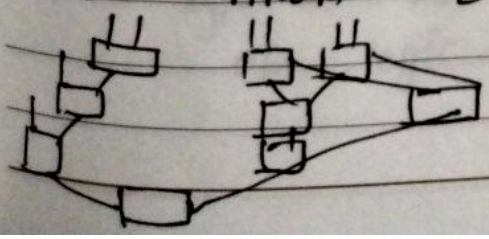


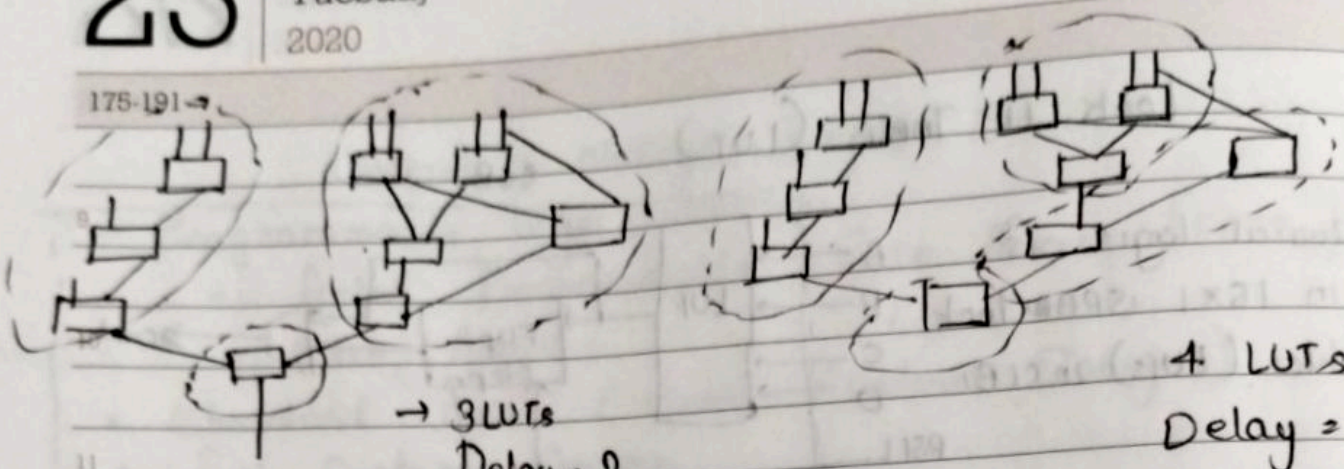
- Combinatorial logic is stored in 16x1 SRAM look up Tables (LUTs) in CLB.
- Capacity is limited by number of input, not complexity.

- Choose to use each function generator as 4-input logic (LUT) or as high-speed RAM.

⊙ LUT mapping : An Example
- A function: $f = A'B + B'C \cdot D$
- The mapping process:
  - create the truth table of the 4-variable function
  - load the output column into the SRAM corresponding to the LUT.
  - Apply the function input to the LUT inputs.
- Any 4-variable function can be realized.
  - Netlist to LUT mapping is an interesting closing tradeoff.

Notes ⊙ AREA - DELAY TRADE OFF

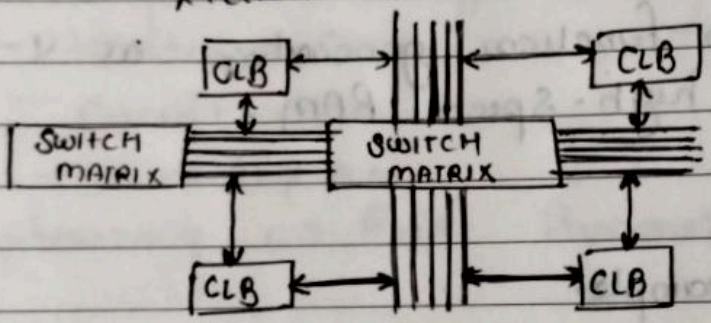




→ 3 LUTs
Delay = 2

4 LUTs
Delay = 3

⊙ XILINX FPGA ROUTING



① First direct interconnect
CLB to CLB

② General purpose interconnect
- uses switch matrix

⊙ FPGA Design Flow

⊙ Design Entry
- in Schematic, VHDL or Verilog.

• Implementation
- Placement & Routing
- Bitstream generation
- Analyze timing, view layout, Simulation, etc.

• Download
- Directly to xilinx hardware devices with unlimited reconfigurations.

Notes

LECTURE :- ⑤ INTRODUCTION

- In view of the Speed of Prototyping capability, the gate array (GA) comes after the FPGA.
- Design implementation of
  - FPGA chip is done with user programming.
  - Gate array is done with metal mask design and processing.

- Gate array implementation requires a two-step manufacturing process:
  ⓐ The first phase, which is based on generic (standard) masks, results in an array of uncommitted transistors on each GA chip.
  ⓑ These uncommitted chips can be customized later, which is completed by defining the metal interconnects between the transistor of the array.

- The GA chip utilization factor is higher than that of FPGA.
  - The used chip area divided by the total chip area.

- Chip speed is also higher.
  - more customized design can be achieved with metal mask designs.

- Typical gate array chips can implement millions of logic gates.

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Week 26

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⊙ STANDARD Cell BASED DESIGN

ASIC

↓ Standard cell (semi custom)

↓ Full Custom

→ INTRODUCTION:

- one of the most prevalent design styles.
  - Also called semi-custom design style.
  - Requires developing full custom mask set.

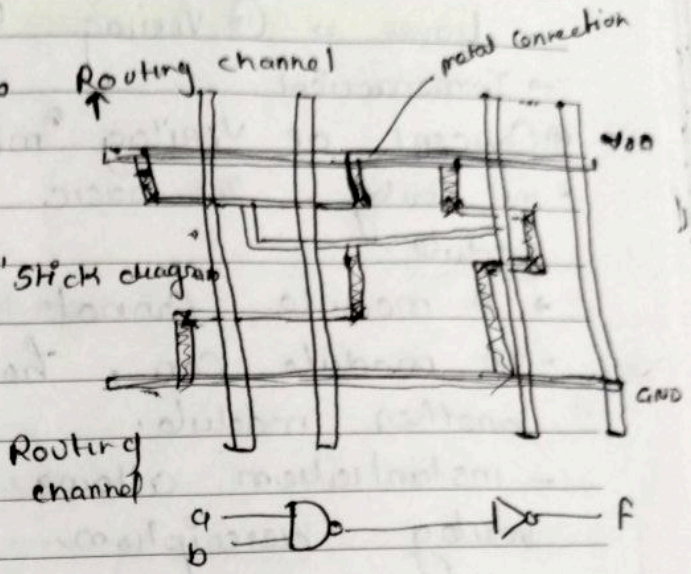
- BASIC Idea:
  - Commonly used logic cells are developed, and stored in a standard cell library.
  - Typical library may contain a few hundred cell (Inverters, nand gates, NOR Gates, AOI gates, 2-to-1 mux, D-latches, flip-flops, etc)

⊙ CHARACTERISTIC OF THE CELL'S

- Each cell is designed with a fixed heigh.
  - To enable automated placement of the cells and routing of inter-cell Connections.
  - A number of cell can be abutted side-by-side to form rows.
- The Power & ground rails typically run parallel to upper and lower boundaries of cell.
  - Neighboring cells share a common power and ground bus.
- The I/P and o/p

Notes

- Standard cell example
- made to stack side by side
  - fixed height
  - width can vary
  - Can abut VDD and GND.



Notes

LECTURE ⇒ ⑥ VERILOG LANGUAGE FEATURES

→ INTRODUCTION

◉ CONCEPT OF VERILOG "MODULE" →

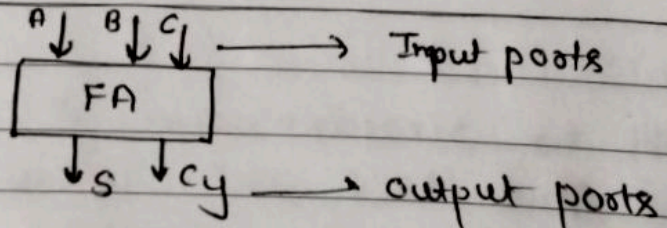
IN verilog, THE basic unit of hardware IS called a module.

→ A module cannot contain definations of other modules

- A module can, however, be instantiated within another module.

- instantiation allows the creation of hierarchy in verilog descriptions.

```
module module_name (list_of_Ports);
    Input/output declarations
    local net declarations
    Parallel statements
endmodule
```




```
// A Simple AND Function
module simpleand (f, x, y);
    input x, y;
    output f;
    assign f = x & y;
endmodule
```

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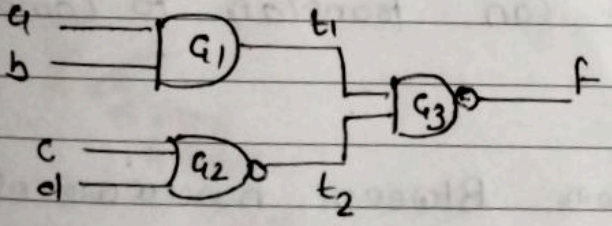
Notes

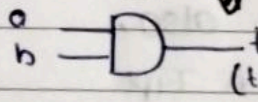
eg:- /* A 2-level Combinational Circuit */

```
module two_level (a, b, c, d, f);
    input a, b, c, d;
    output f;
    wire t1, t2; //intermediate lines
    assign t1 = a & b;
    assign t2 = ~(c | d);
    assign f = ~(t1 | t2);
endmodule
```

- This is behavioral description.
- one possible gate level realization is shown.
- t_1 and t_2 are intermediate lines; termed as wire data type.



assign t_1 = a & b;



(t_1 is continuously driven)

⊙ Point to NOTE:

- The "assign" statement represents Continuous assignment, whereby the variable on the LHS gets updated whenever the expression on the RHS change.

  assign variable = expression.

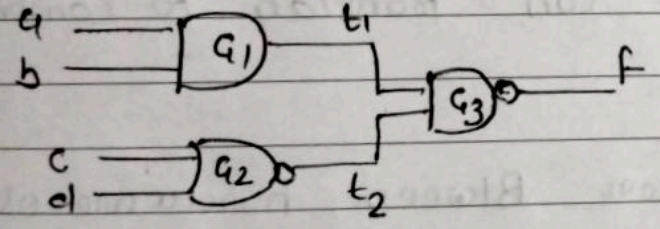
- The LHS must be a "net" type variable, typically a "wire"
- The RHS can contain both "register" and "net" type variables.

Notes

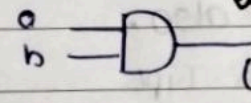
eg:- /* A 2-level Combinational Circuit */

```
module two_level (a, b, c, d, f);
    input a, b, c, d;
    output f;
    wire t1, t2; //intermediate lines
    assign t1 = a & b;
    assign t2 = ~(c | d);
    assign f = ~(t1 | t2);
endmodule
```

- This is behavioral description.
- one possible gate level realization is shown.
- t_1 and t_2 are intermediate lines; termed as wire data type.



assign t_1 = a & b;



(t_1 is continously driven)

⊙ Point to NOTE:

- The "assign" statement represents Continuous assignment, whereby the variable on the LHS gets updated whenever the expression on the RHS change.

assign variable = expression.

- The LHS must be a "net" type variable, typical a "wire"
- The RHS can contain both "register" and "net" type variables.

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Notes

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Week 27

182-184

- The "assign" statement model behavioral design style and is typically used to model combinational circuits

⊙ DATA TYPES IN VERILOG

- A variable in verilog belongs to one of two data types:

ⓐ Net

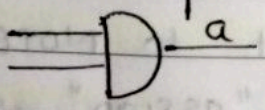
- must be continuously driven.
- Cannot be used to store a value.
- used to model connections between continuous assignments and instantiations.

ⓑ Register

- Retains the last value assigned to it.
- often used to represent storage elements, but sometimes it can translate to combinational circuit also.

⊙ NET DATA TYPE

- Net represents connection Btween hardware elements
- Net are continuously driven by the outputs of the devices they are connected to.



- Net "a" is continuously driven by the o/p of the AND Gate.
- Nets are 1-bit values by default unless they are declared explicitly as vectors.
- Default value of a net is "z".
- Various "Net" data types are supported for Synthesis in verilog:
- wire, wor, wand, tri, supply0 etc.

Notes

01 July Wednesday 2020

Week 27

183-183

DATA VALUES and Signal Strengths

- Verilog supports 4 value levels and 8 strength levels to model the functionality of real hardware.
- strength level are typically used to resolve conflicts between signal drivers of different strengths in real ckt.

Value level	Represents
0	Logic 0 state
1	Logic 1 state
x	Unknown logic state
z.	High impedance state.

initialization

- All unconnected nets are set to "z".
- All register variable set to "x".

Lecture ⇒ ① VERILOG LANGUAGE FEATURES

ⓑ REGISTOR DATA TYPE

⊙ in verilog, a "register" is a variable that can "hold" a value.

- Unlike a "net" that is continuously driven and cannot hold any value.
- Does not necessarily mean that it will map to a hardware register during Synthesis.
- Combinational circuit specifications can also use register type variables.

Notes

184-182

⊙ Register data types supported by verilog:

(i) reg : most widely used
(ii) integer : used for loop counting (typical use)
(iii) real : used to store floating-point numbers.
(iv) time : keeps track of simulation time (not used in synthesis)

• "reg" data type:
- Default value of a "reg" data type is "x".
- It can be assign a value in synchronism with a clock or even otherwise.
- The declaration explicity specifies the size (default is 1-bit):

```
reg x, y;          // Single-bit register variables
reg [15:0] bus;    // A 16-bit bus
```

- Treated as an unsigned number in arithmatic expressions.
- must be used when we model actual sequential/ hardware elements like counters, shift register etc.

Example

```
module Simple_counter (clk rst, count);
    input clk, rst;
    Output [31:0] Count;
    reg [31:0] count;

always @ (Posedge clk)   // apply for whenever there positive edge of the coming.
begin
    if (rst)  count = 32'b0
    else  count = count+1
end
```

∴ 32-bit Counter with Synchronous reset.
- Count value increase at the positive edge of the clock."
- If "rst" is high, the Counter is reset at the +ve edge of the next clk.

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```
module Simple_counter (clk, rst, count);
    input clk, rst;
    output [31:0] count;
    reg [31:0] count;

    always @(posedge clk or posedge rst)
    begin
      if (rst)
          count = 32'b0;
      else
          count = count+1;
    end
endmodule
```

- 32-bit Counter with asynchronous reset.
- Here reset occurs whenever "rst" goes high.
- Does not Synchronize with clk.

◉ "integer" data type:
- It is a general-purpose register data type used for manipulating quantities.
- more convenient to use in situation like loop counting than "reg".
- It is treated as a 2's complement signed integer in arithmetic expressions.
- default size is 32 bits; however, the synthesis tool tries to determine the size using data flow analysis.

example –

```
module Simple_counter (clk, rst, count);
    input clk, rst;
    output [31:0] count;
    reg [31:0] count;

    always @(posedge clk or posedge rst)
    begin
      if (rst)
          count = 32'b0;
      else
          count = count+1;
    end
    endmodule
```

= 32-bit Counter with asynchronous reset.
- Here reset occurs whenever "rst" goes high.
- Does not Synchronize with clk.

◉ "integer" data type:
- It is a general-purpose register data type used for manipulating quantities.
- more convenient to use in situation like look counting than "reg".
- It is treated as a 2's Complment Signed integer in arithmetic expressions.
- default size is 32 bits; however, the Synthesis tool tries to determine the size using data flow analysis.

example -

wire [15:0] x, y;
Integer c;
c = x + y;

- Size of c can be deduced to be 17 (16 bit plus a carry).

② "Real" data type:
- used to store floating-point numbers.
- when a real value is assigned to an integer, the real number is rounded off to the nearest integer.
- Example:

```
real e, pi;
initial
    begin
    e = 2.718
    pi = 3.14159e-2;
    end
```

```
integer x;
initial
    x = pi; // gets value 3
```

③ "time" data type;
- in verilog, simulation is carried out with respect to a logical clock called Simulation time.
- The "time" data type can be used to store Simulation time
- The system function "$time" gives the current Simulation time.
- eg

```
time Curr_time;
initial
    ------
    curr_time = $time;
```

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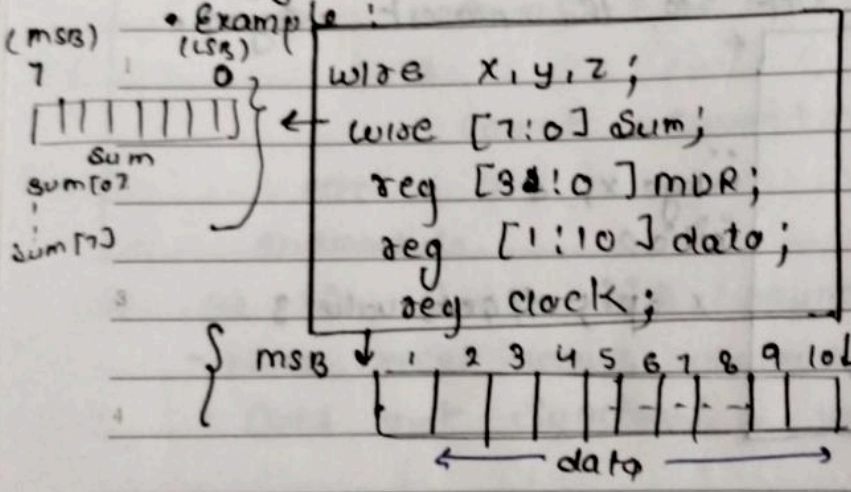
188-178

⊙ VECTORS

- Nets or "reg" type variable can be declared as vectors of multiple bit widths.
  → if bit width is not specified, default size is 1-bit.

- Vectors are declared by specifying a range [range1 : range2] where range1 is always the most significant bit and "range2" is the least significant bit.

- Example :

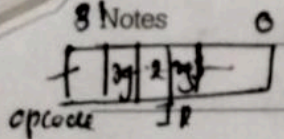


∴ this is just like an array

{ → individual bit i can access by writing
Sum[0]
Sum[1]
Sum[7]

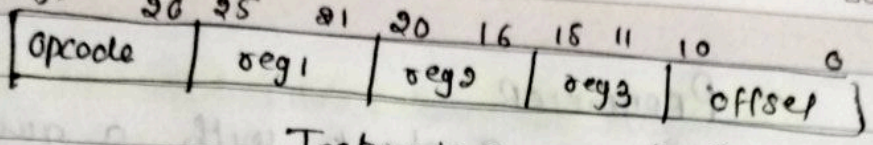
⊙ Parts of a vector can be addressed and used in an expression.

- Example
  - A 32 bit instruction register, that contains a 6-bit opcode, three register operands of 5 bit each, and an 11-bit offset.




```
reg [31:0] IR;
reg [5:0] opcode;
reg [4:0] reg1, reg2, reg3;
reg [10:0]
```

```
opcode = IR[31:26];
reg1 = IR[25:21];
reg2 = IR[20:16];
reg3 = IR[15:11];
offset = IR[10:0];
```



Instruction register (IR)

189-177

⊙ Multi-dimensional Arrays And memories

- multi-dimensional array of any dimension can be declared in verilog.
- example;

```
reg [31:0] register_bank [15:0]; // 16-32 bit registers
integer matrix [7:0][15:0];
```

- memories can be modeled in verilog as a 1D array of registers
- Examples:

```
reg mem_bit [0:2047];          // 2K 1-bit words
reg [15:0] mem_word1 [0:1023]; // 1K 16-bit words
```

⊙ Specifying Constant Values

- A constant value may be specified in either the sized of the unsized form.
  - Syntax of sized form:
    `<size>'<base><number>`
  - Example:

```
4'b0101     // 4-bit binary number 0101
1'bo        // logic 0 (1-bit)
12'hB3C     // 12 bit number 1011 0011 1100
12'h8XF     // 12 bit number 1000 XXXX 1111
25          // signed number, in 32 bits (size not specified)
```

> variable of type integer and real are typically expressed in unsized form.

Notes

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Week 28

190-176

- PARAMETER

- A parameter is a constant with a given name,
  - we cannot specify the size of a parameter.
  - The size gets decided from the constant value itself; if size is not specified, its taken to be 32 bits.

Parameter HI = 25, LO = 5;
Parameter up = 2'b00, down = 2'b01, steady = 2'b10;

Example

```
// Parameter design : an N-bit Counter

module Counter (clear, clock, count);
    parameter N=7;
    input clear, clock;
    output [0:N] Count; reg [0:N] count;

    always @ (negedge clock)
        if (clear)
            Count <=0;
        else
            Count <= Count +1;
endmodule
```

* any variable assigned within the "always" block must be of type "reg".

Notes

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LECTURE :- ⑧ VERILOG LANGUAGE FEATURES

⊙ PREDEFINED LOGIC GATES IN VERILOG

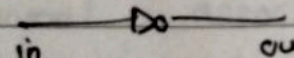
- Verilog provides a set of predefined logic gates.
  - Can be instantiated within a module to create a structured design.
  - The gates respond to logic values (0, 1, X, or Z) in logical way.

2-input AND	2-input OR	2-input EXOR
0 & 0 = 0	0 | 0 = 0	0 ^ 0 = 0
0 & 1 = 0	0 | 1 = 1	0 ^ 1 = 1
1 & 1 = 1	1 | 1 = 1	1 ^ 1 = 0
1 & X = X	1 | X = 1	1 ^ X = X
0 & X = 0	0 | X = X	0 ^ X = X
1 & Z = X	1 | Z = X	1 ^ Z = X
Z & X = X	Z | X = X	Z ^ X = X
∴ X → Undefined	∴ Z → high impedance	

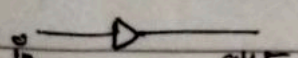
⊙ LIST OF PRIMITIVE GATES :-

```
and  G(out, in1, in2);
nand G(out, in1, in2);
or   G(out, in1, in2);
nor  G(out, in1, in2);
xor  G(out, in1, in2);
xnor G(out, in1, in2);
not  G(out, in);
buf  G(out, in);
```

∴ NOT GATE

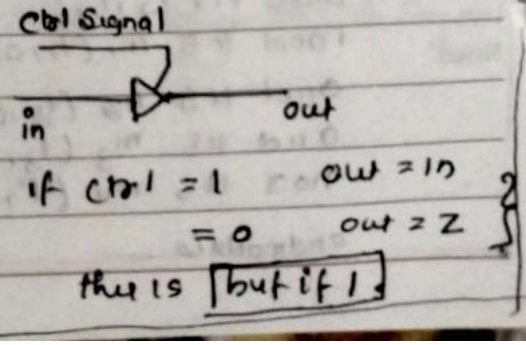


∴ buf




```
bufif1  G(out, in, ctrl);
bufif0  G(out, in, ctrl);
notif0  G(out, in, ctrl);
notif1  G(out, in, ctrl);
```

∴ there are gates with tristate controls.



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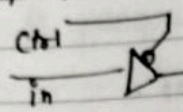
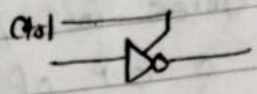
buf if 0



If ctrl = 0 , out = in
= 1 , out = Z

notif 1

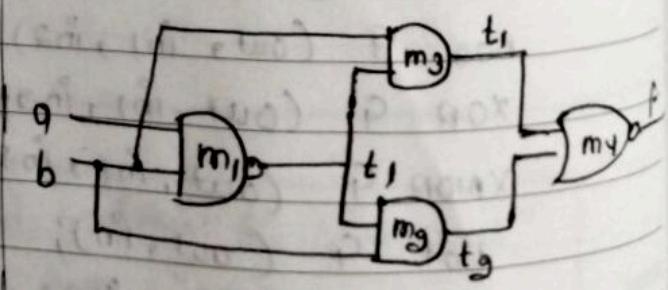


notif 0

⊙ Some restriction when instantiating primitives gates:
- The output port must be connected to a net (e.g a wire)
  - An "output" signal is a wire by default, unless explicitly declared as a register.
- The input port may be connected to net or register type variable.
- They have a single output but can have any number of inputs (except NOT & Buf).
- when instantiating gate, an optional delay may be specified
  - Used for simulation.
  - logic Synthesis tool ignore the time delays.

Example :- shows this delays :-

```
timescale 1ns/1ns
module exclusive-or (f,a,b);
input a,b;
output f;
wire t1, t2, t3;
nand #5 m1 (t1,a,b);
and #5 m2 (t2,a,t1);
and #5 m3 (t3,t1,b);
nor #5 m4 (f,t2,t3);
endmodule
```



• THE 'timescale DIRECTIVE

- often in a single simulation, delay values in one module need to be specified in terms of some time unit, while those in some other module need to be specified in terms of some other time unit.
- The 'timescale compiler directive can be used:

'timescale <reference_time_unit> / <time_precision>

- The <reference_time_unit> specifies the unit of measurement for time.
- The <time_precision> specifies the precision to which the delays are rounded off during simulation.
  - valid values for specifying time unit & time precision are 1, 10 and 100.

• Example:

'timescale 10ns/1ns

- Reference time unit is 10ns, and simulation precision is 1ns.
- if we specify #5 as delay, it will mean 50ns.
- The time units can be specified, s (second), ms (millisecond), us (microsecond), ps (picosecond) & fs (femtosecond)

⊙ Specifying Connectivity during Instantiation

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- when a module is instantiated within another module, there are two ways to specify the connectivity of the signal line btw the two modules
  - (a) positional association
  - (b) Explicit association.

Notes

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Week 28

195-171

⊙ HARDWARE MODELING ISSUES

→ In terms of the hardware realization, the values computed can be assigned to:

- A "wire"
- A "flip-flop" (edge triggered storage cell)
- A "latch" (level triggered storage cell)

→ A variable in verilog can be either "net" or "register"

- A "net" data type always map to a "wire" ~~or "register"~~, during synthesis.
- A "register" data type maps either to "wire" or a "storage cell" depending upon the context under which a value assigned.

```
module reg_maps_to_wire (A,B,C,F1,F2);
    input A,B,C;
    output F1,F2;
    wire A,B,C;
    reg F1,F2;

    always @ (A or B or C)
    begin
        F1 = ~(A & B);
        F2 = F1 ^ C;
    end
endmodule
```

Notes

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196-170

LECTURE ⇒ (9) VERILOG OPERATORS

- Arithmatic operators:

+	unary (sign) plus
-	unary (sign) minus
+	binary plus (add)
-	binary minus (subtract)
*	multiply
/	devide
%	modulus
**	exponentiation

Example
- (b+c) [binary operator
(a-b) + (c*d)
a % b
a ** 3

- Logical operators:

!	logical negation (inverter)
&&	logical AND
||	logical OR

example
(clear && ack)
(a || b)
!(a && b)
((a>b) && !(b>c))

- The value 0 is treated as logical FALSE while any non-zero value is treated as TRUE.
- logical operators return either 0 (FALSE) or 1 (TRUE)

→ RELATIONAL OPERATOR

!=	not equal
==	equal
>=	greater or equal
<=	less or equal
>	greater
<	less

eg →
(a != b)
((a+b) == (c-d))
(count <= 0)

Notes

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Week 28

197-169

- Relational Operators operate on numbers and Return Boolean value (true or false).

→ Bitwise operator

~	bitwise not
&	bitwise AND
|	Bitwise OR
^	Bwise XOR
~^	Bitwise XNOR

eg:
```
wire a, b, c, d, f1, f2, f3, f4;
assign f1 = a ~| b;
assign f2 = (a & b) | (b & c);
assig f3 = a ^ b ^ c;
```

- Bitwise operators operate on bits & return a value that is also a bit.

- Reduction operator accept a single word operand and produce a single bit as output.
- operator on all the bits within the word.

Reduction operator	
&	Bitwise AND
|	Bitwise OR
~&	Bitwise NAND
~|	Bitwise NOR
^	Bitwise exclusive-OR
~^	Bitwise exclusive-NOR

example:
```
wire [7:0] a, b, c;
wire F1, F2, F3;
assign a = 4'b0111;
assign b = 4'b1100;
assign c = 4'b0100;
assign f1 = ^a; // gives a 0
assign f2 = &(a^b); // gives a 0
assign F3 = ^a & ~^b // gives a 1
```

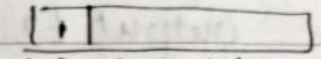
Notes ① The relational operator (>, <, <=, >=, ==, =) also evaluate to a 1 bit result (0 or 1).

→ Shift Operators:

>>	Shift right
<<	left shift
>>>	arithmatic shift right

eg:
```
wire [15:0] data target
assign target = data >>3;
assign target = data >> 2
```

∴ >>> :: 2's Complement number System



∴ Shift right → %2
Shift left → *2

→ Conditional operator:
Cond_expr ? true_expr : false_expr;

• Concatenation operator:
{..., ..., ...}
→ joins together bits from two or more comma-separated expressions

• Replication operator:
{n{m}}
→ joins together n copies of an expression m, where n is an constant

example
```
assign f = {a, b};
assign f = {a, 3'101, b}
assign f = {x[2], y[0], a};
assign f = {2'b10, 3{2'b01}};
```

① Example
```
module operator_example (x, y, f1, f2);
    input x, y;
    output f1, f2;
    wire [2:0] x, y; wire [4:0] f1; wire f2
    assign f1 = x[4:0] & y[4:0];
    assign f2 = x[2] ~^ f1[2];
    assign f2 ~& X;
    assign f1 = f2 & x[2:5] : x[4:0];
```

Notes

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Week 29

199-167

// A 8-bit Adder description

```
module parallel_adder (sum, count, in1, in2, cin);
    input [7:0] in1, in2;
    input cin;
    output [7:0] sum;
    output cout;
    assign #20 {count, sum} = in1 + in2 + cin;
endmodule
```

⊙ OPERATOR PRECEDENCE

- operator on same line have the same precedence.
- All operators associate left or right in an expression except ?:
- parenthesis can be used to change the precedence.

∴ ==, != Check for equality

===, !== exact equality

+ - ! ~ (unary)	
**	
* / %	
<< >> >>>	
< <= > >=	
== != === !==	
& ~&	
^ ~^	
| ~|	
&&	
||	
?:	

Increasing precedence

⊙ Some POINTS :

- The presence of 'z' or 'x' in reg or wire being used in an arithmetic expression or result in the whole expression being unknown ('x')

⊙ The logical operators (!, &&, ||) all evaluate to a 1-bit result (0, 1, or x).

Notes

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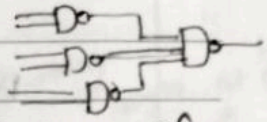
200-166

Lecture ⇒ (10) VERILOG MODELING Examples.

Modeling

Behavioral ⋮ Starting point ⟶ Structural ⋮ Hardware Implementation

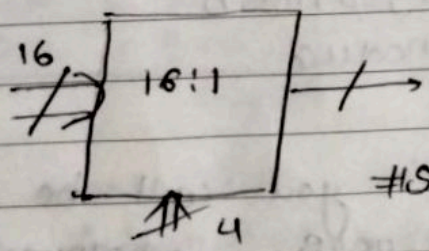
CY = 4 NAND gate



Example ① The structural hierarchical description of a 16-to-1 multiplexer.

ⓐ using pure behavioral modeling
ⓑ structural modeling using 4-to-1 multiplexer specified using behavioral model.
ⓒ make structural modeling of 4-to-1 multiplexer using behavioral modeling of 2-to-1 multiplexer.
ⓓ make structural gate level modeling of 2-to-1 multiplexer, to have a complete structural hierarchical description.

Sol



#Select line = $\log_2$ (input line)

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VERSION 1 : using pure behavioral modeling

Notes

```
module mux16to1 (in, sel, out);
    input [15:0] in;
    input [3:0] sel;
    output out;
    assign out = in[sel];
endmodule
```

- Selects one of the 'input' bits depending upon the value of 'Select Line (Sel)'.

```
module muxtb;
  reg [15:0]A; reg [3:0]S; wire F;

mux16to1 M(.in(A), .sel(S), .out(F));

initial
 begin
    $dumpfile("mux16to1.vcd")
    $dumpvariables(0, muxtest);
    $monitor($time," A=%b, S=%b, F=%b",
                    A,S,F);
    #5  A=16'h3f0a; S=4'h0;
    #5  S=4'h1;
    #5  S=4'h6;
    #5  S=4'hc;
    #5 $finish
 endmodule
```

Test bench purpose :- you will be testing your module once whatever you specified those values will be applying to the input and we will seeing what the outputs are coming. that is the purpose of the test bench.

Notes [explaining test Bench]

→ $monitor → we are monitoring a few of the variables

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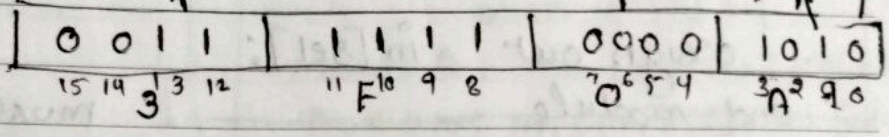
→ $time → it is a System variable that indicates the Simulation time.

→ "A = %h" → mean see like, the we want to print the values A,S,F . h is hexadecimal specifier ~~because~~ because A is 16 bit number, S is 4 bit and F is single bit (F = %b (binary)).

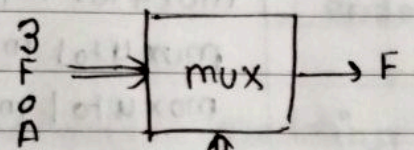
→ #5 A = 16'h 3F0a , (20) delay 3 FOA →

20 · 3FOA →



(15) delay
delay to at 5 time

mux :



S → select line
S = 4'h 0

Select line = 0
Select line = 1
Select line = 6
S = C = 12

at time 0 not in ticks ↑ output

0A	= xxxx,	S= x	, F = x
5A	= 3f0a,	S = 0	; F = 0
10A	= 3f0a,	S = 1	, F = 1
15A	= 3f0A	, S = 6	, F = 0
20A	= 3f0A	, S = C	, F = 1

time (delay) ↑ ↓ input

→ this is tabular form

$dumpfile → It means these variations with time this information you can also dump in to a file VCD.

"mux 16 to 1 .vcd" → file name

Notes

→ why need dumpfile and dump variable?

→ seeing the simulation output in a tabular form or just on the screen is not good enough in form for text.

AUGUST

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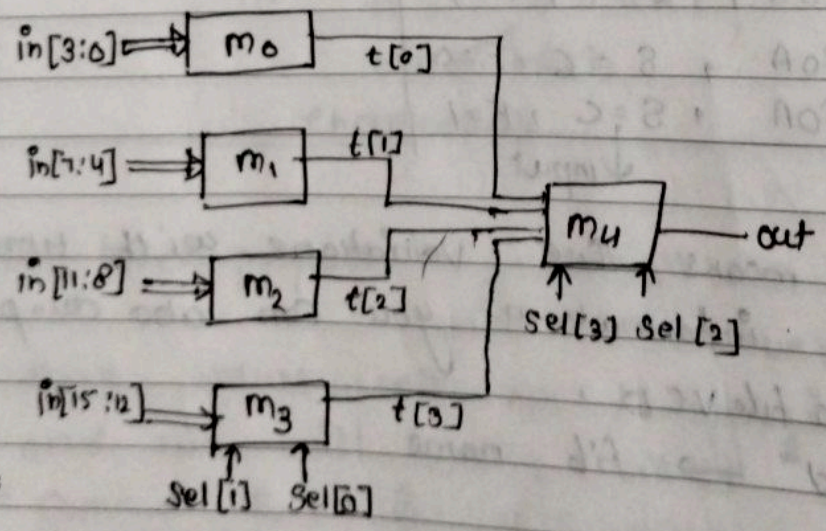
→ VERSION @ Behavioral modeling OF 4-to-1 mux
STRUCTURAL modeling OF 16-to-1 mux

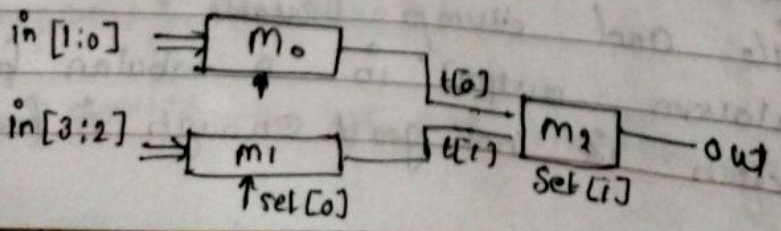
```
module mux 4 to 1 (in, sel, out);
    input [3:0] in;
    input [1:0] sel;
    output out;

    assign out = in [sel];
end module
```

```
module mux 16 to 1 (in, sel, out);
    input [15:0] in;
    input [3:0] sel;
    output out;
    wire [3:0] t;

    mux4to1 m0 (in[3:0], sel[1:0], t[0]);
    mux4to1 m1 (in[7:4], sel[1:0], t[1]);
    mux4to1 m2 (in[11:8], sel[1:0], t[2]);
    mux4to1 m3 (in[15:12], sel[1:0], t[3]);
    mux4to1 m4 (t, sel[3:2], out);
endmodule
```

: Circuit diagram → 16-to-1 multiplexer using 4-to-1 multiplexer



Notes



↓ 4 to 1 multiplexer using 2-to-1 multiplexer

→ VERSION ③ Behavioral modeling OF 2-to-1 mux
Structural modeling OF 4-to-1 mux

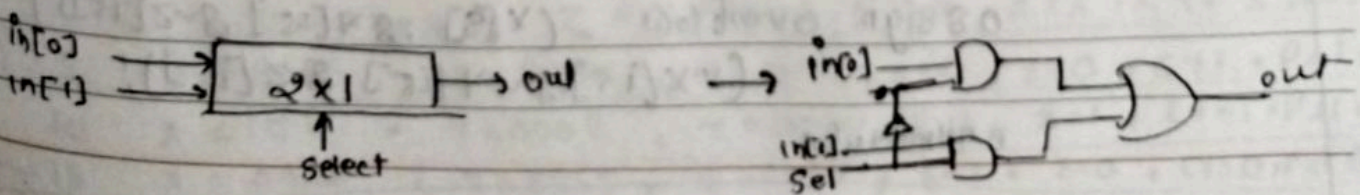
```
module mux2to1 (in, sel, out)
    input [1:0] in;
    input sel;
    output out;
    assign out = in[sel];
endmodule
```

```
module mux4to1 (in, sel, out);
    input [3:0] in;
    input [1:0] sel;
    output out;
    wire [1:0] t;
    mux2to1 m0 (in[1:0], sel[0], t[0]);
    mux2to1 m1 (in[3:2], sel[0], t[1]);
endmodule
```

VERSION ④ Structural modeling OF 2-to-1 mux

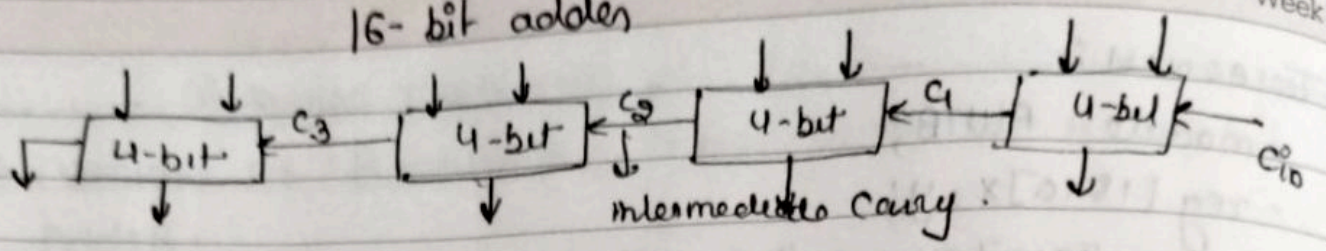
```
module mux2to1 (in, sel, out);
    input [1:0] in;
    input sel;
    output out;
    wire t1, t2, t3;

    NOT G1 (t1, sel);
    AND G2 (t2, in[0], t1);
    AND G3 (t3, in[1], sel);
    OR G4 (out, t2, t3);
endmodule
```

Point to NOTE:
- Same test bench can used for all the version
- Two Versions illustrate hierarchical refinement of design.



Notes

16- bit adder



VERSION ② Structural description of 16-bit adder using 4-bit adder blocks (with ripple carry Between blocks).

```
module ALU (x,y,z, Sign, zero, carry, Parity
                                    overflow);
    Input [15:0] x, y;
    Output [15:0] z;
    output Sign, zero, parity, overflow;
    wire C [3:1];

    assign Sign = z[15];
    assign zero = ~|z;
    assign Parity = ~^z;
    assign overflow = (x[15] & y[15] & ~z[15])
                      (~x[15] & ~y[15] & z[15]);
    adder4 A0 (z[3:0], C[1], x[3:0], y[3:0], 1'b0);
    adder4 A1 (z[7:4], C[2], x[7:4], y[7:4], C[1]);
    adder4 A2 (z[11:8], C[3], x[11:8], y[11:8], c[2]);
    adder4 A3 (z[15:12], carry, x[15:12], y[5:12], C[3]);
endmodule
```

Notes

↪ BEHAVIORAL description of a 4-bit Adder:

```
module adder4 (S, Cout, A, B, Cin)
  input [3:0] A, B;   input Cin;
  output [3:0] S;     output Cout;

  assign {Cout S} = A+B+Cin;
endmodule
```

VESION → ③ STRUCTURAL MODELING OF Ripple Carry Adder

```
module adder4 (S, Cout, A, B, Cin);
 input [3:0] A, B;   input Cin;
 output [3:0] S;     output Cout;
 wire C1, C2, C3;

 fulladder FA0 (S[0], C1, A[0], B[0], Cin);
 full adder FA1 (S[1], C2, A[1], B[1], C1);
 full adder FA2 (S[2], C3, A[2], B[2], C2);
 fulladder FA3 (S[3], Cout, A[3], B[3], C3);

 endmodule
```

```
module full adder (S, Cout, a, b, c);
 input a, b, c;
 output S, Cout;
 wire S1, C1, C2;
 xor G1(S1, a, b); G2 (S, S1, C),
    G3 (Cout, S1, C1);
 and G4 (G1, a, b), G5(C2, S1, C);
 endmodule
```

Notes

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Week 31

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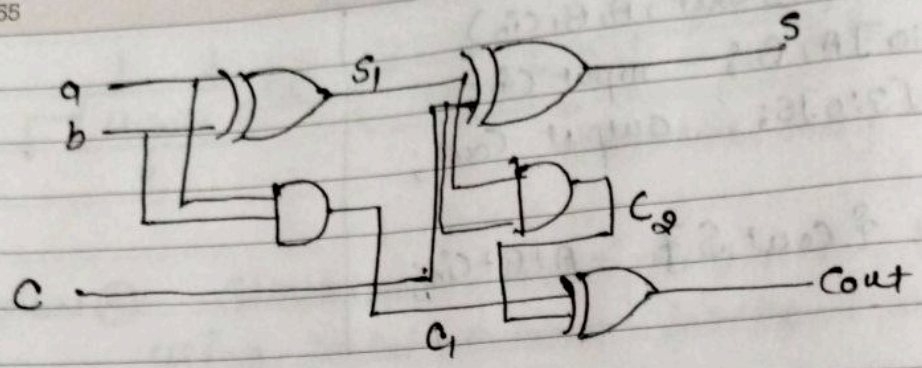


full-adder.

VERSION-4 structural modeling of carry lookahead Adder

```
module adder4 (S, Cout, A, B, Cin);
  input [3:0] A, B;   input Cin;
  output [3:0] S;     output Cout;
  wire P0, g0, P1, g1, P2, g2, P3, g3;
  wire C1, C2, C3;

  assign P0 = A[0] ^ B[0], P1 = A[1] ^ B[1],
         P2 = A[2] ^ B[2], P3 = A[3] ^ B[3];

  assign g0 = A[0] & B[0], g1 = A[1] & B[1],
         g2 = A[2] & B[2], g3 = A[3] & B[3];

  assign C1 = g0 | (P0 & Cin), C2 = g1 | (P1 & g0) |
         (P1 & P0 & Cin), C3 = g2 | (P2 & g1) | (P2 & P1 & g0) |
         (P2 & P1 & P0 & Cin),
         Cout = g3 | (P3 & g2) | (P3 & P2 & g1) | (P3 & P2 & P1 & g0) |
         (P3 & P2 & P1 & P0 & Cin);
```

Notes

```
assign S[0] = P0 ^ Cin;   // sum
       S[1] = P1 ^ C1,
       S[2] = P2 ^ C2,
       S[3] = P3 ^ C3;
endmodule
```

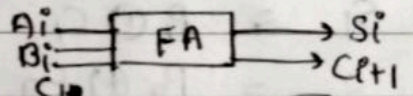
→ How does Carry look-ahead adder work?

- The propagation delay of an n-bit ripple carry adder is proportional to n.
  - due to the rippling effect of carry sequentially from one stage to the next.
- One possible way to speedup the addition.
  - Generate the carry signals for the various stages in Parallel.
  - Time Complexity reduces from O(n) to O(1).
  - Hardware Complexity increse rapidly with n.

- Consider the i-th stage in the addition process.
- We define the Carry generate and Carry propogate function as;

Carry generate → $g_i = A_i B_i$

Carry propogate → $P_i = A_i \oplus B_i$



$C_{i+1} = g_i + P_i C_i$

- $g_i = 1$ represents the Condition when a carry is generate in stage -i independent of the other stages.
- $P_i = 1$ represents the Condition when an input Carry C_i will be propogated to the output Carry C_{i+1}.

Notes

Unrolling the Recurrence

$C_{i+1} = g_i + P_i C_i = g_i + P_i(g_{i-1} + P_{i-1} C_{i-1}) \Rightarrow g_i + P_i g_{i-1} + P_i P_{i-1} C_{i-1}$

$= g_i + P_i g_{i-1} + P_i P_{i-1}(g_{i-2} + P_{i-2} C_{i-2})$

$= g_i + P_i g_{i-1} + P_i P_{i-1} g_{i-2} + P_i P_{i-1} P_{i-2} C_{i-2} = \cdots$

$$C_{i+1} = g_i + \sum_{k=0}^{i-1} g_k \prod_{j=k+1}^{i} P_j + C_0 \prod_{j=0}^{i} P_j$$

Generation of the Carry and Sum bits:

$C_4 = g_3 + g_2 P_3 + g_1 P_2 P_3 + g_0 P_1 P_2 P_3 + C_0 P_0 P_1 P_2 P_3$

$C_3 = g_2 + g_1 P_2 + g_0 P_1 P_2 + C_0 P_0 P_1 P_2$

$C_2 = g_1 + g_0 P_1 + C_0 P_0 P_1$

$C_1 = g_0 + C_0 P_0$

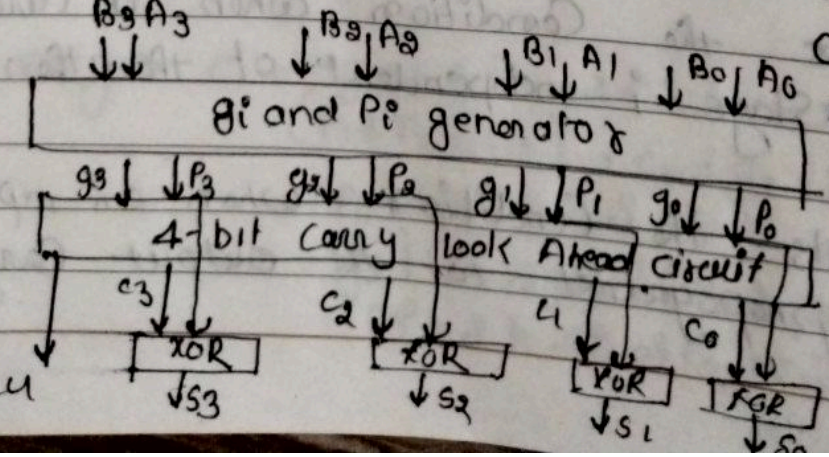
$S_0 = A_0 \oplus B_0 \oplus C_0 = P_0 \oplus C_0$

$S_1 = P_1 \oplus C_1$

$S_2 = P_2 \oplus C_2$

$S_3 = P_3 \oplus C_3$

4 AND2 gates
3 AND 3 gates
2 AND 4 gates
1 AND 5 gate
1 OR 2, 1 OR 3, 1 OR 4 and 1 OR 5 gate
4 XOR 2 gates



01 August Saturday 2020 Week 31

Adityagi-verilg

214-152

LECTURE ⇒ (13) VERILOG DESCRIPTION STYLE

- Two different styles of description:
  1. Data Flow
     - Continuous assignment using assignment statements
  2. Behavioral
     - Procedural assignment using procedural statements
       - Blocking
       - Non-blocking

     Similar to a program in high level language.

- Two different styles of description:
  1. Data flow style : Continuous Assignment
     - Identified by the keyword "assign".
     - Forms a static binding between:
       - The "net" being assigned on the left-hand side (LHS).
       - The expression on the right-hand side (RHS), which may consist of both "net" and "register" type variables.

```
assign a = b+c;
assign Sign = Z[15];
```

     - The assignment is continuously active:
       - Almost exclusively used to model Combinational Circuits.
     - We shall also see some example of modeling Sequential Circuit elements.
     - Some points to note:
       - A Verilog module can contain any numbers of "assign"

02 Sunday

Notes

- Typically, the "assign" statements are followed by procedural descriptions.
- The "assign" statement are used to model behavioral descriptions.
- We shall illustrate various usages of "assign" statement for modeling Combinational and also some Sequential logic blocks.

module
[Signal declaration
{ assign statements
{ = e statement
end module

eg:-

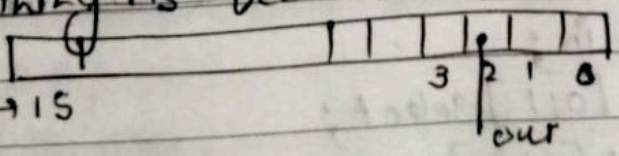
```
module general_mux(data, sel, out);
input [15:0] data;
input [3:0] select;
output out;
assign out = data[select];
endmodule
```

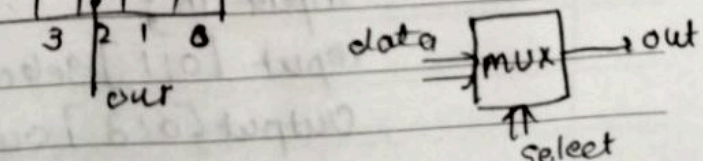
non constant index in expression on RHS generates a mux.

- Point to note:
  - Whenever there is an array reference on the RHS with a variable index, a mux is generated by the Synthesis Tool.
  - If the index is a constant, just a wire will be generated.

Example: assign out = data[2];

→ data is nothing its vector. vector means Collection of bits

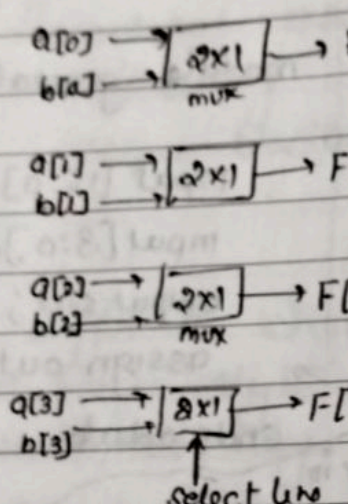




Notes

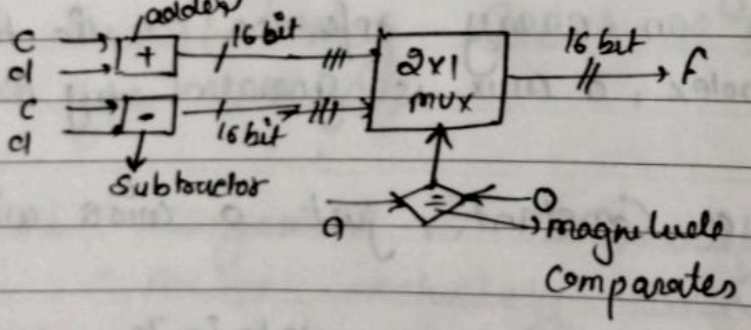
```
module generate_set_of_mux (a, b, f, sel);
    input [0:3] a, b;
    input sel;
    output [0:3] F;
    assign f = sel ? a : b;
endmodule
```

← conditional operator generates a mux



⊙ Point to NOTE :-
- whenever a conditional is encountered in the RHS of an expression, a 2 to 1 mux is generated
- in the previous eg, since the variables "a", "b", and "F" are vectors, an array of 2-to-1 mux-es are generated.

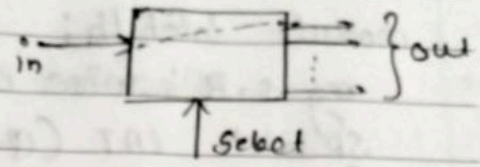
→ what hardware will be generated by the following
assign f = (a==0) ? (c+d) : (c-d);




```
module generate_decoder (out, in, select);
    input in;
    input [0:1] select;
    output [0:3] out;
    assign out[select] = in;
endmodule
```

Notes

Non-Constant index in expression on LHS generates a decoder



- Point to NOTE :-
  - A Constant index in the expression on the LHS will not generate a decoder.
    → eg : assign out[5] = in;
    This will be generate a wire Connection.
  - AS a rule of thumb, whenever the Synthesis tool detects a variable index in the LHS, a decoder is generated.

```
module level_sensitive_latch (D,Q, En);
    input D, En;
    output Q;
    assign Q = En ? D : Q;
endmodule
```

Here is an example to describe a Sequential logic element using "assign" statement.

En	D	Q_n
0	X	Q_{n-1}
1	0	0
1	1	1

generate a D-type latch

```
module SR_latch (Q, Qbar, S, R);
    input S, R;
    output Q, Qbar;
    assign Q = ~(R & Qbar);
    assign Qbar = ~(S & Q);
endmodule
```

Notes

06 August Thursday 2020

219-147

```
module latch_tb;
  reg S,R; wire Q,Qbar;
  SR_latch LAT (Q,Qbar,S,R);
  initial begin
    $monitor ($time, "S=%b, R=%b, Q=%b, Qbar=%b", S,R,Q,Qbar);
        S=1'b0; R=1'b1;
    #5  S=1'b1; R=1'b1;
    #5  S=1'b1; R=1'b0;
    #5  S=1'b1; R=1'b1;
    #5  S=1'b0; R=1'b0;
    #5  S=1'b1; R=1'b1;
  end
endmodule
```

Simulation output

#0	S=0,	R=1,	Q=0,	Qbar=1
#5	S=1,	R=1,	Q=0,	Qbar=1
#10	S=1,	R=0,	Q=1,	Qbar=0
#15	S=1,	R=1,	Q=1,	Qbar=0
#20	S=0,	R=0,	Q=1,	Qbar=1

Verilog lec⇒ (13) PROCEDURAL ASSIGNMENT

- Two kinds of procedural blocks are Supported in

Notes VERILOG:

- The "initial" block
  - executed once at the beginning of simulation.
  - used only in test bench & cannot used in Synthesis.

Week 32

220-146

- The "always" block
  - A continuous loop that never terminates

- The procedural block defines:
  - A Region of code containing Sequential Statements.
  - The statements execute in the order they are written

⊙ The "initial" Block

- All statement inside an "initial" statement Consists the an "itial block."
  - Grouped inside a "begin .... end" structure for multiple statements.
  - The statements starts at time 0, and execute only once.
  - If there are multiple "initial" blocks, all the blocks will start to execute Concurrently at time 0.
- The "initial" block is typically used to write test benches for simulation:
  - Specifies the stimulus to be applied to the design under test (DUT).
  - Specifies how the DUT outputs are to be displayed / handled.
  - Specifies the files where the waveform information is to be dumped.

```
initial
begin
  ...
end
```

} initial block

Notes

08 August Saturday 2020

Week 32

221-145

```
module testbench_example;
  reg a, b, Cin, Sum, Cout;
initial
  Cin = 1'b0;
initial
  begin
  #5 a = 1'b1; b = 1'b1;
  #5 b = 1'b0;
  end
initial
  #25 $finish;
endmodule
```

- The three "initial" blocks execute concurrently.
- The first block executes at time 0.
- The third block terminates simulation at time 25 units

⊙ Some short cuts in Declarations

↔ "output" and "reg" can be declared together in the same statement.

output reg [7:0] data;

instead of output [7:0] data; reg [7:0] data;

↔ A variable can be initialized when it is declared.

reg clock = 0;

instead of reg clock; initial clock = 0;

09 Sunday ⇒ The "always" Block

Notes All behavioral Statements inside an "always" Statement Constitute an "always block".

- multiple Statements are grouped using "begin ... end"

- An "Always" statements starts at time 0 and execute the statements inside the block repeatedly, and never stops.
  - used to model a block of activity that is repeated indefinitly in a digital circuit.
  - for example, a clock signal that is generated continuously.
  - we can specify delay for simulation; however for real circuits; the clock generator will be active as long as there is power supply.

```
always
begin
  ...
  ...
end
```
→ always block

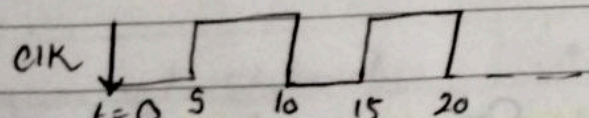
```
module generating_clock;
  output reg clk;

initial
  clk = 1'b0; // initialized to 0 at time 0

always
  #5 clk = ~clk; // toggle after time 5unit

intial
  #500 $Anish;
endmodule
```

"initial" and "always" blocks can execute within the same verilog module.
- They all execute concurrently; "initial" only once and "always" repeatedly



Notes → A module can contain any number of "always" blocks, all of which execute concurrently.
→ The @(event_expression) part is required for both Combinational and Sequential circuit descriptions

11 August Tuesday 2020

224-142

* Basic syntax of "always" block:

```
always @(event expression)
begin
   Sequential statement_1;
   Sequential_statement_2;
   :::::
   Sequential_statement_n;
end
```

- only "reg" type variable can be assign within a "intial" or "always" block.

→ BASIC reason:

→ The sequential "always" block executes only when the event expression triggers

- at other times the block is doing nothing
- an object being assigned to must therefore remember the last value assigned (not continuously driven).
- so, only "reg" type variable can be assign within the "always" block.
- of course, any kind of variable may appear in the event expression (reg, wire, etc).

SEQUENTIAL STATEMENT'S IN VERILOG

Notes

- in verilog, one of more Sequential statement can be present inside an "initial" or "always" block.

- The statements are executed sequentially.
- multiple assignment statement inside a "begin--end" block may either execute sequentially or concurrently depending upon on the type of assignment.
  - Two type of assignment statement: blocking ($a = b+c;$) or non-blocking ($a <= b+c;$).
- The Sequential statements are explained next.

@ begin ---- and

```
begin
  Sequential_statement_1;
  Sequential_statement_2;
  ---
  Sequential_statement_n;
end
```

- A number of Sequential Statements can be grouped together using "begin...end".
- If n=1, "begin...end" is not required.

(b) if ---- else

```
if (<expression>)
  Sequential_statement;
```

```
if (<expression>)
  Sequential_statement;
else
  Sequential_statement
```

```
if (<expression1>)
  Sequential_statement;
else if (<expression2>)
  Sequential_statement;
else default statement;
```

- each Sequential Statement can be a single statement or a group of statement within "begin---end".

Notes

© Case

```
case (<expression>)
  expr1 : Sequential_statment;
  expr2 :   "          "   ;
  - - - - - ;
  exprn : sequential statement;
  default: defuld_statement;
endcase
```

- Each Sequential_statement can be a single statement or a groups of statement within "begin ... end".
- can replace a complex "if ... else" statement for multiway branching.

- The expression is compared to the alternatives (exp1, exp2, etc) in the order they are written
- if none of the alternative matches the default statement is executed.

⊙ Two variation: "casez" and "casex"

- The "casez" statements treats all "z" value in the case alternative or are case expression as don't cares.
- The casex statement treats all "x" and "z" value in the care item as don't care

```
reg [3:0] state ; integer next_state;
case x (state)
  4'b1xxx : next state = 0;
  4'bx1xx : next_state = 1;
  4'bxx1x : next_state = 2;
  4'bxxx1 : next_state = 3;
  default ; next_state = 0;
endcase
```

Notes

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Lecture :- (14) PROCEDURAL ASSIGNMENT

(a) "while" loop

```
while(<expression>)
    Sequential_statement;
```

- The "while" loop executes until the expression is not true
- The Sequential_statement can be a single statement or a group of statements within "begin ... end".

example

```
integer mycount;
intial begin
    mycount=0;
    while (mycount <= 250)
    begin
        $display ("my count : %d", mycount);
        mycount = mycount+1;
    end
endmodule
```

(c) "for" loop

```
for (exp1; exp2; exp3)
    Sequential_statement;
```

- The "for" loop executes as long as the expression exp2 is true
- The Sequential_statement can be a single statement or a group of statements "begin ---- end"

Notes

- The "for" loop consist of three parts:
  - (a) An initial condition (exp1).
  - (b) A check to see if the terminating condition is true (exp2).
  - (c) A procedural assignment to change the value of the control variable (exp3)
- The "for" loops can be conveniently used to initialize an array or memory.

Example

```
integer mycount;
reg [100:1] data;
integer i;
initial
ex① for (mycount=0; mycount<=255; mycount = mycount+1)
     $display ("my count: %d", mycount);

ex② initial
     for(i=1; i<=100; i=i+1)
        data[i] = 1'b0;
```

④ "repeat" loop

```
repeat (<expressions>)
   Sequential_statement;
```

- The "repeat" Construct executes the loop a fixed number of times
- It cannot be used to loop on a general logical expression like "while".

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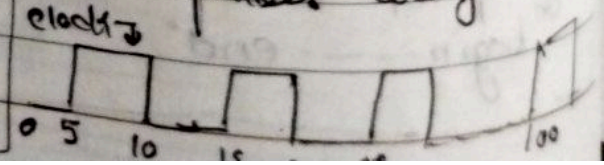
example

```
reg clock;
initial begin
    clock = 1'b0;
    repeat (100)
      #5 clock = ~clock;
end
```

exactly 100 clock pulses are generated



Notes

(9) "FOREVER" loop

```
forever
    Sequential_statement;
```

- The "forever" loop is typically used along with timing specifier.
  - if delay is not specified the simulator, the simulator would execute this statement indefinitely without advancing $time.
- Rest of design will never be executed.

- The "forever" Construct does not use any expression and executes forever until $finish is encountered the testbench
  - Equivalent a "while" loop for which the expression is always true.
- The Sequential_statement can be a single statement or a groups of statement within "begin ... end".

```
// clock generation using "forever" Construct reg clk;
    intial
        begin
            clk = 1'b0;
            forever #5 clok = ~clk; //clk period of 10 units
        end
```

OTHER CONSTRUCTS - Available

#(time value)	• mask a block suspend for "time_value" units of time. • The time unit can be specified using the 'timescale Command.

Notes

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231-135

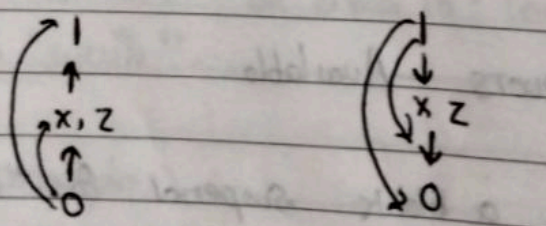
@(event_expression)

- makes a Block suspend for "time-value" units of time.
- The time unit can be specified using the 'timescale compiler directive.

- makes a Block suspend until "event_expression" triggers.
- Various keywords associated with "event_expression" shall be discussed with examples.

- The event expression specifies the event that is required to resume execution of the procedural block.
- The event can be any one of the following:
  - (a) Change of a single value.
  - (b) Positive or negative edge occuring on signal (Posedge or negedge).
  - (c) List of above-mentioned events, separated by "or" or comma.

- A "Posedge" is any transition from {0, x, z} to 1, and from 0 to {z, x}.



for Posedge negedge

```
always @(Posedge x)
{...
```

Notes

Example

```
→ @(in)
→ @(a or b or c)
→ @(a, b, c)
```

// "in" changes
// any of "a", "b", "c" changes
// -- do --

- @ (Posedge clk) // Posedge of "clk"
- @ (Posedge clk or negative reset) // Positive edge of "clk" or negetive edge of "reset"
- @ (*) // any variable changes

Sample // D Flip-flop with Syncronous set and reset

```
module dff (q, qbar, d, set, reset, clk);
input reg q;  output qbar;

assign qbar = ~q;
always @ (Posedge clk)
 begin
    if (reset ==0) q<=0;
    else if (set ==0) q<=1;
    else q<=d;
 end
endmodule
```

Example // D flip-flop with asynchronous set and reset

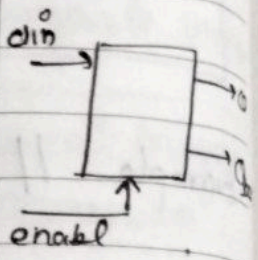
```
module dff (q, qbar, d, set, reset, clk);
 input d, set, reset qbar;
 output reg q; output qbar;
 assign qbar = ~q;
always @ (Posedge clk or negedge set or negedge reset)
 begin
    if (reset ==0)  q<=0;
    else if (set ==0)  q<=1;
    else q<=d;
endmodule
```

Notes

// Transparent (means no clock) latch with enable

```
module latch (q, qbar, din, enable);
    input din, enable;
    output reg q;

    assign qbar = ~q;
    always @ (din or enable)
      begin
        if (enable) q = din;
      end
endmodule
```



Latch means level triggers

Lecture :- (15) PROCEDURAL ASSIGNMENT EXAMPLES

// A Combinational logic example ~~module~~ mux21

```
module mux21 (in1, in0, s, f);
    input in1, in0, s;
    output reg f;

    always @ (in1 or in0 or s)
      if (s)
        f = in1;
      else
        f = in0;
endmodule
```

Notes

- An event expression in the "always" block triggers whenever at least on of "in1", "in0" or "s" changes
- The "or" key words specifies the condition

// A Combinational logic example

```
module mux2_1 (in1, in0, s, f);
    input in1, in0, s;
    output reg f;

    always @(in1, in0, s)
        if (s)
            f = in1;
        else
            f = in0;
    endmodule
```

- An alternate way to specify the event condition by using comma instead of "or".
- Supported in later version of verilog.

② A Combinational logic example

```
module mux2_1 (in1, in0, s, f);
    input in1, in0, s;
    output reg f;
    always @(*)
        if (s)
            f = in1;
        else f = in0;
```

Notes

235-131

• An alternate way to specify the event condition by using a "*", instead of naming the variable.

→ "*" is activated whenever any of the variable change.

● A Sequential logic Example

```
module dff_negedge (D, Clock, Q, Qbar);
    input D, clock;
    output reg Q, Qbar;

    always @(negedge clk)
    begin
        Q = D;
        Qbar = ~D;
    end
endmodule
```

• The keyword "negedge" means at the negative going edge of the specified signal.

23 Sunday • Similarly, we can use "Posedge".

Notes • We can combine various triggering conditions by separating them by commas or "or".

// 4-bit Counter with asynchronous reset

```
module Counter (clk, rst, count);

  input clk, rst;
  output reg [3:0] count;

  always @(posedge clk or posedge rst)
   begin
     if(rst)
      count <=0;
     else
      count <= count+1;
   end
endmodule
```

→ The event Condition triggers when either a Positive edge of "clk" comes, or a Positive edge of "rst".

// Another Sequential logic Example

```
module incomp_state_spec (curr_state, flag);
       input [0:1] curr-state;
       output reg [0:1] flag;
       always @(curr_state)
         case (curr_state)
            0,1 : flag = 2;
             3  : flag = 0;
         endcase
endmodule
```

Notes

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238-128

Lecture :⇒ (16) INTRODUCTION to Blocking AND Non Blocking

PROCEDURAL ASSIGNMENT:

- Procedural assignment statement can be used to update Variable of types "reg", "integer", "real" or "time".
- The value assigned to a variable remains unchanged until another procedural assignment statement assigns a new value to the variable.
  → this is different from Continuous assignment (using "assign") that result in the expression on the RHS to Continously drive the "net" type variable on the left.

→ Two types of Procedural assignment Statements:
(a) Blocking (denoted by "=").
(b) Non-blocking (" "<=")

- The LEFT-hand side of a procedural assignment can be one of:
(a) A register type variable ("reg", "integer", "real", or "time")
(b) A bit select of these variable (eg Sum[15])
(c) A Part Select of these variable (eg IR[31:26])
(d) A Concatenation of any of the above.

- The right-hand side can be any expression consisting of "net" and "register" type variable that evaluates to a value.
- Procedural assignment statement can only appear within procedural blocks ("initial" or "always").

Notes

239-127

(i) Blocking Assignment

→ General Syntax

variable_name = [delay_or_event_control] expression;

→ The "=" operator is used to specify blocking assignment

→ Blocking assignment statement are executed in the order they are specified in a procedural block.

- The target of an assignment gets update before the next Sequential Statement in the procedural block is executed.

- They do not blocks execution of statements in other procedural blocks.

- This is the recommended style for modeling Combinational logic.

• Blocking assignment can also generate Sequential circuit elements during synthesis (eg incomplete specification in multi-way branching with "case").

• An example of blocking assignment

```
integer a, b, c;
initial
  begin
    a = 10; b = 2; c = 15;
    a = b+c
    b = a+5
    c = a-b;
  end
```

240-126

```
module blocking_example;
  reg x,y,z;
  reg [31:0] A, B;    integer Sum;

  intial begin
    x=1'b0 ; y=1'b0 ; z=1'b1          //at time=0
    Sum=1;                            //at time=0
    A=31'b0 ;  B=31'hababababab;      //at time=0
    #5  A[5] = 1'b1;                  //at time=5
    #10  B[31:29] = {x,y,z};          //at time=15
         Sum = Sum+5;                 //at time=15
  end
endmodule
```

→ Simulation of An Example :-

- For 'Blocking Assignment' :-

Ex1

```
module blocking_assign ;
  integer a, b, c, d ;
  always @(*)
    repeat (4)
    begin
      #5  a = b+c;
      #5  d = a-8;
      #5  b = d+10;
      #5  c = c+1;
    end
```

* → it means any variable changes.

Notes

(ii) NON-BLOCKING ASSIGNMENT

- General Syntax:

variable_name <= [delay_or_event_control] expression;

- The "<=" operator is used to specify non-blocking assignment.
- Non-blocking assignment statements allows scheduling of assignment without blocking execution of statement that follows within the procedural block.
  - The assignment to the target gets scheduled for the end of the simulation cycle (at the end of the procedural block).
- statement subsequent to the instruction under consideration are not blocked by the assignment.
- allows concurrent procedural assignment, suitable for sequential logic.

- This is the recommended style for modeling sequential logic
- Several "reg" type variable can be assigned synchronously under the control of a common clock.

```
integer a, b, c;
initial begin
        a=10; b=20; c=15;
end
initial begin
        a<= #5 b+c;
        b<= #5 a+5;
        c<= #5 a-b;
end
```

Notes

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Week 35

242-124

eg → Non-blocking assignment with a clock :-

```
always @ (Posedge clk)
    begin
        a <= b & c;
        b <= a ^ d;
        c <= a | b;
    end
```

All assignments take place synchronously at the rising edge of the clock.

mp

◎ Swaping value of two variables "a" and "b"

```
always @ (Posedge clk)
    a = b;
always @ (Posedge clk)
    b = a;
```

- Either a=b will execute before b=a, or vice versa depending on simulator implementation,
- Both registers will get the same value (either "a" or "b").
- Race Condition

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-in case of non-Blocking assignment

Notes

```
always @ (Posedge clk)
    a <= b;
always @ (Posedge clk)
    b <= a;
```

- Here the variable are correctly swapped.
- All RHS variable are read first and assigned to LHS variables at the positive clock edge.

⊙ Trying to swap using blocking assignment

```
always @(posedge clk)
  begin
      a = b;
      b = a;
  end
```

→ both "a" and "b" will be getting the value previously stored in "b".

⊙
```
always @(posedge clk)
  begin
      ta = a;
      tb = b;
      a = tb;
      b = ta;
  end
```

- Correct swapping will occur, but we need to two temporary variable "ta" and "tb".

⊙
```
module nonblocking_assgn;
integer a, b, c, d;
reg clock
always @ (posedge clock)
begin
```

245-121

```
a <= b+c;
d <= a-8;
b <= d+10;
c <= c+1;
end
```

⊙ TEST BENCH

```
initial
  begin
    $monitor ($time, "a=%d , b=%d , c=%d,
              d=%d", a, b, c, d);
    a=30 ; b=20 ; c=15 ; d=8 ;
    clock = 0;
    forever #5 clock = ~clock;
  end
initial
    #100 $finish;
endmodule
```

⊙ SOME RULE TO FOLLOWED :-

- It is recommended that blocking and non-blocking assignments are not mixed in the same "always" block.
  - Simulator may allow, but this is not good design practice.
- Verilog synthesized ignores the delay specified in a procedural assignment statement (blocking or nonblocking)
  - may lead to functional mismatch between the design model and the synthesized netlist.
- A variable cannot appear as the target of both a blocking and a nonblocking assignment.
  - This is not permissible →

```
n = n+5
n <= y;
```

02 September Wednesday 2020 NPTEL Asli-Iyogi-Verilog

246-120

Lecture: (11) INTRODUCTION

→ We shall be looking at some examples of modeling using blocking and non-blocking assignments.

→ Objective is to get a feel of the type of assignment statement to use for some particular scenario.

→ Avoid some of the "not-so-good" design practices in modeling.

// 8-to-1 multiplexer : Behavioural description

```
module mux_8to1 (in, sel, out);
    input [8:0] in; input [2:0] sel;
    output reg out;
    always @(*)
    begin
        case (sel)
        3'b000 : out = in[0];
        3'b001 : out = in[1];
        3'b010 : out = in[2];
        3'b011 : out = in[3];
        3'b100 : out = in[4];
        3'b101 : out = in[5];
        3'b110 : out = in[6];
        3'b111 : out = in[7];
        default : out = 1'bx;
        endcase
    end
endmodule
```

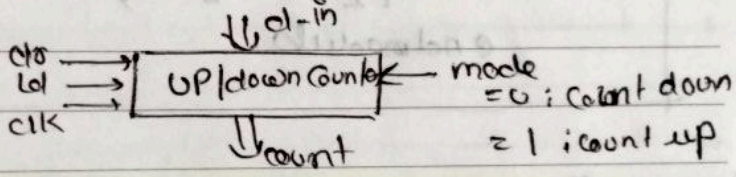
Notes

// up-down Counter (Synchronous clear)

load input → ld, count → cout

```
module Counter (mode, clr, ld, din, clk, cout);
    input mode, clr, ld, clk;
    input [0:7] din;
    output reg [0:7] Count

always @(Posedge clk)
    if (ld)          Count <= din;
    else if (clr)    Count <= 0;
    else if (mode)   Count <= Count+1;
    else             Count <= Count-1;
endmodule
```



// Parameterized design : An N-bit Counter

```
module Counter (clear, clock, Count);
    Parameter N=7;
    Input clear, clock;
    output reg [0:N] Count;

always @(negedge clock)
    if (clear)
        Count <= 0;
    else
        Count <= Count +1;
endmodule
```

→ make a design general for any number of bits.
- using the keyword "Parameter".
- Parameter value are substituted before Simulator or Synthesis.

◉ // using more than one clocks in a module

```
module multiple_clk (clk1, clk2, a, b, c, f1, f2);
output reg f1, f2; input clk1, clk2, a, b, c;
always @(posedge clk1)
    f1 <= a & b;
always @(negedge clk2)
    f2 <= b ^ c;
endmodule
```

◉ // using multiple edges of the same clock

```
module multi_edge_clk (a, b, f, clk);
  input a, b, clk;
  output reg f; reg t;
  always @(posedge clk)
      f <= t & b;
  always @(negedge clk)
      t <= a | b;
  endmodule
```

Notes

// A Ring Counter

```
module ring_Counter (clk, init, Count);
  input clk, init;
  output reg [7:0] Count;
  always @ (Posedge clk)
  begin
    if (init) Count = 8'b10000000;
    else begin
      Count <= Count << 1;
      Count[0] <= Count [7];
    end
  end
endmodule.
```

Lecture :⇒ (18) Blocking Vs. Non-blocking Assignment

```
begin
  a = #5 b;
  c = #5 a;
end
```

- The value of "b" will be assigned to "c" 10 time unit after the "begin..end" block starts.

```
begin
  a <= #5 b;
  c <= #5 a;
end
```

- "a" is scheduled to get the value of "b" 5 time units into the future.
- "c" is also scheduled to get the value of "a" 5 time units into the future.

Value of "c" will be different for the two cases.

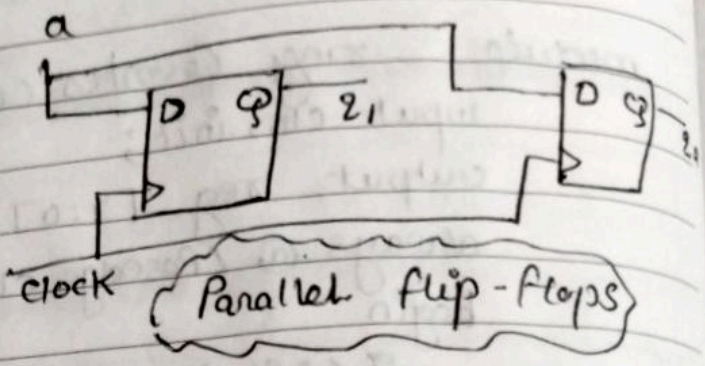
07 September Monday 2020

Week 37

251-115

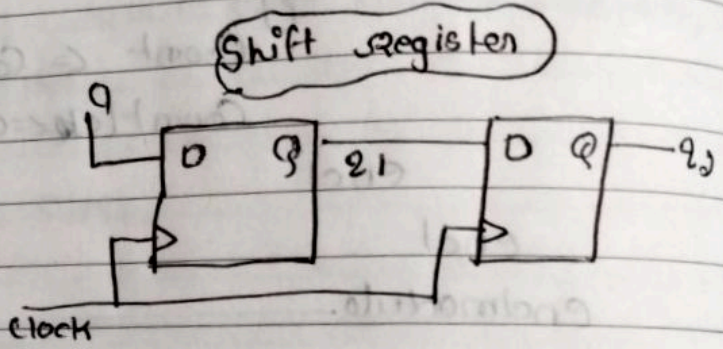
⊙ Blocking Example

```
always @(Posedge clock)
begin
    q1 = a;
    q2 = q1;
end
```



Example :-

```
always @(Posedge clk)
begin
    q2 = q1;
    q1 = q;
end
```

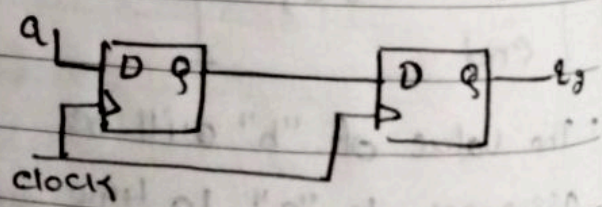


⊙ if we simply interchange them it will become a shift register

eg →

```
always @(Posedge clock)
    q2 <= q1;
always @(Posedge clock)
    q1 <= q;
```

→ here is also generating the same shift Register



Notes eg :-

Lecture :⇒ (19) BLOCKING AND NONBLOCKING ASSIGNMENT FEATOR

BASIC Idea

- It is Posible to Combine both blocking and non-blocking assignment in the same procedural block ("always").
  - Simulator or synthesis tool support this type of usage
- However, interpretation of the circuit behavior under mixed usage is not very straightforward
  - Not recommended for designers.
  - we shall explain the semantics wing two simple examples.
- Such mixing should be avoid in a design.

Example

```
always @(*)
  begin
    x = 10;
    x = 20;
    y = x;
    #10;
  end
```

```
always @(*)
  begin
    x = 10;
    x = 20;
    y <= x;
    #10;
  end
```

→ Same result will be shown for both the version
- "x" will be assigned 10 and then 20 both at time 0.
- The value of "x" at time 0 will be assigned to y. [x=20 ; y=20]

Notes

09 September Wednesday 2020

Week 37

253-113

Keyword

GENERATE Blocks

- "generate" statement allows verilog code to be generated dynamically before the simulation or Synthesis begins.
  - Very convenient to create parameterized module descriptions.
  - Example : N-bit carry adder for Arbitrary value of N.
- Requires the keywords "generate" and "endgenerate"
- Generate instantiations can be carried out for various verilog blocks:
  - modules, user-defined primitives, gate, Continous assignments, "initial" and "always" blocks etc.
  - Generate instances have unique identifier names and can be referenced hierarchically

⊙ Special "genvar" variables :-

- The keyword "genvar" can be used to declare variable that are used in the evaluation of generate block.
- These variable do not exist during Simulation or Synthesis.
- The value of a "genvar" can be defined only in a generate loop.
- Every generate loop is assigned a name so that variable inside the generate loop can be referenced hierarchically.

Notes

example

```
module xor_bitwise (f,a,b);
  parameter N = 16;
    input [N-1 : 0] a,b;
    output [N-1 : 0] f;
    genvar P;

  generate for (P=0 ; P<N ; P= P+1)
      begin xorlp                    :: lp → label
        XOR  xg (f[P], a[P], b[P]);
        end
      endgenerate
    endmodule
```

TEST BENCH :-

```
module generate_To ;
  reg [15:0] x, y ;
  wire [15:0] out;

xor_bitwise  G( .P(out), .a(x), .b(y);
  initial  begin
    $monitor ("x : %b , y : %b , out : %b",
                        x, y, out);
      x = 16'haaaa ; y = 16'h00ff;
    #10  x = 16'hafaf ; y = 16'h3333;
    #20    $finish;
    end
    end module
```

Notes

11 September Friday 2020

Week 37

255-111

- in the bitwise XOR example, the name "XORIP" was given to the generate loop.
- The relative hierarchical names of the XOR gates will be
  xorip[0].xg XORIP[1].xg, ---, xorip[15].xg

eg② DESIGN OF N-bit Ripple CARRY Adder

// structural gate-level description of a full adder

```
module full_adder (a,b,c,Sum,Cout);
    input a,b,c;
    output ,sum, Cout;
    wire t1, t2, t3;
    XOR g1(t1, a, b), g2(Sum, t1, c);
    and g3(t2, a, b), g4(t3, t1, c);
     or g5(Cout, t2, t3);
endmodule
```

Notes

Arli-Iyagi_Verilog

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256-110

Verilog Lecture-20 USER-DEFINED PRIMITIVES

USER DEFINED PRIMITIVES (UDP):-

- They are used to define Custom Verilog primitieves by the use of lookup tables.
- They can Specify:
  - Truth Table for Combinational functions.
  - State-tables for Sequential functions.
  - Don't care, rising and falling edges etc. can be specified

for combinational <input 1> <input 2> .... <input N> : <output>;

→ for Sequential functions, state table entries are specified.
<input 1> <input 2> ... input<N> : <present_state> : <Next state>

Some RULES FOR USING UDP's :-

- The Input terminals to a UDP can only be scalar variables.
  → multiple input terminals can be used.
  → The Input terminals are declared as "input".
  → Input entries in the table must be in the same order as the "input" terminal list.

⊙ only one scalar output terminal must be used.
  → The output terminal must appear in the beginning of the terminal list.
  → for Combinational UDP's, the output terminal is declared as "output".
  → for Sequential UDP's the output terminal is declared as "reg"

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- For Sequential UDP's, the state can be initialized with an "initial" statement.
  - This is optional.

Some Guidelines :-

- user defined Primitives (UDP's) model functionality only.
  - They do not model timing or process technol
- A functional block can be modeled as a UDP o if it has Exactly one output.
  - if a block has more than one output. It has to be modeled as a module.
  - as an alternatives, multiple UDP's can be used, one per unit.
- Inside the Simulator, a UDP is typically implemented as a lookup table in memory.
- The UDP state tables should be specified as Completly as possible.
  - for an specified case, the output is set to "x".

Modeling Combinational Circuit's :-

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```
// full adder Sum generation using udp
primitive Udp-Sum (Sum, a, b, c);
    input a, b, c;
    output Sum;
```

```
table
// a   b   c   :  Sum
   0   0   0   :  0;
   0   0   1   :  1;
   0   1   0   :  1;
   0   1   1   :  0;
   1   0   0   :  1;
   1   0   1   :  0;
   1   1   0   :  0;
   1   1   1   :  1;
endtable
endprimitive
```

```
// full addar Carry generation
// using don't Care ("?")
Primitive udp_cy (cout, a, b, c);
    input a, b, c;
    output cout;
    table
    // a   b   c   :  cout
       0   0   ?   :  0;
       0   ?   0   :  0;
       ?   0   0   :  0;
       1   1   ?   :  1;
       1   ?   1   :  1;
       ?   1   1   :  1;
    endtable
endprimitive
```

```
// instantiating UDP's
// A full adder description

module fullAdder (Sum, cout, a, b, c);
    input a, b, c;
    output Sum, cout;
    udp_Sum  Sum (Sum, a, b, c);
    udp_cy   CARRY (cout, a, b, c);
endmodule
```

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UDPs can be instantiated just like any other Verilog module.

```
// A 4-Input AND Function
primitive udp_and4 (f, a, b, c, d);
    input a, b, c, d;
    output f;
    table
    // a   b   c   d   f
       0   ?   ?   ?  : 0;
       ?   0   ?   ?  : 0;
       ?   ?   0   ?  : 0;
       ?   ?   ?   0  : 0;
       1   1   1   1  : 1;
    endprimitive;
```

MODELING SEQUENTIAL CIRCUITS :-

// A level-sensitive D type latch

```
primitive Dlatch (q, d, clk, clr);
    input d, clk, clr;
    output reg q;
    initial
        q = 0;   // this is optional
    table
    // d   clk  clr  :  q  :  q-new
       ?    ?    1   :  ?  :  0;   // latch is reset
       0    1    0   :  ?  :  0;   // latch is reset
       1    1    0   :  ?  :  1;   // latch is set
       ?    0    0   :  ?  :  -;   // no change
    endprimitive
```

// A T Flip-Flop

```
primitive TFF (q, clk, clr);
  input clk, clr;
  output reg q;
  table
  // clk    clr    q    q_new
       ?      1    :   0   ;   // FF is cleared
       ?     (10)  :   -   ;   // ignore -ve edge of "clr"
     (10)    0    :   0   ;   // FF toggles at -ve edge of
     (10)    0    :   1   ;   //  -do-      "clk"
     (0?)    0    :   -   ;   // ignore -ve edge of "clk"
  endtable
endprimitive
```

// Constructing a 6 bit ripple Counter using T Flip-Flops.

```
primitive ripple_Counter (Count, clk, clr);
    input clk, clr;
    output [5:0] Count;
    TFF F0 (Count[0], clk, clr);
    TFF F1 (Count[1], Count[0], clr);
    TFF F2 (Count[2], Count[1], clr);
    TFF F3 (Count[3], Count[2], clr);
    TFF F4 (Count[4], Count[3], clr);
    TFF F5 (Count[5], Count[4], clr);
endprimitive
```

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// A negative edge Sensitive JK flip-flops

primitive JKFF (q, J, K, clk, clr);
output reg q;
table
// J K clk clr : q : q_new
? ? ? 1 : ? : 0; // clear
? ? ? (10) : ? : -; // ignore --- no change
? ? ? (10) : ? : -; // no change
0 0 (10) 0 : ? : -; // reset condition
0 1 (10) 0 : ? : 0; // set condition
1 0 (10) 0 : ? : 1; // toggle condition
1 1 (10) 0 : 0 : 1; // toggle condition
1 1 (10) 0 : 1 : 0; // toggle condition
? ? (01) 0 : ? : -; // no change

⊙ Some Rule To Follow

→ The "?" Symbol cannot be specified in an output field.
→ The "-" Symbol, indicating no change in the state value, can be specified only in an output field.
→ The shortcut "r", indicating rising edge, can be used instead of (01).
→ The shortcut "f" indicating falling edge, can be used instead of (10).
→ The shortcut "*" indicates any value change in the signal.

Notes

• Verilog is used to describe the low-level hard