1. How many flip-flops are required to make a MOD-32 binary counter?

A. 3 B. 45

C. 5 D. 6

Answer: Option C

2. Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?

A. 50,000 B. 65,536

C. 25,536 D. 15,536

Answer: Option D

3. A MOD-16 ripple counter is holding the count 1001_2. What will the count be after 31 clock pulses?

A. 1000_2 B. 1010_2

C. 1011_2 D. 1101_2

Answer: Option A

4. The terminal count of a modulus-11 binary counter is _____.

A. 1010 B. 1000

C. 1001 D. 1100

Answer: Option A

5. List which pins need to be connected together on a 7493 to make a MOD-12 counter.

A. 12 to 1, 11 to 3, 9 to 2

B. 12 to 1, 11 to 3, 12 to 2

C. 12 to 1, 11 to 3, 8 to 2

D. 12 to 1, 11 to 3, 1 to 2

Answer: Option C

6. How can a digital one-shot be implemented using HDL?

A. By using a resistor and a capacitor

B. By applying the concept of a counter

C. By using a library function

D. By applying a level trigger

Answer: Option B

7. Integrated-circuit counter chips are used in numerous applications including:

A. timing operations, counting operations, sequencing, and frequency multiplication

B. timing operations, counting operations, sequencing, and frequency division

C. timing operations, decoding operations, sequencing, and frequency multiplication

D. data generation, counting operations, sequencing, and frequency multiplication

Answer: Option B

8. Synchronous construction reduces the delay time of a counter to the delay of:

A. all flip-flops and gates

B. all flip-flops and gates after a 3 count

C. a single gate

D. a single flip-flop and a gate

Answer: Option D

9. Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:

A. input clock pulses are applied only to the first and last stages

B. input clock pulses are applied only to the last stage

C. input clock pulses are not used to activate any of the counter stages

D. input clock pulses are applied simultaneously to each stage

Answer: Option D

10. What is the difference between combinational logic and sequential logic?

A. Combinational circuits are not triggered by timing pulses, sequential circuits are triggered by timing pulses.

B. Combinational and sequential circuits are both triggered by timing pulses.

C. Neither circuit is triggered by timing pulses.

Answer: Option A

11. What is the difference between a 7490 and a 7492?

A. 7490 is a MOD-12, 7492 is a MOD-10

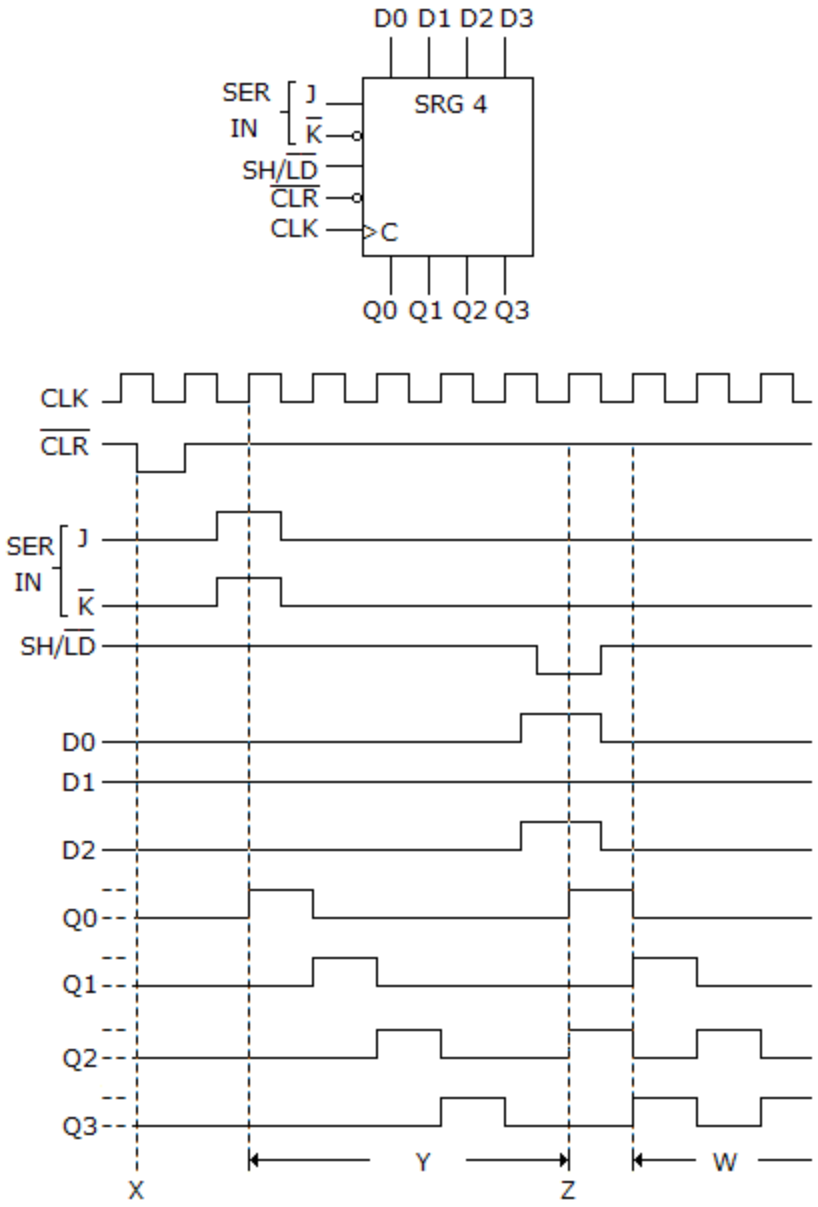
B. 7490 is a MOD-12, 7492 is a MOD-16

C. 7490 is a MOD-16, 7492 is a MOD-10

D. 7490 is a MOD-10, 7492 is a MOD-12

Answer: Option D

12. What type of register is shown below?



A. Parallel in/parallel out register

B. Serial in/parallel out register

C. Serial/parallel-in parallel-out register

D. Parallel-access shift register

Answer: Option D

13.

When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.

A. product

B. sum

C. log

D. reciprocal

Answer: Option A

14.

A MOD-12 and a MOD-10 counter are cascaded. Determine the output frequency if the input clock frequency is 60 MHz.

A. 500 kHz

B. 1,500 kHz

C. 6 MHz

D. 5 MHz

Answer: Option A

15.

Which segments of a seven-segment display would be required to be active to display the decimal digit 2?

A. *a*, *b*, *d*, *e*, and *g*

B. *a*, *b*, *c*, *d*, and *g*

C. *a*, *c*, *d*, *f*, and *g*

D. *a*, *b*, *c*, *d*, *e*, and *f*

Answer: Option A

16.

How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?

A. 128 gates, 6 inputs to each gate

B. 64 gates, 5 inputs to each gate

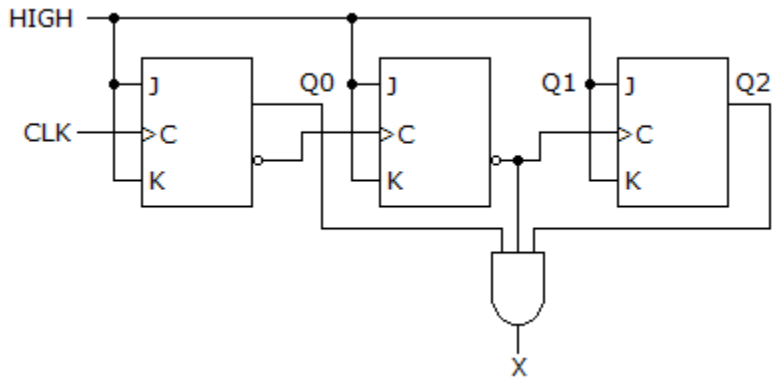
C. 64 gates, 6 inputs to each gate

D. 128 gates, 5 inputs to each gate

Answer: Option C

17.

What decimal value is required to produce an output at "X" ?



A. 1

B. 1 or 4

C. 2

D. 5

Answer: Option D

18.

A BCD counter is a _____.

A. binary counter

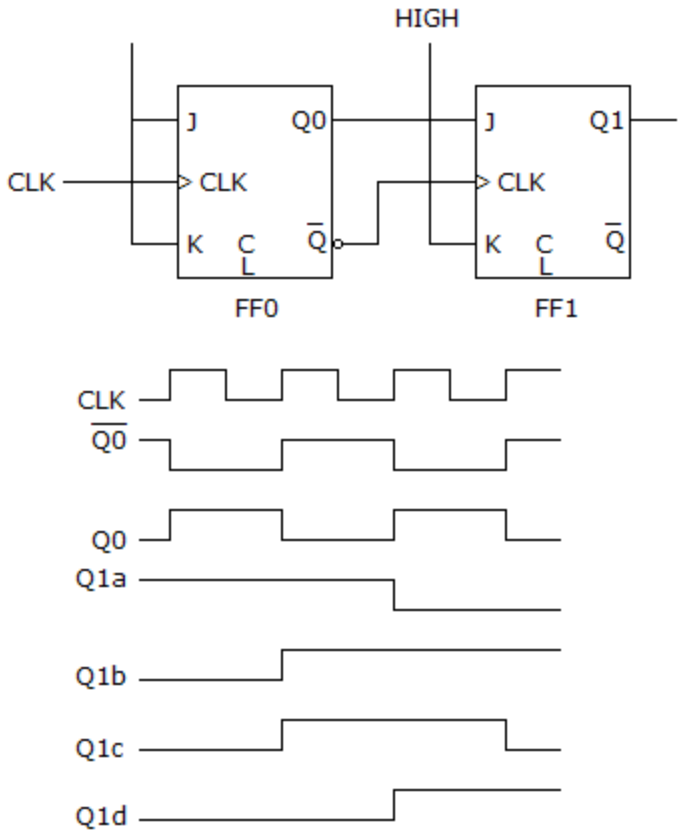
B. full-modulus counter

C. decade counter

D. divide-by-10 counter

Answer: Option C

19. The circuit given below has no output on Q_1 when examined with an oscilloscope. All J-K inputs are HIGH, the CLK signal is present, and the Q_0 is toggling. The *C* input of FF_1 is a constant LOW. What could be causing the problem?



A. The Q_0 output should be connected to the *J* input of FF_1.

B. The output of FF_0 may be shorted to ground.

C. The input of FF_1 may be shorted to ground.

D. Either the output of FF_0 or the input of FF_1 may be shorted to ground.

Answer: Option D

20. How many flip-flops are required to construct a decade counter?

A. 10 B. 8

C. 5 D. 4

Answer: Option D

21. The terminal count of a typical modulus-10 binary counter is _____.

A. 0000 B. 1010

C. 1001 D. 1111

Answer: Option C

22. A seven-segment, common-anode LED display is designed for:

A. all cathodes to be wired together

B. one common LED

C. a HIGH to turn off each segment

D. disorientation of segment modules

Answer: Option C

23. To operate correctly, starting a ring counter requires:

A. clearing one flip-flop and presetting all the others.

B. clearing all the flip-flops.

C. presetting one flip-flop and clearing all the others.

D. presetting all the flip-flops.

Answer: Option C

24.
The process of designing a synchronous counter that will count in a nonbinary manner is primarily based on:

A. external logic circuits that decode the various states of the counter to apply the correct logic levels to the *J-K* inputs

B. modifying BCD counters to change states on every second input clock pulse

C. modifying asynchronous counters to change states on every second input clock pulse

D. elimination of the counter stages and the addition of combinational logic circuits to produce the desired counts

Answer: Option A

25.
Select the response that best describes the use of the Master Reset on typical 4-bit binary counters.

A. When MR_1 and MR_2 are both HIGH, all Qs will be reset to zero.

B. When MR_1 and MR_2 are both HIGH, all Qs will be reset to one.

C. MR_1 and MR_2 are provided to synchronously reset all four flip-flops.

D. To enable the count mode, MR_1 and MR_2 must be held LOW.

Answer: Option A

26.
For a multistage counter to be truly synchronous, the _____ of each stage must be connected to _____.

A. C_p, the same clock input line

B. *CE*, the same clock input line

C. $\overline{PL}$, the terminal count output

D. $\overline{RC}$, both clock input lines

Answer: Option A

27.

Which of the following is an invalid output state for an 8421 BCD counter?

A. 1110

B. 0000

C. 0010

D. 0001

Answer: Option A

28.

How many different states does a 3-bit asynchronous counter have?

A. 2

B. 4

C. 8

D. 16

Answer: Option C

29.

A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay ($t_{p(tot)}$) is _____.

A. 12 ms

B. 24 ns

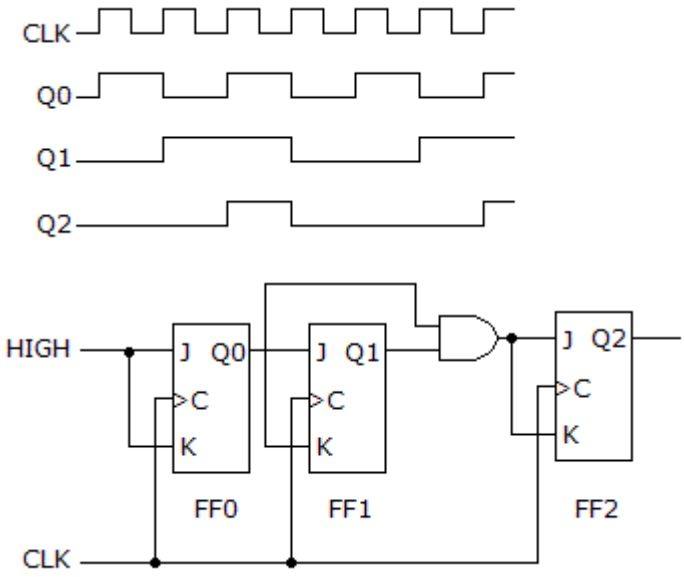
C. 48 ns

D. 60 ns

Answer: Option D

30.

A four-channel scope is used to check the counter in the figure given below. Are the displayed waveforms correct?



A. Yes

B. No

Answer: Option B

31.

Which of the following procedures could be used to check the parallel loading feature of a counter?

A. Preset the *LOAD* inputs, set the *CLR* to its active level, and check to see that the *Q* outputs match the values preset into the *LOAD* inputs.

B. Apply LOWs to the parallel *DATA* inputs, pulse the *CLK* input, and check for LOWs on all the *Q* outputs.

C. Apply HIGHs to all the DATA inputs, pulse the *CLK* and *CLR* inputs, and check to be sure that the *Q* outputs are all LOW.

D. Apply HIGHs to all the *Q* terminals, pulse the *CLK*, and check to see if the *DATA*terminals now match the *Q* outputs.

Answer: Option B

32.
One of the major drawbacks to the use of asynchronous counters is:

A. low-frequency applications are limited because of internal propagation delays

B. high-frequency applications are limited because of internal propagation delays

C. asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications

D. asynchronous counters do not have propagation delays and this limits their use in high-frequency applications

Answer: Option B

33.
Once an up-/down-counter begins its count sequence, it cannot be reversed.

A. True B. False

Answer: Option B

34.
Three cascaded modulus-5 counters have an overall modulus of _____.

A. 5 B. 25

C. 125 D. 500

Answer: Option C

35.
An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?

A. None B. One

C. Two

D. Fifteen

Answer: Option D

36. The final output of a modulus-8 counter occurs one time for every _____.

A. 8 clock pulses

B. 16 clock pulses

C. 24 clock pulses

D. 32 clock pulses

Answer: Option A

37. A 4-bit up/down binary counter is in the DOWN mode and in the 1100 state. To what state does the counter go on the next clock pulse?

A. 1101

B. 1011

C. 1111

D. 0000

Answer: Option B

38. A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____.

A. 15 ns

B. 30 ns

C. 45 ns

D. 60 ns

Answer: Option D

39. The terminal count of a 3-bit binary counter in the DOWN mode is _____.

A. 000 B. 111

C. 101 D. 010

Answer: Option A

40. The hexadecimal equivalent of 15,536 is _____.

A. 3CB0 B. 3C66

C. 63C0 D. 6300

Answer: Option A

41. In an HDL ring counter, many invalid states are included in the programming by:

A. using a case statement.

B. using an elsif statement.

C. including them under others.

D. the *ser_in* line.

Answer: Option C

42. In a VHDL retriggerable edge-triggered one-shot, which condition will not exist when a clock edge occurs?

A. A trigger edge has occurred and we must load the counter.

B. The counter is zero and we need to keep it at zero.

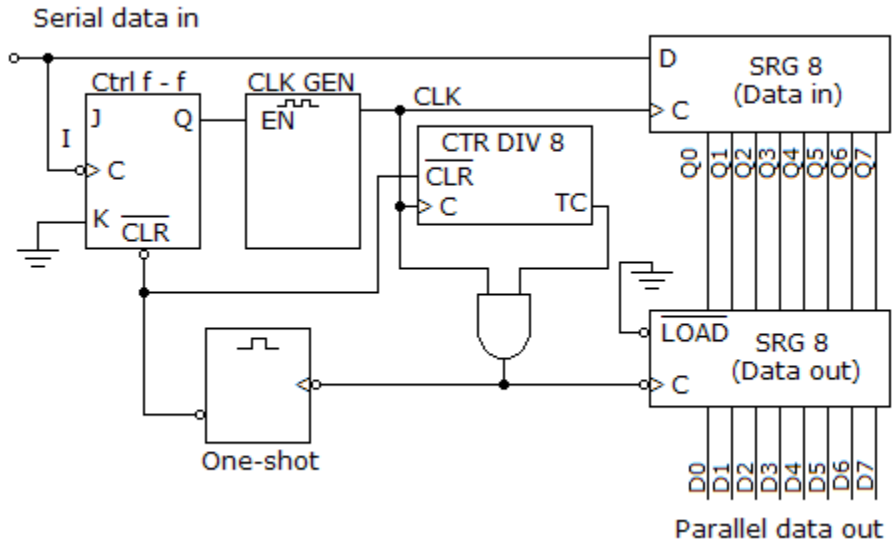
C. The shift register is reset.

D. The counter is not zero and we need to count down by one.

Answer: Option C

43.

What function does the CTR DIV 8 circuit given below perform?



A. It divides the clock frequency down to match the frequency of the serial data in.

B. The divide-by-8 counter is triggered by the control flip-flop and clock, which then allows the data output register to begin storing the input data. Once all eight data bits are stored in the data output register, the data output register and the divide-by-8 counter trigger the one-shot. The one-shot then begins the process all over again.

C. The divide-by-8 counter is used to verify that the parity bit is attached to the input data string.

D. It keeps track of the eight data bits, triggering the transfer of the data through the output register and the one-shot, which then resets the control flip-flop and divide-by-8 counter.

Answer: Option D

44.

Synchronous (parallel) counters eliminate the delay problems encountered with asynchronous (ripple)

counters because the:

A. input clock pulses are applied only to the first and last stages.

B. input clock pulses are applied only to the last stage.

C. input clock pulses are applied simultaneously to each stage.

D. input clock pulses are not used to activate any of the counter stages.

Answer: Option C

45.

List the state of each output pin of a 7447 if $RBI = 0$, $LT = 1$, $A_0 = 1$, $A_1 = 0$, $A_2 = 0$, and $A_3 = 1$.

A. $RBO = 0, a = 0, b = 0, c = 0, d = 1, e = 1, f = 0, g = 0$

B. $RBO = 1, a = 0, b = 0, c = 0, d = 1, e = 1, f = 0, g = 0$

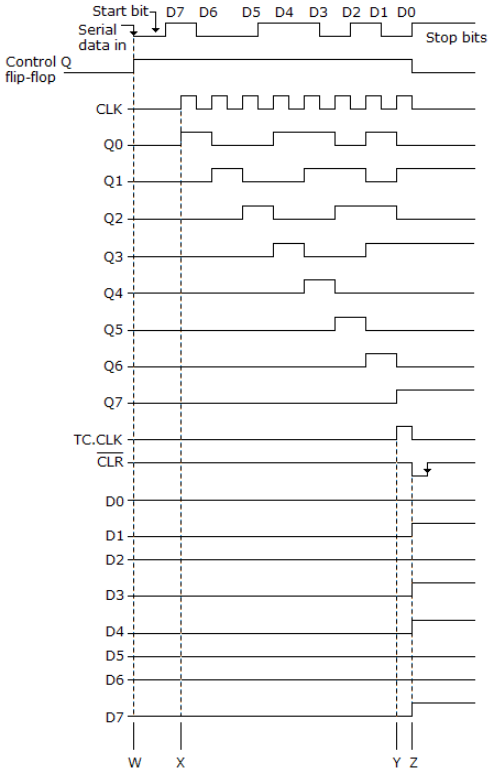
C. $RBO = 0, a = 0, b = 0, c = 0, d = 0, e = 1, f = 0, g = 0$

D. $RBO = 1, a = 0, b = 0, c = 0, d = 0, e = 1, f = 0, g = 0$

Answer: Option A

46.

Referring to the given figure, what causes the Control FF to reset after D7?



A. Once the data cycle is initiated by the Start bit, the one-shot produces an output pulse equal to the duration of the eight data bits. Once the eight data bits have been transferred to the data input register, the falling edge of the one-shot pulse resets the Control FF to start the sequence all over again.

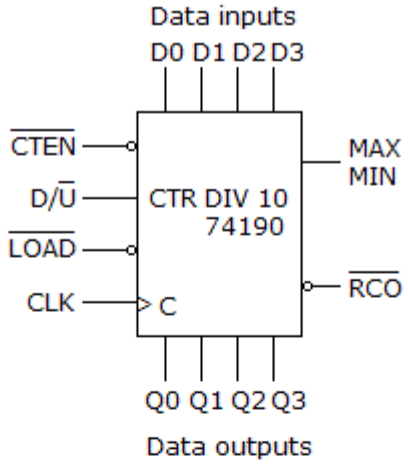
B. After counting the eight data bits, the divide-by-8 counter produces an output on its active-LOW CLR line to reset the Control FF.

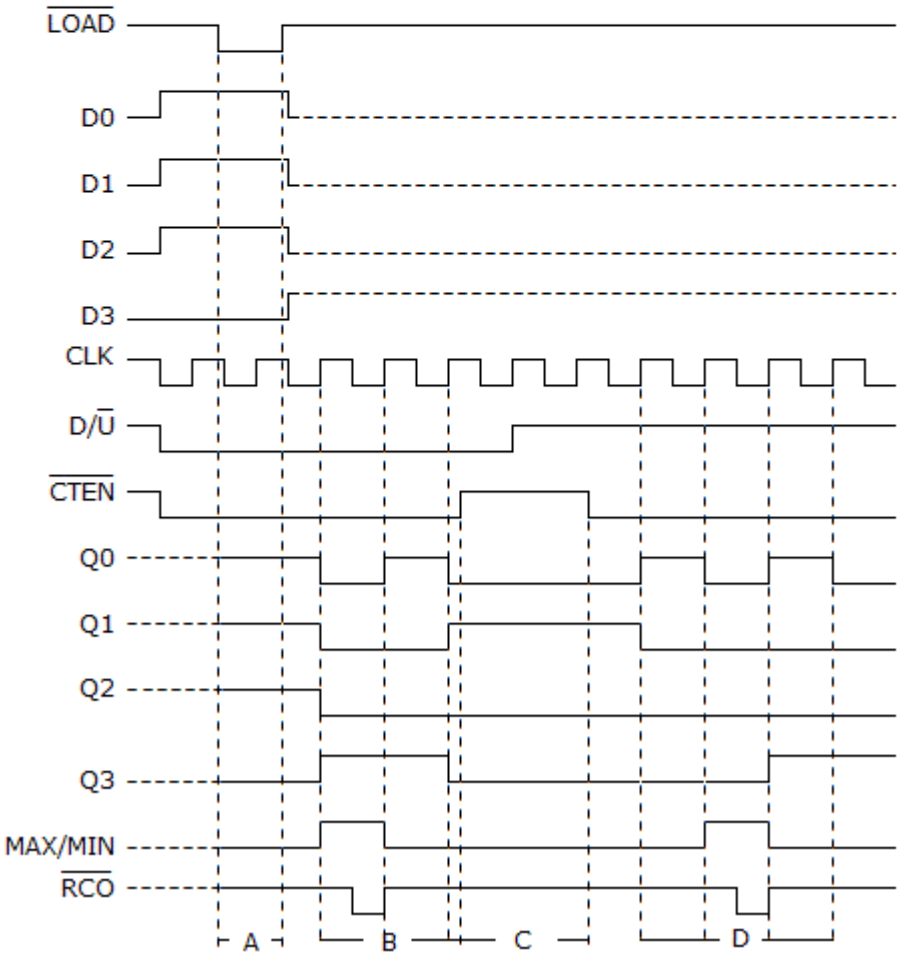
C. After counting eight clock pulses equivalent to eight data periods, the terminal count of the divide-by-8 counter and the clock trigger the one-shot, which in turn resets the Control FF and divide-by-8 circuits to begin the sequence all over again. Simultaneously the data is transferred through the output register.

D. When the data output register is full, it produces an output on its *C* terminal that triggers the one-shot, which in turn resets the Control FF.

Answer: Option C

47. What function will the counter shown below be performing during period "B" on the timing diagram?


Data inputs
D0 D1 D2 D3
CTEN
D/U
LOAD
CLK
C
CTR DIV 10
74190
MAX
MIN
RCO
Q0 Q1 Q2 Q3
Data outputs


LOAD
D0
D1
D2
D3
CLK
D/U
CTEN
Q0
Q1
Q2
Q3
MAX/MIN
RCO
A
B
C
D

A. Counting up

B. Counting down

C. Inhibited

D. Loading

Answer: Option A

48. Three cascaded decade counters will divide the input frequency by _____.

A. 10 B. 20

C. 100 D. 1,000

Answer: Option D

49. A counter with a modulus of 16 acts as a _____.

A. divide-by-8 counter

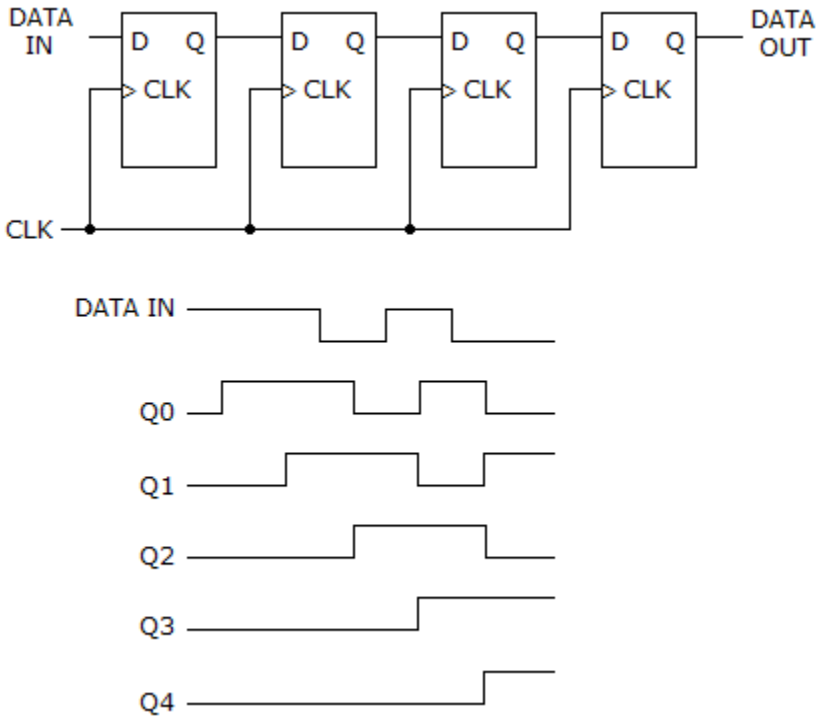
B. divide-by-16 counter

C. divide-by-32 counter

D. divide-by-64 counter

Answer: Option B

50. How many data bits can be stored in the register shown below?



A. 5

B. 32

C. 31

D. 4

Answer: Option A

51. What is the difference between a 7490 and a 7493?

A. 7490 is a MOD-10, 7493 is a MOD-16

B. 7490 is a MOD-16, 7493 is a MOD-10

C. 7490 is a MOD-12, 7493 is a MOD-16

D. 7490 is a MOD-10, 7493 is a MOD-12

Answer: Option A

52.

A ripple counter's speed is limited by the propagation delay of:

A. each flip-flop

B. all flip-flops and gates

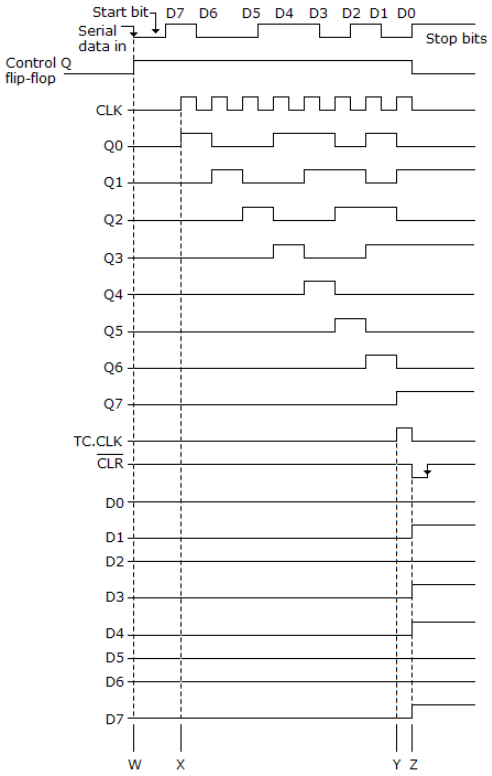
C. the flip-flops only with gates

D. only circuit gates

Answer: Option A

53.

Referring to the given figure, at which point is the serial data transferred to the parallel output?



A. W

B. X

C. Y

D. Z

Answer: Option D

54.

A 4-bit counter has a maximum modulus of _____.

A. 3

B. 6

C. 8

D. 16

Answer: Option D

55.

Which of the following statements best describes the operation of a synchronous up-/down-counter?

A. The counter can count in either direction, but must continue in that direction once started.

B. The counter can be reversed, but must be reset before counting in the other direction.

C. In general, the counter can be reversed at any point in its counting sequence.

D. The count sequence cannot be reversed, once it has begun, without first resetting the counter to zero.

Answer: Option C

56.

The parallel outputs of a counter circuit represent the:

A. parallel data word

B. clock frequency

C. counter modulus

D. clock count

Answer: Option D

57.

Any divide-by-*N* counter can be formed by using external gating to _____ at a predetermined number.

A. HIGH

B. reset

C. LOW

D. preset

Answer: Option B

58.

A MOD-16 synchronous counter has inputs labeled $\bar{R}_O$, $\bar{C}_{PO}$, 2^0, 2^1, 2^2 and 2^3. These inputs would most probably be used to:

A. reset the counter to 0000 at the end of each count cycle

B. preset the counter to a value determined by the $\bar{C}_{PO}$ - 2^3 inputs any time the $\bar{R}_o$ is active-HIGH

C. preset the counter to a value determined by the $\bar{C}_{PO}$ - 2^3 inputs any time the $\bar{R}_o$ is active-LOW

D. reset the counter to 0000 any time $\bar{C}_{PO}$ - 2^3 is active-HIGH and $\bar{R}_o$ is active-LOW

Answer: Option D

59.

How many natural states will there be in a 4-bit ripple counter?

A. 4

B. 8

C. 16

D. 32

Answer: Option C

60.

List which pins need to be connected together on a 7492 to make a MOD-12 counter.

A. 1 to 12, 11 to 6, 9 to 7

B. 1 to 12, 12 to 6, 11 to 7

C. 1 to 12, 9 to 6, 8 to 7

D. 1 to 12

Answer: Option D

61. A principle regarding most display decoders is that when the correct input is present, the related output will switch:

A. HIGH

B. to high impedance

C. to an open

D. LOW

Answer: Option D

62. A modulus-10 counter must have _____.

A. 10 flip-flops

B. flip-flops

C. 2 flip-flops

D. synchronous clocking

Answer: Option B

63. For a one-shot application, how can HDL code be used to make a circuit respond once to each positive transition on its trigger input?

A. By using a counter

B. By using an active clock

C. By using an immediate reload

D. By using edge trapping

Answer: Option D

64. Which is not an example of a truncated modulus?

A. 8 B. 9

C. 11 D. 15

Answer: Option A

65. Four cascaded modulus-10 counters have an overall modulus of _____.

A. 10 B. 100

C. 1,000 D. 10,000

Answer: Option D

66. What is the maximum delay that can occur if four flip-flops are connected as a ripple counter and each flip-flop has propagation delays of t_{PHL} = 22 ns and t_{PLH} = 15 ns?

A. 15 ns

B. 22 ns

C. 60 ns

D. 88 ns

Answer: Option D

67. Which of the following statements are true?

A. Asynchronous events do not occur at the same time.

B. Asynchronous events are controlled by a clock.

C. Synchronous events do not need a clock to control them.

D. Only asynchronous events need a control clock.

Answer: Option A

68.
Which segments (by letter) of a seven-segment display need to be active in order to display a digit 6?

A. *b*, *c*, *d*, *e*, *f*, and *g*

B. *a*, *c*, *d*, *e*, *f*, and *g*

C. *a*, *b*, *c*, *d*, and *f*

D. *b*, *c*, *d*, *e*, and *f*

Answer: Option B

69.
Which of the following groups of logic devices would be the minimum required for a MOD-64 synchronous counter?

A. Five flip-flops, three AND gates

B. Seven flip-flops, five AND gates

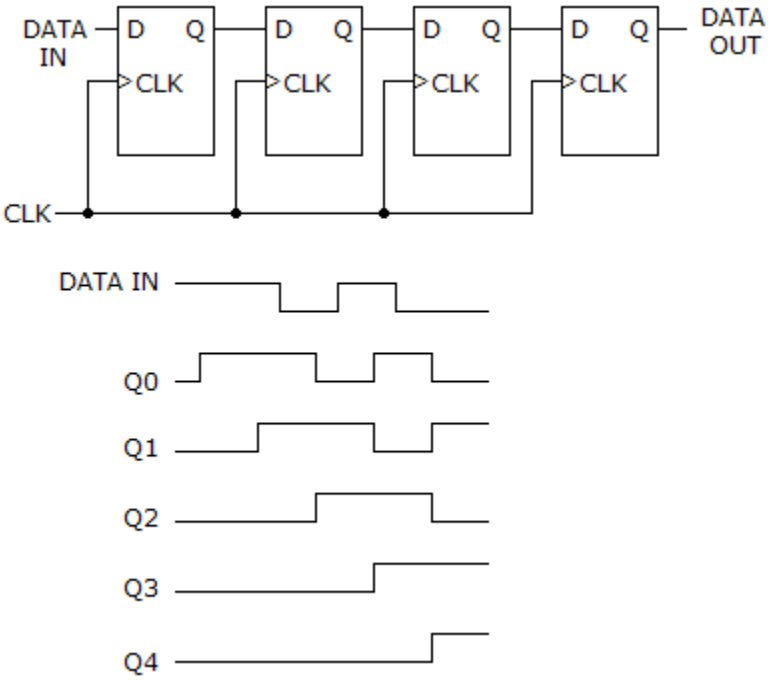
C. Four flip-flops, ten AND gates

D. Six flip-flops, four AND gates

Answer: Option D

70.
The circuit given below fails to produce data output. The individual flip-flops are checked with a logic

probe and pulser, and each checks OK. What could be causing the problem?



A. The data output line may be grounded.

B. One of the clock input lines may be open.

C. One of the interconnect lines between two stages may have a solder bridge to ground.

D. One of the flip-flops may have a solder bridge between its input and V_{cc}.

Answer: Option B

71.

A 22-MHz clock signal is put into a MOD-16 counter. What is the frequency of the *Q*output of each stage of the counter?

A. $Q_1 = 22$ MHz, $Q_2 = 11$ MHz, $Q_3 = 5.5$ MHz, $Q_4 = 2.75$ MHz

B. $Q_1 = 11$ MHz, $Q_2 = 5.5$ MHz, $Q_3 = 2.75$ MHz, $Q_4 = 1.375$ MHz

C. $Q_1 = 11$ MHz, $Q_2 = 11$ MHz, $Q_3 = 11$ MHz, $Q_4 = 11$ MHz

D. $Q_1 = 22$ MHz, $Q_2 = 22$ MHz, $Q_3 = 22$ MHz, $Q_4 = 22$ MHz

Answer: Option B

72.

The designation $\overline{\text{UP/DOWN}}$ means that the _____.

A. up count is active-HIGH, the down count is active-LOW

B. up count is active-LOW, the down count is active-HIGH

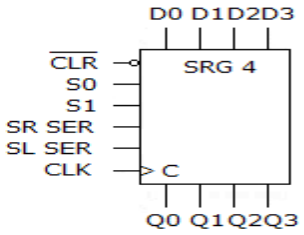
C. up and down counts are both active-LOW

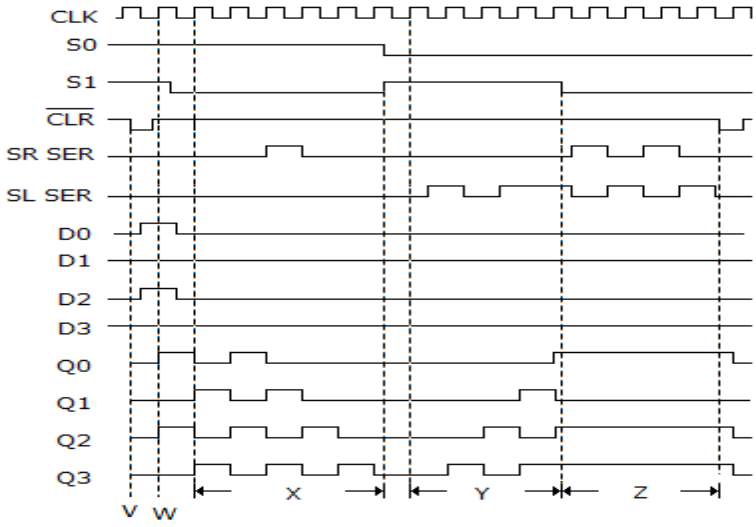
D. up and down counts are both active-HIGH

Answer: Option A

73.

What type of device is shown below?





INPUTS										OUTPUTS			
CLEAR	MODE		CLK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S2		LEFT	RIGHT	D0	D1	D2	D3				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

A. 4-bit bidirectional universal shift register

B. Parallel in/parallel out shift register with bidirectional data flow

C. 2-way parallel in/serial out bidirectional register

D. 2-bit serial in/4-bit parallel out bidirectional shift register

Answer: Option A

74.
Why can a synchronous counter operate at a higher frequency than a ripple counter?

A. The flip-flops change one after the other.

B. The flip-flops change at the same time.

C. A synchronous counter cannot operate at higher frequencies.

D. A ripple counter is faster.

Answer: Option B

75.
A multiplexed display being driven by a logic circuit:

A. accepts data inputs from one line and passes this data to multiple output lines

B. accepts data inputs from several lines and allows one of them at a time to pass to the output

C. accepts data inputs from multiple lines and passes this data to multiple output lines

D. accepts data inputs from several lines and multiplexes this input data to four BCD lines

Answer: Option B

76.
What is meant by parallel load of a counter?

A. Each FF is loaded with data on a separate clock.

B. The counter is cleared.

C. All FFs are preset with data.

Answer: Option C

77.
Which of the following is an example of a counter with a truncated modulus?

A. 8

B. 13

C. 16

D. 32

Answer: Option B

78. Which of the following is a type of shift register counter?

A. Decade

B. Binary

C. Ring

D. BCD

Answer: Option C

79. MOD-6 and MOD-12 counters and multiples are most commonly used as:

A. frequency counters

B. multiplexed displays

C. digital clocks

D. power consumption meters

Answer: Option C

80. Which of the following is an invalid state in an 8421 BCD counter?

A. 0011

B. 1001

C. 1000

D. 1100

Answer: Option D

81. After 10 clock cycles, and assuming that the DATA input had returned to 0 following the storage

sequence, what values would be stored in $Q4$, $Q3$, $Q2$, $Q1$, $Q0$ of the register in Figure 7-5?

A. 0,1,0,1,1

B. 1,1,0,1,0

C. 1,0,1,0,1

D. 0,0,0,0,0

Answer: Option D

82.
How many different states does a 2-bit asynchronous counter have?

A. 1

B. 2

C. 4

D. 8

Answer: Option C

83.
A 12 MHz clock frequency is applied to a cascaded counter containing a modulus-5 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is _____.

A. 10 kHz

B. 20 kHz

C. 30 kHz

D. 60 kHz

Answer: Option C