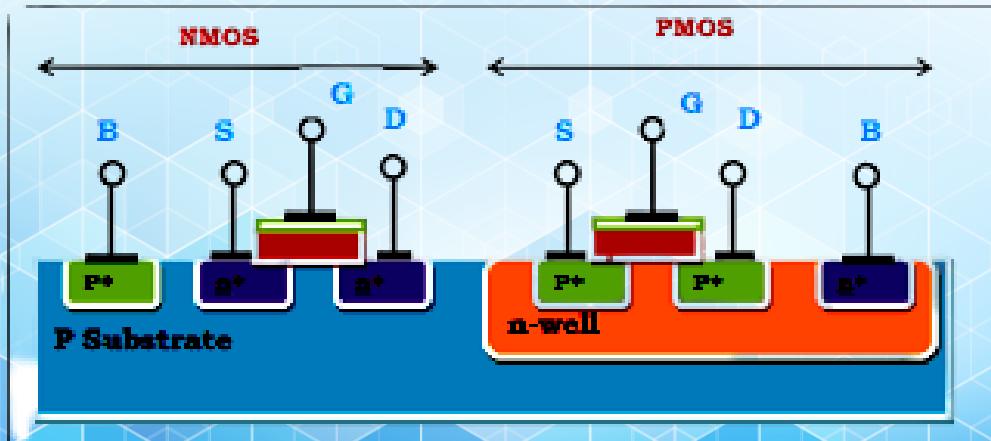


CMOS NOTES

— Sticky Notes —

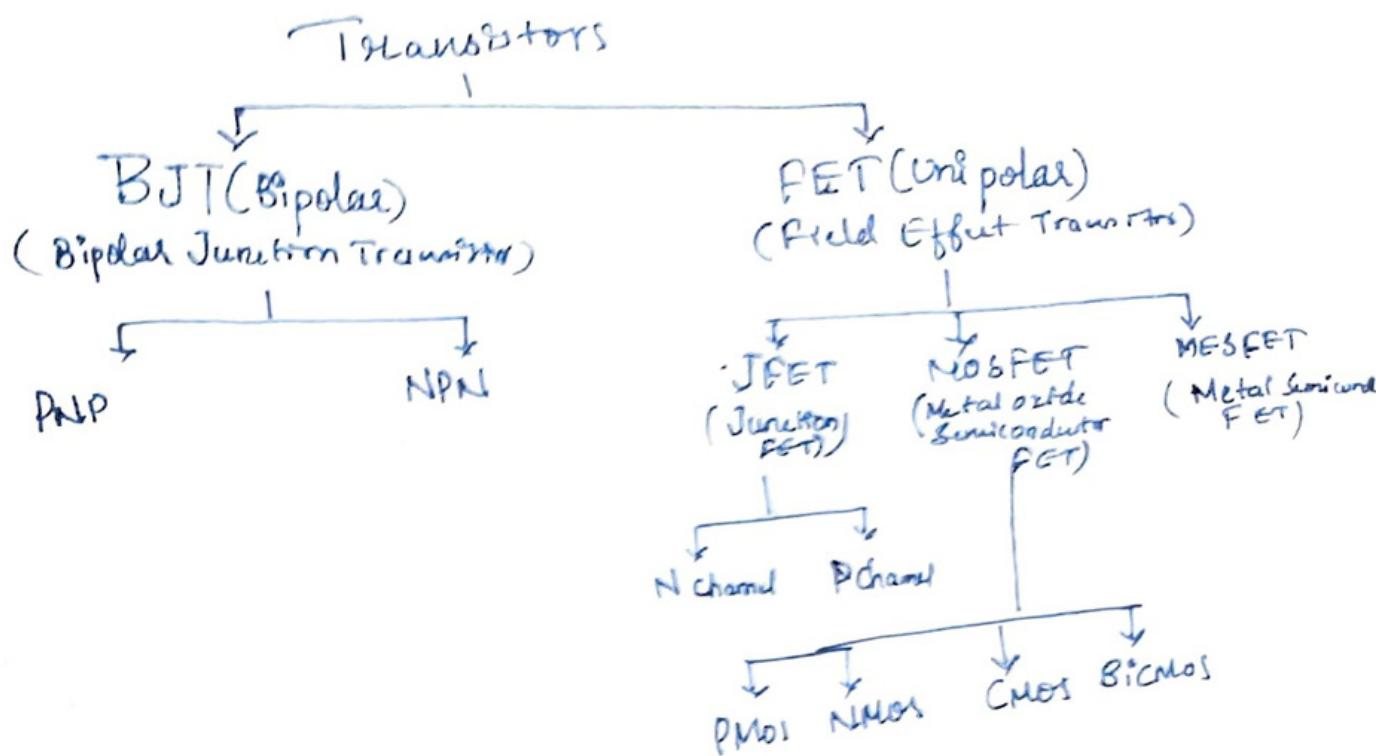


Jairaj Mirashi

Design Verification
Engineer

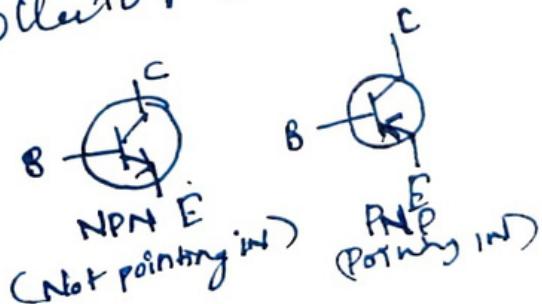


* Classification:

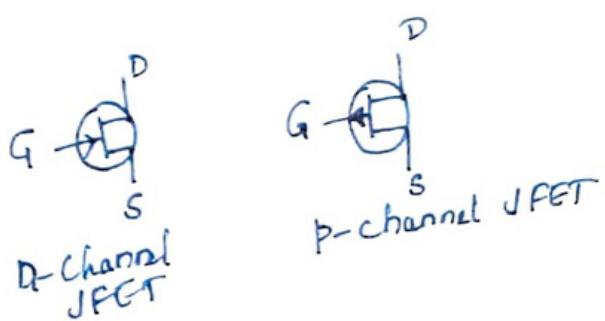


* BJT Vs FET :-

- The Bipolar Junction Transistor (BJT) a current controlled device.
- The base current (I_B) controls the collector current (I_C)



The field Effect Transistor (FET)
a voltage controlled device.
The gate-source voltage (V_{GS})
controls the drain current (I_D).



BJT

(I_Pcurrent Bipolar
Control Current controlled Device
(Opcurrent))

Three terminals:
Emitter, Base, Collector

Type: PNP, NPN

Switching Speed is low
(Transition from $V_{BE} > 0$ to 0)
Switching loss is more

Low Input Impedance

Low package Density

BJT are preferred for low current applications.

+ High Gain

FET

Unipolar.

Voltage controlled Device
(DIP Voltage determine o/p voltage)

Three Terminals:
Source, Gate, Drain

Type: PMOS, NMOS, CMOS, Bi-CMOS.

Switching speed is high

Switching loss is less

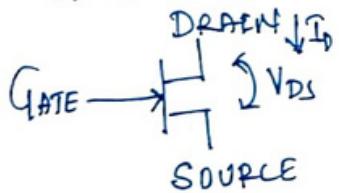
* High Input Impedance (Due to depletion region between gate and source)

+ High Package Density (Substrate)

FETs are for high power applications.

Low Gain (one of the main disadvantages)

JFET and NPN Bipolar Transistor

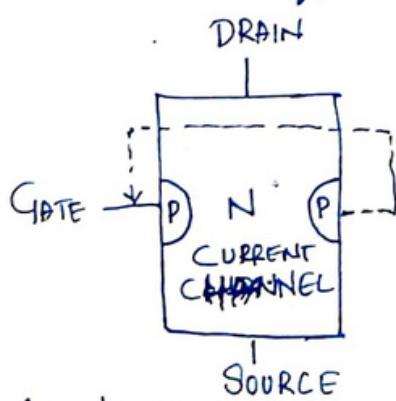


N-channel JFET Symbol



NPN Bipolar Transistor.

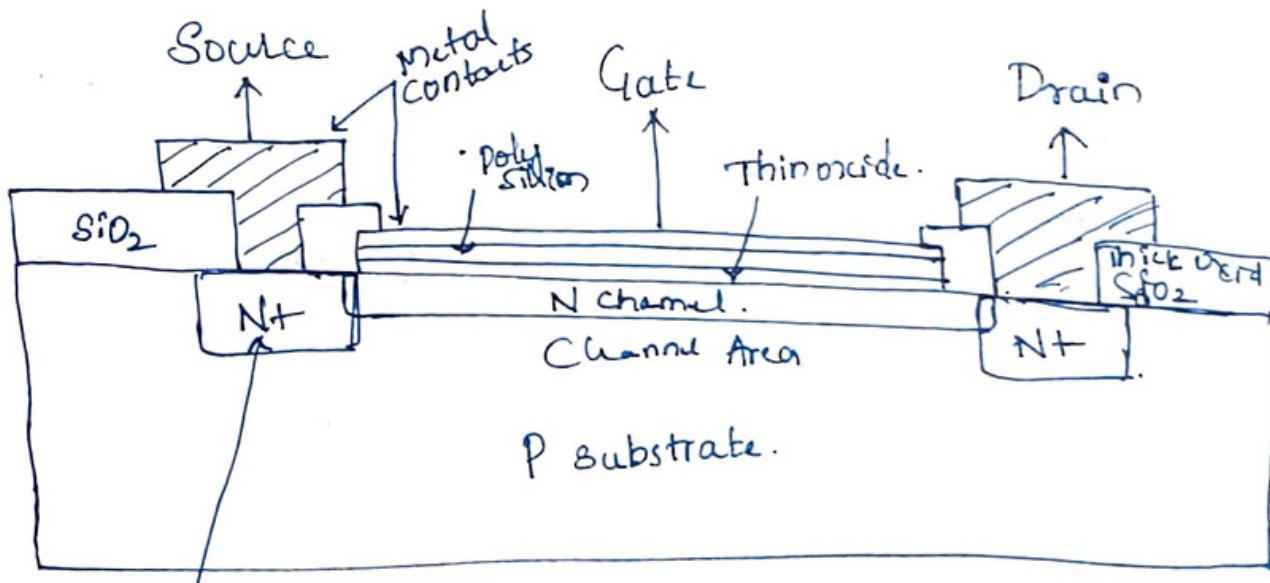
JFET - Junction Field Effect Transistor



An N-channel Junction Field Effect Transistor

- An N-channel JFET has a P-doped gate and a P-channel JFET has a N-doped gate.
- The gate diffusion actually forms a P-N or N-P junction with the main current channel.
- In these JFET the main channel is 'N', So, the N-channel JFET uses electrons as the drain-source majority current carriers.
- The gate-channel P-N junction is always reverse biased under normal operating conditions, so only leakage current flows from the gate to the drain-source current channel.
- This gives the JFET transistor a very high input impedance.

MOSFET:-



Heavily doped with excess electrons.

Modes of Operation of MOSFETs

{ → Types of MOSFET:
↳ NMOS, PMOS, CMOS

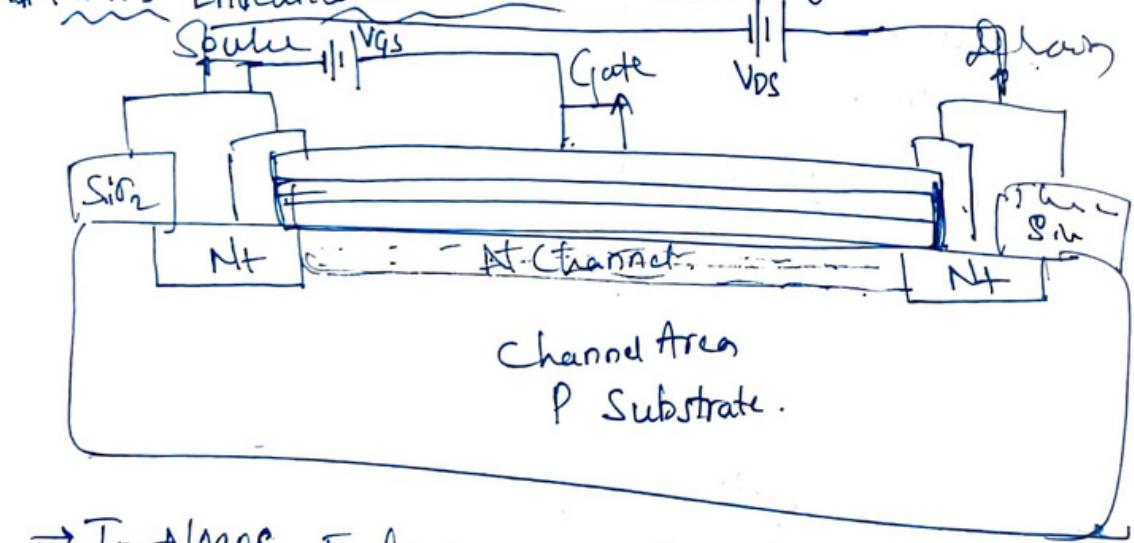
→ Mode of Operation:

↳ Enhancement Mode.

↳ Depletion Mode.

→ Each mode can be used to create an N-channel or P-Channel device.

NMOS Enhancement-mode FET Configuration:



→ In NMOS Enhancement mode first we have to create a channel.

↳ In order to create a channel we have to apply Gate-Source Voltage.

where Source is connected with negative & Gate is connected with positive.

↳ Since the Gate is connected with positive, the electrons will get collected near the oxide layer.

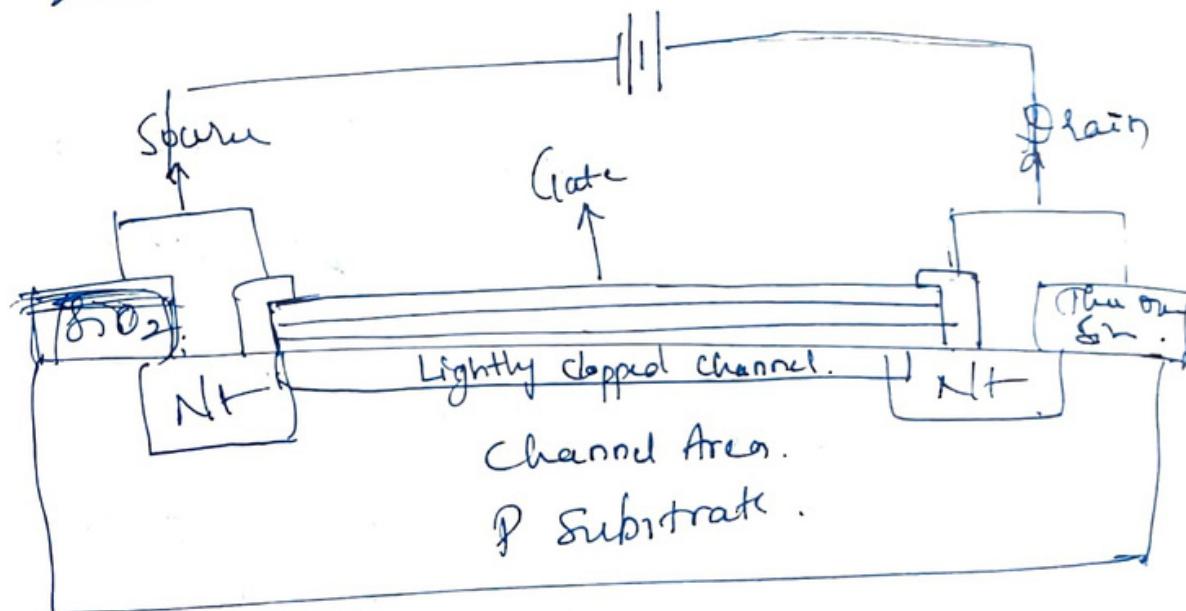
↳ The Minimum Voltage Required to form a channel is called Threshold Voltage.

→ So, there is a formation channel, but there is no flow of charge carriers, so in order to move charge carriers (electrons), so, for that we need to apply Drain - Source Voltage.

→ Here, the Source negative & positive is connected with Drain, so the electrons we get attracted towards Drain, source is negative, so electrons will be repelled.

The electrons flow from Source and Drain, current convention is such a way that, the current ~~flows~~ Opposite to flow of electrons.

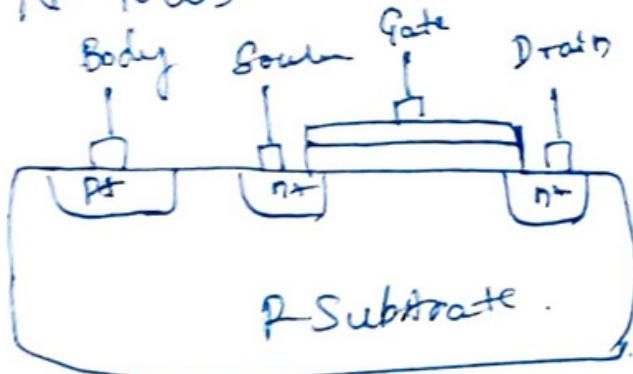
* N Mos Depletion-mode FET Configuration:-



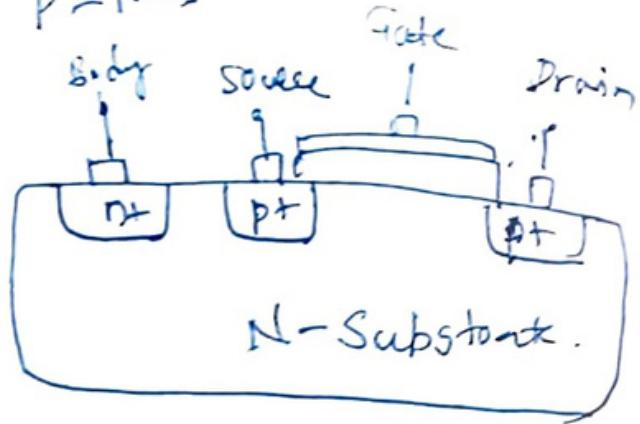
- Here ~~there~~ there ~~already~~ lightly ~~Nmos~~ Depletion-mode already channel will be there.
- Here we have to apply Drain - Source Voltage to flow of charge carriers (electrons).

#MOSFET Structure Review:

N-Mos



P-Mos



- Metal and lightly-doped semiconductor junction forms Schottky Diode which is not desirable.
- Use heavily doped well for substrate contacts (tops).
- Drain & Source are interchangeable (on connection) (have same characteristics at n^+ , n^+)

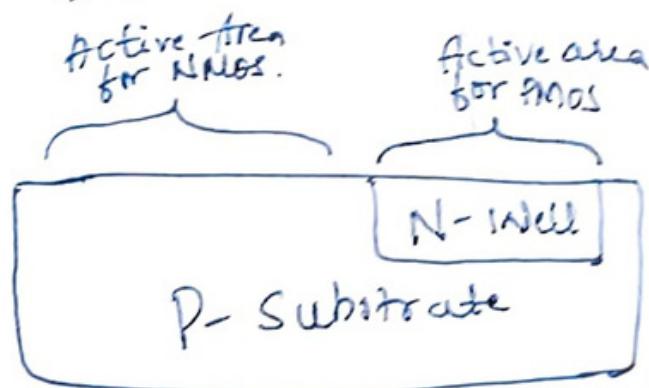
#CMOS Fabrication:

Complexities in Fabrication:

- CMOS logic circuits contains both PMOS and NMOS
- Hence, both of them should be fabricated on a single die.
- But, they require different substrate material.
- Hence, they must be fabricated on separate layers.
- But, the die (starting layer) can be of only type (either 'p' or 'n' type).

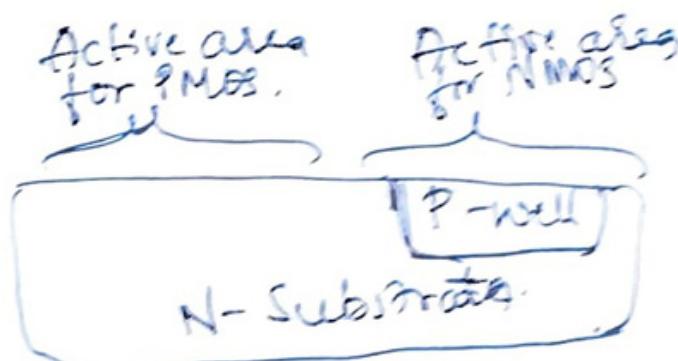
N-Well and P-Well :-

N-Well Process:-



Substrate there we have p-substrate, in that we have ~~Cleate~~ N-well,
p-substrate will be active for NMOS Area and
N-well will be active for PMOS.

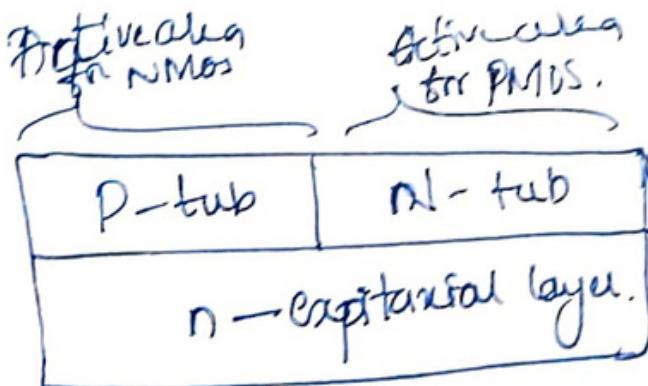
P-Well Process:-



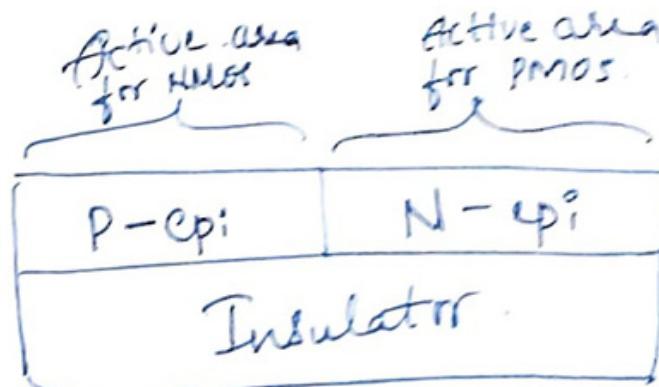
Here the substrate will be N-substrate.

N-substrate will be the active area for PMOS and P-well will be active area for NMOS.

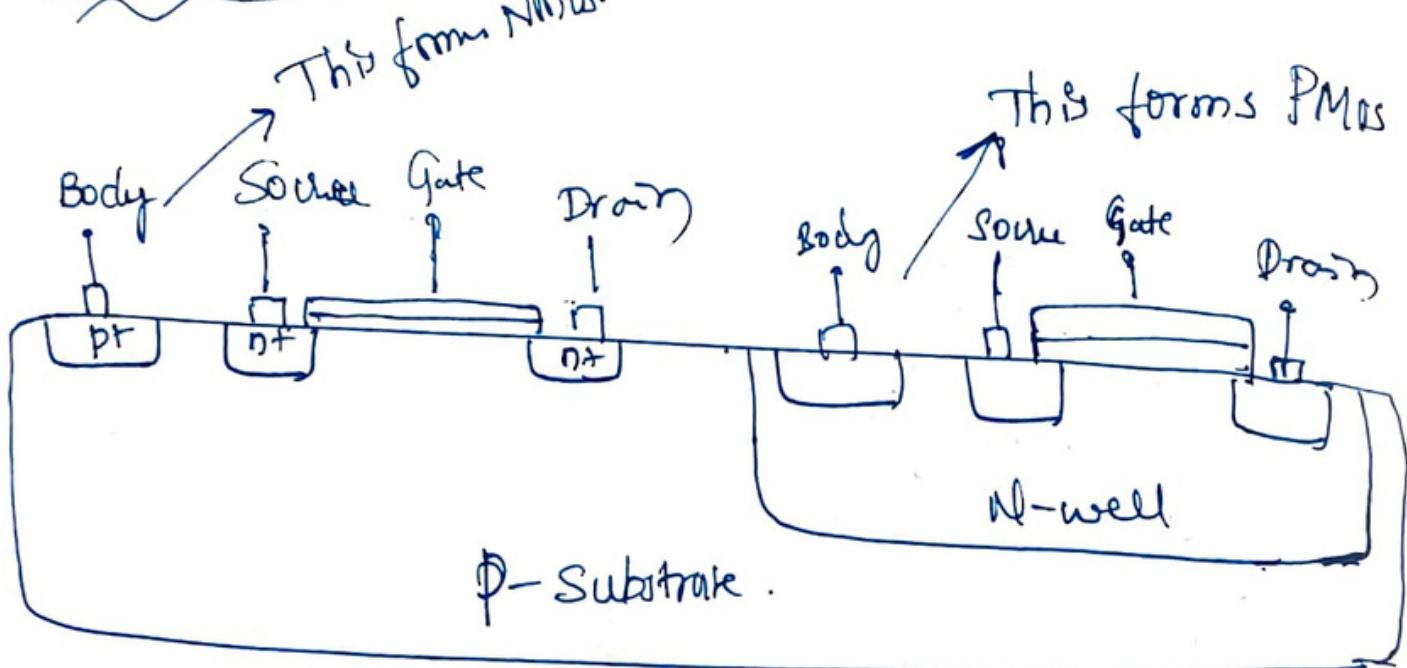
Twin Tub Process:-



Silicon on Insulator:-



Detailed View - At - N-well Process



Key materials used in fabrication:

→ Insulator - Silicon Dioxide (SiO_2)

↳ Used to insulate transistor gate (thin oxide)

↳ Used to insulate layer of wires (field oxide)

→ Polysilicon - polycrystalline silicon.

↳ Key material for transistor gates

↳ Used for short wires because of poor conductivity than metals.

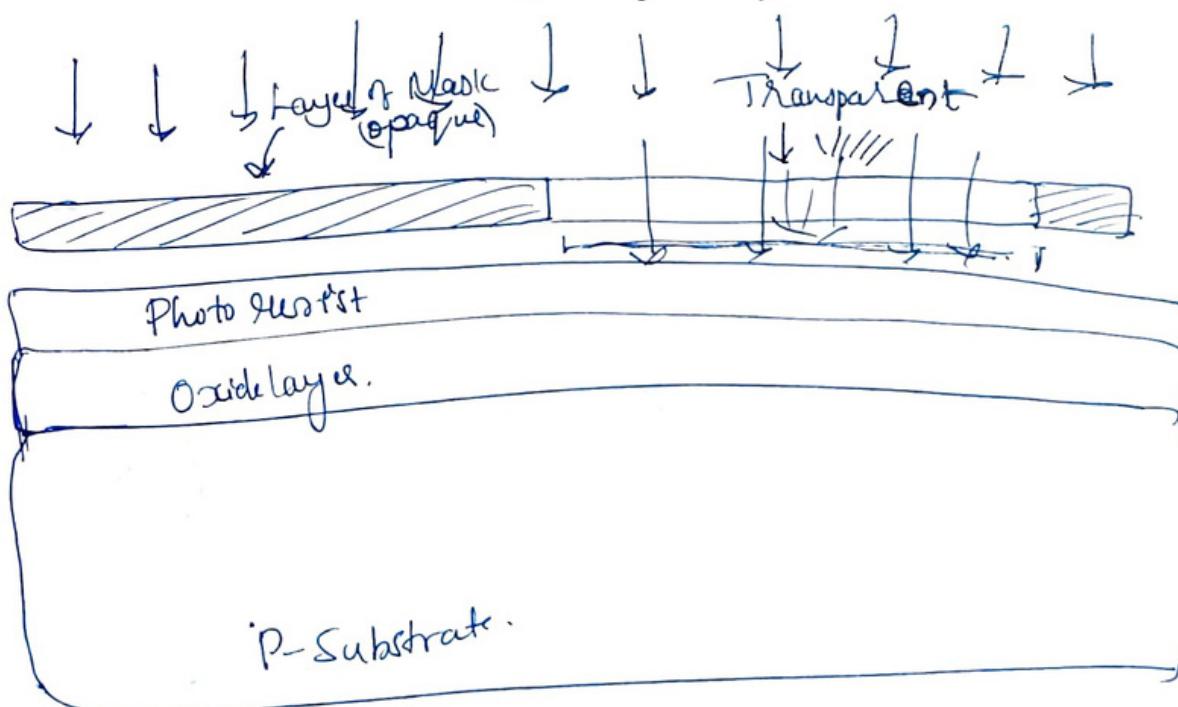
→ Metal - Aluminum (... and more recently Copper)

↳ Used for wires (interconnects)

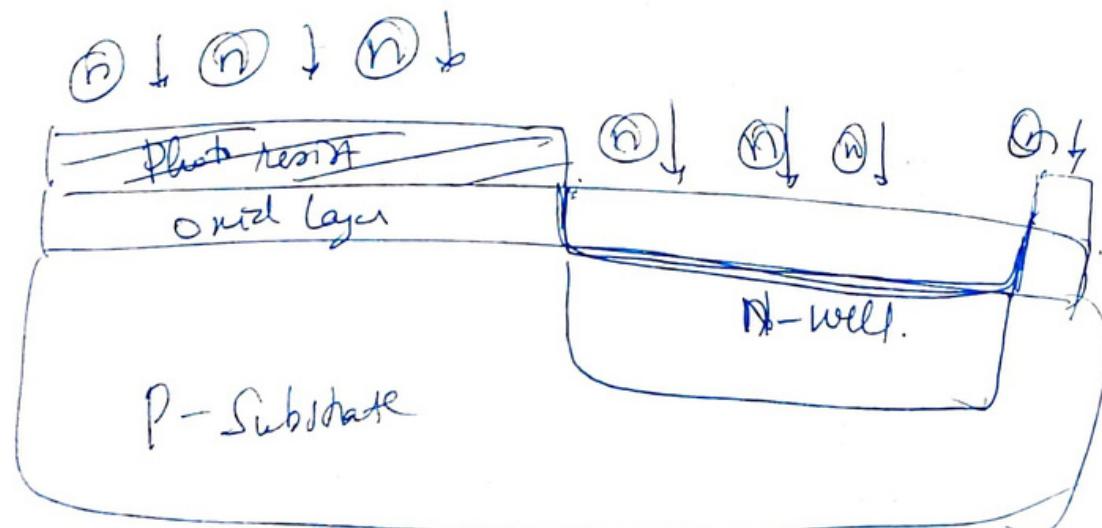
Fabrication Steps:

- Start with blank wafer (for n-well process)
wafer is of p-type where NMOS is created
- First step will be to form the n-well (where PMOS would reside)
- Forming the n-well requires adding enough Group V dopants into the silicon substrate to change the substrate from p-type to n-type in the region well.
- The oxide must be patterned to define the well
- An organic photoresist that softens when exposed UV light rays is spun onto the wafer.
- The pattern for n-well will be created with the aid of mask layer.
- The mask layer will be transparent where the well should be and opaque in the remaining area.
- The photoresist is exposed to UV light rays through n-well mask

UV light rays.



- the softened photo resist can be easily removed as they are soluble in many chemicals
- the hardened resist layer protects the underlying oxide layer from removal process.
- The oxide is etched away (removed) with hydrofluoric acid (HF) where it is not protected by the photo resist
- To define the region of n-well, we grow a protective layer of oxide over the entire wafer.
- Then, remove oxide layer where we want the wells
- we then add the n-type dopants
- The dopants are blocked by oxide
- But enter the substrate
- And the n-well will be formed where there is no oxide



CMOS Characteristics-

→ CMOS: Complementary Metal Oxide Semiconductor
 NMOS (N-Type Metal Oxide Semiconductor) Transistors
 PMOS (P-Type Metal Oxide Semiconductor) Transistors

→ NMOS Transistor

↳ Apply a High (Vdd) to its gate turns the transistor into a "conductor"

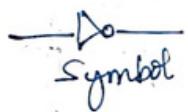
↳ Apply a Low (GND) to its gate shuts off the conduction path.

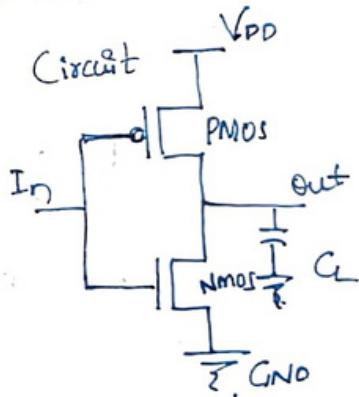
→ PMOS Transistor

↳ Apply a High (Vdd) to its gate shuts off the conduction path

↳ Apply a Low (GND) to its gate turns the transistor into a "conductor"

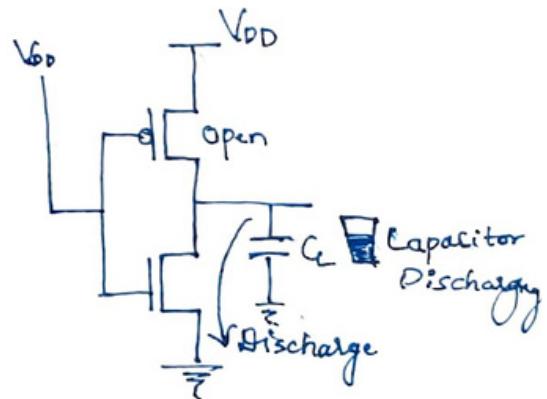
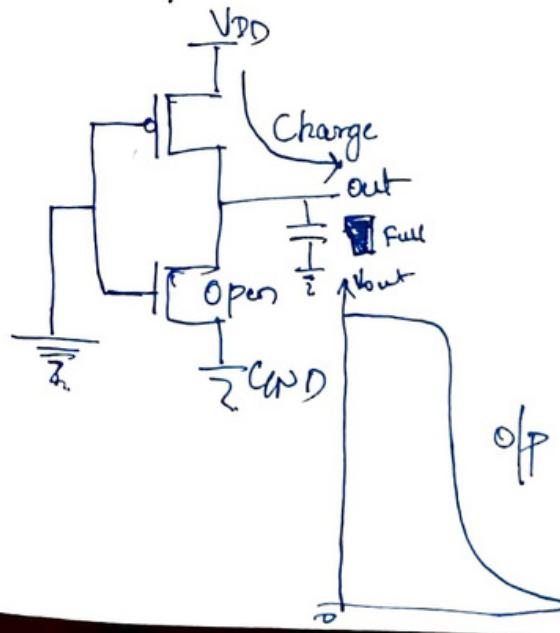
* Basic Component - CMOS Inverter.

→  Symbol



Why PMOS connected to VDD is bcz PMOS are Strong 1
 NMOS are Strong 0

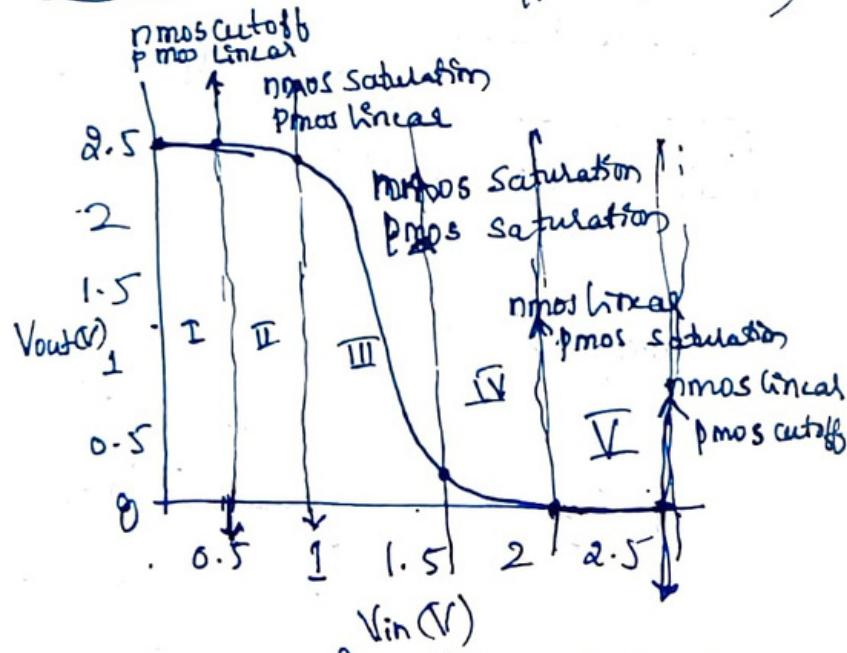
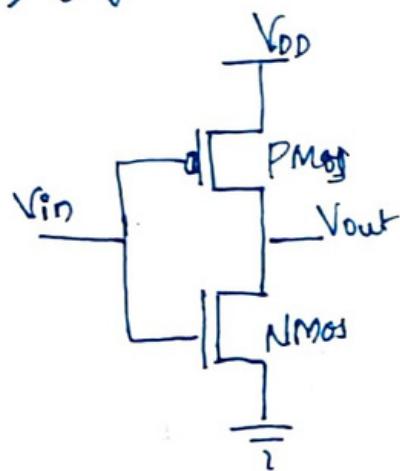
Invert operation.



#CMOS Properties -

- Drive large fan-out
- High noise margins (is required for good circuit)
- Logic levels independent of device sizes
- Always a path to V_{DD} or GND in steady state
- Low output impedance (Output resistance in k_O range)
- less sensitive to noise
- Extremely high input resistance (I/P characteristic for circuit)
- No direct path steady-state between power and ground.

Voltage Transfer Characteristics (Relation b/w O/P V & I/P V)



→ PMOS & NMOS will be working in different regions

↳ Three major regions

① Saturation

② Cut-off

③ Linear region

Design for Performance :-

w - width
L - Length

(Aspect ratio)

- Increase W/L Ratio of the transistor
 - ↳ The most powerful and effective performance optimization tool in the hands of the designer.
- Reduce CL (Load capacitive)
 - ↳ Keep drain diffusion small
 - ↳ Limit interconnect capacitance.
 - ↳ Limit fan-out
- Increase V_DO (Supply Voltage)
 - ↳ Trade-off energy for performance.
 - ↳ Increasing V_DO above a certain level yields minimal improvements.
 - ↳ Reliability concerns enforce a firm upper bound on V_DO

Design Metrics :-

Design metrics that govern digital design is crucial

- ↳ functionality.
- ↳ Cost
 - ↳ NRE (fixed) costs - design effort
 - ↳ RE (Variable) costs - cost of parts, assembly, test
(Reusable Engineering cost)
- Reliability, Robustness
 - ↳ Noise margins.
 - ↳ Noise immunity.
- Performance
 - ↳ Speed (delay)
 - ↳ power consumption; energy.

Cost of Integrated Circuits:

→ NRE (non-recurring engineering) costs

↳ Fixed cost to produce the design

↳ Design effort

↳ Design verification effort

↳ Mask generation.

↳ Influenced by the design complexity & designs

productivity.

↳ More pronounced for small volume products.

→ Recurring costs - proportional to product volume.

↳ Silicon processing

↳ Also proportional to chip area.

↳ Assembly (packing)

↳ Test

Reliability - Noise in Digital Integrated Circuits

→ Noise - Unwanted variations of Voltage and currents at the logic nodes

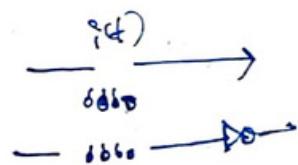
$$\frac{V(t)}{\frac{1}{T}} \rightarrow$$

→ From two wires placed side by side

↳ Capacitive coupling

↳ Voltage change on one wire

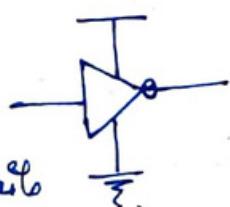
can influence signal on the neighboring wire



↳ Crosstalks

→ Inductive coupling

↳ Current change on one wire can influence signal on the neighboring



→ From noise on the power and ground supply lines

↳ Can influence signal levels on the gate

Noise Margin:-

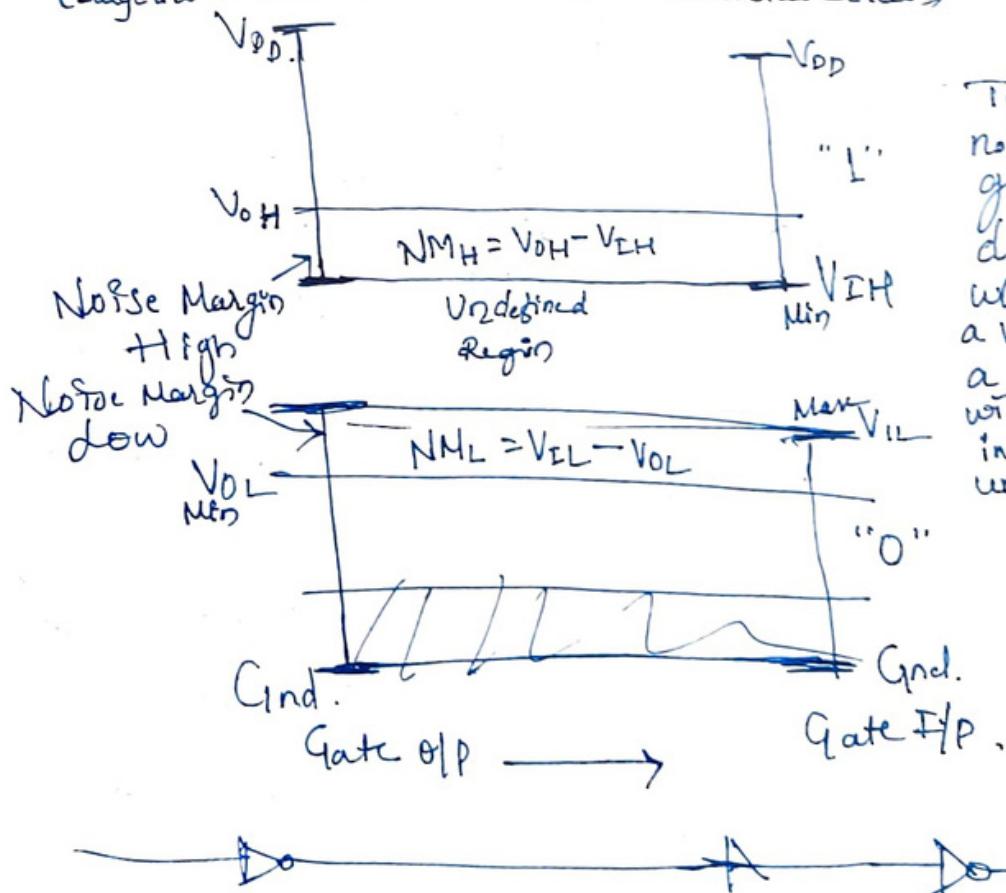
→ In a digital circuit, the noise margin is the amount by which the signal exceeds the threshold for a proper '0' or '1'.

For example:

- A digital circuit might be designed to swing between 0.0 and 1.2 volts, with anything below 0.2 volts considered '0', and anything above 1.0 volts considered a '1'.
- Then the noise margin for a '0' would be the amount that a signal is below 0.2 volts, and the noise margin for a '1' would be the amount by which a signal exceeds 1.0 volts.

→ Robust circuits want the '0' and '1' intervals to be as large as possible.

→ Large noise margins are desirable, but not sufficient (large b/c there will be very less undefined region) (meta-stable state)



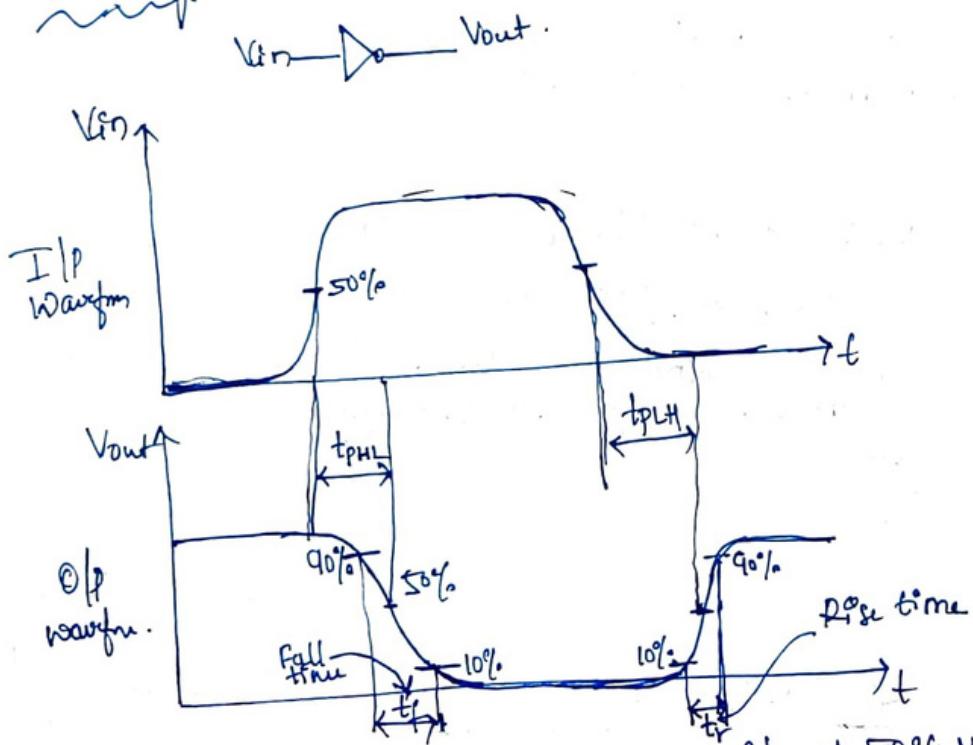
The higher the noise margin, the greater the difference b/w what is considered a valid high or a valid low without going into an undefined region.

Noise immunity :-

→ Noise immunity expresses the ability of the system to process and transmit information correctly in the presence of noise.

→ For good noise immunity, the signal swing (i.e. the difference b/w V_{OH} and V_{OL}) and the margin have to be large enough to overpower the impact of fixed sources of noise.

Delay :-



t_{PHL} → The time required for I/P to change 50% value

The taken for O/p to change 50% of initial value

t_{PLH} → Time duration for I/P to change 50% of final value
to O/p to change 50% of final value

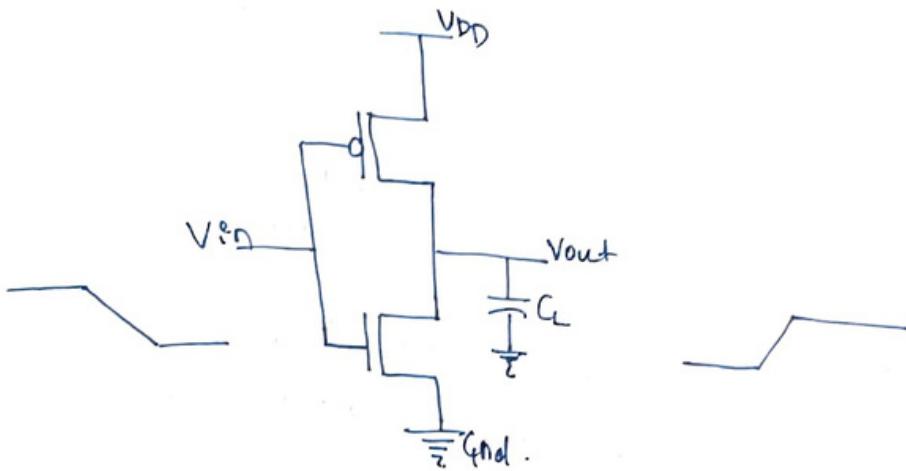
Propagation Delay

$$t_p = (t_{PHL} + t_{PLH}) / 2$$

Rise time → Time taken for O/p
change from 10% to 90% of
the final value

Fall time → O/p to change 90% of initial value to 10%
of the final value

Dynamic Power Consumption :-



$$\text{Energy / Transition} = C_L \times V_{DD}^2 \times P_0 \rightarrow 1 \xrightarrow{\text{means charging}} \text{without care sent to}$$

$$P_{DYN} = (\text{Energy / Transition}) * f = C_L \times V_{DD}^2 \times P_0 \rightarrow 1 \times f$$

Lowering Dynamic Power :-

Capacitance : function of fanout
wire length, transistor size

$$P_{DYN} = C_L \times V_{DD} \times P_0 \rightarrow 1 \times f$$

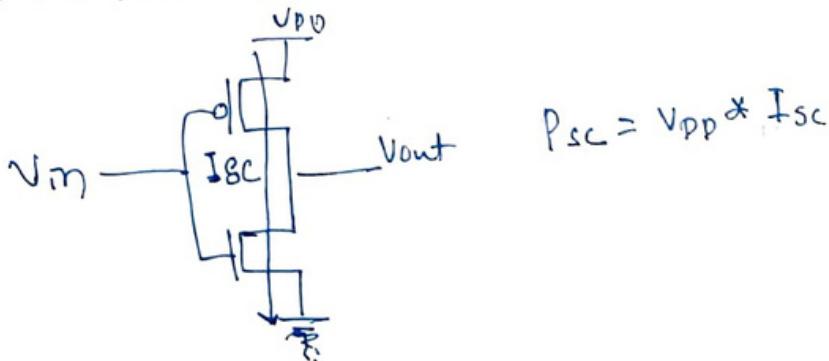
Activity factor : how often,
On average, do wires switch?

Supply Voltage : has been
dropping with successive
generations.

Clock frequency : Increasing

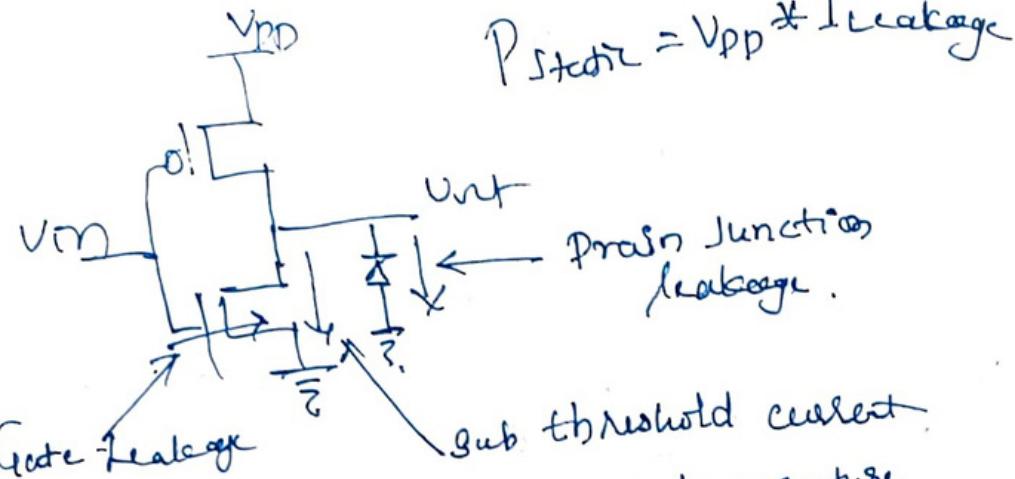
Short Circuit Power Consumption

→ Finite Slope of the i/p signal causes a direct current path
b/w VDD and GND for a short period of time during switching
when both the NMOS and PMOS transistors are conducting.



$$P_{SC} = V_{DD} \times I_{SC}$$

Leakage (Static) Power Consumption:-



$$P_{\text{static}} = V_{\text{DD}} \times I_{\text{leakage}}$$

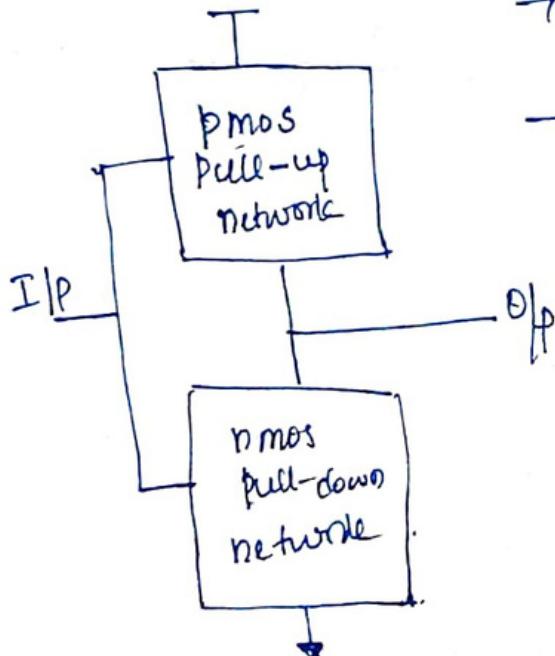
All increase exponentially with temperature.

* CMOS Energy & Power Equations:-

$$E = C_L V_{\text{DD}}^2 P_0 \rightarrow 1 + I_{\text{sc}} \cdot V_{\text{DD}} I_{\text{sc}} P_0 \rightarrow 1 + V_{\text{DD}} I_{\text{leakage}} t$$

$$P = C_L V_{\text{DD}}^2 P_0 \rightarrow 1 + V_{\text{DD}} I_{\text{sc}} + V_{\text{DD}} I_{\text{leakage}}.$$

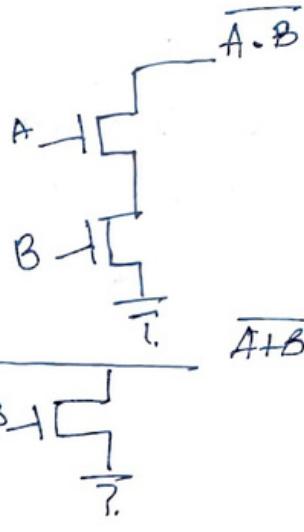
* CMOS Circuit Design:-



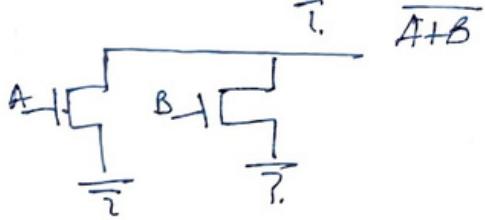
- Pull-up network is complement of pull-down
- Complementary CMOS logic gates
- ↳ nMOS pull-down D/W
- ↳ pMOS pull-up D/W

Construction of PPN's

→ NMOS devices in series implement a NAND function



→ NMOS devices in parallel implement a NOR function



Dual PUN and PDN :-

→ PUN and PDN are dual networks

→ DeMorgan's theorems

$$(\overline{A+B}) = \overline{A} \cdot \overline{B} = [!(A+B) = !A \cdot !B \text{ or } !(A+B) = !A + !B]$$

$$(\overline{A \cdot B}) = \overline{A} + \overline{B} = [!(A \cdot B) = !A + !B \text{ or } !(A \cdot B) = !A \cdot !B]$$

→ A parallel connection of transistors in the PUN corresponds to a series connection of the PDN

→ Complementary gate is naturally inverting (NAND, NOR)

→ Number of transistors for an N-flip logic gate is 2^N .

Signal Strength :-

→ Strength of signal.

↳ How close it approximates ideal voltage source.

↳ GND rails are strongest 1 and 0

→ V_{DD} and GND rails are strongest 1 and 0

→ nMOS pass strong 0

↳ But degraded or weak 1

→ pMOS pass Strong 1

↳ But degraded or weak 0.

→ Thus nMOS are best for pull-down n/w & pMOS are best for pull-up n/w.

Values and Strength

→ Values: 0 1 x and z

↳ 0 - represents a logic zero, or a false condition.

↳ 1 - represents a logic one, or a true condition

↳ x - represents an unknown logic value

↳ z - represents a high-impedance state.

→ Strength

↳ Strongest signal prevails.

↳ Useful for switch level modeling and not for RTL

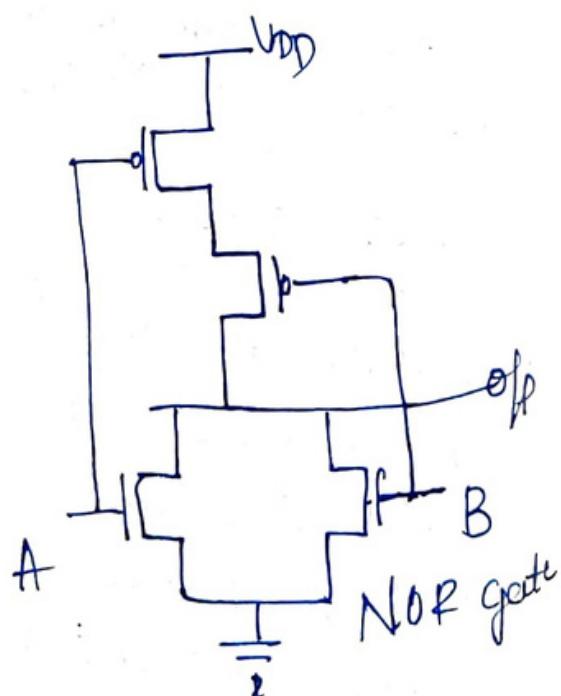
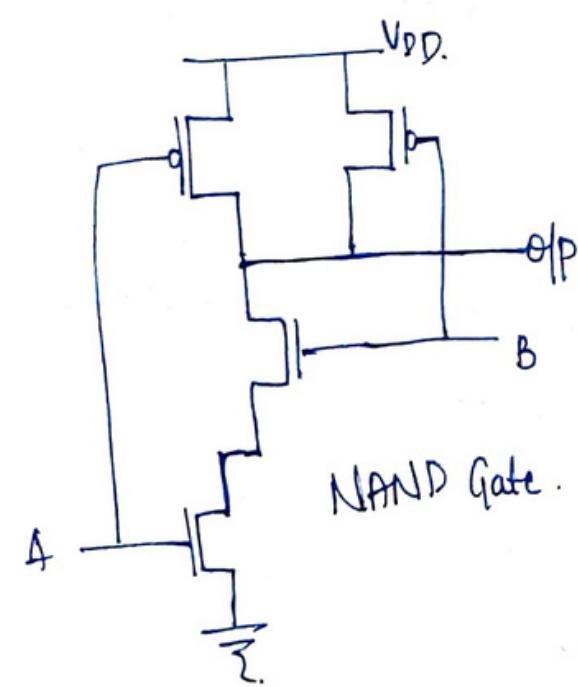
Basic Logic gates:-

$$y = (\overline{A} \cdot B)$$

A	B	Out
0	0	1
0	1	1
1	0	0
1	1	0

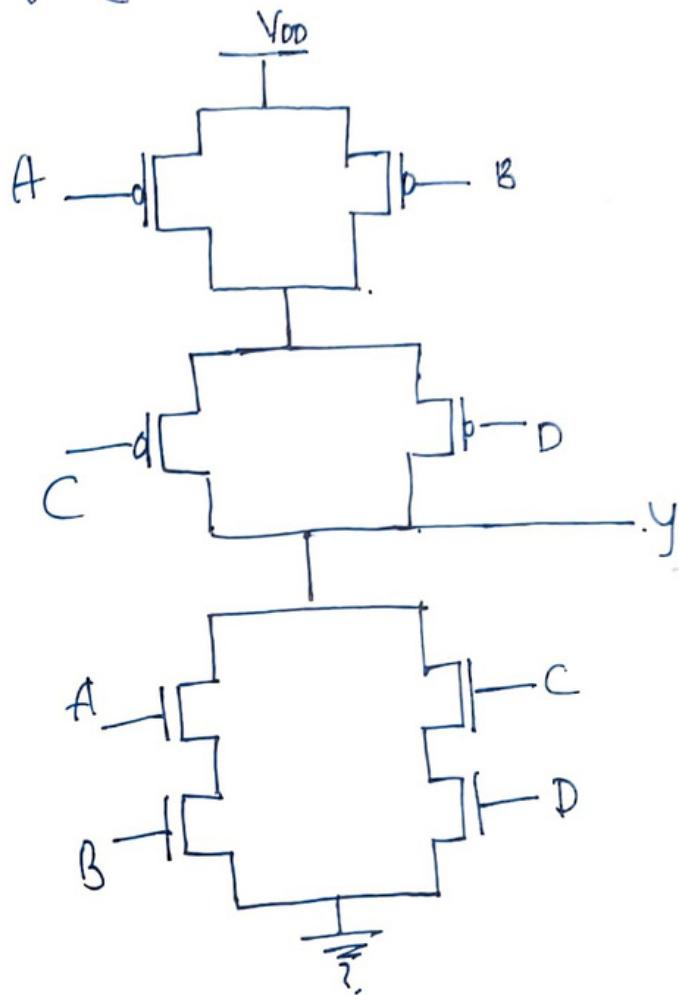
$$y = (\overline{A} + \overline{B})$$

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

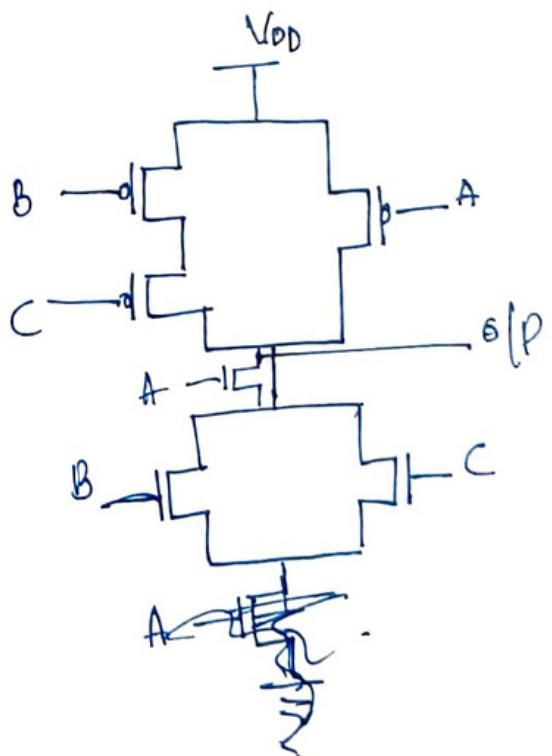


Example :-

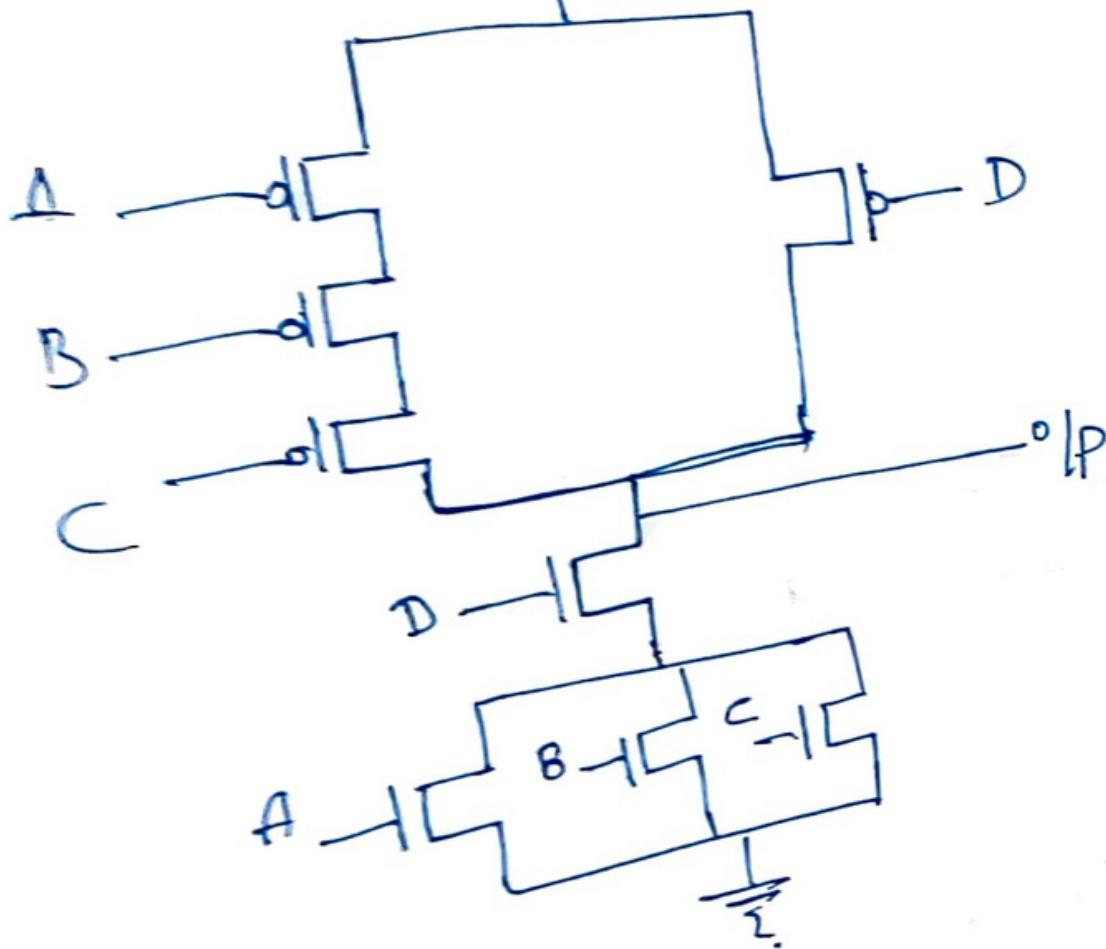
$$y = (A \cdot B + C \cdot D)$$



$$y = \overline{A \cdot (B+C)}$$



$$Y = \overline{((A+B+C) \cdot D)}$$



* PP2006

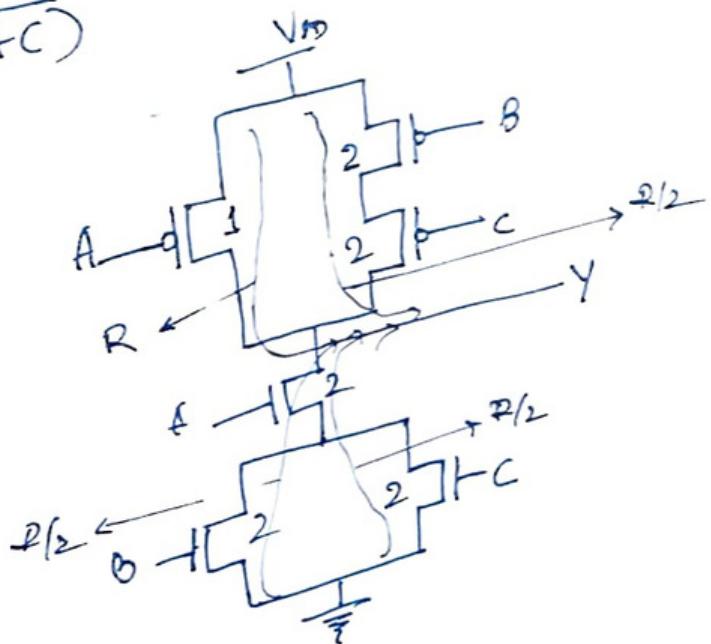
CMOS Transistor Sizing :-

→ Relative Transistor Sizing:-

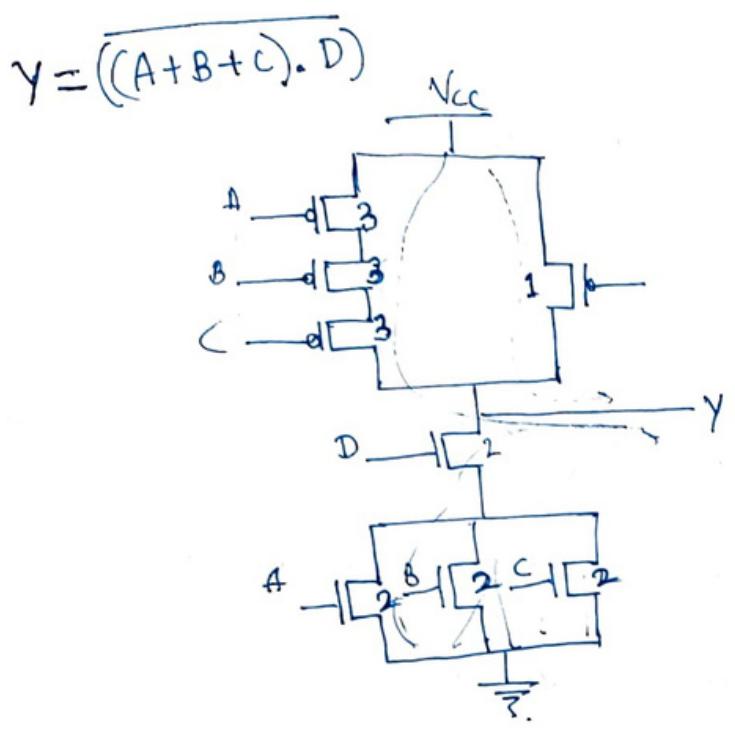
- ↳ When designing static CMOS circuits, balance the driving strengths of the transistors by making the PMOS section wider than the NMOS. Section to
 - ↳ maximize the noise margins and
 - ↳ obtain symmetrical characteristics.
- NMOS device has approximately 3.5× the drive strength of PMOS device
 - ↳ Mainly due to differences in mobility of carriers.
 - ↳ In practice, a ratio of 2-2.5× is measurable.

Exercise :-

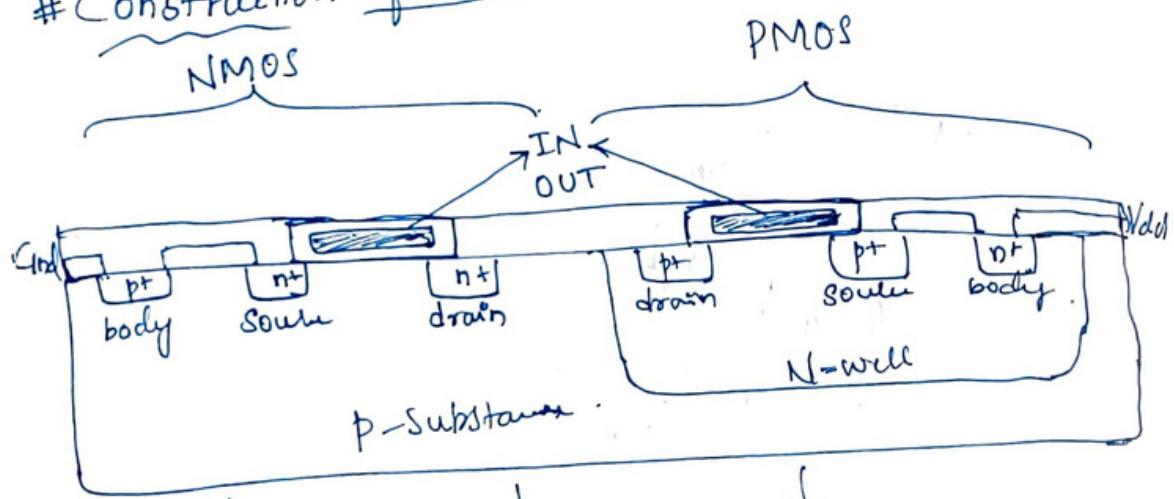
$$Y = \overline{A(B+C)}$$



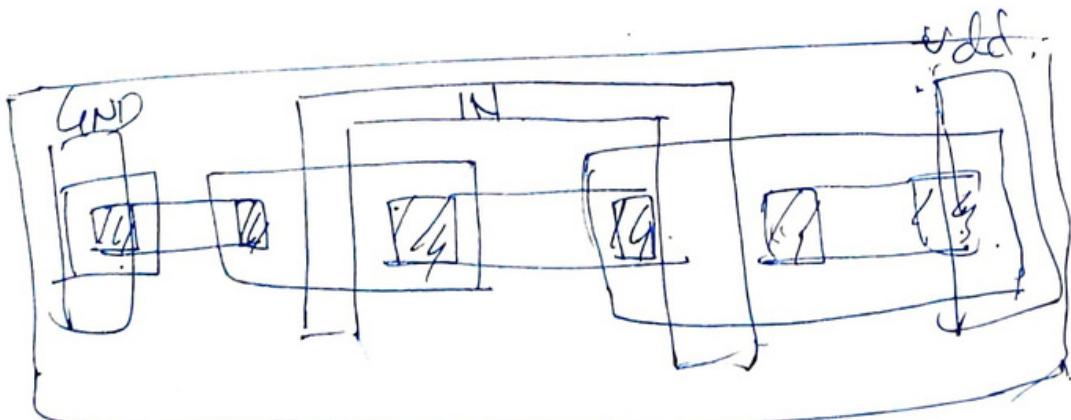
- * In case of PMOS Conduction due to Hole
- * NMOS conduction due to electrons.



Construction of CMOS Inverter:-



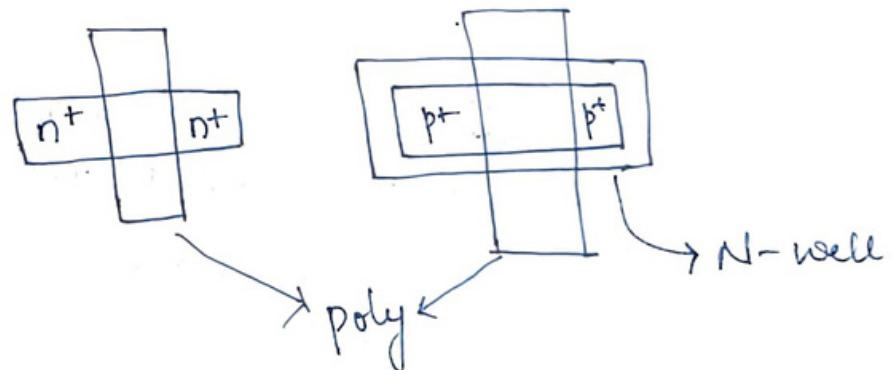
Inverter Cross-section & Top views:-



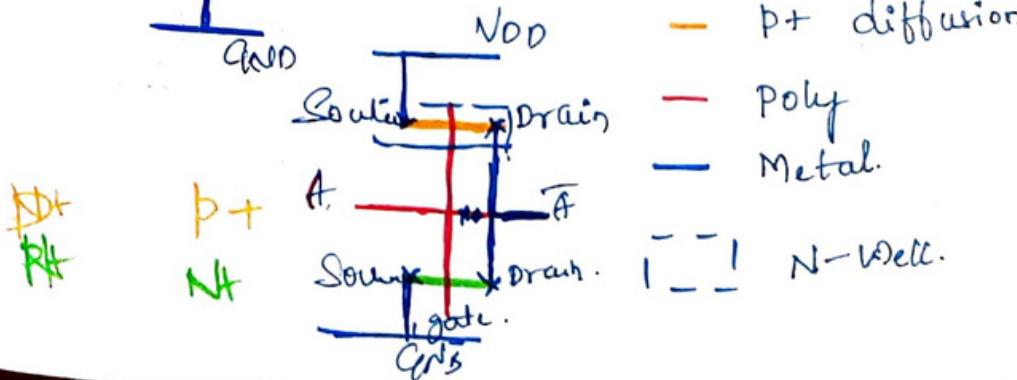
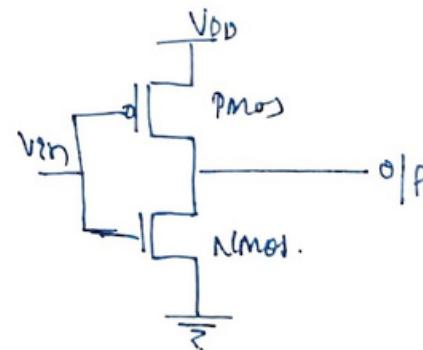
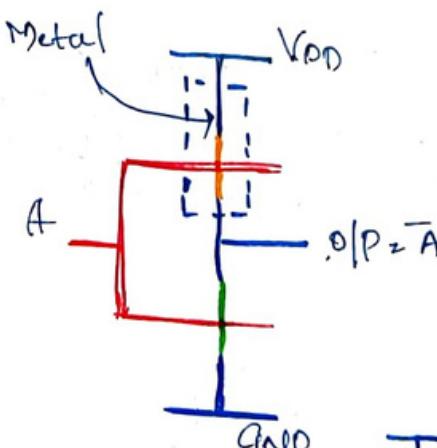
MOS layers:-

- N-well
- Active (Diffusion) of n-type or p-type
- poly
- Metal Contact (+ poly or active)
- Metal layer
- Via
- Gate Oxide
- Field Oxide (provides electrical isolation).

Top View of the MOSFET pattern:-



Simplified layout of CMOS Inverter:-



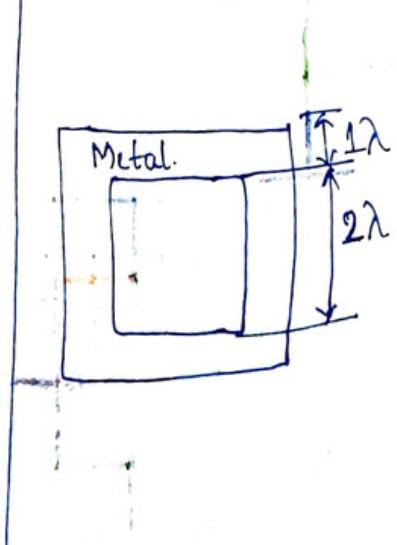
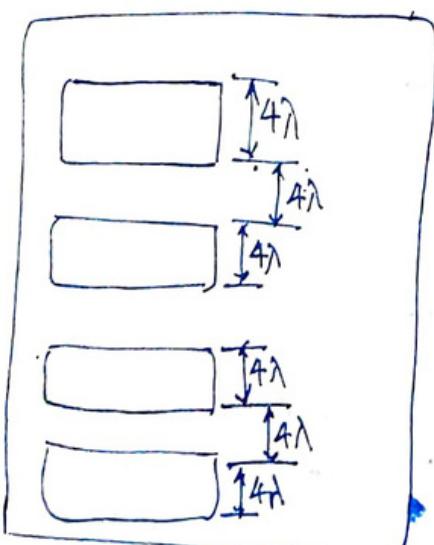
- What is Layout?
- The process of creating an accurate physical representation of an CMOS logic circuit that conforms to constraints imposed by the manufacturing unit.
- The layout should be drawn as per design rules.
- Layouts are used to estimate the floor area required to fabricate that particular logic circuit.
- Based on layouts, masks are prepared in the fab unit.

Layout Design Rules

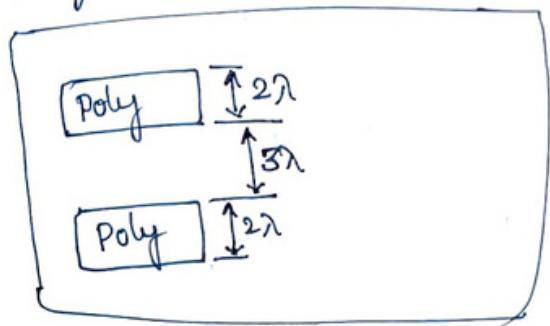
- These rules specify the size of each layer in the layout.
- Lambda (λ) based design rules are most popularly used design rules.
half of the channel length of MOSFET
(distance b/w drain & source in minimum poly wire)
- MOSIS is the organization that has set an industrial for λ based design rules.
- These rules describe the minimum spacing to avoid shorts b/w two lines.

Standard Layout Design Rules in n-well process

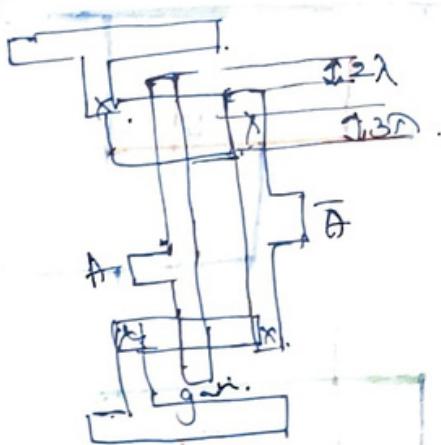
- Metal and Diffusion layers have minimum width and spacing of 4λ .
- Contacts are $2\lambda \times 2\lambda$ and must be surrounded by λ on the layers above and below.



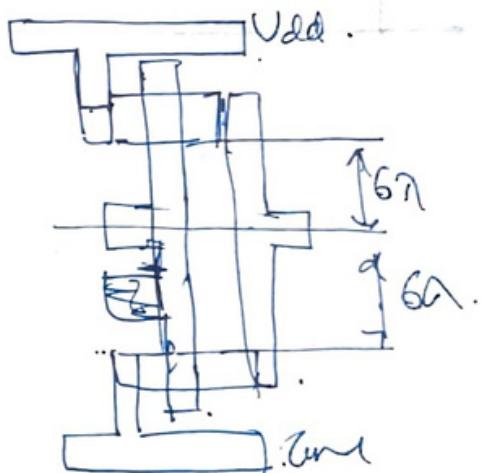
→ Poly uses a width of 2λ and a spacing of 3λ b/w two poly layers



→ Poly overlaps diffused by 2λ . Contacts have a spacing of 3λ from other contact.



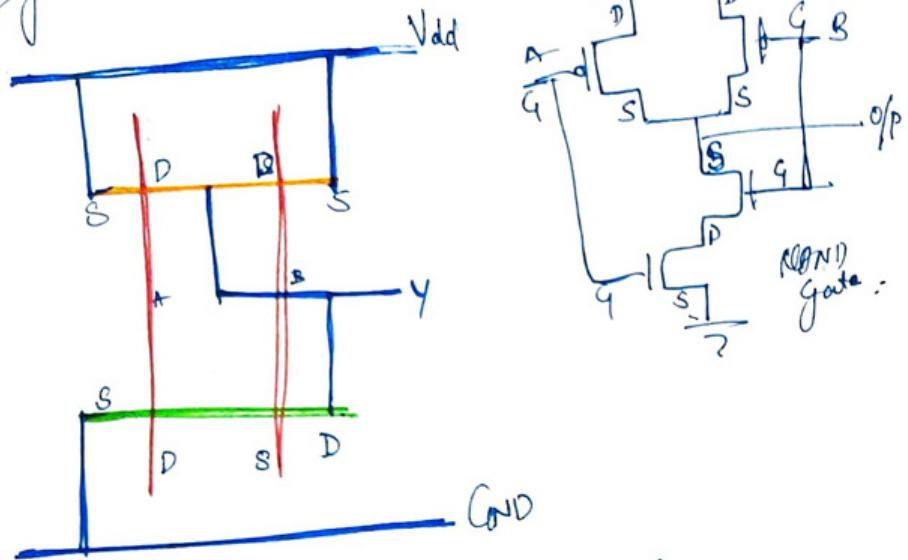
→ N-well surrounds PMOS transistors by 6λ and avoids NMOS transistors by 6λ .



Advantages of λ based design Rules:

- They make the scaling of layouts more easier.
- They same layout can be moved to a new process technology simply by specifying the new value of λ .

Layout of CMOS 2nd NAND Gate $y = \bar{A} \cdot \bar{B}$



Symbolic layout - stick diagram :-

→ layout structure may be cumbersome
to draw.

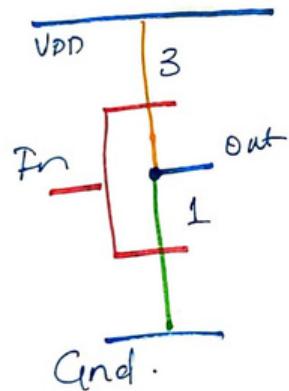
→ Instead use of symbolic layout approach.

→ Each of the different layers is represented with sticks.

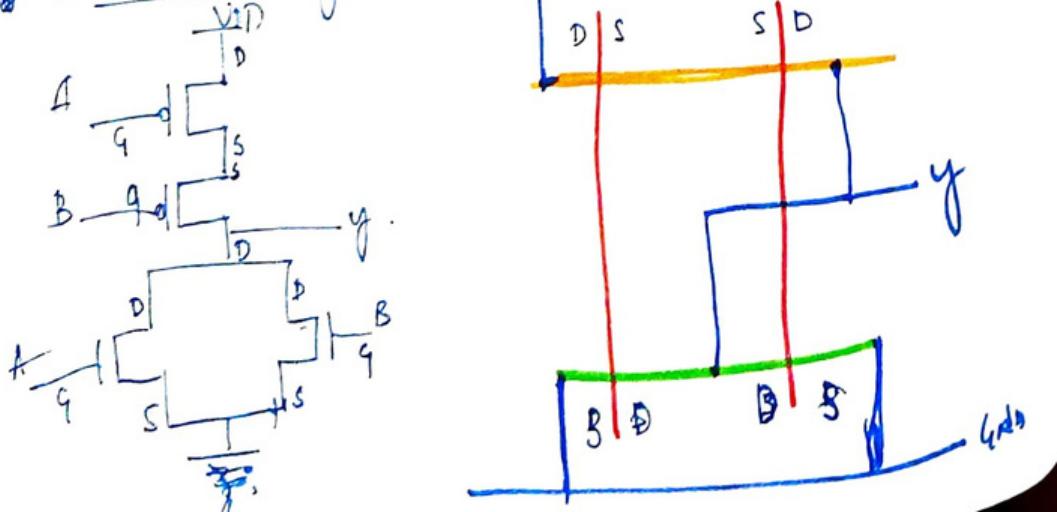
↳ the initials are dimensionless

↳ Positioning is most important

↳ Avoid dealing with rule checks at this stage.



~~Worst~~ - Layout and Stick Diagram:



Channel Length Modulation :-

→ Ideally

↳ I_{ds} is independent of V_{ds} for a transistor in saturation.

→ In Real

↳ P-n-p-n junction b/w the drain and body forms a depletion region with a width L_d that increases with V_{ds} .

$$\hookrightarrow L_{eff} = L - L_d$$

↳ Shorter channel length, higher resulting current I_{ds} with increasing V_{ds} .

+ Body Effect :-

→ The substrate is an implicit fourth terminal of a transistor.

→ The potential difference b/w the source and body V_{sb} affects the threshold voltage.

$$V_t = V_{to} + \gamma (\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s})$$

V_{to} — threshold voltage for zero substrate bias

ϕ — Surface potential.

γ — Body effect coefficient (range 0.4 to $1V_{t/2}$)

CMOS QUESTIONS

1. Ionization within a P-N junction causes a layer on each side of the barrier called the:
 - a. Junction
 - b. depletion region
 - c. barrier voltage
 - d. forward voltage

2. What causes the depletion region?
 - a. Doping
 - b. Diffusion
 - c. barrier potential
 - d. ions

3. What is an energy gap?
 - a. the space between two orbital shells
 - b. the energy equal to the energy acquired by an electron passing a 1 V electric field
 - c. the energy band in which electrons can move freely
 - d. an energy level at which an electron can exist

4. When an electron jumps from the valence shell to the conduction band, it leaves a gap. What is this gap called?
 - a. energy gap
 - b. hole
 - c. electron-hole pair
 - d. recombination

5. Forward bias of a silicon P-N junction will produce a barrier voltage of approximately how many volts?
 - a. 0.2
 - b. 0.3
 - c. 0.7
 - d. 0.8

6. When is a P-N junction formed?
 - a. in a depletion region
 - b. in a large reverse biased region
 - c. the point at which two opposite doped materials come together

- d. whenever there is a forward voltage drop
7. What is the voltage across R₁ if the P-N junction is made of silicon?
-
- ```
graph LR; V1[12 V] --- D[P --- N]; D --- R1[1 kOhm]; R1 --- G(());
```
- a. 12 V  
b. 11.7 V  
c. 11.3 V  
d. 0 V
8. If conductance increases as temperature increases, this is known as a:
- a. positive coefficient
  - b. negative current flow
  - c. negative coefficient
  - d. positive resistance
9. Which of the following cannot actually move?
- a. majority carriers
  - b. ions
  - c. holes
  - d. free electrons
10. What electrical characteristic of intrinsic semiconductor material is controlled by the addition of impurities?
- a. Conductivity
  - b. Resistance
  - c. Power
  - d. all of the above
11. Junction Field Effect Transistors (JFET) contain how many diodes?
- a. 4
  - b. 3
  - c. 2
  - d. 1

12. In the constant-current region, how will the IDS change in an n-channel JFET?

- a. As VGS decreases ID decreases.
- b. As VGS increases ID increases.
- c. As VGS decreases ID remains constant.
- d. As VGS increases ID remains constant.

13. A MOSFET has how many terminals?

- a. 2 or 3
- b. 3
- c. 4
- d. 3 or 4

14. IDSS can be defined as:

- a. the minimum possible drain current
- b. the maximum possible current with VGS held at -4 V
- c. the maximum possible current with VGS held at 0 V
- d. the maximum drain current with the source shorted

15. A very simple bias for a D-MOSFET is called:

- a. self-biasing
- b. gate biasing
- c. zero biasing
- d. voltage-divider biasing

16. With the E-MOSFET, when gate input voltage is zero, drain current is:

- a. at saturation
- b. zero
- c. IDSS
- d. widening the channel

17. When an input signal reduces the channel size, the process is called:

- a. Enhancement
- b. substrate connecting
- c. gate charge
- d. depletion

18. Which JFET configuration would connect a high-resistance signal source to a low-resistance load?

- a. source follower

- b. common-source
  - c. common-drain
  - d. common-gate
19. How will electrons flow through a p-channel JFET?
- a. from source to drain
  - b. from source to gate
  - c. from drain to gate
  - d. from drain to source
20. When  $V_{GS} = 0$  V, a JFET is:
- a. Saturated
  - b. an analog device
  - c. an open switch
  - d. cut off
21. When applied input voltage varies the resistance of a channel, the result is called:
- a. Saturation
  - b. Polarization
  - c. Cutoff
  - d. field effect
22. When is a vertical channel E-MOSFET used?
- a. for high frequencies
  - b. for high voltages
  - c. for high currents
  - d. for high resistances
23. When the JFET is no longer able to control the current, this point is called the:
- a. breakdown region
  - b. depletion region
  - c. saturation point
  - d. pinch-off region
24. With a JFET, a ratio of output current change against an input voltage change is called:
- a. transconductance
  - b. siemens
  - c. resistivity
  - d. gain

25. Which type of JFET bias requires a negative supply voltage?

- a. Feedback
- b. Source
- c. Gate
- d. voltage divider

26. The type of bias most often used with E-MOSFET circuits is:

- a. constant current
- b. drain-feedback
- c. voltage-divider
- d. zero biasing

27. The transconductance curve of a JFET is a graph of:

- a.  $I_S$  versus  $V_{DS}$
- b.  $I_C$  versus  $V_{CE}$
- c.  $I_D$  versus  $V_{GS}$
- d.  $I_D \times R_{DS}$

28. Which component is considered to be an "OFF" device?

- a. Transistor
- b. JFET
- c. D-MOSFET
- d. E-MOSFET

29. In an n-channel JFET, what will happen at the pinch-off voltage?

- a. the value of  $V_{DS}$  at which further increases in  $V_{DS}$  will cause no further increase in  $I_D$
- b. the value of  $V_{GS}$  at which further decreases in  $V_{GS}$  will cause no further increases in  $I_D$
- c. the value of  $V_{DG}$  at which further decreases in  $V_{DG}$  will cause no further increases in  $I_D$
- d. the value of  $V_{DS}$  at which further increases in  $V_{GS}$  will cause no further increases in  $I_D$

30. The primary function of the bias circuit is to

- a. hold the circuit stable at VCC
- b. hold the circuit stable at  $v_{in}$
- c. ensure proper gain is achieved
- d. hold the circuit stable at the designed Q-point

31. A JFET
- a. is a current-controlled device
  - b. has a low input resistance
  - c. is a voltage-controlled device
  - d. is always forward-biased
32. The capacitor that produces an ac ground is called a(n)
- a. coupling capacitor
  - b. dc open
  - c. bypass capacitor
  - d. ac open
33. When transistors are used in digital circuits they usually operate in the:
- a. active region
  - b. breakdown region
  - c. saturation and cutoff regions
  - d. linear region
34. A current ratio of  $IC/IE$  is usually less than one and is called:
- a. beta
  - b. theta
  - c. alpha
  - d. omega
35. In a C-E configuration, an emitter resistor is used for:
- a. Stabilization
  - b. ac signal bypass
  - c. collector bias
  - d. higher gain
36. Voltage-divider bias provides:
- a. an unstable Q point
  - b. a stable Q point
  - c. a Q point that easily varies with changes in the transistor's current gain
  - d. a Q point that is stable and easily varies with changes in the transistor's current gain

37. The digital logic family which has minimum power dissipation is

- a. TTL
- b. RTL
- c. DTL
- d. CMOS

38. CMOS circuits are extensively used for ON-chip computers mainly because of their extremely

- a. low power dissipation.
- b. high noise immunity.
- c. large packing density.
- d. low cost.

39. The guard rings are used to reduce

- a.  $V_t$
- b. latch up
- c. Width of channel
- d.  $C_{GS}$

40. The rate of oxidation depends on

- a) Supply of oxidation to the surface
- b) The reaction rate constant  $R_i$  and  $C_i$
- c) Mobility
- d) Both a and b.

41. The layers of MOS technology are isolated from each other by

- a. Dielectric
- b. Thinox
- c. Polysilicon
- d. Oxide layers

42. Load capacitance effects\_\_\_\_\_.

- a. Power Consumption
- b. Connectivity
- c. Chip Density
- d. None

43. An interconnect line is made from a material with resistivity  $4\text{ ohm/cm}$  and thickness of  $1200\text{ nm}$ . Sheet resistance is \_\_\_\_\_

- a.  $1375\Omega$
- b.  $1200\Omega$
- c.  $500\Omega$
- d.  $2000\Omega$

44. For P- transistor channel Rs in  $5\mu\text{m}$  technology is
- $10^4$
  - $2.5*10^4$
  - $3*10^4$
  - $3.5*10^4$
45. The source and drain are connected by a conducting channel but the channel may now be cleared by applying a suitable \_\_\_\_\_ voltage to the gate.
- Positive
  - negative
  - not possible
  - threshold voltage
46. Guard rings prevent the formation of \_\_\_\_\_ and contact cuts.
- Parasitic Transistors
  - Capacitance
  - Resistance
  - None
47. \_\_\_\_\_ is used to provide a connection between the output and Vdd any time the output of the logic gate is meant to be 1.
- Pull Up Network (PUN)
  - Pull Down Network (PUD)
  - A and b
  - None
48. If a gate is connected to a suitable positive voltage then a \_\_\_\_\_ is formed between the source and drain.
- Conductive layer.
  - Transistor
  - Capacitance
  - Resistance
49. The thickness of Silicon dioxide layer ( $\text{SiO}_2$ ) layer is typically \_\_\_\_\_ thick.
- $10\mu\text{m}$ .
  - $5\mu\text{m}$ .
  - $1\mu\text{m}$ .
  - $23\mu\text{m}$ .
50. The voltage applied between the gate and source of a MOS device, below which the drain -to-source current effectively drops to zero, is \_\_\_\_\_.
- Threshold voltage
  - Bulk Voltage
  - Parasitic voltage
  - None

51. The slope of the voltage transfer characteristics is equal to\_\_\_\_\_.

- a. -3/4
- b. 3
- c. -1
- d. 1

52. \_\_\_\_\_ is used to reduce the number of transistors required to implement a given logic information.

Ans: Ratioed Logic

53. Scaling improves the\_\_\_\_\_ by shrinking the dimensions of transistors and interconnection between them.

- a. packing density
- b. power dissipation
- c. figure of merit
- d. Channel Length

54. The high noise margin is given by  $NM_H =$

- a.  $2(V_{IH} - V_{OH})$
- b.  $V_{IH} - V_{OH}$
- c.  $V_{OH} - V_{IH}$
- d.  $V_{IH} + V_{OH}$

55. The process of transferring patterns of geometric shapes in a mask to a layer of radiation sensitive material for covering surface of semiconductor wafer is called

- a. Metallization
- b. Lithography
- c. Diffusion
- d. Ion implantation

56. Which of the following is due to the switching transient current and charging and discharging of load capacitance?

- a. static power dissipation
- b. dynamic power dissipation
- c. steady state power dissipation
- d. none of the above

57. The variation of threshold voltage due to source to substrate voltage is referred as\_\_\_\_\_

- a. Body effect
- b. Latch up
- c. ESD
- d. Antenna Effect

58. A parallel combination of nMOS and pMOS transistor is called as \_\_\_\_\_

- a. CMOS

- b. Transmission Gates
  - c. Dynamic CMOS
  - d. None
59. \_\_\_\_\_ is an alternate gate circuit that is used as supplement for complementary MOS circuits.
- a. Transmission Gates
  - b. Pesudo-Nmos
  - c. Both
  - d. None
60. The technique to increase number of devices per chip is called \_\_\_\_\_

ANS: Level of Integration

## **Question 1.**

**Why Does The Present Vlsi Circuits Use Mosfets Instead Of Bjts?**

## **Answer :**

Compared to BJTs, MOSFETs can be made very small as they occupy very small silicon area on IC chip and are relatively simple in terms of manufacturing. Moreover digital and memory ICs can be implemented with circuits that use only MOSFETs i.e. no resistors, diodes, etc.

## **Question 2.**

**What Are The Various Regions Of Operation Of Mosfet?  
How Are Those Regions Used?**

### **Answer :**

MOSFET has three regions of operation: the cut-off region, the triode region, and the saturation region.

The cut-off region and the triode region are used to operate as switch. The saturation region is used to operate as amplifier.

### **Question 3.**

**What Is Threshold Voltage?**

### **Answer :**

The value of voltage between Gate and Source i.e.  $V_{GS}$  at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called threshold voltage.

## **Question 4.**

**What Is Channel-length Modulation?**

### **Answer :**

In practice, when VDS is further increased beyond saturation point, it does has some effect on the characteristics of the MOSFET. When VDS is increased the channel pinch-off point starts moving away from the Drain and towards the Source. Due to which the effective channel length decreases, and this phenomenon is called as Channel Length Modulation.

## **Question 5.**

**Explain Depletion Region.**

## **Answer :**

When a positive voltage is applied across Gate, it causes the free holes (positive charge) to be repelled from the region of substrate under the Gate (the channel region). When these holes are pushed down the substrate they leave behind a carrier-depletion region.

## **Question 6.**

### **What Is Body Effect?**

#### **Answer :**

Usually, in an integrated circuit there will be several MOSFETs and in order to maintain cut-off condition for all MOSFETs the body substrate is connected to the most negative power supply (in case of PMOS most positive power supply). Which causes a reverse bias voltage between source and body that effects the transistor operation, by widening the depletion region. The widened depletion region will result in the reduction of channel depth. To restore the channel depth to its normal depth the VGS has to be increased. This is effectively seen as change in the threshold voltage -  $V_t$ . This effect, which is caused by applying some voltage to body is known as body effect.

## **Question 7.**

**Give Various Factors On Which Threshold Voltage Depends?**

### **Answer :**

As discussed in the above question, the  $V_t$  depends on the voltage connected to the Body terminal. It also depends on the temperature, the magnitude of  $V_t$  decreases by about 2mV for every 1oC rise in temperature.

## **Question 8.**

**What Are The Steps Required To Solve Setup And Hold Violations In Vlsi?**

**Answer :**

There are few steps that has to be performed to solved the set up and hold violations in VLSI. The steps are as follows:

- The optimization and restructuring of the logic between the flops are carried way. This way the logics are combined and it helps in solving this problem.
- There is way to modify the flip-flops that offer lesser setup delay and provide faster services to setup a device. Modifying the launch-flop to have a better hold on the clock pin, which provides CK->Q that makes the launch-flop to be fast and helps in fixing the setup violations.

## **Question 14.**

**What Are The Different Types Of Skews Used In Vlsi?**

**Answer :**

There are three types of skew that are used in VLSI. The skew are used in clock to reduce the delay or to understand the process accordingly. The skew are as follows:

**Local skew:** This contain the difference between the launching flip-flop and the destination flip-flop. This defines a time path between the two.

**Global skew:** Defines the difference between the earliest component reaching the flip flow and the the latest arriving at the flip flow with the same clock domain. In this delays are not measured and the clock is provided the same.

**Useful skew:** Defines the delay in capturing a flip flop paths that helps in setting up the environment with specific requirement for the launch and capture of the timing path.

## **01. Why Are Mosfets Used Instead Of Bjs In Today's Vlsi Circuits?**

**A.** MOSFETs, in comparison to BJTs, may be manufactured very small since they occupy a small silicon space on an IC chip and are relatively simple to manufacture. Furthermore, circuits that employ only MOSFETs, i.e. no resistors, diodes, or other components, can be used to create digital and memory ICs.

## **02. What Are Mosfet's Different Operating Regions? What Are the Functions of Those Regions?**

**A.** The cut-off area, the triode region, and the saturation region are the three operating regions of a MOSFET. To work as a switch, the cut-off region and the triode region are used. The saturation area is employed as amplification.

## **03. What Is Threshold Voltage and How Does It Work?**

**A.** The threshold voltage is defined as the voltage between Gate and Source (VGS) at which a sufficient number of mobile electrons aggregate in the channel region to produce a conducting channel ( $V_t$  is positive for NMOS and negative for PMOS).

## **04. What Does "The Channel Has Been Pinched Off" Mean?**

**A.** When  $V_{GS}$  is larger than  $V_t$ , a channel is induced in a MOSFET. As  $V_{DS}$  rises, current begins to flow from Drain to Source (triode region). When we increase  $V_{DS}$  to the point where the voltage between the gate and the channel at the drain end equals  $V_t$ , i.e.  $V_{GS} - V_{DS} = V_t$ , the channel depth at the drain end reduces to practically zero, and the channel is said to be pinched off. This is the point at which a MOSFET reaches saturation.

## **05. What Is Channel-length Modulation and How Does It Work?**

**A.** When  $V_{DS}$  is increased beyond the saturation point, it affects the MOSFET's properties in practice. The channel pinch-off point moves away from the Drain and towards the Source as  $V_{DS}$  is increased. As a result, the effective channel length shortens, a process known as Channel Length Modulation.

## **06. Explanation of the Depletion Region?**

**A.** When a positive voltage is supplied across Gate, free holes (positive charge) are repelled from the substrate region beneath the Gate (the channel region). When these pores are driven down the substrate, a carrier-depletion region is left behind.

## **07. What are the several factors that influence the threshold voltage?**

**A.** It is determined by the voltage applied to the Body terminal, as stated in the previous question. It also relies on the temperature; for every 10C increase in temperature, the amplitude of  $V_t$  reduces by around 2mV.

## **08. What Role Do Tie-High And Tie-Low Cells Play?**

**A.** Using either the power or the ground, tie-high and tie-low are utilized to link the transistors of the gate. The gates are connected to the power or ground, and the power bounce from the ground allows them to be turned off and on.

## **09. What Is Chain Reordering's Purpose?**

**A.** Due to the congestion generated by the positioning of the cells, the chain ordering system finds it difficult to route due to the optimization technique applied. Some tools automate the reordering of the chain to decrease the congestion caused by the first stage.

## **10. What Is An Enhancement Mode Transistor And What Does It Do?**

**A.** Because they rely on the electric field to change the shape and conductivity of the channel, enhancement mode transistors are also known as field-effect transistors. In a semiconductor material environment, this consists of one sort of charge carrier.

## **11. What Does It Mean To Have A Depletion Mode Device?**

**A.** Depletion modes are employed in MOSFETs, which are devices that stay on even when the gate-source voltage is zero. Load resistors are utilized in logic circuits, and this gadget contains them. This kind is employed in N-type depletion-load devices that allow for the measurement of threshold voltages and the use of -3 V to +3V.

## **12. What Are Tie-High And Tie-Low Cells, And How Do They Work?**

**A.** The gate of the transistor is connected to either power or ground using tie-high and tie-low cells. If the gate is coupled to power or ground in deep submicron processes, the transistor may be turned on or off owing to power or ground bounce.

## **13. What Is The Difference Between Latches And Flip-Flops?**

**A.** Flip-flops are edge sensitive, while latches are level sensitive. The difference between latch and flop design is that latch allows time borrowing, whereas a traditional flop does not. As a result, latch-based design becomes more efficient.

## **14. What Do the Terms “Local-skew,” “Global-skew,” and “Useful-skew” Mean?**

**A.** The disparity between the clock reaching the launching flop and the clock reaching the destination flip-flop of a timing path is known as local skew.

For the same clock domain, global skew is the difference between the earliest reaching

flip-flop and the latest reaching flip-flop. Useful skew is a notion that involves delaying the capturing flip-flop clock path to meet setup requirements in the launch and capture timing paths.

**15. Why is it that the number of gate inputs to CMOS gates is often limited to four?**

A. The gate will be slower as the amount of stacks increases. The number of gates in the stack of NOR and NAND gates is usually the same as the number of inputs plus one. As a result, the number of inputs is limited to four.

**16. What exactly is a multiplexer?**

A. A multiplexer is a circuit that selects one of several input signals and sends it to the single output.

**17. What does SCR (Silicon Controlled Rectifier) stand for?**

A. The SCR is a four-layered solid-state device that regulates the current flow. It's a form of rectifier that uses a logical gate signal to control it. It's a three-terminal gadget with four layers.

**18. What exactly is Slack?**

A. A time delay disparity between the expected and actual delay in a given path is referred to as slack. Slack can be both positive and unpleasant.

**19. What distinguishes Verilog from other programming languages?**

A. Verilog differs from other programming languages in the following ways.

- Concept of simulation time
- Several threads
- Primitive gates and network links are basic circuit ideas.

**20. What exactly is Verilog?**

A. The HDL (Hardware Description Language) Verilog is used to describe electronic circuits and systems. Circuit components are prepared inside a Module in Verilog. It includes behavioral as well as structural statements.

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21. Difference between analog layout and digital layout design?
22. What is fanin dependent delay?
23. What is the worst case propagation delay?
24. Difference between TTL and CMOS?
25. What is twin-tub process in CMOS VLSI?
26. What is p-well process in CMOS VLSI?
27. What is design rule check (DRC) in CMOS VLSI?
28. What is Intrinsic delay of the gate?
29. What is RC model in CMOS?
30. What is VLSI design flow?
31. What is Elmore delay in CMOS VLSI?
32. What is standard gate capacitance in CMOS VLSI?
33. What is sheet resistance in CMOS VLSI?
34. What is high to low transition in CMOS VLSI?
35. What are the limitation of Dynamic CMOS logic?
36. What are the objectives for Euler path and Stick Diagrams?
37. What is the worst case propagation delay of the circuit?
38. What is tpLH and tpHL in CMOS VLSI circuits?
39. What is Rise time in CMOS VLSI circuits?
40. With a neat diagram, explain the various timing parameters of a CMOS circuit?
41. What is dynamic logic design?
42. What is static logic design?
43. UV Lithography is used for?
44. What is the primary motivation for replacing planar MOSFETs with FinFETs?
45. What is stick diagram in CMOS?
46. What is fullform of ASIC is?
47. What is RTL in VLSI?
48. Which MOS is controlled in P-well, N-well and twin-tub process in fabrication?
49. Discuss the recent trends in fabrication technology?
50. Why P-sub is preferred over N-sub? Give reason.