DESIGN AND IMPLEMENTATION EFFICIENT DCT ARCHITECTURE

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Abstract— Two dimensional DCT takes a very important role in JPEG image and video compression. Architecture and Verilog design of 2-D DCT is described in this paper. Multiplier-free approximate DCT transforms have been proposed that that offer high compression performance at very low hardware complexity. The approximation can be realized using VLSI hardware using additions and subtractions only leading to decrease in chip area and power consumption compared to other DCT transforms. This paper comprises of a 8-point DCT approximation with 14 addition operation. The proposed approximation possesses low complexity in terms of computation and is compared to other DCT approximation in terms of algorithm complexity.

Index Terms— Approximate DCT, image compression, low complexity algorithms, low power consumption, multiplier free approximation.

I. INTRODUCTION

Image data compression has been an active research area for image processing and has been used in variety of applications. The noticeable fields are geospatial remote sensing, traffic cameras, automatic surveillance, homeland security, automotive industry and multimedia wireless sensor networks. In this context Discrete cosine transform is an essential tool for image processing.

DCT provides good energy compaction for natural images. Practically the image is defined over a large matrix of picture elements with each bit represented by 8 or 16 bit gray scale value. This representation is so large that it is difficult to store or transmit. The purpose of DCT is to reduce the size of image and to keep the most of the information in the original image.

The aim of the paper is to unfold the DCT approximation that possesses extremely low complexity with only 14 additions. Secondly hardware implementations of 2-D 8-point approximate is proposed. The approximate DCT under consideration is the DCT approximation. The implementation is fully time multiplexed 2-D architecture for 8 X 8 data blocks. The design is based on successive calls of 1-D architecture using separability property of the 2-D DCT Kernel.

II. DISCRETE COSINE TRANSFORM

DCT algorithm is very important due to its symmetry.DCT performs energy compaction in which the unwanted energy components are removed opting only required frequency components.Image is divided into blocks and in each block compression is carried out using quantization.

A. DCT Equations

The most common DCT definition of a 1-D sequence of length N is:

$$C(u) = \alpha(u)\sum_{x=0}^{N-1} f(x)\cos\left[\frac{\pi(2x+1)u}{2N}\right] \quad (1)$$

For u=0,1,2,N-1.Similarly,the inverse transformation is defined as

$$f(x) = \sum_{x=0}^{N-1} \alpha(u)c(u)\cos\left[\frac{\pi(2x+1)u}{2N}\right] \quad (2)$$

For x= 0,1,2,N-1.In both equations (1) and (2) α(u) is defined as

$$\alpha(u) = \begin{cases} \sqrt{\frac{1}{N}} & for\ u = 0 \\ \sqrt{\frac{2}{N}} & for\ u \neq 0 \end{cases} \quad (3)$$

It is clear from equation (1) that for

$$u = 0, c(u=0) = \sqrt{\frac{1}{N}}\sum_{x=0}^{N-1} f(x) \quad (4)$$

The first transform coefficient is referred to as the DC coefficient. All other transform coefficients are called the AC Coefficients.

B. Two Dimensional DCT

The 2-D DCT is a direct extension of the 1-D case and is given by

$$C(u,v)= a(u)a(v)\sum_{x=0}^{N-1}\sum_{y=0}^{N-1} f(x,y)\cos\left[\frac{\pi(2x+1)u}{2N}\right]\cos\left[\frac{\pi(2y+1)V}{2N}\right] \quad \ldots\ldots\ldots\ldots(5)$$

For u,v = 0,1,2,N-1 and (u) and (v) are defined in equation (4)

$$F(x,y)= a(u)a(v)\sum_{U=0}^{N-1}\sum_{v=0}^{N-1} C(u,v)\cos\left[\frac{\pi(2x+1)u}{2N}\right]\cos\left[\frac{\pi(2y+1)v}{2N}\right] \quad \ldots\ldots\ldots\ldots(6)$$

The 2-D basis functions can be generated by multiplying the horizontally oriented 1-D basis functions with vertically oriented set of same functions.

III. DCT PROCESS

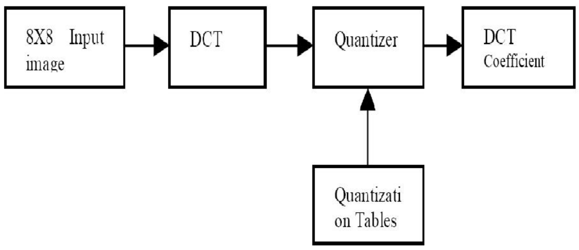

Fig.1 Block diagram of DCT Process

In DCT process the input image is divided into blocks of 8 X 8 pixels .The pixel values are converted into signed integer format and DCT is performed on each block.DCT transforms the pixel data into spatial frequencies that are called DCT coefficients .The output of DCT will result in most of the block energy being stored in the lower spatial frequencies .The higher frequencies will have values equal to or close to zero and hence can be ignored while encoding without affecting the quality of image.

The selection of quantized value is critical since it affects both compression efficiency and the reconstructed image quality.

The human eye in not as sensitive to high frequencies as that to low frequencies. The human eye is not able to differentiate changes in intensity or color that occur between successive pixels. When the DCT is used for compression purpose the quantizer forces the insignificant high coefficient value to be zero while retaining the important low frequency coefficients. The 2-D DCT transforms an 8x8 block of spatial data samples into an 8x8 block of spatial frequency components.

IV. REVIEW OF APPROXIMATE DCT METHODS

The mathematical description of the selected 8-point DCT approximation consists of a transformation matrix that can be put in the following format:
[diagonal matrix] x [low-complexity matrix]

The diagonal matrix usually contains irrational numbers in the form 1/√m, where m is a small positive integer. The low complexity matrix corresponds to the complexity of algorithm.

(i) Proposed transform

In order to derive a novel low complexity apporximate DCT we propose a search to 8X8 matrices that doesn't require a multiplication operations for its entries to gurantee a good candidate martices with low computation cost (i.e with minimumm Arithmetic operations).Thus we have the following optimization problem.

$$T^* = \arg\ min_T \ \text{cost}\ (T)$$

where $\mathbf{T}_*$ is the sought matrix and $\text{cost}(\mathbf{T})$ returns the arith-metic complexity of $\mathbf{T}$. Additionally, the following constraints were adopted:

1) Elements of matrix $\mathbf{T}$ must be in $\{0,\pm1,\pm2\}$ to ensure that resulting multiplicative complexity is null;

2) We impose the following form for matrix $\mathbf{T}$:

$$\mathbf{T} = \begin{bmatrix} a_3 & a_3 & a_3 & a_3 & a_3 & a_3 & a_3 & a_3 \\ a_0 & a_2 & a_4 & a_6 & -a_6 & -a_4 & -a_2 & -a_0 \\ a_1 & a_5 & -a_5 & -a_1 & -a_1 & -a_5 & a_5 & a_1 \\ a_2 & -a_6 & -a_0 & -a_4 & a_4 & a_0 & a_6 & -a_2 \\ a_3 & -a_3 & -a_3 & a_3 & a_3 & -a_3 & -a_3 & a_3 \\ a_4 & -a_0 & a_6 & a_2 & -a_2 & -a_6 & a_0 & -a_4 \\ a_5 & -a_1 & a_1 & -a_5 & -a_5 & a_1 & -a_1 & a_5 \\ a_6 & -a_4 & a_2 & -a_0 & a_0 & -a_2 & a_4 & -a_6 \end{bmatrix}$$

Where $a_i \in \{0,1,2\}$, for I = 0,1,….,6;

3) All rows of $\mathbf{T}$ are non-null;

4) Matrix $\mathbf{T}.\mathbf{T}^T$ must be a diagonal matrix to ensure orthog-onality of the resulting approximation.

Constraint 2) is required to preserve the DCT-like matrix structure. We recall that the *exact* 8-point DCT matrix is given by:

$$\mathbf{C} = \frac{1}{2}\cdot \begin{bmatrix} \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 & \gamma_3 \\ \gamma_0 & \gamma_2 & \gamma_4 & \gamma_6 & -\gamma_6 & -\gamma_4 & -\gamma_2 & -\gamma_0 \\ \gamma_1 & \gamma_5 & -\gamma_5 & -\gamma_1 & -\gamma_1 & -\gamma_5 & \gamma_5 & \gamma_1 \\ \gamma_2 & -\gamma_6 & -\gamma_0 & -\gamma_4 & \gamma_4 & \gamma_0 & \gamma_6 & -\gamma_2 \\ \gamma_3 & -\gamma_3 & -\gamma_3 & \gamma_3 & \gamma_3 & -\gamma_3 & -\gamma_3 & \gamma_3 \\ \gamma_4 & -\gamma_0 & \gamma_6 & \gamma_2 & -\gamma_2 & -\gamma_6 & \gamma_0 & -\gamma_4 \\ \gamma_5 & -\gamma_1 & \gamma_1 & -\gamma_5 & -\gamma_5 & \gamma_1 & -\gamma_1 & \gamma_5 \\ \gamma_6 & -\gamma_4 & \gamma_2 & -\gamma_0 & \gamma_0 & -\gamma_2 & \gamma_4 & -\gamma_6 \end{bmatrix}$$

Where $Y_k = \cos(2\pi(k+1)/32)$, k=0,1,….,6;

Above optimization problem is algebraically intractable. with comprehensive computational search.I found 8 minimal cost matrices among which one with best performance in terms of image quality of compressed images with JPEG like technique is separated.

An important parameter in the image compression routine is the number of retained coefficients in ther transform domain. In several applications the number of retained coefficient is very low like For Ex- Bouguezel applied only 10 DCT coefficient when assessing image compression method. Therefore I adopted the number of retained coefficient equal to 10 as suggested by the bouguezel.

The solution of (1) is the following DCT approximation:

$$C^* = D^*.T^*$$

$$= \mathbf{D}^* \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & -1 & -1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 \end{bmatrix}$$

WhereD*=diag([1//√8,1/√2,1/2,1/√2,1/√8,1/√2,1/2,1/√2]} Matrix T* has enteries in {0,±1} and it can be given a sparse factorization according to :$T^* = P_4 . A_{12} . A_{11} . A_1$, Where

$$\mathbf{A_{11}} = \mathrm{diag}\left(\begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix}, \mathbf{I}_4\right)$$

$$\mathbf{A_{12}} = \mathrm{diag}\left(\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, -1, \mathbf{I}_5\right)$$

And P_4 is the permutation (1)(2 5 6 8 4 3 7).

(B) CB-2011 Approximation

By means of judiciously rounding-off the elements of the exact DCT matrix results into 8-point approximation matrix which is orthogonal and contains only elements in {0,±1}. Clearly, it possesses very low arithmetic complexity. The matrix de-rived transformation matrix $\mathbf{C_2}$ is given by.

$C_2 = D_2 . T_2$

$$= \mathbf{D_2} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & -1 & -1 & -1 \\ 1 & 0 & 0 & -1 & -1 & 0 & 0 & 1 \\ 1 & 0 & -1 & -1 & 1 & 1 & 0 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & 0 & 1 & -1 & 0 & 1 & -1 \\ 0 & -1 & 1 & 0 & 0 & 1 & -1 & 0 \\ 0 & -1 & 1 & -1 & 1 & -1 & 1 & 0 \end{bmatrix}$$

Where D_2 = diag(1/√8,1/√6,1/2,1/√6,1/√8,1/√6,1/2,1/√6) An efficient factorization for the fast algorithm for T_2 is described as below: $T = P_2 . A_6 . A_5 . A_1$ Where

$$\mathbf{A_5} = \mathrm{diag}\left(\begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix}, \begin{bmatrix} -1 & 1 & -1 & 0 \\ -1 & -1 & 0 & 1 \\ 1 & 0 & -1 & 1 \\ 0 & 1 & 1 & 1 \end{bmatrix}\right)$$

and

$$\mathbf{A_6} = \mathrm{diag}\left(\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, -1, \mathbf{I}_5\right).$$

Matrix P_2 corresponds to the following permutation (1)(2 5 8)(3 7 6 4).

V. PROPOSED TWO DIMENSIONAL DCT ARCHITECTURE

In this implementation, we explore four design of hardware implementation using verilog HDL and evaluate the area-performance trade-off. The design comprises of four modules per design point , one module for DCT computation, one module for IDCT computation, one top module that instantiates both the DCT and IDCT modules and a test bench to test the entire design.

Core idea is to implement a fully pipelined architecture that takes 8 inputs and provides a single DCT output which in turn is used to compute the IDCT . A 1D-DCT is implemented on the input pixels first. The output of this so called the intermediate value stored in a RAM . The 2nd 1D-DCT operation is done on this stored value to give the final 2D-DCT outpur dct_2d. The inputs are 8bits wide and the 2d-dct are 9 bits wide. A 1D-DCT is implented on the input DCT values . This intermediate value is stored in a RAM. The 2nd 1D-DCT operation is done on this stored value to give the final 2D-DCT output idct_2d. The inputs are 9 bits wide and 2d-idct outputs are 8 bits wide.The 8X8 1D-DCT Transform is expressed as.

$$z_k = \frac{c(k)}{2}\sum_{i=0}^{7} cos\frac{(2i+1)k\pi}{16}x_i \qquad ,k=0,1,2\ldots\ldots7$$

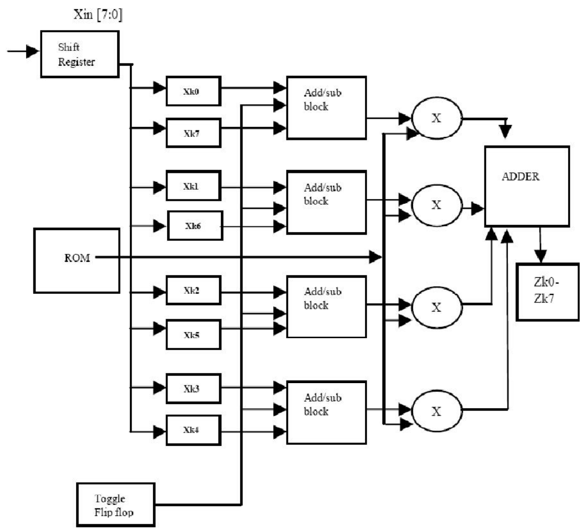

Fig 2: 1D-DCT Architecture

A. Transposed buffer

All the ouputs of the adder are stored in RAMS . When WR is high, the corresponding RAM address takes the right operations . Otherwise the contents of the RAM address are read. The period of the address signals is 64 times of the input clocks . Two RAMS are used so that data write can be continuous . The 1st valid input for the RAM1 is available at the 15th clk RAM1 enable is active after 15 clks . After the write operation continue for 64 clks.At the 65th clock ,since z_out is continuous, we get the calid z_out_00.These2nd sets of valid 1D-DCT coefficients are written into RAM2 which is enabled at 15+64 clks. So at 65th Clk .RAM1 goes into read mode for the next 64clks and RAM2 is in Write mod .After this for every 64 clks, the read and write switches between th 2 RAMS. Data is written in different order ,data is assumed to be written in each row at a time in an 8XX matrix .When RAM1 is full , the 2nd 1D calculations can start.

B. Two Dimensional DCT CORE

The DCT core is two dimensional discrete cosine transform implementation designed for use in compression systems like JPEG . Architecture is based on parallel distributed arithmetic with butterfly computation. The 8 bit signed input pixels will provide a 12 bit signed output coefficient for the DCT. pixels will provide a 12 bit signed output coefficient for the DCT. The data bits are multiplied by 3 bits can result 11 bits and the sign bit to give a total of 12 bits.

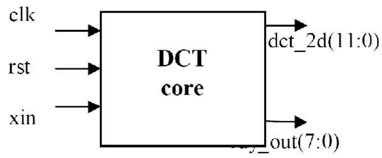

Fig 3: Top level schematic for DCT core

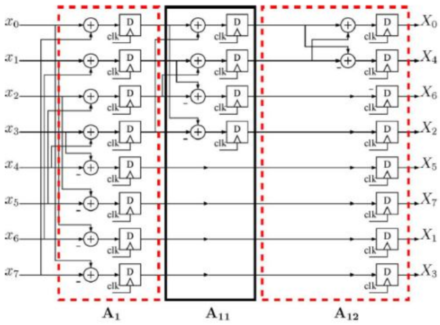

Fig 4: Proposed transform Architecture

VI. ARITHMETIC COMPLEXITY

We adopt the arithmetic complexity as figure of merit for estimating the computational complexity. The arithmetic complexity consists of the number of elementary arithmetic operations (additions/ subtractions, multiplications/divisions, and bitshiftoperations) required to compute a given transformation. In other words, in all cases, we focus our attention to the low-complexity matrices and the proposed matrix. For instance, in the context of image and video compression, the complexity of the diagonal matrix can be absorbed into the quantization step; therefore the diagonal matrix does not contribute towards an increase of the arithmetic complexity. Because all considered DCT approximations have null multiplicative complexity, we resort to comparing them in terms of their arithmetic complexity assessed by the number of additions/subtractions and bit-shift operations.

8X8 DCT	Proposed Method	CB 2011 approximatee DCT
Multipliers	0	0
Adders	14	22
Transpose Memory	Required	Required
Shifters	0	0
Scalability	Easy	Difficult
Structure Regularity	Regular	Not regular

Fig.5 Comparative study of DCT Method

VII. INTERPRETATION OF RESULTS

A. Verilog Implementation

DCT and IDCT both the blocks were written in the form of synthesizable Verilog code. Verilog test-benches were written and Cadence IUS simulator was used for behavioral simulation.After behavioral verification was done, RTL Complier was used to synthesize the Verilog code. Cadence RTL compiler was used to synthesize and generate schematic for both chips.

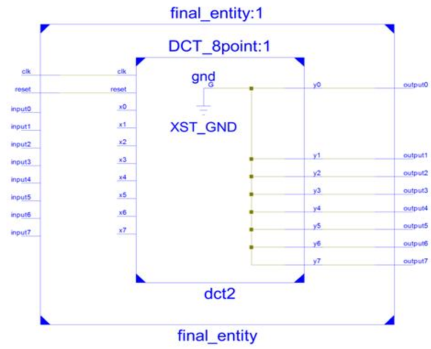

Fig.6 RTL view of 2-D DCT

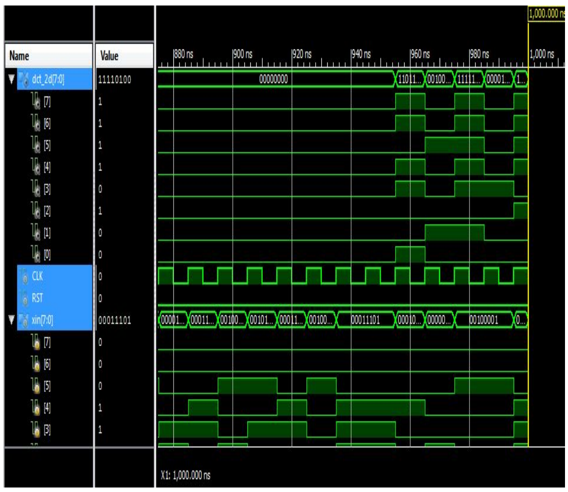

Fig.7 Verilog output of Proposed 2-D DCT

B. Power Analysis

CADENCE tool is used to simulate and synthesis the verilog HDL code. After power and area analysis is done.

Table I. Area and power analysis

DCT	Power in mW	Area in mm^2
Proposed DCT core	1.0278	0.6281
DCT Architecture [1]	29.78	0.343
DCT Core[12]	29.92	0.569

CONCLUSION

All transform coefficients can be encoded independently without compromising coding efficiency. In addition, the DCT packs energy in the low frequency regions. Therefore, some of the high frequency content can be discarded without significant quality degradation. Such A quantization scheme causes further reduction in the entropy (or average number of bits per pixel). However, the modified CB-2011 approximation and the proposed transform possess lower computational complexity and are faster than all other approximation method.

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