How to Setting ModelSim on Linux

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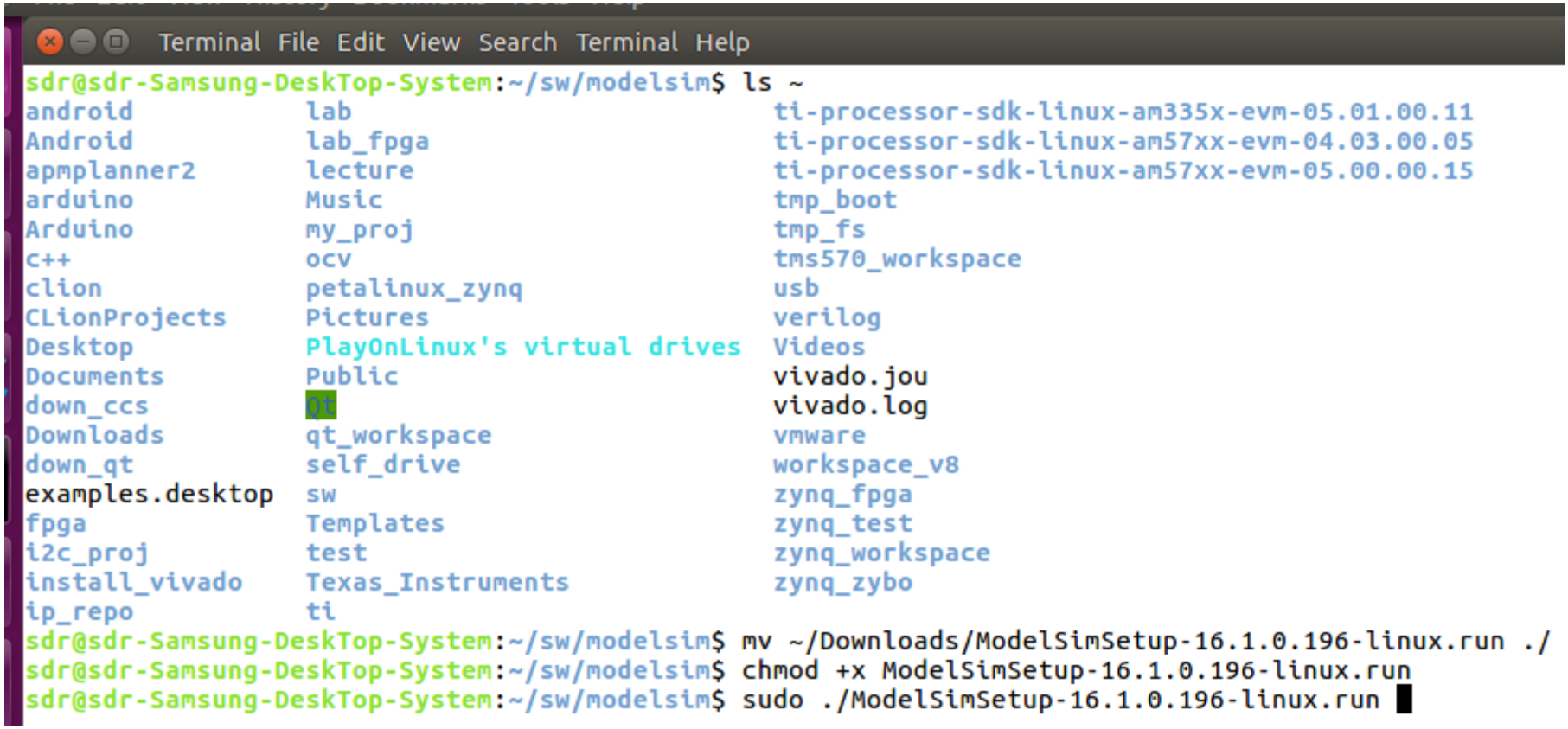
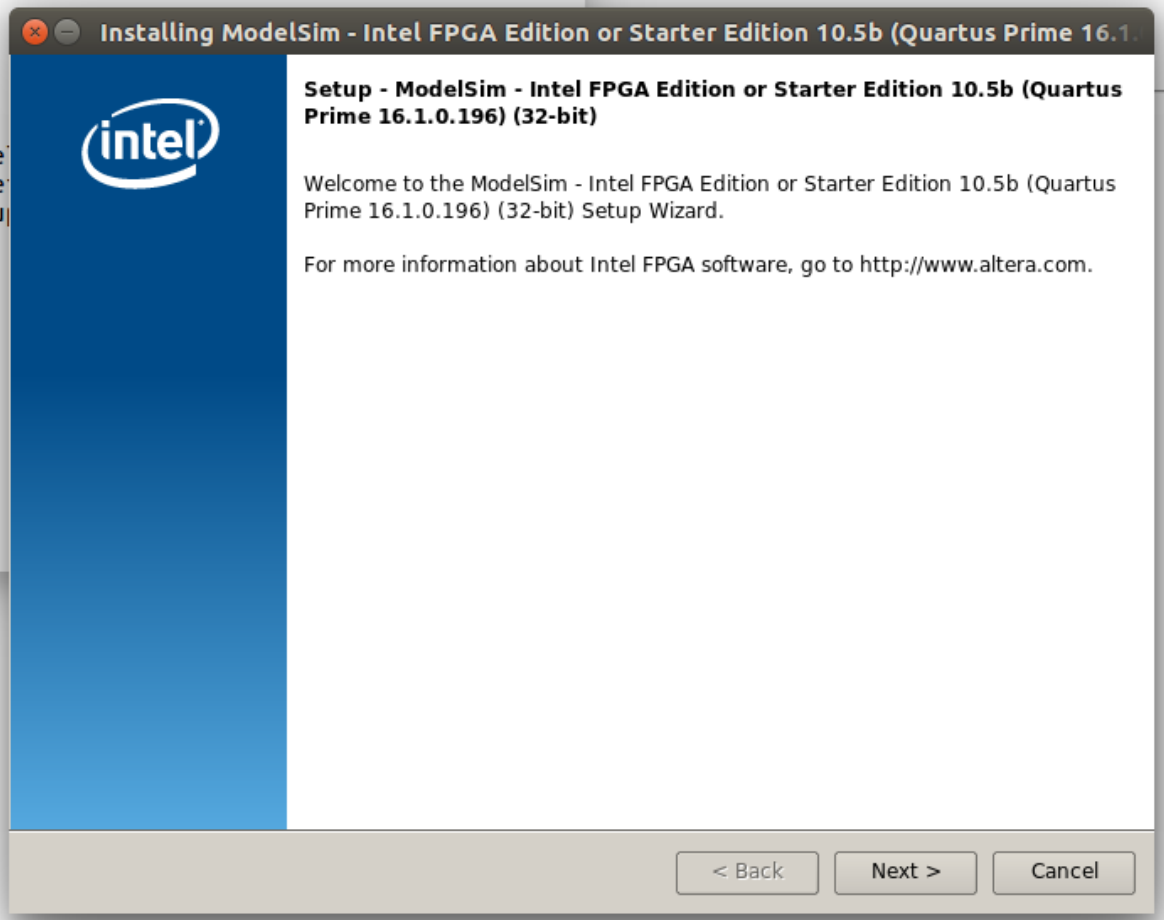
적절한 ModelSim 을 Intel 사이트에서 다운 받도록 한다.

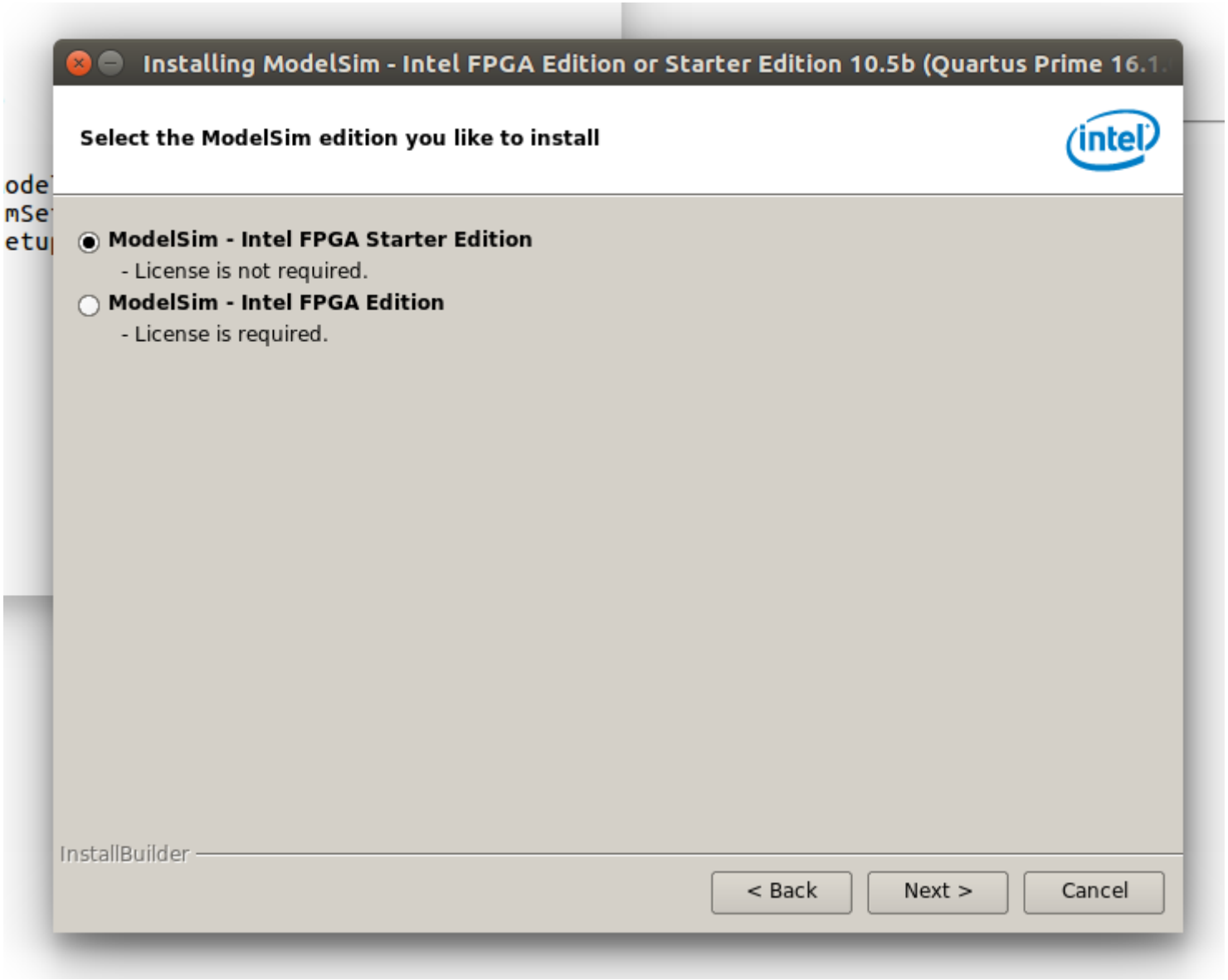


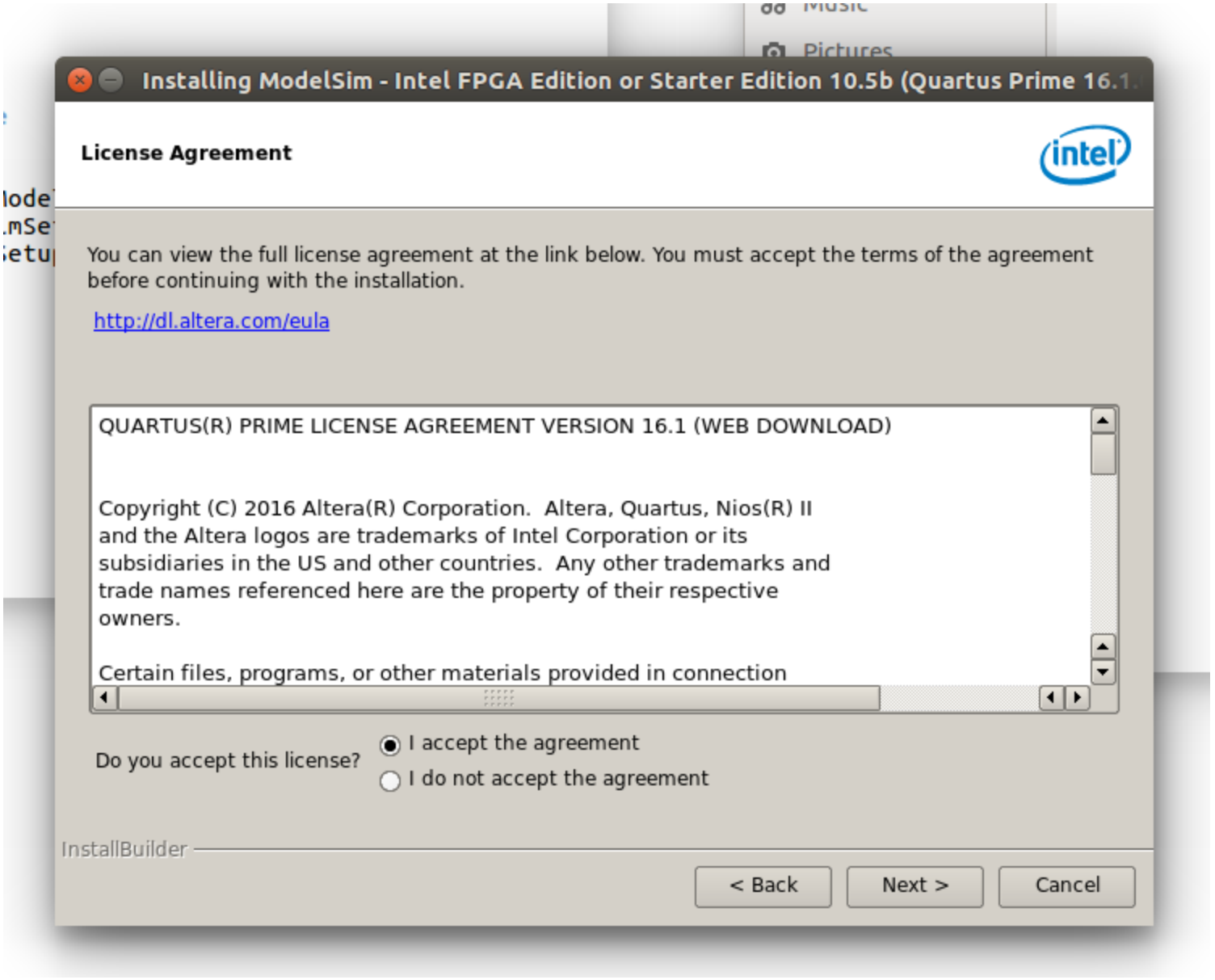
```
Pictures                        verilog
PlayOnLinux's virtual drives    Videos
Public                          vivado.jou
Qt                              vivado.log
qt_workspace                    vmware
self_drive                      workspace_v8
sw                              zynq_fpga
Templates                       zynq_test
test                            zynq_workspace
Texas_Instruments               zynq_zybo
ti
eskTop-System:~/sw/modelsim$ mv ~/Downloads/Mode
eskTop-System:~/sw/modelsim$ chmod +x ModelSimSe
eskTop-System:~/sw/modelsim$ sudo ./ModelSimSetu
for sdr:
```

ile for viruses.

n (1.1G) is too large for Google to scan for
nload this file?




Installing ModelSim - Intel FPGA Edition or Starter Edition 10.5b (Quartus Prime 16.1
Select the ModelSim edition you like to install
ModelSim - Intel FPGA Starter Edition
- License is not required.
ModelSim - Intel FPGA Edition
- License is required.
InstallBuilder
< Back
Next >
Cancel


Installing ModelSim - Intel FPGA Edition or Starter Edition 10.5b (Quartus Prime 16.1.
License Agreement
intel
You can view the full license agreement at the link below. You must accept the terms of the agreement before continuing with the installation.
http://dl.altera.com/eula
QUARTUS(R) PRIME LICENSE AGREEMENT VERSION 16.1 (WEB DOWNLOAD)
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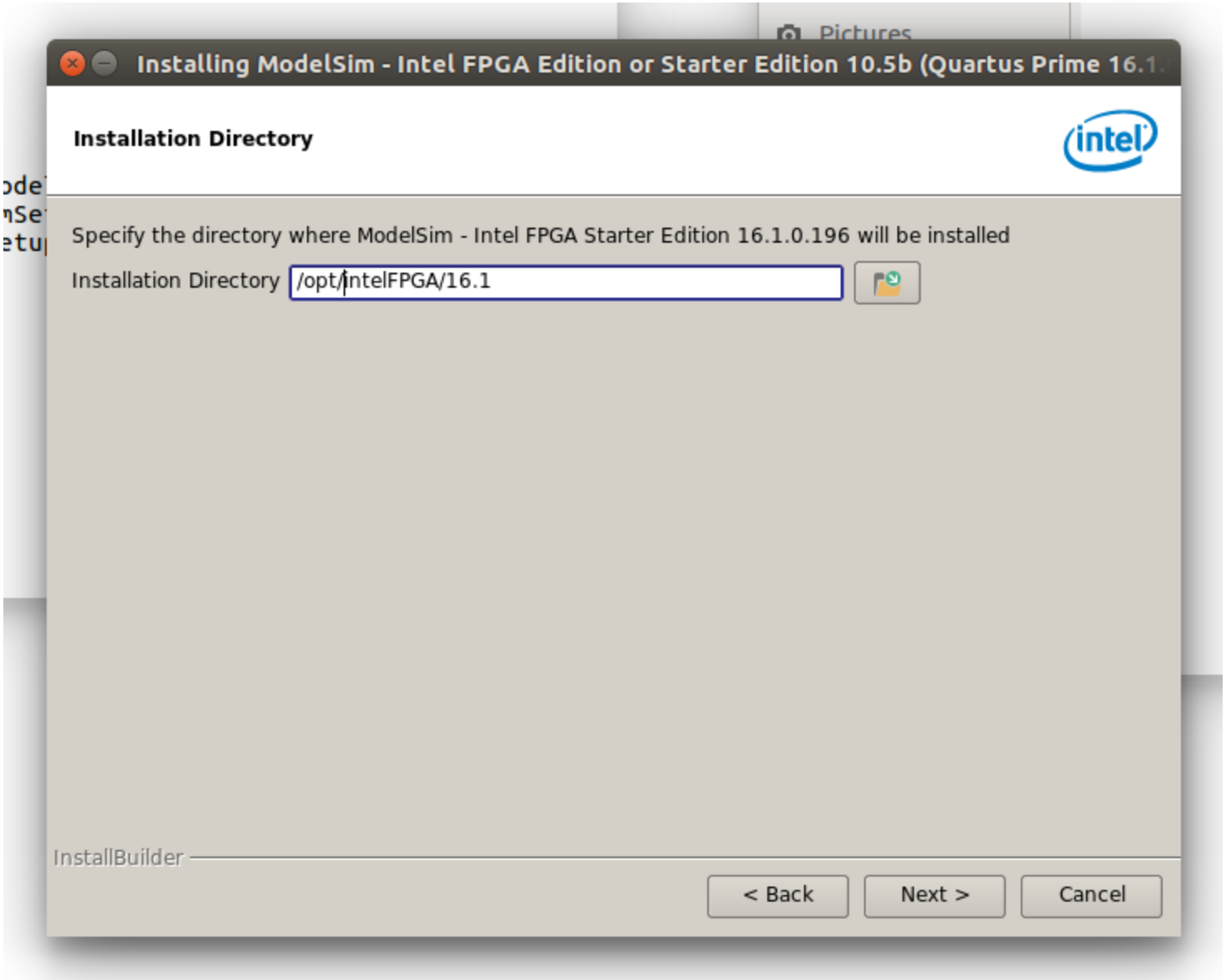
Certain files, programs, or other materials provided in connection
Do you accept this license?
I accept the agreement
I do not accept the agreement
InstallBuilder
< Back
Next >
Cancel


Pictures
Installing ModelSim - Intel FPGA Edition or Starter Edition 10.5b (Quartus Prime 16.1
Installation Directory
intel
Specify the directory where ModelSim - Intel FPGA Starter Edition 16.1.0.196 will be installed
Installation Directory
/opt/intelFPGA/16.1
InstallBuilder
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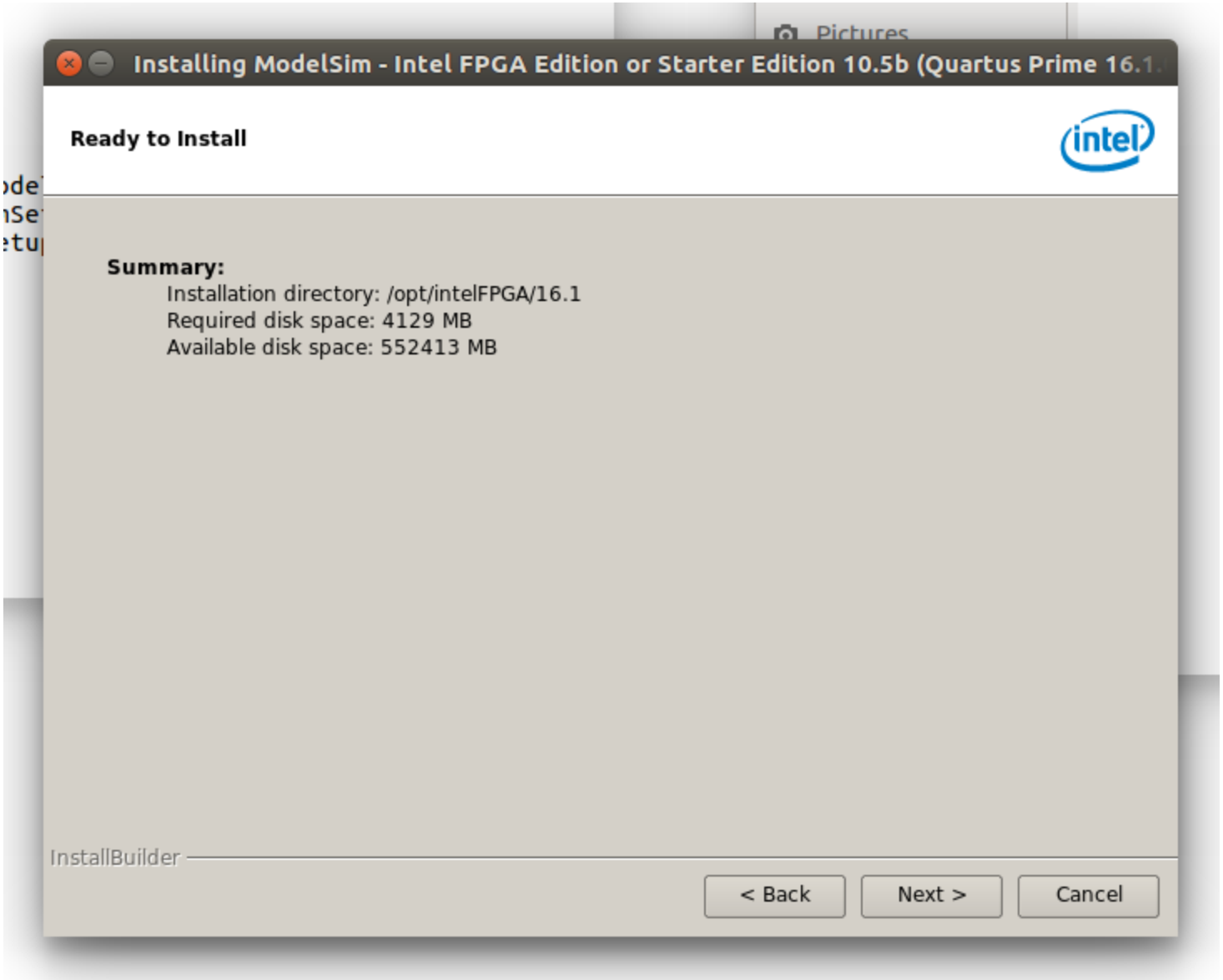
Cancel


Pictures
Installing ModelSim - Intel FPGA Edition or Starter Edition 10.5b (Quartus Prime 16.1
Ready to Install
intel
Summary:
Installation directory: /opt/intelFPGA/16.1
Required disk space: 4129 MB
Available disk space: 552413 MB
InstallBuilder
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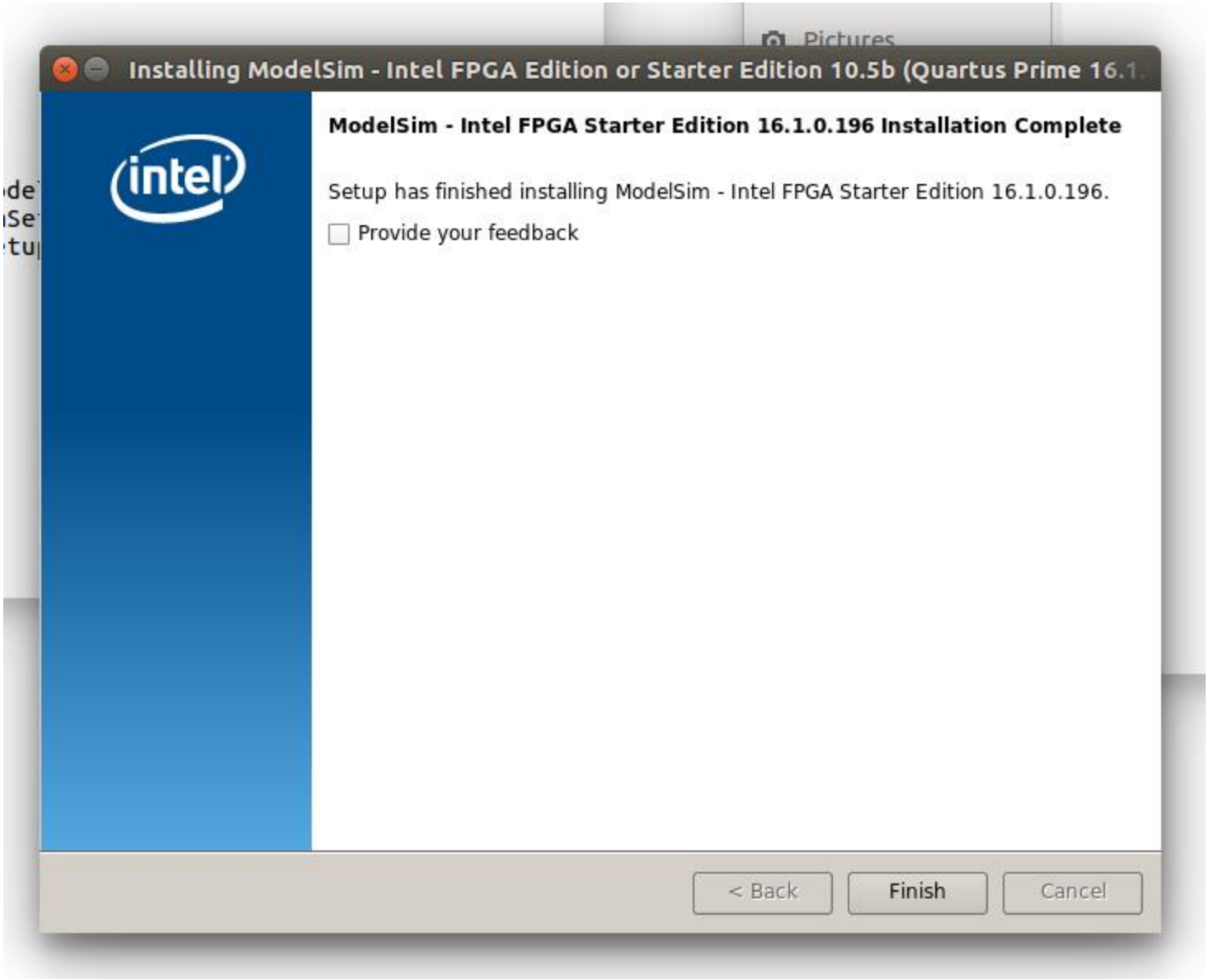
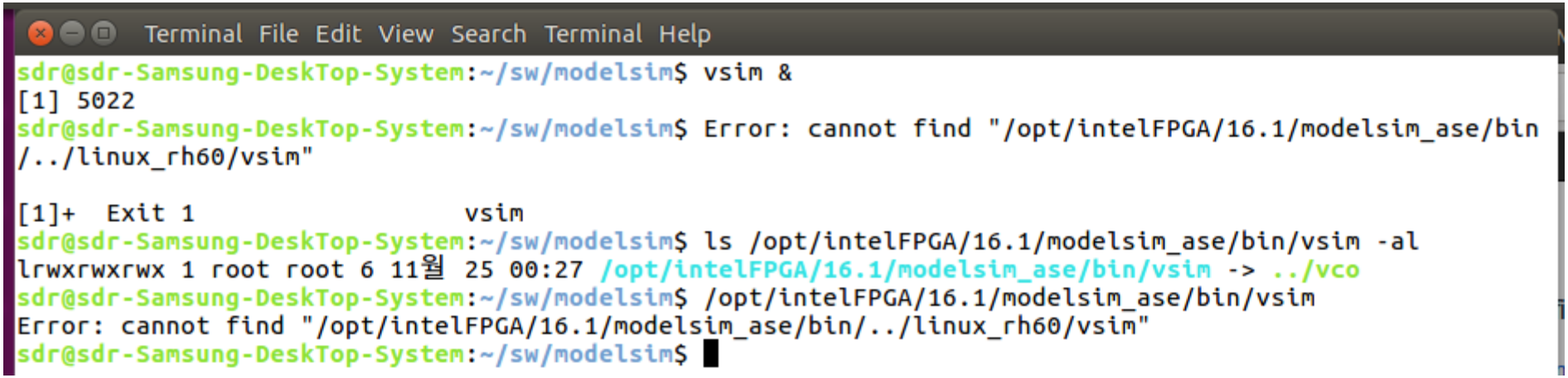
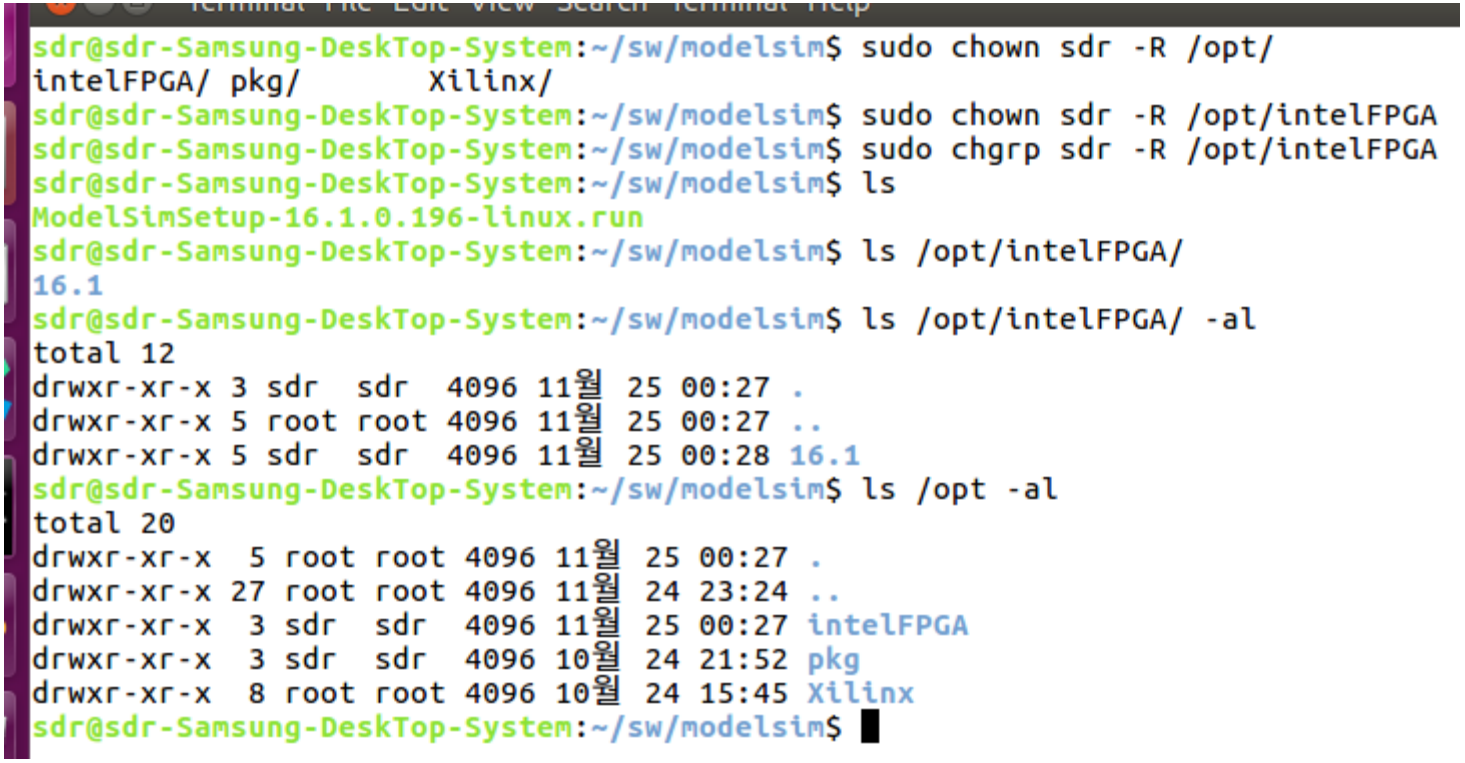
Cancel


Pictures
Installing ModelSim - Intel FPGA Edition or Starter Edition 10.5b (Quartus Prime 16.1.
ModelSim - Intel FPGA Starter Edition 16.1.0.196 Installation Complete
Setup has finished installing ModelSim - Intel FPGA Starter Edition 16.1.0.196.
Provide your feedback
< Back
Finish
Cancel

```
108 # enable programmable completion features (you don't need to enable
109 # this, if it's already enabled in /etc/bash.bashrc and /etc/profile
110 # sources /etc/bash.bashrc).
111 if ! shopt -oq posix; then
112   if [ -f /usr/share/bash-completion/bash_completion ]; then
113     . /usr/share/bash-completion/bash_completion
114   elif [ -f /etc/bash_completion ]; then
115     . /etc/bash_completion
116   fi
117 fi
118
119 # Enable Vivado 2015 & Petalinux 2015
120 #source /home/sdr/petalinux_zynq/petalinux-v2015.4-final/settings.sh
121 #source /opt/Xilinx/Vivado/2015.4/settings64.sh
122
123 # Enable Vivado 2017 & Petalinux 2017
124 source /opt/Xilinx/Vivado/2017.4/settings64.sh
125 source /opt/pkg/petalinux/settings.sh
126
127 # Enable QT5 QWT6
128 QT_PLUGIN_PATH="/usr/local/qwt-6.1.3/plugins:$QT_PLUGIN_PATH"
129 export QT_PLUGIN_PATH
130
131 # Enable LD_LIB_PATH
132 LD_LIBRARY_PATH=/usr/local/qwt-6.1.3/lib:$LD_LIBRARY_PATH
133 export LD_LIBRARY_PATH
134
135 # Enable Nvidia CUDA
136 export PATH=/usr/local/cuda-9.0/bin${PATH:+:${PATH}}
137 export LD_LIBRARY_PATH=/usr/local/cuda-9.0/lib64${LD_LIBRARY_PATH:+:${LD_LIBRARY_PATH}}
138
139 # Enable ModelSim
140 export PATH=$PATH:/opt/intelFPGA/16.1/modelsim_ase/bin
"~/.bashrc" [Modified] 140 lines --100%--                                    140,54
```


Terminal File Edit View Search Terminal Help
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ vsim &
[1] 5022
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ Error: cannot find "/opt/intelFPGA/16.1/modelsim_ase/bin/../linux_rh60/vsim"
[1]+ Exit 1 vsim
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ ls /opt/intelFPGA/16.1/modelsim_ase/bin/vsim -al
lrwxrwxrwx 1 root root 6 11월 25 00:27 /opt/intelFPGA/16.1/modelsim_ase/bin/vsim -> ../vco
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ /opt/intelFPGA/16.1/modelsim_ase/bin/vsim
Error: cannot find "/opt/intelFPGA/16.1/modelsim_ase/bin/../linux_rh60/vsim"
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$


Terminal File Edit View Search Terminal Help
194 if ["$umach" = "ia64"] && [-x "$dir/linux_ia64_gcc3/vsim"]; then
195 vco="linux_ia64_gcc3"
196 else
197 vco="linux_$umach"
198 fi
199 else
200 if [-x "$dir/linux_gcc3/vsim"] \
201 && [! -x "$dir/linux/vsim"]; then
202 vco="linux_gcc3"
203 else
204 case $utype in
205 2.4.[7-9]*) vco="linux" ;;
206 2.4.[1-9][0-9]*) vco="linux" ;;
207 2.[5-9]*) vco="linux" ;;
208 2.[1-9][0-9]*) vco="linux" ;;
209 3.[0-9]*) vco="linux" ;;
210 *) vco="linux_rh60" ;;
211 esac
212 if [! -x "$dir/$vco/vsim"]; then
213 if [-x "$dir/linuxle/vsim"]; then
214 vco="linuxle"
215 elif [-x "$dir/linuxpe/vsim"]; then
216 vco="linuxpe"
217 fi
218 fi
219 fi
220 fi
221 ;;
222 CYGWIN_NT*)
223 if [-x "$dir/win32/vsim"]; then
224 vco="win32"
225 elif [-x "$dir/win32pe/vsim"]; then
226 vco="win32pe"
:%s/linux_rh60/linux/g

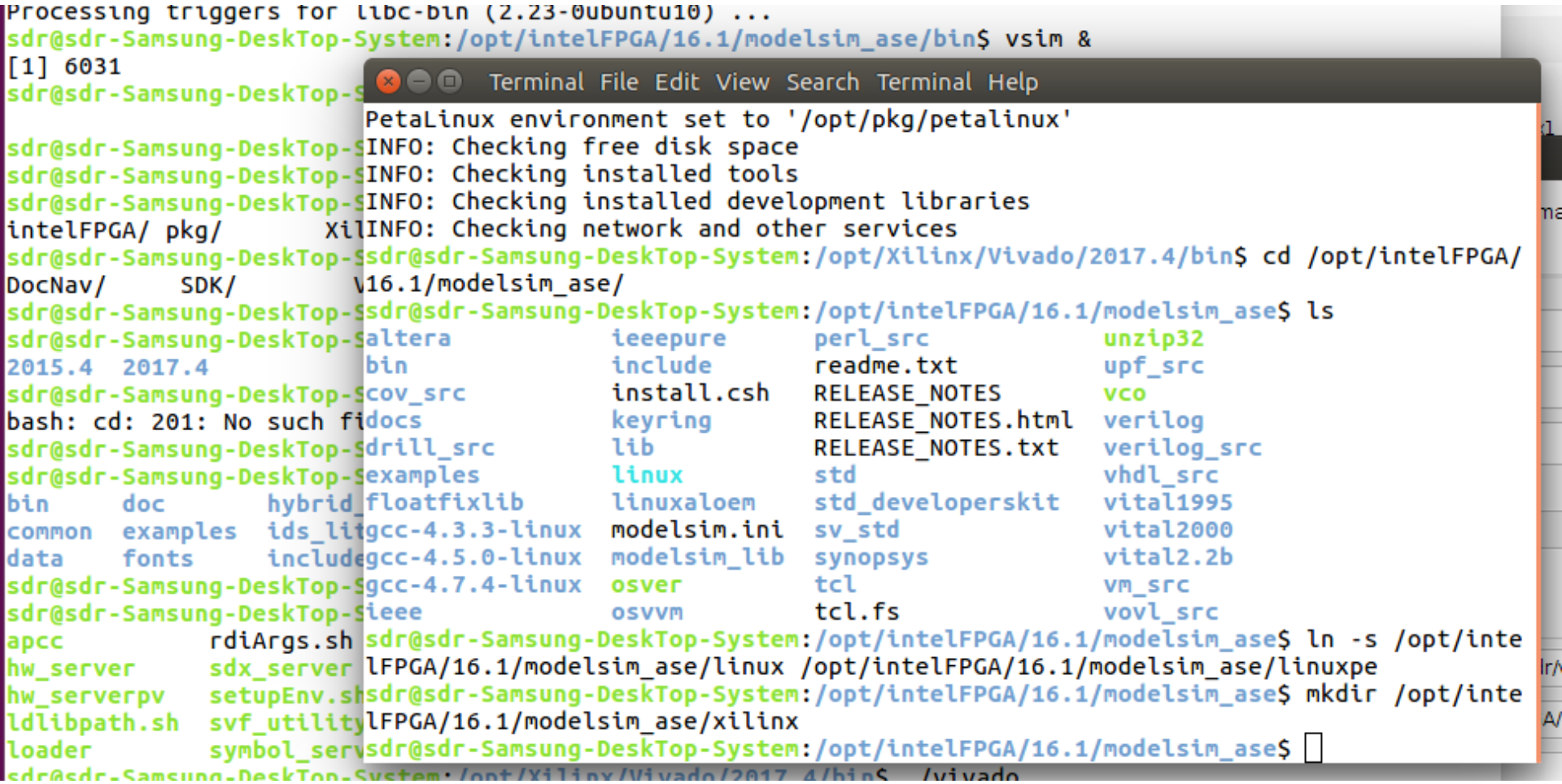

sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ sudo chown sdr -R /opt/
intelFPGA/ pkg/ Xilinx/
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ sudo chown sdr -R /opt/intelFPGA
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ sudo chgrp sdr -R /opt/intelFPGA
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ ls
ModelSimSetup-16.1.0.196-linux.run
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ ls /opt/intelFPGA/
16.1
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ ls /opt/intelFPGA/ -al
total 12
drwxr-xr-x 3 sdr sdr 4096 11월 25 00:27 .
drwxr-xr-x 5 root root 4096 11월 25 00:27 ..
drwxr-xr-x 5 sdr sdr 4096 11월 25 00:28 16.1
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$ ls /opt -al
total 20
drwxr-xr-x 5 root root 4096 11월 25 00:27 .
drwxr-xr-x 27 root root 4096 11월 24 23:24 ..
drwxr-xr-x 3 sdr sdr 4096 11월 25 00:27 intelFPGA
drwxr-xr-x 3 sdr sdr 4096 10월 24 21:52 pkg
drwxr-xr-x 8 root root 4096 10월 24 15:45 Xilinx
sdr@sdr-Samsung-DeskTop-System:~/sw/modelsim$

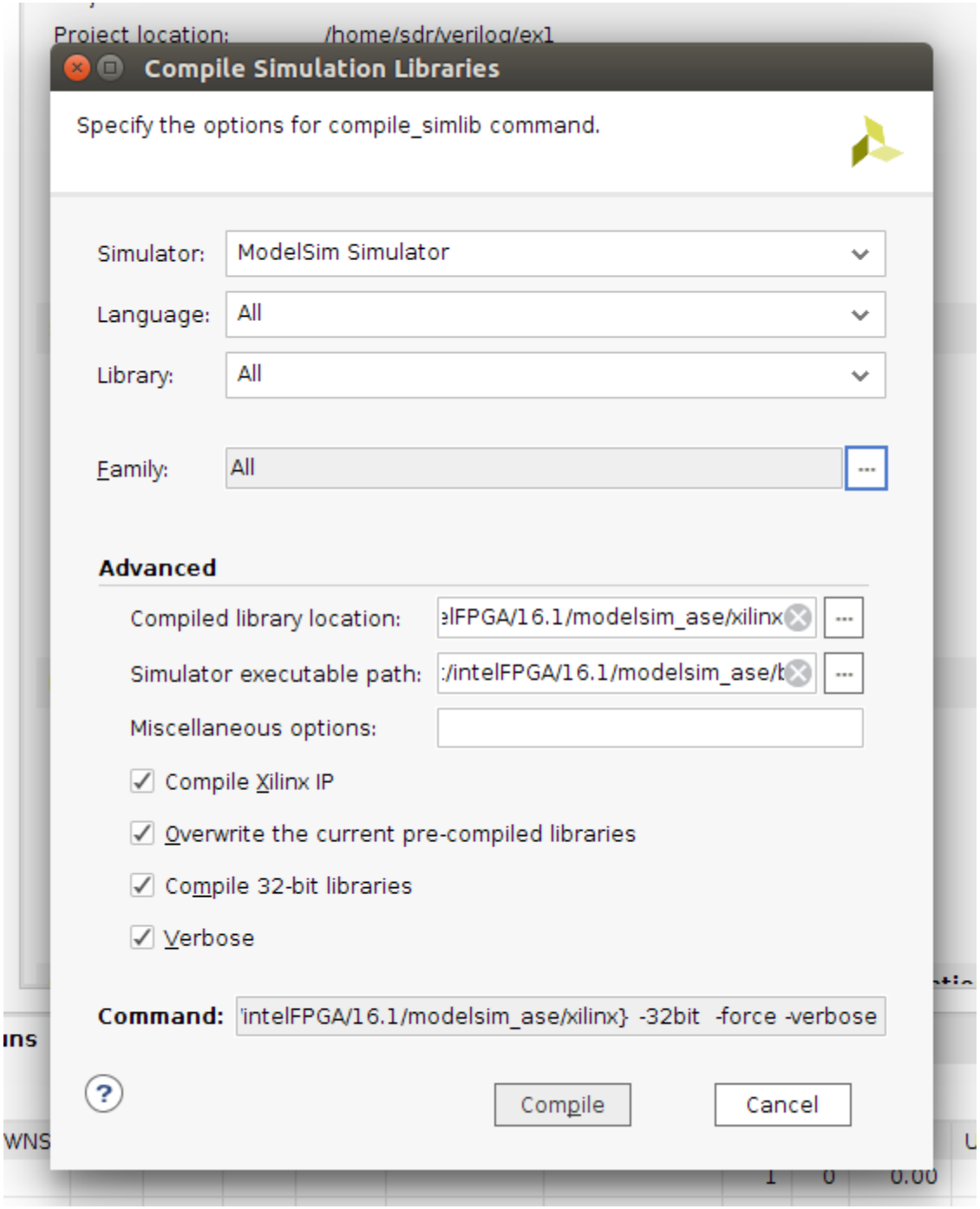
```
 1 #!/bin/sh
 2 #
 3 #Copyright 1991-2016 Mentor Graphics Corporation
 4 #
 5 #All Rights Reserved.
 6 #
 7 #THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION WHICH IS THE PROPERTY OF
 8 #MENTOR GRAPHICS CORPORATION OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
 9 #
10
11 # MTI_VCO_MODE environment variable may be set to "32" or "64"
12 # to force selection of 32-bit or 64-bit platform directory for executables.
13 mode=${MTI_VCO_MODE:-"32"}
14
15 PATH="/bin:$PATH"
16
17 arg0="$0"
18 cmd=`basename "$arg0"`
19
20 uname=`uname`
21 utype=`uname -r`
22 umach=`uname -m`
23
24 case $uname in
25   AIX)
26     islink=-L
27     ;;
28   CYGWIN_NT*)
29     arg0=`dirname "$arg0"`
-- INSERT -- W10: Warning: Changing a readonly file                    13,25
```

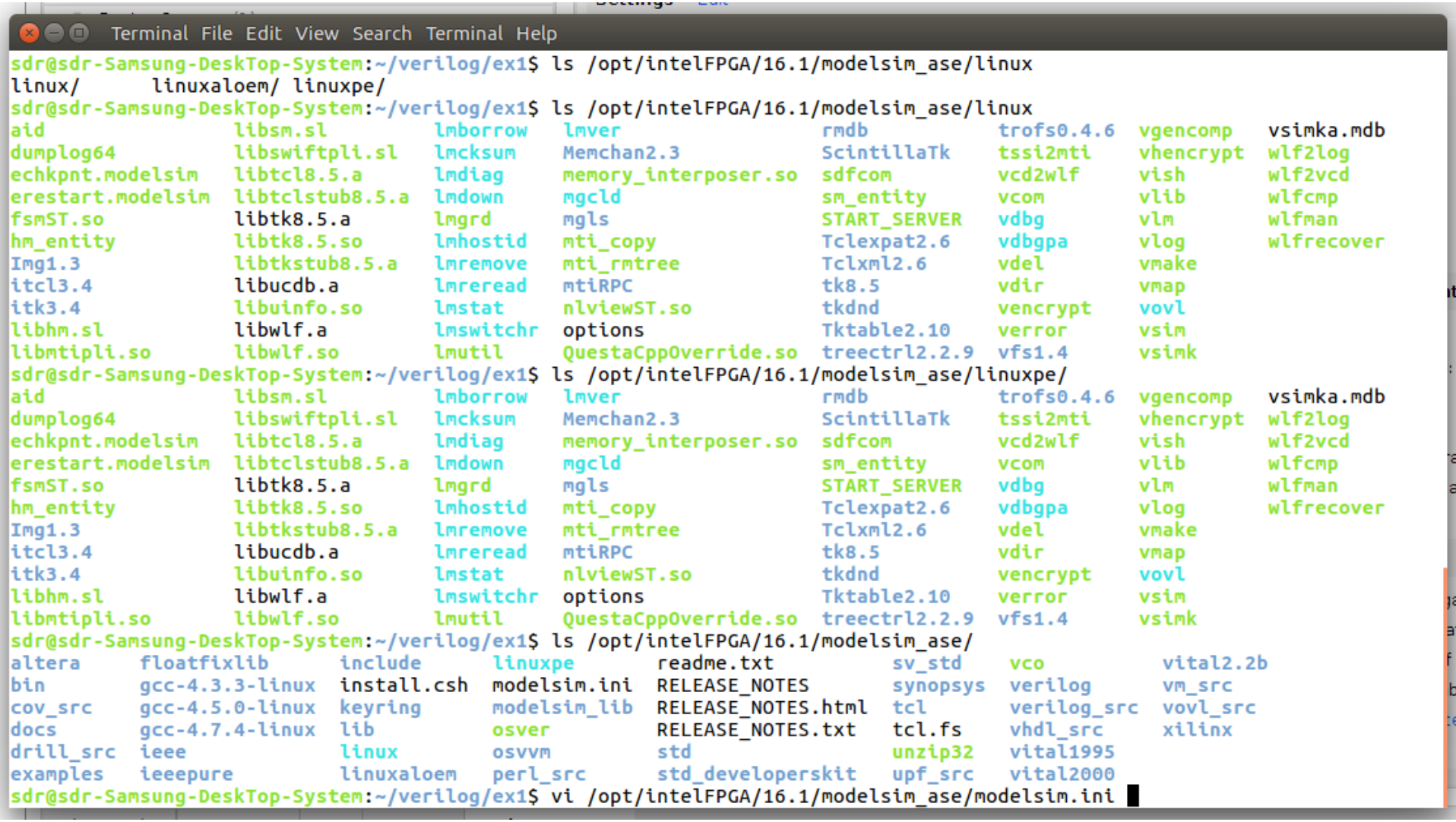
```
 36   *)
 37     islink=-h
 38     ;;
 39 esac
 40
 41 while [ $islink "$arg0" ] ; do
 42   x=`/bin/ls -ld "$arg0"`
 43   x=`expr "$x" : '.* \(.*\)'`
 44   case "$x" in
 45     /*) arg0="$x"                ;;
 46     *)  arg0="`dirname ""$arg0""`/$x" ;;
 47   esac
 48 done
 49
 50 dir=`dirname "$arg0"`
 51 export LD_LIBRARY_PATH=${dir}/lib32
 52
 53 vco=${uname}${utype}
 54 case $vco in
 55   SunOS4*)
 56     echo "Error: $cmd is not supported on ${uname} ${utype}"
 57     exit 1
 58     ;;
 59   SunOS5.5*)
 60     echo "Error: $cmd is not supported on ${uname} ${utype}"
 61     exit 1
 62     ;;
 63   SunOS5.6*)
 64     echo "Error: $cmd is not supported on ${uname} ${utype}"
-- INSERT --
```

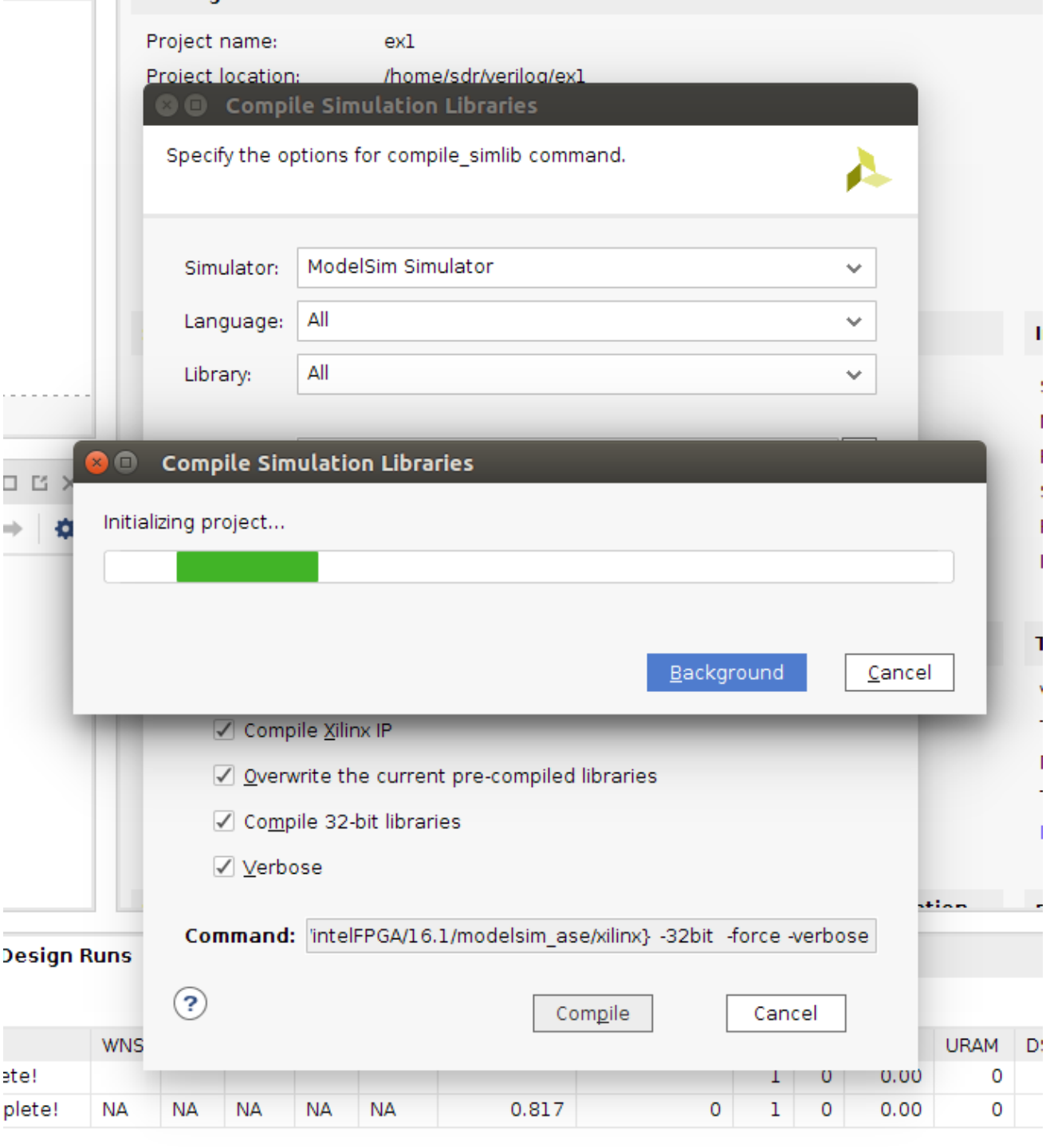
```
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/bin$ sudo dpkg --add-architecture i386
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/bin$ sudo apt-get update
Ign:1 http://developer.download.nvidia.com/compute/cuda/repos/ubuntu1604/x86_64  InRelease
Hit:2 http://developer.download.nvidia.com/compute/cuda/repos/ubuntu1604/x86_64  Release
Get:3 http://developer.download.nvidia.com/compute/cuda/repos/ubuntu1604/x86_64  Release.gpg [801 B]
Ign:3 http://developer.download.nvidia.com/compute/cuda/repos/ubuntu1604/x86_64  Release.gpg
Hit:4 http://ppa.launchpad.net/maarten-baert/simplescreenrecorder/ubuntu xenial InRelease
Get:5 http://security.ubuntu.com/ubuntu xenial-security InRelease [107 kB]
Hit:6 http://kaist.archive.ubuntu.com/ubuntu xenial InRelease
Get:7 http://kaist.archive.ubuntu.com/ubuntu xenial-updates InRelease [109 kB]
Hit:8 http://deb.playonlinux.com precise InRelease
Hit:9 http://ppa.launchpad.net/soylent-tv/screenstudio/ubuntu xenial InRelease
Get:10 http://security.ubuntu.com/ubuntu xenial-security/main amd64 DEP-11 Metadata [67.7 kB]
Get:11 http://kaist.archive.ubuntu.com/ubuntu xenial-backports InRelease [107 kB]
Get:12 http://security.ubuntu.com/ubuntu xenial-security/main DEP-11 64x64 Icons [72.2 kB]
Get:13 http://security.ubuntu.com/ubuntu xenial-security/universe amd64 DEP-11 Metadata [108 kB]
Get:14 http://security.ubuntu.com/ubuntu xenial-security/universe DEP-11 64x64 Icons [150 kB]
Get:15 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/main amd64 Packages [884 kB]
Get:16 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/main i386 Packages [786 kB]
Get:17 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/main amd64 DEP-11 Metadata [320 kB]
Get:18 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/main DEP-11 64x64 Icons [227 kB]
Get:19 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/universe amd64 Packages [706 kB]
Get:20 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/universe i386 Packages [647 kB]
Get:21 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/universe amd64 DEP-11 Metadata [247 kB]
Get:22 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/universe DEP-11 64x64 Icons [333 kB]
Get:23 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/multiverse amd64 DEP-11 Metadata [5,960 B
]
Get:24 http://kaist.archive.ubuntu.com/ubuntu xenial-updates/multiverse DEP-11 64x64 Icons [14.3 kB]
Get:25 http://kaist.archive.ubuntu.com/ubuntu xenial-backports/main amd64 DEP-11 Metadata [3,328 B]
Get:26 http://kaist.archive.ubuntu.com/ubuntu xenial-backports/universe amd64 DEP-11 Metadata [5,104 B
]
Fetched 4,900 kB in 4s (1,032 kB/s)
AppStream cache update completed, but some metadata was ignored due to errors.
Reading package lists... Done
W: GPG error: http://developer.download.nvidia.com/compute/cuda/repos/ubuntu1604/x86_64  Release: The
following signatures couldn't be verified because the public key is not available: NO_PUBKEY F60F4B3D7
FA2AF80
W: The repository 'http://developer.download.nvidia.com/compute/cuda/repos/ubuntu1604/x86_64  Release'
 is not signed.
N: Data from such a repository can't be authenticated and is therefore potentially dangerous to use.
N: See apt-secure(8) manpage for repository creation and user configuration details.
```

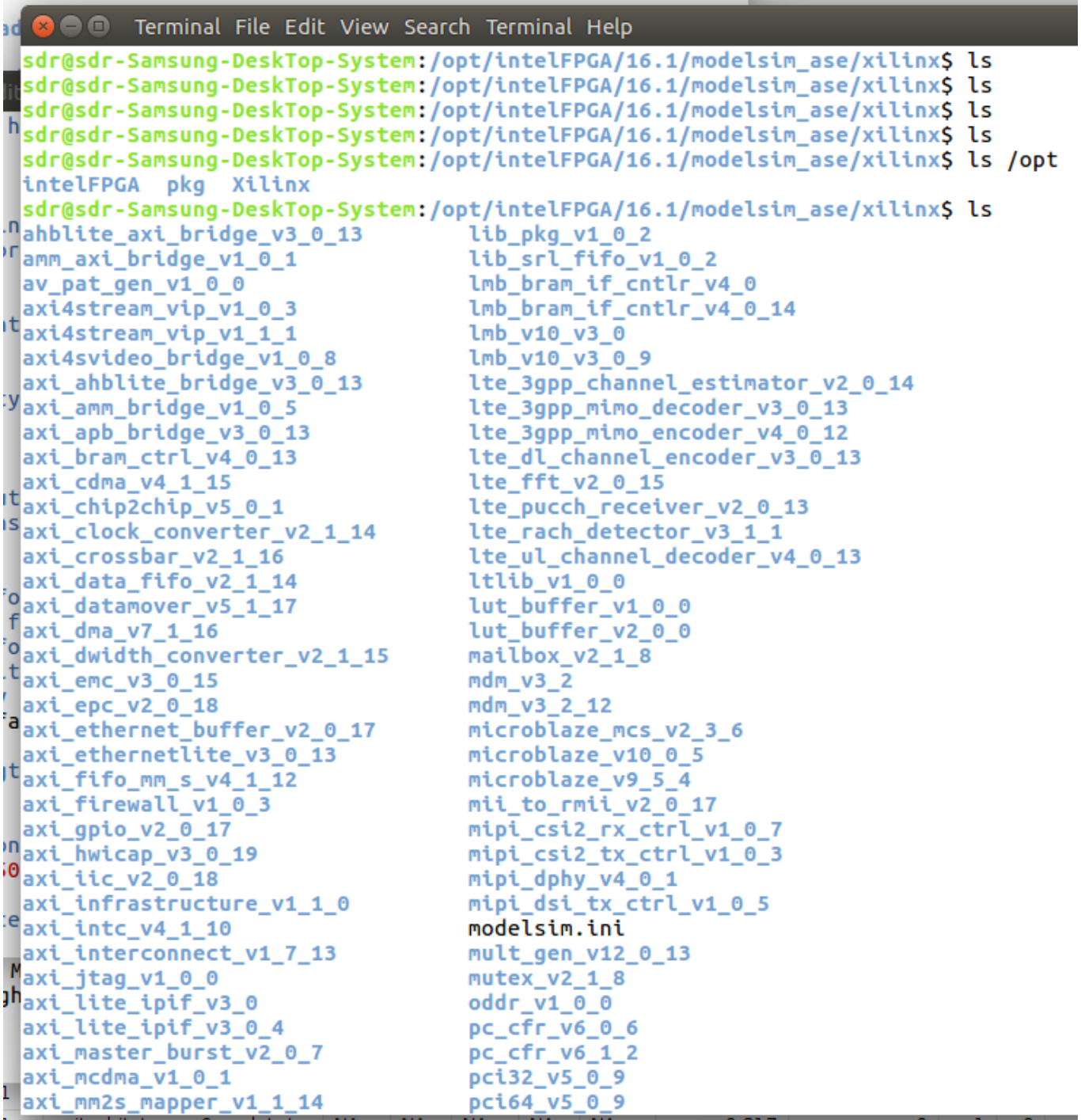
```
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/bin$ sudo apt-get install libxft2:i386
 libxext6:i386 libncurses5:i386
Reading package lists... Done
Building dependency tree
Reading state information... Done
libncurses5:i386 is already the newest version (6.0+20160213-1ubuntu1).
libxext6:i386 is already the newest version (2:1.3.3-1).
libxext6:i386 set to manually installed.
The following packages were automatically installed and are no longer required:
  linux-headers-4.15.0-33 linux-headers-4.15.0-33-generic linux-image-4.15.0-33-generic
  linux-modules-4.15.0-33-generic
Use 'sudo apt autoremove' to remove them.
The following NEW packages will be installed:
  libxft2:i386
0 upgraded, 1 newly installed, 0 to remove and 241 not upgraded.
Need to get 35.5 kB of archives.
After this operation, 127 kB of additional disk space will be used.
Do you want to continue? [Y/n] y
Get:1 http://kaist.archive.ubuntu.com/ubuntu xenial/main i386 libxft2 i386 2.3.2-1 [35.5 kB]
Fetched 35.5 kB in 1s (31.9 kB/s)
Selecting previously unselected package libxft2:i386.
(Reading database ... 295592 files and directories currently installed.)
Preparing to unpack .../libxft2_2.3.2-1_i386.deb ...
Unpacking libxft2:i386 (2.3.2-1) ...
Setting up libxft2:i386 (2.3.2-1) ...
Processing triggers for libc-bin (2.23-0ubuntu10) ...
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/bin$
```

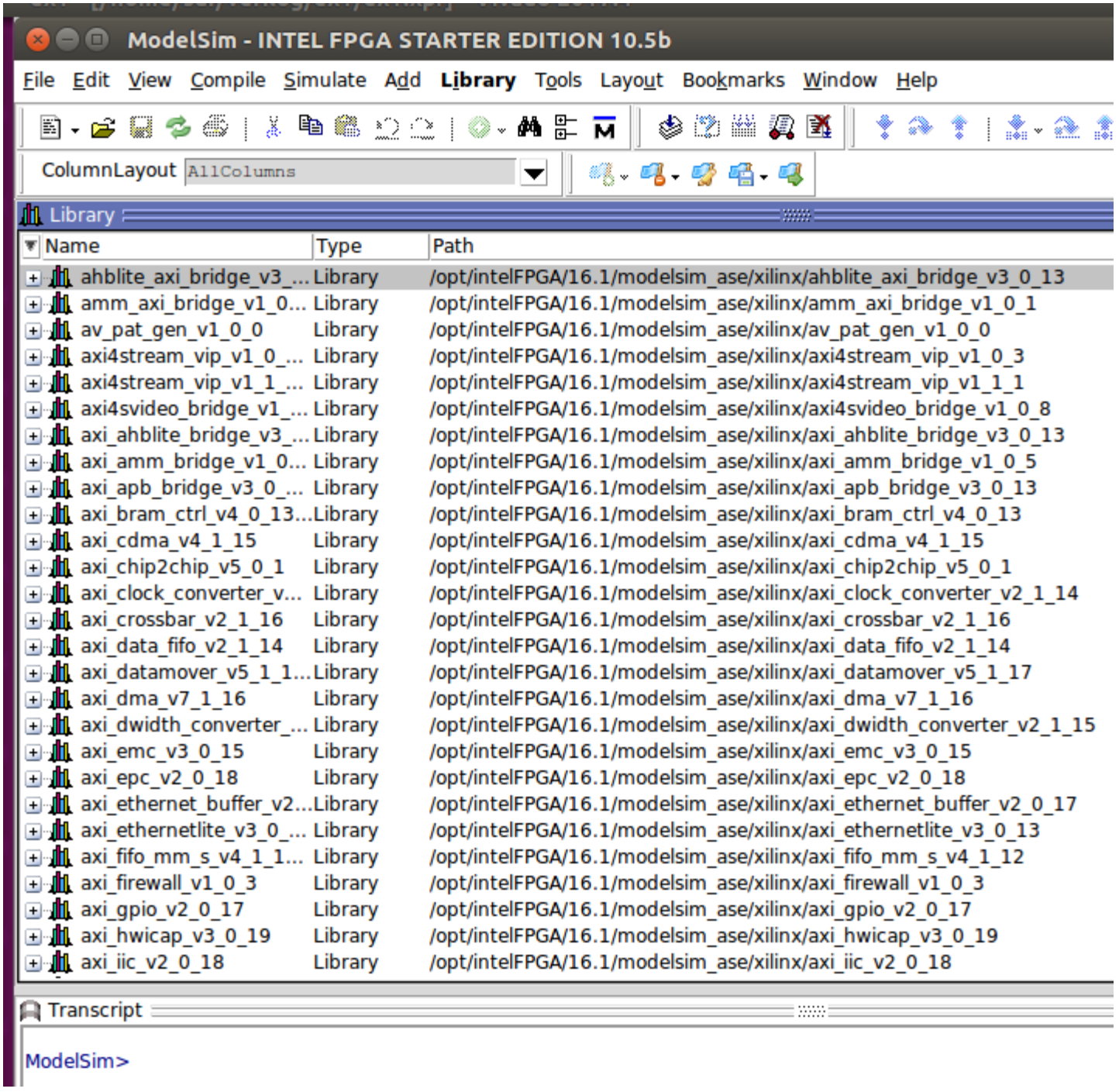

Processing triggers for libc-bin (2.23-0ubuntu10) ...
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/bin$ vsim &
[1] 6031
intelFPGA/ pkg/
DocNav/ SDK/
2015.4 2017.4
bash: cd: 201: No such fi
bin doc hybrid_
common examples ids_lit
data fonts include
apcc rdiArgs.sh
hw_server sdx_server
hw_serverpv setupEnv.sh
ldlibpath.sh svf_utility
loader symbol_serv
Terminal File Edit View Search Terminal Help
PetaLinux environment set to '/opt/pkg/petalinux'
INFO: Checking free disk space
INFO: Checking installed tools
INFO: Checking installed development libraries
INFO: Checking network and other services
sdr@sdr-Samsung-DeskTop-System:/opt/Xilinx/Vivado/2017.4/bin$ cd /opt/intelFPGA/16.1/modelsim_ase/
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase$ ls
altera ieeepure perl_src unzip32
bin include readme.txt upf_src
cov_src install.csh RELEASE_NOTES vco
docs keyring RELEASE_NOTES.html verilog
drill_src lib RELEASE_NOTES.txt verilog_src
examples linux std vhdl_src
floatfixlib linuxaloem std_developerskit vital1995
gcc-4.3.3-linux modelsim.ini sv_std vital2000
gcc-4.5.0-linux modelsim_lib synopsys vital2.2b
gcc-4.7.4-linux osver tcl vm_src
ieee osvvm tcl.fs vovl_src
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase$ ln -s /opt/intelFPGA/16.1/modelsim_ase/linux /opt/intelFPGA/16.1/modelsim_ase/linuxpe
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase$ mkdir /opt/intelFPGA/16.1/modelsim_ase/xilinx
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase$

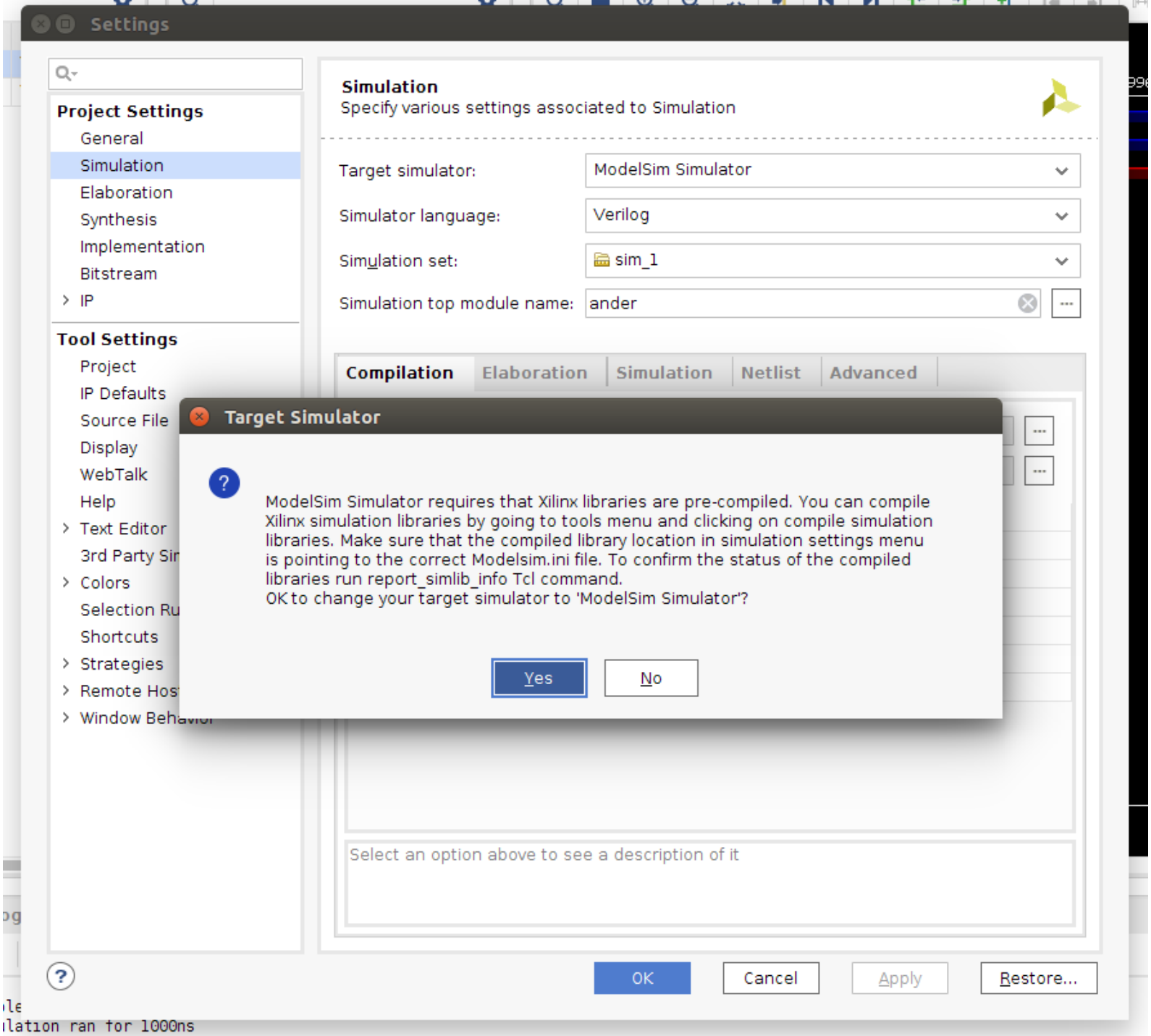

Project location: /home/sdr/verilog/ex1
Compile Simulation Libraries
Specify the options for compile_simlib command.
Simulator: ModelSim Simulator
Language: All
Library: All
Family: All
Advanced
Compiled library location: elFPGA/16.1/modelsim_ase/xilinx
Simulator executable path: :/intelFPGA/16.1/modelsim_ase/b
Miscellaneous options:
Compile Xilinx IP
Overwrite the current pre-compiled libraries
Compile 32-bit libraries
Verbose
Command: 'intelFPGA/16.1/modelsim_ase/xilinx} -32bit -force -verbose
Compile
Cancel


Terminal File Edit View Search Terminal Help
sdr@sdr-Samsung-DeskTop-System:~/verilog/ex1$ ls /opt/intelFPGA/16.1/modelsim_ase/linux
linux/ linuxaloem/ linuxpe/
sdr@sdr-Samsung-DeskTop-System:~/verilog/ex1$ ls /opt/intelFPGA/16.1/modelsim_ase/linux
aid libsm.sl lmborrow lmver rmdb trofs0.4.6 vgencomp vsimka.mdb
dumplog64 libswiftpli.sl lmcksum Memchan2.3 ScintillaTk tssi2mti vhencrypt wlf2log
echkpnt.modelsim libtcl8.5.a lmdiag memory_interposer.so sdfcom vcd2wlf vish wlf2vcd
erestart.modelsim libtclstub8.5.a lmdown mgcld sm_entity vcom vlib wlfcmp
fsmST.so libtk8.5.a lmgrd mgls START_SERVER vdbg vlm wlfman
hm_entity libtk8.5.so lmhostid mti_copy Tclexpat2.6 vdbgpa vlog wlfrecover
Img1.3 libtkstub8.5.a lmremove mti_rmtree Tclxml2.6 vdel vmake
itcl3.4 libucdb.a lmreread mtiRPC tk8.5 vdir vmap
itk3.4 libuinfo.so lmstat nlviewST.so tkdnd vencrypt vovl
libhm.sl libwlf.a lmswitchr options Tktable2.10 verror vsim
libmtipli.so libwlf.so lmutil QuestaCppOverride.so treectrl2.2.9 vfs1.4 vsimk
sdr@sdr-Samsung-DeskTop-System:~/verilog/ex1$ ls /opt/intelFPGA/16.1/modelsim_ase/linuxpe/
aid libsm.sl lmborrow lmver rmdb trofs0.4.6 vgencomp vsimka.mdb
dumplog64 libswiftpli.sl lmcksum Memchan2.3 ScintillaTk tssi2mti vhencrypt wlf2log
echkpnt.modelsim libtcl8.5.a lmdiag memory_interposer.so sdfcom vcd2wlf vish wlf2vcd
erestart.modelsim libtclstub8.5.a lmdown mgcld sm_entity vcom vlib wlfcmp
fsmST.so libtk8.5.a lmgrd mgls START_SERVER vdbg vlm wlfman
hm_entity libtk8.5.so lmhostid mti_copy Tclexpat2.6 vdbgpa vlog wlfrecover
Img1.3 libtkstub8.5.a lmremove mti_rmtree Tclxml2.6 vdel vmake
itcl3.4 libucdb.a lmreread mtiRPC tk8.5 vdir vmap
itk3.4 libuinfo.so lmstat nlviewST.so tkdnd vencrypt vovl
libhm.sl libwlf.a lmswitchr options Tktable2.10 verror vsim
libmtipli.so libwlf.so lmutil QuestaCppOverride.so treectrl2.2.9 vfs1.4 vsimk
sdr@sdr-Samsung-DeskTop-System:~/verilog/ex1$ ls /opt/intelFPGA/16.1/modelsim_ase/
altera floatfixlib include linuxpe readme.txt sv_std vco vital2.2b
bin gcc-4.3.3-linux install.csh modelsim.ini RELEASE_NOTES synopsys verilog vm_src
cov_src gcc-4.5.0-linux keyring modelsim_lib RELEASE_NOTES.html tcl verilog_src vovl_src
docs gcc-4.7.4-linux lib osver RELEASE_NOTES.txt tcl.fs vhdl_src xilinx
drill_src ieee linux osvvm std unzip32 vital1995
examples ieeepure linuxaloem perl_src std_developerskit upf_src vital2000
sdr@sdr-Samsung-DeskTop-System:~/verilog/ex1$ vi /opt/intelFPGA/16.1/modelsim_ase/modelsim.ini

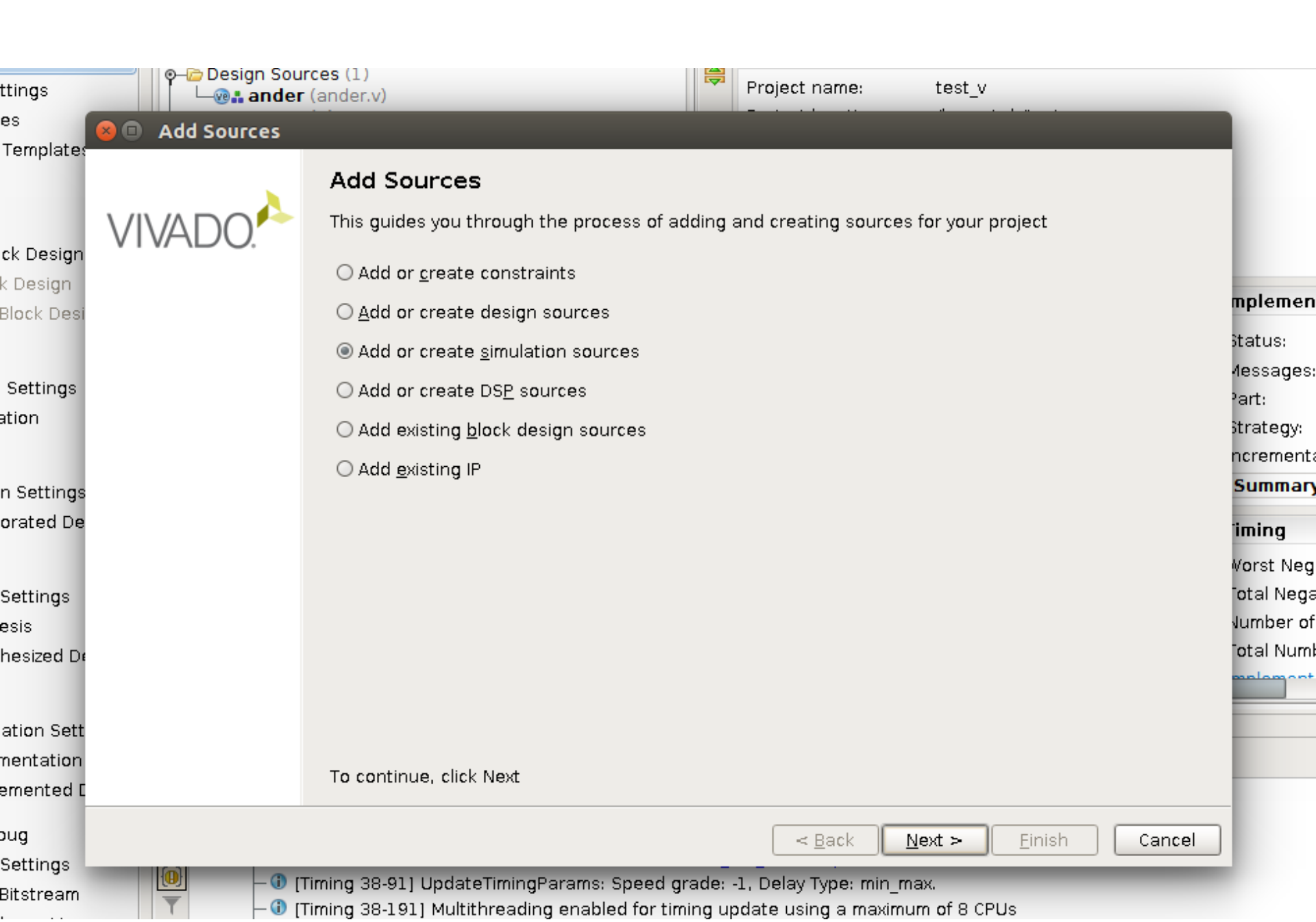

Project name: ex1
Project location: /home/sdr/verilog/ex1
Compile Simulation Libraries
Specify the options for compile_simlib command.
Simulator: ModelSim Simulator
Language: All
Library: All
Compile Simulation Libraries
Initializing project...
Background
Cancel
Compile Xilinx IP
Overwrite the current pre-compiled libraries
Compile 32-bit libraries
Verbose
Command: 'intelFPGA/16.1/modelsim_ase/xilinx} -32bit -force -verbose
Compile
Cancel
Design Runs
WNS
URAM
plete! NA NA NA NA NA 0.817 0 1 0 0.00 0

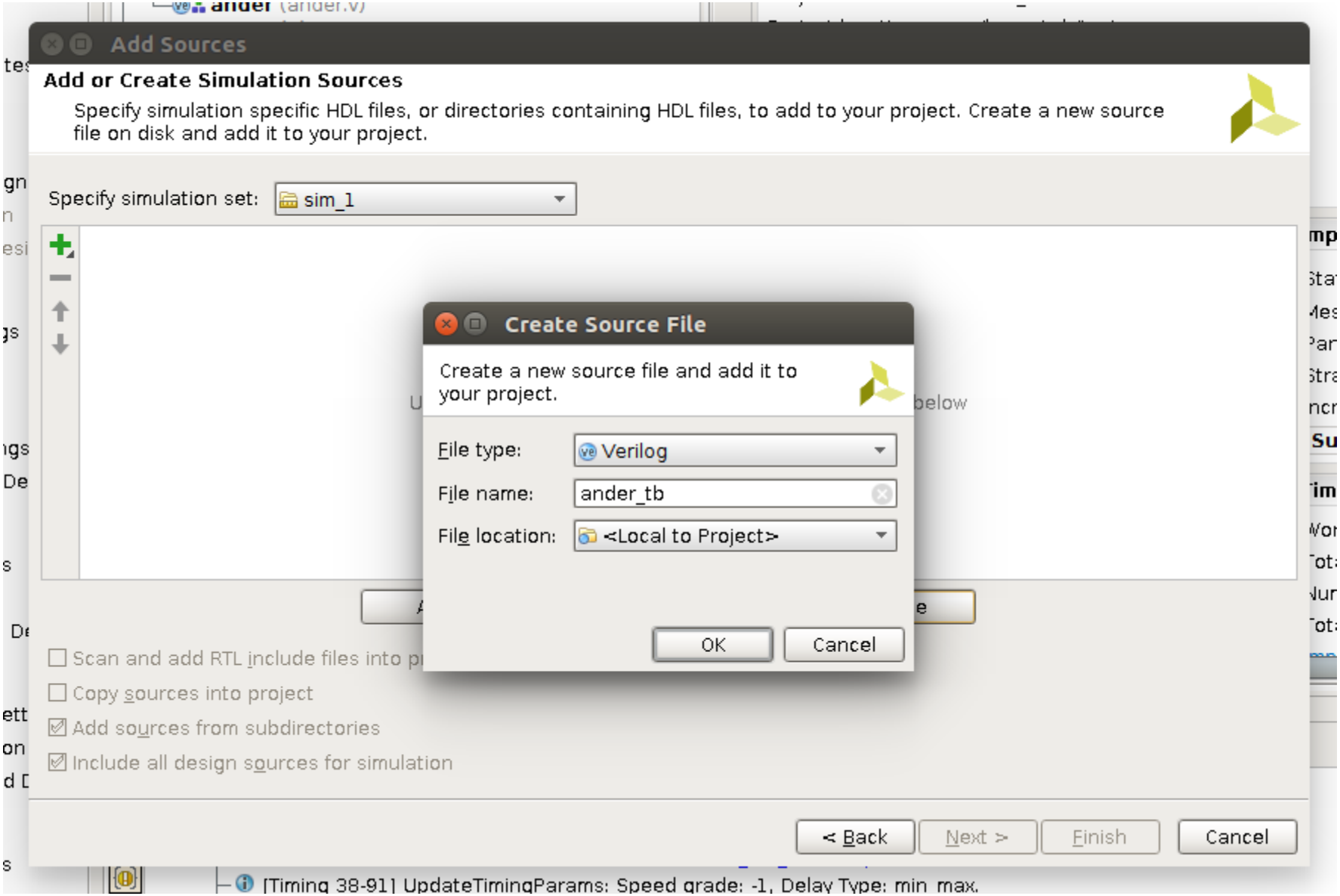

Terminal File Edit View Search Terminal Help
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/xilinx$ ls
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/xilinx$ ls
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/xilinx$ ls
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/xilinx$ ls
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/xilinx$ ls /opt
intelFPGA pkg Xilinx
sdr@sdr-Samsung-DeskTop-System:/opt/intelFPGA/16.1/modelsim_ase/xilinx$ ls
ahblite_axi_bridge_v3_0_13
amm_axi_bridge_v1_0_1
av_pat_gen_v1_0_0
axi4stream_vip_v1_0_3
axi4stream_vip_v1_1_1
axi4svideo_bridge_v1_0_8
axi_ahblite_bridge_v3_0_13
axi_amm_bridge_v1_0_5
axi_apb_bridge_v3_0_13
axi_bram_ctrl_v4_0_13
axi_cdma_v4_1_15
axi_chip2chip_v5_0_1
axi_clock_converter_v2_1_14
axi_crossbar_v2_1_16
axi_data_fifo_v2_1_14
axi_datamover_v5_1_17
axi_dma_v7_1_16
axi_dwidth_converter_v2_1_15
axi_emc_v3_0_15
axi_epc_v2_0_18
axi_ethernet_buffer_v2_0_17
axi_ethernetlite_v3_0_13
axi_fifo_mm_s_v4_1_12
axi_firewall_v1_0_3
axi_gpio_v2_0_17
axi_hwicap_v3_0_19
axi_iic_v2_0_18
axi_infrastructure_v1_1_0
axi_intc_v4_1_10
axi_interconnect_v1_7_13
axi_jtag_v1_0_0
axi_lite_ipif_v3_0
axi_lite_ipif_v3_0_4
axi_master_burst_v2_0_7
axi_mcdma_v1_0_1
axi_mm2s_mapper_v1_1_14
lib_pkg_v1_0_2
lib_srl_fifo_v1_0_2
lmb_bram_if_cntlr_v4_0
lmb_bram_if_cntlr_v4_0_14
lmb_v10_v3_0
lmb_v10_v3_0_9
lte_3gpp_channel_estimator_v2_0_14
lte_3gpp_mimo_decoder_v3_0_13
lte_3gpp_mimo_encoder_v4_0_12
lte_dl_channel_encoder_v3_0_13
lte_fft_v2_0_15
lte_pucch_receiver_v2_0_13
lte_rach_detector_v3_1_1
lte_ul_channel_decoder_v4_0_13
ltlib_v1_0_0
lut_buffer_v1_0_0
lut_buffer_v2_0_0
mailbox_v2_1_8
mdm_v3_2
mdm_v3_2_12
microblaze_mcs_v2_3_6
microblaze_v10_0_5
microblaze_v9_5_4
mii_to_rmii_v2_0_17
mipi_csi2_rx_ctrl_v1_0_7
mipi_csi2_tx_ctrl_v1_0_3
mipi_dphy_v4_0_1
mipi_dsi_tx_ctrl_v1_0_5
modelsim.ini
mult_gen_v12_0_13
mutex_v2_1_8
oddr_v1_0_0
pc_cfr_v6_0_6
pc_cfr_v6_1_2
pci32_v5_0_9
pci64_v5_0_9
write_bitstream Complete! NA NA NA NA NA 0.817 0 1 0

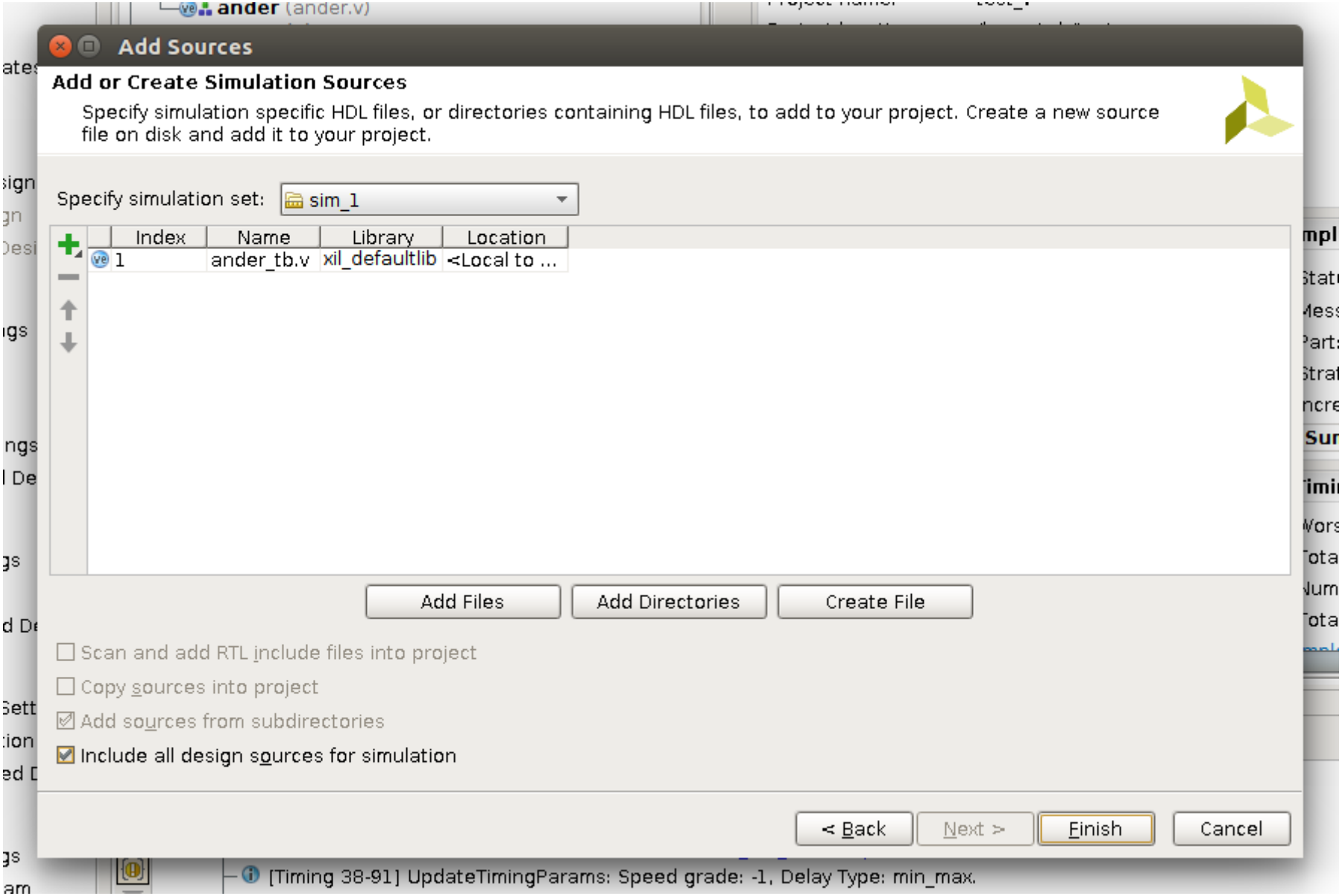

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help
ColumnLayout AllColumns
Library
Name Type Path
ahblite_axi_bridge_v3_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/ahblite_axi_bridge_v3_0_13
amm_axi_bridge_v1_0... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/amm_axi_bridge_v1_0_1
av_pat_gen_v1_0_0 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/av_pat_gen_v1_0_0
axi4stream_vip_v1_0_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi4stream_vip_v1_0_3
axi4stream_vip_v1_1_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi4stream_vip_v1_1_1
axi4svideo_bridge_v1_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi4svideo_bridge_v1_0_8
axi_ahblite_bridge_v3_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_ahblite_bridge_v3_0_13
axi_amm_bridge_v1_0... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_amm_bridge_v1_0_5
axi_apb_bridge_v3_0_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_apb_bridge_v3_0_13
axi_bram_ctrl_v4_0_13... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_bram_ctrl_v4_0_13
axi_cdma_v4_1_15 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_cdma_v4_1_15
axi_chip2chip_v5_0_1 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_chip2chip_v5_0_1
axi_clock_converter_v... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_clock_converter_v2_1_14
axi_crossbar_v2_1_16 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_crossbar_v2_1_16
axi_data_fifo_v2_1_14 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_data_fifo_v2_1_14
axi_datamover_v5_1_1... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_datamover_v5_1_17
axi_dma_v7_1_16 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_dma_v7_1_16
axi_dwidth_converter_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_dwidth_converter_v2_1_15
axi_emc_v3_0_15 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_emc_v3_0_15
axi_epc_v2_0_18 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_epc_v2_0_18
axi_ethernet_buffer_v2... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_ethernet_buffer_v2_0_17
axi_ethernetlite_v3_0_... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_ethernetlite_v3_0_13
axi_fifo_mm_s_v4_1_1... Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_fifo_mm_s_v4_1_12
axi_firewall_v1_0_3 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_firewall_v1_0_3
axi_gpio_v2_0_17 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_gpio_v2_0_17
axi_hwicap_v3_0_19 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_hwicap_v3_0_19
axi_iic_v2_0_18 Library /opt/intelFPGA/16.1/modelsim_ase/xilinx/axi_iic_v2_0_18
Transcript
ModelSim>

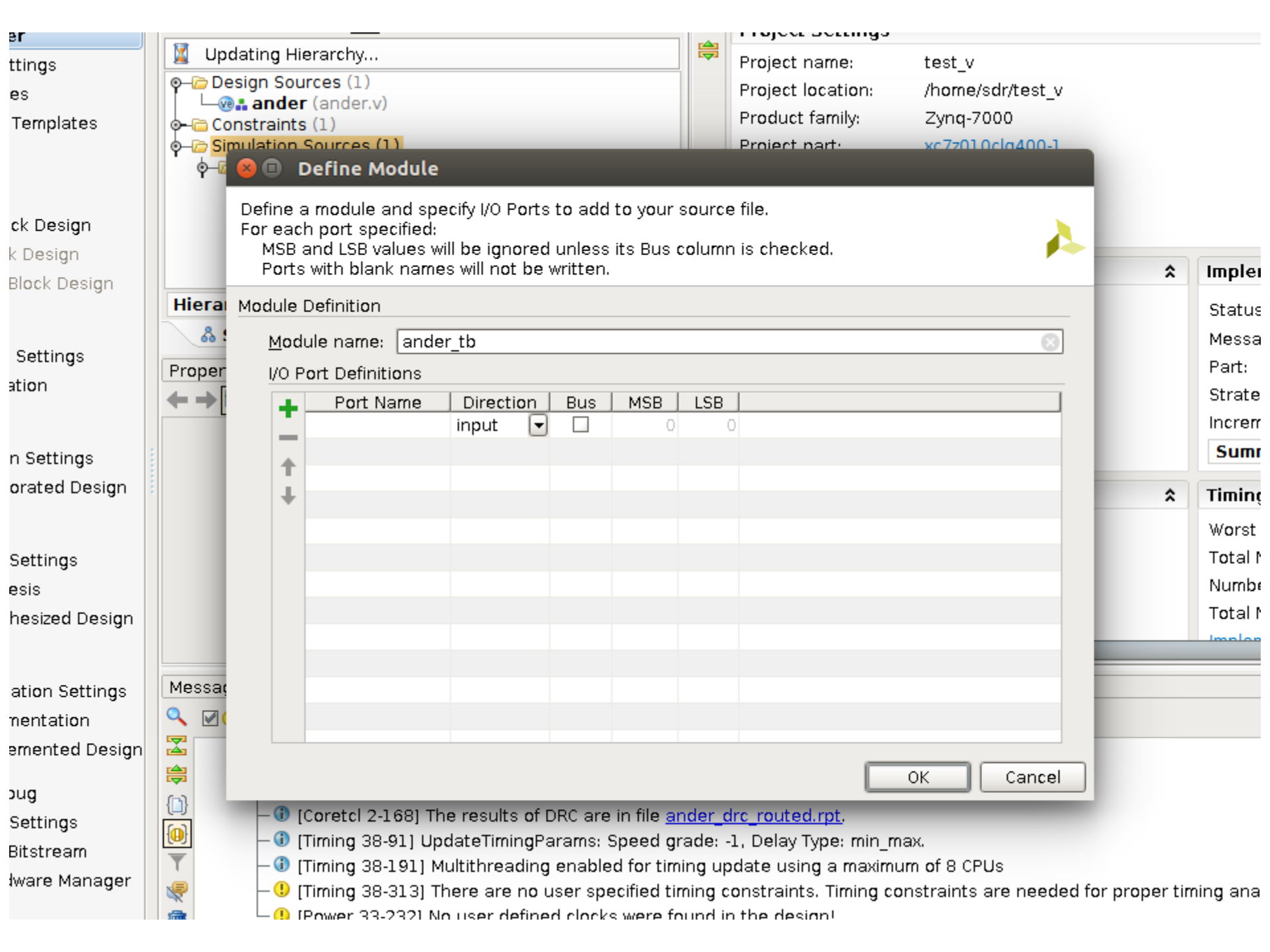

Settings
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
Tool Settings
Project
IP Defaults
Source File
Display
WebTalk
Help
Text Editor
3rd Party Sir
Colors
Selection Ru
Shortcuts
Strategies
Remote Hos
Window Behavior
Simulation
Specify various settings associated to Simulation
Target simulator:
ModelSim Simulator
Simulator language:
Verilog
Simulation set:
sim_1
Simulation top module name:
ander
Compilation
Elaboration
Simulation
Netlist
Advanced
Select an option above to see a description of it
OK
Cancel
Apply
Restore...
Target Simulator
ModelSim Simulator requires that Xilinx libraries are pre-compiled. You can compile Xilinx simulation libraries by going to tools menu and clicking on compile simulation libraries. Make sure that the compiled library location in simulation settings menu is pointing to the correct Modelsim.ini file. To confirm the status of the compiled libraries run report_simlib_info Tcl command.
OK to change your target simulator to 'ModelSim Simulator'?
Yes
No
ulation ran for 1000ns

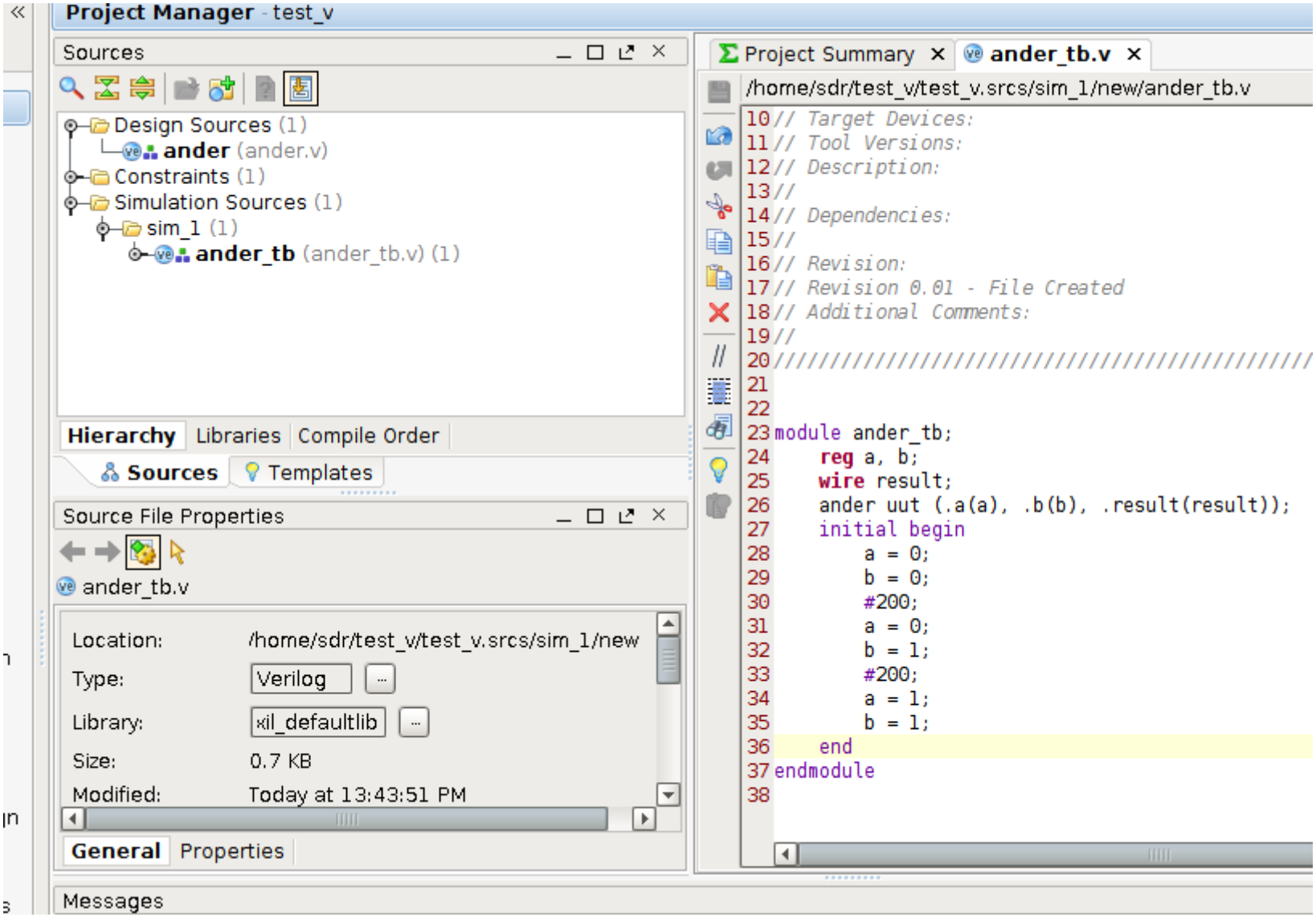
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 11/24/2018 12:34:07 PM
// Design Name:
// Module Name: ander
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module ander(a, b, result);
    input a, b;
    output result;

    assign result = a & b;
endmodule
```

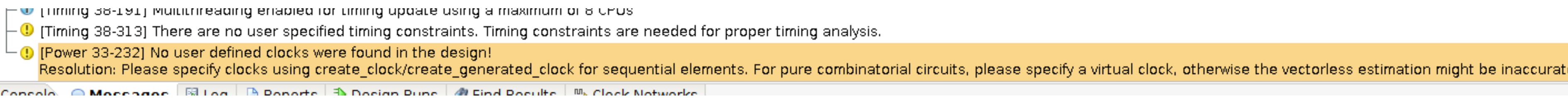

Design Sources (1)
ander (ander.v)
Project name: test_v
Add Sources
Add Sources
This guides you through the process of adding and creating sources for your project
Add or create constraints
Add or create design sources
Add or create simulation sources
Add or create DSP sources
Add existing block design sources
Add existing IP
To continue, click Next
< Back
Next >
Finish
Cancel
[Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs

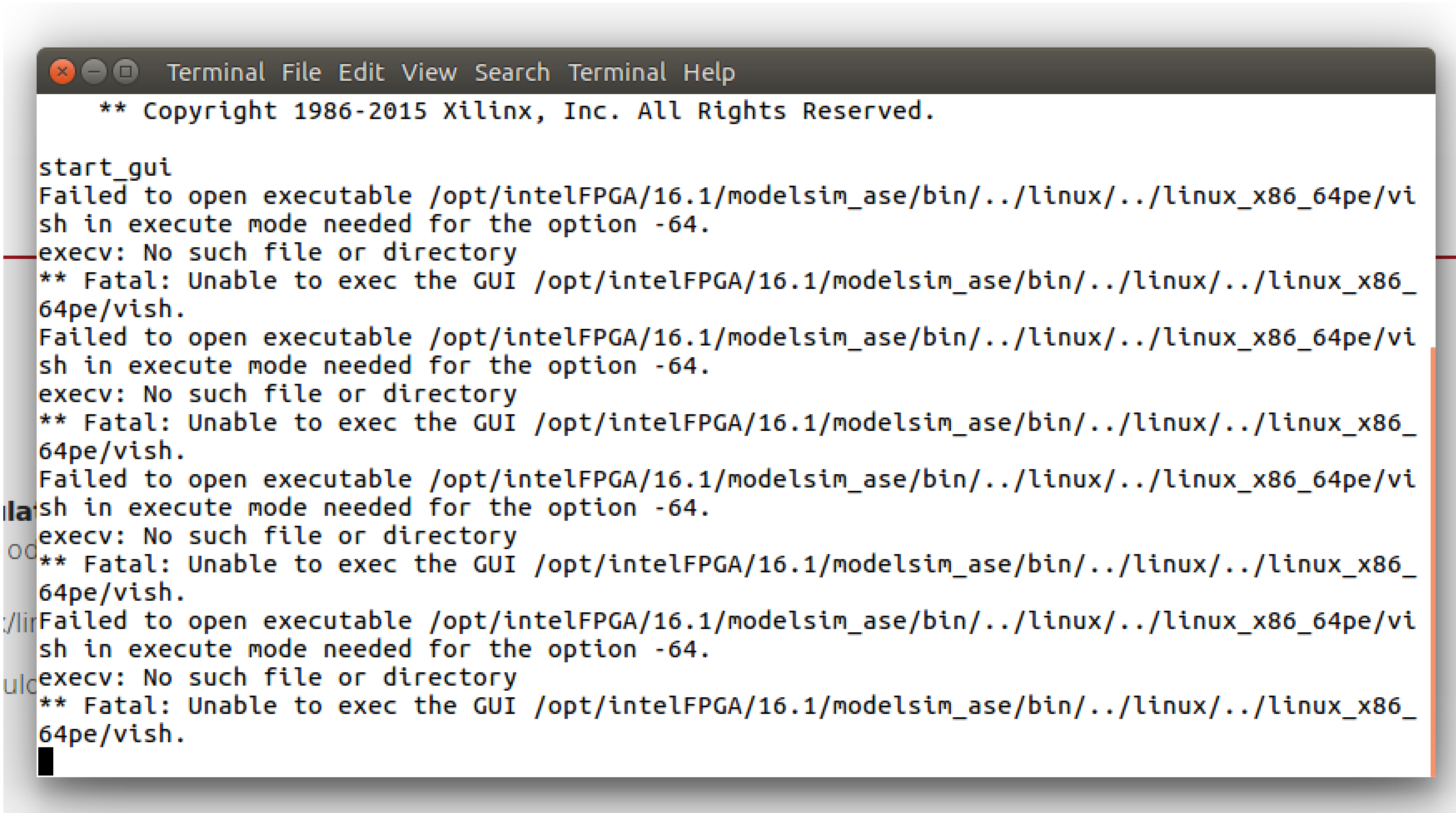

Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Create Source File
Create a new source file and add it to your project.
File type:
Verilog
File name:
ander_tb
File location:
<Local to Project>
OK
Cancel
Scan and add RTL include files into p
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel
[Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min, max.

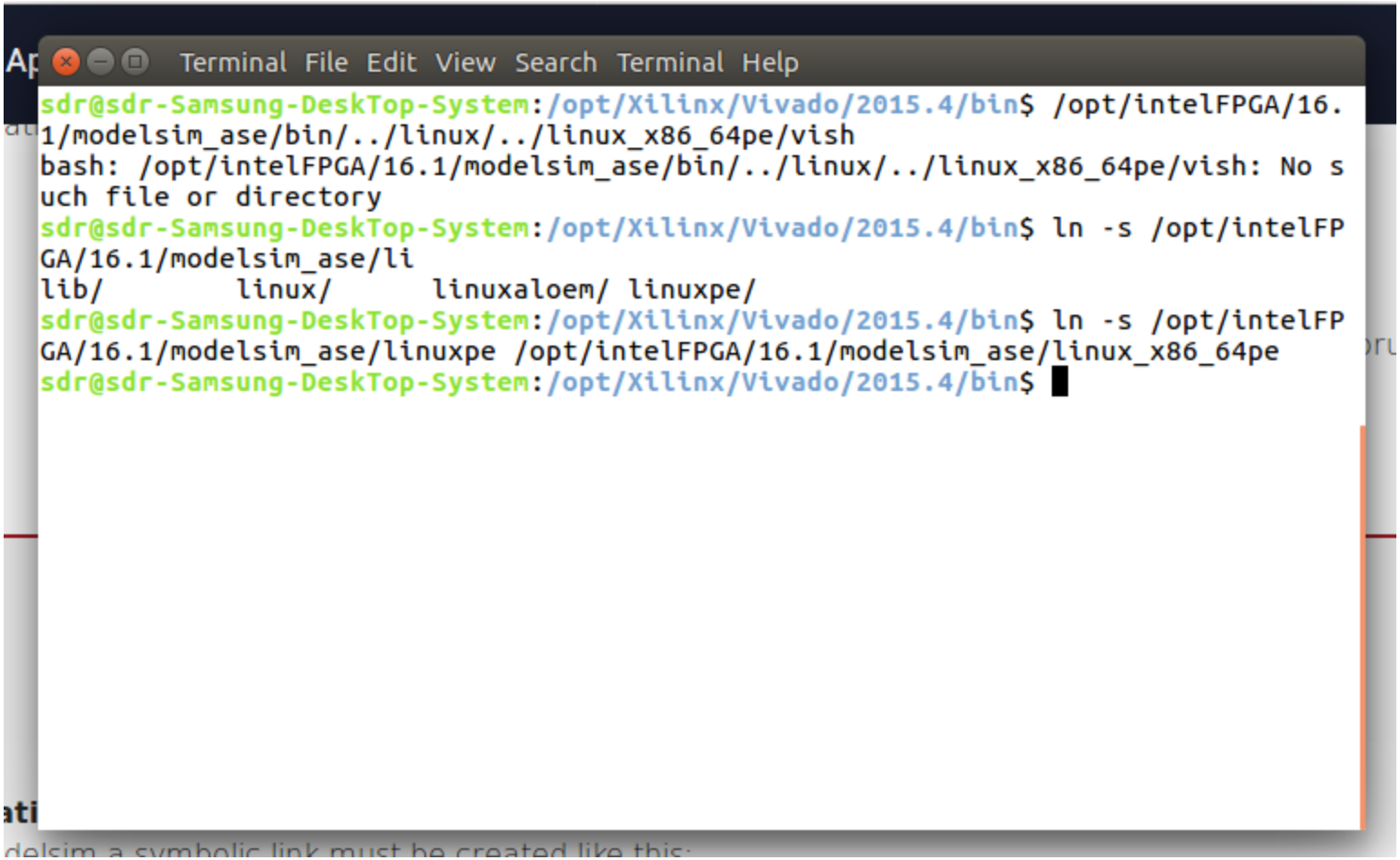

ander (ander.v)
Add Sources
Add or Create Simulation Sources
Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.
Specify simulation set:
sim_1
Index
Name
Library
Location
1
ander_tb.v
xil_defaultlib
<Local to ...
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Include all design sources for simulation
< Back
Next >
Finish
Cancel
[Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.

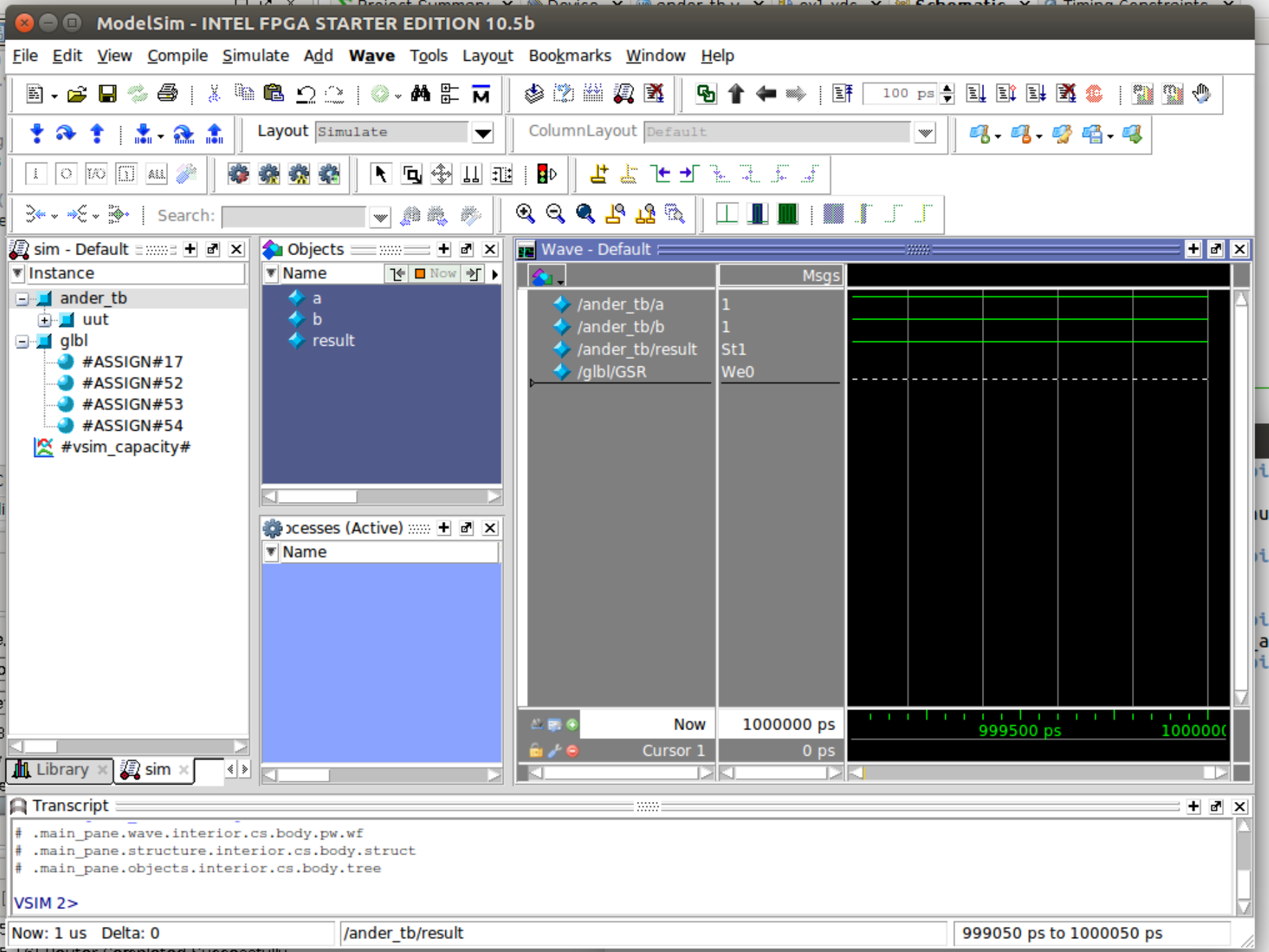

Updating Hierarchy...
Design Sources (1)
ander (ander.v)
Constraints (1)
Simulation Sources (1)
Project name: test_v
Project location: /home/sdr/test_v
Product family: Zynq-7000
Define Module
Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.
Module Definition
Module name: ander_tb
I/O Port Definitions
Port Name
Direction
Bus
MSB
LSB
input
0
0
OK
Cancel
[Coretcl 2-168] The results of DRC are in file ander_drc_routed.rpt.
[Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min_max.
[Timing 38-191] Multithreading enabled for timing update using a maximum of 8 CPUs
[Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing ana

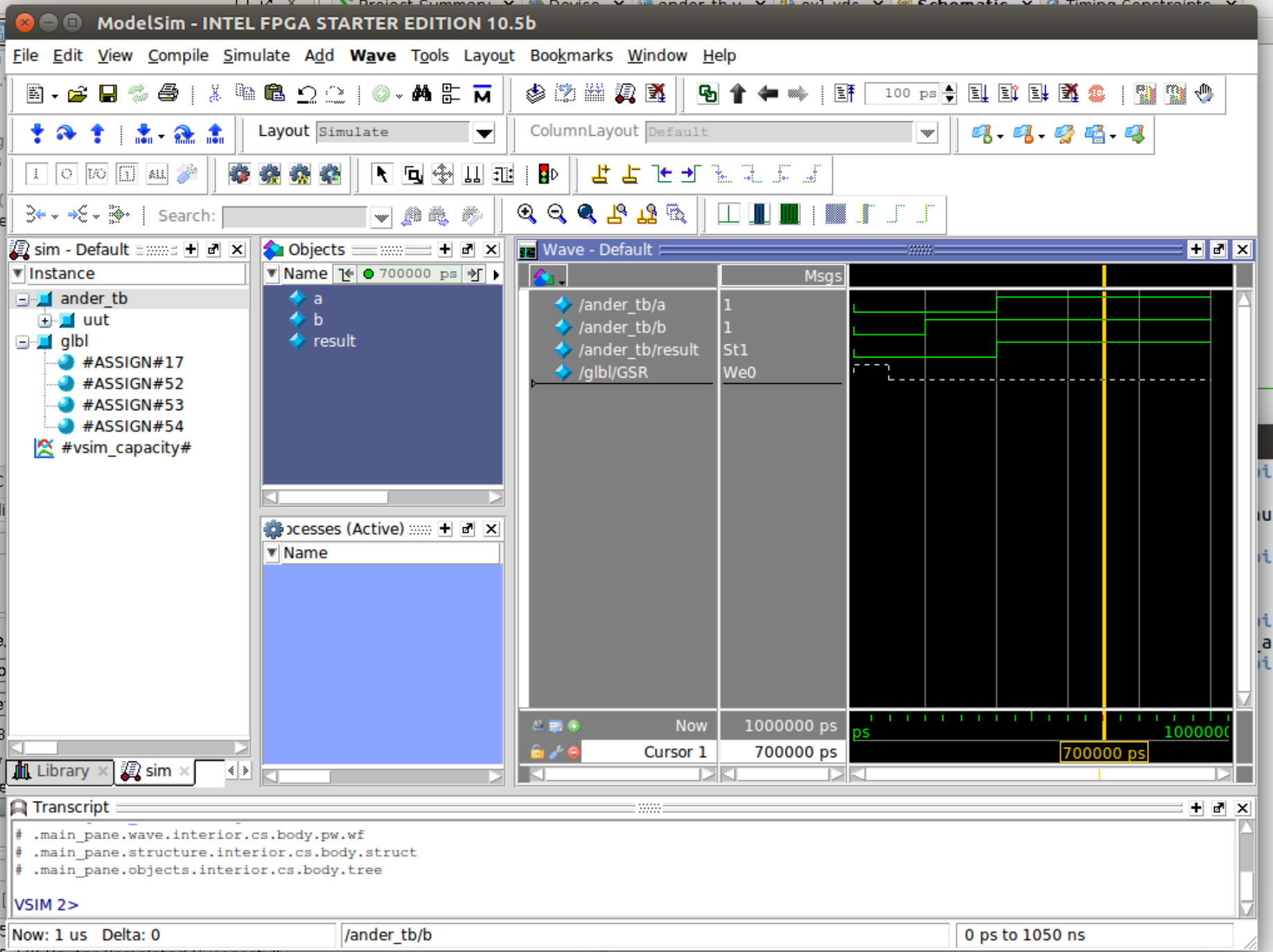

Project Manager - test_v
Sources
Design Sources (1)
ander (ander.v)
Constraints (1)
Simulation Sources (1)
sim_1 (1)
ander_tb (ander_tb.v) (1)
Hierarchy
Libraries
Compile Order
Sources
Templates
Source File Properties
ander_tb.v
Location: /home/sdr/test_v/test_v.srcs/sim_1/new
Type: Verilog
Library: xil_defaultlib
Size: 0.7 KB
Modified: Today at 13:43:51 PM
General
Properties
Project Summary
ander_tb.v
/home/sdr/test_v/test_v.srcs/sim_1/new/ander_tb.v
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21
22
23 module ander_tb;
24 reg a, b;
25 wire result;
26 ander uut (.a(a), .b(b), .result(result));
27 initial begin
28 a = 0;
29 b = 0;
30 #200;
31 a = 0;
32 b = 1;
33 #200;
34 a = 1;
35 b = 1;
36 end
37 endmodule
38
Messages


[Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.
[Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate


Terminal File Edit View Search Terminal Help
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.
start_gui
Failed to open executable /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish in execute mode needed for the option -64.
execv: No such file or directory
** Fatal: Unable to exec the GUI /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish.
Failed to open executable /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish in execute mode needed for the option -64.
execv: No such file or directory
** Fatal: Unable to exec the GUI /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish.
Failed to open executable /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish in execute mode needed for the option -64.
execv: No such file or directory
** Fatal: Unable to exec the GUI /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish.
Failed to open executable /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish in execute mode needed for the option -64.
execv: No such file or directory
** Fatal: Unable to exec the GUI /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish.


Terminal File Edit View Search Terminal Help
sdr@sdr-Samsung-DeskTop-System:/opt/Xilinx/Vivado/2015.4/bin$ /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish
bash: /opt/intelFPGA/16.1/modelsim_ase/bin/../linux/../linux_x86_64pe/vish: No such file or directory
sdr@sdr-Samsung-DeskTop-System:/opt/Xilinx/Vivado/2015.4/bin$ ln -s /opt/intelFPGA/16.1/modelsim_ase/li
lib/ linux/ linuxaloem/ linuxpe/
sdr@sdr-Samsung-DeskTop-System:/opt/Xilinx/Vivado/2015.4/bin$ ln -s /opt/intelFPGA/16.1/modelsim_ase/linuxpe /opt/intelFPGA/16.1/modelsim_ase/linux_x86_64pe
sdr@sdr-Samsung-DeskTop-System:/opt/Xilinx/Vivado/2015.4/bin$


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
sim - Default
Instance
ander_tb
uut
glbl
#ASSIGN#17
#ASSIGN#52
#ASSIGN#53
#ASSIGN#54
#vsim_capacity#
Objects
Name
Now
a
b
result
ocesses (Active)
Name
Wave - Default
Msgs
/ander_tb/a
/ander_tb/b
/ander_tb/result
/glbl/GSR
1
1
St1
We0
Now
1000000 ps
Cursor 1
0 ps
999500 ps
Library
sim
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>
Now: 1 us Delta: 0
/ander_tb/result
999050 ps to 1000050 ps


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
sim - Default
Instance
ander_tb
uut
glbl
#ASSIGN#17
#ASSIGN#52
#ASSIGN#53
#ASSIGN#54
#vsim_capacity#
Objects
Name
700000 ps
a
b
result
ocesses (Active)
Name
Wave - Default
Msgs
/ander_tb/a
/ander_tb/b
/ander_tb/result
/glbl/GSR
1
1
St1
We0
Now
1000000 ps
Cursor 1
700000 ps
ps
700000 ps
Library
sim
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>
Now: 1 us Delta: 0
/ander_tb/b
0 ps to 1050 ns