TI DSP, MCU, Xilinx Zynq FPGA
프로그래밍 전문가 과정

Servo Motor IP Create

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진행상황

Vivado - PWM IP Create

my_pwm_v1_0

```
timescale 1 ns / 1 ps

    module my_pwm_v1_0 #
    (
        // Users to add parameters here

        // User parameters ends
        // Do not modify the parameters beyond this line
        parameter integer PWM_COUNTER_MAX = 128,

        // Parameters of Axi Slave Bus Interface S00_AXI
        parameter integer C_S00_AXI_DATA_WIDTH  = 32,
        parameter integer C_S00_AXI_ADDR_WIDTH  = 4
    )
    (
        // Users to add ports here

        // User ports ends
        // Do not modify the ports beyond this line

        output wire PWM,
        // Ports of Axi Slave Bus Interface S00_AXI
        input wire  s00_axi_aclk,
```

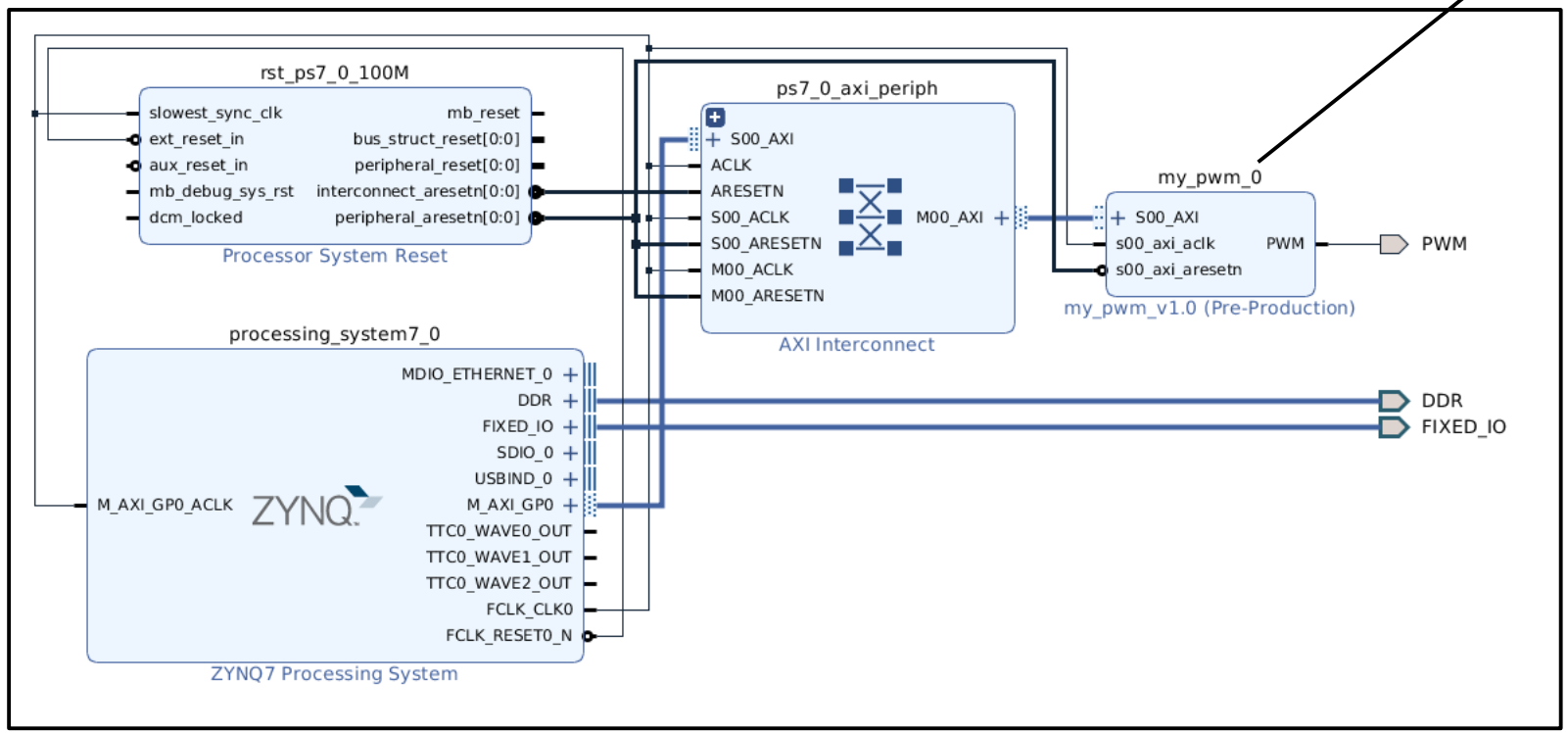
```
// Instantiation of Axi Bus Interface S00_AXI
    my_pwm_v1_0_S00_AXI # (
        .C_S_AXI_DATA_WIDTH(C_S00_AXI_DATA_WIDTH),
        .C_S_AXI_ADDR_WIDTH(C_S00_AXI_ADDR_WIDTH),
        .PWM_COUNTER_MAX(PWM_COUNTER_MAX)
    ) my_pwm_v1_0_S00_AXI_inst (
        .PWM(PWM),
        .S_AXI_ACLK(s00_axi_aclk),
        .S_AXI_ARESETN(s00_axi_aresetn),
        .S_AXI_AWADDR(s00_axi_awaddr),
```

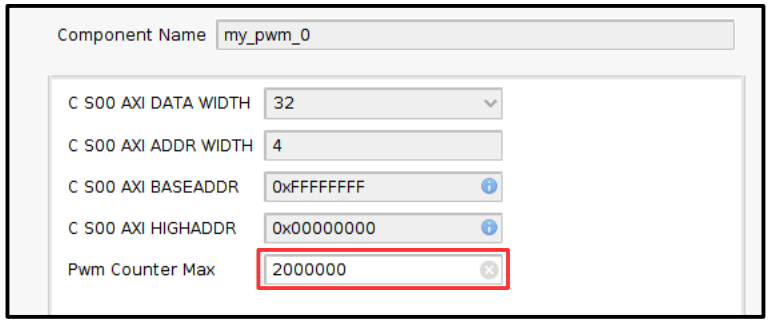
my_pwm_v1_0_S00_AXI_inst

```
timescale 1 ns / 1 ps

    module my_pwm_v1_0_S00_AXI #
    (
        // Users to add parameters here
        parameter integer PWM_COUNTER_MAX = 2000000,
        // User parameters ends
        // Do not modify the parameters beyond this line

        // Width of S_AXI data bus
        parameter integer C_S_AXI_DATA_WIDTH    = 32,
        // Width of S_AXI address bus
        parameter integer C_S_AXI_ADDR_WIDTH    = 4
    )
    (
        // Users to add ports here

        output wire PWM,
        // User ports ends
        // Do not modify the ports beyond this line
```

```
reg [31:0] counter = 0;
// Add user logic here
always @(posedge S_AXI_ACLK) begin
    if(counter < PWM_COUNTER_MAX - 32'd1 )
        counter <= counter + 32'd1;
    else
        counter <= 32'd0;

end

assign PWM = slv_reg0 < counter ? 1'b0 : 1'b1;
// User logic ends
```

Vivado - Block Design





SDK - 각도제어

```
float duty (int angle)
{
    return ((1.0 + angle/180.0) / 20.0 );
}
//1ms == 0도
//2ms == 180도
```

→ 정확한 제어 불가능
180 도 보다 적게 돌게 된다

```
#include "xparameters.h"
#include "xil_io.h"
#define MY_PWM 0x43C00000
#define period  2000000

int main(){
    int i, angle=0;
    float num=0;
    while(1){
        //0
        num = 62800;
        Xil_Out32(MY_PWM, num);
        for(i=0;i<140000000; i++);
        //90
        num = 151400;
        Xil_Out32(MY_PWM, num);
        for(i=0;i<140000000; i++);
        //180
        num = 240000;
        Xil_Out32(MY_PWM, num);
        for(i=0;i<140000000; i++);
    }

}
```

진행상황

Vivado - Servo PWM IP Create

My_SERVO_CORE_v1_0

```
`timescale 1 ns / 1 ps

    module My_SERVO_Core_v1_0 #
    (
        // Users to add parameters here
        parameter real ANGLE = 5.4 ,
        parameter integer PWM_MAX = 2000000,
        // User parameters ends
        // Do not modify the parameters beyond this line


        // Parameters of Axi Slave Bus Interface S00_AXI
        parameter integer C_S00_AXI_DATA_WIDTH  = 32,
        parameter integer C_S00_AXI_ADDR_WIDTH  = 4
    )
    (
        // Users to add ports here
        output wire PWM,
        // User ports ends
        // Do not modify the ports beyond this line
```

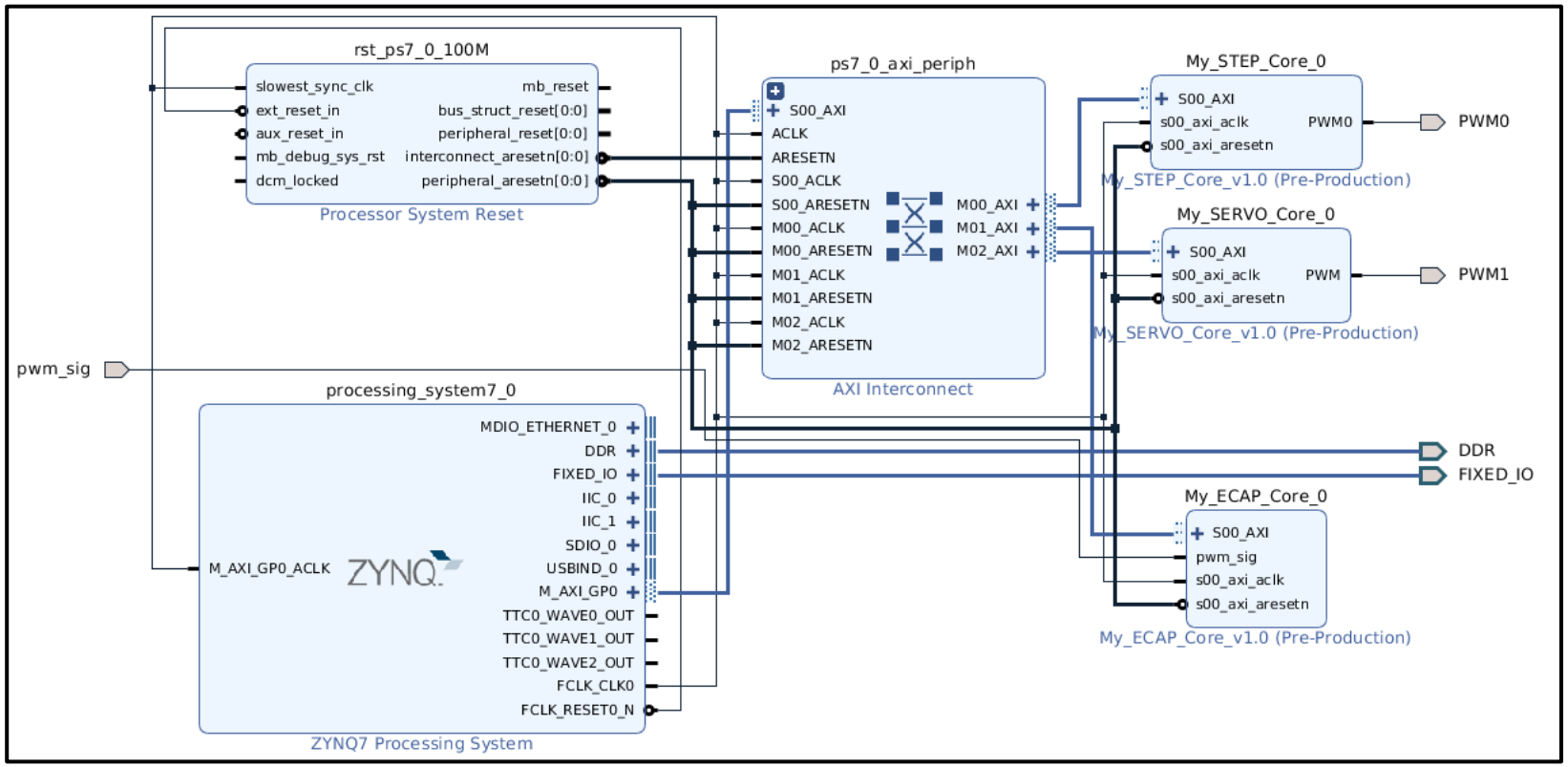
```
// Instantiation of Axi Bus Interface S00_AXI
    My_SERVO_Core_v1_0_S00_AXI # (
        .C_S_AXI_DATA_WIDTH(C_S00_AXI_DATA_WIDTH),
        .C_S_AXI_ADDR_WIDTH(C_S00_AXI_ADDR_WIDTH),
        .PWM_MAX(PWM_MAX),
        .ANGLE(ANGLE)
    ) My_SERVO_Core_v1_0_S00_AXI_inst (
        .PWM(PWM),
        .S_AXI_ACLK(s00_axi_aclk),
        .S_AXI_ARESETN(s00_axi_aresetn)
```

My_SERVO_CORE_v1_0_S00_AXI_inst

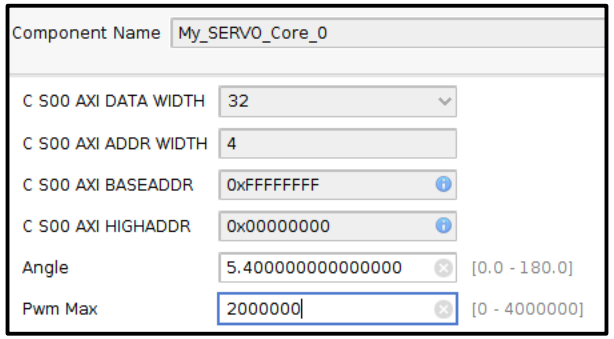
```
`timescale 1 ns / 1 ps

    module My_SERVO_Core_v1_0_S00_AXI #
    (
        // Users to add parameters here
        parameter real ANGLE = 5.4,
        parameter integer PWM_MAX = 2000000,
        // User parameters ends
        // Do not modify the parameters beyond this line

        // Width of S_AXI data bus
        parameter integer C_S_AXI_DATA_WIDTH    = 32,
        // Width of S_AXI address bus
        parameter integer C_S_AXI_ADDR_WIDTH    = 4
    )
    (
        // Users to add ports here
        output wire PWM,
        // User ports ends
        // Do not modify the ports beyond this line
```

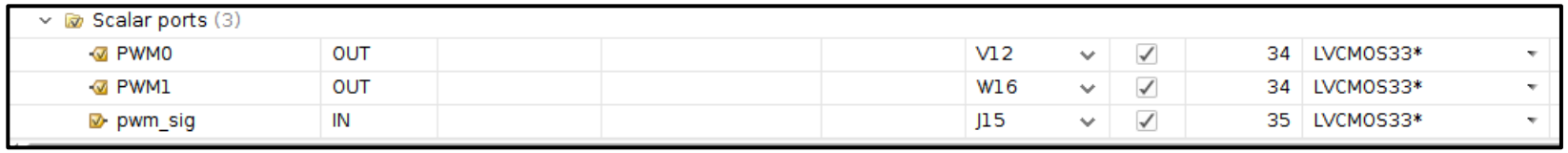
```
// Add user logic here
reg [31:0] counter = 0;
reg [31:0] duty = 32'd62800 + ANGLE * 32'd88600 / 90;
always @(posedge S_AXI_ACLK) begin

    if(counter > PWM_MAX - 32'd1 )
        counter <= 0;
    else
        counter = counter + 32'd1;

end

assign PWM = counter > duty ? 32'd0 : 32'd1;
// User logic ends
```

Vivado - All Test Block Design



Device_tree 에서
My_STEP_Core_0 는
uio 장치파일을 생성하지 않음 .





Scalar ports (3)								
PWM0	OUT				V12	✓	34	LVCMOS33*
PWM1	OUT				W16	✓	34	LVCMOS33*
pwm_sig	IN				J15	✓	35	LVCMOS33*

감사합니다