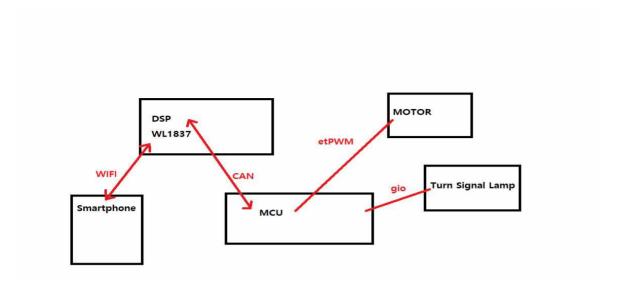
Xilinx Zynq FPGA, TI DSP, MCU 기반의 회로 설계 및 임베디드 전문가 과정

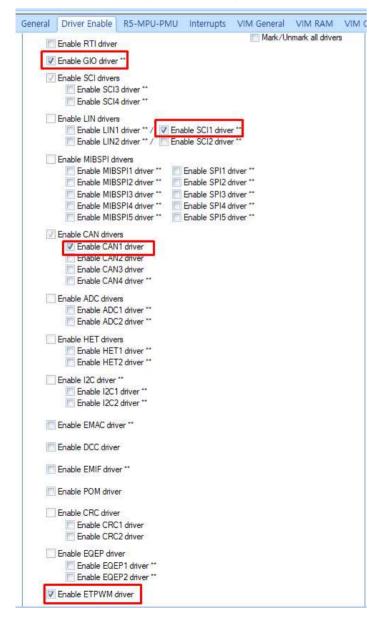
통합테스트 - MCU

1.통합 테스트 전체 구성도



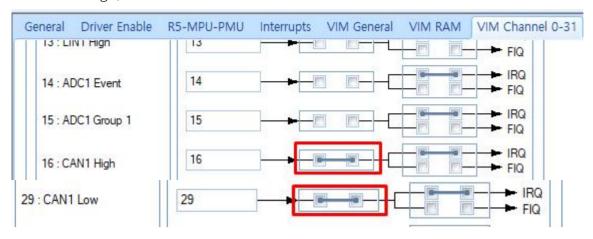
2.HalCoGen 설정.

Driver Enable: GIO, SCI1, CAN1, etPWM



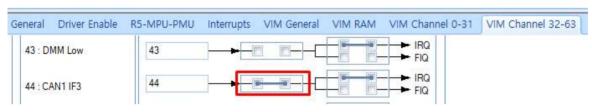
VIM Channel 0-31

16: CAN1 High, 29: CAN1 LOW



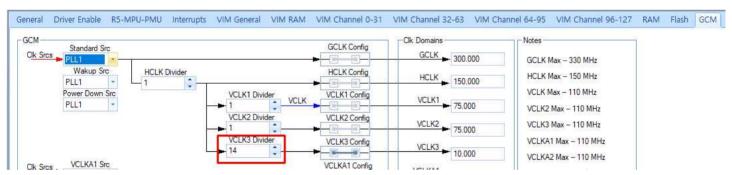
VIM Channel 32-63

44 : CAN1 IF3

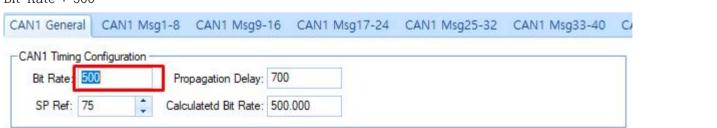


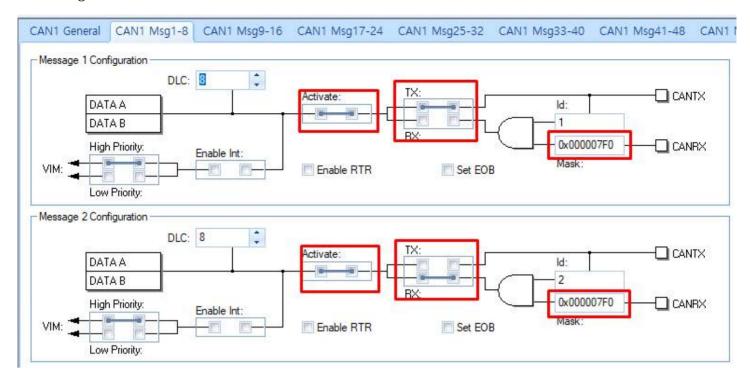
GCM

VCLK3 Divider: 14

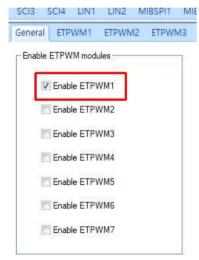


CAN1 General Bit Rate: 500



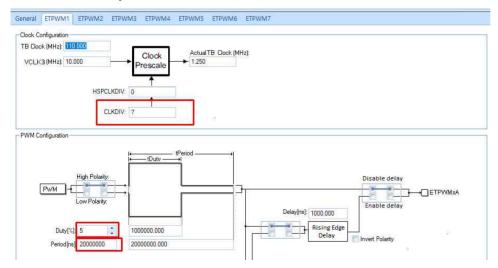


ETPWM General



ETPWM1

CLKDIV: 7, Duty 5%, Period 20000000



완료 후 F5 or Code Gernerate를 한다.

```
#include <HL_etpwm.h>
#include <HL_hal_stdtypes.h>
#include <HL_reg_sci.h>
#include <HL_sci.h>
#include "HL_can.h"
#include "HL_gio.h"
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
int main(void)
    uint8 rx_data[32] = \{0,\};
    uint8 tx_data[8]= {8, 7, 6, 5, 1, 1, 1, 1};
    int data = 0;
    int i, j;
    etpwmInit();
    sciInit();
    canInit();
    gioInit();
    etpwmStartTBCLK();
    canEnableErrorNotification(canREG1); //canIoSetDirection(canREG1, canMESSAGE_BOX1, canMESSAGE_BOX2);
    gioSetBit(gioPORTA, 0, 1);
    for(i=0;i<1000;i++)
        for(j=0;j<300000;j++)
        canTransmit(canREG1, canMESSAGE_BOX3, (const uint8*)&tx_data[0]);
    while(1)
        while(!canIsRxMessageArrived(canREG1, canMESSAGE_BOX4))
            canGetData(canREG1, canMESSAGE_BOX4, (const uint8*)&rx_data[0]);
              switch(rx_data[0]){
                   case 13:
                       data = (rx_data[1])*1000 + (rx_data[2])*100 + (rx_data[3])*10 + (rx_data[4]);
                       data *= 1.25;
                       break
                   case 7:
                       gioSetBit(gioPORTA, 0, rx_data[1]);
//
               data = (rx_data[0] - 48)*1000 + (rx_data[1] - 48)*100 + (rx_data[2] - 48)*10 + (rx_data[3] - 48);
//
               data = atoi(rx_data);
            etpwmREG1->CMPA = data;
            memset(rx_data, 0, sizeof(rx_data));
            data = 0;
//
    return 0;
}
```

4.MCU 선 연결

