Pmod CAN Control with Zybo

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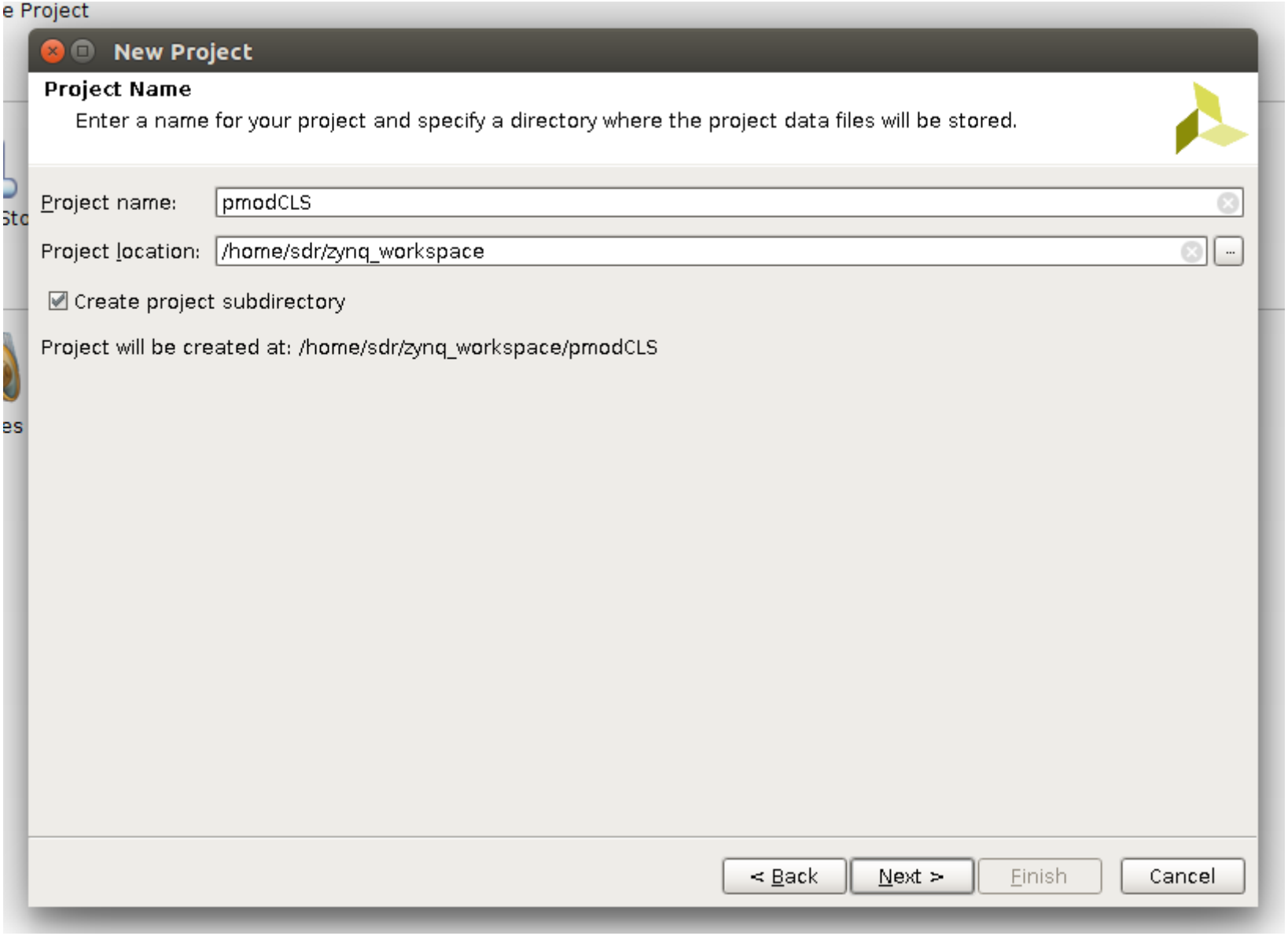
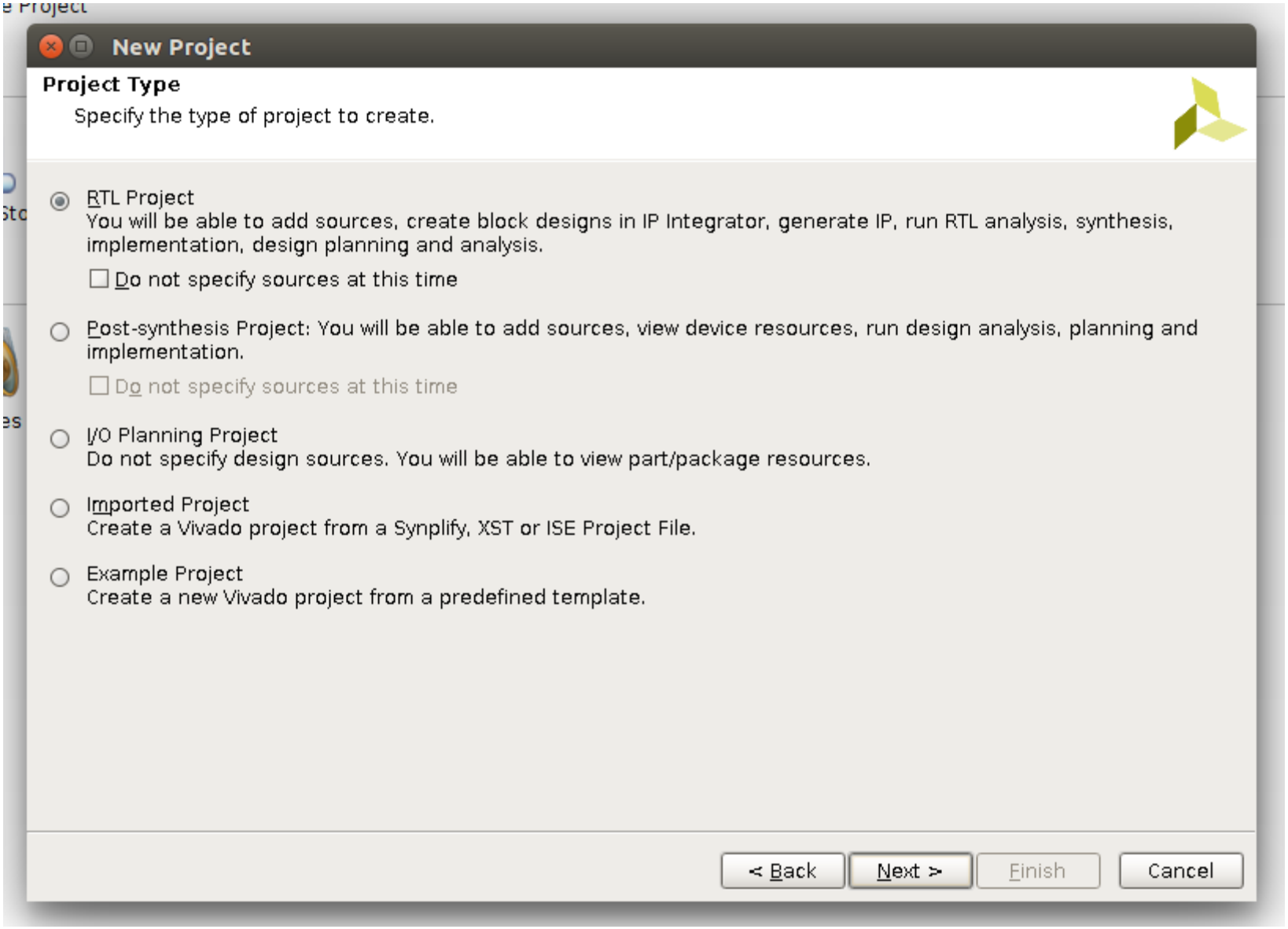
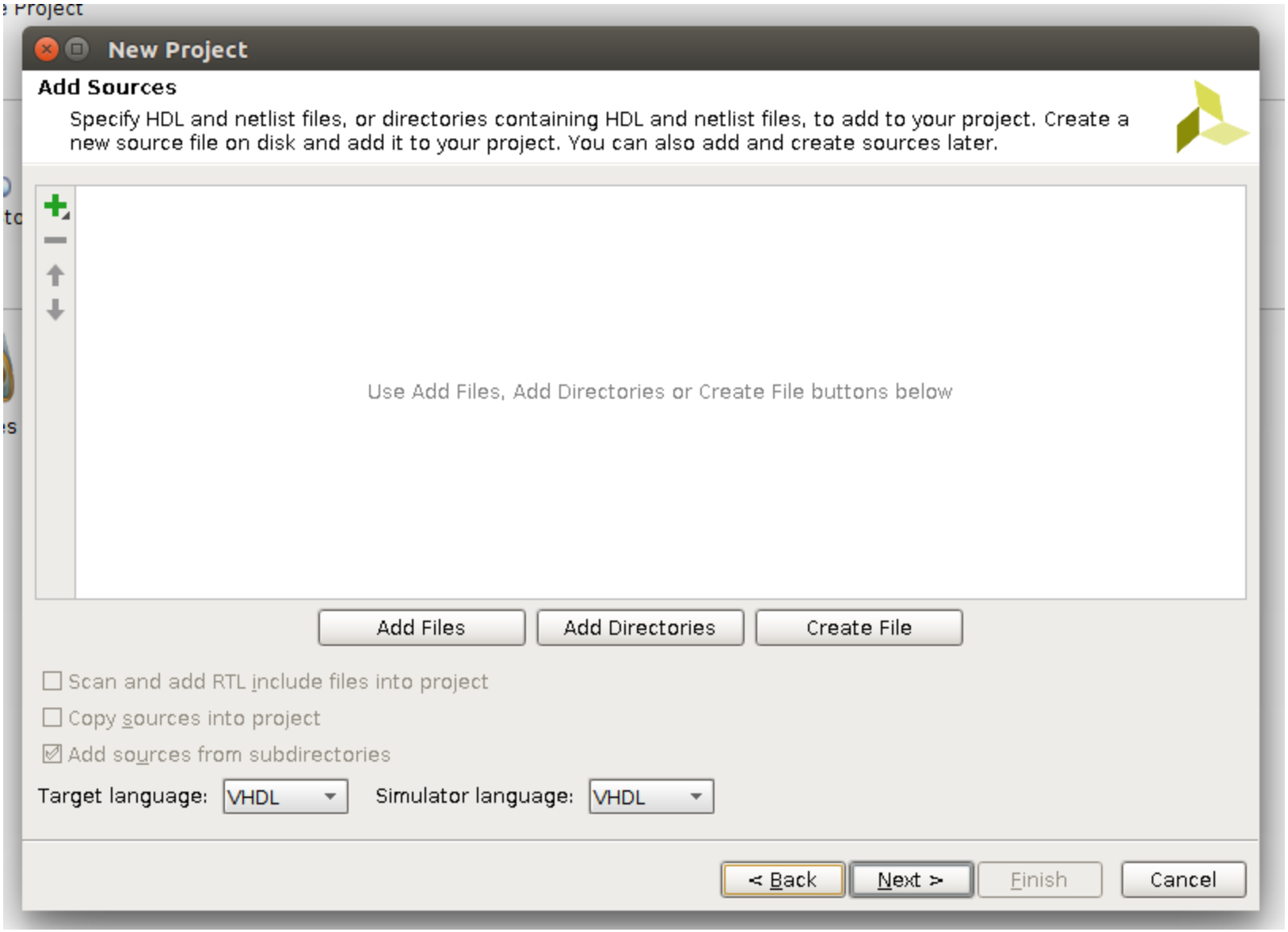
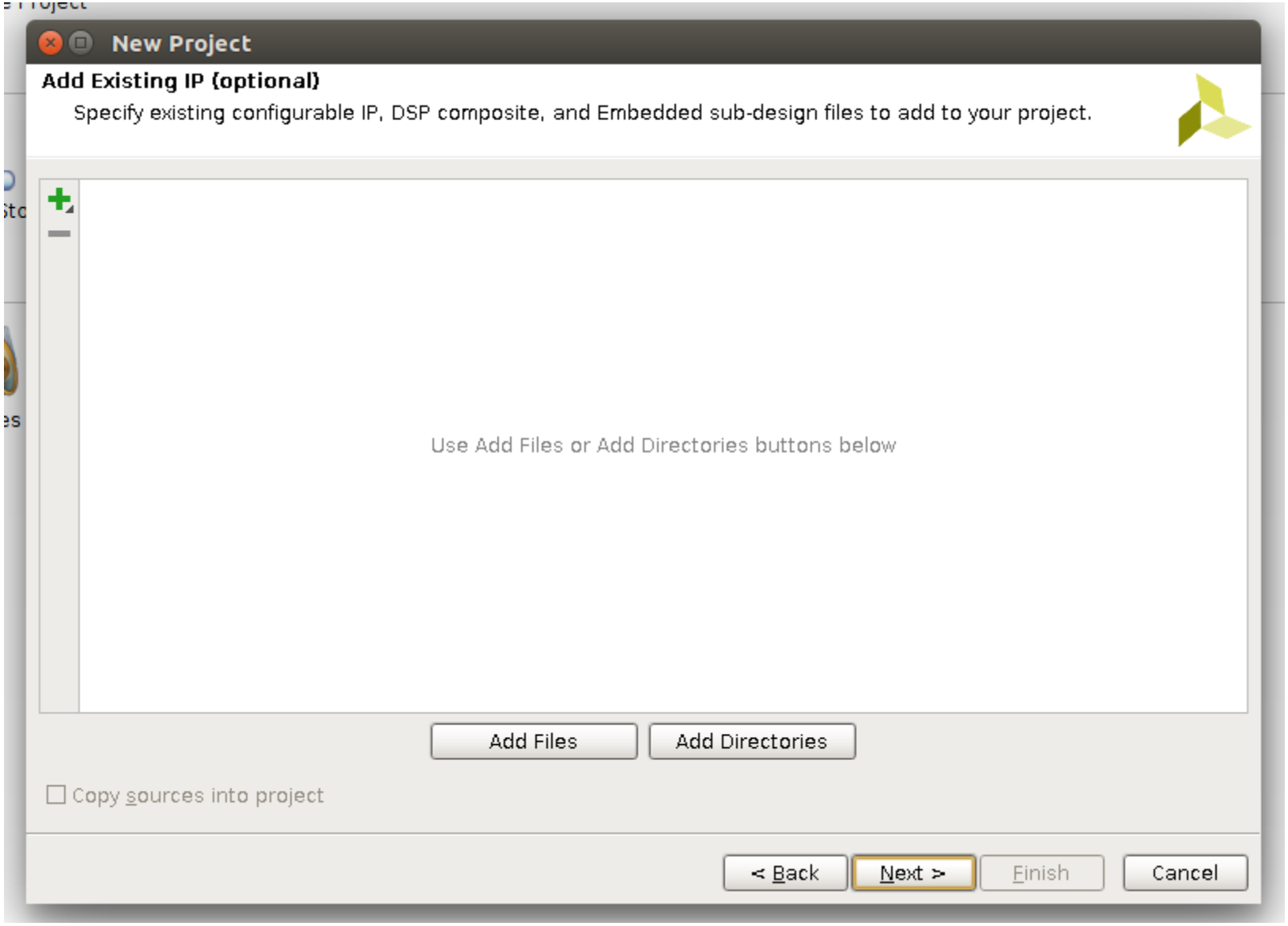
gcccompil3r@gmail.com

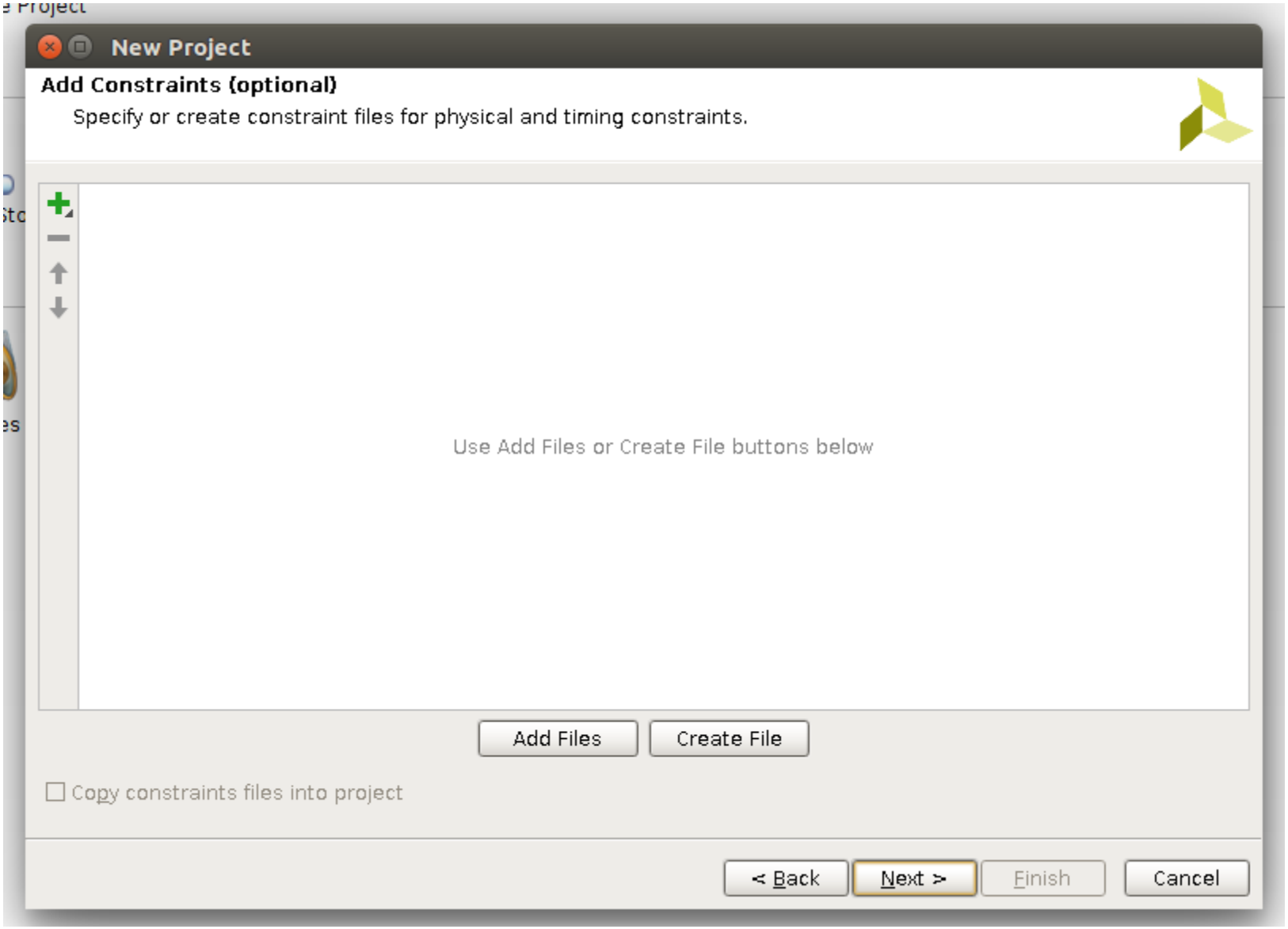
이름이 pmodCLS 라고 되어 있는데 pmodCAN 으로 수정하도록 한다.

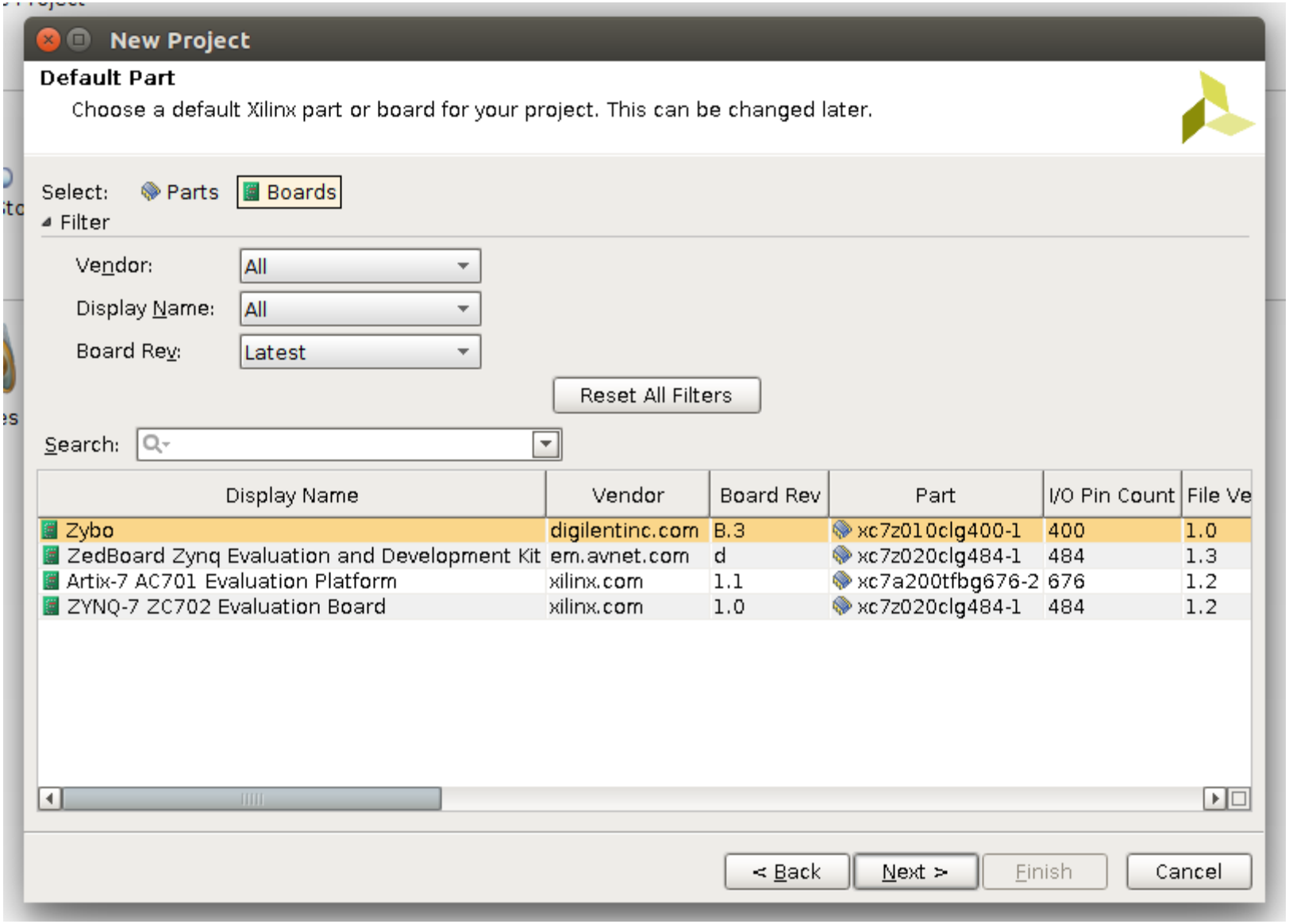


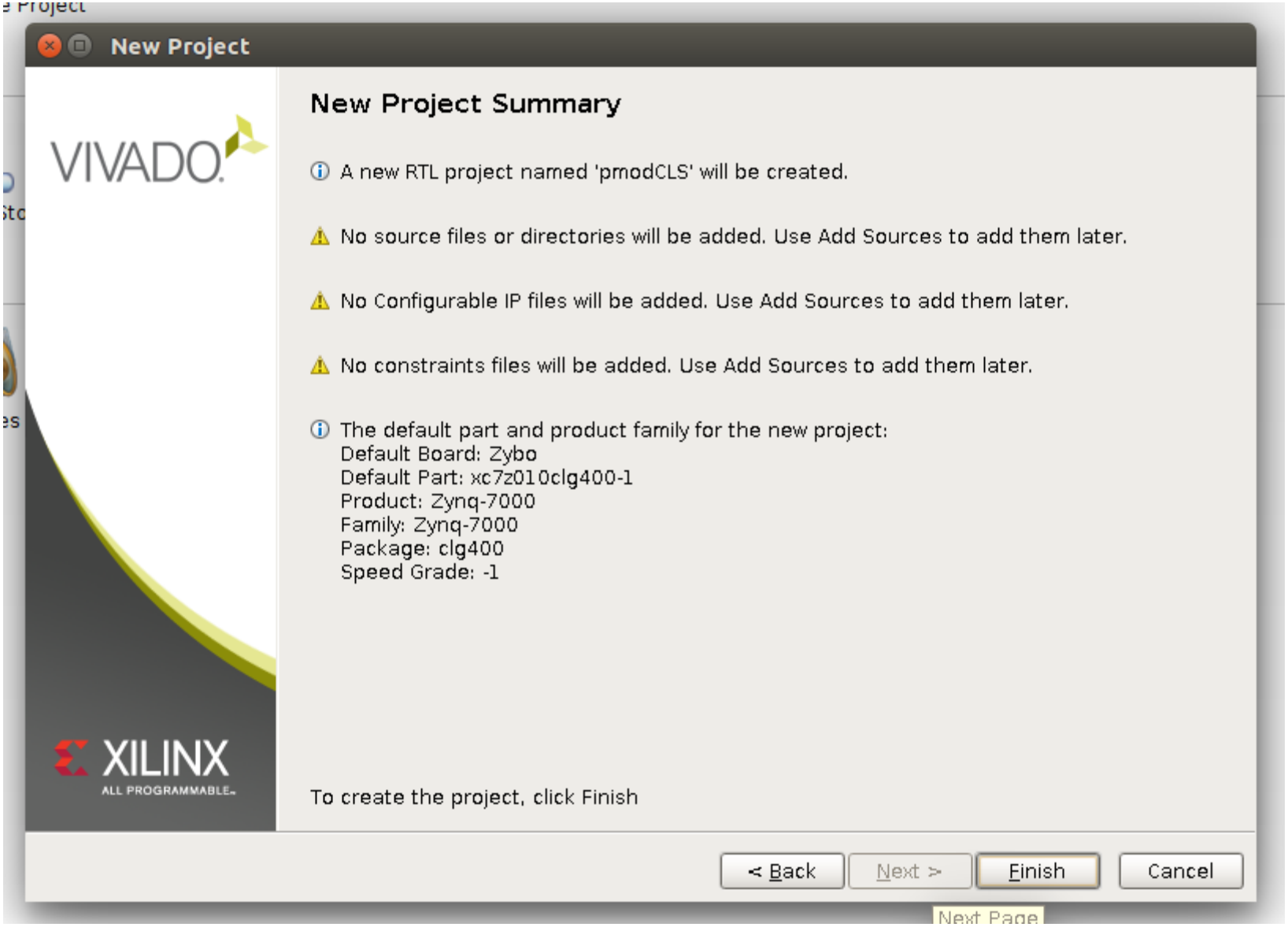

New Project
Project Type
Specify the type of project to create.
RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
Do not specify sources at this time
Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
Do not specify sources at this time
I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.
Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.
Example Project
Create a new Vivado project from a predefined template.
< Back
Next >
Finish
Cancel

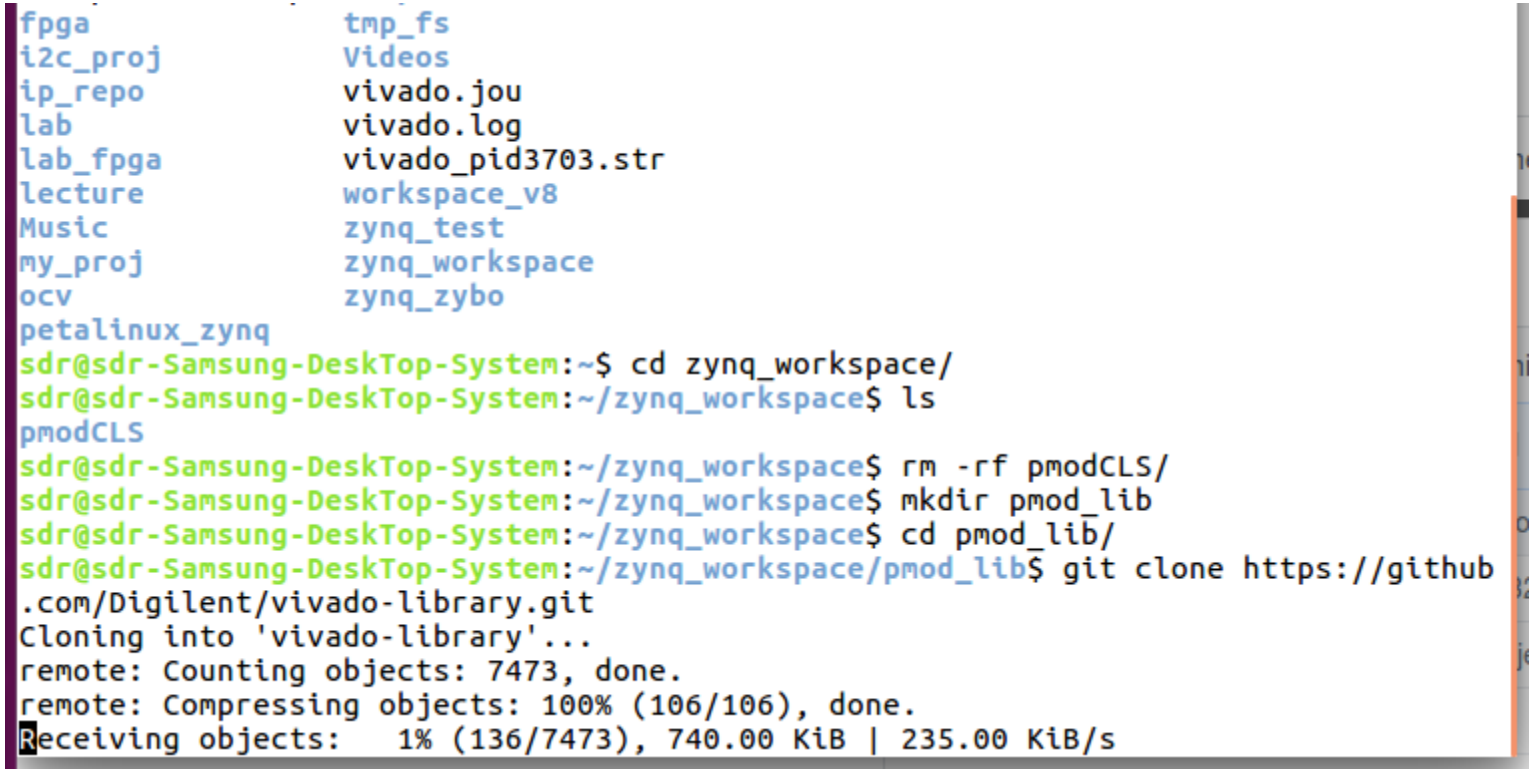

Project
New Project
Add Sources
Specify HDL and netlist files, or directories containing HDL and netlist files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Use Add Files, Add Directories or Create File buttons below
Add Files
Add Directories
Create File
Scan and add RTL include files into project
Copy sources into project
Add sources from subdirectories
Target language: VHDL
Simulator language: VHDL
< Back
Next >
Finish
Cancel

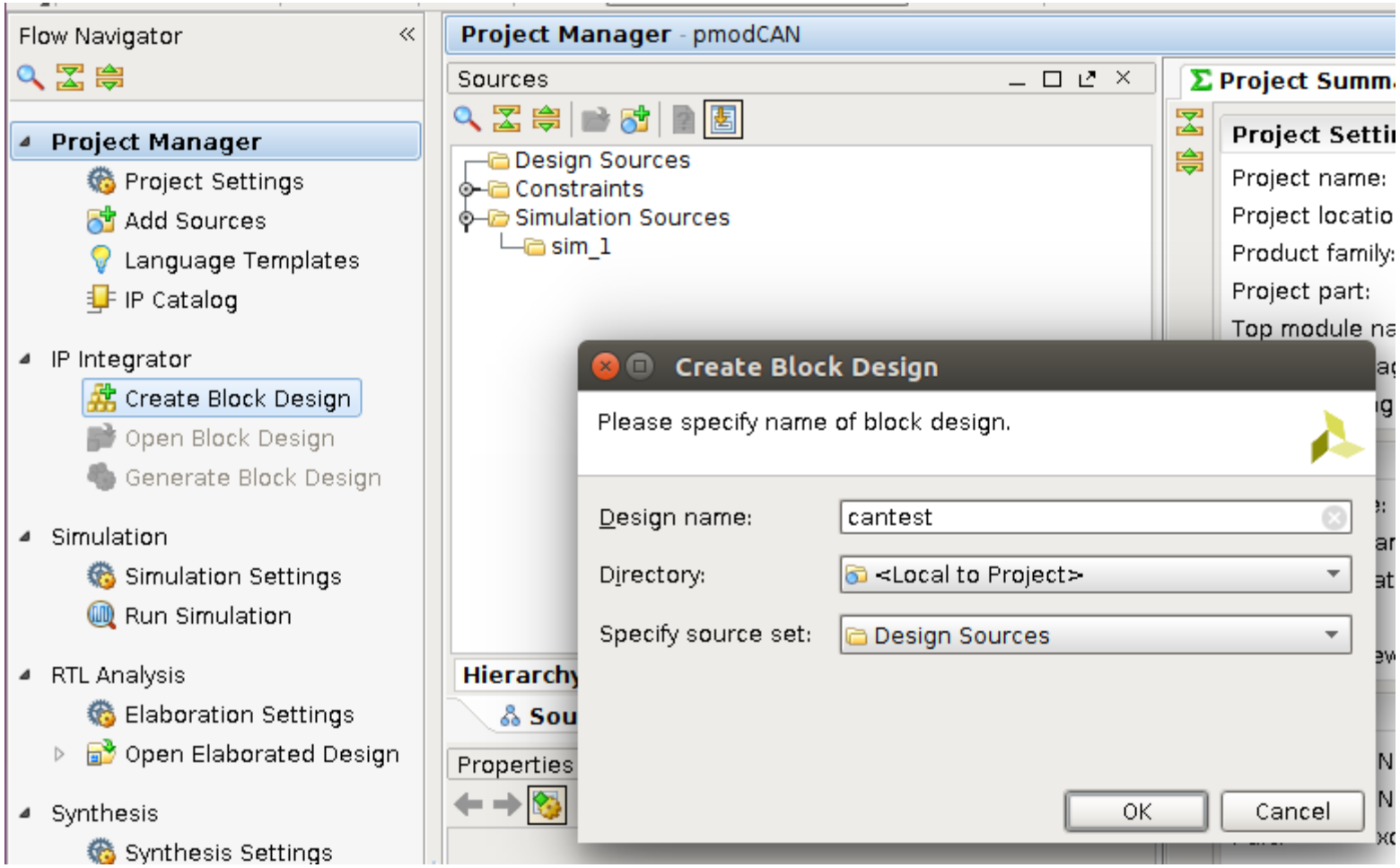

New Project
Add Existing IP (optional)
Specify existing configurable IP, DSP composite, and Embedded sub-design files to add to your project.
Use Add Files or Add Directories buttons below
Add Files
Add Directories
Copy sources into project
< Back
Next >
Finish
Cancel


New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Use Add Files or Create File buttons below
Add Files
Create File
Copy constraints files into project
< Back
Next >
Finish
Cancel


New Project
Default Part
Choose a default Xilinx part or board for your project. This can be changed later.
Select:
Parts
Boards
Filter
Vendor:
All
Display Name:
All
Board Rev:
Latest
Reset All Filters
Search:
Display Name
Vendor
Board Rev
Part
I/O Pin Count
File Ve
Zybo
digilentinc.com
B.3
xc7z010clg400-1
400
1.0
ZedBoard Zynq Evaluation and Development Kit
em.avnet.com
d
xc7z020clg484-1
484
1.3
Artix-7 AC701 Evaluation Platform
xilinx.com
1.1
xc7a200tfbg676-2
676
1.2
ZYNQ-7 ZC702 Evaluation Board
xilinx.com
1.0
xc7z020clg484-1
484
1.2
< Back
Next >
Finish
Cancel


New Project
VIVADO
New Project Summary
A new RTL project named 'pmodCLS' will be created.
No source files or directories will be added. Use Add Sources to add them later.
No Configurable IP files will be added. Use Add Sources to add them later.
No constraints files will be added. Use Add Sources to add them later.
The default part and product family for the new project:
Default Board: Zybo
Default Part: xc7z010clg400-1
Product: Zynq-7000
Family: Zynq-7000
Package: clg400
Speed Grade: -1
XILINX
ALL PROGRAMMABLE
To create the project, click Finish
< Back
Next >
Finish
Cancel
Next Page


fpga
i2c_proj
ip_repo
lab
lab_fpga
lecture
Music
my_proj
ocv
petalinux_zynq
tmp_fs
Videos
vivado.jou
vivado.log
vivado_pid3703.str
workspace_v8
zynq_test
zynq_workspace
zynq_zybo
sdr@sdr-Samsung-DeskTop-System:~$ cd zynq_workspace/
sdr@sdr-Samsung-DeskTop-System:~/zynq_workspace$ ls
pmodCLS
sdr@sdr-Samsung-DeskTop-System:~/zynq_workspace$ rm -rf pmodCLS/
sdr@sdr-Samsung-DeskTop-System:~/zynq_workspace$ mkdir pmod_lib
sdr@sdr-Samsung-DeskTop-System:~/zynq_workspace$ cd pmod_lib/
sdr@sdr-Samsung-DeskTop-System:~/zynq_workspace/pmod_lib$ git clone https://github
.com/Digilent/vivado-library.git
Cloning into 'vivado-library'...
remote: Counting objects: 7473, done.
remote: Compressing objects: 100% (106/106), done.
Receiving objects: 1% (136/7473), 740.00 KiB | 235.00 KiB/s


Flow Navigator
Project Manager
Project Settings
Add Sources
Language Templates
IP Catalog
IP Integrator
Create Block Design
Open Block Design
Generate Block Design
Simulation
Simulation Settings
Run Simulation
RTL Analysis
Elaboration Settings
Open Elaborated Design
Synthesis
Synthesis Settings
Project Manager - pmodCAN
Sources
Design Sources
Constraints
Simulation Sources
sim_1
Hierarchy
Properties
Project Summ
Project Setti
Project name:
Project locatio
Product family:
Project part:
Top module na
Create Block Design
Please specify name of block design.
Design name:
cantest
Directory:
<Local to Project>
Specify source set:
Design Sources
OK
Cancel

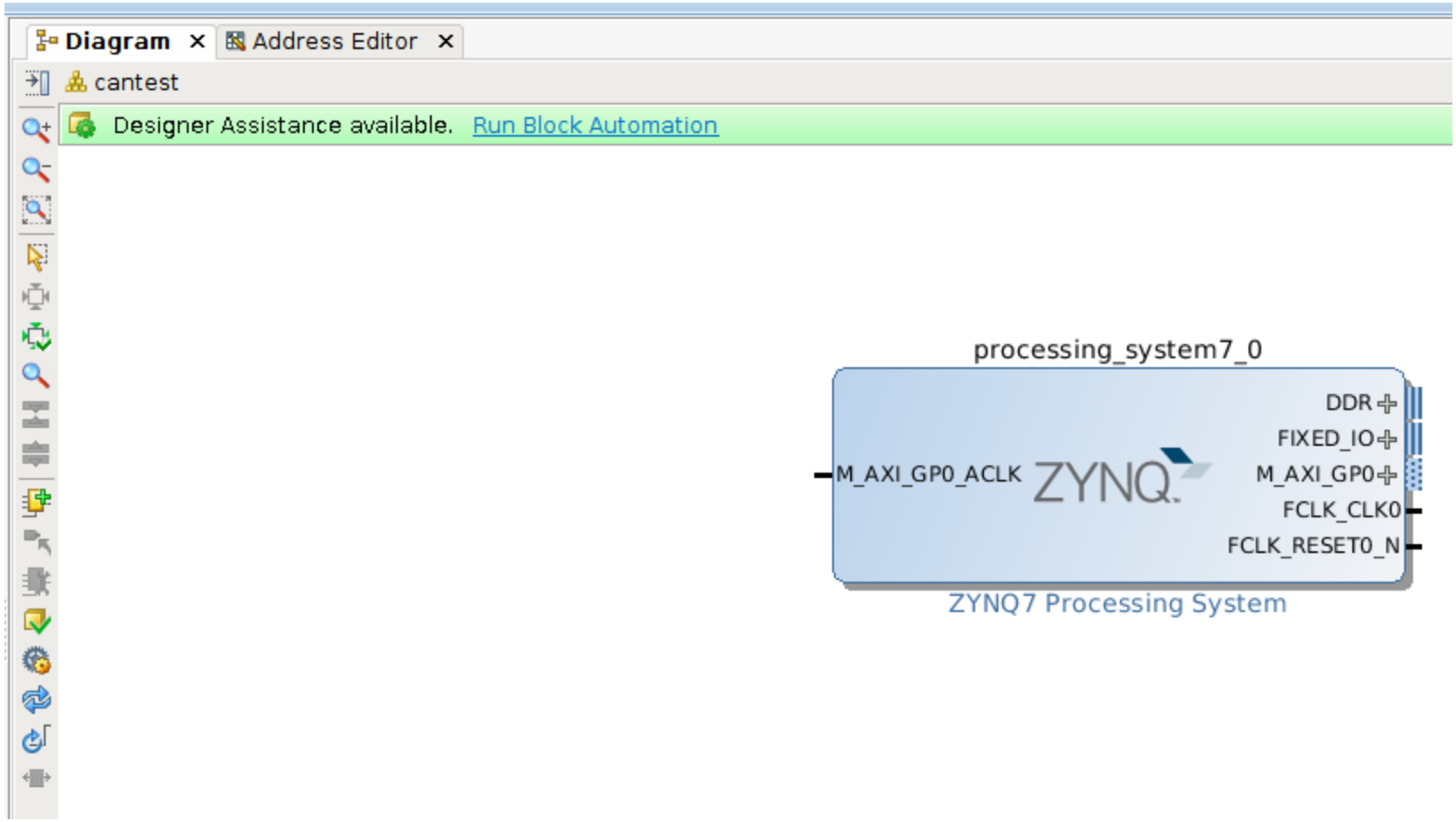


Diagram
Address Editor
cantest
Designer Assistance available.
Run Block Automation
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System

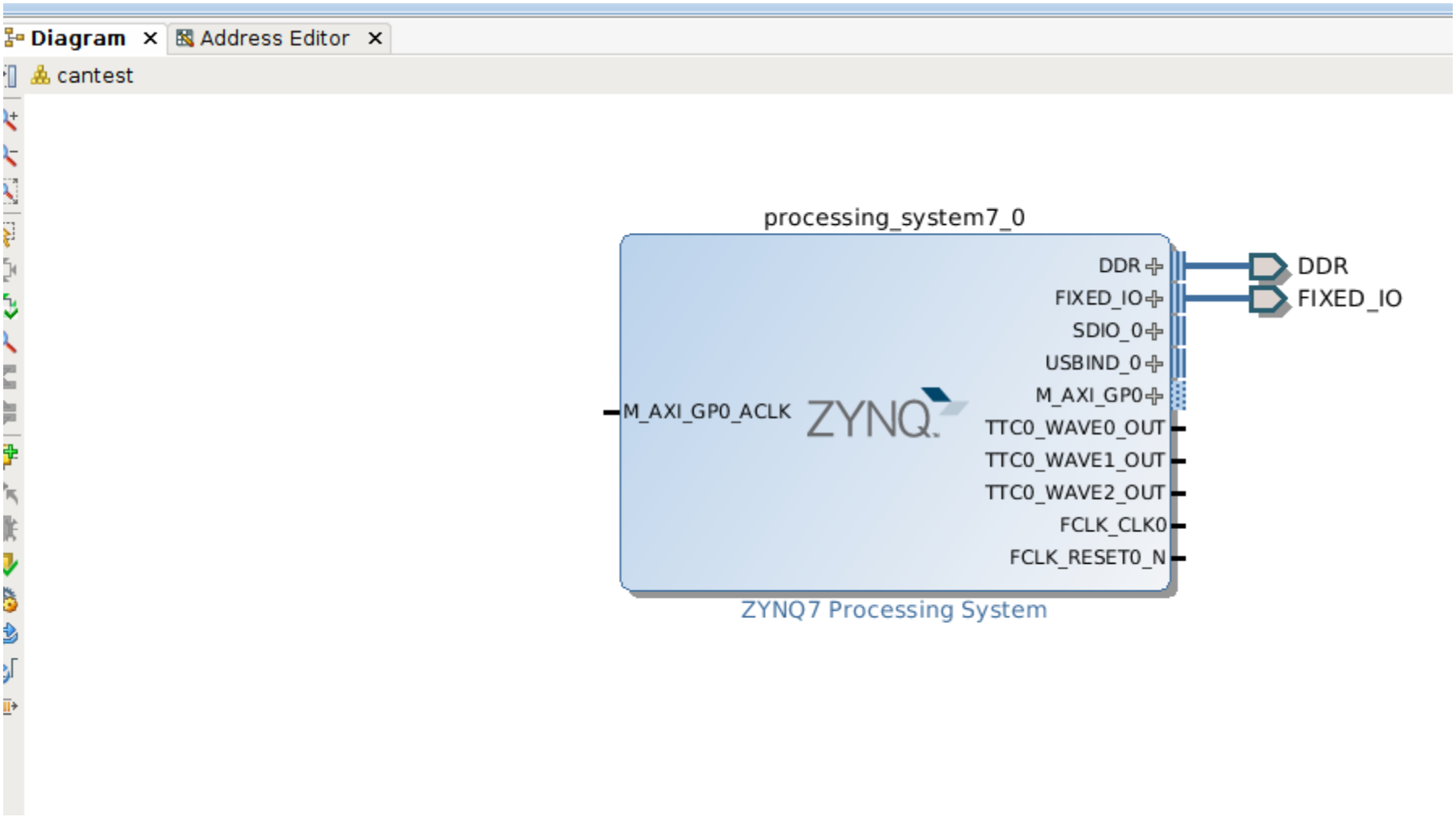
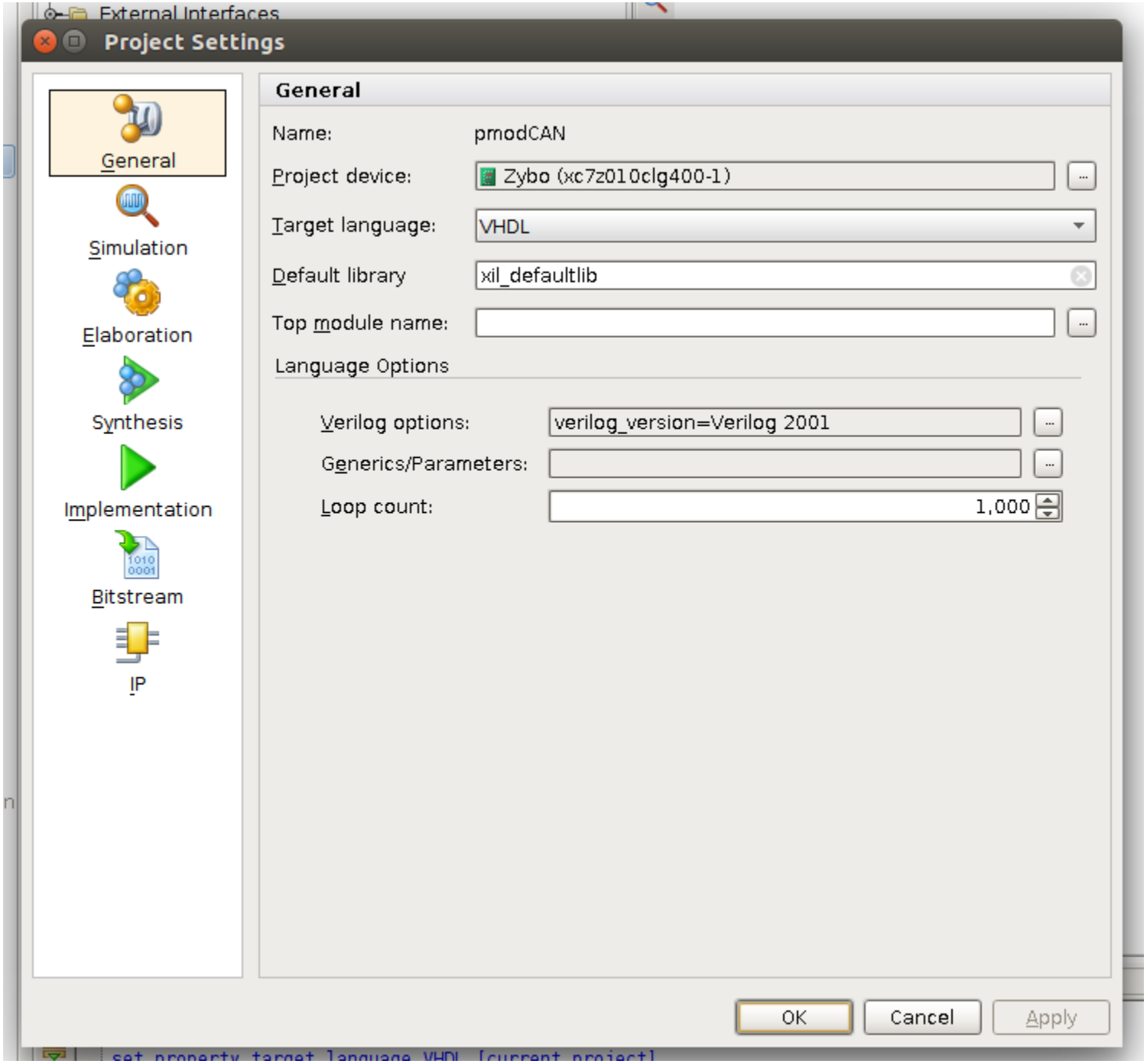
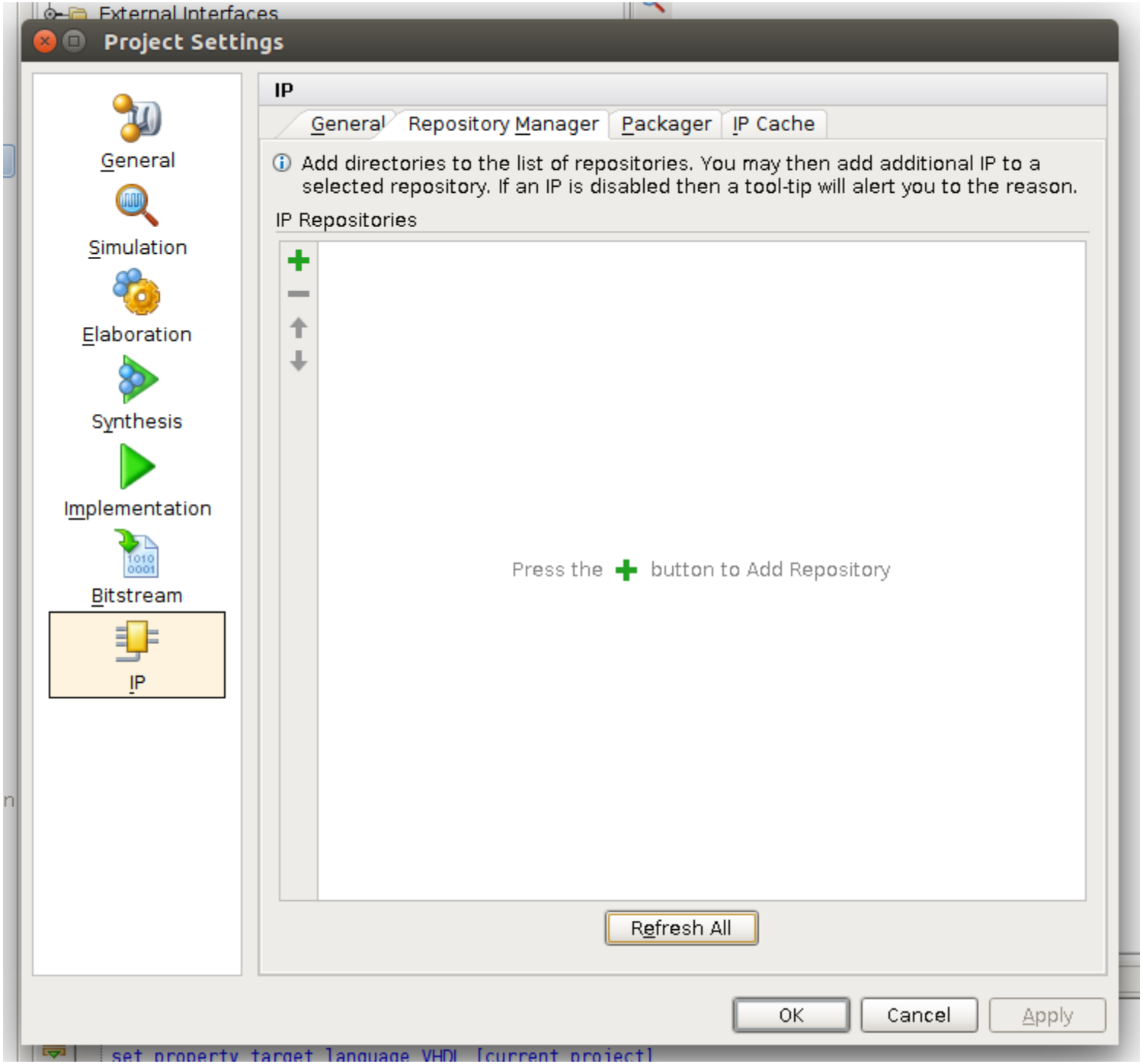
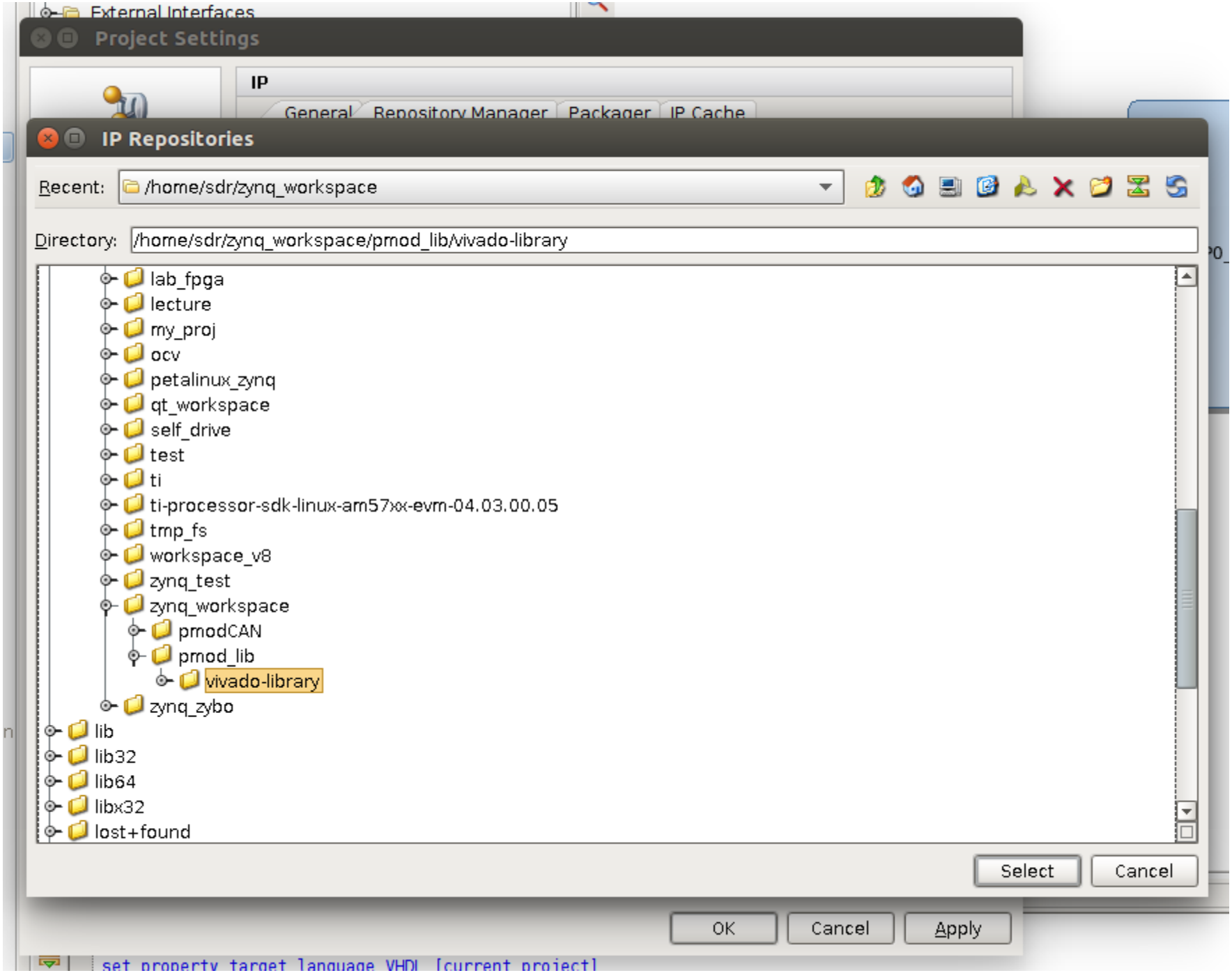
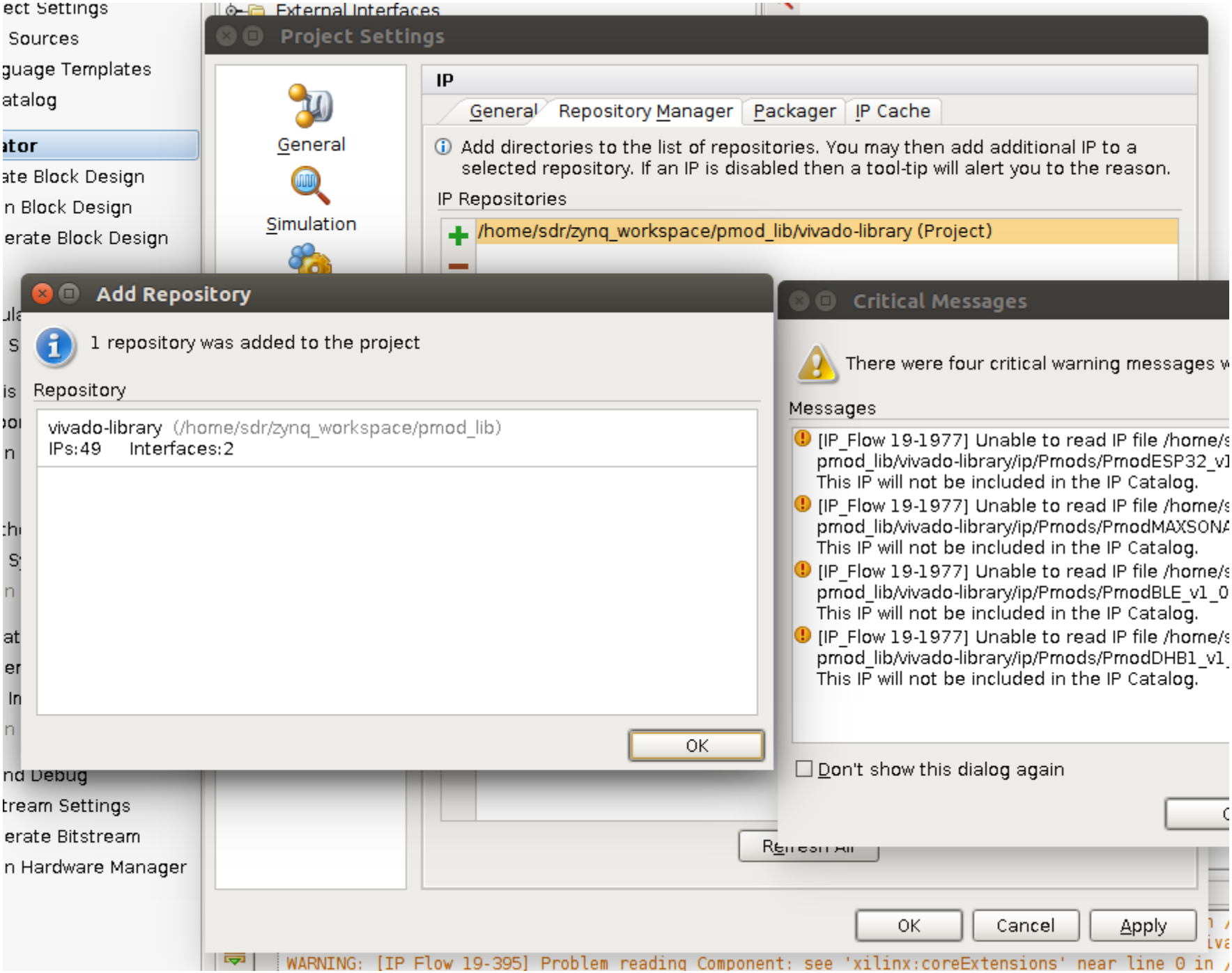


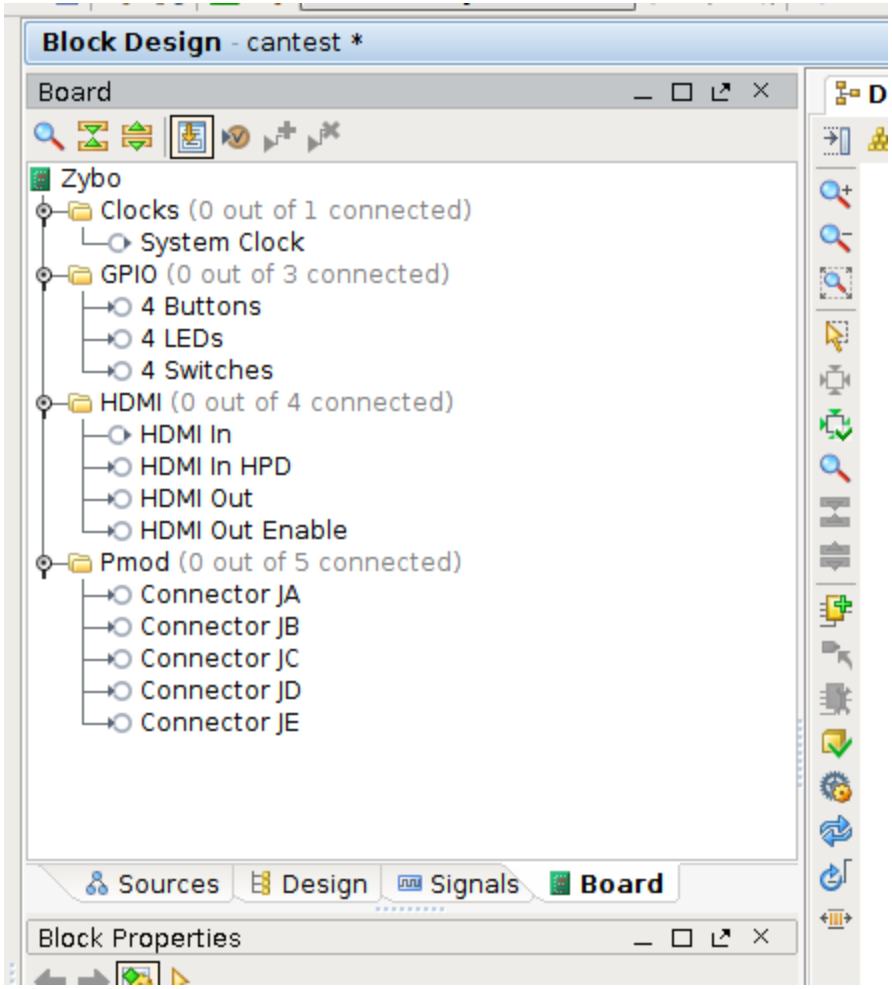
Diagram
Address Editor
cantest
processing_system7_0
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
ZYNQ7 Processing System

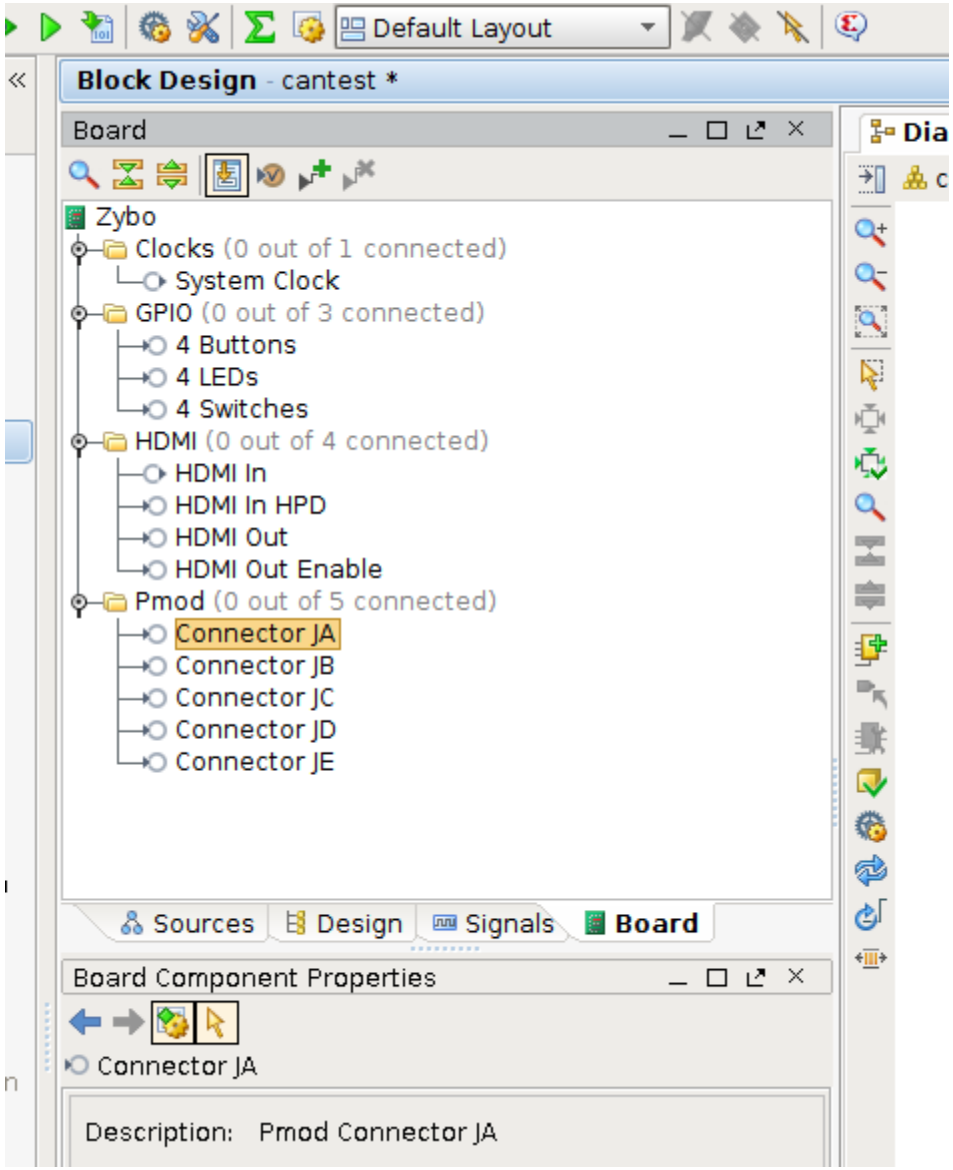

External Interfaces
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
General
Name:
pmodCAN
Project device:
Zybo (xc7z010clg400-1)
Target language:
VHDL
Default library
xil_defaultlib
Top module name:
Language Options
Verilog options:
verilog_version=Verilog 2001
Generics/Parameters:
Loop count:
1,000
OK
Cancel
Apply

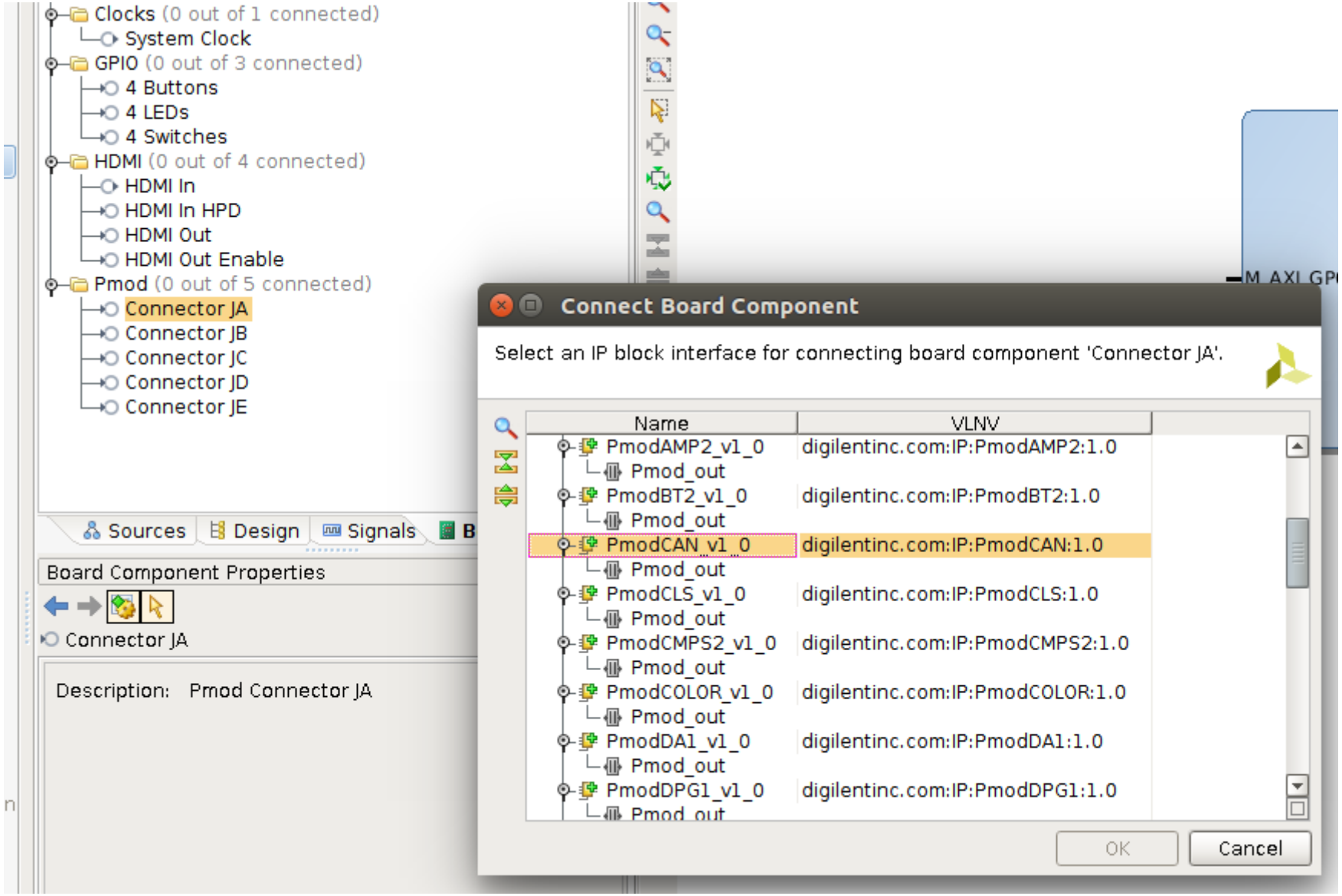

External Interfaces
Project Settings
General
Simulation
Elaboration
Synthesis
Implementation
Bitstream
IP
IP
General
Repository Manager
Packager
IP Cache
Add directories to the list of repositories. You may then add additional IP to a selected repository. If an IP is disabled then a tool-tip will alert you to the reason.
IP Repositories
Press the + button to Add Repository
Refresh All
OK
Cancel
Apply
set property target_language VHDL [current_project]


External Interfaces
Project Settings
IP
General
Repository Manager
Packager
IP Cache
IP Repositories
Recent:
/home/sdr/zynq_workspace
Directory:
/home/sdr/zynq_workspace/pmod_lib/vivado-library
lab_fpga
lecture
my_proj
ocv
petalinux_zynq
qt_workspace
self_drive
test
ti
ti-processor-sdk-linux-am57xx-evm-04.03.00.05
tmp_fs
workspace_v8
zynq_test
zynq_workspace
pmodCAN
pmod_lib
vivado-library
zynq_zybo
lib
lib32
lib64
libx32
lost+found
Select
Cancel
OK
Cancel
Apply
set property target language VHDL [current project]


Project Settings
General
Simulation
IP
General
Repository Manager
Packager
IP Cache
Add directories to the list of repositories. You may then add additional IP to a selected repository. If an IP is disabled then a tool-tip will alert you to the reason.
IP Repositories
/home/sdr/zynq_workspace/pmod_lib/vivado-library (Project)
Add Repository
1 repository was added to the project
Repository
vivado-library (/home/sdr/zynq_workspace/pmod_lib)
IPs:49 Interfaces:2
OK
Critical Messages
There were four critical warning messages w
Messages
[IP_Flow 19-1977] Unable to read IP file /home/s
pmod_lib/vivado-library/ip/Pmods/PmodESP32_v1
This IP will not be included in the IP Catalog.
[IP_Flow 19-1977] Unable to read IP file /home/s
pmod_lib/vivado-library/ip/Pmods/PmodMAXSONA
This IP will not be included in the IP Catalog.
[IP_Flow 19-1977] Unable to read IP file /home/s
pmod_lib/vivado-library/ip/Pmods/PmodBLE_v1_0
This IP will not be included in the IP Catalog.
[IP_Flow 19-1977] Unable to read IP file /home/s
pmod_lib/vivado-library/ip/Pmods/PmodDHB1_v1_
This IP will not be included in the IP Catalog.
Don't show this dialog again
OK
Cancel
Apply
WARNING: [IP Flow 19-395] Problem reading Component: see 'xilinx:coreExtensions' near line 0 in


Block Design - cantest *
Board
Zybo
Clocks (0 out of 1 connected)
System Clock
GPIO (0 out of 3 connected)
4 Buttons
4 LEDs
4 Switches
HDMI (0 out of 4 connected)
HDMI In
HDMI In HPD
HDMI Out
HDMI Out Enable
Pmod (0 out of 5 connected)
Connector JA
Connector JB
Connector JC
Connector JD
Connector JE
Sources
Design
Signals
Board
Block Properties


Default Layout
Block Design - cantest *
Board
Zybo
Clocks (0 out of 1 connected)
System Clock
GPIO (0 out of 3 connected)
4 Buttons
4 LEDs
4 Switches
HDMI (0 out of 4 connected)
HDMI In
HDMI In HPD
HDMI Out
HDMI Out Enable
Pmod (0 out of 5 connected)
Connector JA
Connector JB
Connector JC
Connector JD
Connector JE
Sources
Design
Signals
Board
Board Component Properties
Connector JA
Description: Pmod Connector JA


Clocks (0 out of 1 connected)
System Clock
GPIO (0 out of 3 connected)
4 Buttons
4 LEDs
4 Switches
HDMI (0 out of 4 connected)
HDMI In
HDMI In HPD
HDMI Out
HDMI Out Enable
Pmod (0 out of 5 connected)
Connector JA
Connector JB
Connector JC
Connector JD
Connector JE
Sources
Design
Signals
Board Component Properties
Connector JA
Description: Pmod Connector JA
Connect Board Component
Select an IP block interface for connecting board component 'Connector JA'.
Name
VLNV
PmodAMP2_v1_0
digilentinc.com:IP:PmodAMP2:1.0
Pmod_out
PmodBT2_v1_0
digilentinc.com:IP:PmodBT2:1.0
Pmod_out
PmodCAN_v1_0
digilentinc.com:IP:PmodCAN:1.0
Pmod_out
PmodCLS_v1_0
digilentinc.com:IP:PmodCLS:1.0
Pmod_out
PmodCMPS2_v1_0
digilentinc.com:IP:PmodCMPS2:1.0
Pmod_out
PmodCOLOR_v1_0
digilentinc.com:IP:PmodCOLOR:1.0
Pmod_out
PmodDA1_v1_0
digilentinc.com:IP:PmodDA1:1.0
Pmod_out
PmodDPG1_v1_0
digilentinc.com:IP:PmodDPG1:1.0
Pmod_out
OK
Cancel

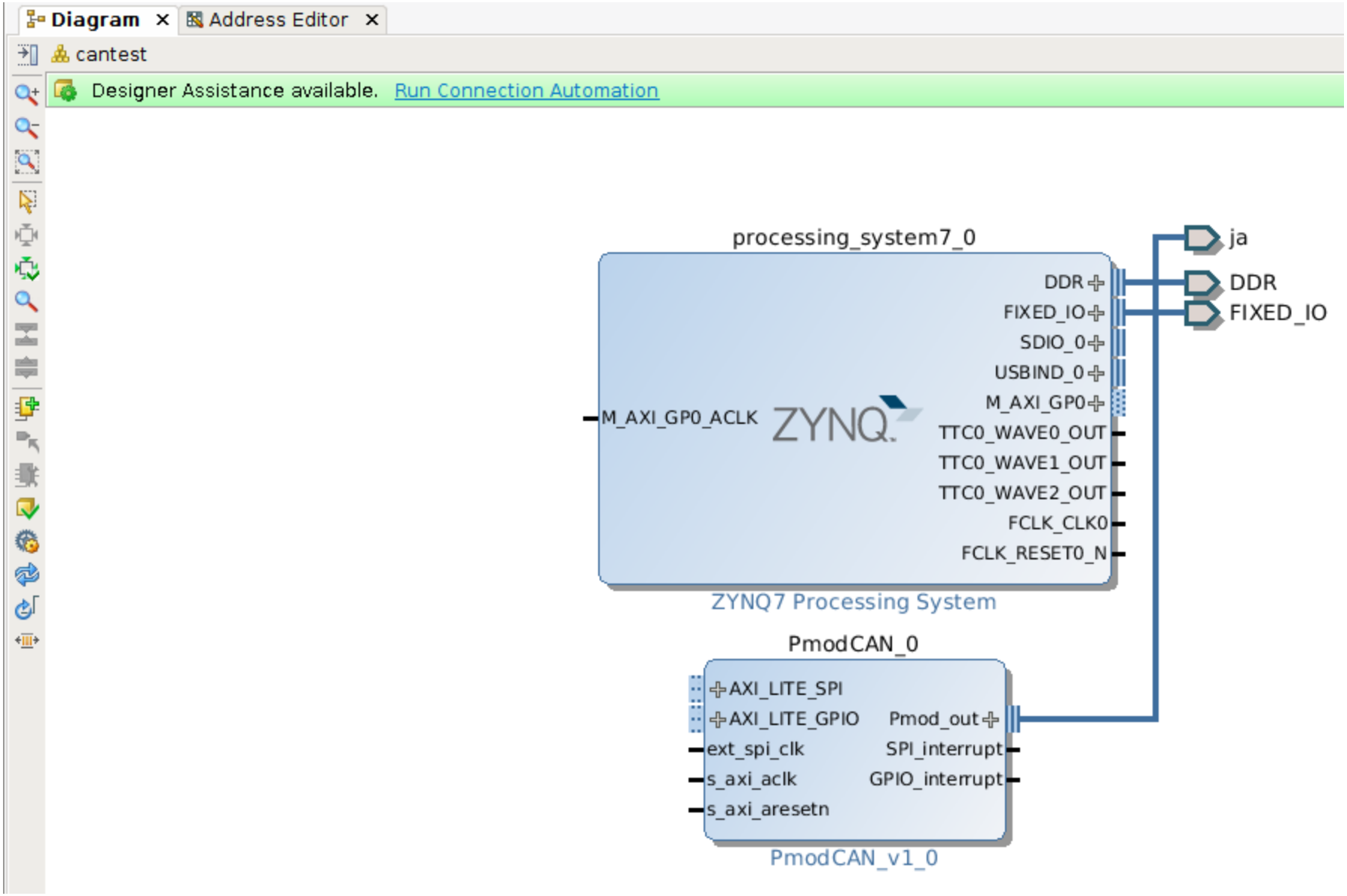
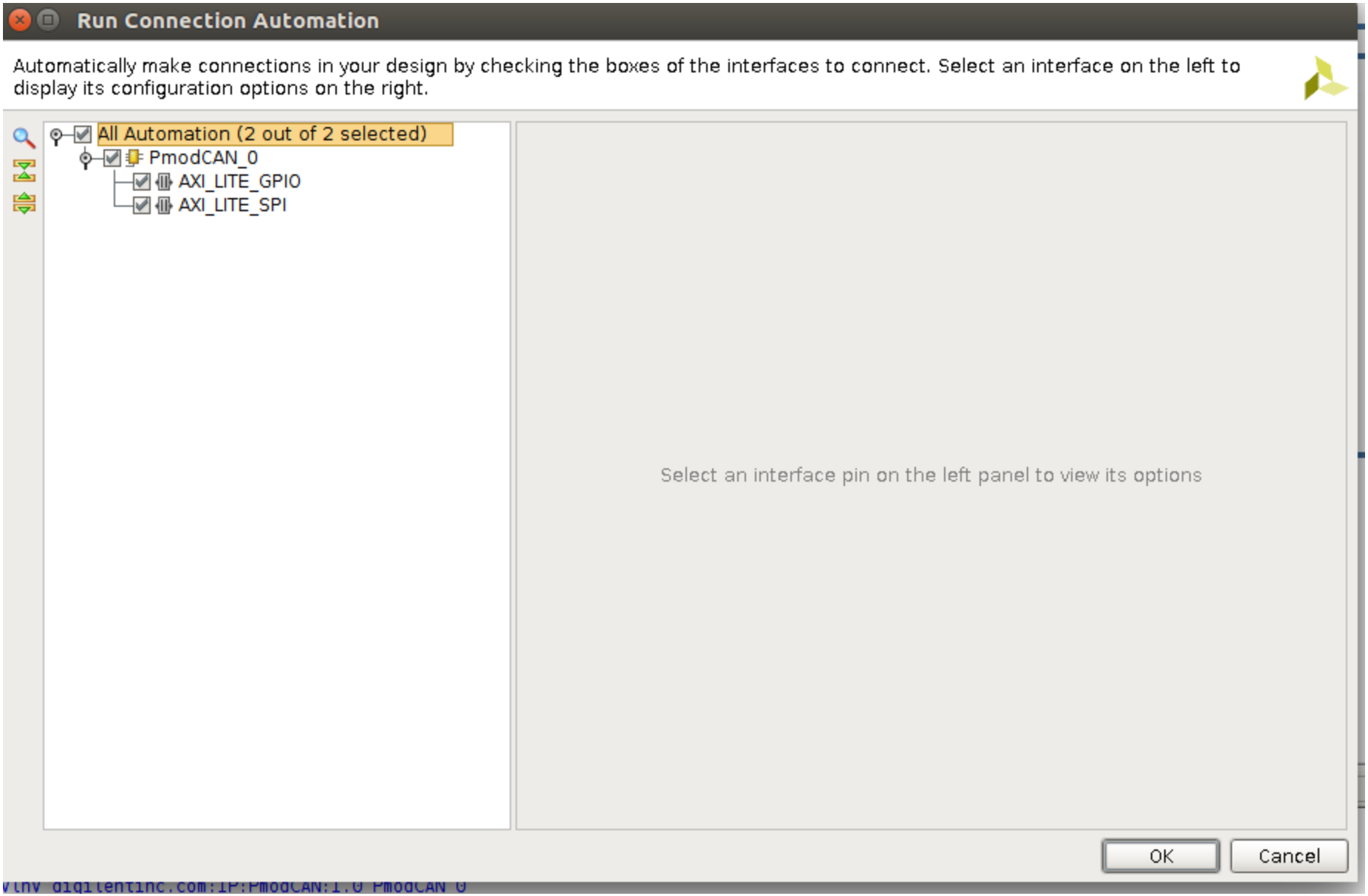
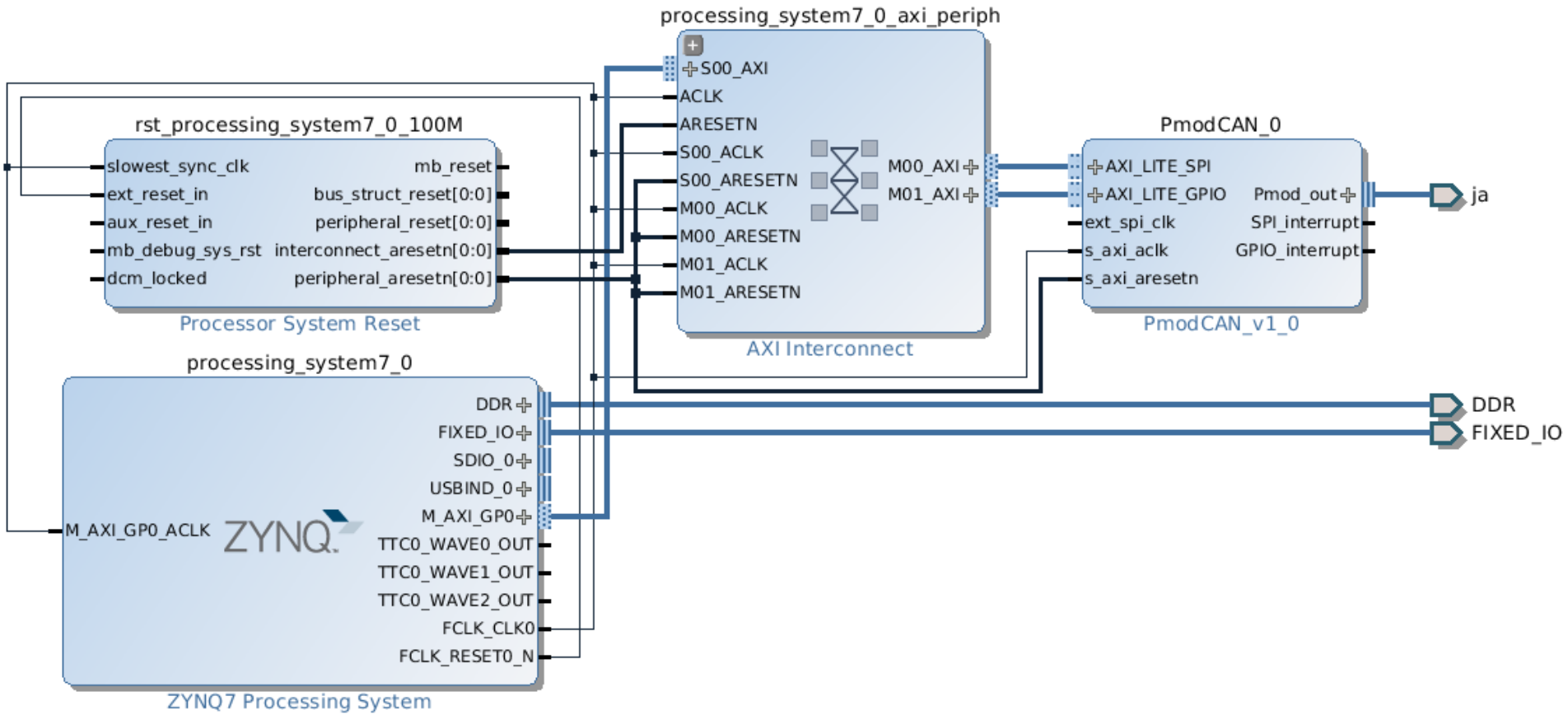


Diagram
Address Editor
cantest
Designer Assistance available.
Run Connection Automation
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
ja
DDR
FIXED_IO
PmodCAN_0
AXI_LITE_SPI
AXI_LITE_GPIO
ext_spi_clk
s_axi_aclk
s_axi_aresetn
Pmod_out
SPI_interrupt
GPIO_interrupt
PmodCAN_v1_0


Run Connection Automation
Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.
All Automation (2 out of 2 selected)
PmodCAN_0
AXI_LITE_GPIO
AXI_LITE_SPI
Select an interface pin on the left panel to view its options
OK
Cancel


processing_system7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
rst_processing_system7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
PmodCAN_0
AXI_LITE_SPI
AXI_LITE_GPIO
ext_spi_clk
s_axi_aclk
s_axi_aresetn
Pmod_out
SPI_interrupt
GPIO_interrupt
PmodCAN_v1_0
ja
processing_system7_0
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
M_AXI_GP0_ACLK
ZYNQ
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO

Pmods Supported

Pmod	Interface Type	Reference clock frequency (MHz)	Reference Clock signal name	Interrupt pin name/s	Uses PmodGPIO
8LD	GPIO	-	-	-	Yes
ACL	SPI	80	ext_spi_clk	-	-
ACL2	SPI	50	ext_spi_clk	-	-
AD1	SPI	-	-	-	-
AD2	IIC	-	-	-	-
AD5	SPI	50	-	-	-
ALS	SPI	50	ext_spi_clk	-	-
AMP2	GPIO	-	-	timer_interrupt	-
BB	GPIO	-	-	-	Yes
BT2	UART	-	-	-	-
BTN	GPIO	-	-	-	Yes
CAN	SPI	100	ext_spi_clk	SPI_interrupt, GPIO_interrupt	-

Re-customize IP

ZYNQ7 Processing System (5.5)

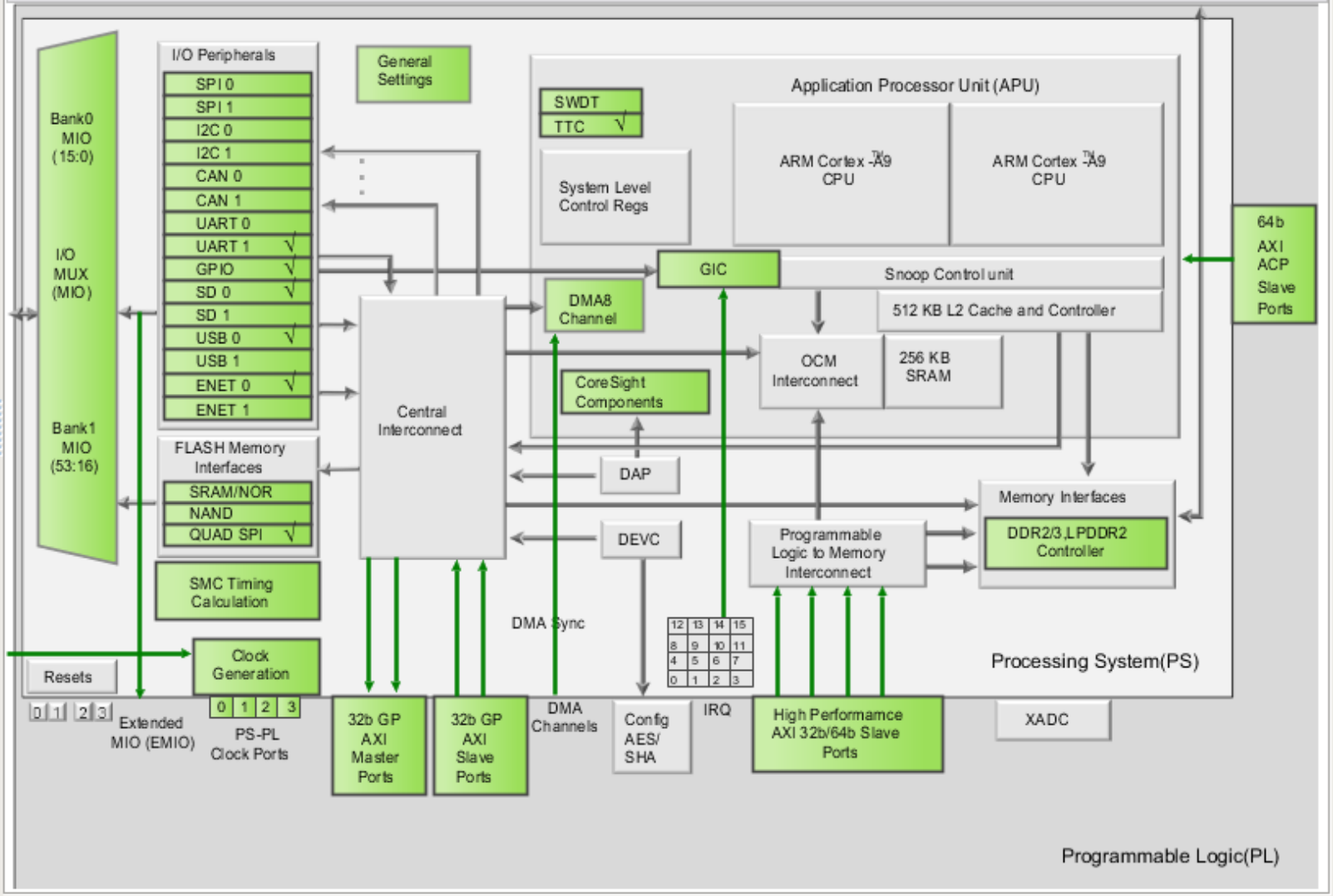
Documentation | Presets | IP Location | Import XPS Settings

Page Navigator

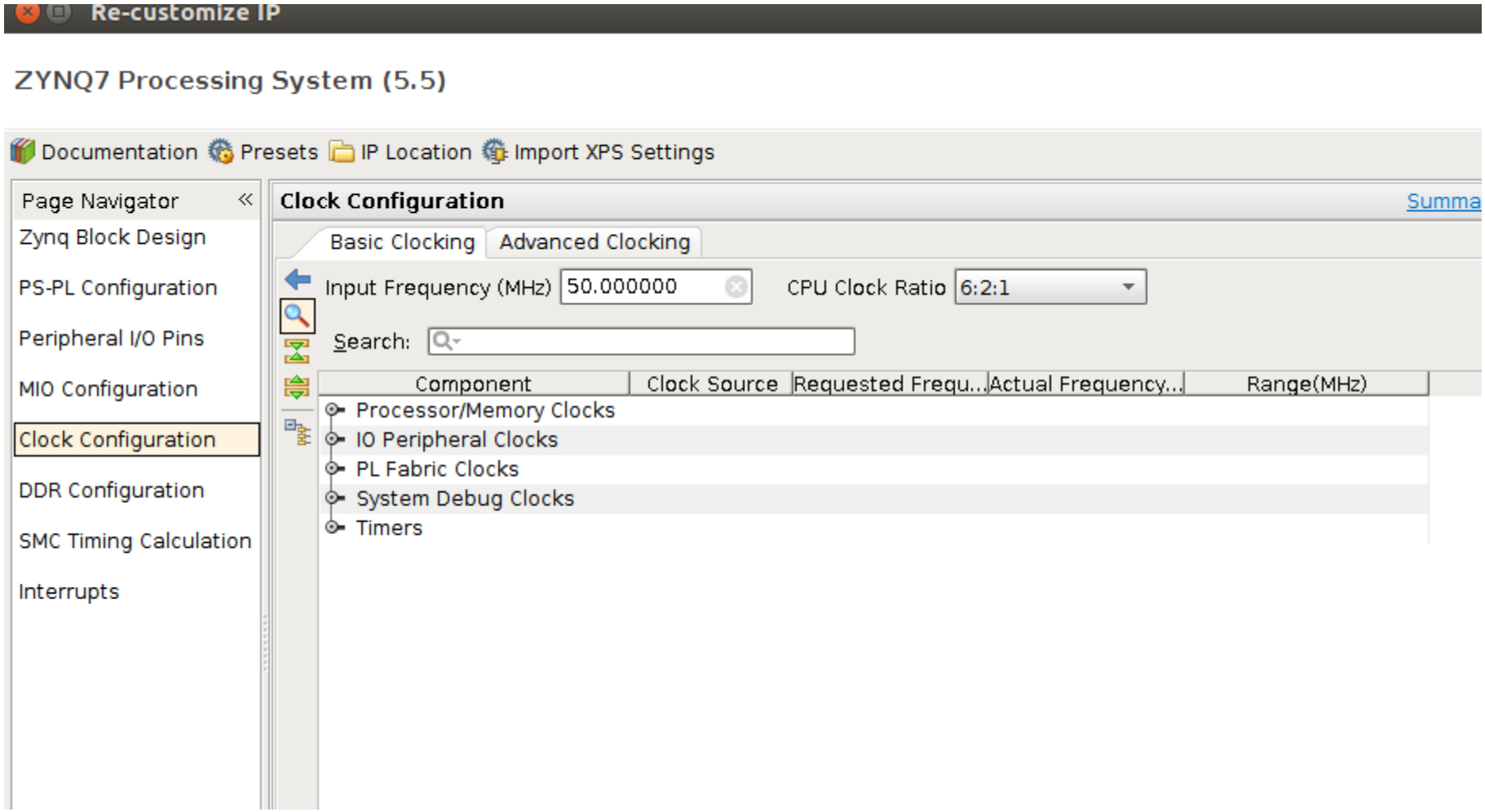
- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

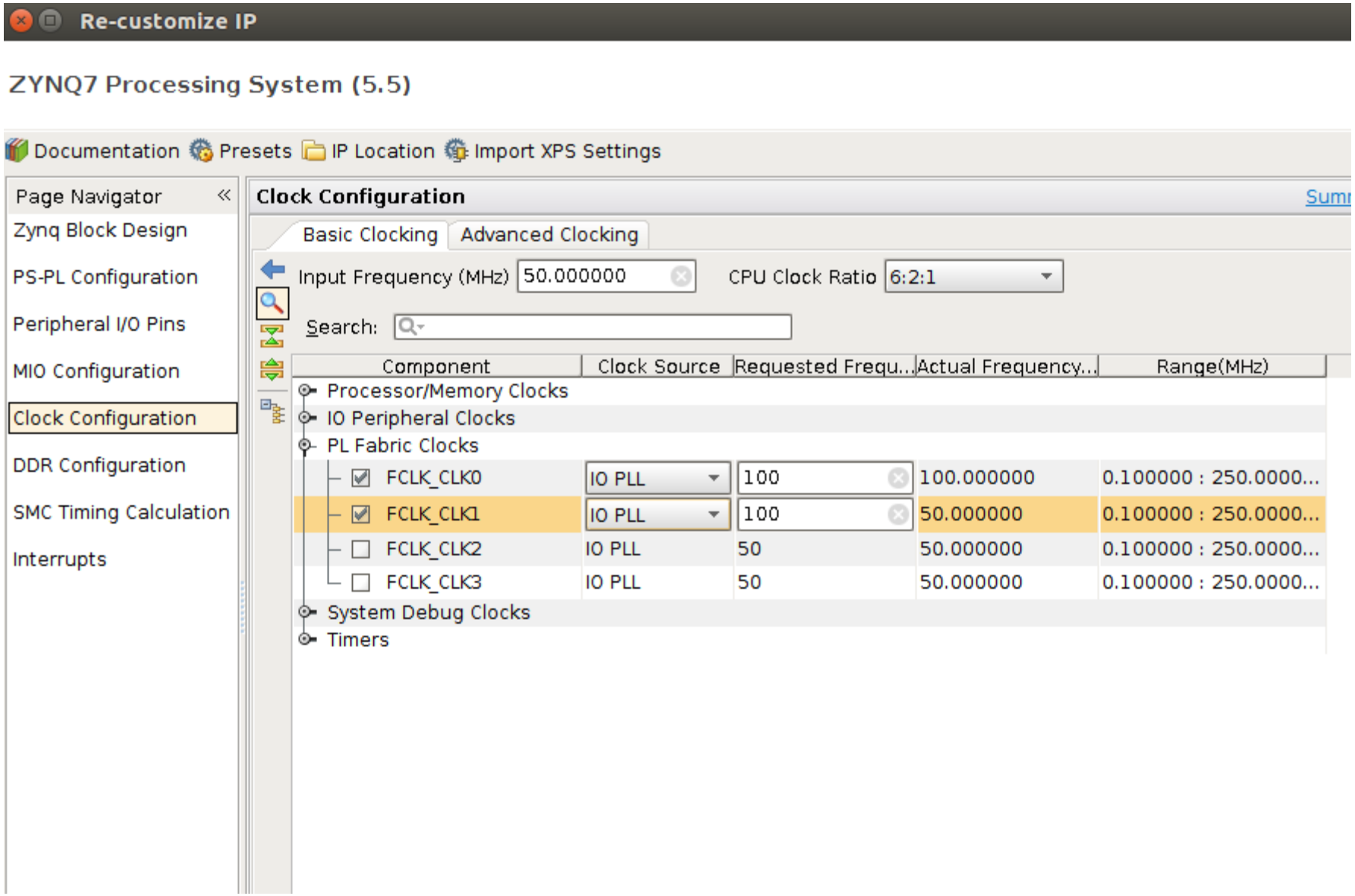
Zynq Block Design

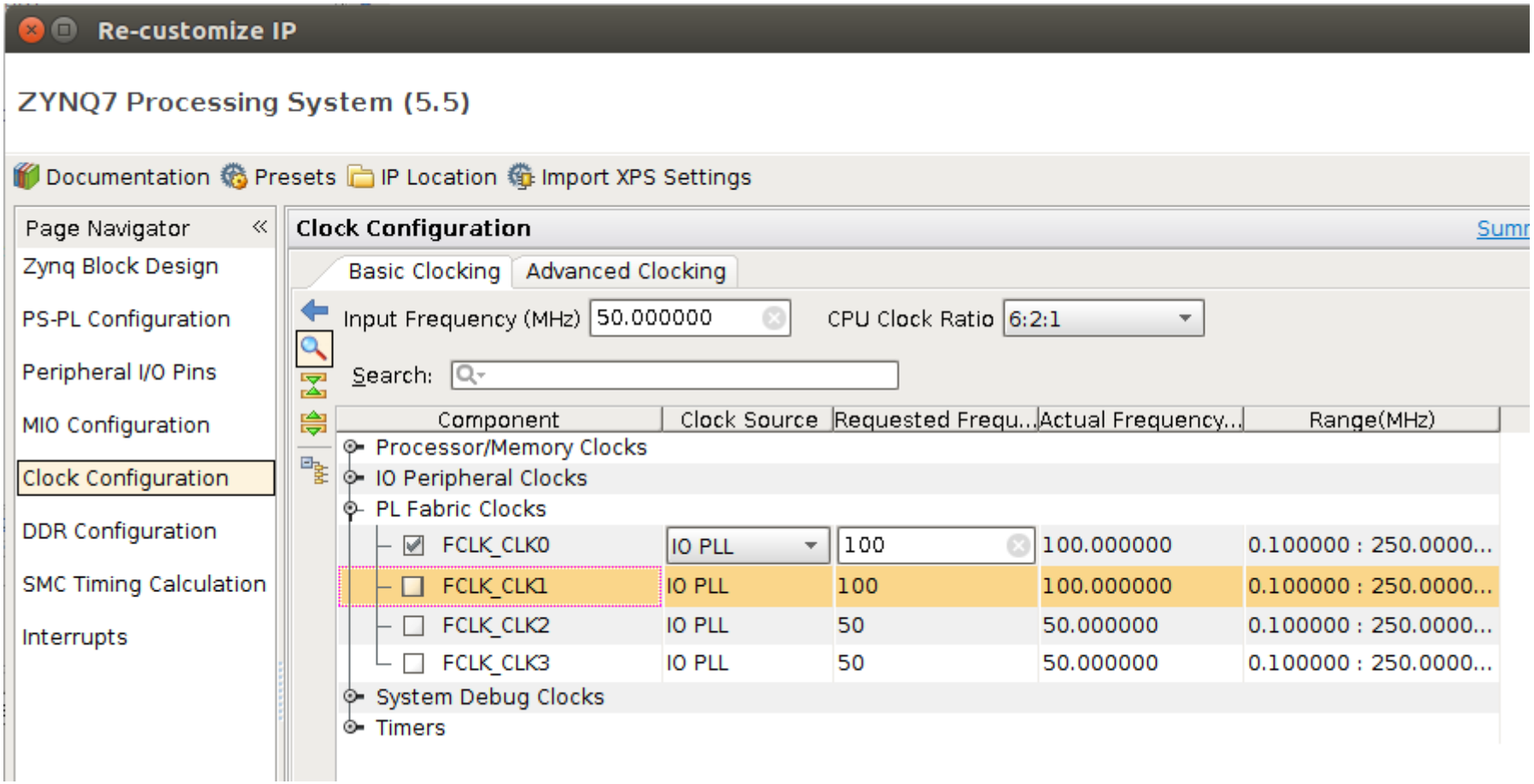
Summary Report

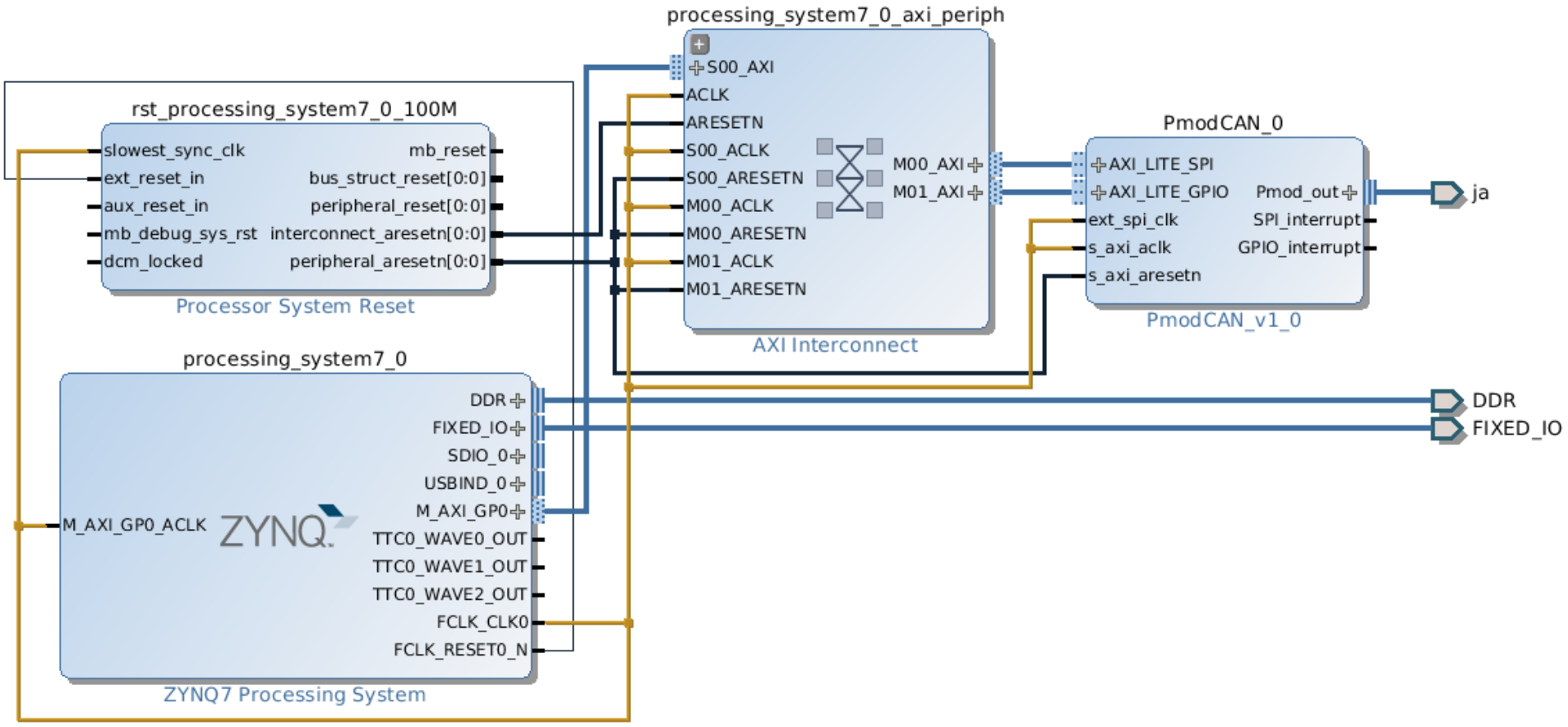


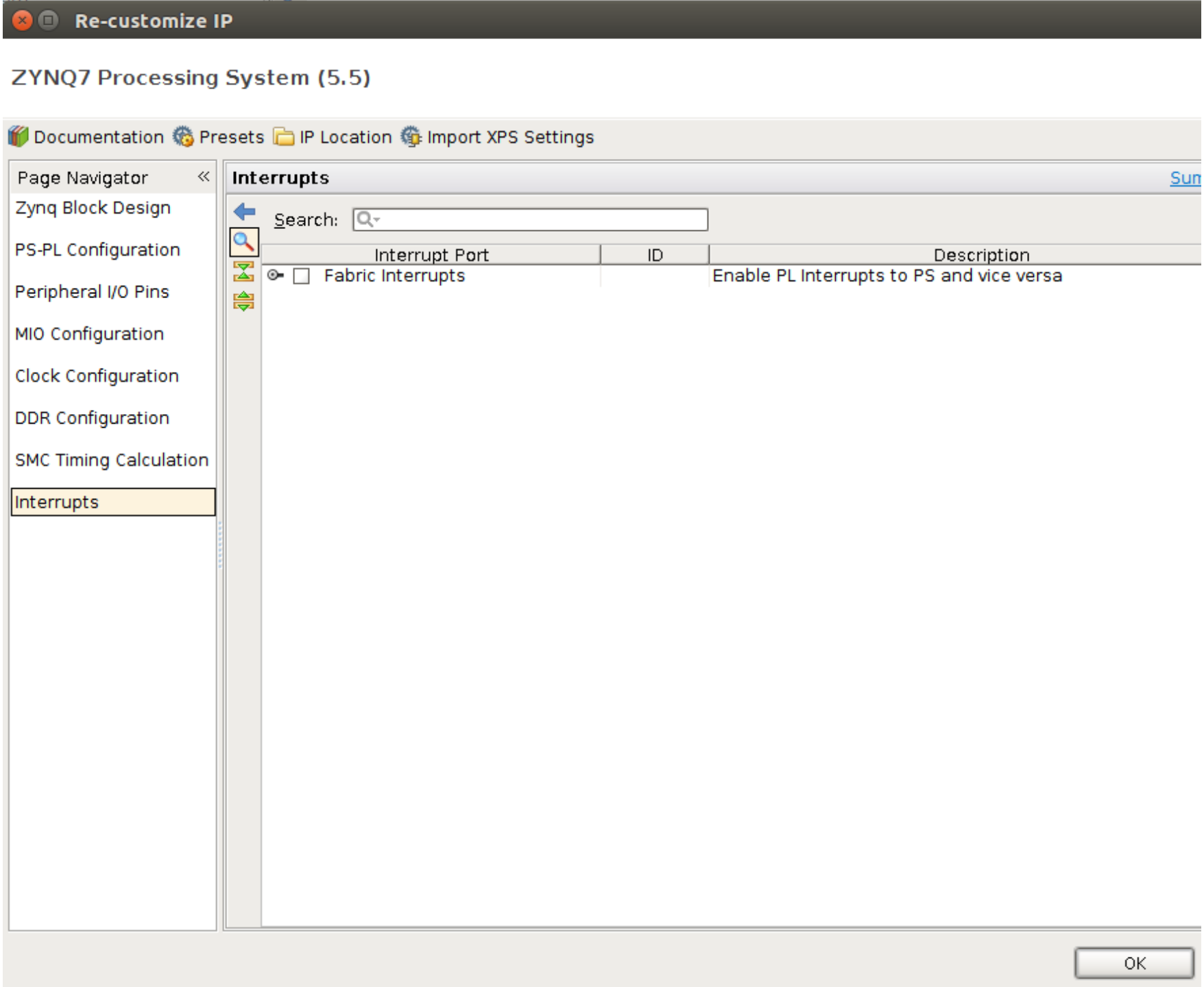
OK | Cancel

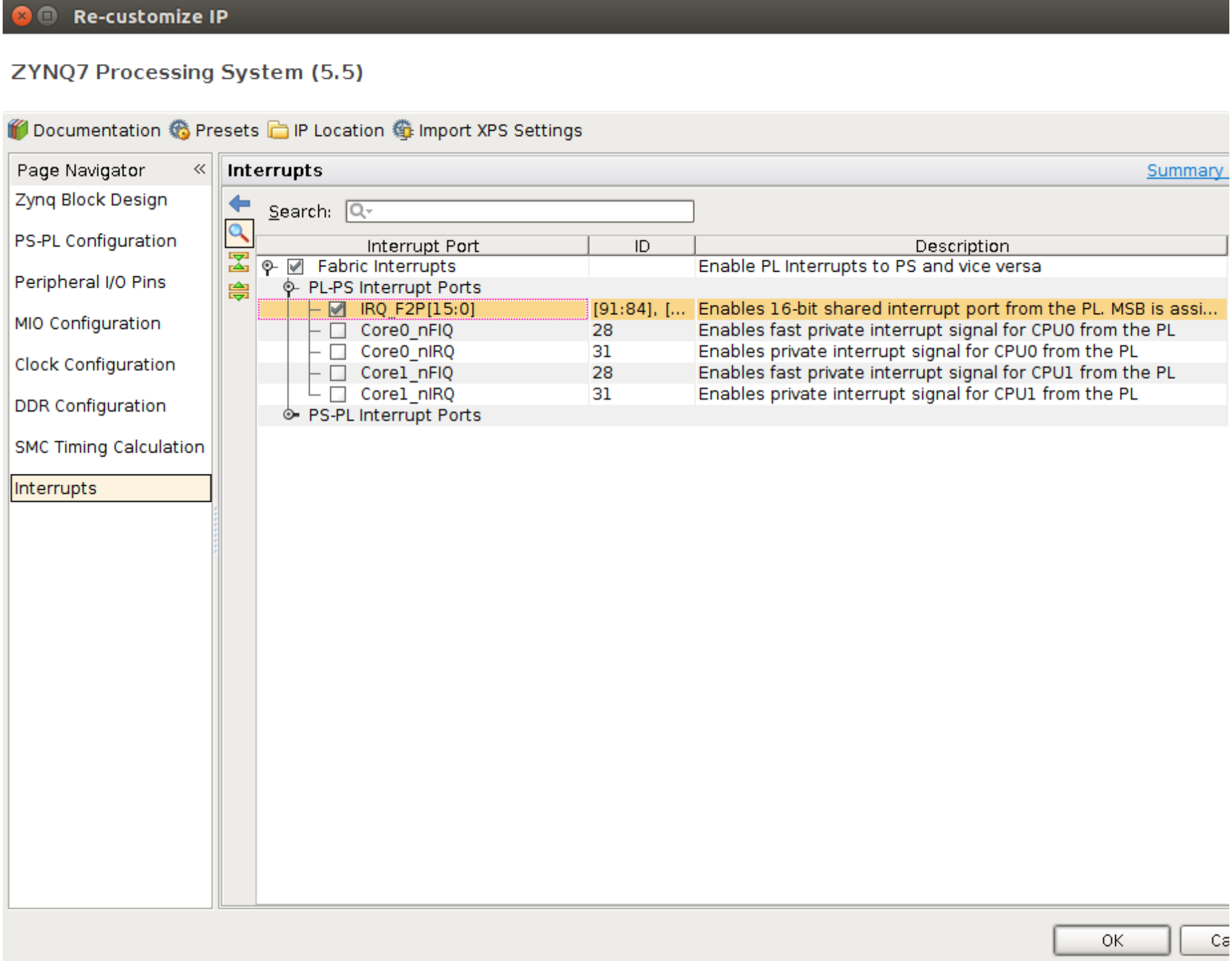

Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Clock Configuration
Summa
Basic Clocking
Advanced Clocking
Input Frequency (MHz)
50.000000
CPU Clock Ratio
6:2:1
Search:
Component
Clock Source
Requested Frequ...
Actual Frequency...
Range(MHz)
Processor/Memory Clocks
IO Peripheral Clocks
PL Fabric Clocks
System Debug Clocks
Timers

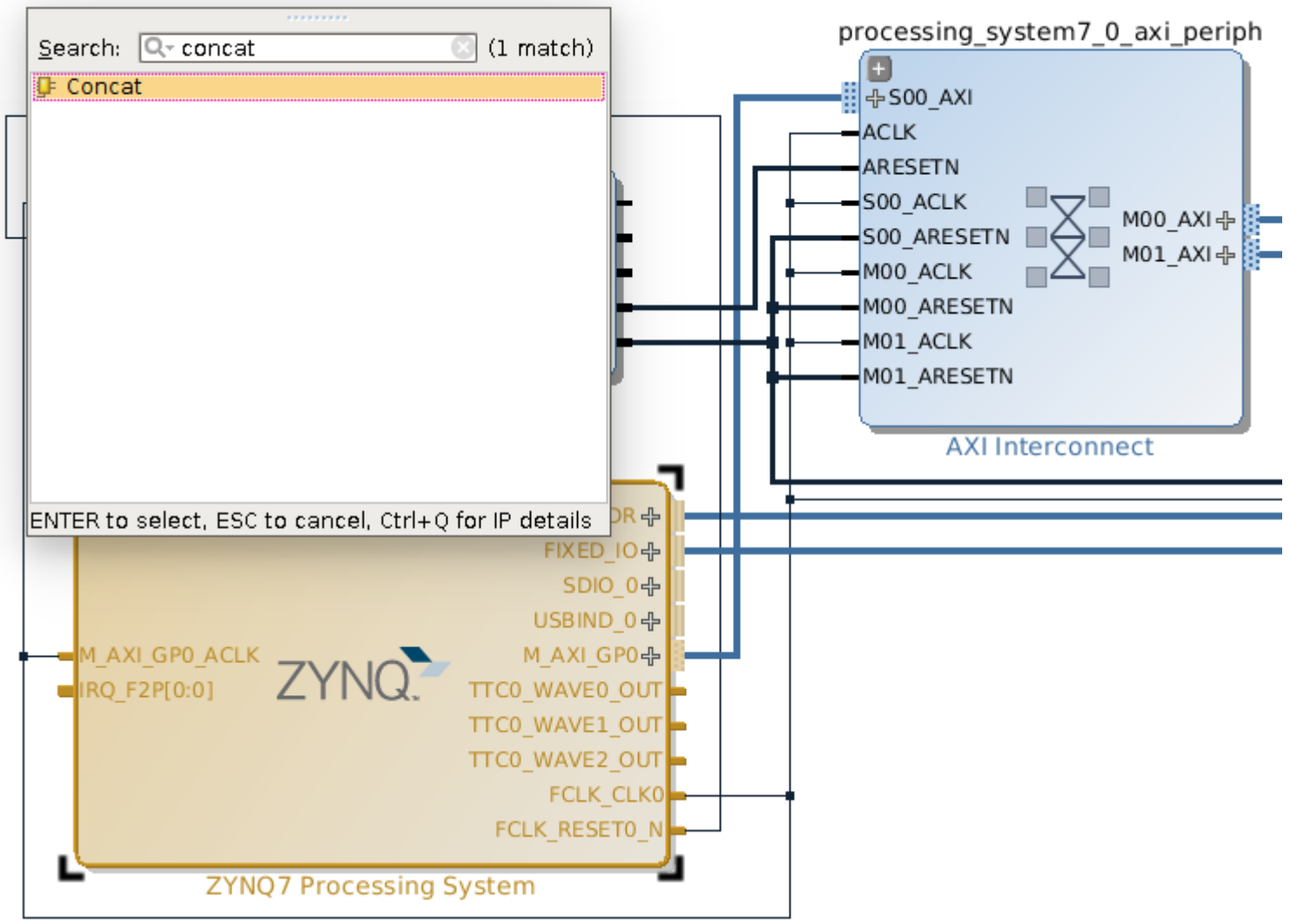

Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Clock Configuration
Basic Clocking
Advanced Clocking
Input Frequency (MHz) 50.000000
CPU Clock Ratio 6:2:1
Search:
Component
Clock Source
Requested Frequ...
Actual Frequency...
Range(MHz)
Processor/Memory Clocks
IO Peripheral Clocks
PL Fabric Clocks
FCLK_CLK0 IO PLL 100 100.000000 0.100000 : 250.0000...
FCLK_CLK1 IO PLL 100 50.000000 0.100000 : 250.0000...
FCLK_CLK2 IO PLL 50 50.000000 0.100000 : 250.0000...
FCLK_CLK3 IO PLL 50 50.000000 0.100000 : 250.0000...
System Debug Clocks
Timers

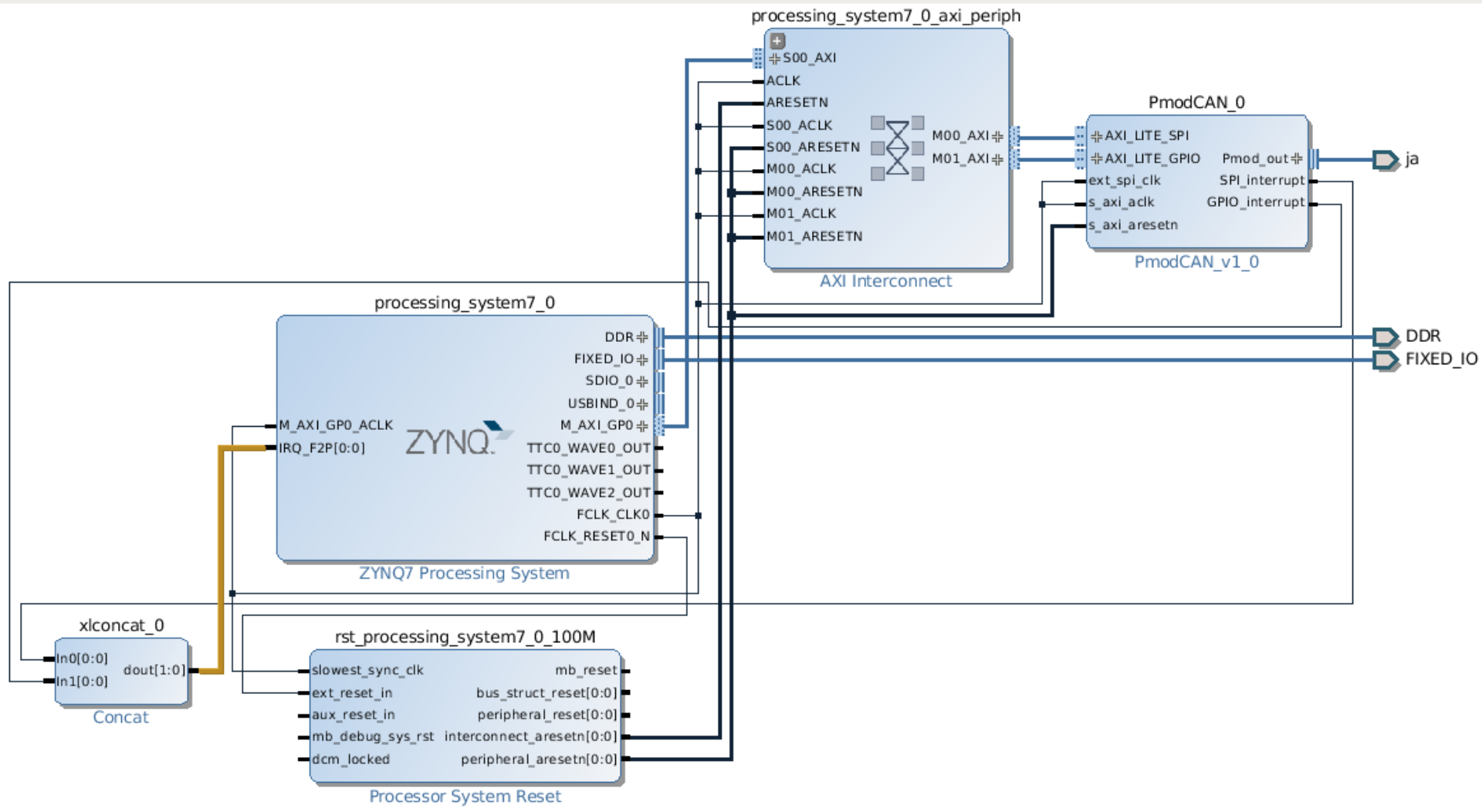

Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Clock Configuration
Basic Clocking
Advanced Clocking
Input Frequency (MHz)
50.000000
CPU Clock Ratio
6:2:1
Search:
Component
Clock Source
Requested Frequ...
Actual Frequency...
Range(MHz)
Processor/Memory Clocks
IO Peripheral Clocks
PL Fabric Clocks
FCLK_CLK0
IO PLL
100
100.000000
0.100000 : 250.0000...
FCLK_CLK1
IO PLL
100
100.000000
0.100000 : 250.0000...
FCLK_CLK2
IO PLL
50
50.000000
0.100000 : 250.0000...
FCLK_CLK3
IO PLL
50
50.000000
0.100000 : 250.0000...
System Debug Clocks
Timers

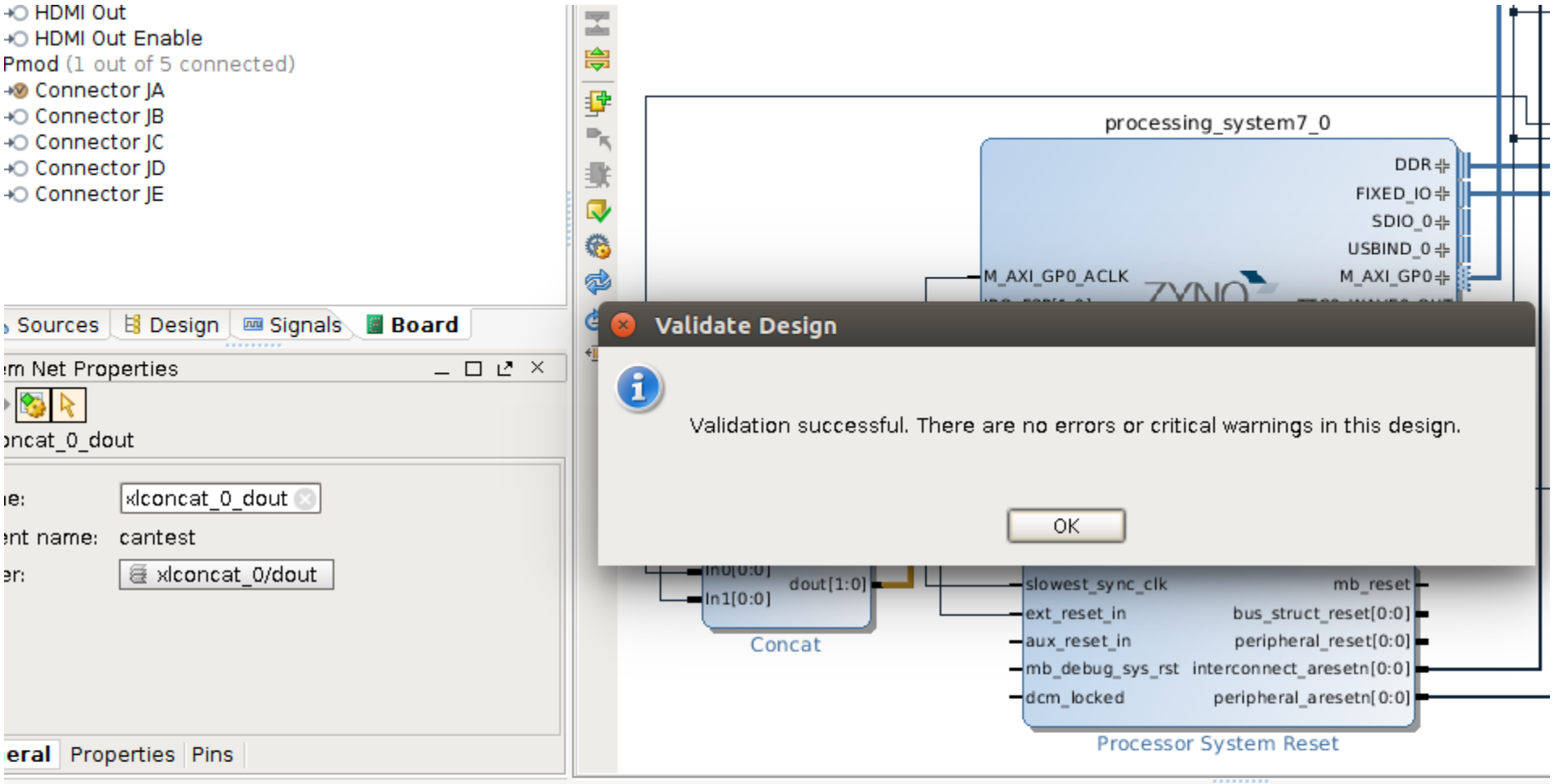

processing_system7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
rst_processing_system7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
PmodCAN_0
AXI_LITE_SPI
AXI_LITE_GPIO
ext_spi_clk
s_axi_aclk
s_axi_aresetn
Pmod_out
SPI_interrupt
GPIO_interrupt
PmodCAN_v1_0
ja
processing_system7_0
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
M_AXI_GP0_ACLK
ZYNQ
ZYNQ7 Processing System
DDR
FIXED_IO


Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Interrupts
Search:
Interrupt Port
ID
Description
Fabric Interrupts
Enable PL Interrupts to PS and vice versa
OK


Re-customize IP
ZYNQ7 Processing System (5.5)
Documentation
Presets
IP Location
Import XPS Settings
Page Navigator
Zynq Block Design
PS-PL Configuration
Peripheral I/O Pins
MIO Configuration
Clock Configuration
DDR Configuration
SMC Timing Calculation
Interrupts
Interrupts
Summary
Search:
Interrupt Port
ID
Description
Fabric Interrupts
Enable PL Interrupts to PS and vice versa
PL-PS Interrupt Ports
IRQ_F2P[15:0]
[91:84], [...
Enables 16-bit shared interrupt port from the PL. MSB is assi...
Core0_nFIQ
28
Enables fast private interrupt signal for CPU0 from the PL
Core0_nIRQ
31
Enables private interrupt signal for CPU0 from the PL
Core1_nFIQ
28
Enables fast private interrupt signal for CPU1 from the PL
Core1_nIRQ
31
Enables private interrupt signal for CPU1 from the PL
PS-PL Interrupt Ports
OK
Ca

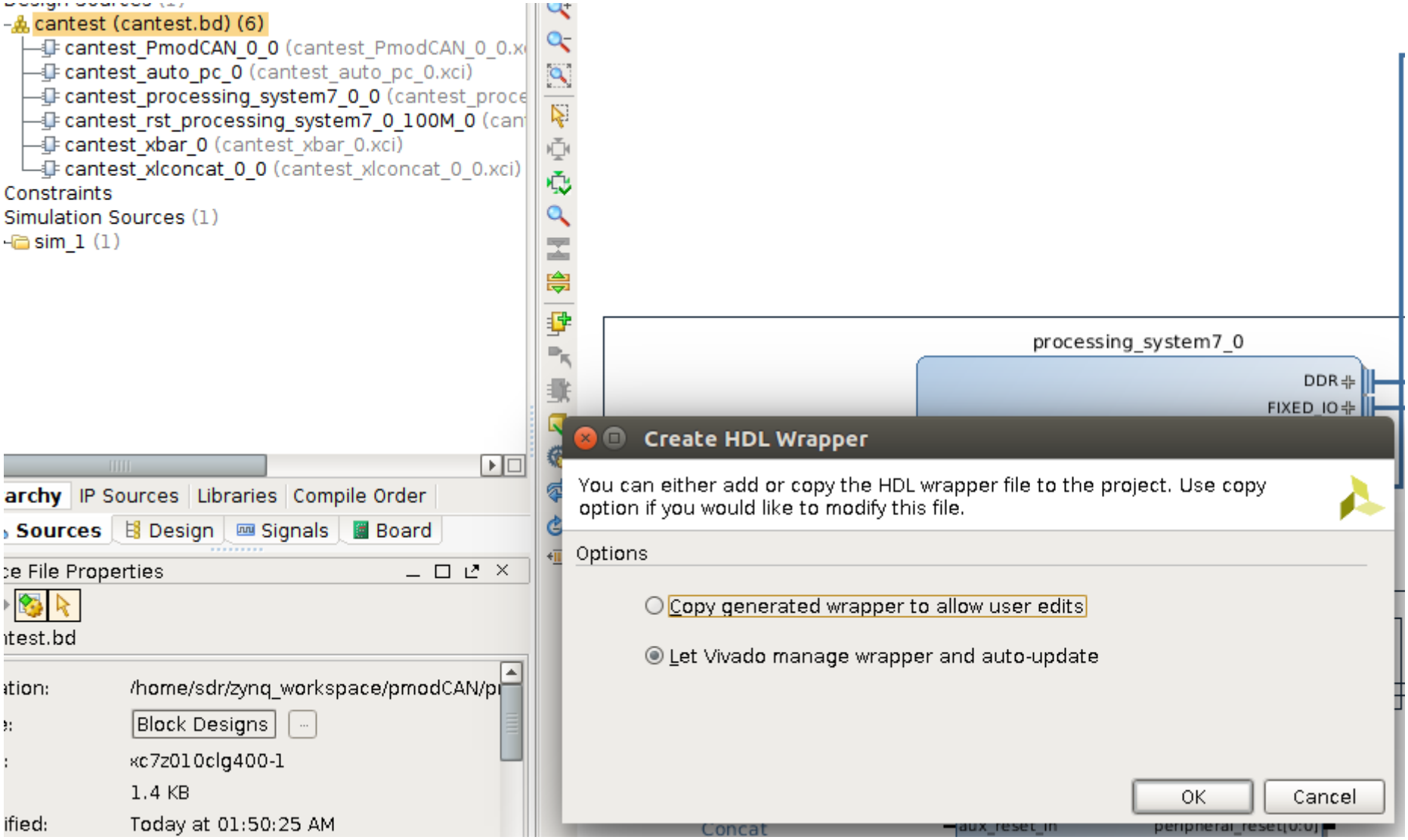

Search: concat (1 match)
Concat
ENTER to select, ESC to cancel, Ctrl+Q for IP details
processing_system7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0_ACLK
IRQ_F2P[0:0]
ZYNQ
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System

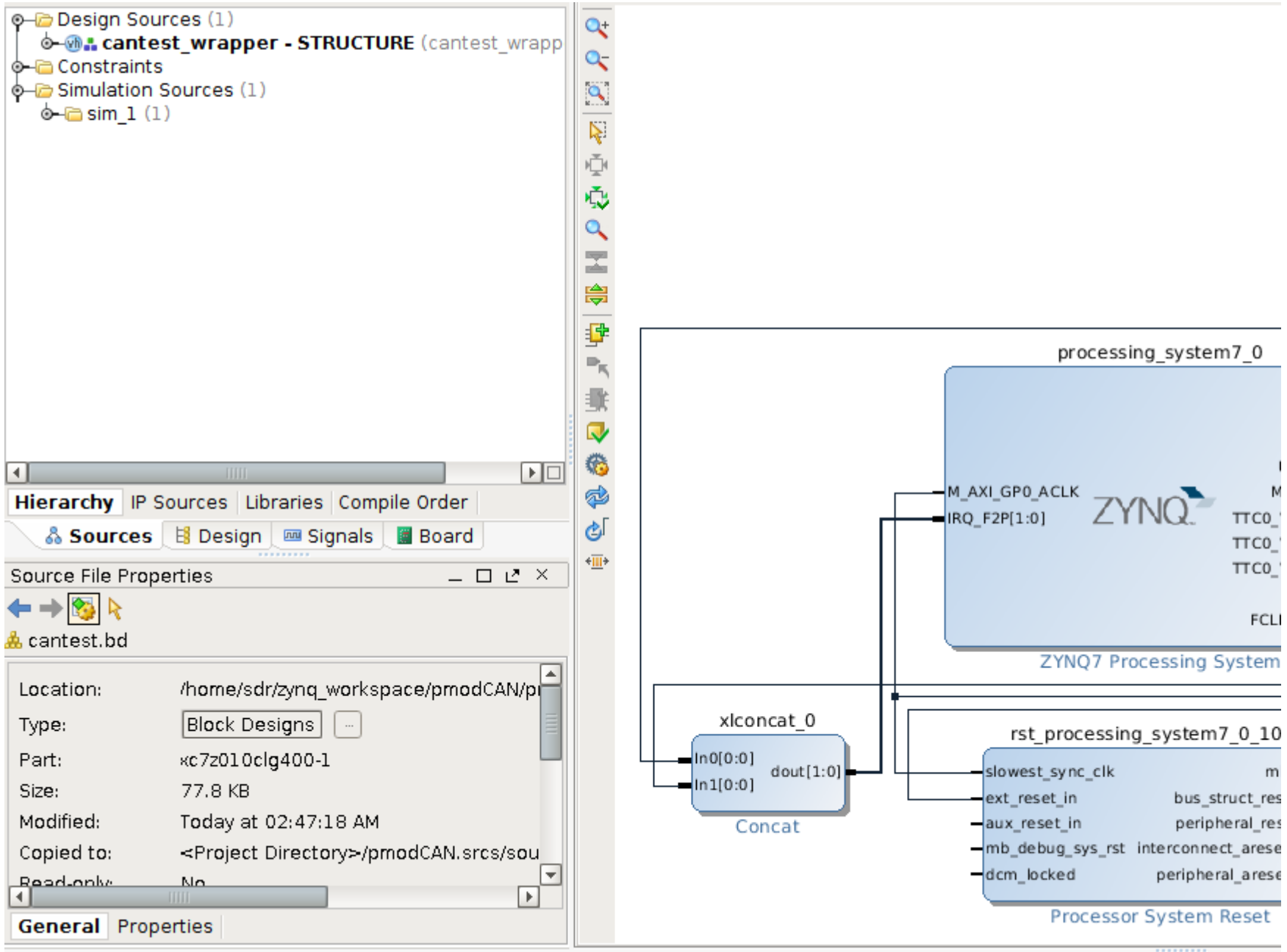

processing_system7_0_axi_periph
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
M01_ACLK
M01_ARESETN
M00_AXI
M01_AXI
AXI Interconnect
PmodCAN_0
AXI_LITE_SPI
AXI_LITE_GPIO
ext_spi_clk
s_axi_aclk
s_axi_aresetn
Pmod_out
SPI_interrupt
GPIO_interrupt
PmodCAN_v1_0
ja
processing_system7_0
DDR
FIXED_IO
SDIO_0
USBIND_0
M_AXI_GP0
M_AXI_GP0_ACLK
IRQ_F2P[0:0]
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
TTC0_WAVE2_OUT
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO
xlconcat_0
In0[0:0]
In1[0:0]
dout[1:0]
Concat
rst_processing_system7_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset

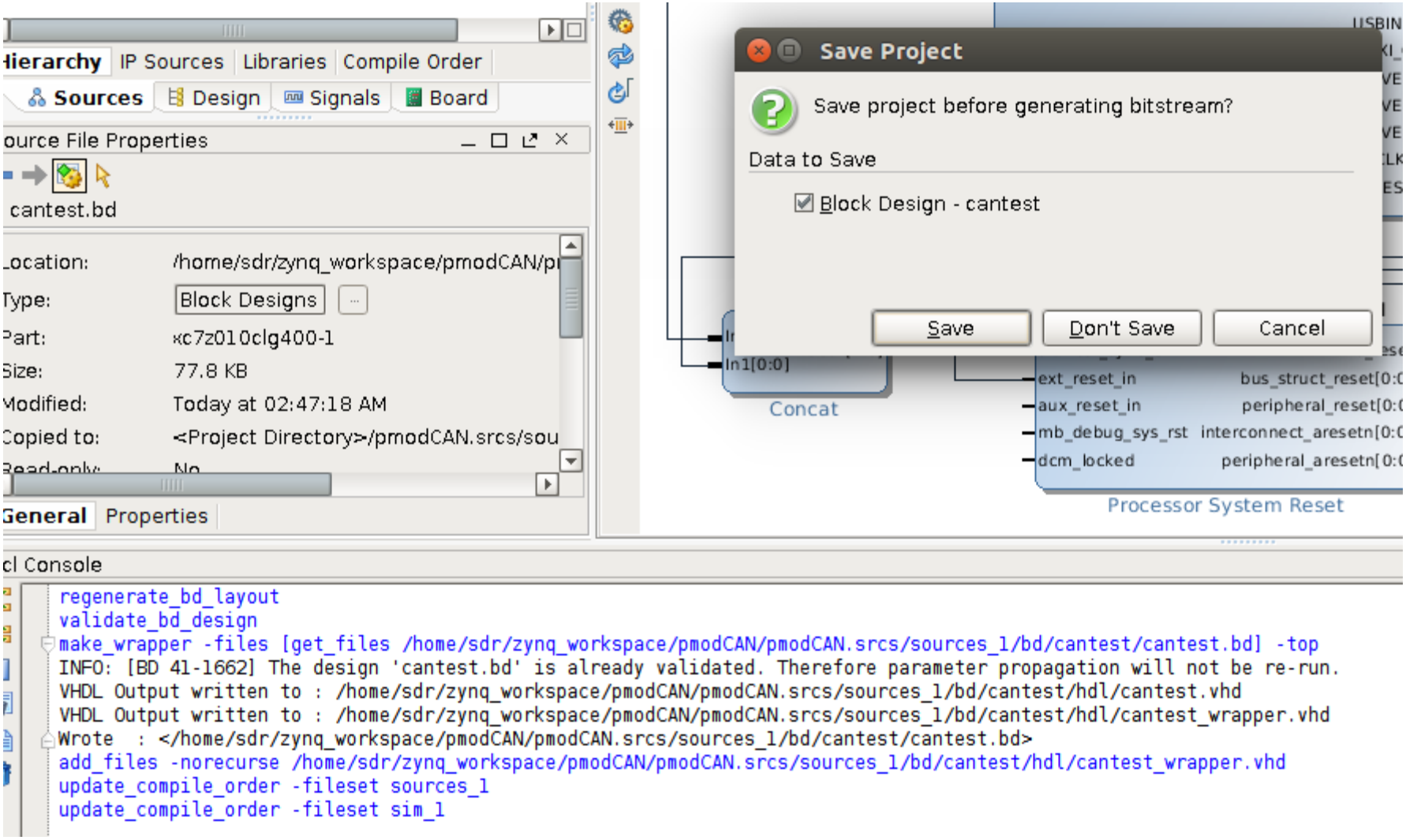


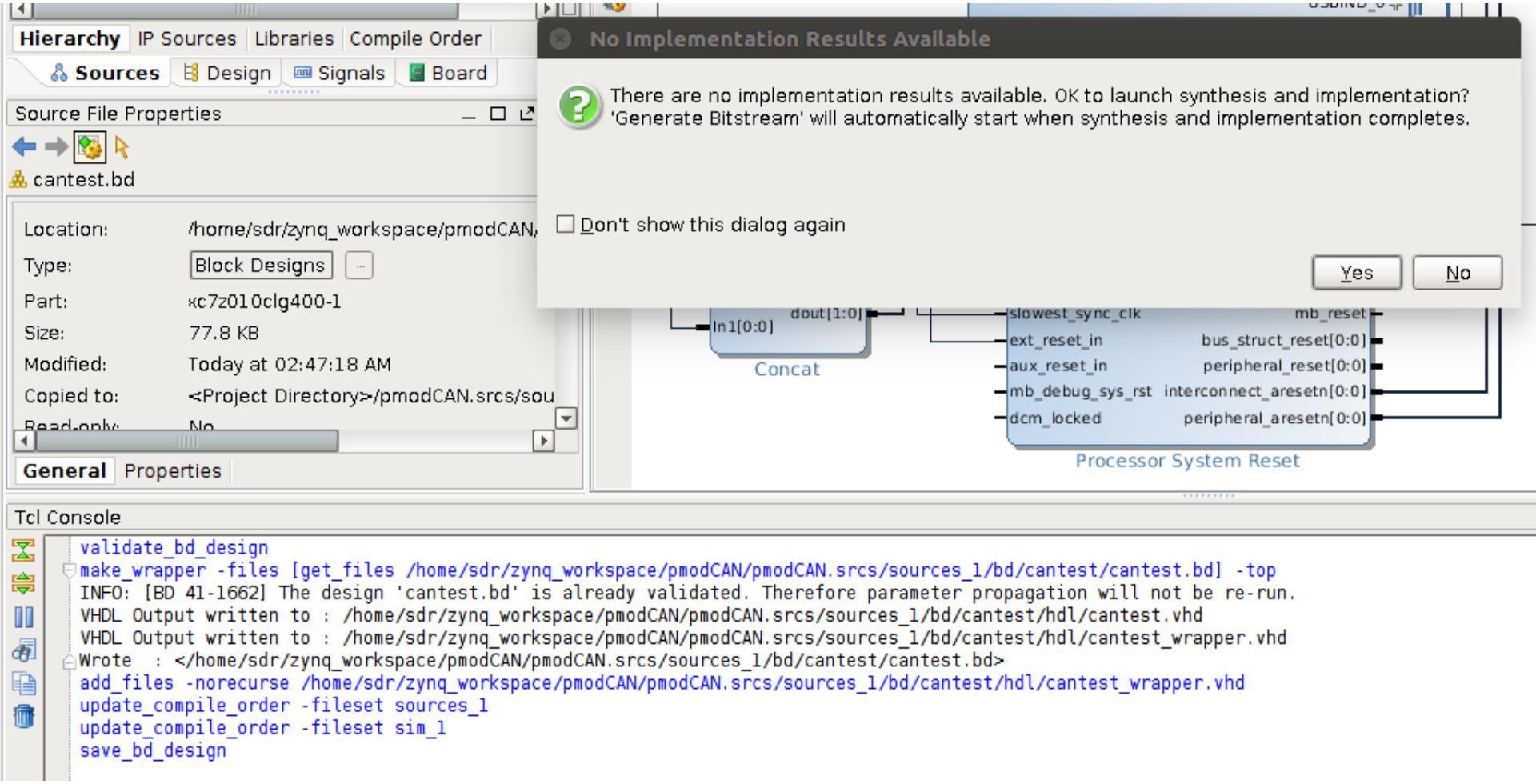
onsole

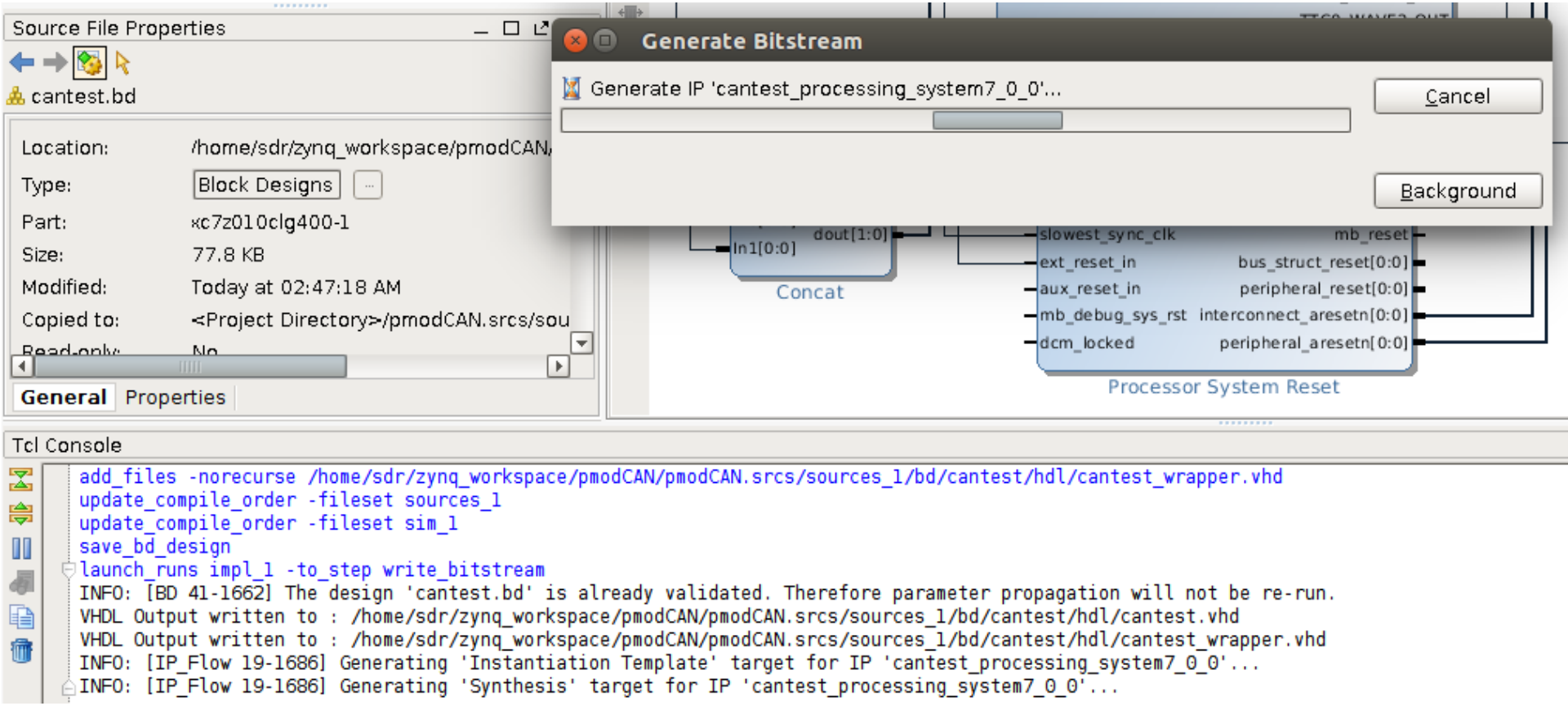
```
endgroup
startgroup
create_bd_cell -type ip -vlnv xilinx.com:ip:xlconcat:2.1 xlconcat_0
endgroup
connect_bd_net [get_bd_pins PmodCAN_0/SPI_interrupt] [get_bd_pins xlconcat_0/In0]
regenerate_bd_layout
connect_bd_net [get_bd_pins xlconcat_0/In1] [get_bd_pins PmodCAN_0/GPIO_interrupt]
connect_bd_net [get_bd_pins xlconcat_0/dout] [get_bd_pins processing_system7_0/IRQ_F2P]
regenerate_bd_layout
validate_bd_design
```

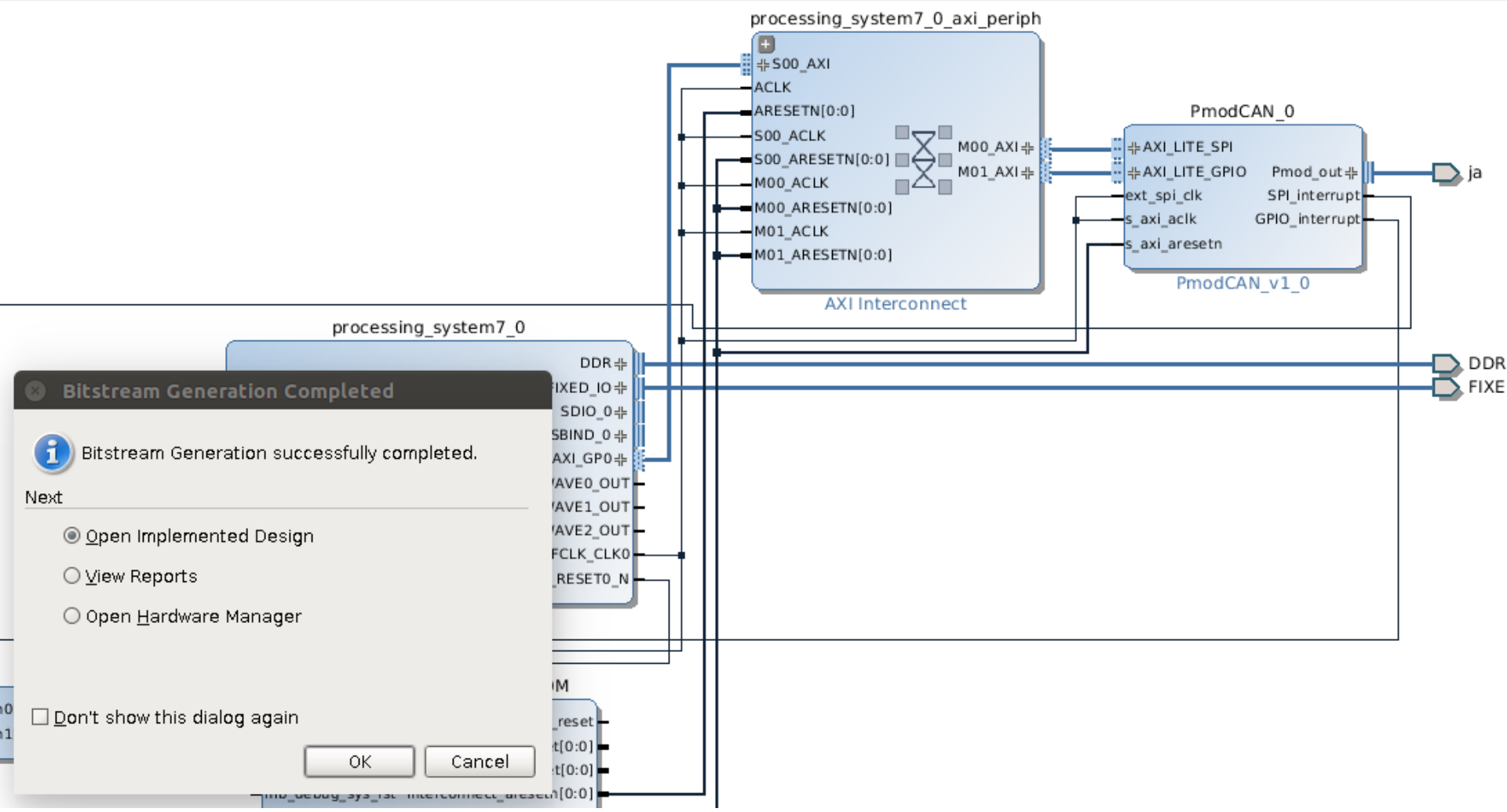

cantest (cantest.bd) (6)
cantest_PmodCAN_0_0 (cantest_PmodCAN_0_0.x
cantest_auto_pc_0 (cantest_auto_pc_0.xci)
cantest_processing_system7_0_0 (cantest_proce
cantest_rst_processing_system7_0_100M_0 (can
cantest_xbar_0 (cantest_xbar_0.xci)
cantest_xlconcat_0_0 (cantest_xlconcat_0_0.xci)
Constraints
Simulation Sources (1)
sim_1 (1)
IP Sources
Libraries
Compile Order
Sources
Design
Signals
Board
File Properties
test.bd
/home/sdr/zynq_workspace/pmodCAN/p
Block Designs
xc7z010clg400-1
1.4 KB
Today at 01:50:25 AM
processing_system7_0
DDR
FIXED_IO
Create HDL Wrapper
You can either add or copy the HDL wrapper file to the project. Use copy option if you would like to modify this file.
Options
Copy generated wrapper to allow user edits
Let Vivado manage wrapper and auto-update
OK
Cancel
Concat

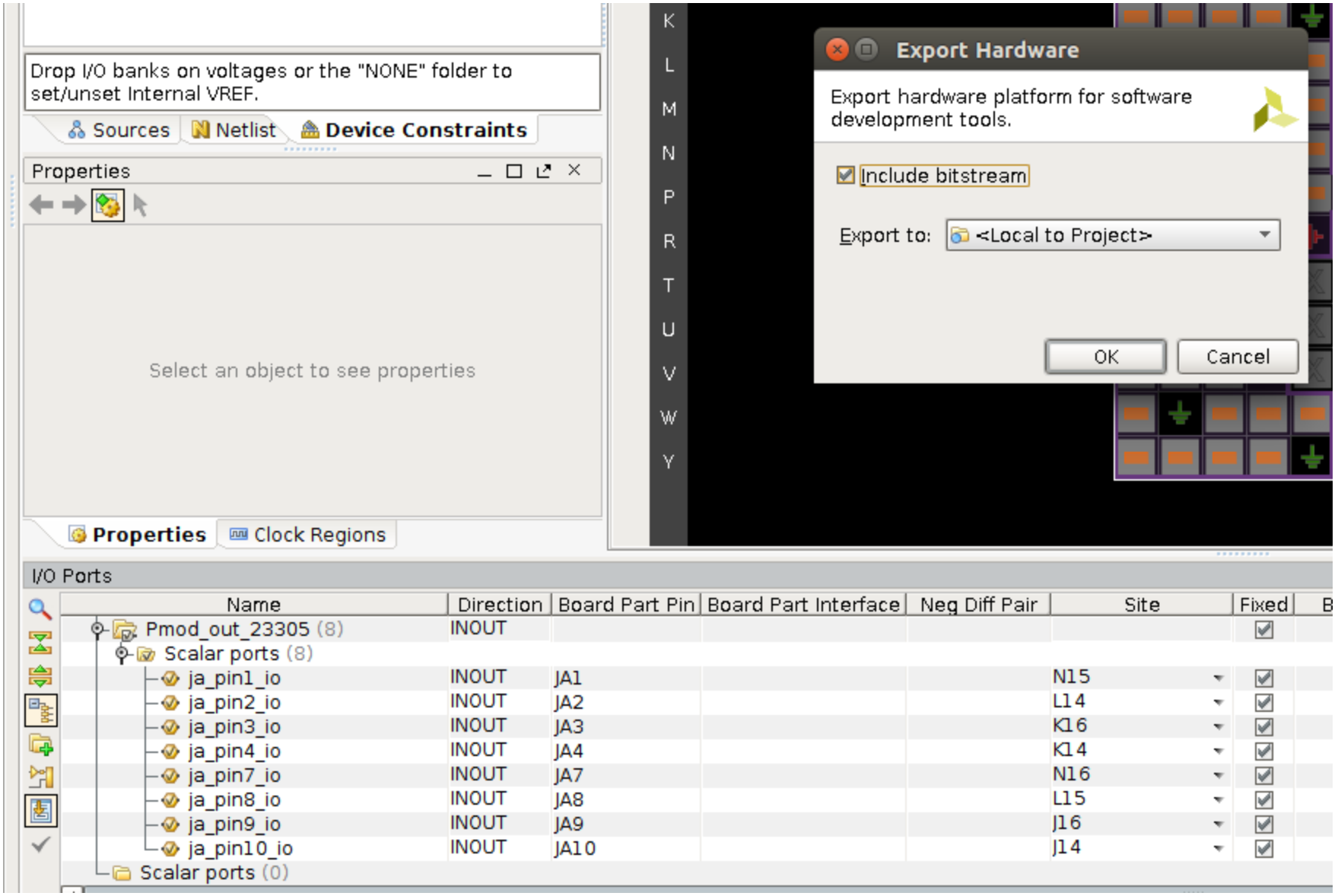

Design Sources (1)
cantest_wrapper - STRUCTURE (cantest_wrapp
Constraints
Simulation Sources (1)
sim_1 (1)
Hierarchy
IP Sources
Libraries
Compile Order
Sources
Design
Signals
Board
Source File Properties
cantest.bd
Location:
/home/sdr/zynq_workspace/pmodCAN/p
Type:
Block Designs
Part:
xc7z010clg400-1
Size:
77.8 KB
Modified:
Today at 02:47:18 AM
Copied to:
<Project Directory>/pmodCAN.srcs/sou
Read-only:
No
General
Properties
processing_system7_0
M_AXI_GP0_ACLK
IRQ_F2P[1:0]
ZYNQ
TTC0_
TTC0_
TTC0_
FCL
ZYNQ7 Processing System
xlconcat_0
In0[0:0]
In1[0:0]
dout[1:0]
Concat
rst_processing_system7_0_10
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
bus_struct_res
peripheral_res
interconnect_arese
peripheral_arese
Processor System Reset

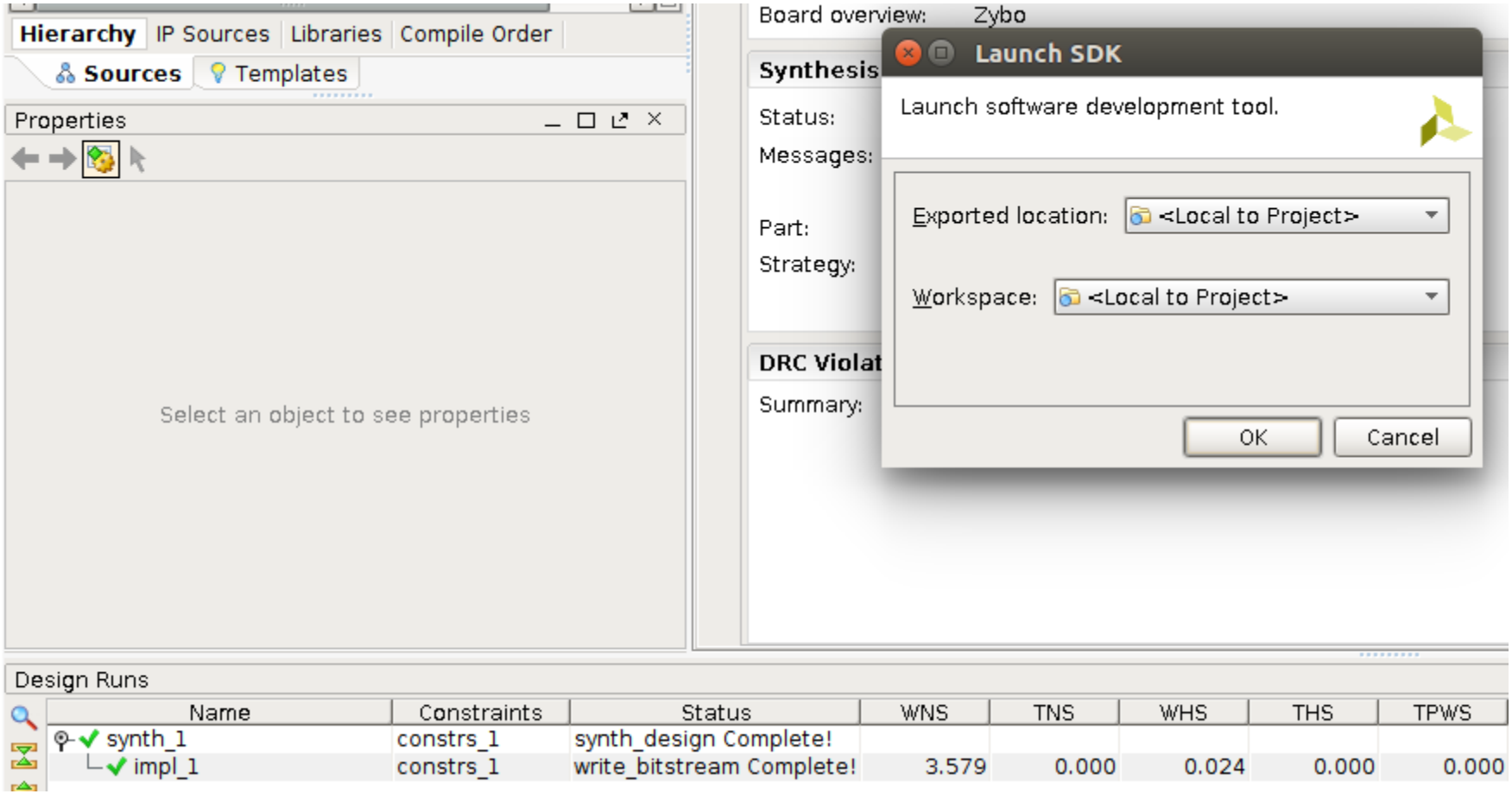

Hierarchy
IP Sources
Libraries
Compile Order
Sources
Design
Signals
Board
ource File Properties
cantest.bd
Location:
/home/sdr/zynq_workspace/pmodCAN/p
Type:
Block Designs
Part:
xc7z010clg400-1
Size:
77.8 KB
Modified:
Today at 02:47:18 AM
Copied to:
<Project Directory>/pmodCAN.srcs/sou
Read-only:
No
General
Properties
Save Project
Save project before generating bitstream?
Data to Save
Block Design - cantest
Save
Don't Save
Cancel
In1[0:0]
Concat
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
cl Console
regenerate_bd_layout
validate_bd_design
make_wrapper -files [get_files /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/cantest.bd] -top
INFO: [BD 41-1662] The design 'cantest.bd' is already validated. Therefore parameter propagation will not be re-run.
VHDL Output written to : /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest.vhd
VHDL Output written to : /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest_wrapper.vhd
Wrote : </home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/cantest.bd>
add_files -norecurse /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest_wrapper.vhd
update_compile_order -fileset sources_1
update_compile_order -fileset sim_1

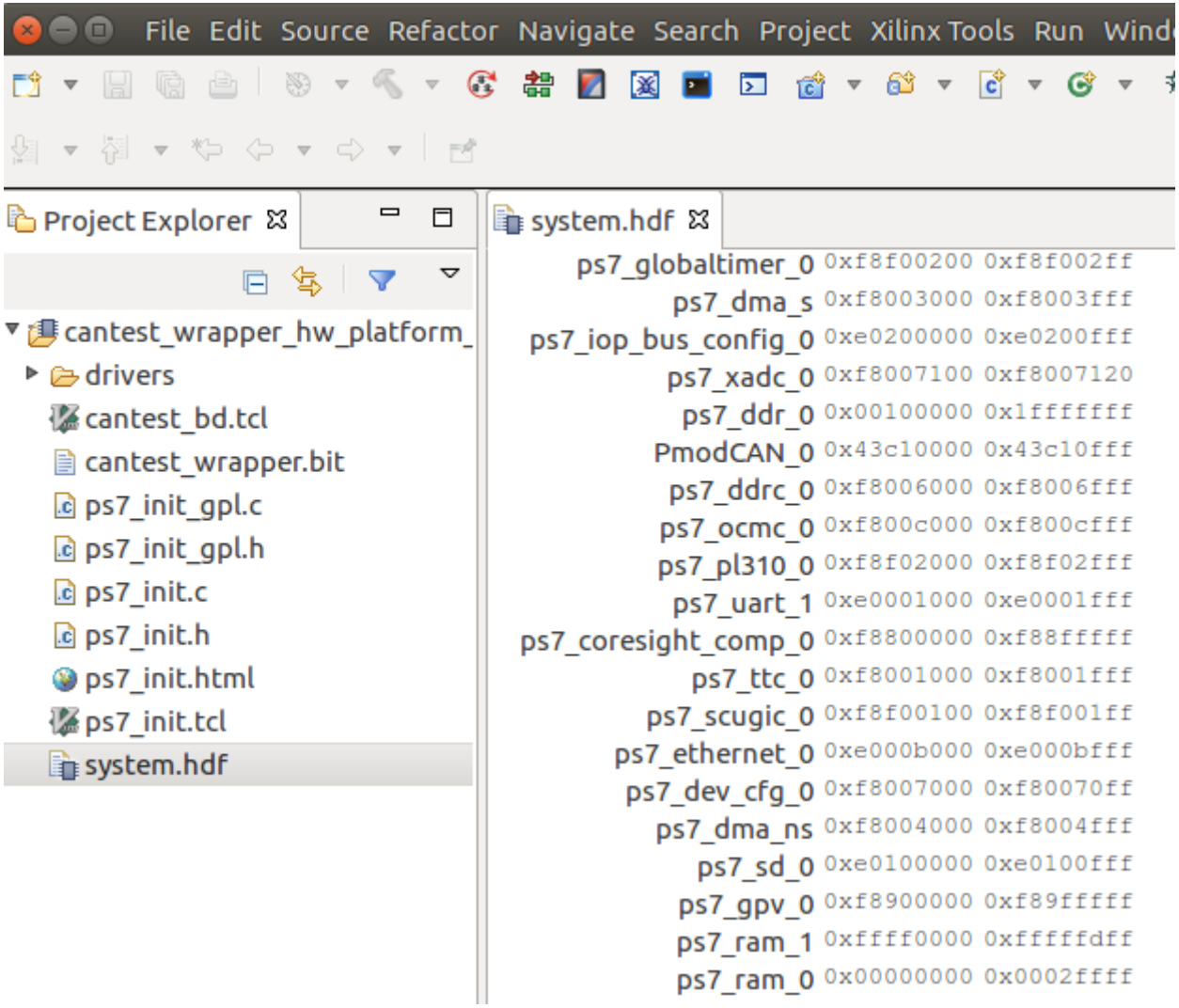

Hierarchy
IP Sources
Libraries
Compile Order
Sources
Design
Signals
Board
Source File Properties
cantest.bd
Location: /home/sdr/zynq_workspace/pmodCAN/
Type: Block Designs
Part: xc7z010clg400-1
Size: 77.8 KB
Modified: Today at 02:47:18 AM
Copied to: <Project Directory>/pmodCAN.srcs/sou
Read-only: No
General
Properties
No Implementation Results Available
There are no implementation results available. OK to launch synthesis and implementation?
'Generate Bitstream' will automatically start when synthesis and implementation completes.
Don't show this dialog again
Yes
No
dout[1:0]
In1[0:0]
Concat
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
Tcl Console
validate_bd_design
make_wrapper -files [get_files /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/cantest.bd] -top
INFO: [BD 41-1662] The design 'cantest.bd' is already validated. Therefore parameter propagation will not be re-run.
VHDL Output written to : /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest.vhd
VHDL Output written to : /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest_wrapper.vhd
Wrote : </home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/cantest.bd>
add_files -norecurse /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest_wrapper.vhd
update_compile_order -fileset sources_1
update_compile_order -fileset sim_1
save_bd_design

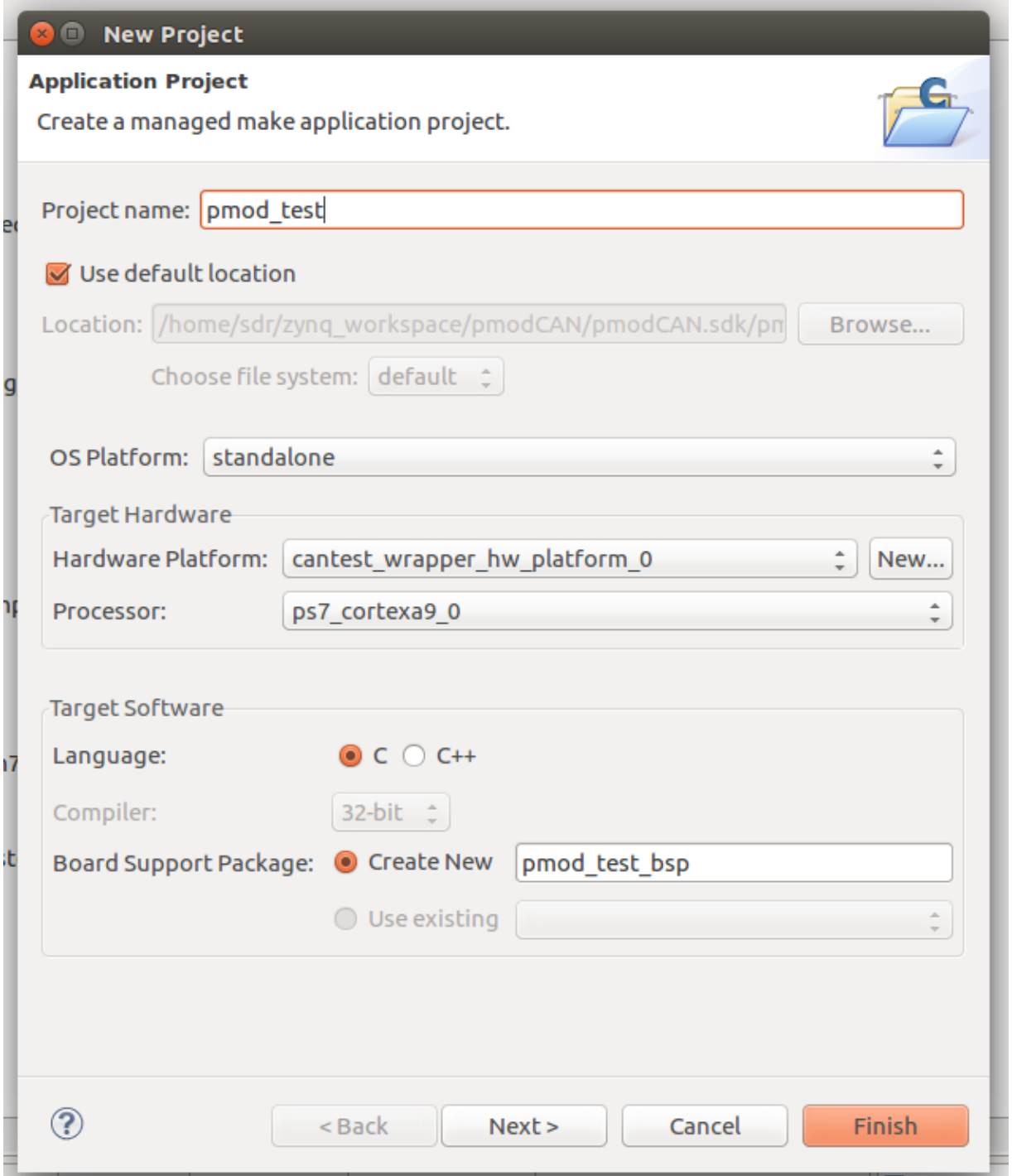

Source File Properties
cantest.bd
Location: /home/sdr/zynq_workspace/pmodCAN/
Type: Block Designs
Part: xc7z010clg400-1
Size: 77.8 KB
Modified: Today at 02:47:18 AM
Copied to: <Project Directory>/pmodCAN.srcs/sou
Read-only: No
General
Properties
Generate Bitstream
Generate IP 'cantest_processing_system7_0_0'...
Cancel
Background
dout[1:0]
In1[0:0]
Concat
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
Tcl Console
add_files -norecurse /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest_wrapper.vhd
update_compile_order -fileset sources_1
update_compile_order -fileset sim_1
save_bd_design
launch_runs impl_1 -to_step write_bitstream
INFO: [BD 41-1662] The design 'cantest.bd' is already validated. Therefore parameter propagation will not be re-run.
VHDL Output written to : /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest.vhd
VHDL Output written to : /home/sdr/zynq_workspace/pmodCAN/pmodCAN.srcs/sources_1/bd/cantest/hdl/cantest_wrapper.vhd
INFO: [IP_Flow 19-1686] Generating 'Instantiation Template' target for IP 'cantest_processing_system7_0_0'...
INFO: [IP_Flow 19-1686] Generating 'Synthesis' target for IP 'cantest_processing_system7_0_0'...

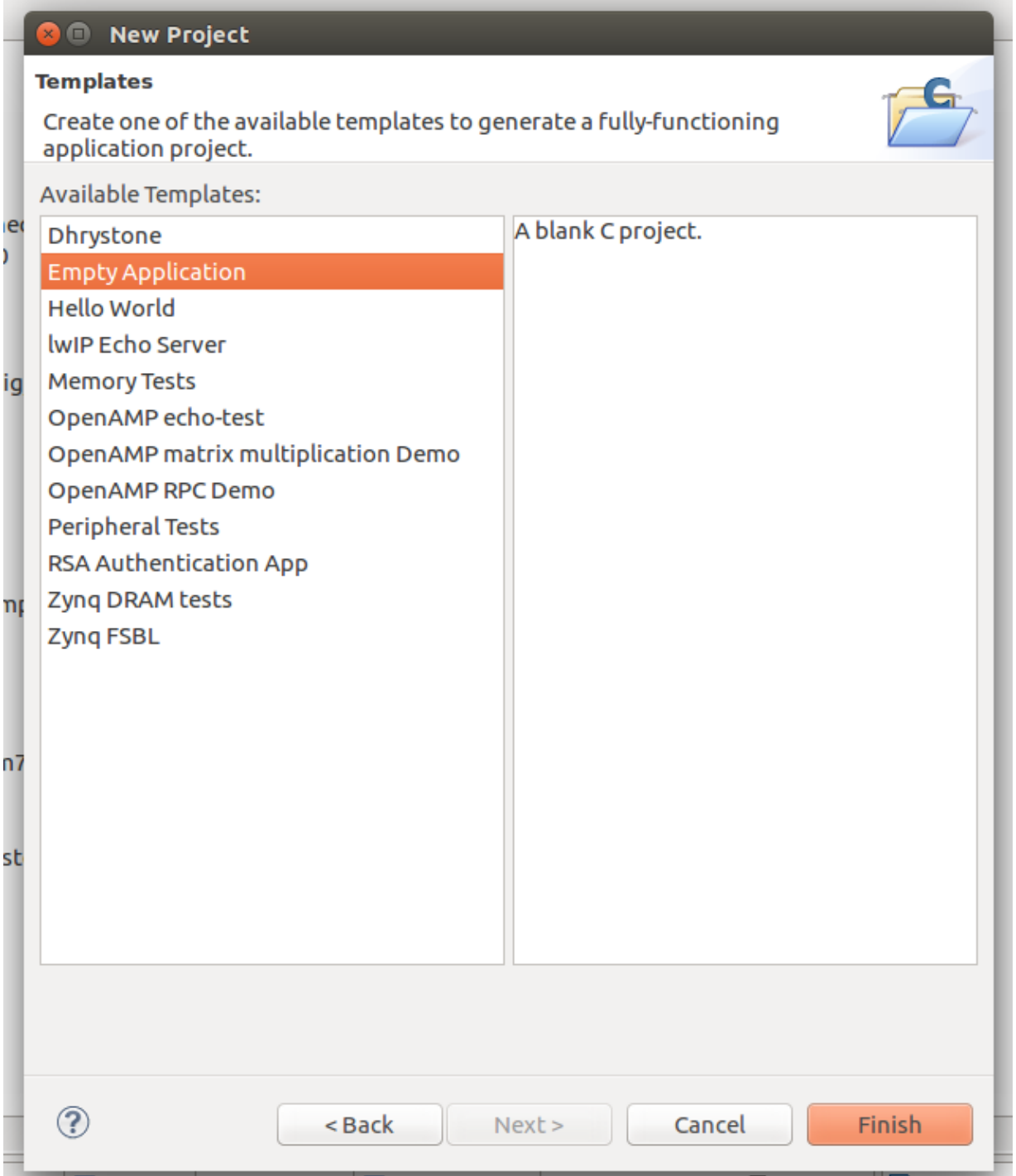

processing_system7_0_axi_periph
S00_AXI
ACLK
ARESETN[0:0]
S00_ACLK
S00_ARESETN[0:0]
M00_ACLK
M00_ARESETN[0:0]
M01_ACLK
M01_ARESETN[0:0]
M00_AXI
M01_AXI
AXI Interconnect
PmodCAN_0
AXI_LITE_SPI
AXI_LITE_GPIO
ext_spi_clk
s_axi_aclk
s_axi_aresetn
Pmod_out
SPI_interrupt
GPIO_interrupt
PmodCAN_v1_0
ja
processing_system7_0
DDR
FIXED_IO
SDIO_0
SBIND_0
AXI_GP0
DDR
FIXE
Bitstream Generation Completed
Bitstream Generation successfully completed.
Next
Open Implemented Design
View Reports
Open Hardware Manager
Don't show this dialog again
OK
Cancel

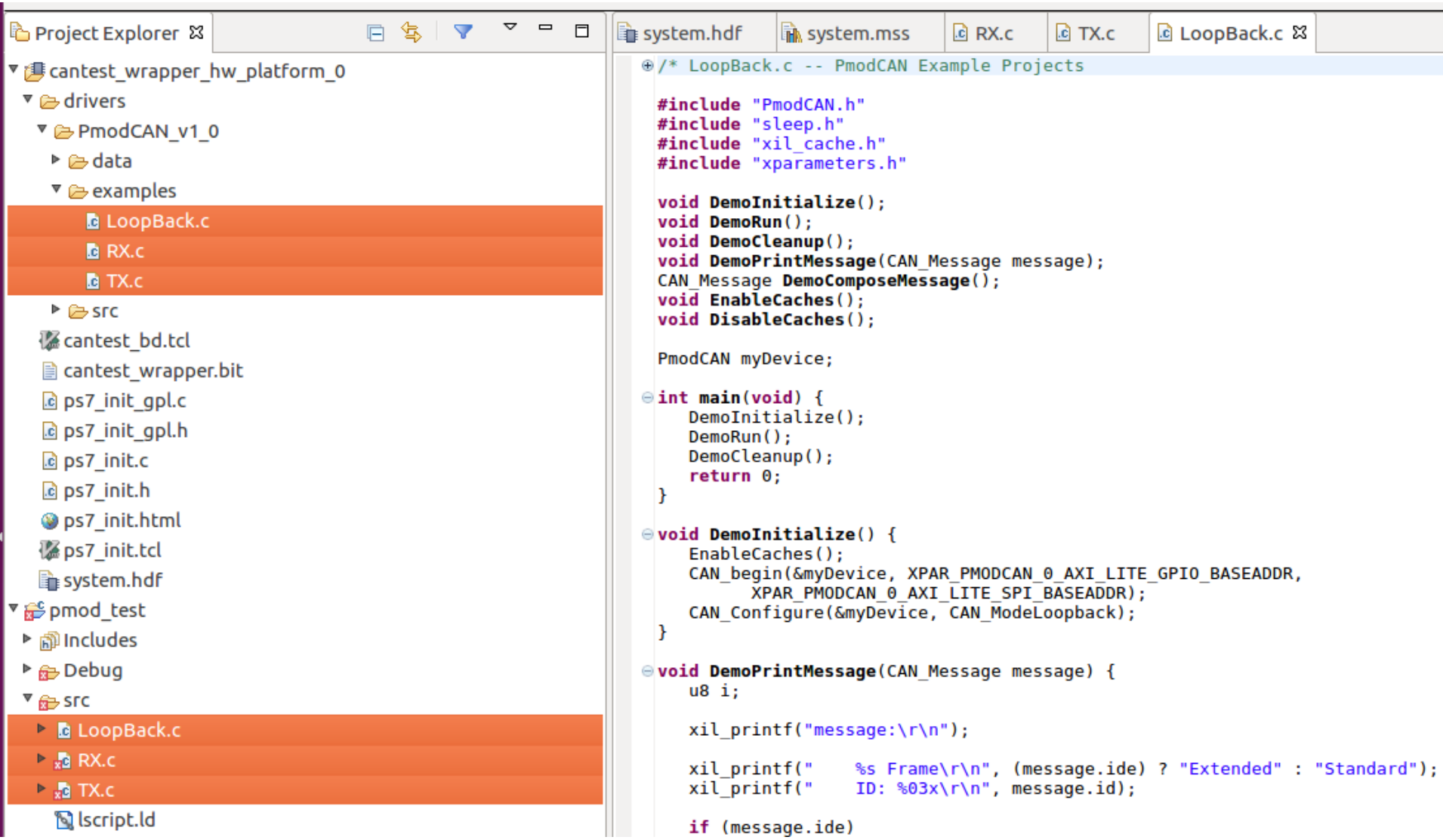

Drop I/O banks on voltages or the "NONE" folder to set/unset Internal VREF.
Sources
Netlist
Device Constraints
Properties
Select an object to see properties
Properties
Clock Regions
K
L
M
N
P
R
T
U
V
W
Y
Export Hardware
Export hardware platform for software development tools.
Include bitstream
Export to:
<Local to Project>
OK
Cancel
I/O Ports
Name
Direction
Board Part Pin
Board Part Interface
Neg Diff Pair
Site
Fixed
Pmod_out_23305 (8)
INOUT
Scalar ports (8)
ja_pin1_io
INOUT
JA1
N15
ja_pin2_io
INOUT
JA2
L14
ja_pin3_io
INOUT
JA3
K16
ja_pin4_io
INOUT
JA4
K14
ja_pin7_io
INOUT
JA7
N16
ja_pin8_io
INOUT
JA8
L15
ja_pin9_io
INOUT
JA9
J16
ja_pin10_io
INOUT
JA10
J14
Scalar ports (0)

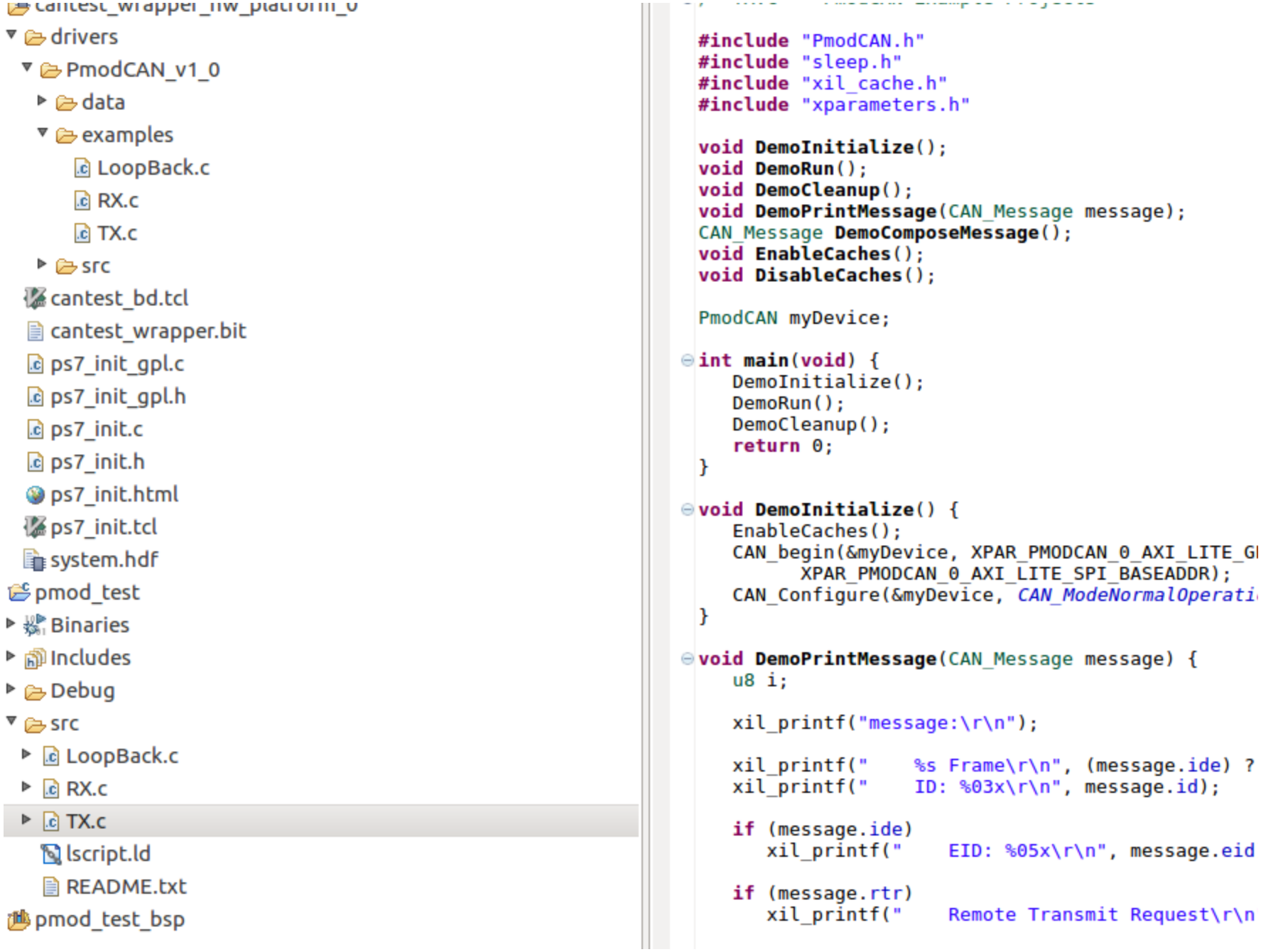

Hierarchy
IP Sources
Libraries
Compile Order
Sources
Templates
Properties
Select an object to see properties
Board overview:
Zybo
Synthesis
Status:
Messages:
Part:
Strategy:
DRC Violat
Summary:
Launch SDK
Launch software development tool.
Exported location:
<Local to Project>
Workspace:
<Local to Project>
OK
Cancel
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
synth_1
constrs_1
synth_design Complete!
impl_1
constrs_1
write_bitstream Complete!
3.579
0.000
0.024
0.000
0.000

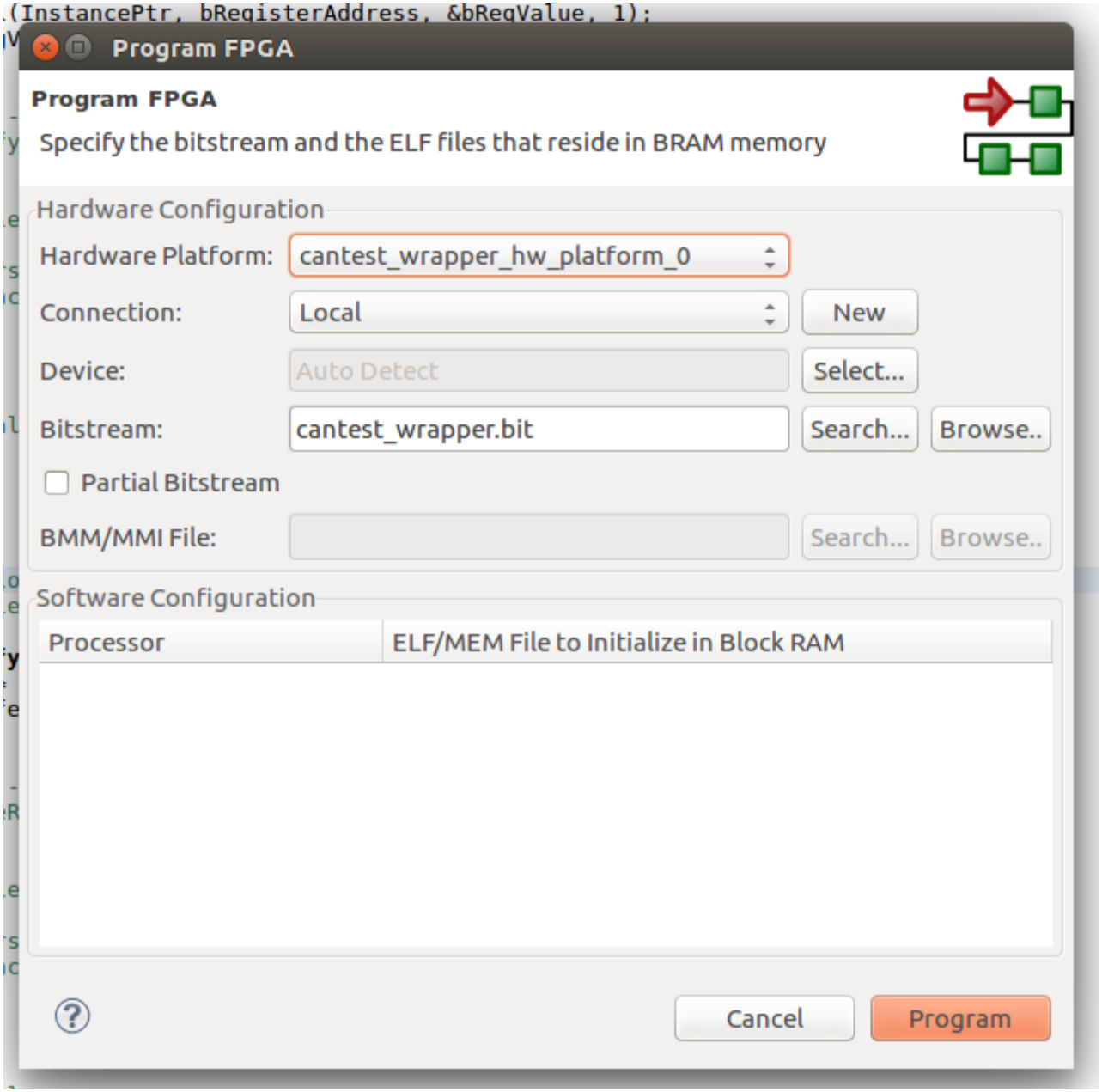

File Edit Source Refactor Navigate Search Project Xilinx Tools Run Wind
Project Explorer
cantest_wrapper_hw_platform_
drivers
cantest_bd.tcl
cantest_wrapper.bit
ps7_init_gpl.c
ps7_init_gpl.h
ps7_init.c
ps7_init.h
ps7_init.html
ps7_init.tcl
system.hdf
system.hdf
ps7_globaltimer_0 0xf8f00200 0xf8f002ff
ps7_dma_s 0xf8003000 0xf8003fff
ps7_iop_bus_config_0 0xe0200000 0xe0200fff
ps7_xadc_0 0xf8007100 0xf8007120
ps7_ddr_0 0x00100000 0x1fffffff
PmodCAN_0 0x43c10000 0x43c10fff
ps7_ddrc_0 0xf8006000 0xf8006fff
ps7_ocmc_0 0xf800c000 0xf800cfff
ps7_pl310_0 0xf8f02000 0xf8f02fff
ps7_uart_1 0xe0001000 0xe0001fff
ps7_coresight_comp_0 0xf8800000 0xf88fffff
ps7_ttc_0 0xf8001000 0xf8001fff
ps7_scugic_0 0xf8f00100 0xf8f001ff
ps7_ethernet_0 0xe000b000 0xe000bfff
ps7_dev_cfg_0 0xf8007000 0xf80070ff
ps7_dma_ns 0xf8004000 0xf8004fff
ps7_sd_0 0xe0100000 0xe0100fff
ps7_gpv_0 0xf8900000 0xf89fffff
ps7_ram_1 0xffff0000 0xffffdfff
ps7_ram_0 0x00000000 0x0002ffff

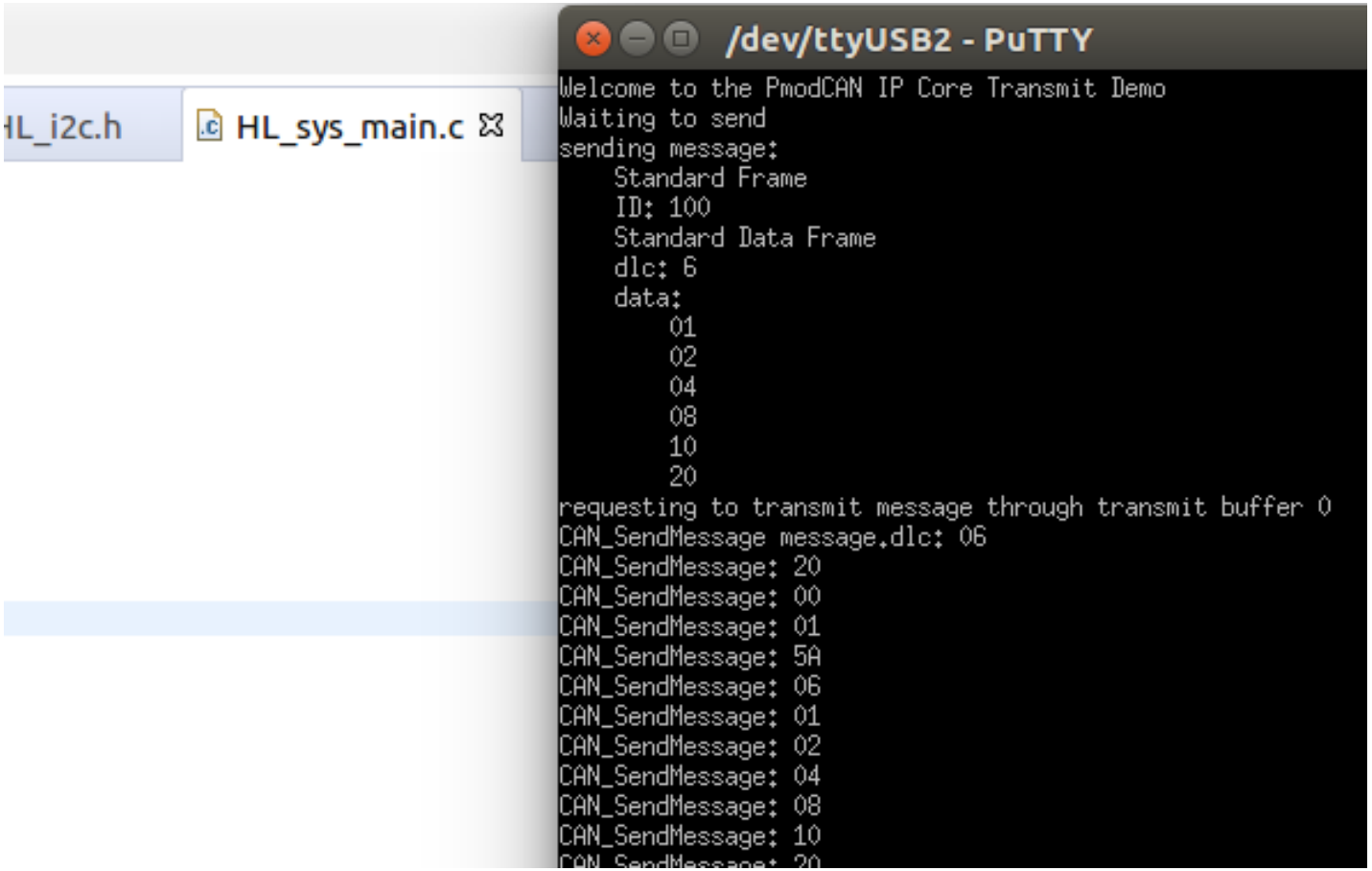

New Project
Application Project
Create a managed make application project.
Project name: pmod_test
Use default location
Location: /home/sdr/zynq_workspace/pmodCAN/pmodCAN.sdk/pm
Browse...
Choose file system: default
OS Platform: standalone
Target Hardware
Hardware Platform: cantest_wrapper_hw_platform_0
New...
Processor: ps7_cortexa9_0
Target Software
Language: C C++
Compiler: 32-bit
Board Support Package: Create New pmod_test_bsp
Use existing
< Back
Next >
Cancel
Finish


New Project
Templates
Create one of the available templates to generate a fully-functioning application project.
Available Templates:
Dhrystone
Empty Application
Hello World
lwIP Echo Server
Memory Tests
OpenAMP echo-test
OpenAMP matrix multiplication Demo
OpenAMP RPC Demo
Peripheral Tests
RSA Authentication App
Zynq DRAM tests
Zynq FSBL
A blank C project.
< Back
Next >
Cancel
Finish


Project Explorer
cantest_wrapper_hw_platform_0
drivers
PmodCAN_v1_0
data
examples
LoopBack.c
RX.c
TX.c
src
cantest_bd.tcl
cantest_wrapper.bit
ps7_init_gpl.c
ps7_init_gpl.h
ps7_init.c
ps7_init.h
ps7_init.html
ps7_init.tcl
system.hdf
pmod_test
Includes
Debug
src
LoopBack.c
RX.c
TX.c
lscript.ld
system.hdf
system.mss
RX.c
TX.c
LoopBack.c
/* LoopBack.c -- PmodCAN Example Projects
#include "PmodCAN.h"
#include "sleep.h"
#include "xil_cache.h"
#include "xparameters.h"
void DemoInitialize();
void DemoRun();
void DemoCleanup();
void DemoPrintMessage(CAN_Message message);
CAN_Message DemoComposeMessage();
void EnableCaches();
void DisableCaches();
PmodCAN myDevice;
int main(void) {
DemoInitialize();
DemoRun();
DemoCleanup();
return 0;
}
void DemoInitialize() {
EnableCaches();
CAN_begin(&myDevice, XPAR_PMODCAN_0_AXI_LITE_GPIO_BASEADDR,
XPAR_PMODCAN_0_AXI_LITE_SPI_BASEADDR);
CAN_Configure(&myDevice, CAN_ModeLoopback);
}
void DemoPrintMessage(CAN_Message message) {
u8 i;
xil_printf("message:\r\n");
xil_printf(" %s Frame\r\n", (message.ide) ? "Extended" : "Standard");
xil_printf(" ID: %03x\r\n", message.id);
if (message.ide)


cantest_wrapper_hw_platform_0
drivers
PmodCAN_v1_0
data
examples
LoopBack.c
RX.c
TX.c
src
cantest_bd.tcl
cantest_wrapper.bit
ps7_init_gpl.c
ps7_init_gpl.h
ps7_init.c
ps7_init.h
ps7_init.html
ps7_init.tcl
system.hdf
pmod_test
Binaries
Includes
Debug
src
LoopBack.c
RX.c
TX.c
lscript.ld
README.txt
pmod_test_bsp
#include "PmodCAN.h"
#include "sleep.h"
#include "xil_cache.h"
#include "xparameters.h"
void DemoInitialize();
void DemoRun();
void DemoCleanup();
void DemoPrintMessage(CAN_Message message);
CAN_Message DemoComposeMessage();
void EnableCaches();
void DisableCaches();
PmodCAN myDevice;
int main(void) {
DemoInitialize();
DemoRun();
DemoCleanup();
return 0;
}
void DemoInitialize() {
EnableCaches();
CAN_begin(&myDevice, XPAR_PMODCAN_0_AXI_LITE_G
XPAR_PMODCAN_0_AXI_LITE_SPI_BASEADDR);
CAN_Configure(&myDevice, CAN_ModeNormalOperati
}
void DemoPrintMessage(CAN_Message message) {
u8 i;
xil_printf("message:\r\n");
xil_printf(" %s Frame\r\n", (message.ide) ?
xil_printf(" ID: %03x\r\n", message.id);
if (message.ide)
xil_printf(" EID: %05x\r\n", message.eid
if (message.rtr)
xil_printf(" Remote Transmit Request\r\n


(InstancePtr, bRegisterAddress, &bRegValue, 1);
Program FPGA
Program FPGA
Specify the bitstream and the ELF files that reside in BRAM memory
Hardware Configuration
Hardware Platform:
cantest_wrapper_hw_platform_0
Connection:
Local
New
Device:
Auto Detect
Select...
Bitstream:
cantest_wrapper.bit
Search...
Browse..
Partial Bitstream
BMM/MMI File:
Search...
Browse..
Software Configuration
Processor
ELF/MEM File to Initialize in Block RAM
Cancel
Program


HL_i2c.h
HL_sys_main.c
/dev/ttyUSB2 - PuTTY
Welcome to the PmodCAN IP Core Transmit Demo
Waiting to send
sending message:
Standard Frame
ID: 100
Standard Data Frame
dlc: 6
data:
01
02
04
08
10
20
requesting to transmit message through transmit buffer 0
CAN_SendMessage message.dlc: 06
CAN_SendMessage: 20
CAN_SendMessage: 00
CAN_SendMessage: 01
CAN_SendMessage: 5A
CAN_SendMessage: 06
CAN_SendMessage: 01
CAN_SendMessage: 02
CAN_SendMessage: 04
CAN_SendMessage: 08
CAN_SendMessage: 10