

Xilinx

Zynq FPGA

TI DSP MCU 기반의

프로그래밍 및 회로 설계 전문가

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New Project

Family:

TMS570LS04x

TMS570LS03x

TMS570LS02x

RM42x

RM41x

TMS570LS09x\_07x

RM44x

TMS570LC43x

RM57Lx

Device:

TMS570LC4357ZWT

TMS570LC4357ZWT\_FREERTOS

TMS570LC4357ZWT

PINMUX

RTI

GIO

ESM

SCI1

SCI2

SCI3

SCI4

LIN1

LIN2

MIBS

General

Driver Enable

R5-MPU-PMU

Interrupts

VIM General

VIM RAM

VIM Channel 0-31

16 : CAN1 High

16

17 : MIBSPI2 High

17

18 : FlexRay High

18

19 : CRC 1

19

20 : ESM Low

20

21 : SSI

21

22 : PMU TAP

22

23 : GIO Low

23

24 : HET1 Low

24

25 : HET TU1 Low

25

26 : MIBSPI1 Low

26

27 : LIN1 Low

27

28 : ADC1 Group 2

28

29 : CAN1 Low

29

TMS570LC4357ZWT

PINMUX

RTI

GIO

ESM

SCI1

SCI2

SCI3

SCI4

LIN1

LIN2

MIBSPI1

MIBSPI2

MIBSPI3

General

Driver Enable

R5-MPU-PMU

Interrupts

VIM General

VIM RAM

VIM Channel 0-31

VIM Channel 32-63

VIM Channel 64-95

42 : PMM Low

42

44 : CAN1 IF3

44

45 : CAN3 High

45

General

Driver Enable

R5-MPU-PMU

Interrupts

VIM General

VIM

Enable Driver Compilation

Click and mark the required modules for driver compilation from below

☐ Enable RTI driver

☒ Enable GIO driver \*\*

☐ Enable SCI drivers

☐ Enable SCI3 driver \*\*  
☐ Enable SCI4 driver \*\*

☐ Enable LIN drivers

☐ Enable LIN1 driver \*\* / ☐ Enable SCI1 driver \*\*  
☐ Enable LIN2 driver \*\* / ☐ Enable SCI2 driver \*\*

☐ Enable MIBSPI drivers

☐ Enable MIBSPI1 driver \*\* ☐ Enable SPI1 driver \*\*  
☐ Enable MIBSPI2 driver \*\* ☐ Enable SPI2 driver \*\*  
☐ Enable MIBSPI3 driver \*\* ☐ Enable SPI3 driver \*\*  
☐ Enable MIBSPI4 driver \*\* ☐ Enable SPI4 driver \*\*  
☐ Enable MIBSPI5 driver \*\* ☐ Enable SPI5 driver \*\*

☒ Enable CAN drivers

☒ Enable CAN1 driver  
☐ Enable CAN2 driver  
☐ Enable CAN3 driver  
☐ Enable CAN4 driver \*\*

☒ Enable ETPWM driver  
☐ Enable ECAP driver

☐ Mark/Unmark all

Enable ETPWM modules

☒ Enable ETPWM1

☐ Enable ETPWM2

☐ Enable ETPWM3

☐ Enable ETPWM4

☐ Enable ETPWM5

☐ Enable ETPWM6

☐ Enable ETPWM7

General

ETPWM1

ETPWM2

ETPWM3

ETPWM4

ETPWM5

ETPWM6

ETPWM7

Clock Configuration

TB Clock (MHz): 110.000

VCLK3 (MHz): 9.375

Actual TB Clock (MHz): 0.146

Clock Prescale

HSPCLKDIV: 3

CLKDIV: 10

PWM Configuration

PWM

High Polarity:

Low Polarity:

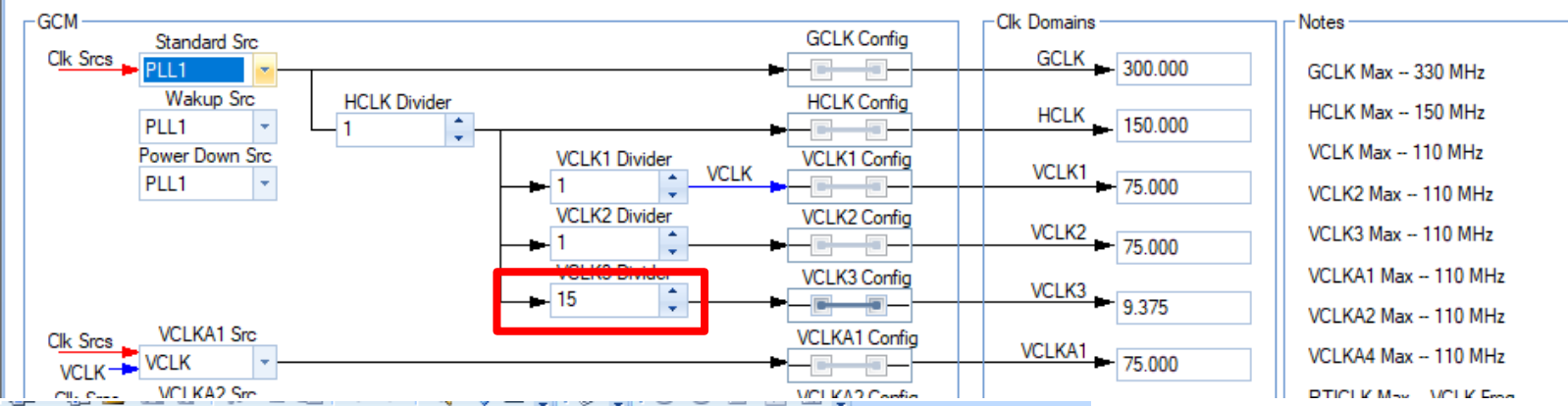
Duty[%]: 70

Period[ns]: 1420000000

940000000.000

1420000000.000

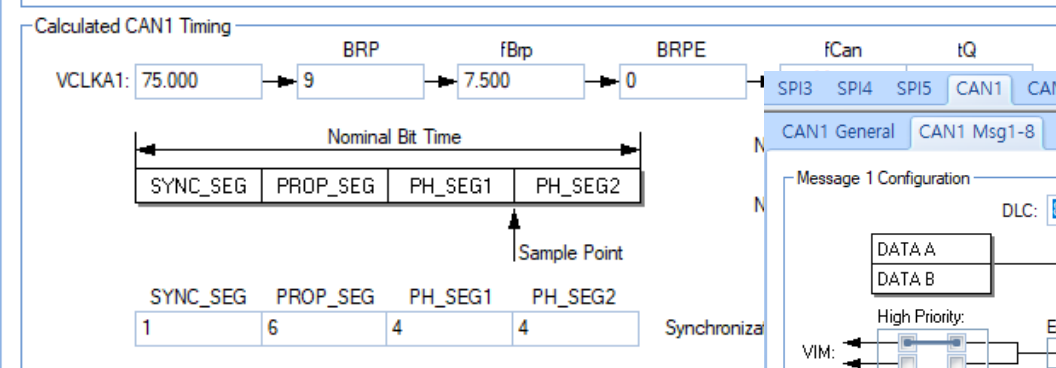
# Buzzer\_CAN Setting



**CAN1 Timing Configuration**

Bit Rate: 500 (highlighted with red box) | Propagation Delay: 700

SP Ref: 75 | Calculated Bit Rate: 500.000



**CAN1 Auto Bus On Configuration**

☐ Enable Auto Bus On

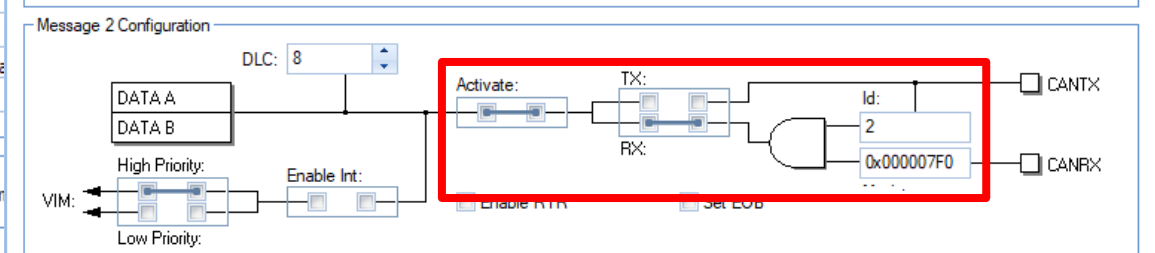
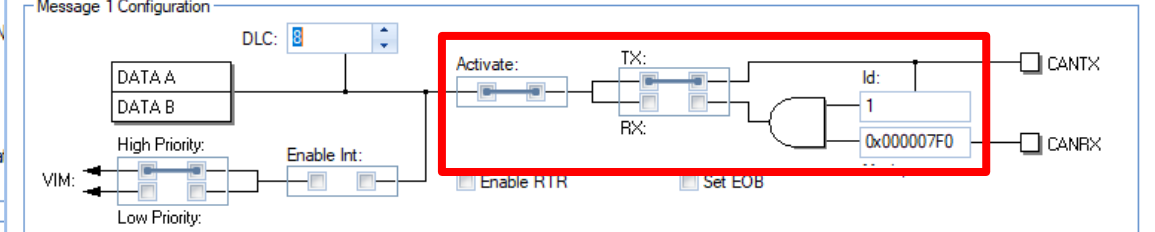
ABOTR: 0 | tAbo: 0

VCLK1: 75.000 → ABO Counter → tAbo Nominal: 0.000

**CAN1 General Configuration**

☐ Disable Automatic Retransmission | ☒ Enable Identifier Extension | ☐ Enable Ram

## Buzzer\_CAN Setting



```

#include <HL_can.h>
#include <HL_etpwm.h>
#include <HL_reg_can.h>
#include <HL_reg_etpwm.h>
#include <stdio.h>

```

```

char tr;
char re;

```

```

void delay(int time)
{
    int i;
    for (i = 0; i < time; i++)
        ;
}

```

```

int main()
{
    canInit();
    etpwmlnit();

    while (1)
    {
        delay(1000000);
        canTransmit(canREG1, canMESSAGE_BOX1, &tr);
        delay(1000000);

        if (canIsRxMessageArrived(canREG1, canMESSAGE_BOX2))
        {
            canGetData(canREG1, canMESSAGE_BOX2, &re);
            printf("rx =%dWn", re);
            switch (re)
            {

```

```

case 5:
    etpwmStartTBCLK();
    etpwmREG1->CMPA = 2300;
    break;

default:
    etpwmStopTBCLK();
    break;
    }
}
}
}

```

**Buzzer\_CAN CODE**

Buzzer\_CAN

Designer : 황수정, 김민호

2018.08.28

Project AI CAR

CAN



R1  
100Ω



Q1  
2SC2873

V1  
12V

LS1

BUZZER  
7Hz





## USB2CAN UI

Version 1.10 (2016. 9. 20)

UI Config.

## USB(VCP) Devices

NTREX USB2CAN(FIFO) [NT2ASDZL]

Search

Connect

Disconnect

## CAN Configuration

Btrrate

500K bps

Filter Identification

1

(Hexa)

Filter Mask

7F0

(Hexa)

Set

## CAN Messages

Time	ID(Hex)	Flags	Data(Hex)
192794.327211	1	Ext	00 00 00 00 00 00 00 00 (8)
192793.925464	1	Ext	00 00 00 00 00 00 00 00 (8)
192793.521720	1	Ext	00 00 00 00 00 00 00 00 (8)
192793.117978	1	Ext	00 00 00 00 00 00 00 00 (8)
192792.714249	1	Ext	00 00 00 00 00 00 00 00 (8)
192792.311418	1	Ext	00 00 00 00 00 00 00 00 (8)
192791.907691	1	Ext	00 00 00 00 00 00 00 00 (8)
192791.503999	1	Ext	00 00 00 00 00 00 00 00 (8)
192791.101188	1	Ext	00 00 00 00 00 00 00 00 (8)
192790.697500	1	Ext	00 00 00 00 00 00 00 00 (8)
192789.566079	1	Self Ext	05 (1)
192789.276441	1	Ext	00 00 00 00 00 00 00 00 (8)
192788.873624	1	Ext	00 00 00 00 00 00 00 00 (8)
192788.469861	1	Ext	00 00 00 00 00 00 00 00 (8)
192788.067197	1	Ext	00 00 00 00 00 00 00 00 (8)
192787.664419	1	Ext	00 00 00 00 00 00 00 00 (8)
192787.260686	1	Ext	00 00 00 00 00 00 00 00 (8)

☒ Receive CAN Message

Clear

## Transmit Message

ID(Hexa)	1	<input checked="" type="checkbox"/> Ext	<input type="checkbox"/> RTR	Data(Hexa)	5	Send
ID(Hexa)	1	<input checked="" type="checkbox"/> Ext	<input type="checkbox"/> RTR	Data(Hexa)	1	Send
ID(Hexa)	0	<input type="checkbox"/> Ext	<input type="checkbox"/> RTR	Data(Hexa)		Send

