

Ultra96 dm2 How to

Innova Lee(이상훈)
gcccompil3r@gmail.com

본 문서 작업의 절차는 이니프로의 hokim(김현욱)님에 의해 만들어졌습니다.
메일 문의: hokim1972@naver.com

```
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study$ ls
ultra96_trd
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study$ cp -r ultra96_trd dm2_trd
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study$ ls
dm2_trd  ultra96_trd
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study$ cd dm2_trd/
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd$ ls
create_dsa.tcl  dm1.tcl          dm6.tcl  mipi_csi2_rx_hier.tcl  sdsoc
dm1             dm1.xdc          dm6.xdc  petalinux              tpg_input_hier.tcl
dm1_preset.tcl  dm6_preset.tcl  LICENSE  README.md              workspaces
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd$ cd dm1
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/dm1$ vivado dm1.xpr
```

```
***** Vivado v2018.2 (64-bit)
**** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
**** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.
```

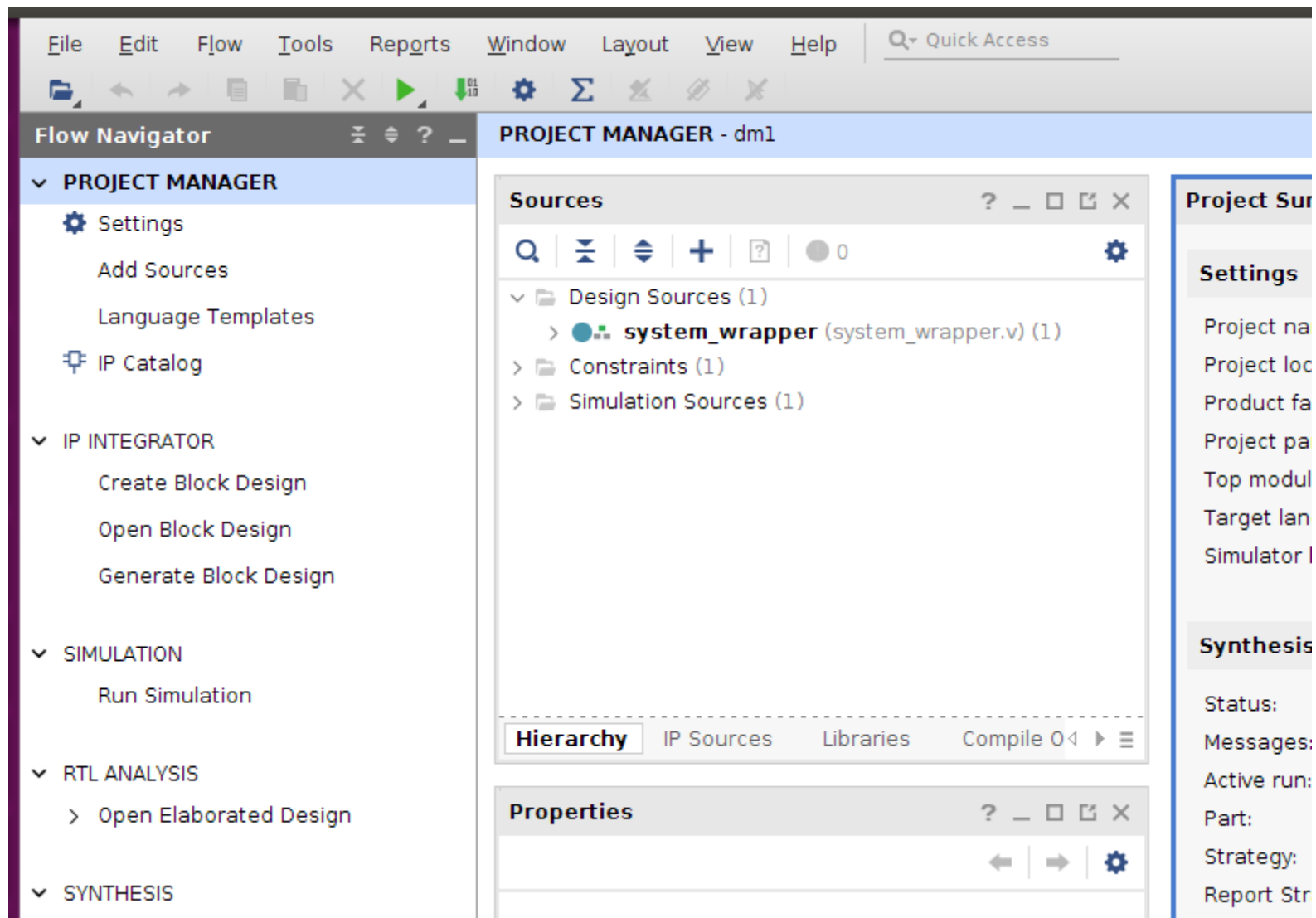
```
start_gui
```

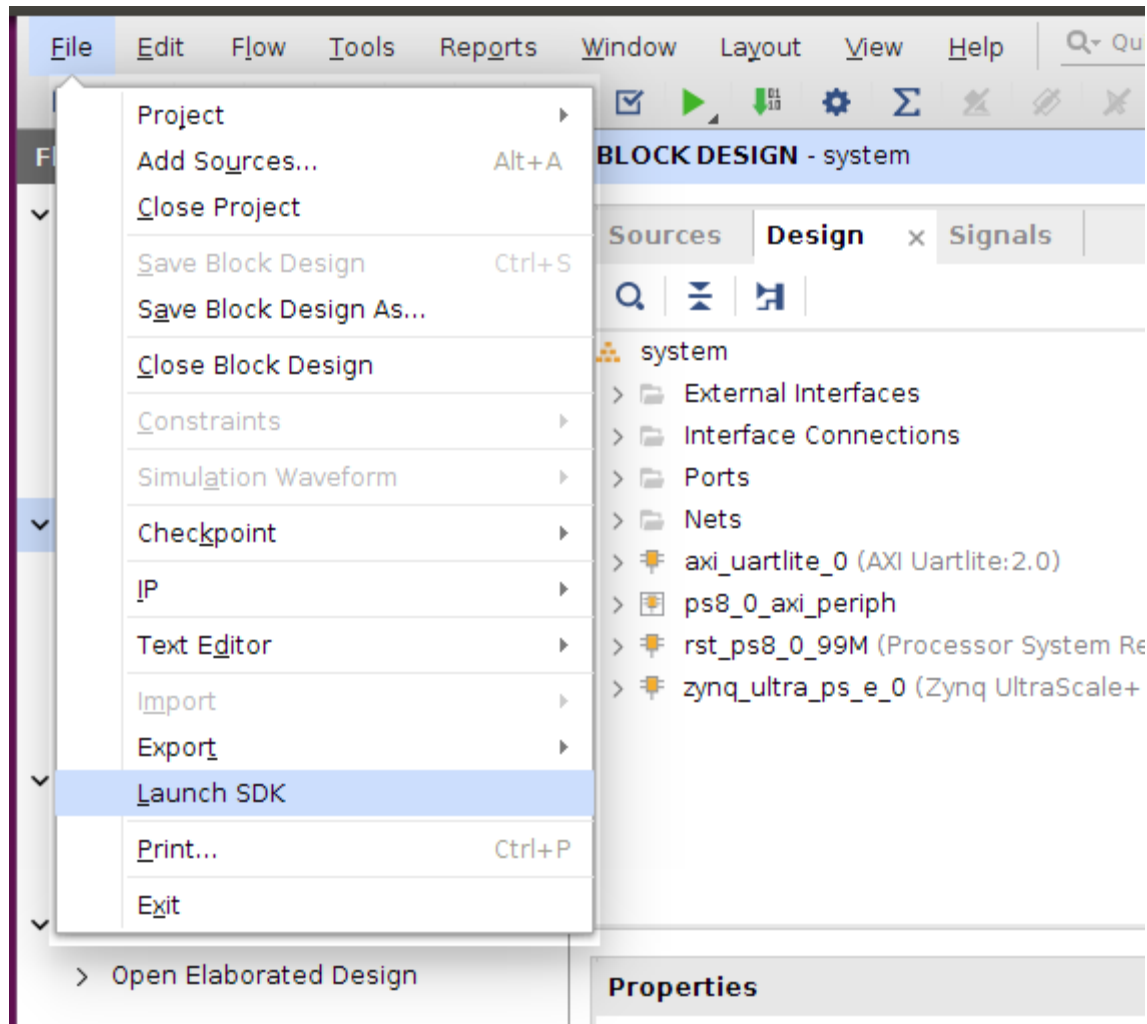
Projects/html_tutorial
factor Run Tools VC

background

Projects/html_tu
1
2
3
4
5
6
7
8
9
10
11

VIVADO
HLx Editions





rtlite:2.0)

essor System Reset:5.0)

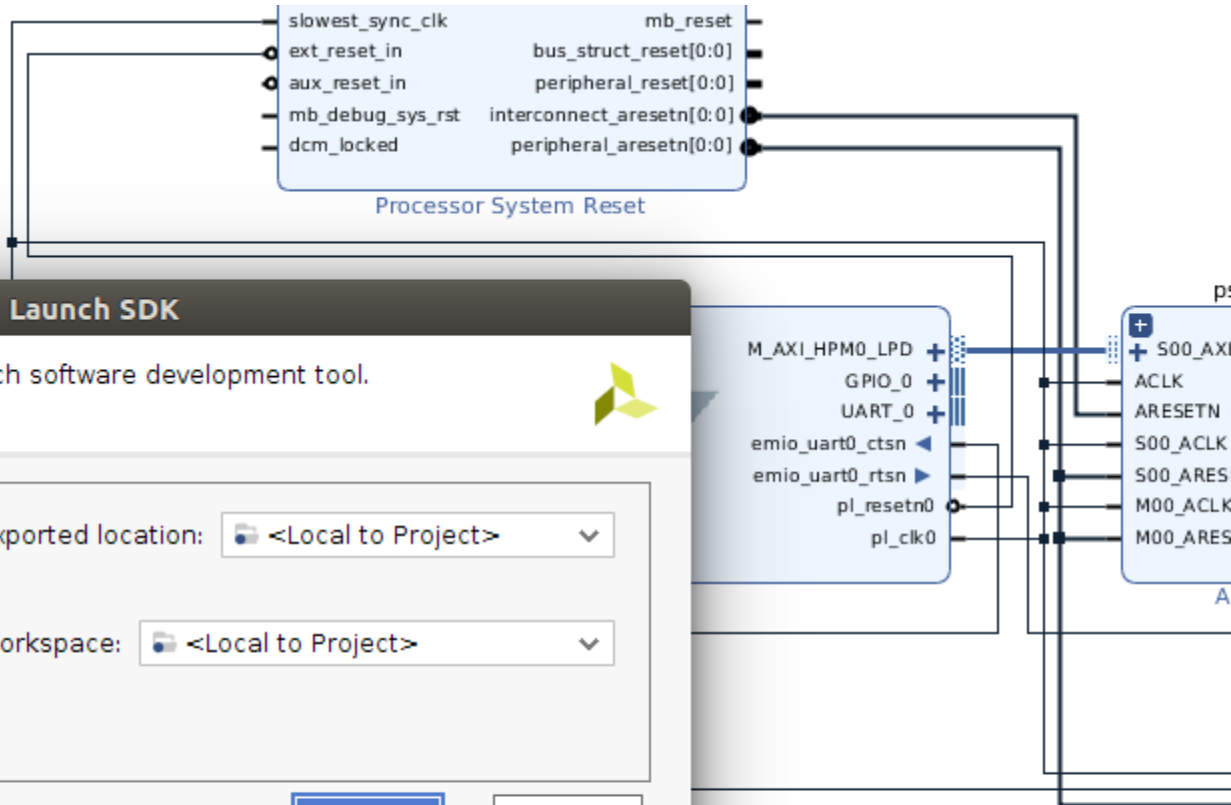
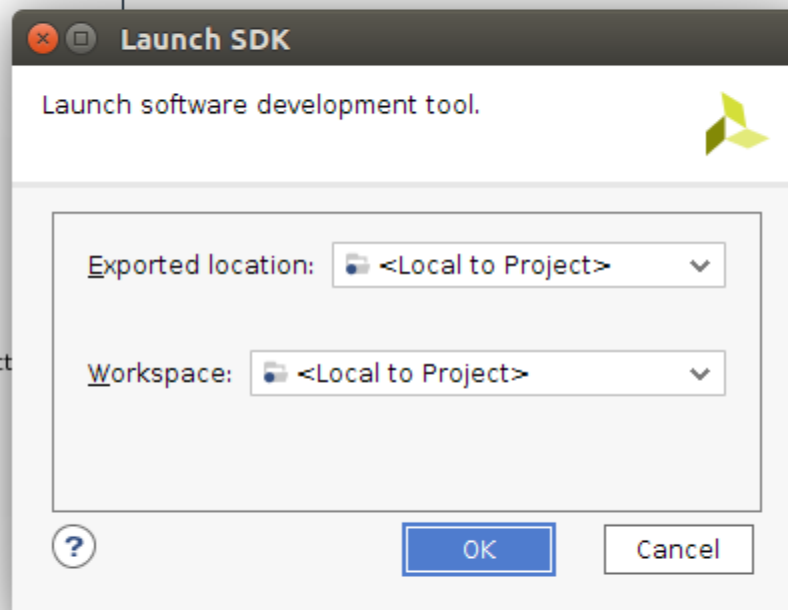
/nq UltraScale+ MPSoC:3.2)

? _ □ □ ×

← → ⚙

it to see properties

BT_ct



ges | Log | Reports | Design Runs



oh
(Processor System Reset:5.0)
e_0 (Zynq UltraScale+ MPSoC:3.2)



Launch SDK

Launch software development tool.

M_AXI_HPM0_LPD +
GPIO_0 +
UART_0 +

ps8_0_axi_perip

S00_AXI +
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN

AXI Interconne

Exported hardware system out-of-date

Exported Hardware file is out of date. Exported hardware information may be inconsistent with respect to the current state of the design. It is recommended that you re-export the design and launch SDK otherwise SDK is launched with out of date hardware system file.

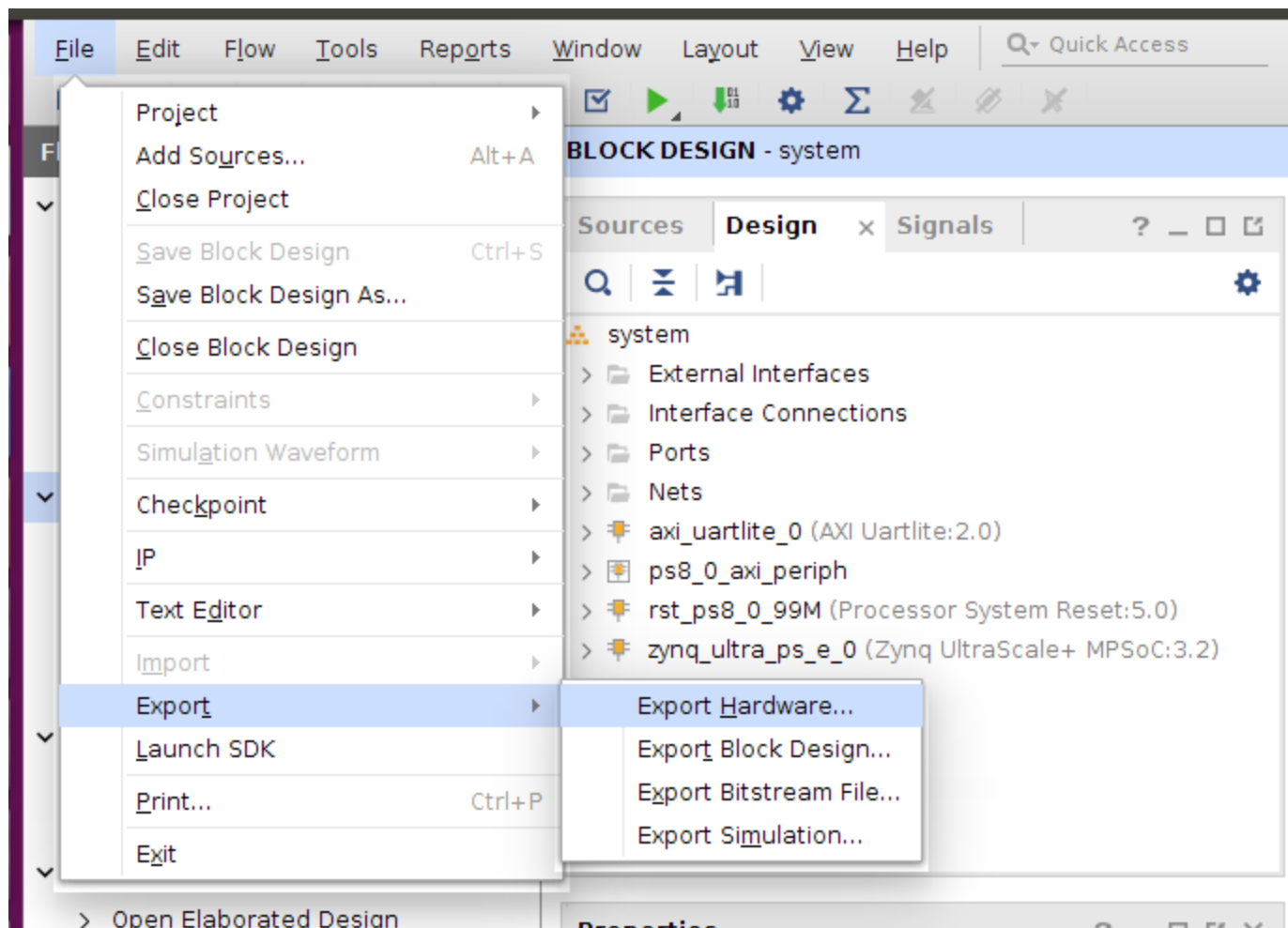
Do you want to proceed?

Yes No

Messages Log Reports Design Runs



19-2313] Loaded Vivado IP repository '/media/wrg/evo_860/Xilinx/Vivado/2018.2/data/ip'.
Time (s): cpu = 00:00:20 ; elapsed = 00:00:17 . Memory (MB): peak = 6564.570 ; gain = 526.922 ; free physical = 506 ; free virtual = 14152
order -filesset sources_1
f/media/wrg/evo_860/ultra96_study/dm2_ted/dm1/dm1_csrc/sources_1/hd/custom/custom_hdl



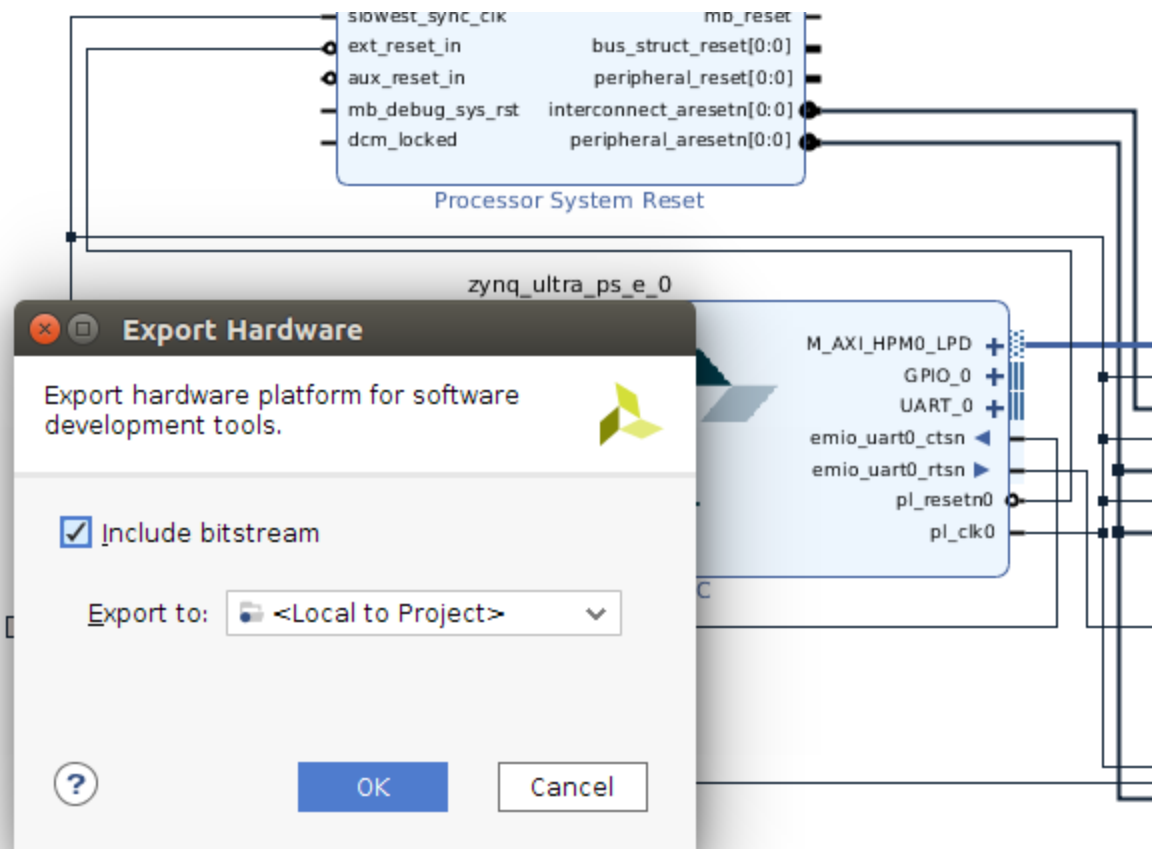
Reset:5.0)
e+ MPSoC:3.2)

? _ □ □ ×

← → ⚙

roperties

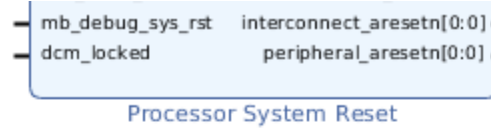
BT_ctsn [



Reports

Design Runs

ystem Reset:5.0)
aScale+ MPSoC:3.2)



Processor System Reset

zynq_ultra_ps_e_0

Export Hardware

Export hardware platform for software
development tools

M_AXI_HPM0_LPD
GPIO_0
UART_0

Bitstream out-of-date



Implementation run is out of date. Exported hardware information may be inconsistent with respect to the current state of the design. It is recommended that you re-run implementation and re-generate bitstream before doing hardware export.
Do you want to proceed?

Yes

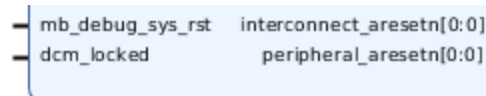
No

e properties

Log Reports Design Runs



ystem Reset:5.0)
aScale+ MPSoC:3.2)



Processor System Reset

zynq_ultra_ps_e_0

Export Hardware

Export hardware platform for software development tools.



M_AXI_HP0_LPD
GPIO_0
UART_0
emio_uart0_ctsn

AC
AR
S0
S0
MC
MC

Module Already Exported



An exported file for this module was found at this location. Do you want to overwrite it?

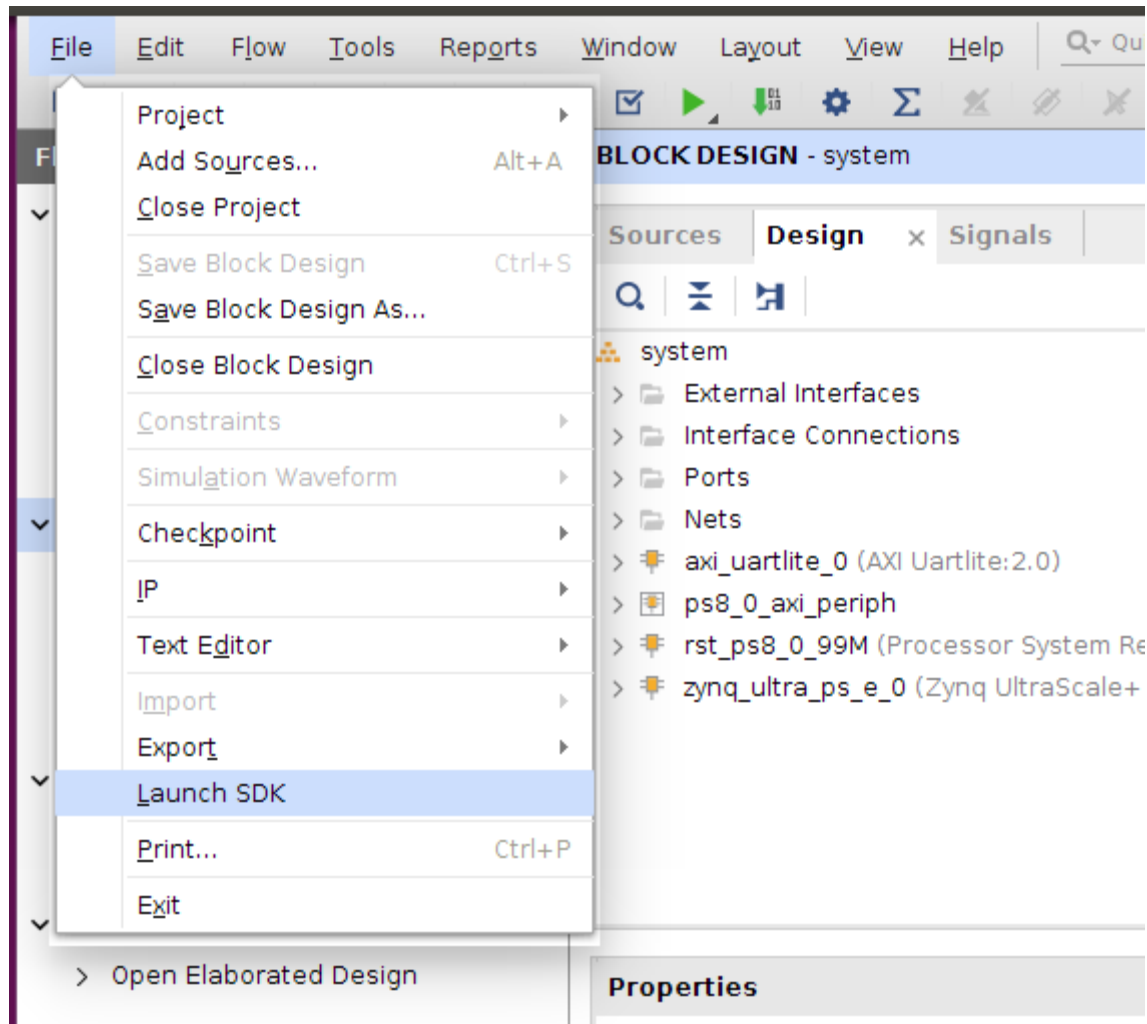
Yes

No

e properties

Log Reports Design Runs





Jartlite:2.0)

ocessor System Reset:5.0)

[Zynq UltraScale+ MPSoC:3.2)

```
3  #BT_HCI_RTS on FPGA / emio_uart0_ctsn connect to
4  set_property PACKAGE_PIN B7 [get_ports BT_ctsn]
5  #BT_HCI_CTS on FPGA / emio_uart0_rtsn
6  set_property PACKAGE_PIN B5 [get_ports BT_rtsn]
7
8  set_property IOSTANDARD LVCMOS18 [get_ports UART*]
9
10 #HD_GPIO_3 on FPGA / Connector pin 9 / UART0_rxd
11 #set_property PACKAGE_PIN C7 [get_ports UART0_rxd]
```

SDK

Software Development Kit

2018.2



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a/wrg/evo_860/ultra96_stud



3

r at 11:10:18 AM

ect Directory>/dml.srcs/constrs

Pages | Log | Reports | Design Runs



Welcome to Xilinx Software Development Kit

Importing Hardware Specification



Importing Hardware Specification



Always run in background



Cancel

Details >>

Run in Background



Quick Access

 Project Explorer 

▼ system_wrapper_hw_platform


psu_init_gpl.c

 `psu_init_gpl.h`

psu init.c

psu init.h

[psu_init.html](#)



system wrapper.bit

 system.hdf

system.hdf ✕

system wrapper hw platform 0 Hardware Platform Specific

Design Information

Target FPGA Device: xczu3eq

Part: xczu3eq-sbva484-1-i



Created With: Vivado 2018.2

Created On: Tue Jan 22 14:08:15 2019

Address Map for processor psu_cortexa53_[0-3]

Cell	Base Addr	High Addr	Slave I/f	M
psu_gdma_1	0xfd510000	0xfd51ffff		RI
psu_gdma_2	0xfd520000	0xfd52ffff		RI
psu_gdma_3	0xfd530000	0xfd53ffff		RI
psu_crf_apb	0xfd1a0000	0xfd2dffff		RI
psu_gdma_4	0xfd540000	0xfd54ffff		RI
psu_adma_2	0xffaa0000	0xffaaffff		RI
psu_gdma_5	0xfd550000	0xfd55ffff		RI
psu_adma_1	0xffa90000	0xffa9ffff		RI

Overview

 Target Connection 



► Hardware Server

- ▶ Linux TCF Agent

► QEMU TcfGdbClient

0 items

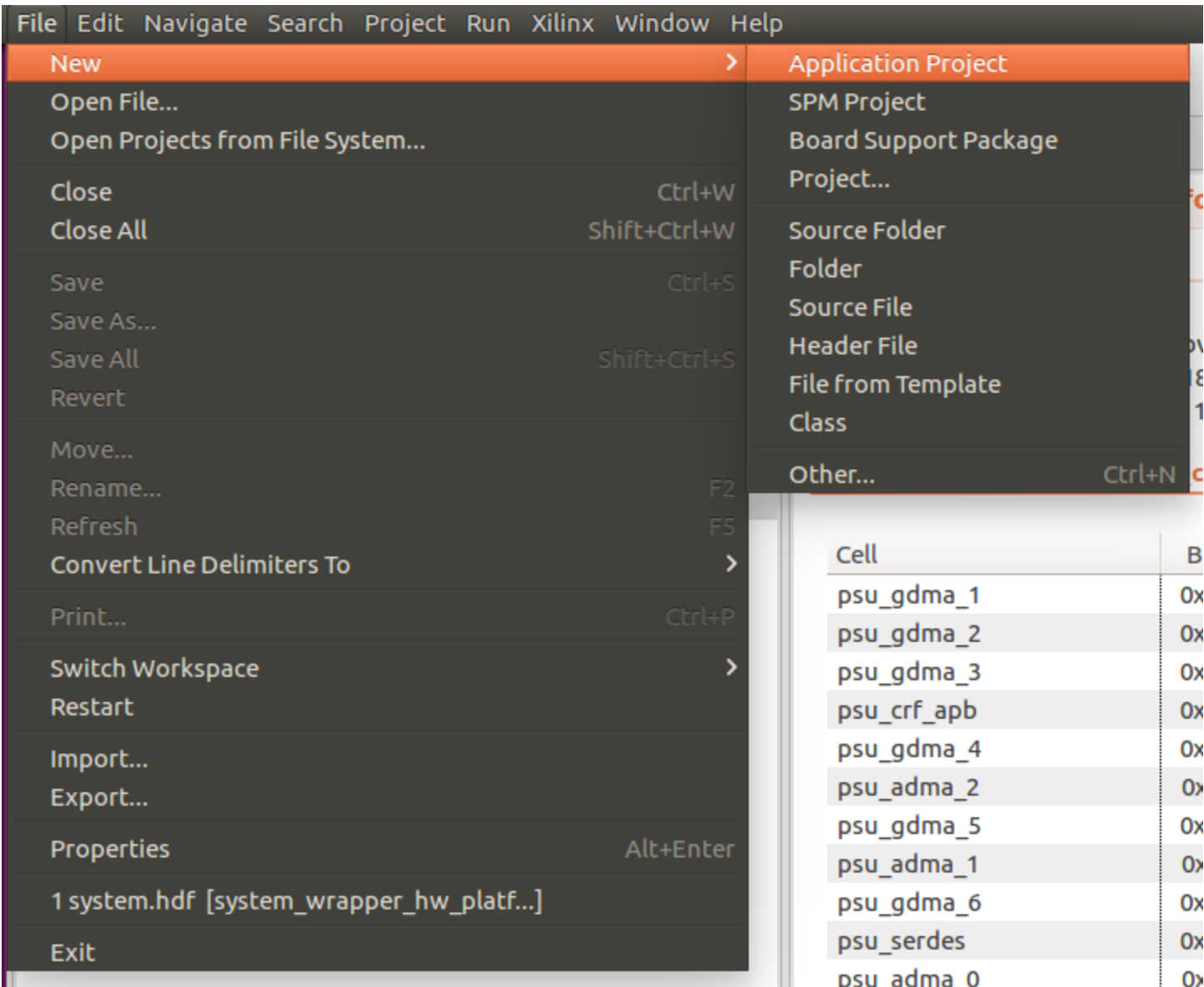
Description

Re

SDK Log



```
14:08:51 INFO : Registering command handle
14:08:51 INFO : Launching XSCT server: xs
14:08:51 INFO : XSCT server has started su
14:08:52 INFO : Successfully done setting
14:08:52 INFO : Successfully done setting
14:08:52 INFO : Processing command line op
```



Cell	B
psu_gdma_1	0x
psu_gdma_2	0x
psu_gdma_3	0x
psu_crf_apb	0x
psu_gdma_4	0x
psu_adma_2	0x
psu_gdma_5	0x
psu_adma_1	0x
psu_gdma_6	0x
psu_serdes	0x
psu adma 0	0x

New Project

Application Project

Create a managed make application project.



Project name:

☒ Use default location

Location:

Choose file system:

OS Platform:

Target Hardware

Hardware Platform:

Processor:

Target Software

Language: ☒ C ☐ C++

Compiler:

Hypervisor Guest:

Board Support Package: ☒ Create New

☐ Use existing



< Back

Next >

Cancel

Finish

Templates

Create one of the available templates to generate a fully-functioning application project.



Available Templates:

Empty Application

A blank C project.

FreeRTOS Hello World

FreeRTOS lwIP Echo Server

FreeRTOS lwIP TCP Perf Client

FreeRTOS lwIP TCP Perf Server

FreeRTOS lwIP UDP Perf Client

FreeRTOS lwIP UDP Perf Server

Libmetal AMP Demo

OpenAMP echo-test

OpenAMP matrix multiplication Demo

OpenAMP RPC Demo



< Back

Next >

Cancel

Finish



Project Explorer

- ▼ heartbeat
 - ▶ Includes
 - ▼ src
 - lscrip.ld
 - README.txt
- ▶ heartbeat_bsp
- ▼ system_wrapper_hw_platform_0
 - psu_init_gpl.c
 - psu_init_gpl.h
 - psu_init.c
 - psu_init.h
 - psu_init.html
 - psu_init.tcl
 - system_wrapper.bit
 - system.hdf

system.hdf

system.mss

heartbeat_bsp Board Support Package

[Modify this BSP's Settings](#)[Re-generate BSP Sources](#)

Target Information

This Board Support Package is compiled to run on the following target.

Hardware Specification: /media/wrg/evo_860/ultra96_study/dm2_trd/dm

Target Processor: psu_cortexr5_0

Operating System

Board Support Package OS.

Name: freertos10_xilinx

Version: 1.1

Description: FreeRTOS is a market leading open source RTOS

Documentation: Not found

Peripheral Drivers

Drivers present in the Board Support Package.

axi_uartlite_0 [uartlite](#)

[Documentation](#) [Import Examples](#)

psu_acpu_gic [scugic](#)

[Documentation](#) [Import Examples](#)

psu_adma_0 [zdma](#)

[Documentation](#) [Import Examples](#)

psu_adma_1 [zdma](#)

[Documentation](#) [Import Examples](#)

psu_adma_2 [zdma](#)

[Documentation](#) [Import Examples](#)

psu_adma_3 [zdma](#)

[Documentation](#) [Import Examples](#)

psu_adma_4 [zdma](#)

[Documentation](#) [Import Examples](#)

psu_adma_5 [zdma](#)

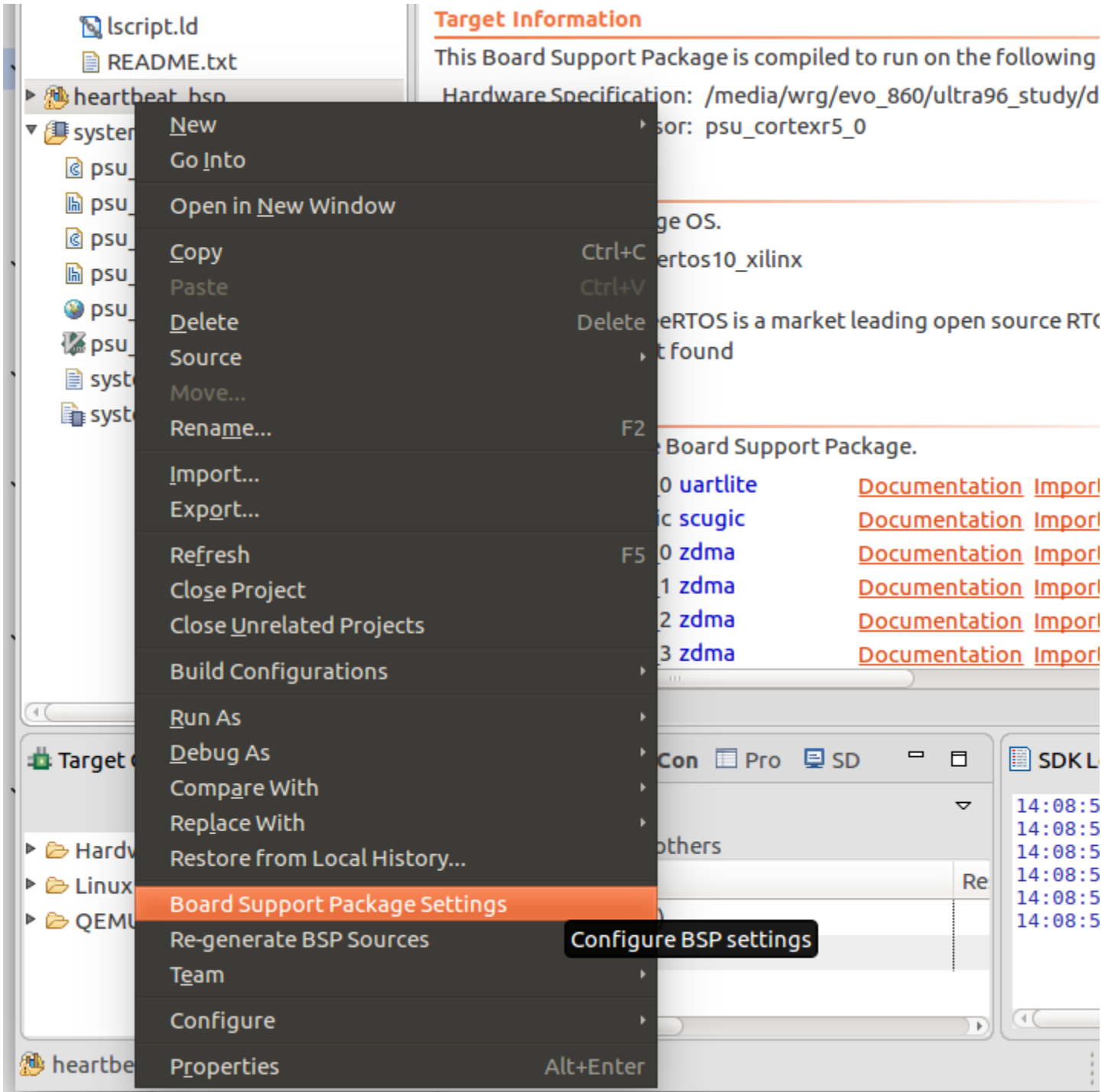
[Documentation](#) [Import Examples](#)

psu_adma_6 [zdma](#)

[Documentation](#) [Import Examples](#)

psu_adma_7 [zdma](#)

[Documentation](#) [Import Examples](#)





Board Support Package Settings

Control various settings of your Board Support Package.

▼ Overview

freertos10_xilinx

▼ drivers

psu_cortexr5_0

heartbeat_bsp

OS Type: *freertos10_xilin* FreeRTOS is a market leading open source RTOS

OS Version: 1.1 ▼

Target Hardware

Hardware Specification: /media/wrg/evo_860/ultra96_study/dm2_trd/dm1/dm1.sdk/system_wrapper_hw_platf

Processor: psu_cortexr5_0

Supported Libraries

Check the box next to the libraries you want included in your Board Support Package. You can configure the library in the navigator on the left.

	Name	Version	Description
<input type="checkbox"/>	libmetal	1.4	Libmetal Library
<input type="checkbox"/>	lwip202	1.1	lwip202 library: lwIP (light weight IP) is an open source TCP/IP stack configured
<input type="checkbox"/>	openamp	1.5	OpenAmp Library
<input type="checkbox"/>	xilffs	3.9	Generic Fat File System Library
<input type="checkbox"/>	xilflash	4.4	Xilinx Flash library for Intel/AMD CFI compliant parallel flash
<input type="checkbox"/>	xilfpga	4.1	XilFPGA library provides an interface to the Linux or bare-metal users for confi
<input type="checkbox"/>	xilisf	5.11	Xilinx In-system and Serial Flash Library
<input type="checkbox"/>	xilmfs	2.3	Xilinx Memory File System
<input type="checkbox"/>	xilpm	2.3	Power Management API Library for ZynqMP
<input type="checkbox"/>	xilsecure	3.1	Xilinx Secure Library provides interface to AES, RSA and SHA hardware engines
<input type="checkbox"/>	xilskey	6.5	Xilinx Secure Key Library supports programming efuse and bbram

여기서 **stdin** 과 **stdout** 을 변경해야함(다음 페이지)

Board Support Package Settings

Board Support Package Settings

Control various settings of your Board Support Package.

Overview

freertos10_xilinx

drivers

psu_cortexr5_0

Configuration for OS: freertos10_xilinx

Name	Value	Default	Type	Description
SYSINTC_SPEC	*			
SYSTMV_DEV	*			
SYSTMV_SPEC	true			
stdin	psu_uart_0	none	peripheral	stdin peripheral
stdout	psu_uart_0	none	peripheral	stdout peripheral
▶ enable_stm_event_trace	false	false	boolean	Enable event tracing thro
▶ hook_functions	true	true	boolean	Include or exclude applic
▶ kernel_behavior	true	true	boolean	Parameters relating to th
▶ kernel_features	true	true	boolean	Include or exclude kernel
▶ software_timers	true	true	boolean	Options relating to the s
▶ tick_setup	true	true	boolean	Configuration for enablin

Board Support Package Settings

Board Support Package Settings

Control various settings of your Board Support Package.



▼ Overview

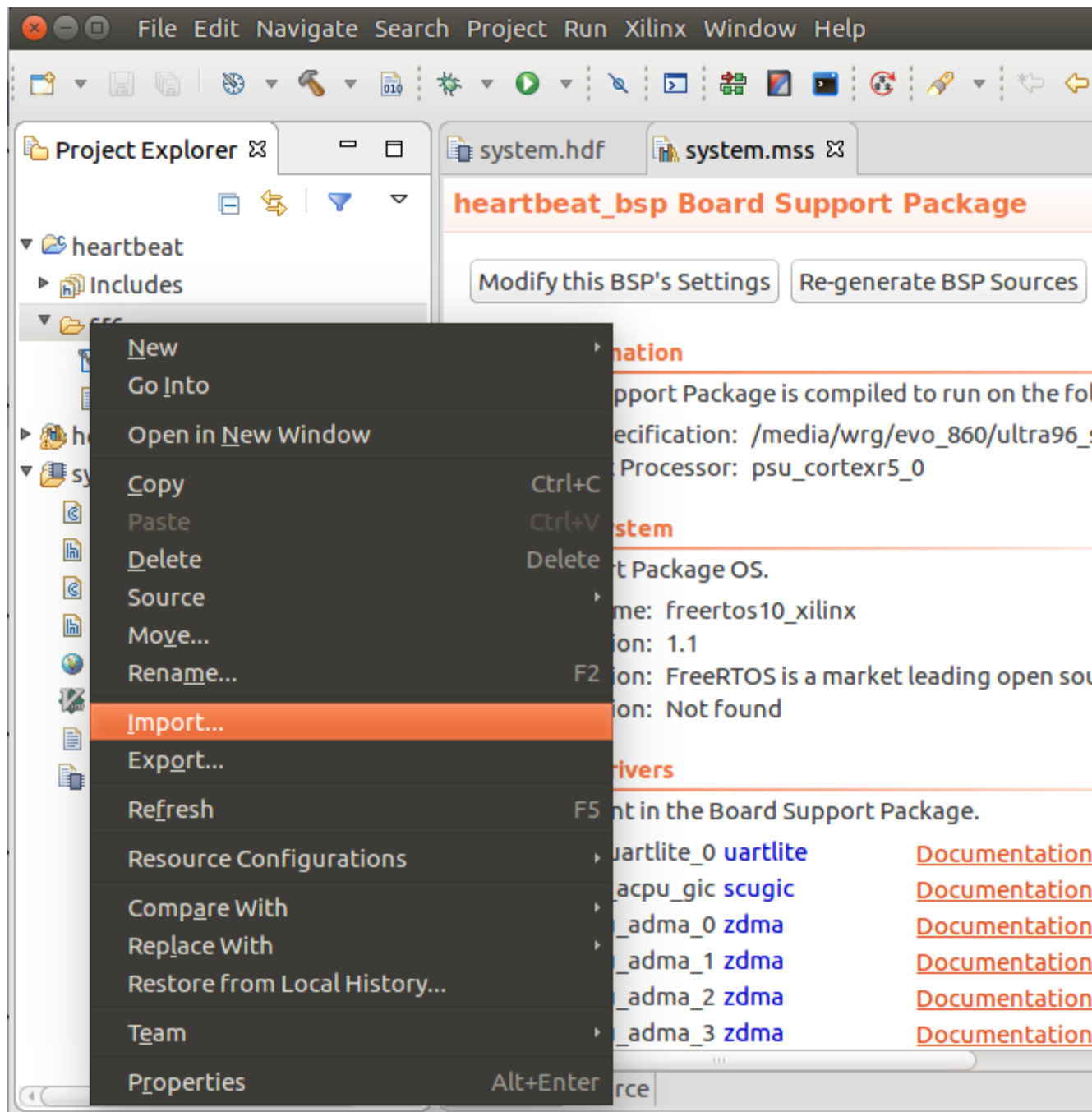
freertos10_xilinx

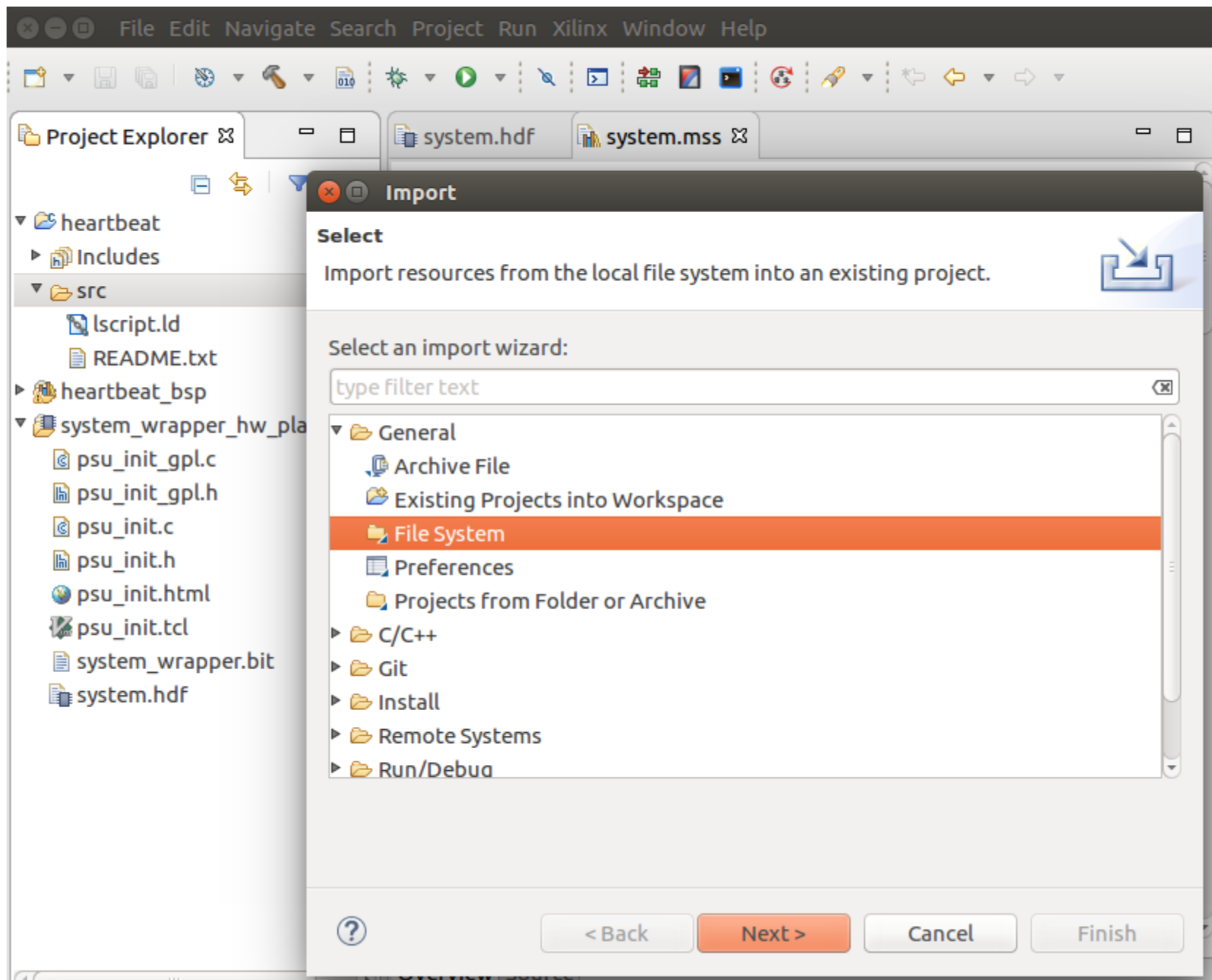
▼ drivers

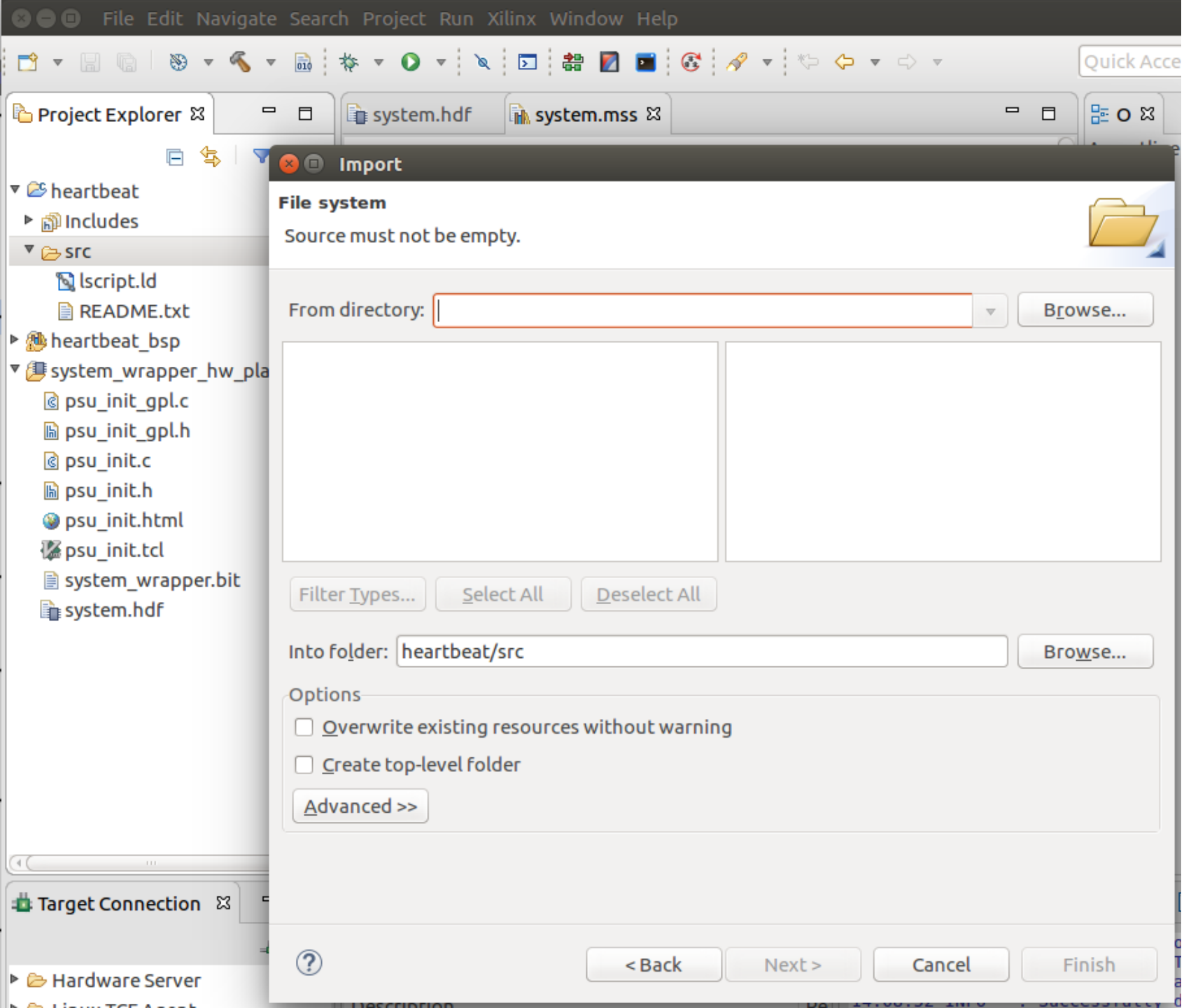
psu_cortexr5_0

Configuration for OS: [freertos10_xilinx](#)

Name	Value	Default	Type	Description
SYSINTC_SPEC	*			
SYSTMV_DEV	*			
SYSTMV_SPEC	true			
stdin	psu_uart_1	none	peripheral	stdin peripheral
stdout	psu_uart_1	none	peripheral	stdout peripheral
▶ enable_stm_event_trace	false	false	boolean	Enable event tracing throu
▶ hook_functions	true	true	boolean	Include or exclude applic
▶ kernel_behavior	true	true	boolean	Parameters relating to th
▶ kernel_features	true	true	boolean	Include or exclude kernel
▶ software_timers	true	true	boolean	Options relating to the s
▶ tick_setup	true	true	boolean	Configuration for enablin







Import from directory



evo_860

ultra96_study

dm2_trd

workspaces

ws_heartbeat

heartbeat

src



Create Folder

Places

Search

Recently Used

dm1

wrg

Desktop

File System

evo_860

220 GB Volume

새 볼륨

Documents

Music

Pictures

Videos

Downloads

Name



Size

Modified

heartbeat.c

11.2 kB

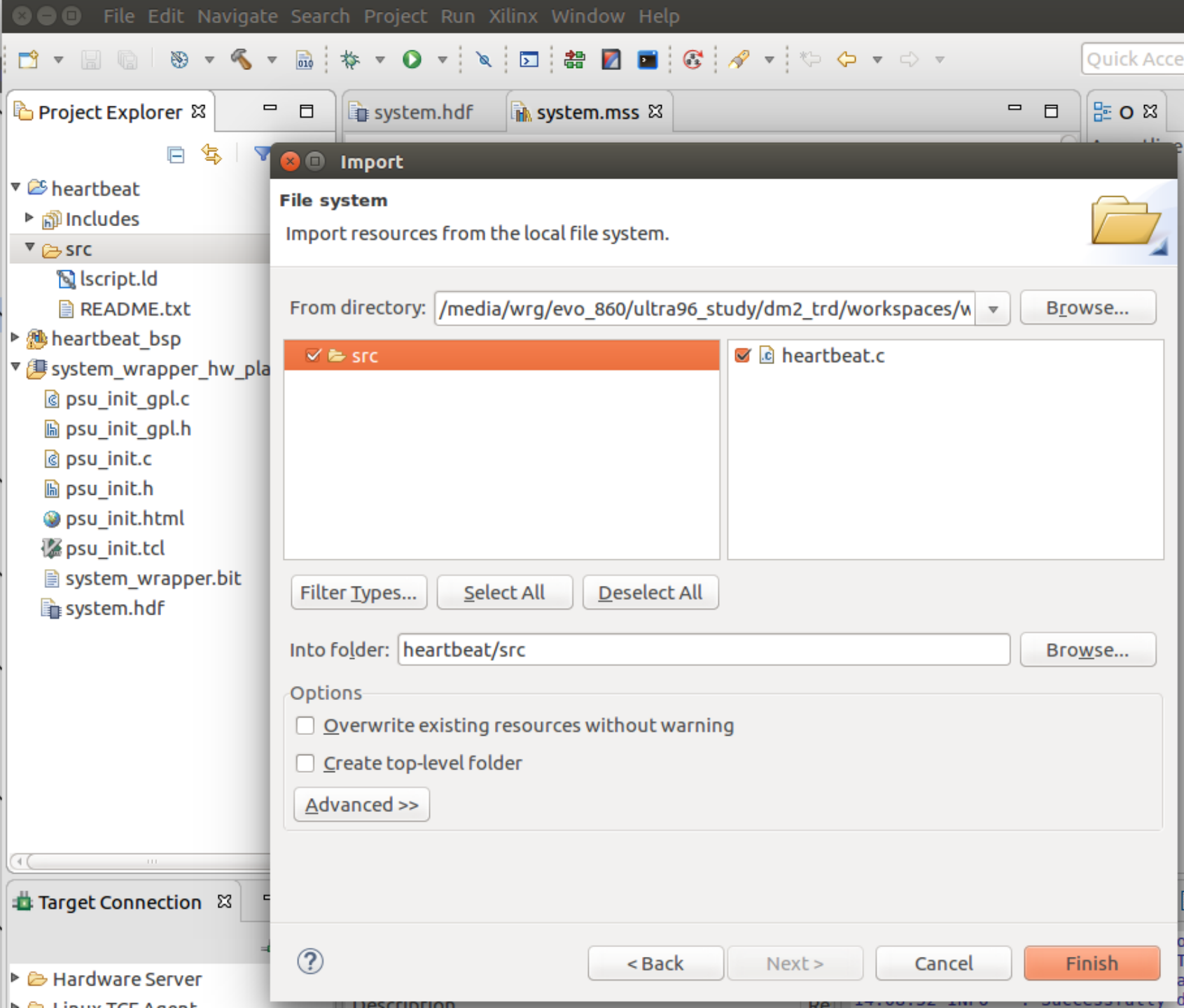
11:10



Select a directory to import from.

Cancel

OK



File Edit Navigate Search Project Run Xilinx Window Help

system.hdf system.mss lscript.ld

psu_r5_ddr_0_MEM_0 의 Base 와 Size,
그리고 Stack 과 Heap 의 크기를 조정해야한다(다음 페이지 참고)

Available Memory Regions

Name	Base Address	Size
psu_ocm_ram_0_MEM_0	0xFFFC0000	0x40000
psu_r5_0_atcm_MEM_0	0x0	0x10000
psu_r5_0_btcm_MEM_0	0x20000	0x10000
psu_r5_ddr_0_MEM_0	0x100000	0x7FE00000
psu_r5_tcm_ram_0_MEM_0	0x0	0x40000

Stack and Heap Sizes

Stack Size

Heap Size

Section to Memory Region Mapping

Section Name	Memory Region
.vectors	psu_r5_0_atcm_MEM_0
.text	psu_r5_ddr_0_MEM_0
.init	psu_r5_ddr_0_MEM_0
.fini	psu_r5_ddr_0_MEM_0

File Edit Navigate Search Project Run Xilinx Window Help

Projex

system.hdf system.mss *lscript.ld

Project Explorer

heartbeat

Binaries

Includes

Debug

src

heartbeat.c

lscript.ld

README.txt

heartbeat_bsp

system_wrapper

psu_init_gpl.c

psu_init_gpl.h

psu_init.c

psu_init.h

psu_init.html

psu_init.tcl

system_wrapper

system.hdf

Linker Script: lscript.ld

A linker script is used to control where different sections of an executable are placed in memory. In this page, you can define new memory regions, and change the assignment of sections to memory regions.

Available Memory Regions

Name	Base Address	Size
psu_ocm_ram_0_MEM_0	0xFFFFC0000	0x40000
psu_r5_0_atcm_MEM_0	0x0	0x10000
psu_r5_0_btcm_MEM_0	0x20000	0x10000
psu_r5_ddr_0_MEM_0	0x4E000000	0x1000000
psu_r5_tcm_ram_0_MEM_0	0x0	0x40000

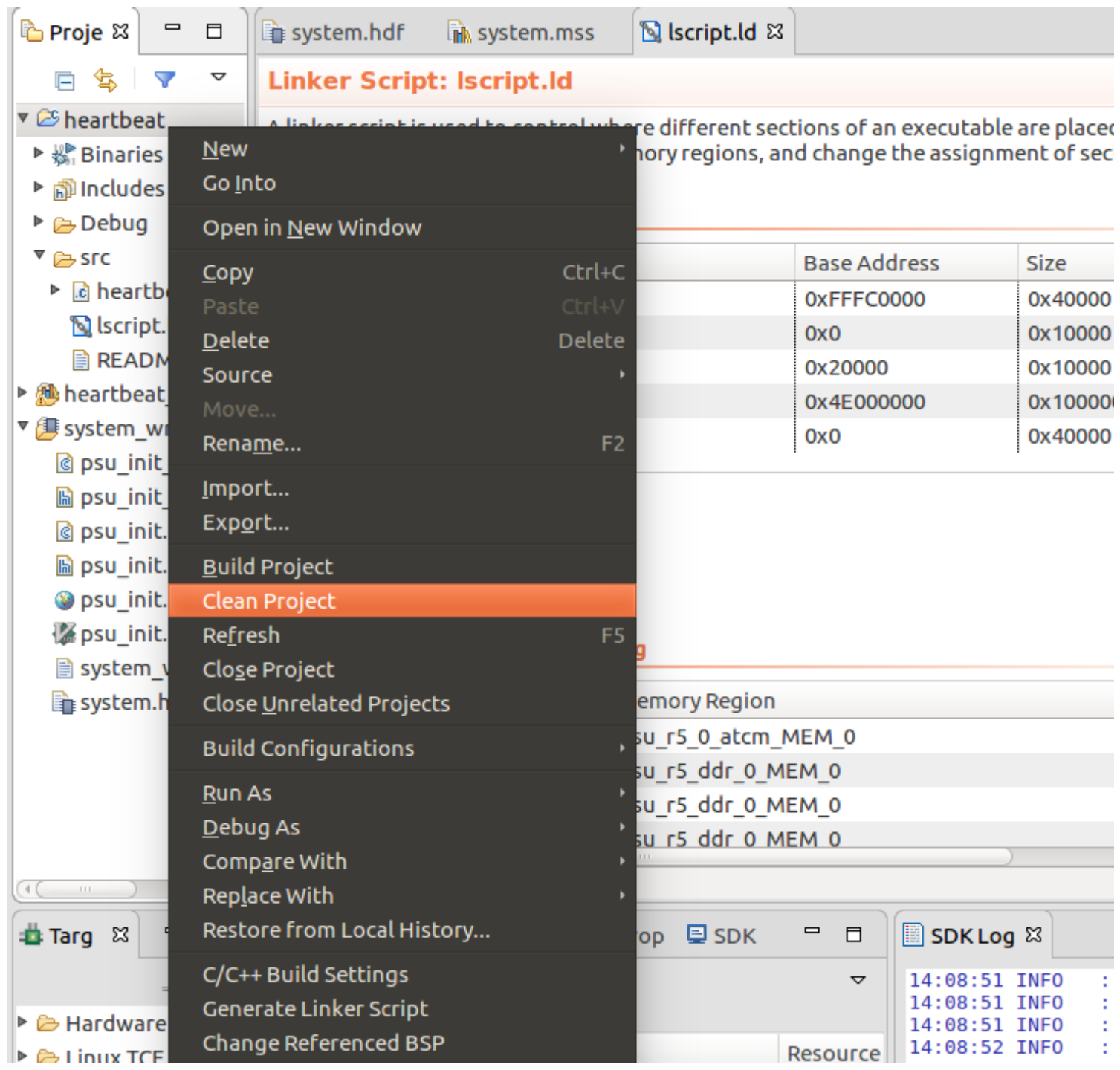
Stack and Heap Sizes

Stack Size

Heap Size

Section to Memory Region Mapping

Section Name	Memory Region
.vectors	psu_r5_0_atcm_MEM_0
.text	psu_r5_ddr_0_MEM_0
.init	psu_r5_ddr_0_MEM_0
.fini	psu_r5_ddr_0_MEM_0



Projex

system.hdfsystem.mssIscrip.ld

FileEditViewTools

heartbeatsystem

psu

Targ

HardLinux

system.hdfsystem.mssIscrip.ld

Linker Script: Iscrip.ld

A linker script is used to control where different sections of an executable are placed in memory regions, and change the assignment of

	Base Address	Size
	0xFFFFC0000	0x40
	0x0	0x10
	0x20000	0x10
	0x4E000000	0x10
	0x0	0x40

Building

Memory Region
psu_r5_0_atcm_MEM_0
psu_r5_ddr_0_MEM_0
psu_r5_ddr_0_MEM_0
psu_r5_ddr_0_MEM_0

PropSDK

SDK Log

14:08:51 INFO
14:08:51 INFO
14:08:51 INFO
14:08:52 INFO
14:08:52 INFO

Resource

New

Go Into

Open in New Window

CopyCtrl+C

PasteCtrl+V

DeleteDelete

Source

Move...

Rename...F2

Import...

Export...

Build Project

Clean Project

RefreshF5

Close Project

Close Unrelated Projects

Build Configurations

Run As

Debug As

Compare With

Replace With

Restore from Local History...

C/C++ Build Settings

Generate Linker Script

Change Referenced BSP

Project Explorer

- heartbeat
 - Binaries
 - heartbeat.elf - [arm/le]**
 - Includes
 - Debug
 - src
 - heartbeat.c
 - lscript.ld
 - README.txt
 - heartbeat_bsp
 - system_wrapper_hw_platf
 - psu_init_gpl.c
 - psu_init_gpl.h
 - psu_init.c
 - psu_init.h
 - psu_init.html
 - psu_init.tcl
 - system_wrapper.bit
 - system.hdf

system.hdf system.mss lscript.ld

Linker Script: lscript.ld

A linker script is used to control where different sections of an executable are placed in memory. In this page, you can define new memory regions, and change the assignment of sections to memory regions.

Available Memory Regions

Name	Base Address
	0xFFFC0000
psu_r5_0_atcm_MEM_0	0x0
psu_r5_0_btcm_MEM_0	0x20000
psu_r5_ddr_0_MEM_0	0x4E000000
psu_r5_tcm_ram_0_MEM_0	0x0

heartbeat.elf 파일이 나오면 된다.

Stack and Heap Sizes

Stack Size: 0x400

Heap Size: 0x400

Section to Memory Region Mapping

Section Name	Memory Region
.vectors	psu_r5_0_atcm_MEM_0
.text	psu_r5_ddr_0_MEM_0
.init	psu_r5_ddr_0_MEM_0
.fini	psu_r5_ddr_0_MEM_0

Summary Source


```

wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/dm1$ cd ..
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd$ ls
create_dsa.tcl  dm1.tcl          dm6.tcl  mipi_csi2_rx_hier.tcl  sdsoc
dm1             dm1.xdc          dm6.xdc  petalinux              tpg_input_hier.tcl
dm1_preset.tcl  dm6_preset.tcl  LICENSE  README.md              workspaces
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd$ cd petalinux/ultra96_trd/images/linux/
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/images/linux$ ls
bl31.bin      rootfs.cpio      rootfs.ext4      rootfs.testdata.json  vmlinux
bl31.elf      rootfs.cpio.bz2  rootfs.ext4.gz   system.bit             zynqmp_fsbl.elf
BOOT.BIN      rootfs.cpio.gz   rootfs.jffs2     system.dtb
Image         rootfs.cpio.gz.u-boot  rootfs.manifest  System.map.linux
image.ub      rootfs.ext3      rootfs.tar.bz2   u-boot.bin
pmufw.elf     rootfs.ext3.bz2  rootfs.tar.gz    u-boot.elf
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/images/linux$ cp
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/images/linux$ pet
alinux-package --force --boot --bif=../../dm2.bif
WARNING: You have specified BIF file, it will override all your other package boot settings.
INFO: Generating zynq binary package BOOT.BIN...

***** Xilinx Bootgen v2018.2
**** Build date : Jun 14 2018-20:09:18
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

[ERROR] : Can't read BIF file - dm2.bif
ERROR: Fail to create BOOT image
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/images/linux$ █

```

```
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/images/linux$ pet
alinux-package --force --boot --bif=../../dm2.bif
WARNING: You have specified BIF file, it will override all your other package boot settings.
INFO: Generating zynq binary package BOOT.BIN...

***** Xilinx Bootgen v2018.2
**** Build date : Jun 14 2018-20:09:18
** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

INFO: Binary is ready.
wrg@wrg-900X5N:/media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/images/linux$
```

```
PetaLinux environment set to '/media/wrg/evo_860/pkg/petalinux'
WARNING: /bin/sh is not bash!
bash is PetaLinux recommended shell. Please set your default shell to bash.
INFO: Checking free disk space
INFO: Checking installed tools
INFO: Checking installed development libraries
INFO: Checking network and other services
WARNING: No tftp server found - please refer to "PetaLinux SDK Installation Guide" for its
impact and solution
wrg@wrg-900X5N:~$ putty
```

```
/dev/ttyUSB1 - PuTTY
root@ultra96:~# ifconfig
lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1%4890784/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:2 errors:0 dropped:0 overruns:0 frame:0
          TX packets:2 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:140 (140.0 B)  TX bytes:140 (140.0 B)

usb0      Link encap:Ethernet  HWaddr 26:DF:1A:0B:D3:75
          inet addr:192.168.7.2  Bcast:0.0.0.0  Mask:255.255.255.0
          UP BROADCAST MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)

wlan0     Link encap:Ethernet  HWaddr 20:C3:8F:8C:AD:1C
          inet addr:192.168.219.117  Bcast:192.168.219.255  Mask:255.255.255.0
          inet6 addr: fe80::22c3:8fff:fe8c:ad1c%4890784/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:35 errors:0 dropped:0 overruns:0 frame:0
          TX packets:58 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:5004 (4.8 KiB)  TX bytes:10821 (10.5 KiB)

wlan1     Link encap:Ethernet  HWaddr 20:C3:8F:8C:AD:1D
          inet addr:192.168.2.1  Bcast:192.168.2.255  Mask:255.255.255.0
          inet6 addr: fe80::22c3:8fff:fe8c:ad1d%4890784/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:33 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:6618 (6.4 KiB)

root@ultra96:~#
```

```

wrg@wrg-900X5N: /media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/im
ages/linux$ ls
bl31.bin          rootfs.cpio          rootfs.ext4.gz      system.dtb
bl31.elf          rootfs.cpio.bz2      rootfs.jffs2        System.map.linux
BOOT.BIN          rootfs.cpio.gz       rootfs.manifest     u-boot.bin
heartbeat.elf     rootfs.cpio.gz.u-boot rootfs.tar.bz2      u-boot.elf
Image            rootfs.ext3          rootfs.tar.gz       vmlinux
image.ub         rootfs.ext3.bz2      rootfs.testdata.json zynqmp_fsbl.elf
pmufw.elf        rootfs.ext4          system.bit
wrg@wrg-900X5N: /media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/im
ages/linux$ scp BOOT.BIN root@192.168.2.1:/media/card
^Cwrg@wrg-900X5N: /media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/
ages/linux$ ping 192.168.2.1
PING 192.168.2.1 (192.168.2.1) 56(84) bytes of data.
^C
--- 192.168.2.1 ping statistics ---
6 packets transmitted, 0 received, 100% packet loss, time 5106ms

wrg@wrg-900X5N: /media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/im
ages/linux$ ping 192.168.2.1
PING 192.168.2.1 (192.168.2.1) 56(84) bytes of data.
64 bytes from 192.168.2.1: icmp_seq=1 ttl=64 time=8.21 ms
^C
--- 192.168.2.1 ping statistics ---
1 packets transmitted, 1 received, 0% packet loss, time 0ms
rtt min/avg/max/mdev = 8.210/8.210/8.210/0.000 ms
wrg@wrg-900X5N: /media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/im
ages/linux$ scp BOOT.BIN root@192.168.2.1:/media/card
root@192.168.2.1's password:
BOOT.BIN                               100% 5741KB 820.1KB/s   00:07
wrg@wrg-900X5N: /media/wrg/evo_860/ultra96_study/dm2_trd/petalinux/ultra96_trd/im
ages/linux$ █

```

```

wlan1    Link encap:Ethernet  HWaddr 20:C3:8F:8C:AD:1D
          inet addr:192.168.2.1  Bcast:192.168.2.255  Mask:255.255.255.0
          inet6 addr: fe80::22c3:8fff:fe8c:ad1d%4890784/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:33 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:6618 (6.4 KiB)

```

```

root@ultra96:~# [ 807.627605] random: crng init done

```

```

root@ultra96:~# ls
root@ultra96:~# ls /media/card/
BOOT.BIN  Image  image.ub  system.dtb
root@ultra96:~# ls /media/card/
BOOT.BIN Image image.ub system.dtb
root@ultra96:~# █

```



```
[ 1348.142779] wlc0: down
done.
[ OK ] watchdog: [ OK ]
Sending all processes the TERM signal..
Sending all processes the KILL signal..
Unmounting remote filesystems..
Deactivating swap..
Unmounting local filesystems..
[ 1353.661345] EXT4-fs (mmcblk0p2): re-mounted. Opts: (null)
Rebooting... [ 1355.814660] usb 1-1: USB disconnect, device number 2
[ 1355.819570] usb 1-1.4: USB disconnect, device number 3
[ 1355.887262] reboot: Restarting system
Xilinx Zynq MP First Stage Boot Loader
Release 2018.2 Jan 22 2019 - 23:03:42
Hello from Freertos example main
Rx task (task number: 0) received string from Tx task: I am alive
Rx task (task number: 1) received string from Tx task: I am alive
Rx task (task number: 2) received string from Tx task: I am alive
Rx task (task number: 3) received string from Tx task: I am alive
Rx task (task number: 4) received string from Tx task: I am alive
Rx task (task number: 5) received string from Tx task: I am alive
Rx task (task number: 6) received string from Tx task: I am alive
Rx task (task number: 7) received string from Tx task: I am alive
Rx task (task number: 8) received string from Tx task: I am alive
Rx task (task number: 9) received string from Tx task: I am alive
Rx task (task number: 10) received string from Tx task: I am alive
Rx task (task number: 11) received string from Tx task: I am alive
Rx task (task number: 12) received string from Tx task: I am alive
Rx task (task number: 13) received string from Tx task: I am alive
Rx task (task number: 14) received string from Tx task: I am alive
Rx task (task number: 15) received string from Tx task: I am alive
Rx task (task number: 16) received string from Tx task: I am alive
Rx task (task number: 17) received string from Tx task: I am alive
Rx task (task number: 18) received string from Tx task: I am alive
Rx task (task number: 19) received string from Tx task: I am alive
Rx task (task number: 20) received string from Tx task: I am alive
Rx task (task number: 21) received string from Tx task: I am alive
Rx task (task number: 22) received string from Tx task: I am alive
Rx task (task number: 23) received string from Tx task: I am alive
Rx task (task number: 24) received string from Tx task: I am alive
Rx task (task number: 25) received string from Tx task: I am alive
```