

TI DSP, MCU 및 Xilinx Zynq FPGA 프로그래밍 전문가 과정

(Altium Artwork Practice)

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[1] BOM 작성

Bill of Materials

<http://www.greatek.com.tw/product4.html>

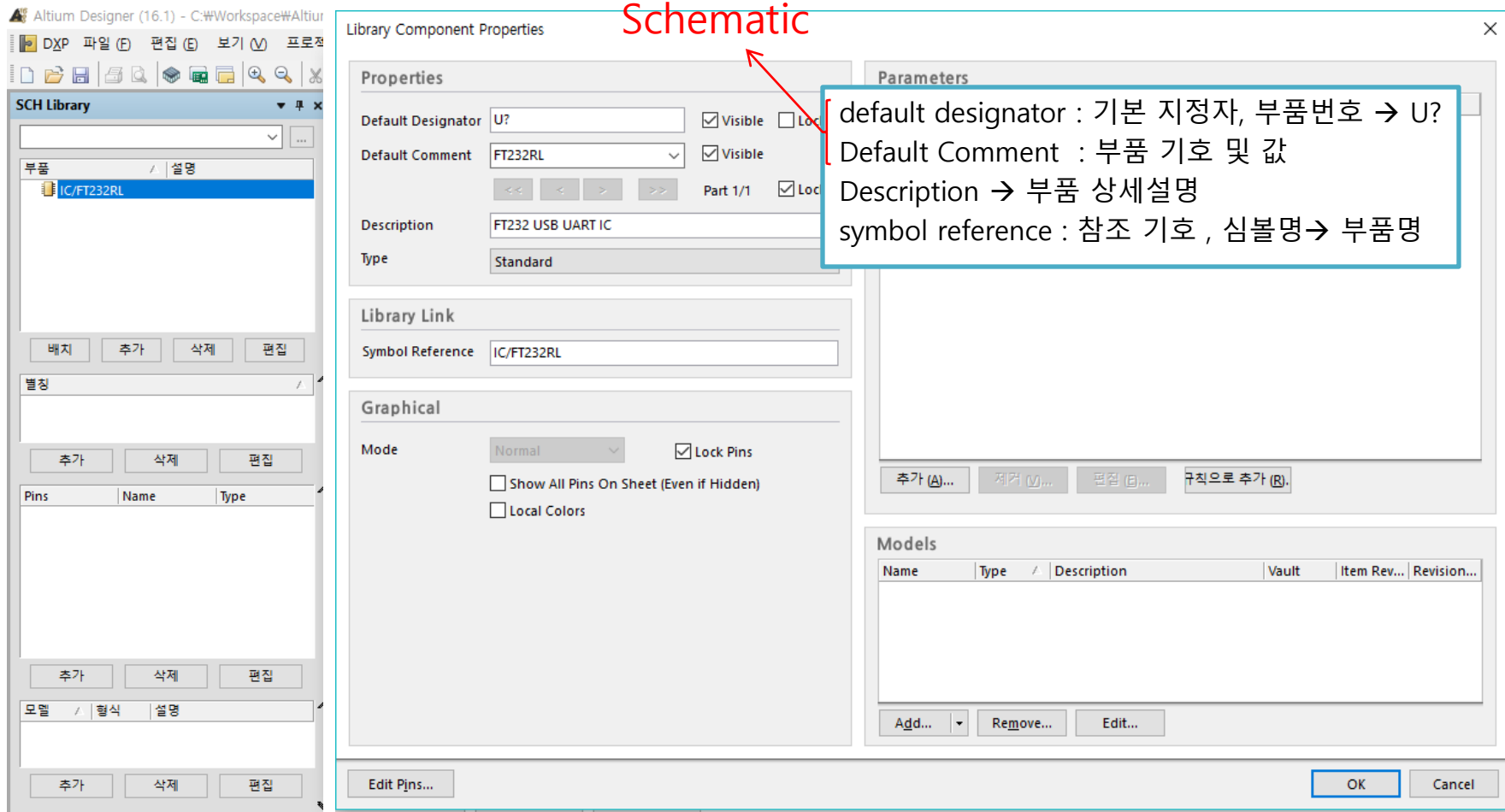
→ IC Package에 따라 크기가 정해져 있다.



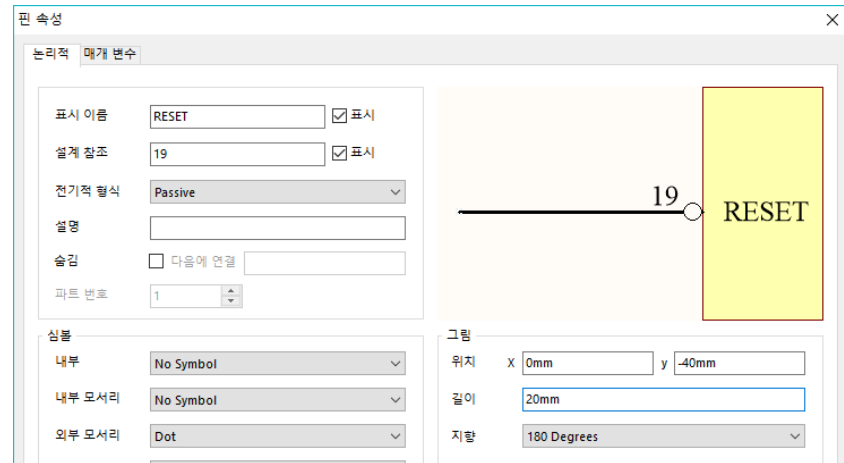
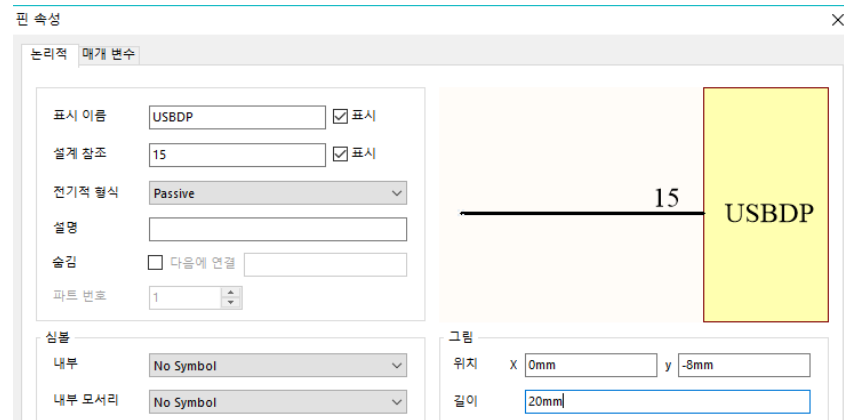
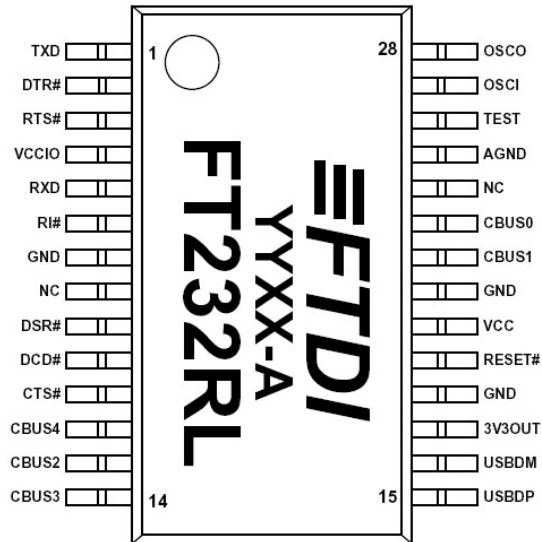
부품명	URL	Package
FT232RL	http://www.devicemart.co.kr/1057895	SSOP-28
ISO7221	http://www.ti.com/lit/ds/symlink/iso7220a.pdf	SOIC-8
Mini USB	Mini USB.pdf	AB Type
Pin Header	http://www.devicemart.co.kr/1312958	2.54mm Pitch
1kohm 저항	http://www.devicemart.co.kr/19277	2012
0.1uF 캐패시터	http://www.devicemart.co.kr/8191	2012
10uF/16V 탄탈콘덴서	http://www.devicemart.co.kr/5000	A Size
LED	http://www.devicemart.co.kr/2745	2012

[2] 라이브러리 작성

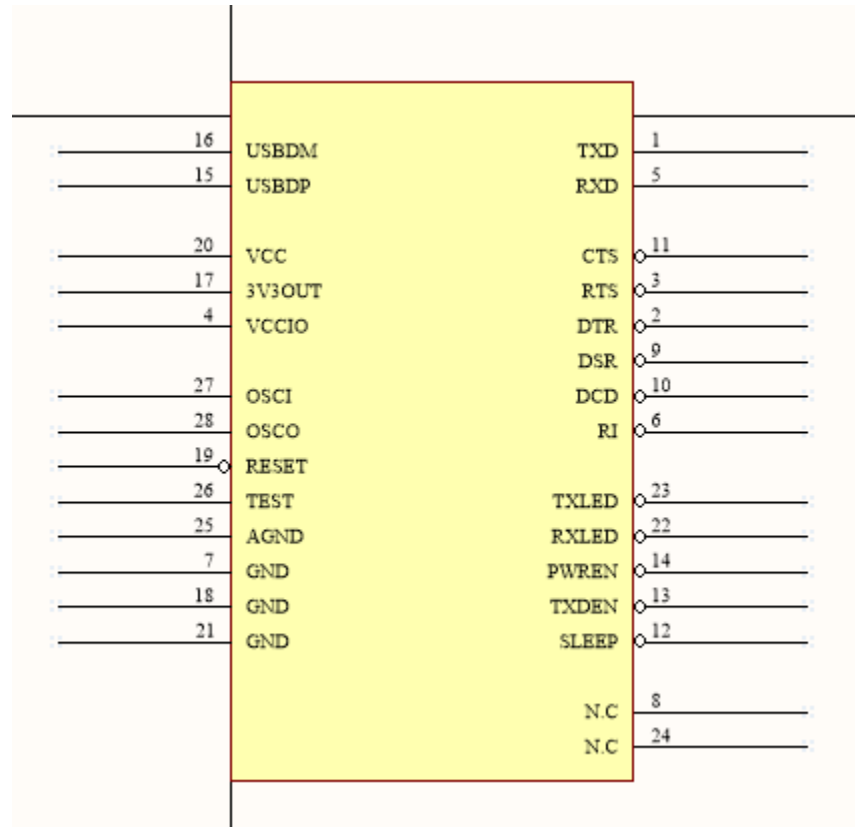
1. FT232 Schematic 라이브러리 생성



IC의 패키지를 보고, 표시이름과 설계참조를 다음과 같이 변경



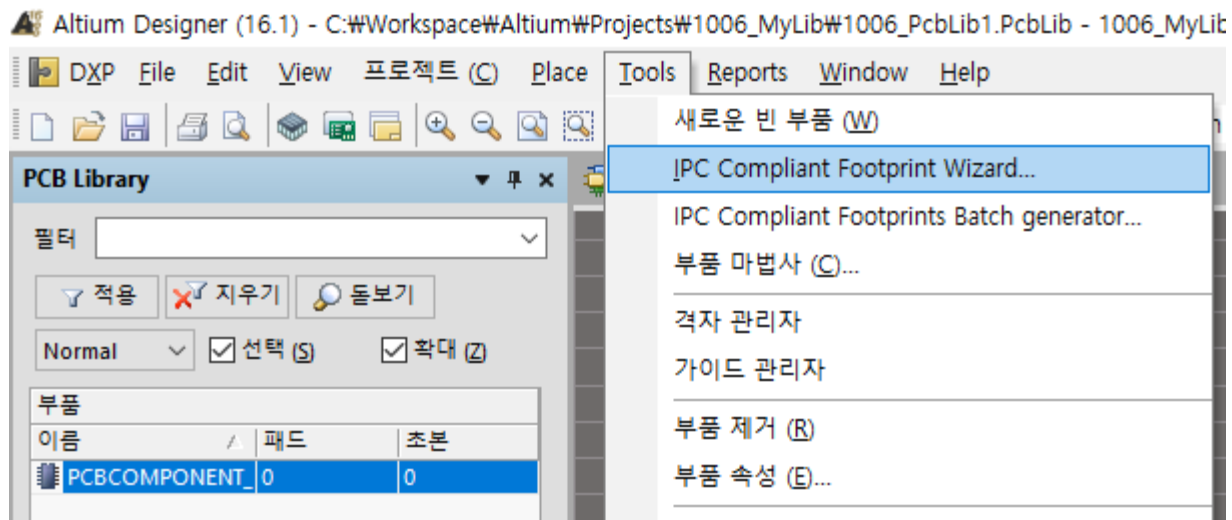
다음과 같이 schematic library 생성



PCB document 작성

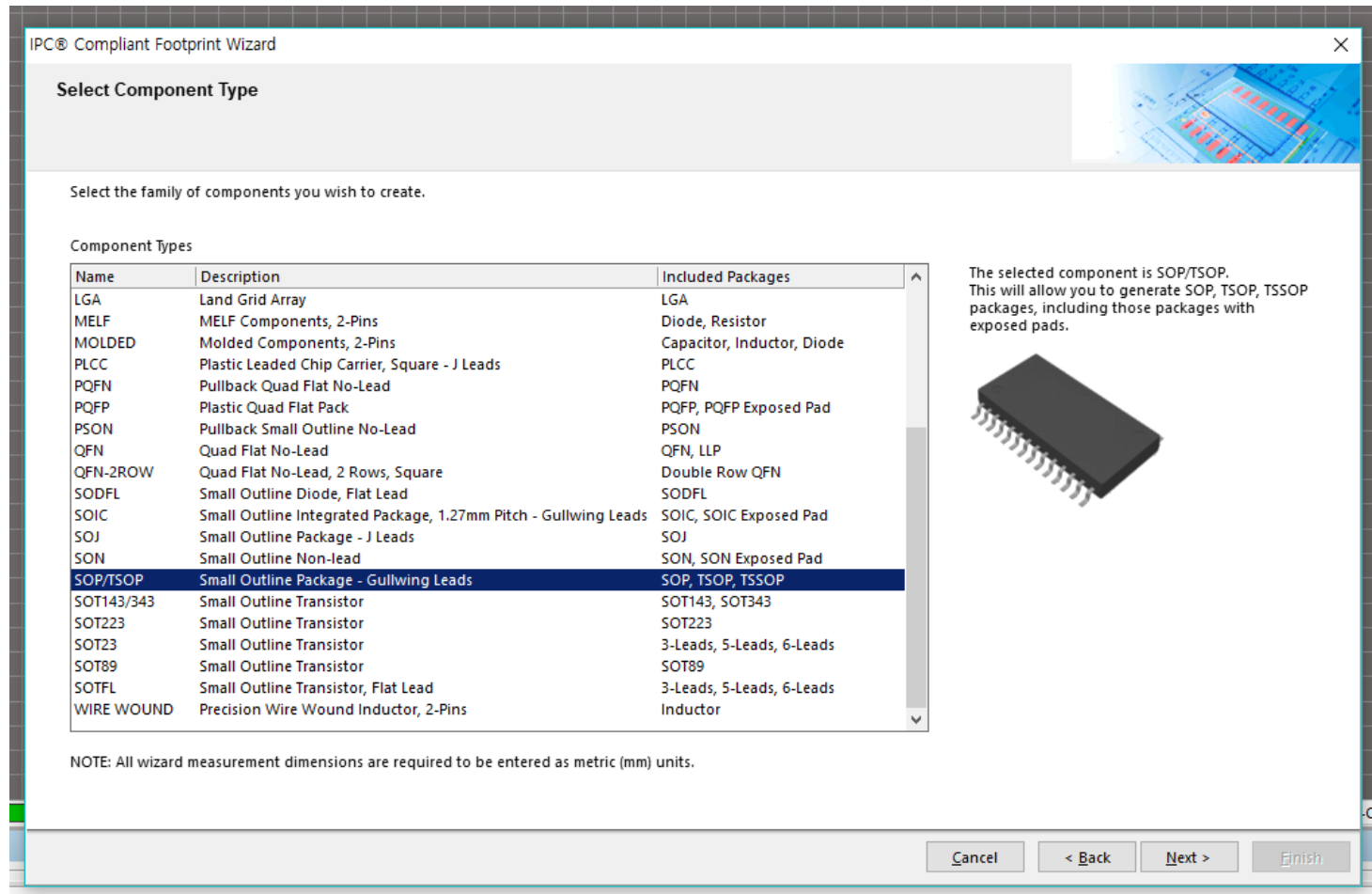
IPC Compliant Footprint Wizard 사용

IPC 준수, [IPC \(단체\)](#): 국제전자산업표준협회(IPC Association Connecting Electronics Industries)
→ 즉, PCB 표준에 따른 Footprint를 만들겠다는 의미



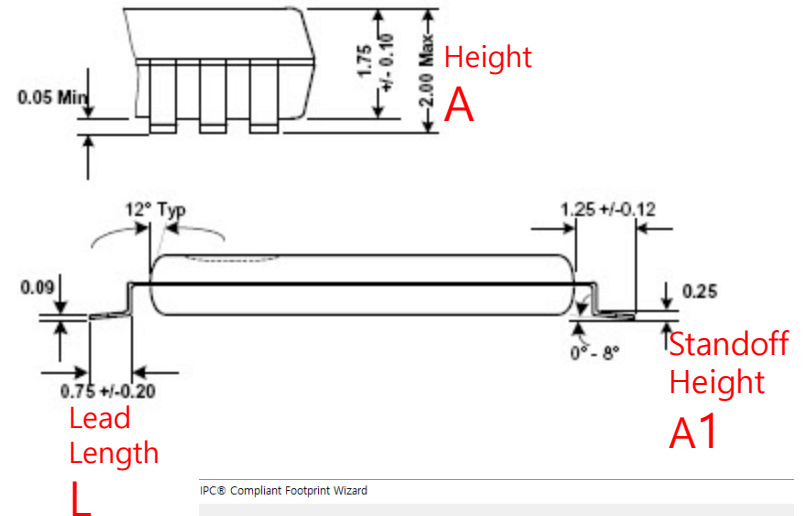
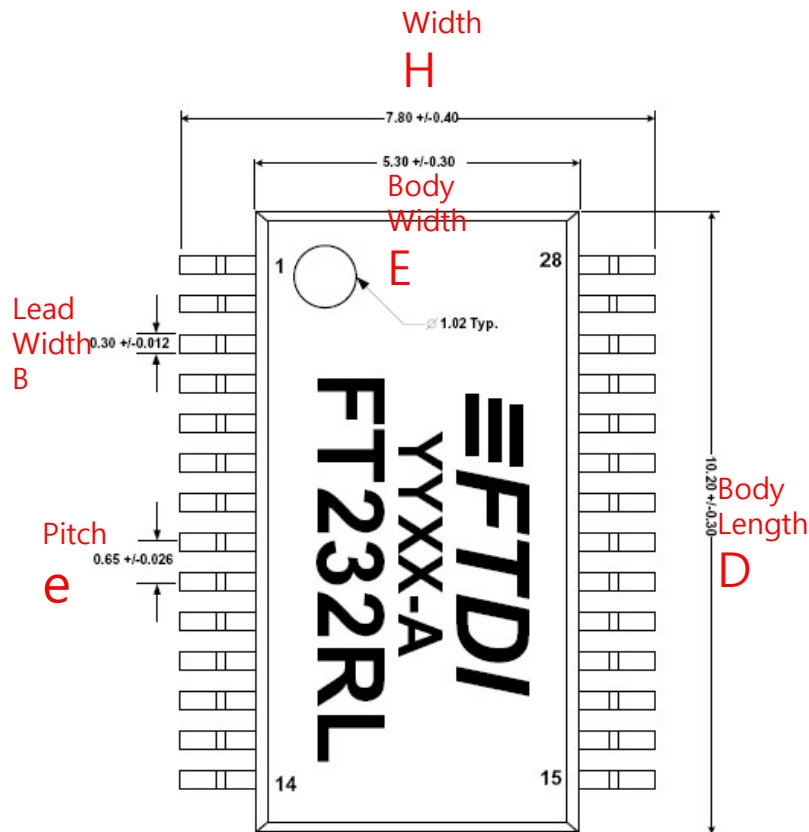
<https://blog.naver.com/mjg5080/124266444>

→ SOP, SSOP, TSOP, TSSOP, UTSOP 형식의 차이점



Datasheet의 패키지 크기부분을 참조하여 Package Dimensions(부품 사이즈) 기록

SSOP-28 Package Dimensions



IPC® Compliant Footprint Wizard

SOP/T SOP Package Dimensions

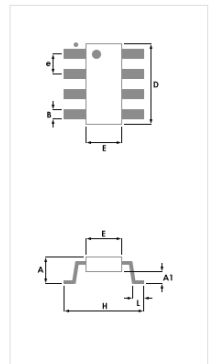
Enter the required package values.

Overall Dimensions

Width Range (H)	Minimum	7.4mm
	Maximum	8.2mm
Maximum Height (A)		2mm
Minimum standoff height (A1)		0.25mm
Body width range (E)	Minimum	5mm
	Maximum	5.6mm
Body length range (D)	Minimum	9.9mm
	Maximum	10.5mm

Pin Information

Number of pins		28
Lead Width Range (B)	Minimum	0.288mm
	Maximum	0.312mm
Lead Length Range (L)	Minimum	0.55mm
	Maximum	0.95mm
Pitch (e)		0.65mm



☐ Generate STEP Model Preview

Thermal Pad Dimensions

단열패드 추가할 경우 체크하고, 크기를 입력

IPC® Compliant Footprint Wizard

SOP/TSOP Package Thermal Pad Dimensions

Enter the required thermal pad values.

☐ Add Thermal Pad

Thermal Pad Range (E2)

Minimum

0mm

Maximum

0mm

Thermal Pad Range (D2)

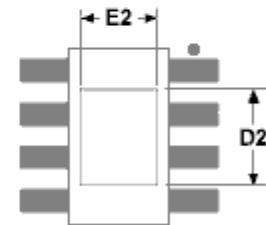
Minimum

0mm

Maximum

0mm

Bottom View



Package Heel Spacing

(부품 몸체 사이즈)

IPC® Compliant Footprint Wizard

SOP/TSOP Package Heel Spacing

Enter the heel spacing values.

$$7.4 - (0.95 \times 2) = 5.5\text{mm}$$
$$H_{\min} - (L_{\max} \times 2)$$

The minimum heel spacing is calculated by subtracting twice the Maximum Lead Width Range.

The maximum heel spacing is calculated by adding the tolerance on the inner distance between the heels of the opposing rows of leads to the minimum heel spacing.

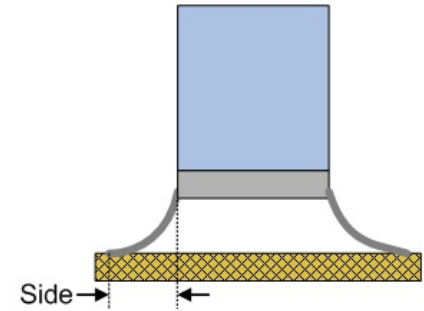
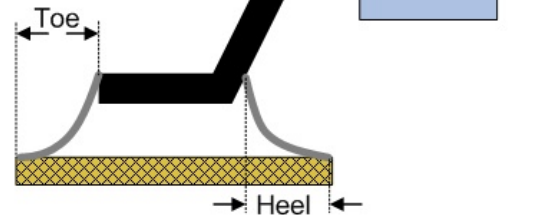
☐ Use calculated values

S Minimum

6mm

S Maximum

6.3mm



Solder Fillets for Surface Mount Footprints

End View



마주보는 Lead의 Heel 사이의 내부 거리에 대한 허용오차를 더한다.
(Minimum heel spacing에)

*. S Maximum은 커도 문제는 안될 것
S Minimum의 경우는 문제 될 수 있으므로 주의하자

리드 납땜 형태에 따른, Fillet Size

(납땜 형태에 따라 패드에 여유를 주기 위함)

IPC® Compliant Footprint Wizard

SOP/TSOP Solder Fillets

Enter the required fillet values.

Solder fillet

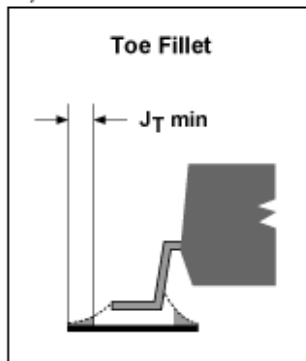
솔더 응고 후 접속부에 형성되는 솔더 표면의 형태로
통상 오목한 표면 형태가 바람직함.

Solder fillet refers to the shape of the solder joint between the component lead and the PCB pad. Adequate fillet is required to ensure both the strength and reliability of the solder joints. A solder joint may be described by three fillets: toe, heel, and side. Minimum values for solder fillets at the toe, heel and side of the component lead have been determined by IPC®, based on industry empirical knowledge and reliability testing. These values are displayed below; however they may be adjusted to suit specific conditions.

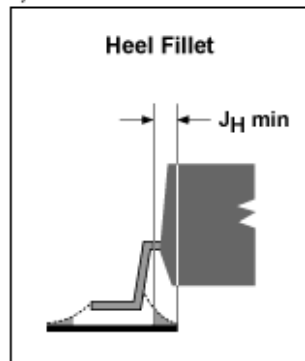
☒ Use default values

Board density Level **Level B - Medium density** ▼

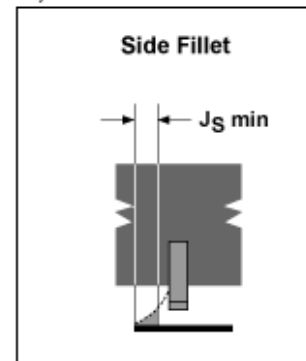
Toe Fillet (J_T
Min) 0.35mm



Heel Fillet (J_H
Min) 0.35mm



Side Fillet (J_S
Min) 0.03mm



부품 전체 폭에 대한 tolerance(허용오차) 입력

IPC® Compliant Footprint Wizard

SOP/T SOP Component Tolerances

Enter the required component tolerance values.

Component manufacturers usually specify the minimum and maximum value for each package dimension. Component tolerance ranges are derived by subtracting the minimum value from the maximum. These ranges may be adjusted based upon experience from suppliers.

☒ Use calculated component tolerance

Tolerance on the overall width of the component,
including leads

0.8mm

Tolerance on the inner distance between the heels of the opposing
rows of leads

1.0267mm

Tolerance on the width of the
component leads

0.024mm

제조 및 배치와 관련된 tolerance (실장패키지 허용오차) 입력 IPC 규격에서 벗어날 수 있으므로 default로 진행

IPC® Compliant Footprint Wizard

SOP/TSOP IPC Tolerances

Enter the required tolerance values.

IPC® specifies certain tolerances for a number of standardized surface-mount package types. These tolerances are assumed by this wizard in order to calculate a corresponding PCB footprint. You can modify here the tolerances related to fabrication and placement. Such modification may result in the creation of non IPC® compliant PCB footprints.

☒ Use Default Values

Fabrication Tolerance Assumption

This allowance may be adjusted according to the accuracy of the PCB fabricator to reproduce the PCB footprint dimensions on the printed board.

Placement Tolerance Assumption

This allowance may be adjusted according to the accuracy of the assembler to center the component on the PCB footprint.

Courtyard Excess

The Courtyard of a PCB footprint defines the area required for electrical and mechanical clearance of both the component and its footprint. The dimensions of the courtyard boundary are calculated by the addition of a courtyard excess to the maximum dimensions of the combined component and footprint. The value of the courtyard excess differs according to the density level of the printed circuit board.

Pad 크기, 모양, 간격 입력

IPC® Compliant Footprint Wizard

SOP/TSOP Footprint Dimensions

The footprint dimensions can now be inferred from the package dimensions.
You can review and modify them here.

The footprint has 28 pads and a pitch (P) of 0.65mm. You can modify here the calculated dimensions of the footprint.

☐ Use calculated footprint values

Pad Dimensions

X

Y

Pad Spacing

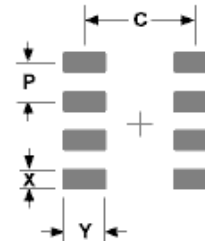
C

Pad Shape

☐ Rounded

☒ Rectangular

Top View



실크스크린 두께설정

IPC® Compliant Footprint Wizard

SOP/TSOP Silkscreen Dimensions

The silkscreen dimensions can now be inferred from the package dimensions.
You can review and modify them here.

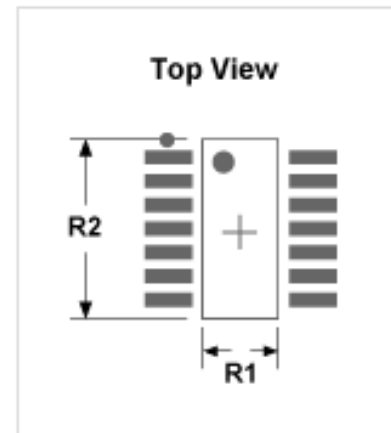
The recommended silkscreen dimensions have been calculated based on the above selection of package and dimensions.
On this page you can further refine the silkscreen aspect by defining the used line width and by modifying the calculated silkscreen dimensions.

Silkscreen Line Width

☒ Use calculated silkscreen dimensions

R1

R2



조립시 필요한 부품크기 (Courtyard, Assembly, Component)

<http://blog.mbedded.ninja/electronics/general/altium/altium-tricks-and-standards>
→PCB 각 Layer의 Standard한 역할

IPC® Compliant Footprint Wizard

SOP/TSOP Courtyard, Assembly and Component Body Information

The mechanical dimensions can now be inferred from the package dimensions.
You can review and modify them here.

Cho
eith
the
whi

Mechanical 15
(M15)

탑 레이어의 어셈블리 정보. 이는 일반적으로 부품의 원점에 십자 모양을 포함함. (IPC 호환 풋프린트 워저드로 풋프린트를 만들 때 초록색 레이어로 십자 표시가 이루어져 있는게 이것이며, 주로 어셈블리 정보를 만드는 데 쓰입니다. EAGLE 캐드 라이브러리를 가져올 때 초록색으로 이루어져 있는 부분이 이것입니다.)

☒ Add Courtyard Information

☒ Use calculated values

V1 Line Width
V2 Layer

☒ Add Assembly Information

☐ Use calculated values

A Line Width
B Layer

☒ Add Component Body Information

☐ Use calculated values

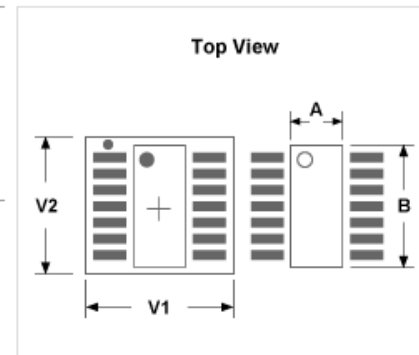
Width
Length

Mechanical 13
(M13)

Top layer component body information (3D models and mechanical outlines, paired with M14).

Mechanical 14
(M14)

Bottom layer component body information (3D models and mechanical outlines, paired with M13).



생성한 Footprint의 Name과 Description 기록

IPC® Compliant Footprint Wizard

SOP/TSOP Footprint Description

The footprint values can now be inferred from the package dimensions.
You can review and modify them here.

☒ Use suggested values

Name

SOP65P780X200-28N

Description

SOP, 28-Leads, Body 10.20x5.30mm, Pitch 0.65mm, IPC Medium Density

작업영역 지정하여 저장

IPC® Compliant Footprint Wizard

Footprint Destination

Select where to store the finished footprint.

☐ Existing PcbLib File

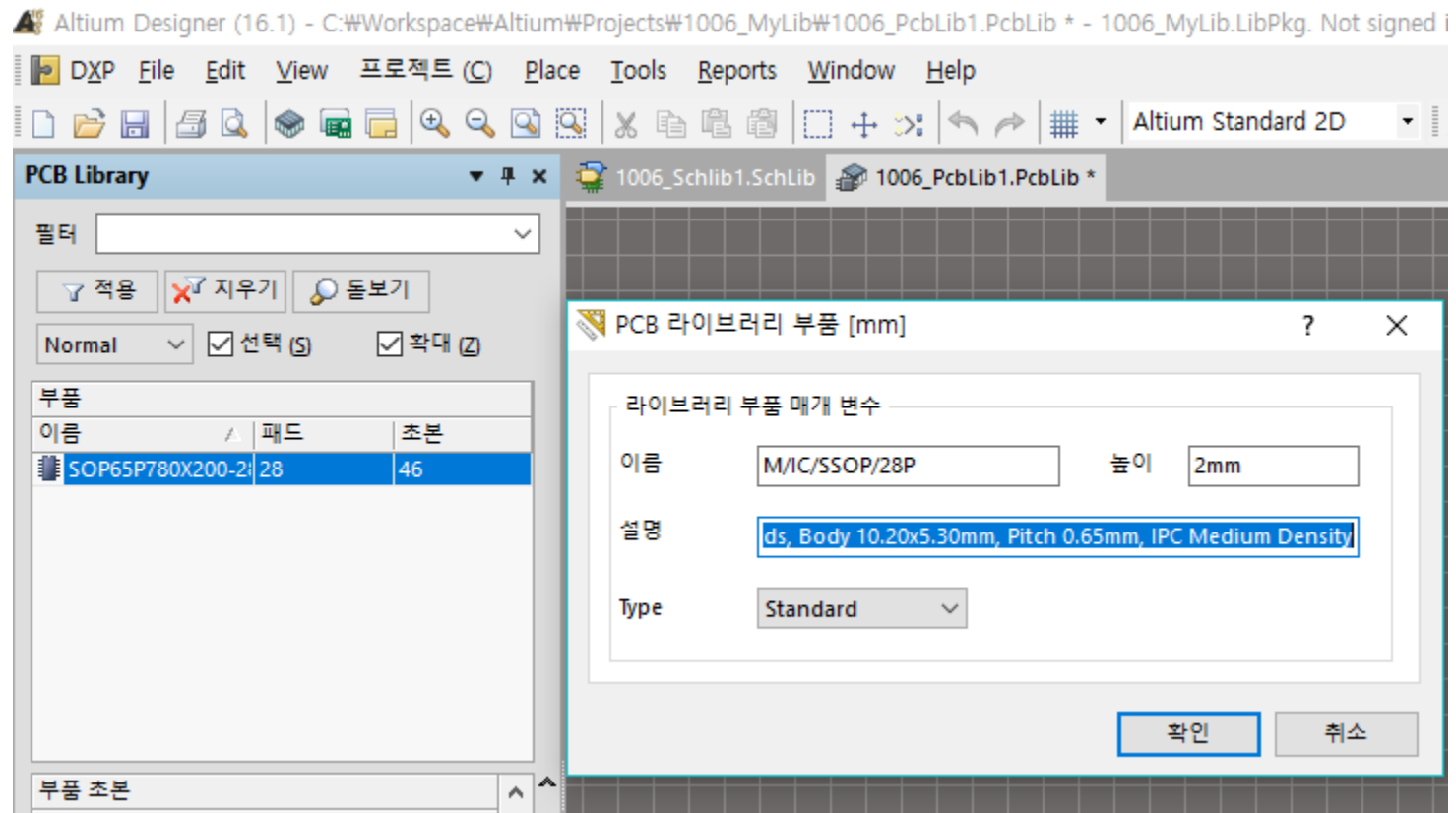
...

☐ New PcbLib File

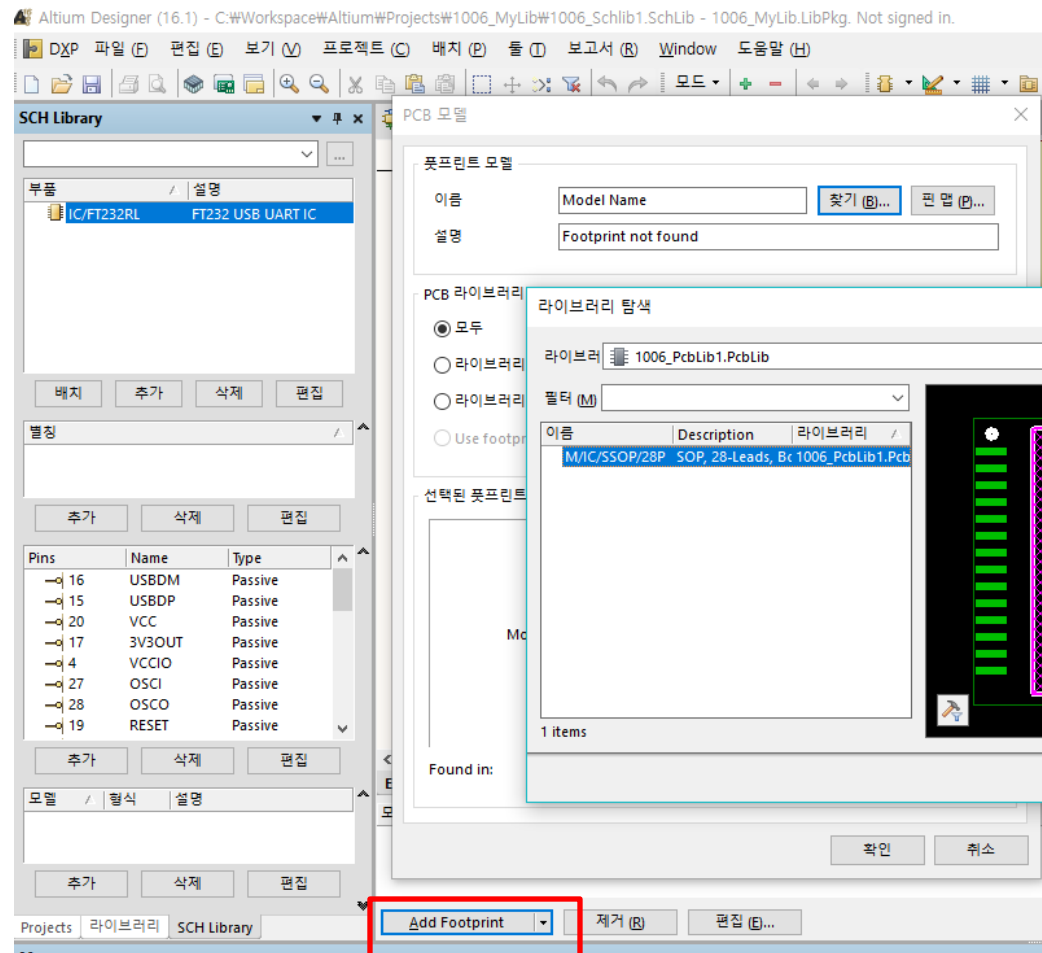
.PcbLib

☒ Current PcbLib File C:\Workspace\Altium\Projects\1006_MyLib\1006_PcbLib1.PcbLib

Suggested value로 생성됐던 부품이름 변경



회로도 라이브러리에 PCB 라이브러리 추가하기



2. ISO7221 라이브러리 만들기

Altium Designer (16.1) - C:\Workspace\Altium\Projects\1006_MyLib\1006_SchLib1.SchLib - 1006_MyLib.LibPkg. Not signed in.

DXP 파일 (F) 편집 (E) 보기 (V) 프로젝트 (C) 배치 (P) 툴 (T) 보고서 (R) Window 도움말 (H)



SCH Library 1006_SchLib1.SchLib 1006_PcbLib1.PcbLib

부품 / 설명

- IC/FT232RL FT232 USB UART IC
- IC/ISO7221**

배치 추가 삭제 편집

별칭

추가 삭제 편집

Pins	Name	Type
1	VCC1	Passive
2	OUTA	Passive

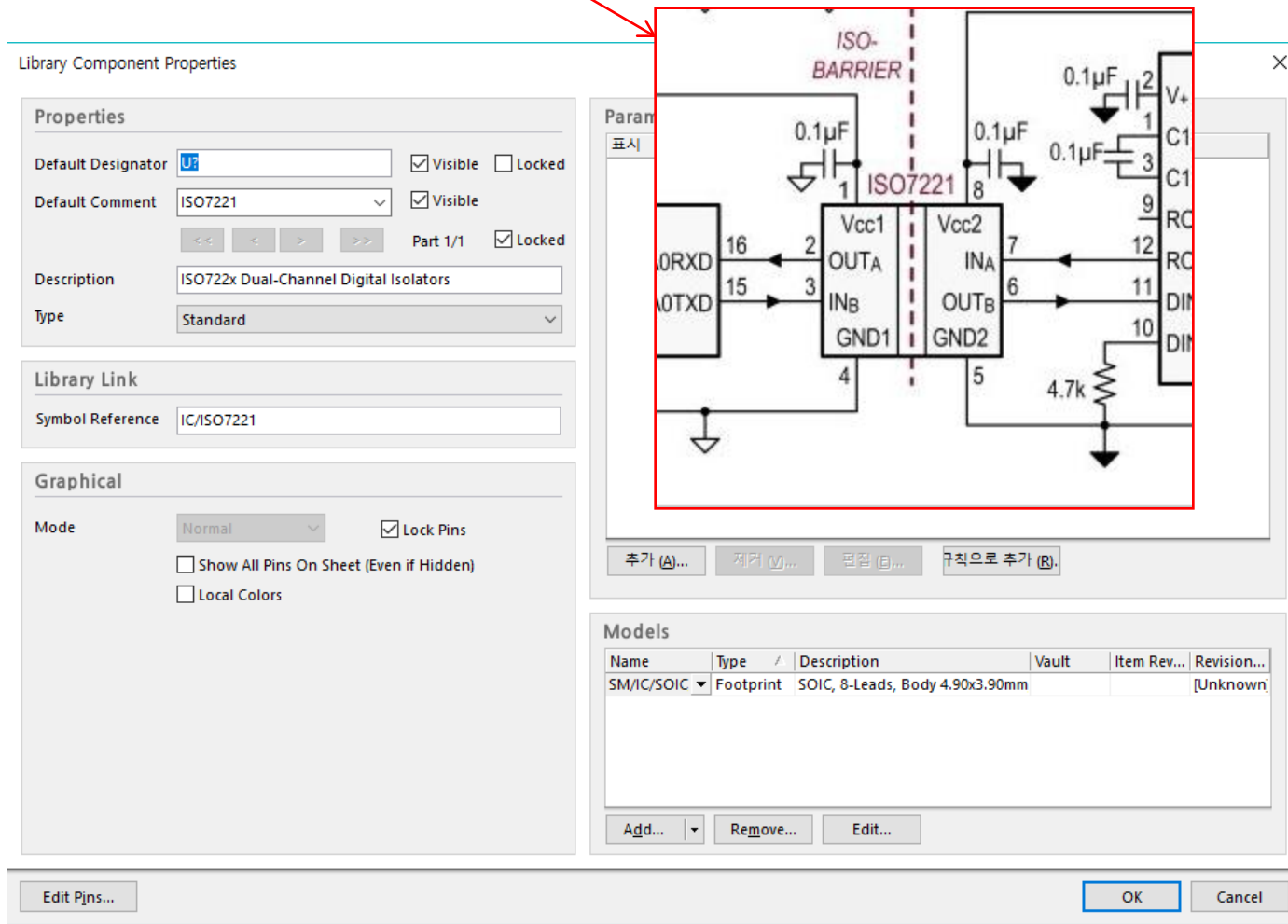
1 VCC1 VCC2 8

2 OUTA ← INA 7

3 INB → OUTB 6

4 GND1 GND2 5

[참고] Isolator : 전력의 흐름을 한 방향으로 고정하는 수동소자
 어떤 신호경로 중간에 isolator가 위치하면 한쪽 방향으로만 전력이 전달되고, 나머지 반대방향으로는
 전력이 전달되지 않음으로써 전력 흐름의 방향을 고정시킴.
 역방향으로 유입되는 신호는 받지 않고 차단



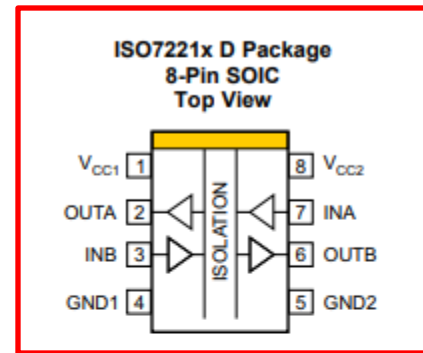
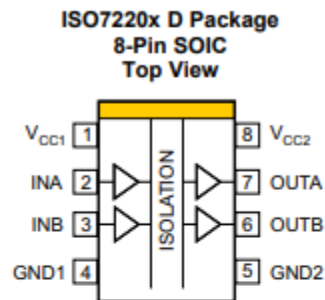
The screenshot displays the 'Library Component Properties' dialog for the ISO7221 component. The 'Properties' section includes fields for 'Default Designator' (U), 'Default Comment' (ISO7221), 'Description' (ISO722x Dual-Channel Digital Isolators), and 'Type' (Standard). The 'Library Link' section shows the 'Symbol Reference' as IC/ISO7221. The 'Graphical' section has a 'Mode' dropdown set to 'Normal' and checkboxes for 'Lock Pins', 'Show All Pins On Sheet (Even if Hidden)', and 'Local Colors'. A red arrow points from the text '역방향으로 유입되는 신호는 받지 않고 차단' to the 'ISO-BARRIER' label in the graphical representation of the component. The graphical representation shows the ISO7221 component with its pins and internal connections, including a dashed line labeled 'ISO-BARRIER' separating the two channels. The 'Models' section at the bottom contains a table with the following data:

Name	Type	Description	Vault	Item Rev...	Revision...
SM/IC/SOIC	Footprint	SOIC, 8-Leads, Body 4.90x3.90mm			[Unknown]

Buttons at the bottom of the dialog include 'Edit Pins...', 'OK', and 'Cancel'.

Datasheet 에서 pin configuration 확인

5 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7220x	ISO7221x		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	—	Ground connection for V _{CC1}
GND2	5	5	—	Ground connection for V _{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V _{CC1}	1	1	—	Power supply, V _{CC1}
V _{CC2}	8	8	—	Power supply, V _{CC2}

IPC Footprint Wizard 사용

IPC® Compliant Footprint Wizard

Select Component Type

Select the family of components you wish to create.

Component Types

Name	Description	Included Packages
LGA	Land Grid Array	LGA
MELF	MELF Components, 2-Pins	Diode, Resistor
MOLDED	Molded Components, 2-Pins	Capacitor, Inductor, Diode
PLCC	Plastic Leaded Chip Carrier, Square - J Leads	PLCC
PQFN	Pullback Quad Flat No-Lead	PQFN
PQFP	Plastic Quad Flat Pack	PQFP, PQFP Exposed Pad
PSON	Pullback Small Outline No-Lead	PSON
QFN	Quad Flat No-Lead	QFN, LLP
QFN-2ROW	Quad Flat No-Lead, 2 Rows, Square	Double Row QFN
SODFL	Small Outline Diode, Flat Lead	SODFL
SOIC	Small Outline Integrated Package, 1.27mm Pitch - Gullwing Leads	SOIC, SOIC Exposed Pad
SOJ	Small Outline Package - J Leads	SOJ
SON	Small Outline Non-lead	SON, SON Exposed Pad
SOP/TSOP	Small Outline Package - Gullwing Leads	SOP, TSOP, TSSOP
SOT143/343	Small Outline Transistor	SOT143, SOT343
SOT223	Small Outline Transistor	SOT223
SOT23	Small Outline Transistor	3-Leads, 5-Leads, 6-Leads
SOT89	Small Outline Transistor	SOT89
SOTFL	Small Outline Transistor, Flat Lead	3-Leads, 5-Leads, 6-Leads
WIRE WOUND	Precision Wire Wound Inductor, 2-Pins	Inductor

The selected component is SOIC.
This will allow you to generate SOIC, SOIC Exposed Pad packages.



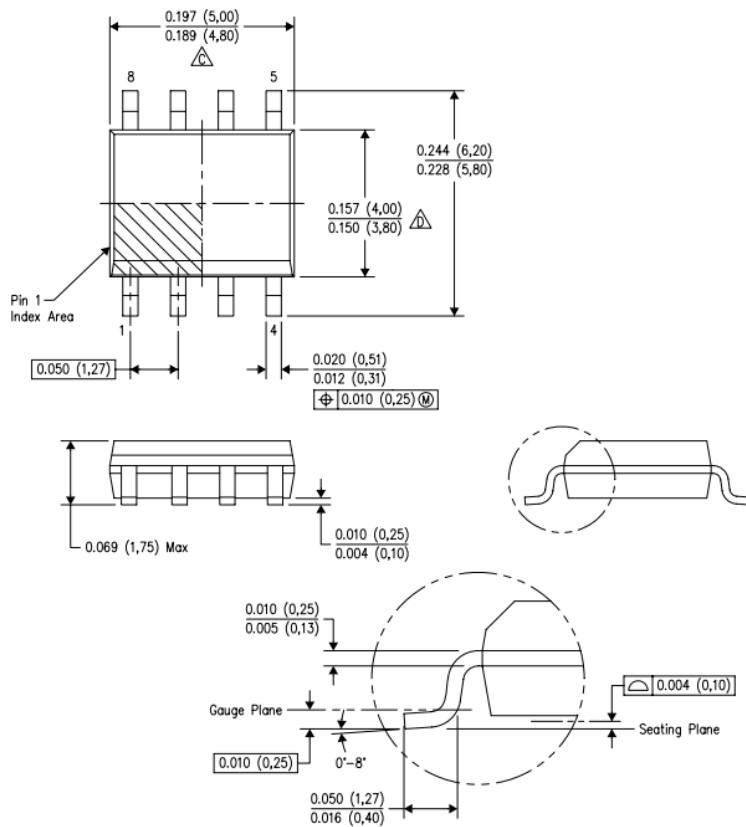
NOTE: All wizard measurement dimensions are required to be entered as metric (mm) units.

Cancel

< Back

Next >

datasheet상의 수치를 확인하고, SOIC Package Dimensions 기록



IPC® Compliant Footprint Wizard

SOIC Package Dimensions

Enter the required package values.

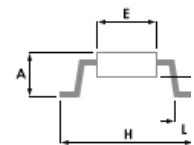
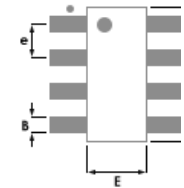
Overall Dimensions

Width Range (H)	Minimum	5.8mm
	Maximum	6.2mm
Maximum Height (A)		1.75mm
Minimum Standoff Height (A1)		0.18mm
Body Width Range (E)	Minimum	3.8mm
	Maximum	4mm
Body Length Range (D)	Minimum	4.8mm
	Maximum	5mm

Pin Information

Number of pins		8
Lead Width Range (B)	Minimum	0.31mm
	Maximum	0.51mm
Lead Length Range (L)	Minimum	0.4mm
	Maximum	1.27mm

All SOIC packages have a pitch (e) of 1.27mm



Pad 모양을 Rectangular로 변경

IPC® Compliant Footprint Wizard

SOIC Footprint Dimensions

The footprint dimensions can now be inferred from the package dimensions.
You can review and modify them here.

The footprint has 8 pads and a pitch (P) of 1.27mm. You can modify here the calculated dimensions of the foot

☒ Use calculated footprint values

Pad Dimensions

X

Y

Pads are trimmed to prevent from extending under body

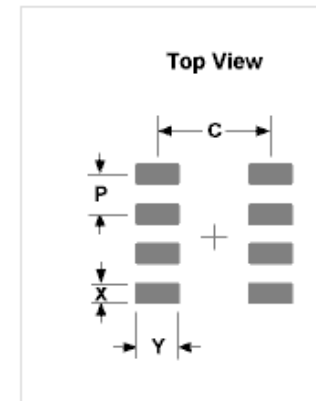
Pad Spacing

C

Pad Shape

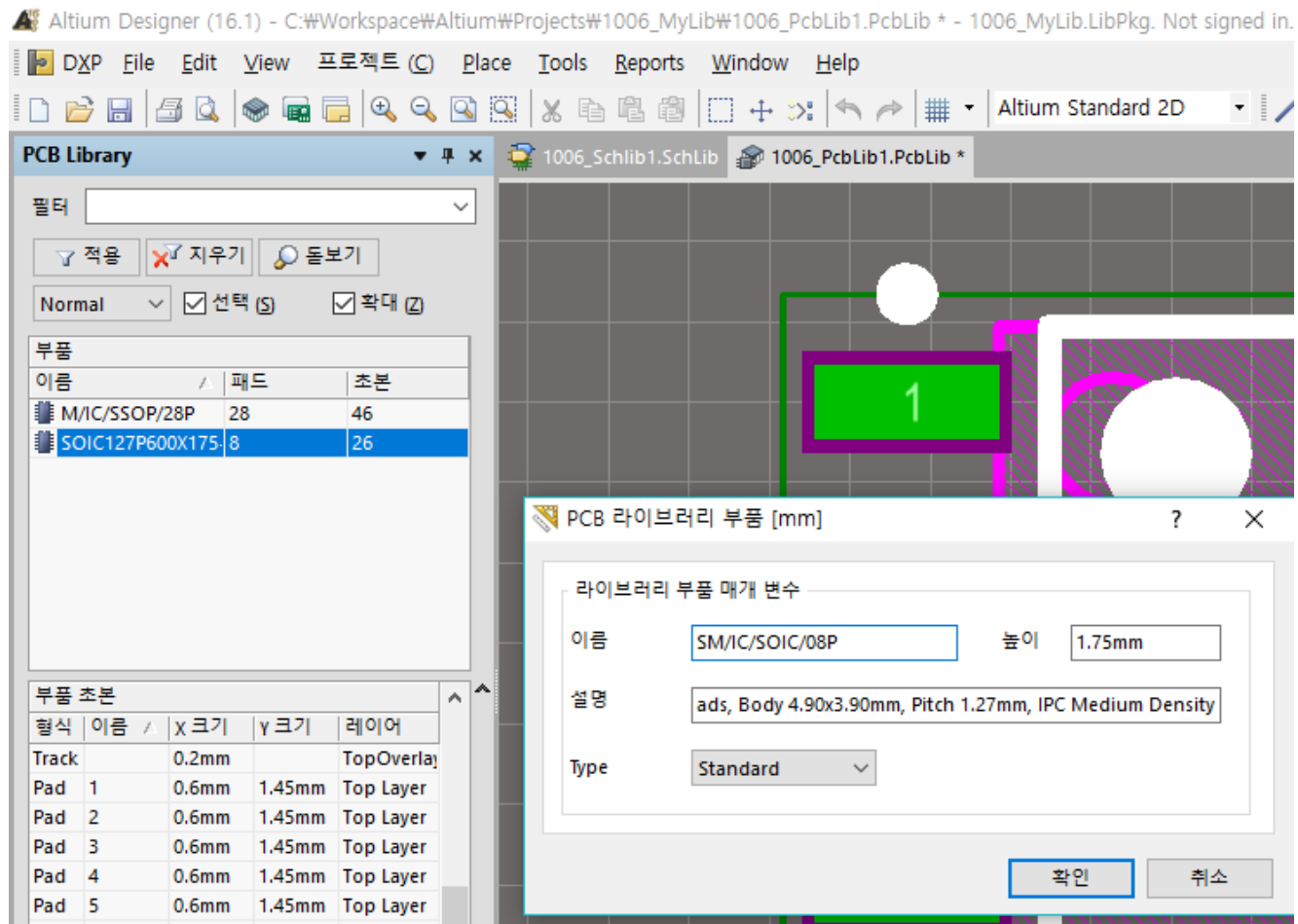
☐ Rounded

☒ Rectangular

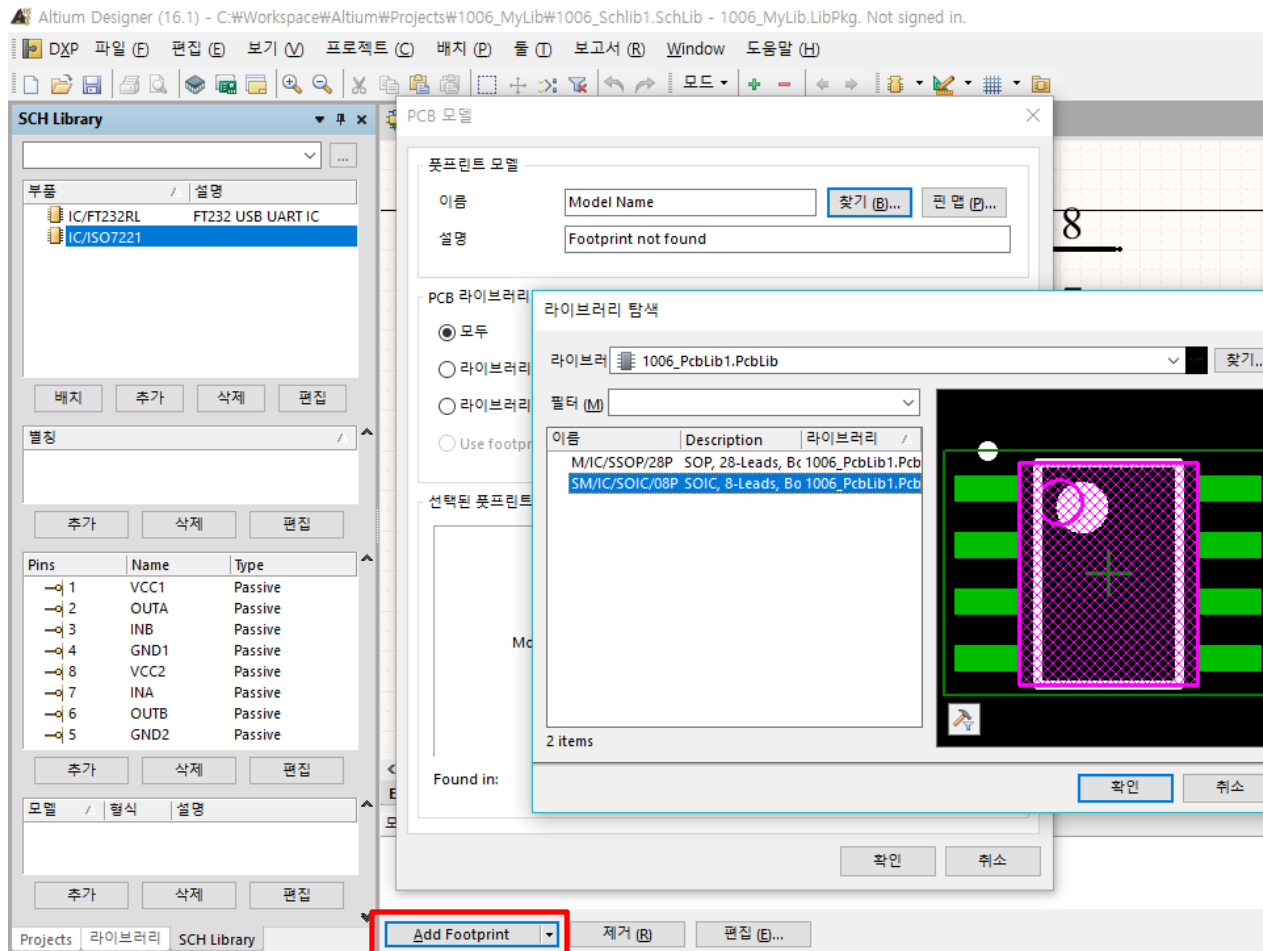


이후 모두 default 설정으로 진행함

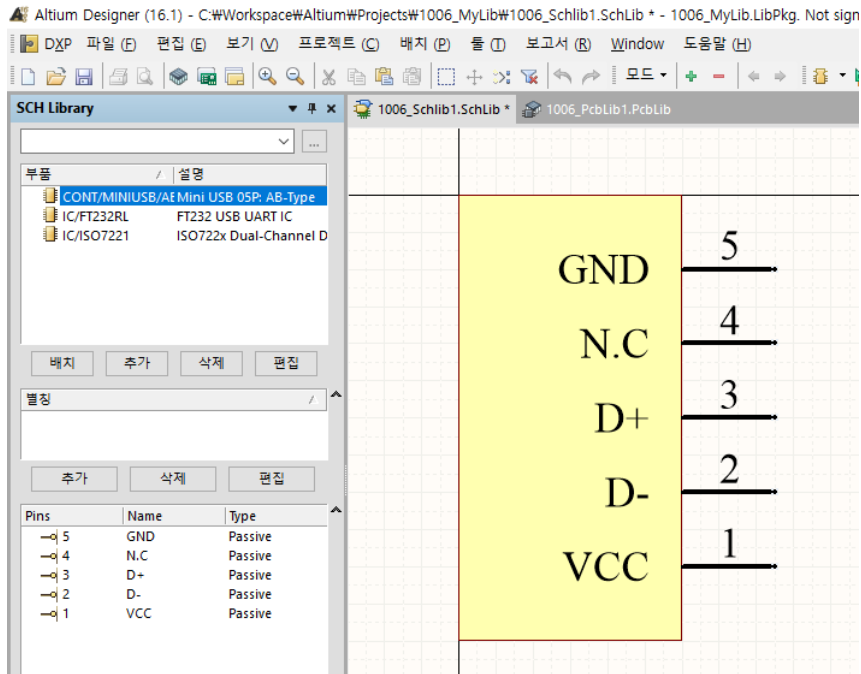
생성한 Footprint 이름변경



회로도 라이브러리에 PCB라이브러리 추가



3. USB 라이브러리 만들기



Library Component Properties

Properties

Default Designator: U? ☐ Visible ☐ Locked

Default Comment: Mini USB ☐ Visible

Part 1/1 ☒ Locked

Description: Mini USB 05P: AB-Type

Type: Standard

Library Link

Symbol Reference: CONT/MINIUSB/AB

Graphical

Mode: Normal ☒ Lock Pins

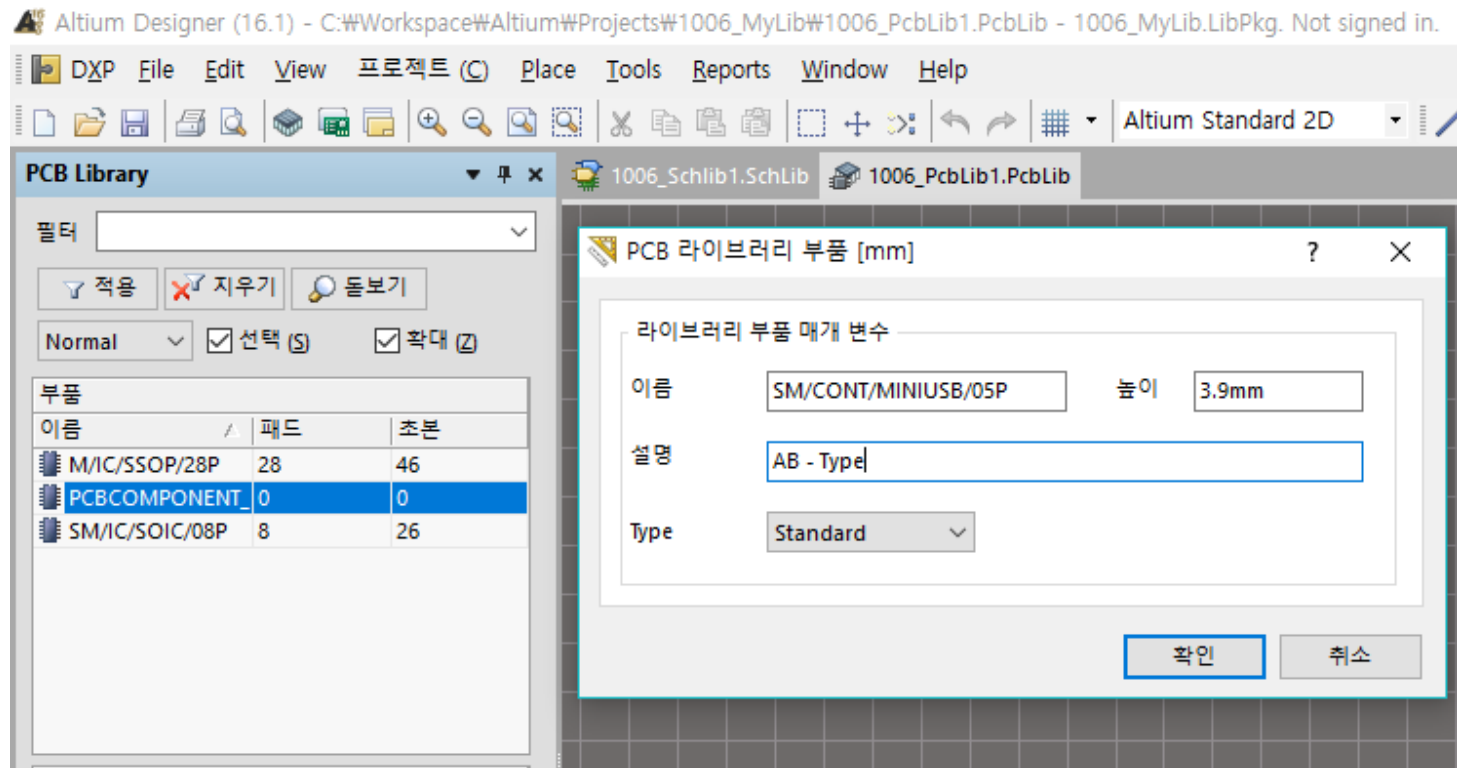
☐ Show All Pins On Sheet (Even if Hidden)

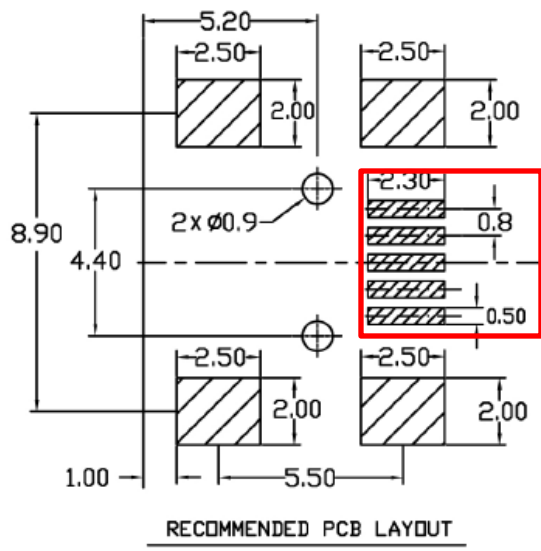
☐ Local Colors

Parameters

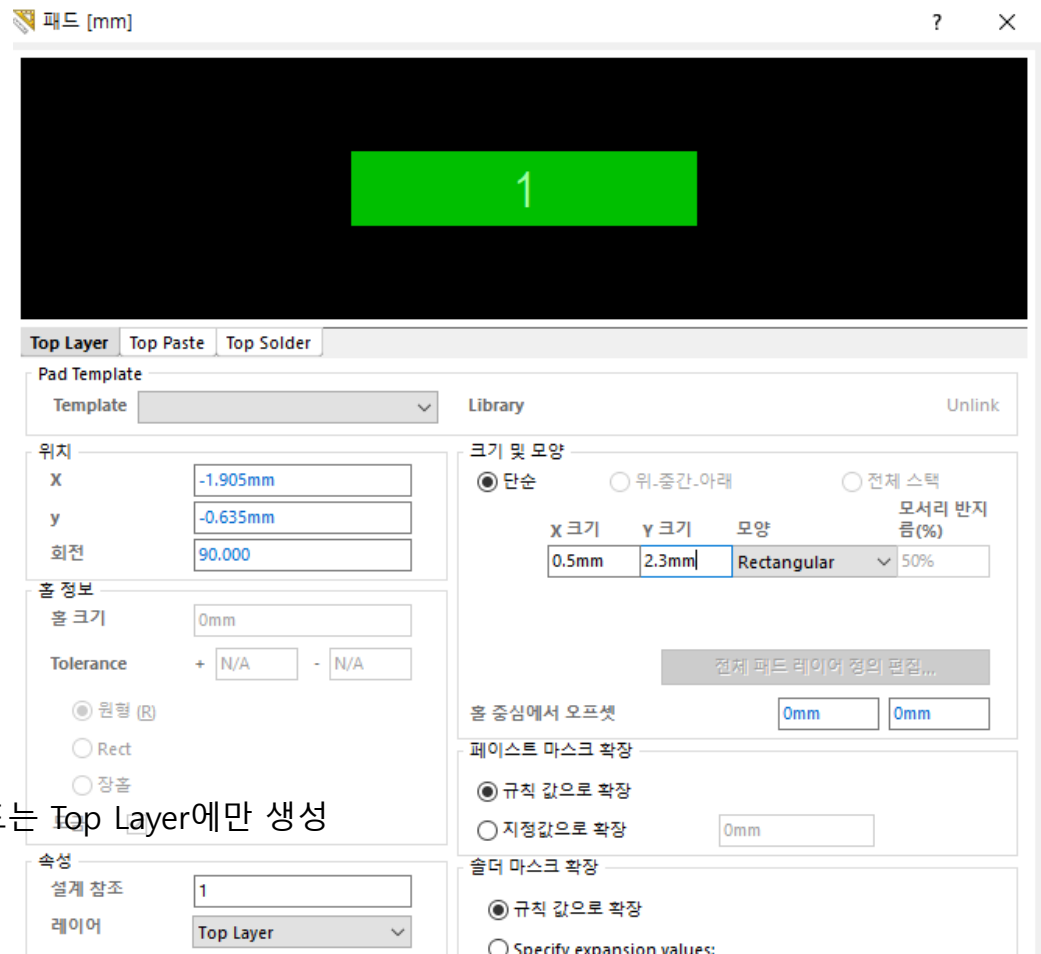
표시 이름

이번엔, Wizard 사용하지 않고 Datasheet만 참고하여 Footprint 제작

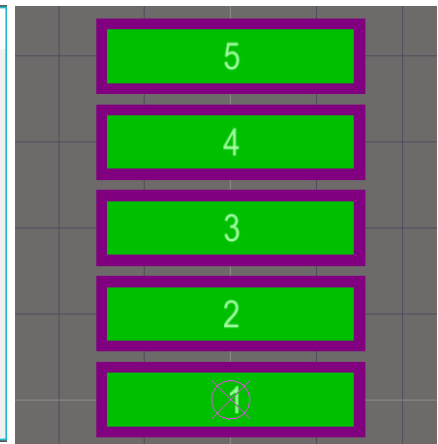
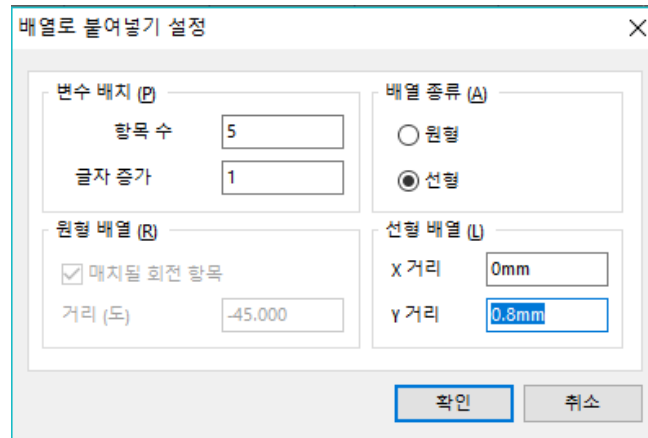
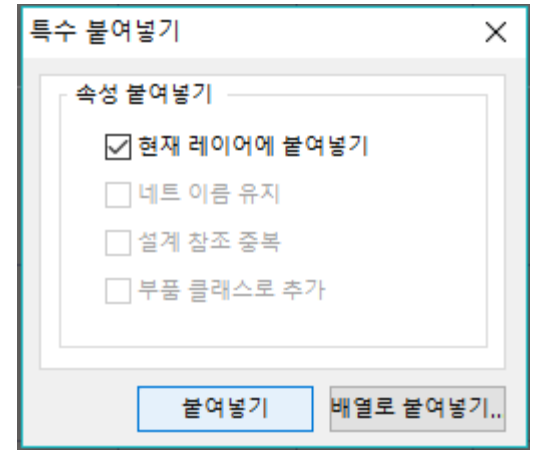
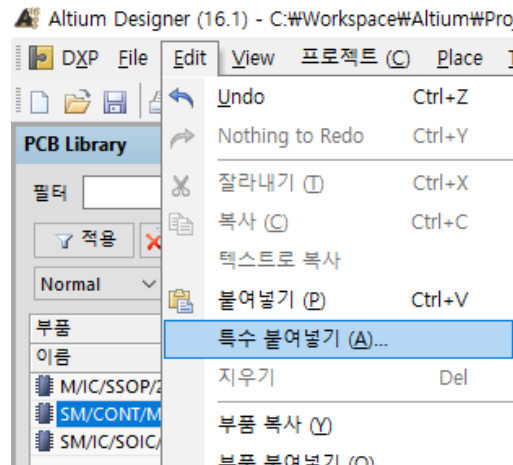
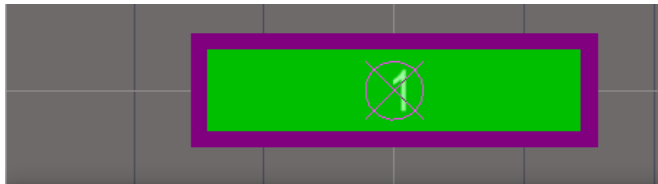




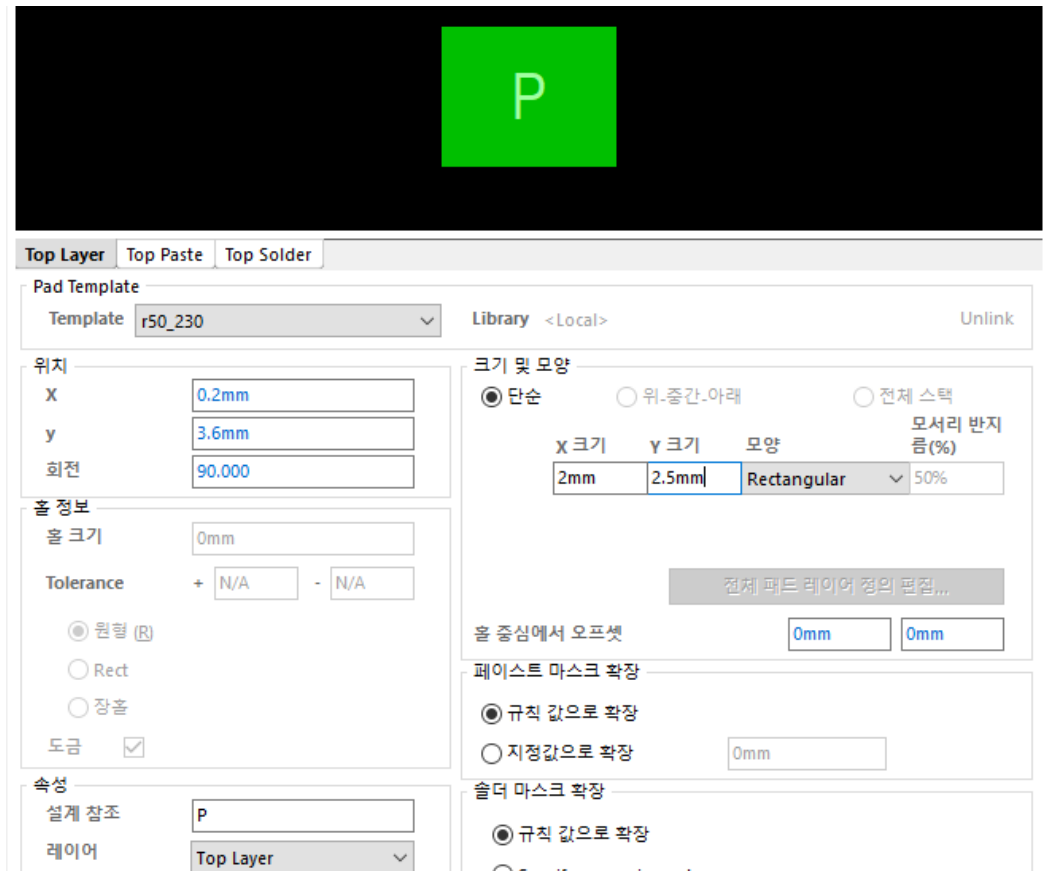
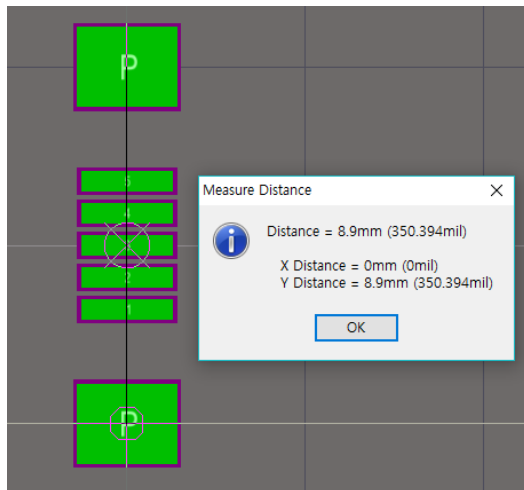
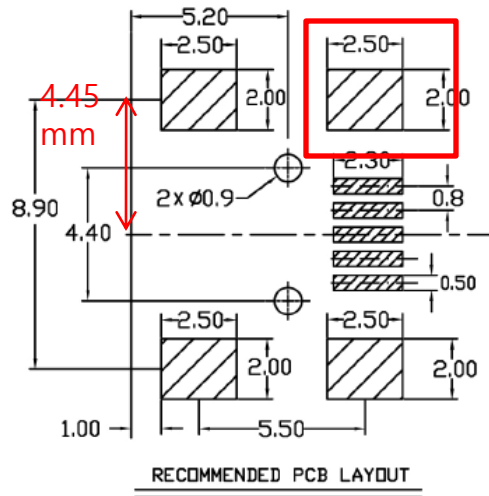
패드는 Top Layer에만 생성



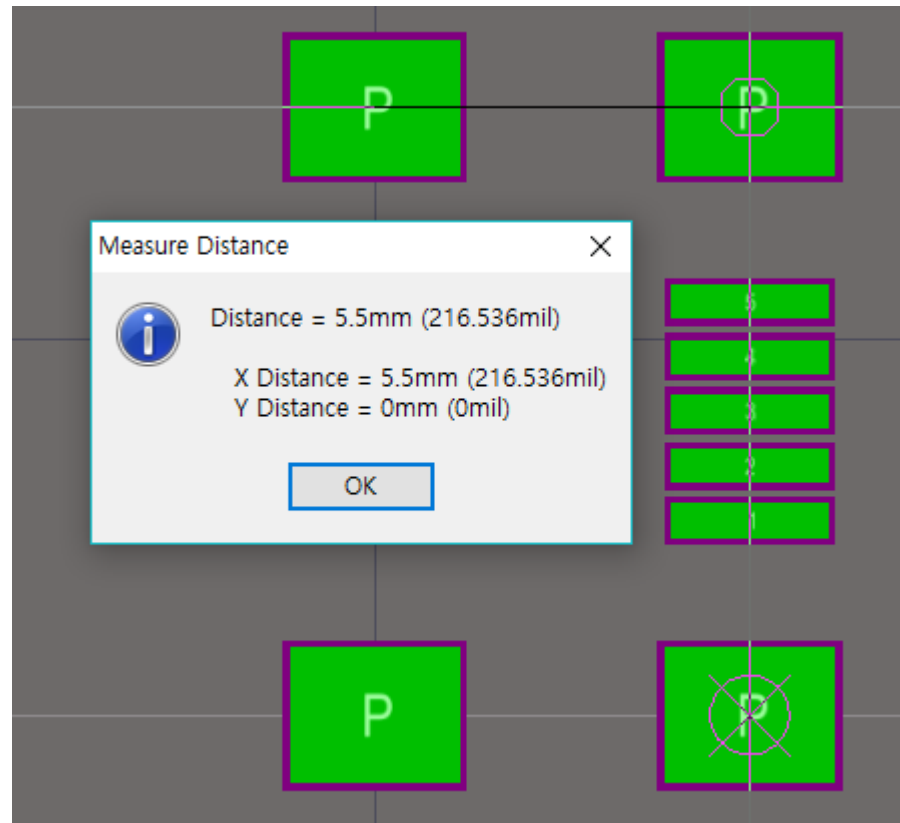
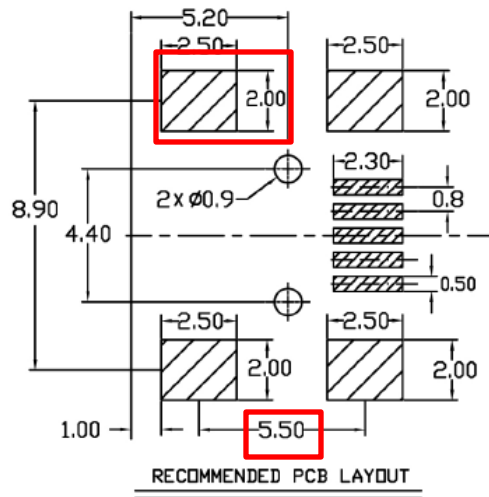
0.8mm pitch를 고려하여 Ctrl+G 그리드 변경하고,
잘라내기→ 원점클릭 → 특수붙여넣기 → 현재레이어에 배열로 붙여넣기



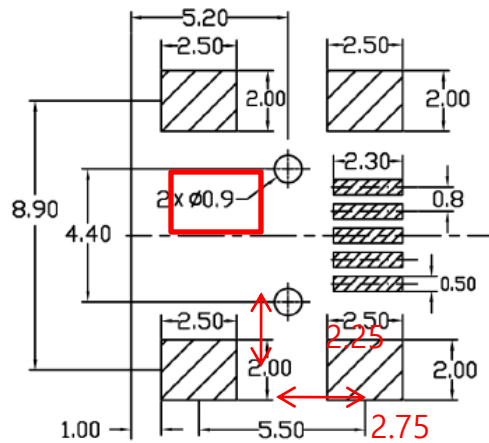
Set Reference를 가운데로 위치
그리드 간격 4.45mm로 변경 → ctrl+M으로 확인



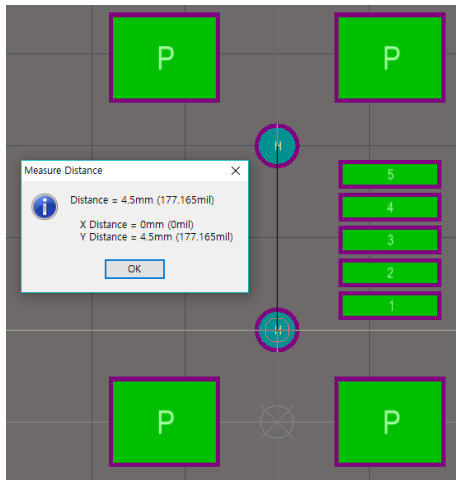
기준점을 패드에 두고 그리드 변경(5.5mm)
나머지 패드 2개도 그려준다.



고정용으로 쓰일 Hole

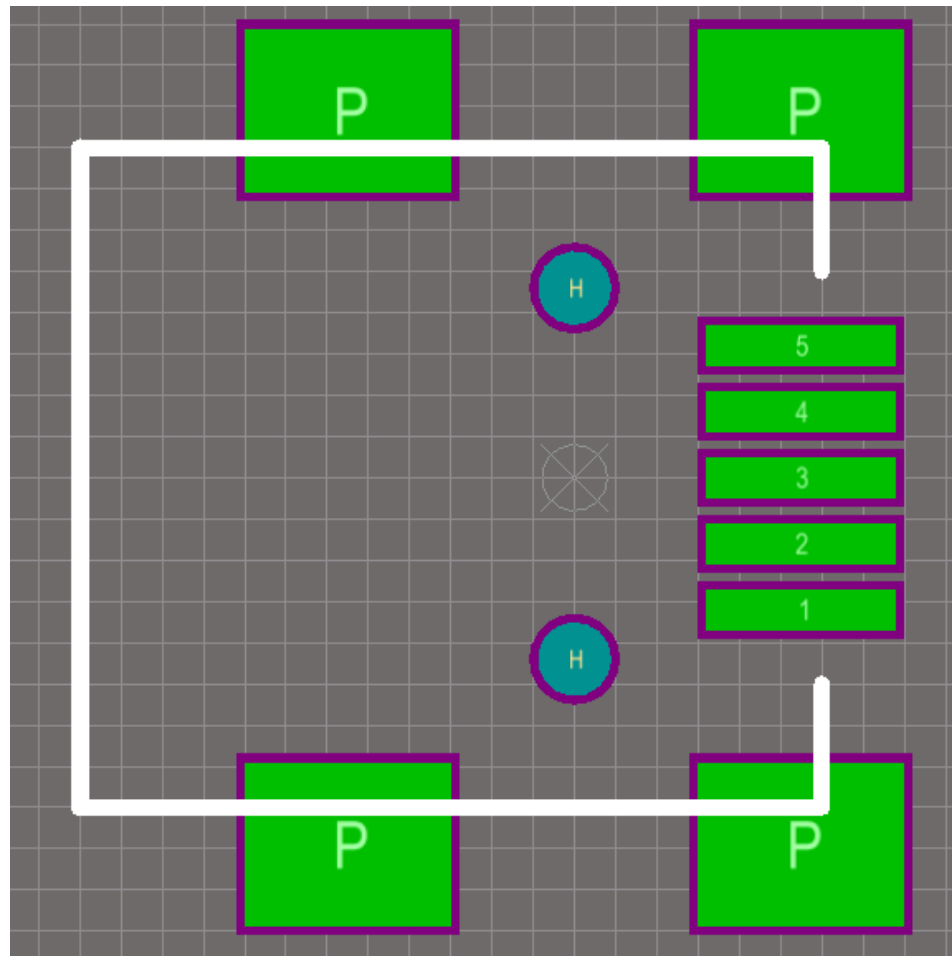


RECOMMENDED PCB LAYOUT

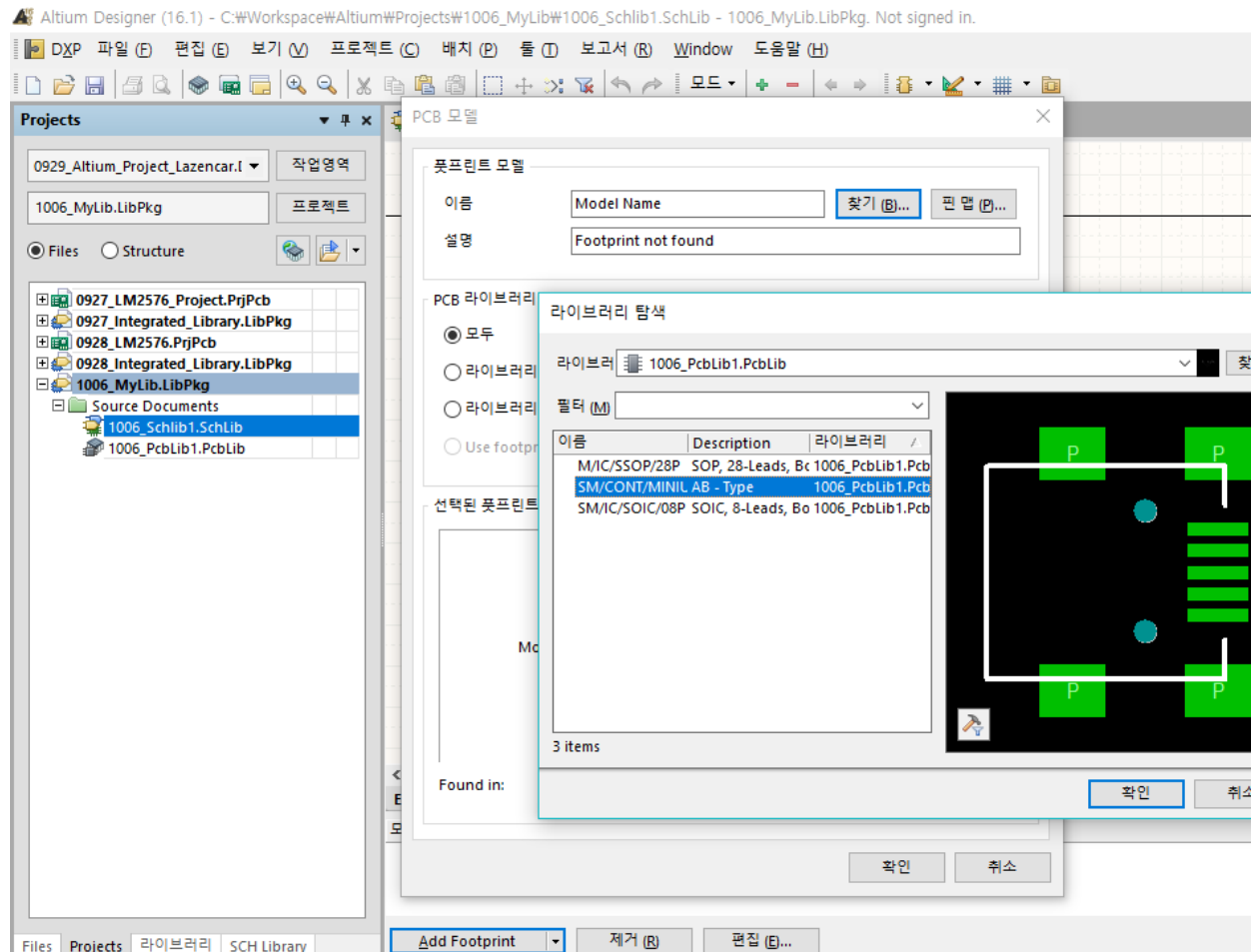


Screenshot of the 'Top Paste' tab in a PCB layout software interface. The 'Pad Template' section shows 'Template' set to 'r50_230'. The '위치' (Location) section shows X: -5.5mm, Y: 5.5mm, and Rotation: 90.000. The '홀 정보' (Hole Info) section shows '홀 크기' (Hole Size) set to '0.9mm'. The '속성' (Properties) section shows '설계 참조' (Design Reference) set to 'H' and '레이어' (Layer) set to 'Multi-Layer'. The '크기 및 모양' (Size and Shape) section shows '단순' (Simple) selected, with '크기' (Size) set to '0.9mm' and '모양' (Shape) set to 'Round'.

Top Overlay에서 Silk Screen 작업 수행 (tap: 폭 0.2mm)



Schematic 라이브러리에 PCB 라이브러리 추가



4. Pin Header 라이브러리 생성

핀헤더 **Single 1x4Pin Straight(2.54mm)**

Features

- 핀헤더 single 1x4Pin
- Straight=직선타입
- 핀간격: 2.54mm



Pin Header 라이브러리 생성

Library Component Properties

Properties

Default Designator: J? ☒ Visible ☐ Locked

Default Comment: 04P ☒ Visible

Description: Pin Header, Pitch 2.54mm

Type: Standard

Library Link

Symbol Reference: HAD/P2.54/04P

Graphical

Mode: Normal ☒ Lock Pins

☐ Show All Pins On Sheet (Even if Hidden)

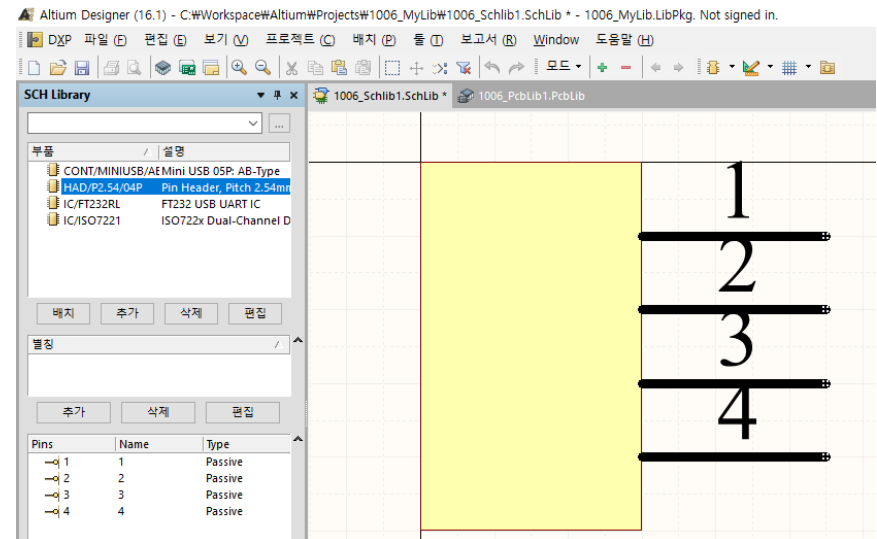
☐ Local Colors

Parameters

표시

추가 (A)...

Models



PCB document 작성

Altium Designer (16.1) - C:\Workspace\Altium\Projects\1006_MyLib\1006_PcbLib1.PcbLib - 1006_MyLib.LibPkg. Not signed in.

DXP File Edit View 프로젝트(C) Place Tools Reports Window Help

PCB Library

필터

적용 지우기 돌보기

Normal 선택(S) 확대(Z)

부품	이름	패드	초본
M/IC/SSOP/28P	28	46	
PCBCOMPONENT	0		
SM/CONT/MINIUSI	11	16	
SM/IC/SOIC/08P	8	26	

부품 초본

형식	이름	X 크기	Y 크기	레이어
----	----	------	------	-----

PCB 라이브러리 부품 [mm]

라이브러리 부품 매개 변수

이름 HL/HAD/P2.54/04H

설명

Type Standard

위치

X 0mm

Y 0mm

회전 90.000

홀 정보

홀 크기 1.02mm

Tolerance + N/A - N/A

원형(R) ☒

Rect ☐

속성

설계 참조 1

레이어 Multi-Layer

Top Layer Bottom Layer Top Paste Top Solder Bottom Solder Bottom Paste Multi-Layer

Pad Template

Template Library Unlink

크기 및 모양

단순 ☒ 위-중간-아래 ☐ 전체 스택 ☐

X 크기 1.6mm Y 크기 1.6mm 모양 Rounded Rectar 모서리 반지름(%) 50%

전체 패드 레이어 정의 편집...

홀 중심에서 오프셋 0mm 0mm

페이스트 마스크 확장

외곽으로 확장

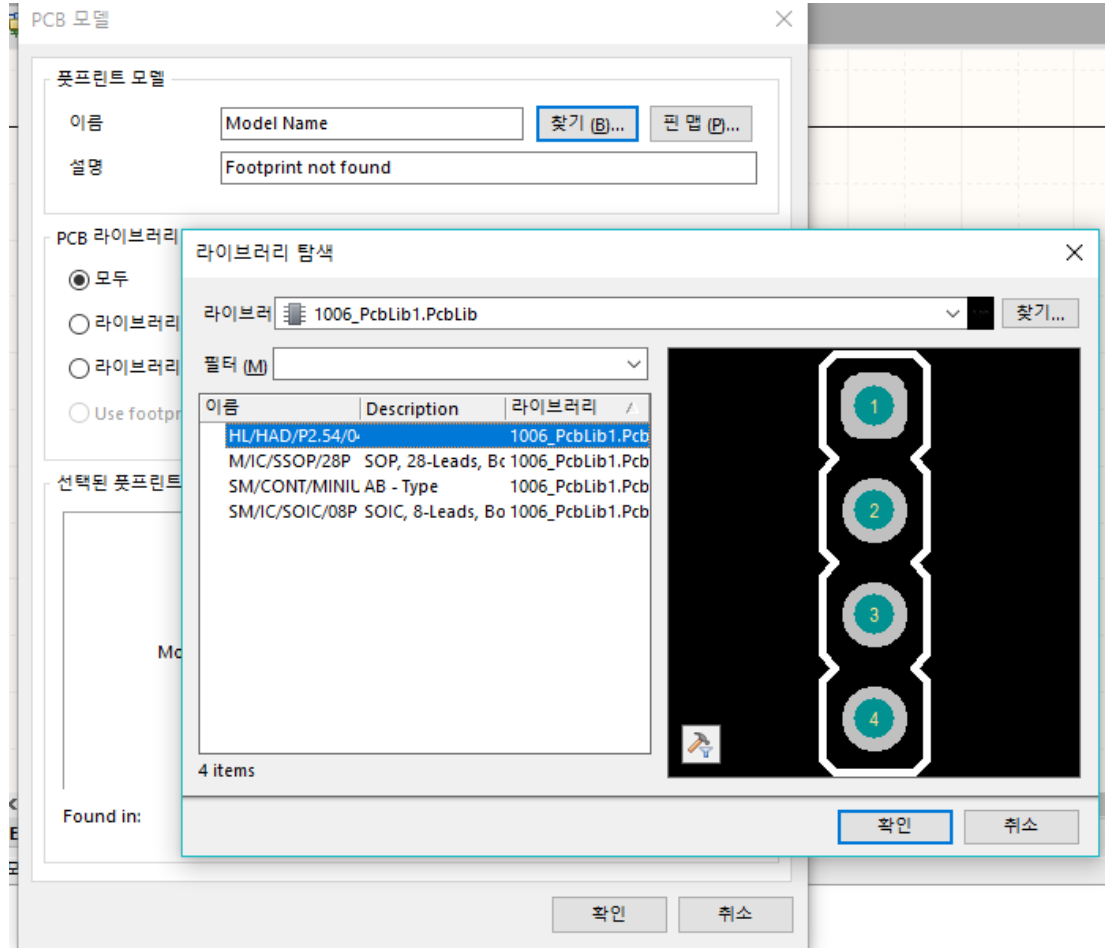
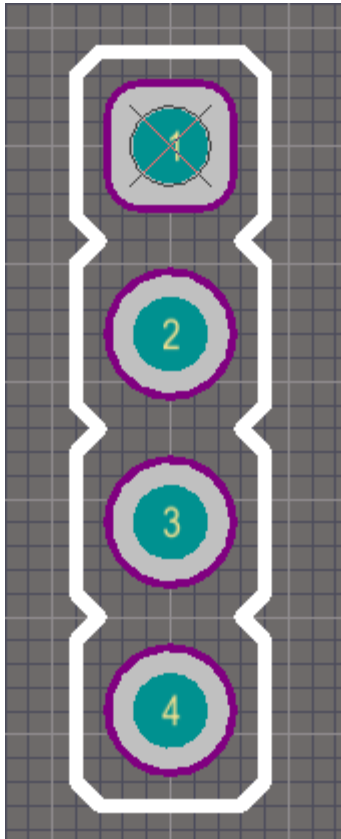
내곽으로 확장 0mm

슬더 마스크 확장

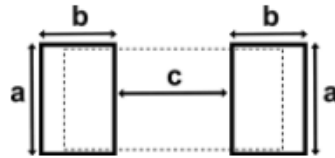
규칙 값으로 확장 ☒

PAD 1번을 구분하기 위해서 Rounded Rectangular 설정
*. 1번이 VCC인 경우가 많지만 꼭 VCC는 아니다. 주의할 것

Top Overlay에서 Silk Screen 작업(Grid: 0.318mm)하고, Add Footprint



(*) 칩저항, 칩 capacitor Artwork 시 참고



Code		Pad length (a)		Pad width (b)		Gap (c)	
Imperial	Metric	inch	mm	inch	mm	inch	mm
0201	0603	0.012	0.3	0.012	0.3	0.012	0.3
0402	1005	0.024	0.6	0.020	0.5	0.020	0.5
0603	1608	0.035	0.9	0.024	0.6	0.035	0.9
0805	2012	0.051	1.3	0.028	0.7	0.047	1.2
1206	3216	0.063	1.6	0.035	0.9	0.079	2.0
1218	3246	0.19	4.8	0.035	0.9	0.079	2.0
2010	5025	0.11	2.8	0.059	0.9	0.15	3.8
2512	6332	0.14	3.5	0.063	1.6	0.15	3.8

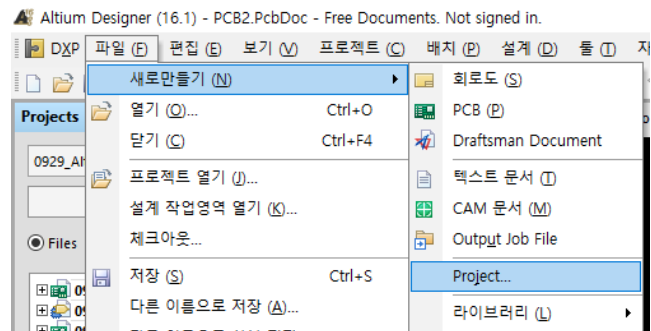
mil	mm
0402	1005
0603	1608
0805	2012
1206	3216

(*) 칩저항 읽는 법



- 3자리 marking : $10\text{3} = 10 \times 10^3 = 10000 = 10\text{k}\Omega$
R22 = 0.22
- 4자리 marking : $5621 = 562 \times 10^1 = 5620 = 5.62\text{k}\Omega$
3R48 = 3.48
('R' 은 'Round' 를 의미 → 소수점)

[3] 새로운 PCB 프로젝트 생성



New Project

Project Types:

PCB Project
FPGA Project
Core Project
Embedded Project
Integrated Library
Script Project

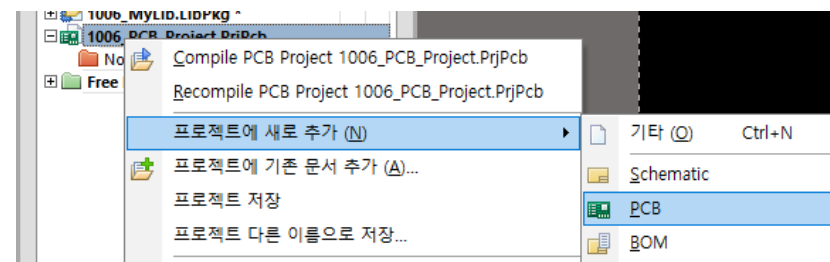
Project Templates:

< Default >
AT long bus (13.3 x 4.2 inches)
AT long bus (13.3 x 4.5 inches)
AT long bus (13.3 x 4.8 inches)
AT long bus with break-away tab (13.3 x 4.2 inches)
AT long bus with break-away tab (13.3 x 4.5 inches)
AT long bus with break-away tab (13.3 x 4.8 inches)
AT short bus (7 x 4.2 inches)
AT short bus (7 x 4.5 inches)
AT short bus (7 x 4.8 inches)
AT short bus with break-away tab (7 x 4.2 inches)
AT short bus with break-away tab (7 x 4.5 inches)
AT short bus with break-away tab (7 x 4.8 inches)
Eurocard VME 3U (3.937 x 6.299 inches)
Eurocard VME 3U (3.937 x 8.660 inches)
Eurocard VME 3U with break-away tab (3.937 x 6.299 ...

Manage Templates...

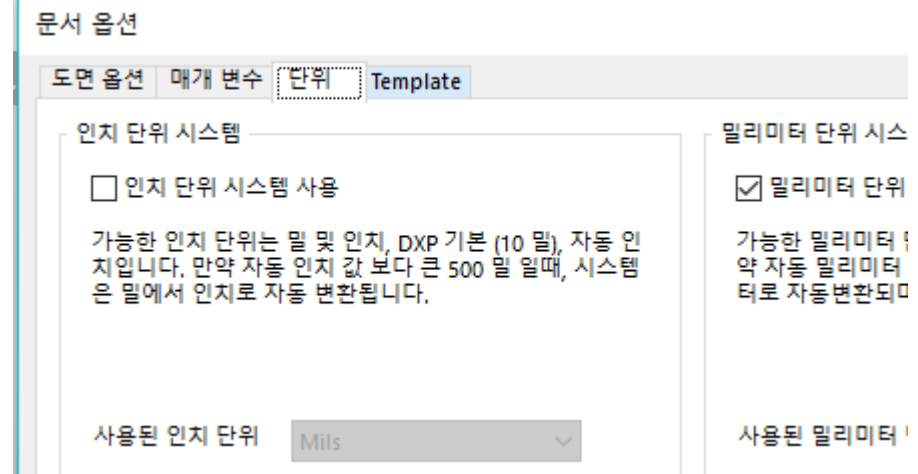
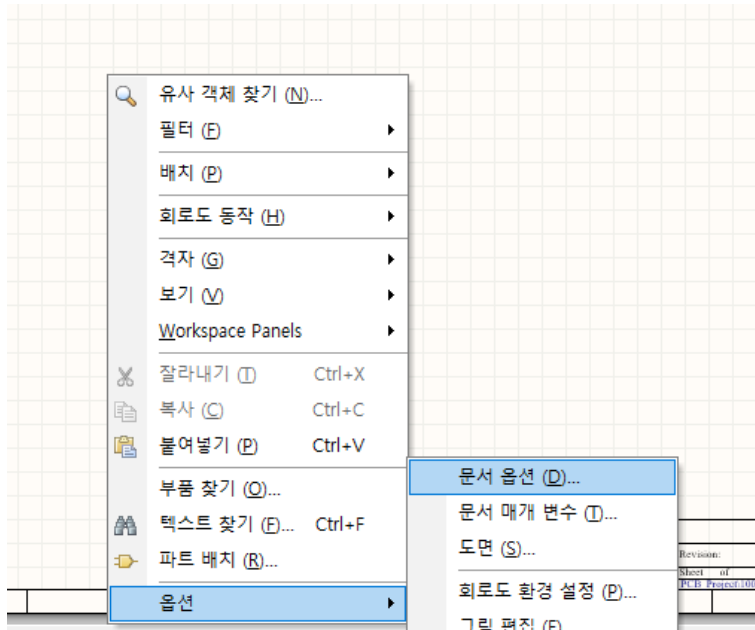
Name

1006_PCB_Project

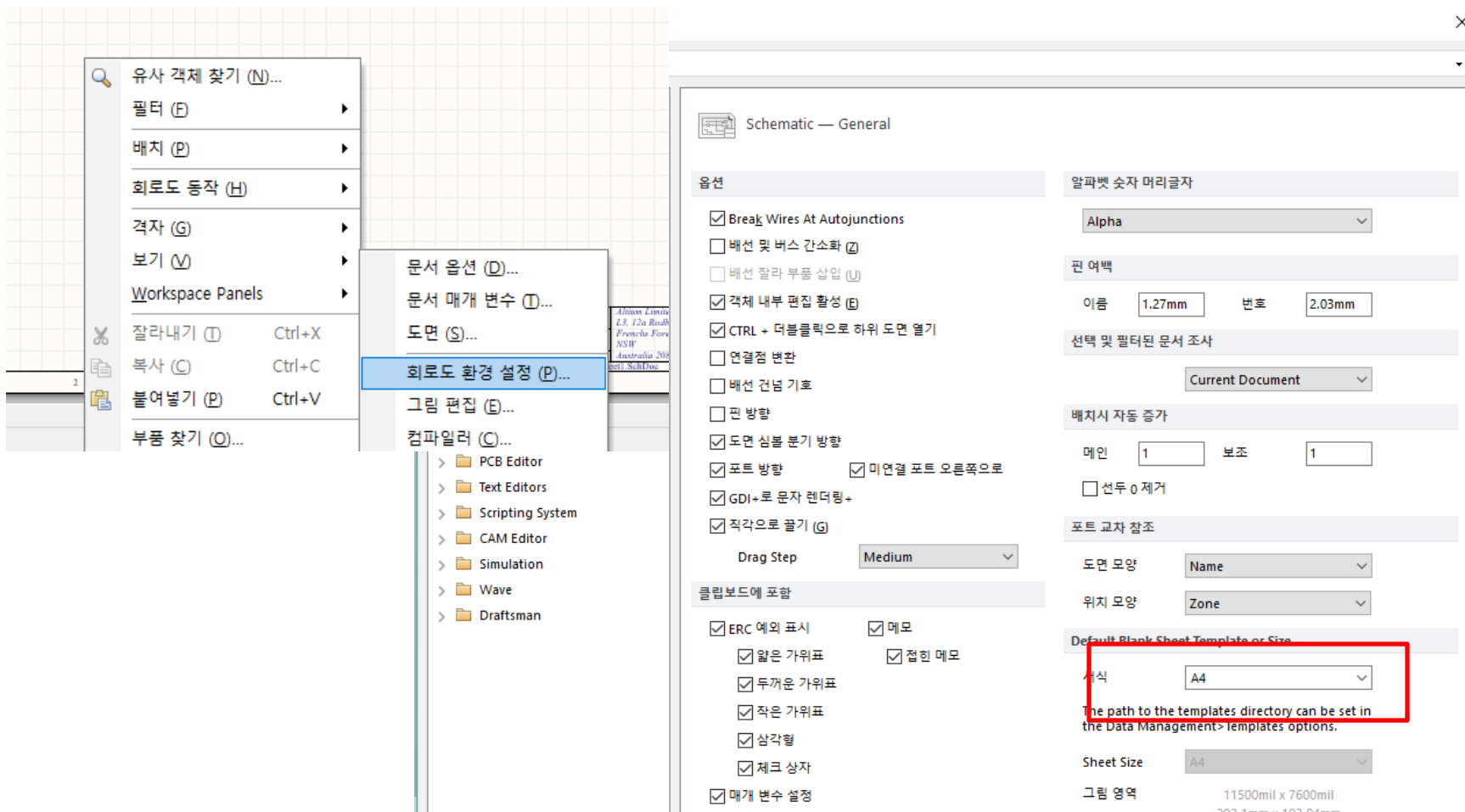


현재 Project에 적용되는 문서 옵션

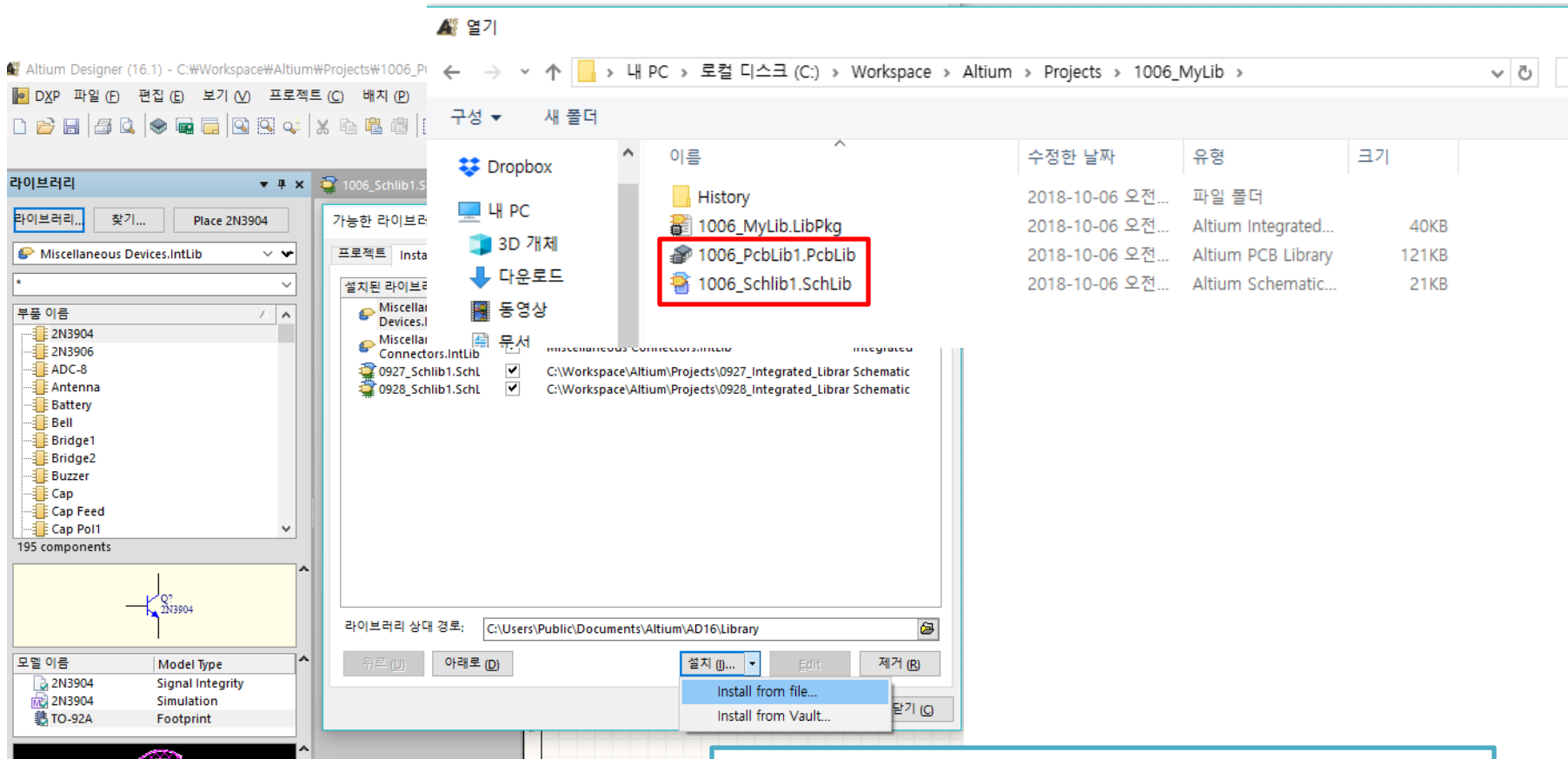
(기본적인 사항들 - 작성자, 날짜, 소속, 문서 Template, 크기 등 - 을 변경)



(*) 문서 옵션의 Default 설정 변경

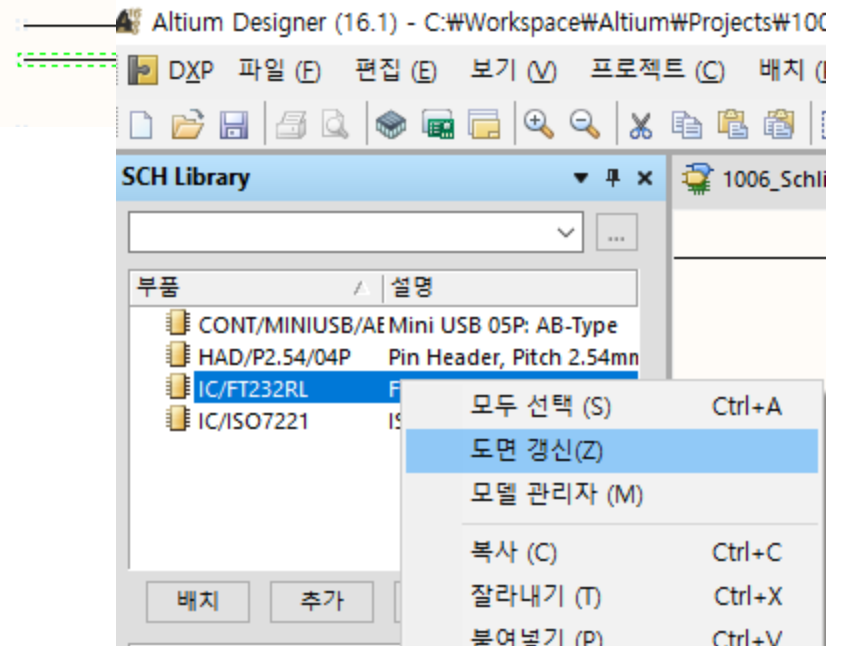
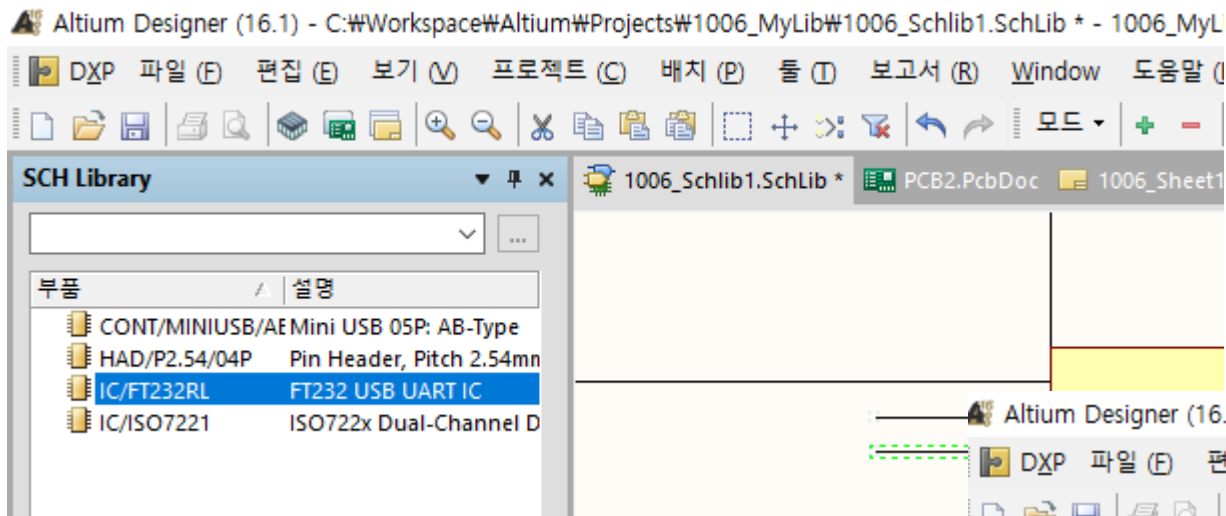


프로젝트에서 사용할 외부 라이브러리 설치



- (*) 라이브러리를 공유하는 다음의 사이트를 적절히 활용한다.
1. 전자카드 라이브러리(symbol, footprint) 공유
<https://www.snapeda.com/home/>
(Import 방법 : <https://www.youtube.com/watch?v=jM6L8SiklaQ>)
 2. 기구설계 라이브러리 공유
<https://www.3dcontentcentral.com/>

Schematic 라이브러리 갱신



설계참조 넣기

주석 넣기

회로도 주석 설정

처리 순서
Across Then Down

경신 진행 방향
Designator

회로도 도면 설계 참조 넣기

회로도 도면
1006_Sheet1.SchDoc

기술 변경 명령

변경	활성	행동	영향 대상	영향 문서	상태	검사	마침	메시지
Annotate Component(11)								
Modify	<input checked="" type="checkbox"/>	C? -> C1	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	C? -> C2	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	C? -> C3	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	J? -> J1	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	LED? -> LED1	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	LED? -> LED2	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	R? -> R1	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	R? -> R2	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	U? -> U1	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	U? -> U2	In	1006_Sheet1.SchDoc	✓	✓		
Modify	<input checked="" type="checkbox"/>	U? -> U3	In	1006_Sheet1.SchDoc	✓	✓		

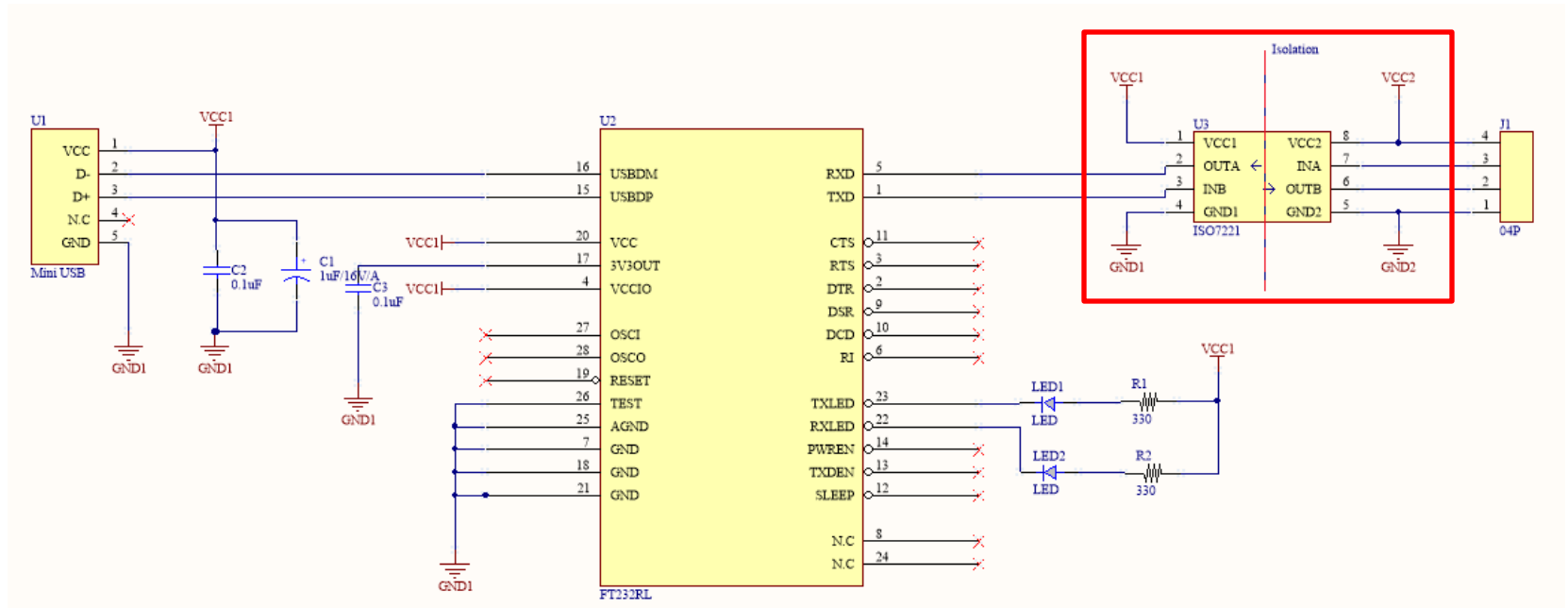
변경 검증 변경 실행 변경 보고서 (R)... ☐ 오류만 표시 닫기

be put into new packages.

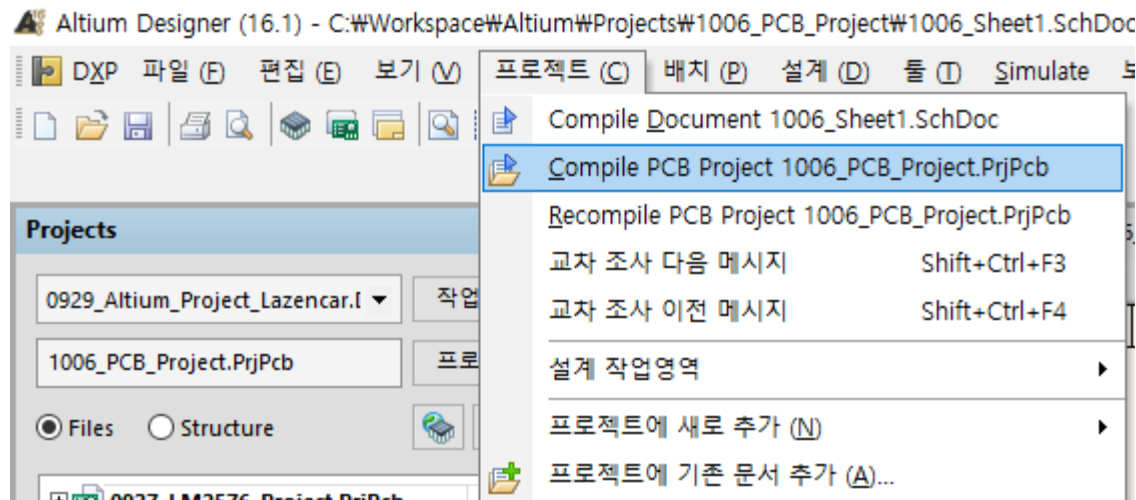
모두 켜기 (O) 모두 끄기 (O) 변경 목록 갱신 Reset All 주석 취소 (B) 변경 확인(ECO 생성) 닫기 마스크 레이어

전원포트 네트이름 변경,
배선배치, 사용하지 않는 핀에 지정되지 않은 **ERC** 배치

ERC - Electronic Rule Checking



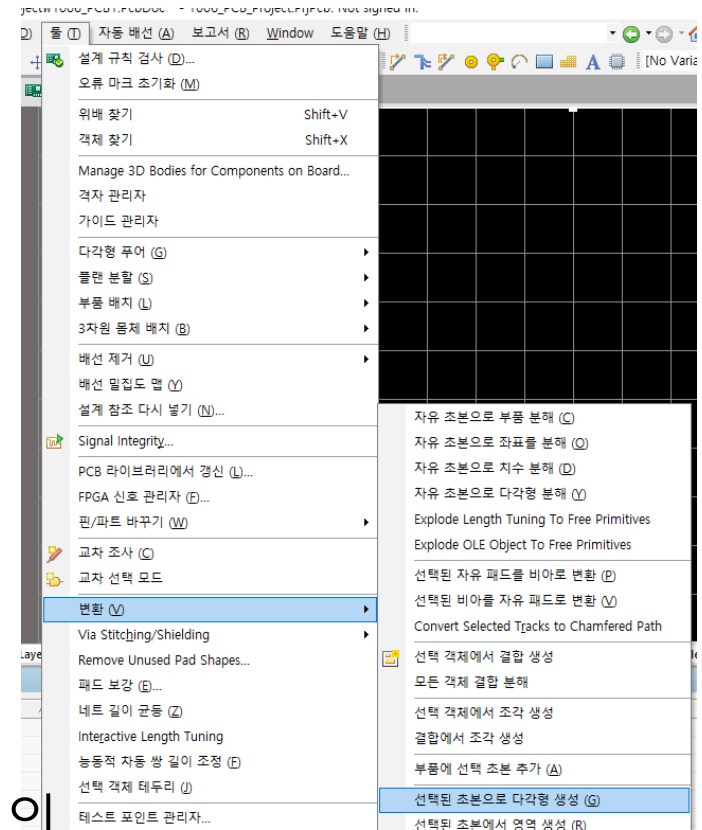
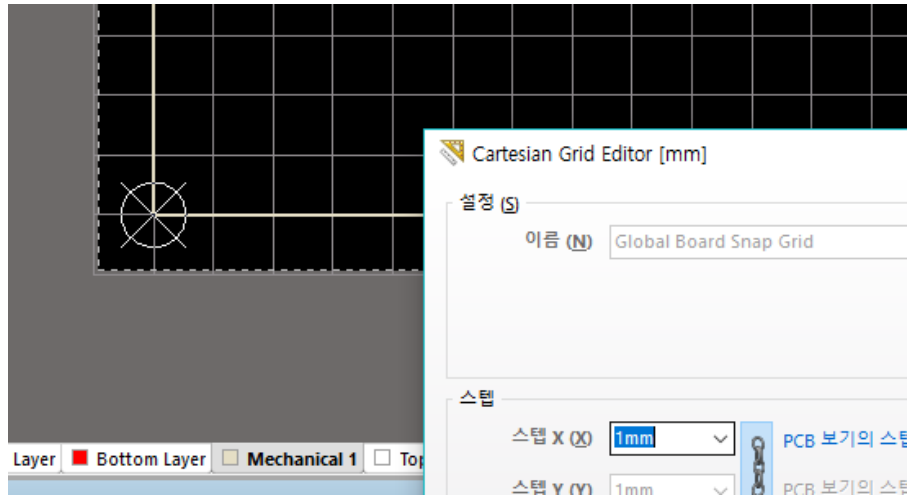
회로도 오류검사(Compile Project(.PrjPcb))



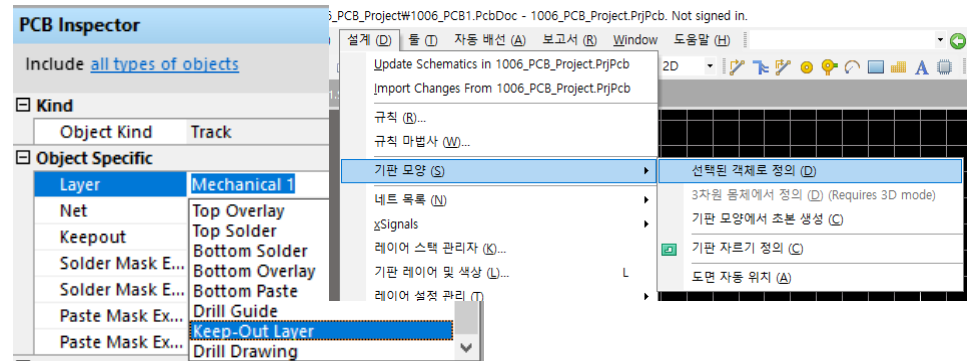
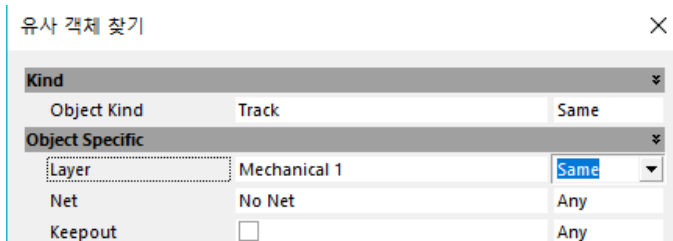
Message창에 Compile Successful 확인 → 회로도에 부품배치 및 wiring 완료

[Info]	1006_PCB_Project.PrjPcb	Compiler	Compile successful, no errors found.
--------	-------------------------	----------	--------------------------------------

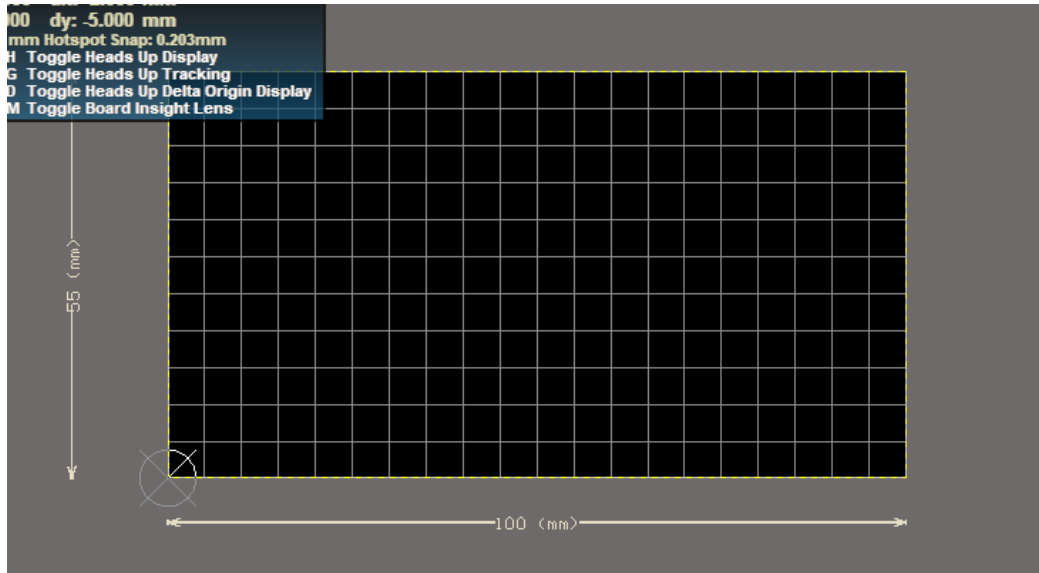
기준점 설정하고 100mm x 55mm
(place line / jump to location)



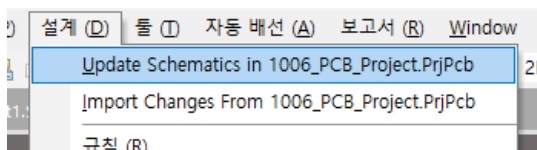
유사객체 찾기 → 다각형 생성, 기판모양 정의



Place dimension 보드 치수 표시하기 (차후에 수정가능)



Netlist 가져오기

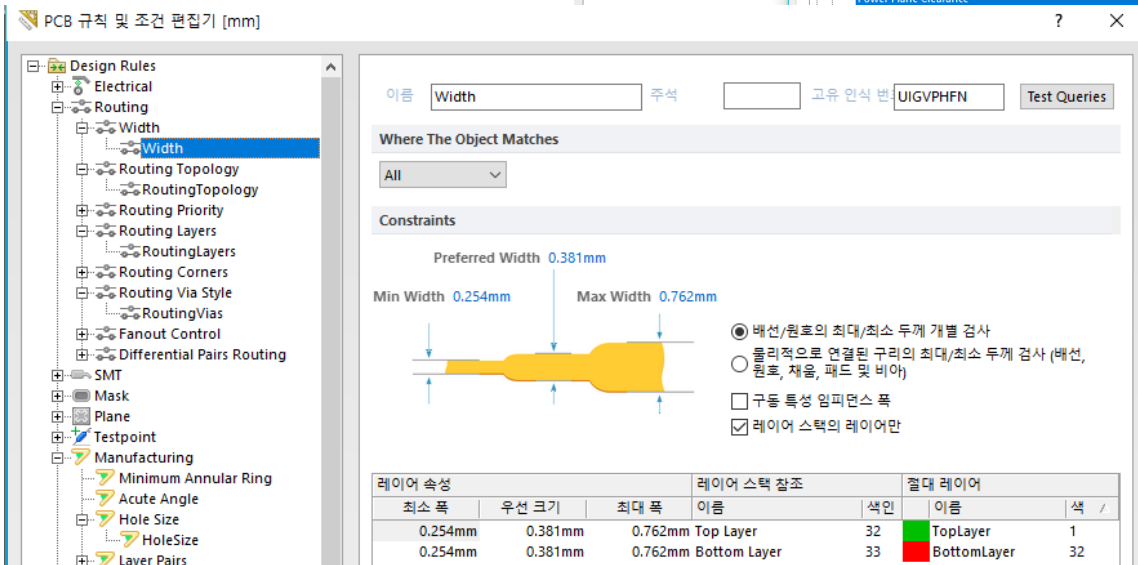
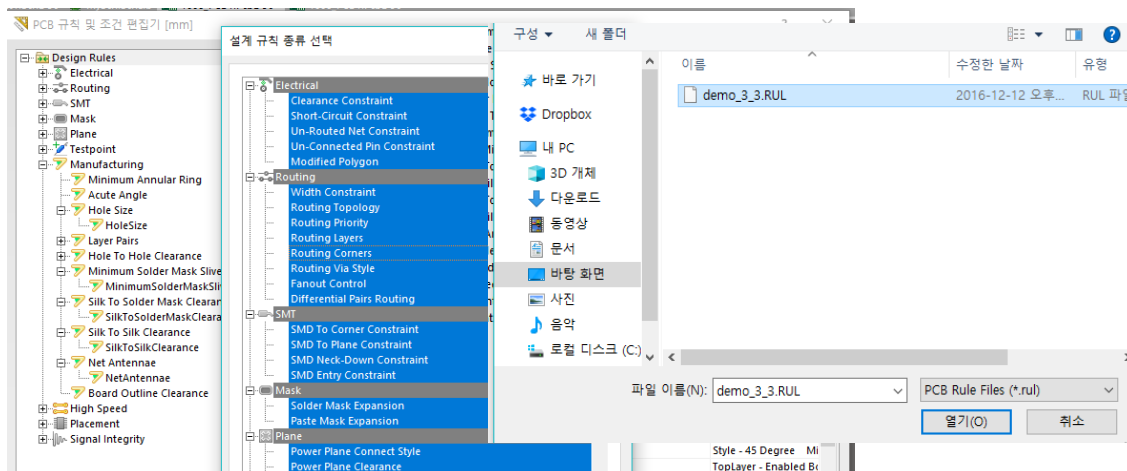
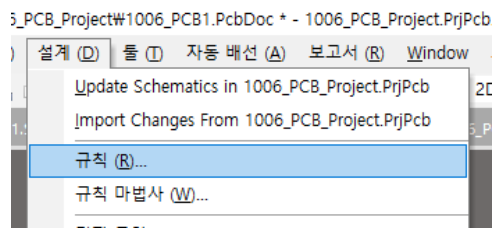


기술 변경 명령

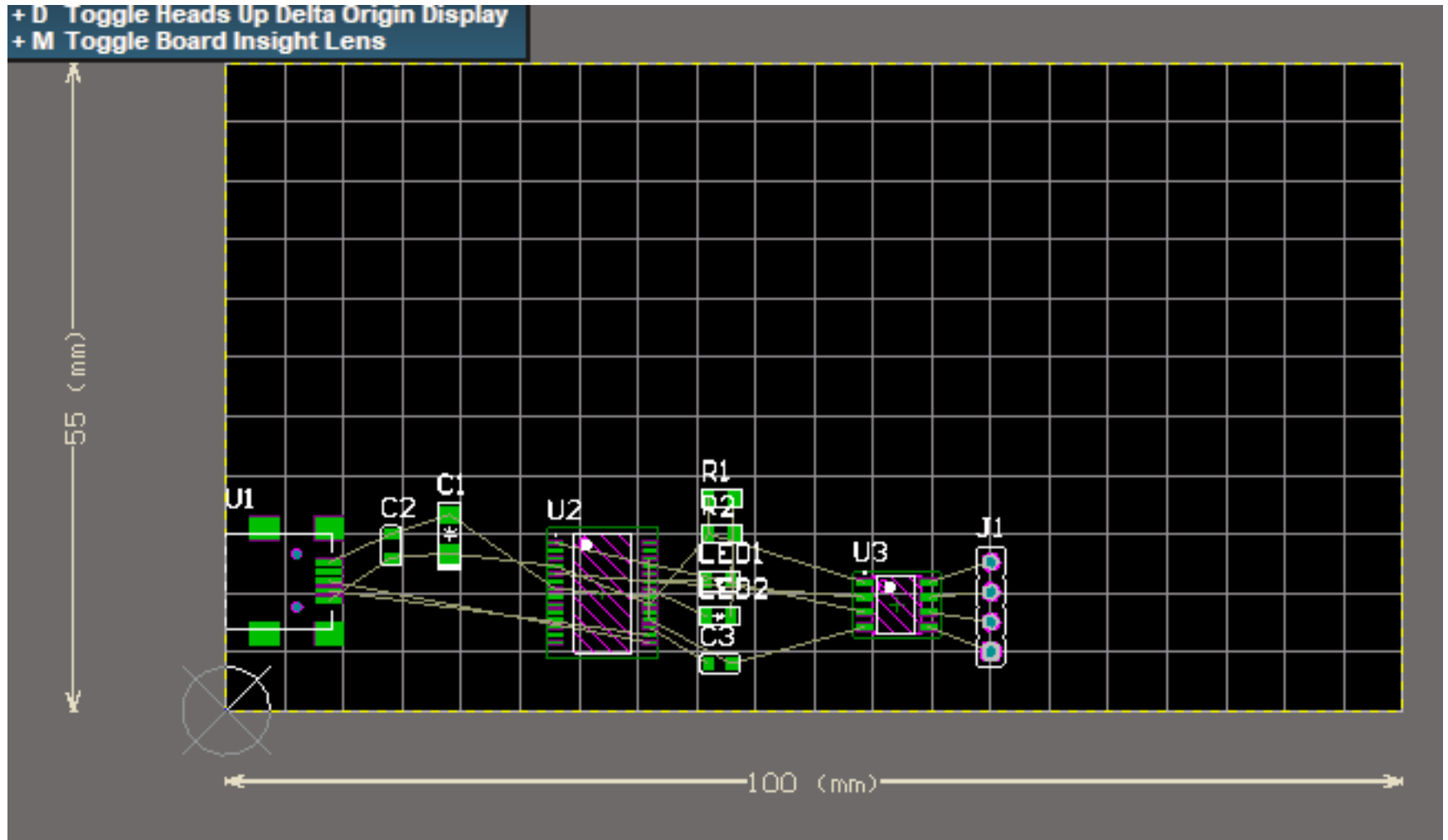
변경	활성	활동	영향 대상	영향 문서	상태	검사	마침	메시지
Add Components(11)								
<input checked="" type="checkbox"/>	Add		C1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		C2	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		C3	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		J1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		LED1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		LED2	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		R1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		R2	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		U1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		U2	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		U3	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
Add Nets(15)								
<input checked="" type="checkbox"/>	Add		GND1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		GND2	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetC3_1	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetU1_2	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetU1_3	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetLED1_A	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetLED1_C	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetLED2_A	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	
<input checked="" type="checkbox"/>	Add		NetLED2_C	To	1006_PCB1.PcbDoc	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	

변경 검토 변경 승인 변경 보고서 (B)... ☐ 오류만 표시 닫기

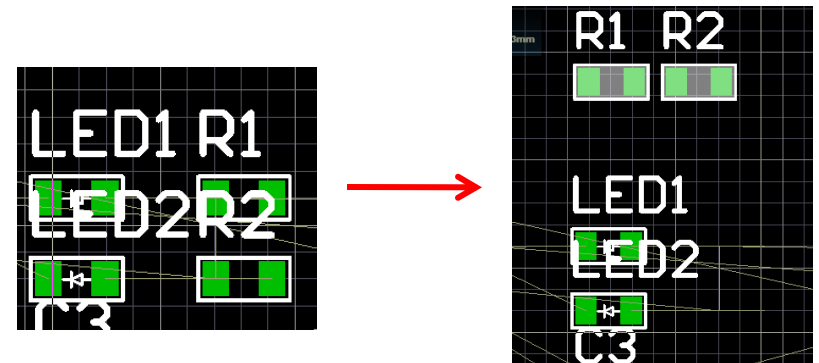
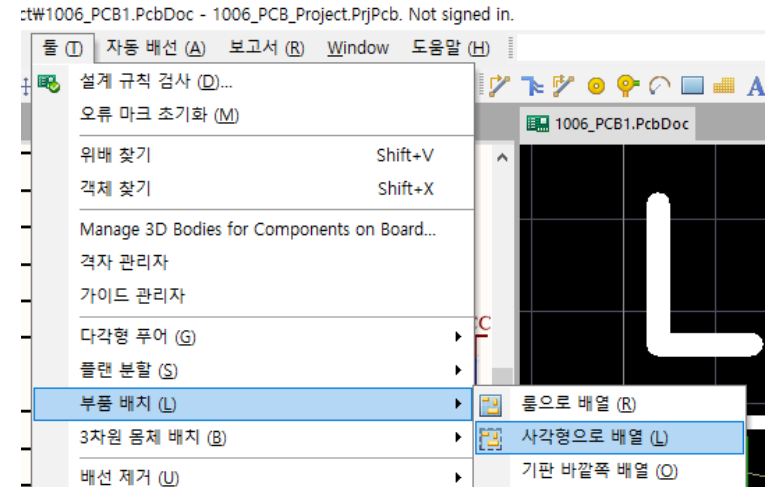
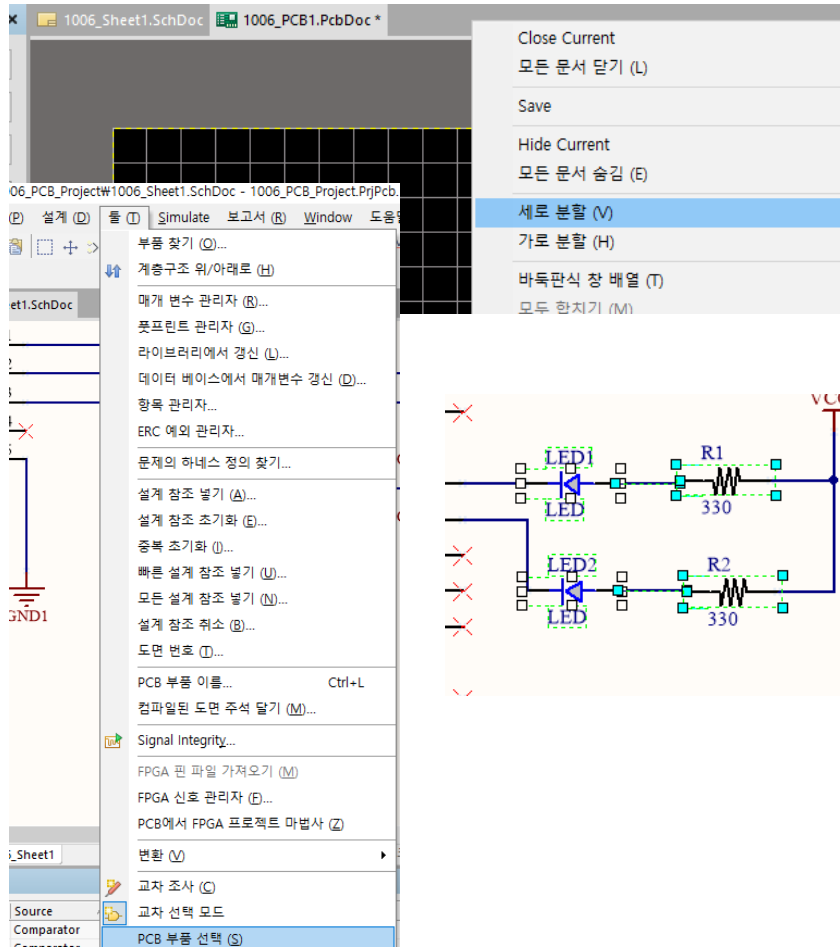
Export 해놓은 설계규칙 Import하기



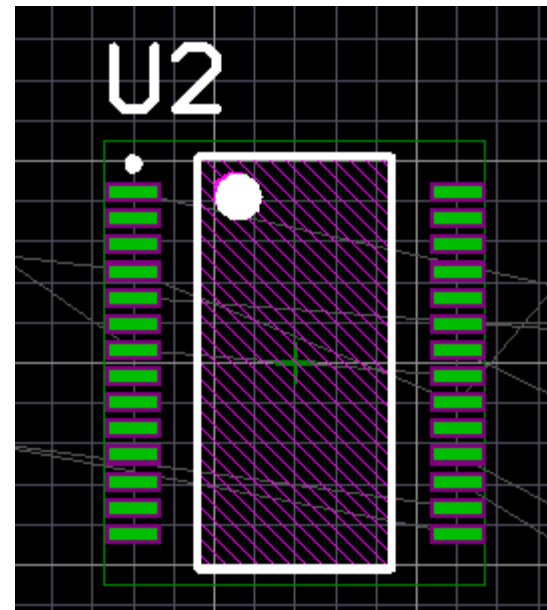
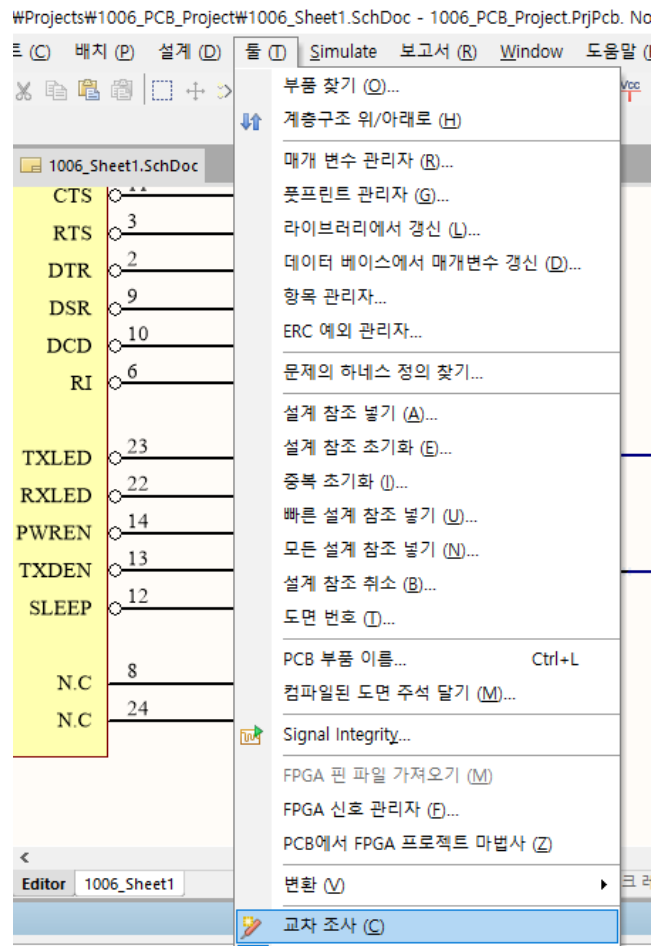
수동부품배치 (Move Component)



(*) 원하는 모양으로 부품배치하기 :
회로도에서 PCB 부품선택 → PCB에서 부품배치 → 사각형으로 배열

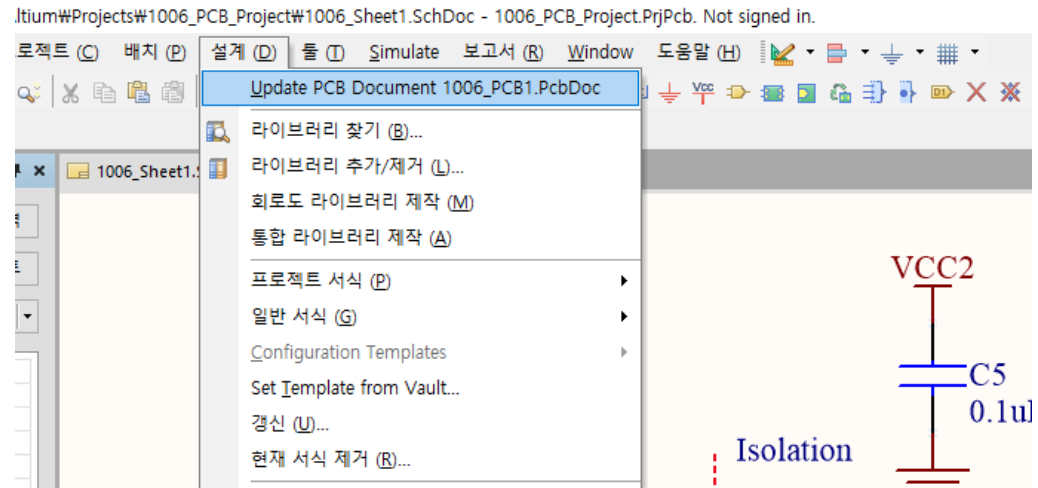
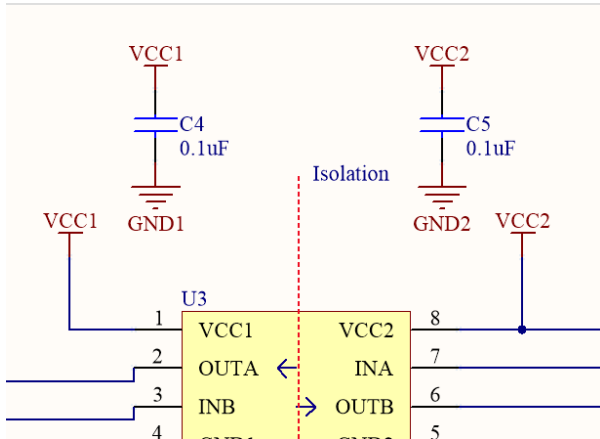


(*) 교차조사 : 회로도 PCB간 교차 탐색할 수 있다.
회로도에서 U2 클릭시 PCBdoc의 U2가 확대되어 보인다
마찬가지로 PCBdoc에서 클릭시
회로도 영역에서 PCB에서 선택된 부품만 표시된다



shift +c 로 취소

(*) 부품추가 후 Compile하고 PCB 갱신하기 (추가사항: isolation chip에 바이패스 콘덴서 2개 추가)

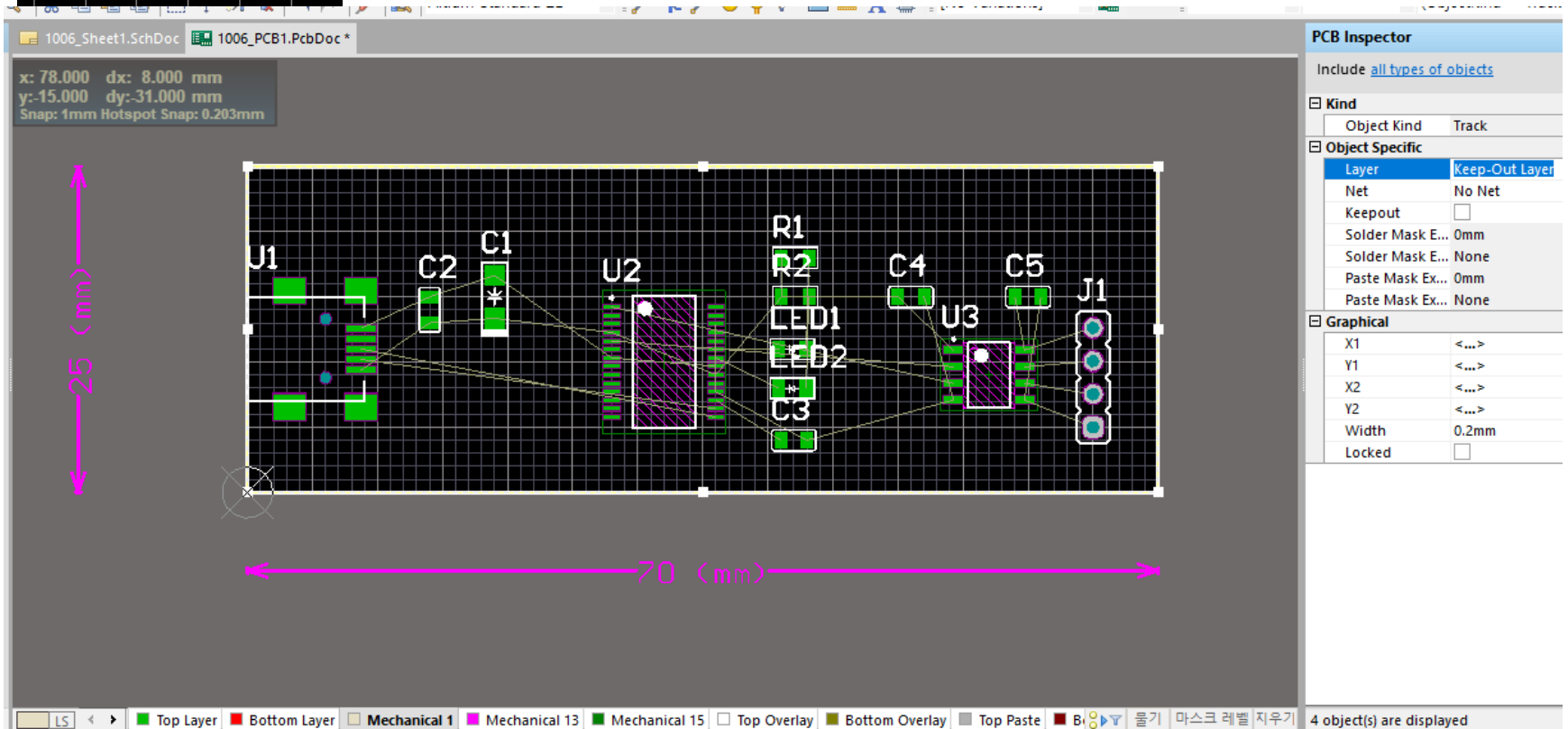
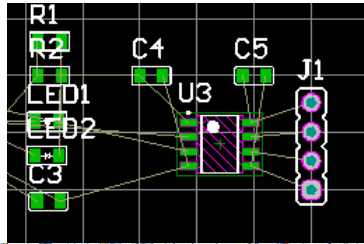


기술 변경 명령

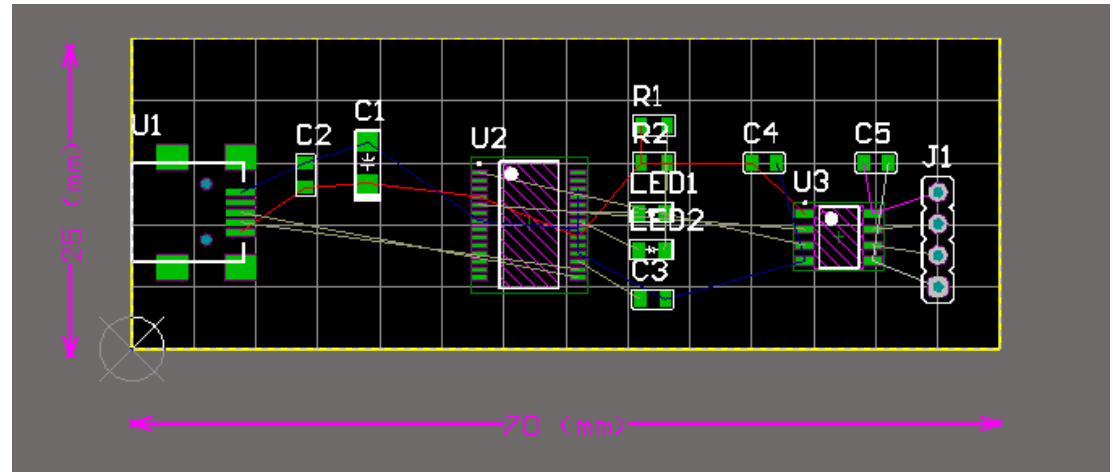
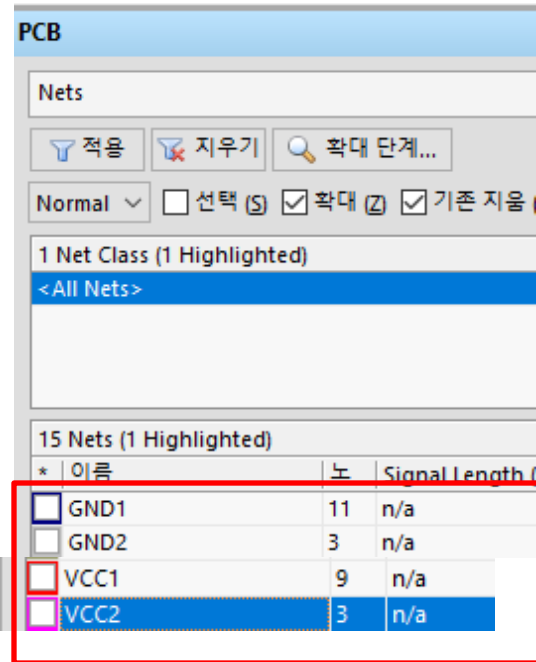
변경	활동	영향 대상	영향 문서	상태	검사	마침	메시지
+	Add Components(2)						
✓	Add	C4	To	1006_PCB1.PcbDoc	✓	✓	
✓	Add	C5	To	1006_PCB1.PcbDoc	✓	✓	
+	Add Pins To Nets(4)						
✓	Add	C4-1 to VCC1	In	1006_PCB1.PcbDoc	✓	✓	
✓	Add	C4-2 to GND1	In	1006_PCB1.PcbDoc	✓	✓	
✓	Add	C5-1 to VCC2	In	1006_PCB1.PcbDoc	✓	✓	
✓	Add	C5-2 to GND2	In	1006_PCB1.PcbDoc	✓	✓	
+	Add Component Class Members(2)						
✓	Add	C4 to 1006_Sheet1	In	1006_PCB1.PcbDoc	✓	✓	
✓	Add	C5 to 1006_Sheet1	In	1006_PCB1.PcbDoc	✓	✓	
+	Add Rooms(1)						
✓	Add	Room 1006_Sheet1 (Scope=InCompor To		1006_PCB1.PcbDoc	✓	✓	

변경 검증 변경 설명 변경 보고서 (R)... ☐ 오류만 표시 닫기

Room삭제 후 추가한 부품배치,
보드사이즈를 70 x 25mm로 축소



VCC, GND의 네트 색상 변경



규칙변경

PCB 규칙 및 조건 편집기 [mil]

Design Rules

Electrical

Routing

Width

Width

Routing Topology

RoutingTopology

Routing Priority

Routing Layers

RoutingLayers

Routing Corners

Routing Via Style

RoutingVias

Fanout Control

Differential Pairs Routing

SMT

Mask

Plane

Testpoint

Manufacturing

Minimum Annular Ring

Acute Angle

Hole Size

HoleSize*

Layer Pairs

이름

HoleSize

주석

Where The Object Matches

All

Constraints

측정 방법

Absolute

최소

1mil

최대

400mil

Manufacturing

Minimum Annular Ring

Acute Angle

Hole Size

HoleSize

Layer Pairs

Hole To Hole Clearance

Minimum Solder Mask Sliver

MinimumSolderMaskSliver

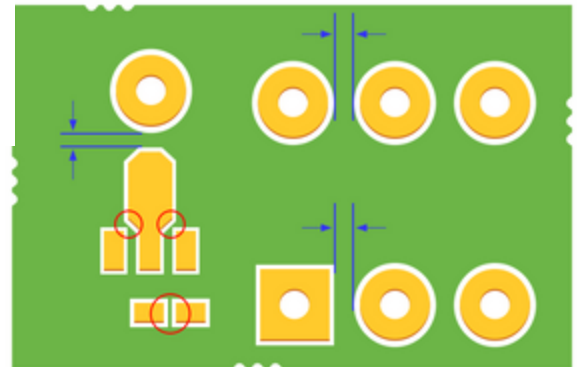
Silk To Solder Mask Clearance

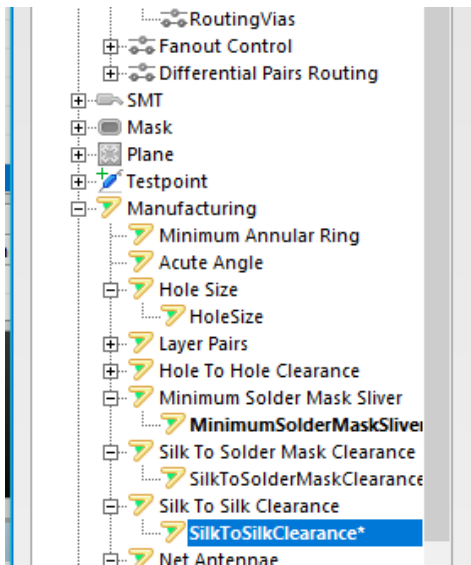


nstraints

최소 솔더마스크 간격

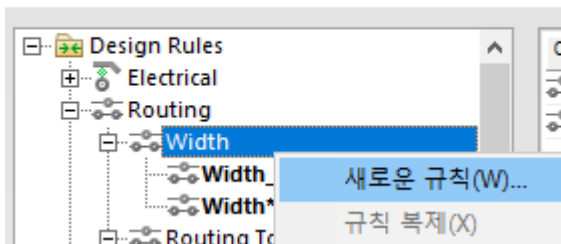
5mil



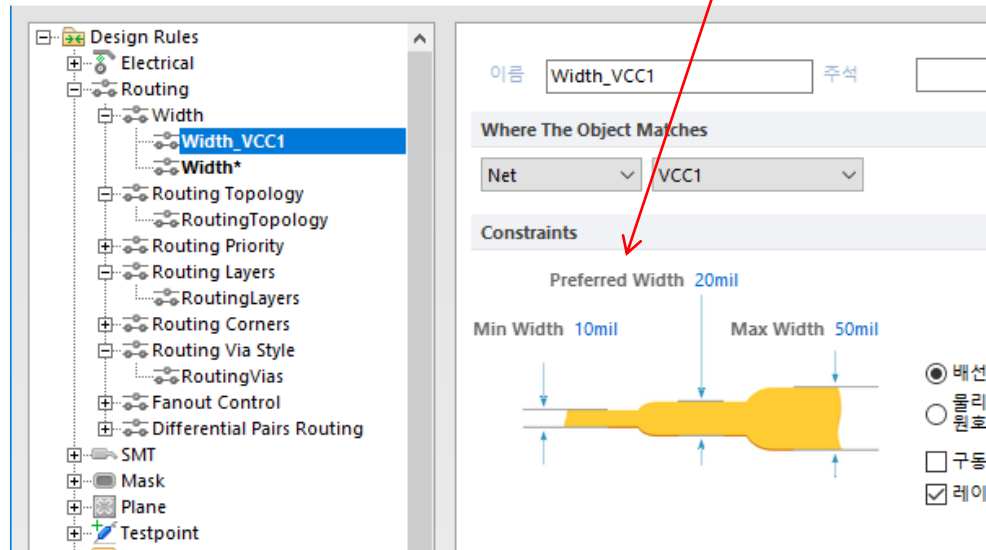


Min/Pref/Max Width는
 능동배선 배치할때
 '3' 입력하여 전환할 수 있다.

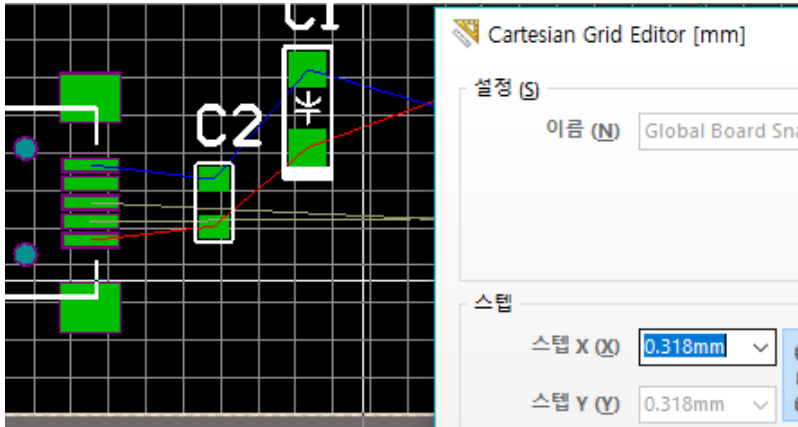
PCB 규칙 및 조건 편집기 [mil]



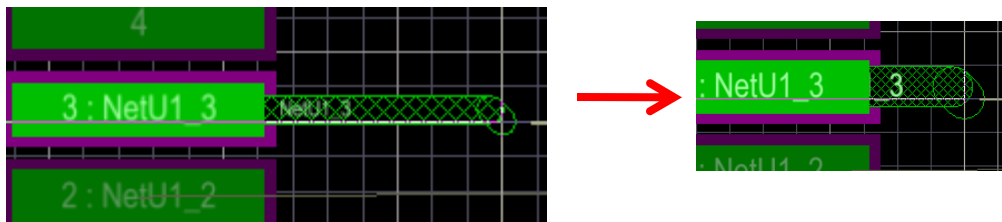
PCB 규칙 및 조건 편집기 [mil]



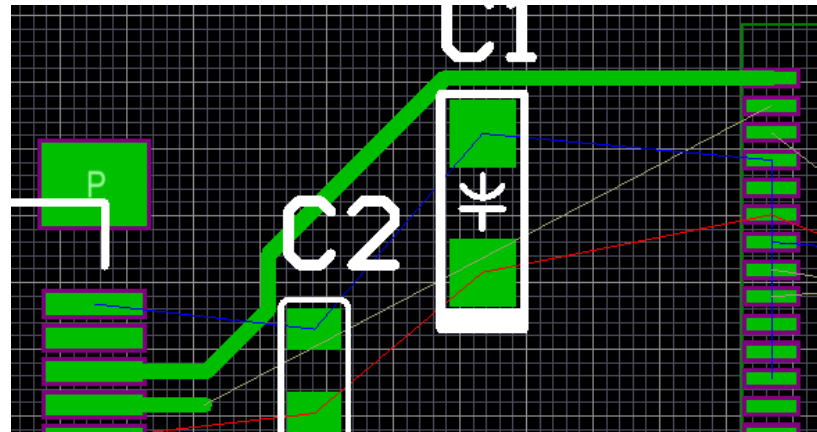
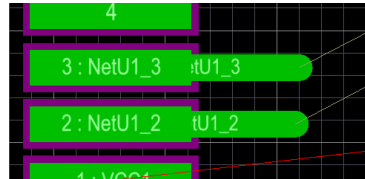
Grid를 0.318mm(12.5mil)로 변경



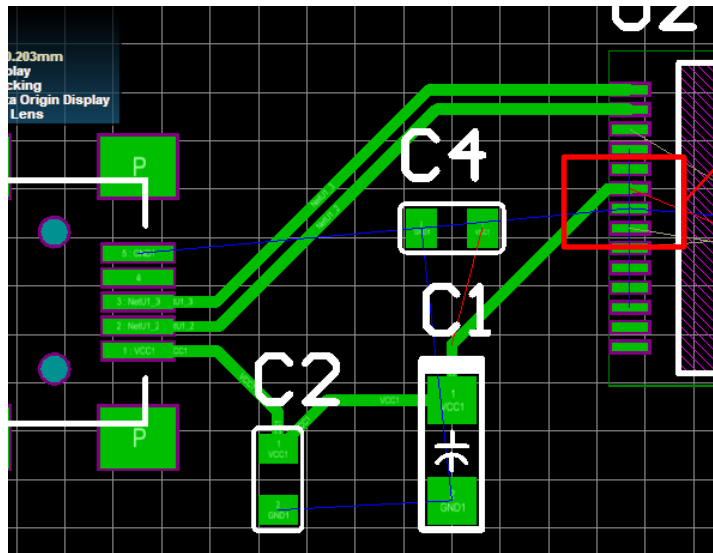
능동배선 중에 '3'을 누르면 두께 변경



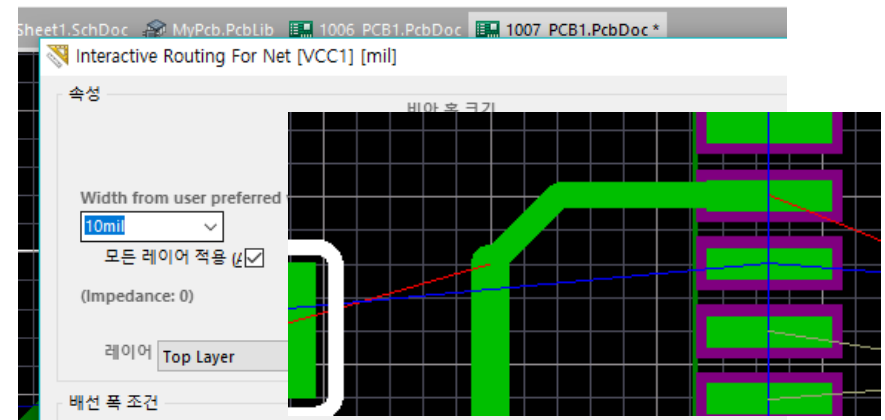
일부만 라우팅하고 연결될 부분에서 능동배선 모드로 들어간 후, ctrl+왼쪽클릭 하면 자동으로 배선이 완성된다.



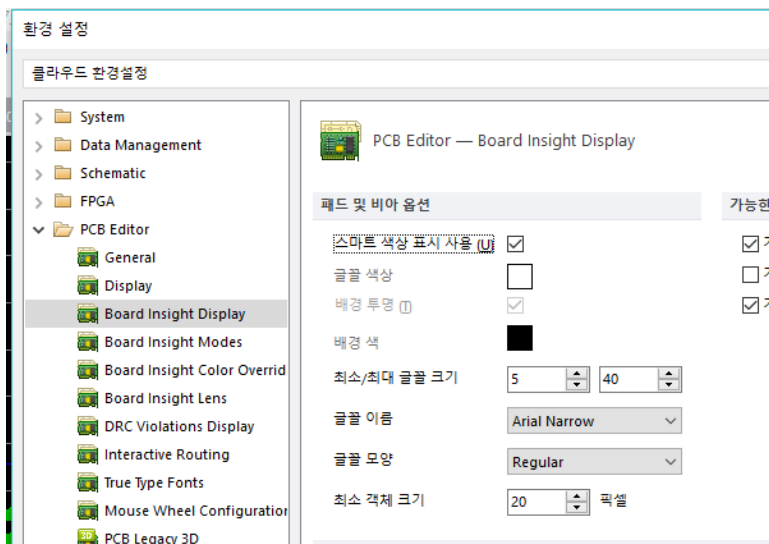
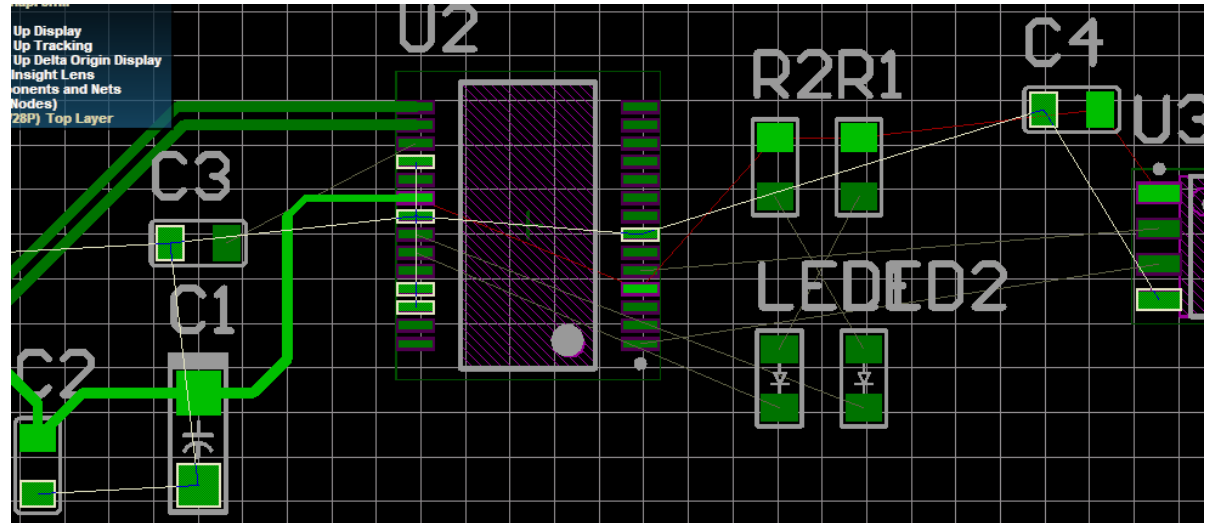
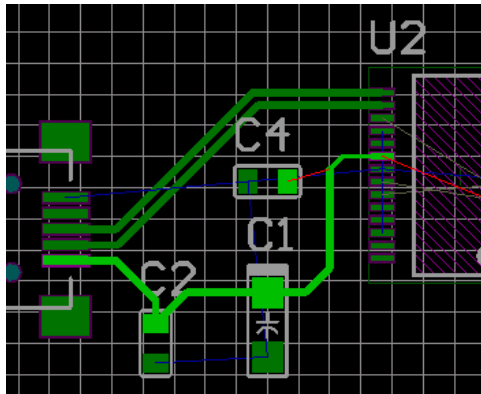
부품 이동 시 'R' 키 누르면 3가지 모드를 순환한다.
부품 밀어내기 / 겹치기 / 겹돌기



선 폭이 패드보다 넓다. 즉
실시간 DRC(Design Rule Check)오류 발생
Tab하여 다음과 같이 변경

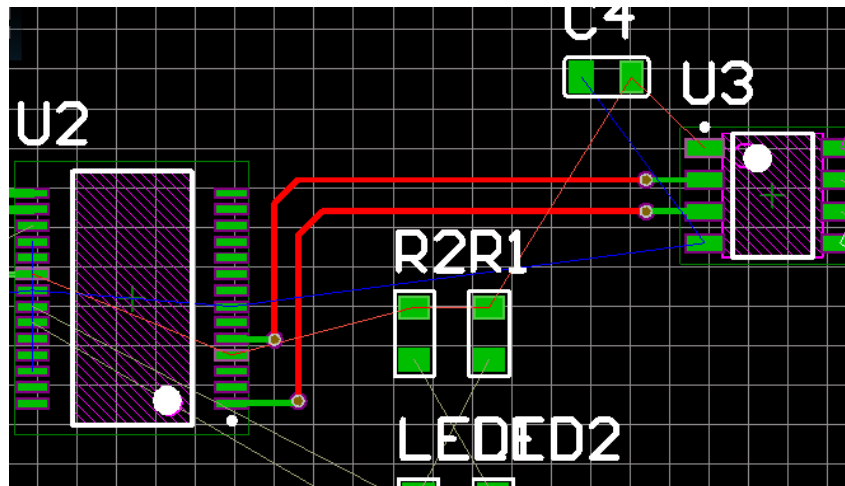
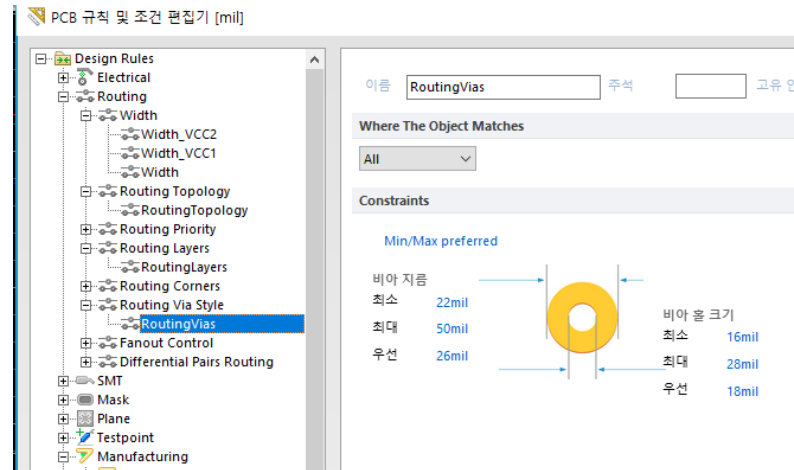
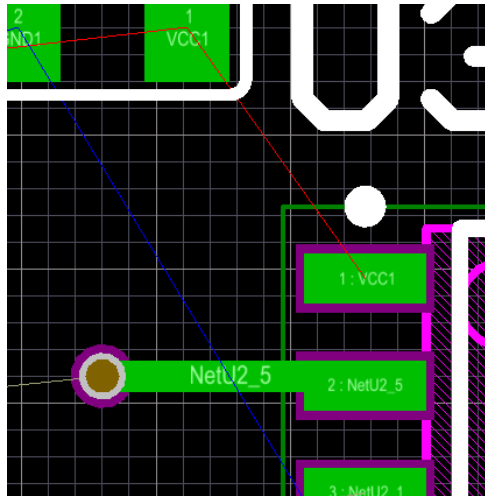


VCC1 영역만 강조해서 보고 싶을때는 PAD 를 ctrl+왼쪽클릭 → ctrl+ 더블클릭 Shift 누르면, 네트와 패드가 강조된다.



← 강조기능은 여기서 설정

일부 배선하고 '2' (비아형성), '4' (비아크기 변경)
(여기서는 설정해 준 최소크기로 비아를 형성하였다)



← 레이어 변경 : 'L'

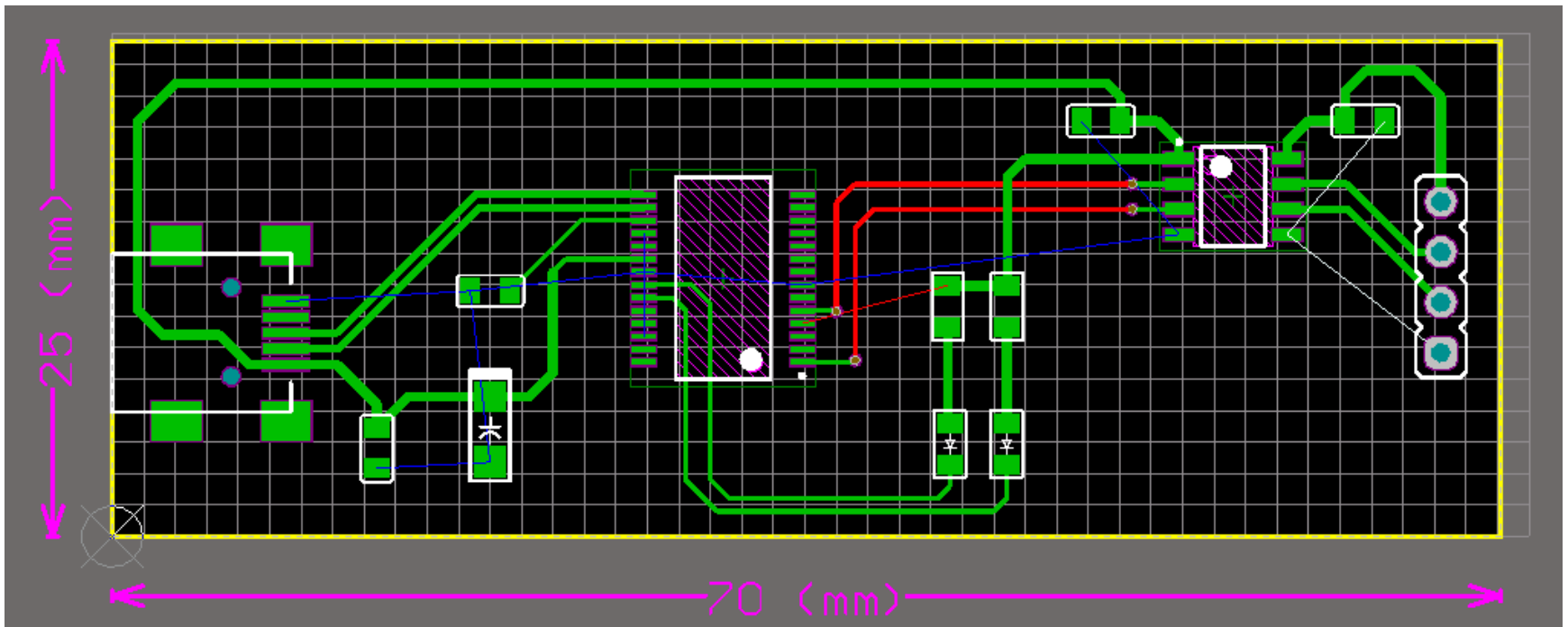
GND1,2 를 제외하고 배선작업을 완료한다.

(*) 옵션 > 표시/숨김 > 문자

(*) 일반적으로 TOP면은 수직배선해놓고 BOTTOM면은 수평배선한다.
→PCB 뒤틀림 방지방법 최근에는 제조사양이 좋아져서 사용하지 않음

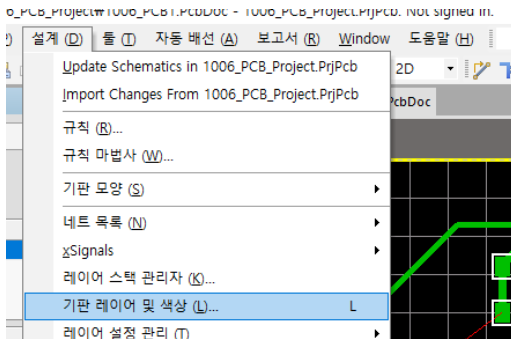
(*) 비아를 사용하던 아니던 TOP면으로 배선을 시작하면 될수있으면 TOP면으로 배선할수있는 만큼 배선한다. 비아를 많이 사용하것은 결코 좋은 아트웍이라고 할수없다.

(*) T분기는 피한다. 설계규칙, EMI관련해서도 금지하고 있음



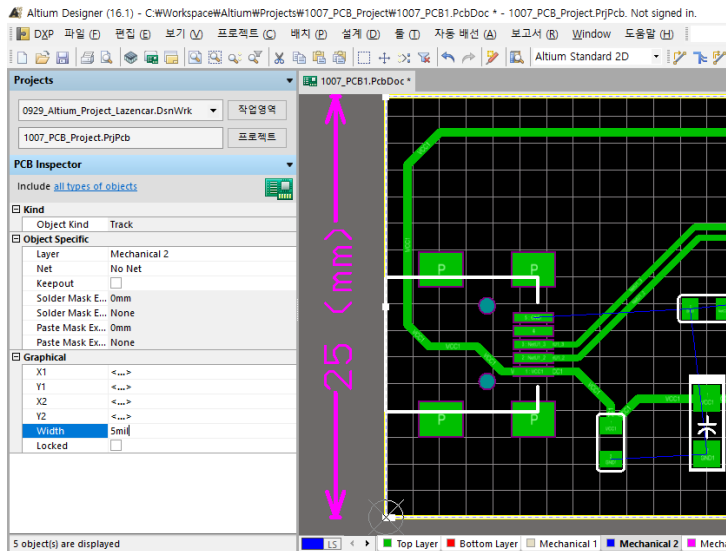
Mechanical 2 Layer 추가한다

×

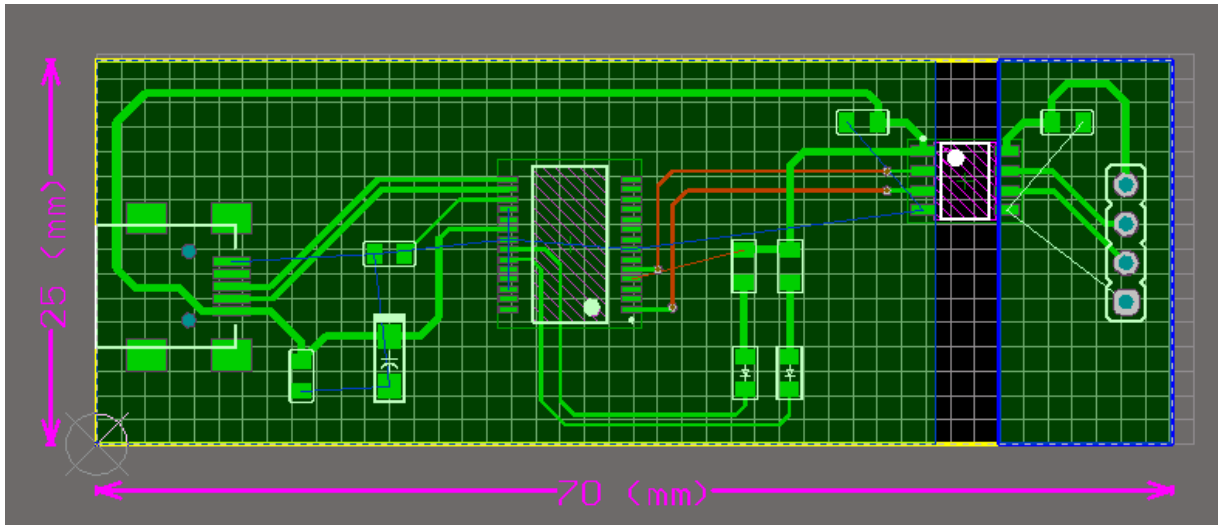
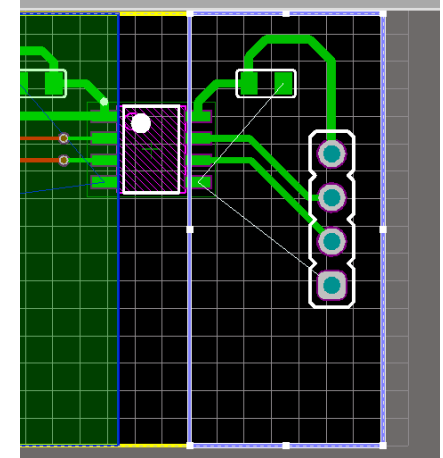
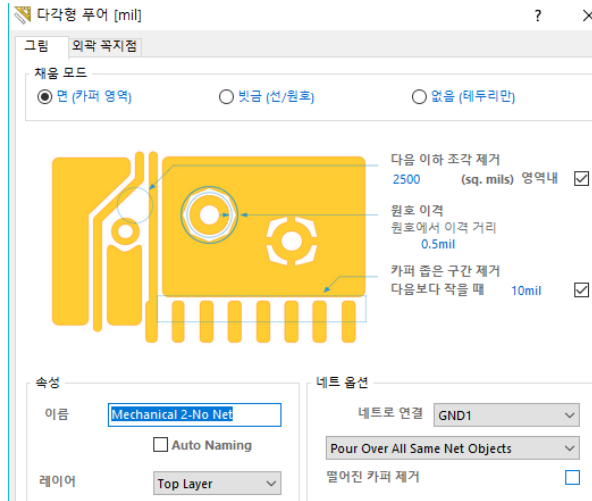
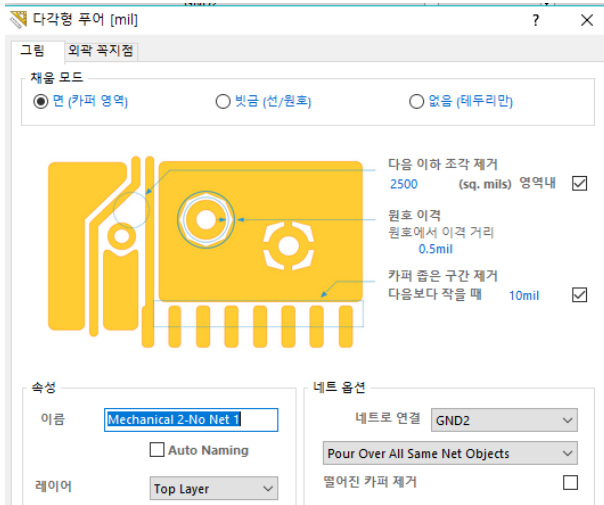


색상	보기	기구 레이어 (M)	색상	보기	활성	단일 레	연결된 도면
		Mechanical 1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Mechanical 2		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Mechanical 13		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		Mechanical 15		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Mechanical2 Layer에서 Place Line하여 사각형 그리고
PCB Inspector 에서 width 5mil로 변경 → 톨>변환> 선택된 초본으로 다각형 생성



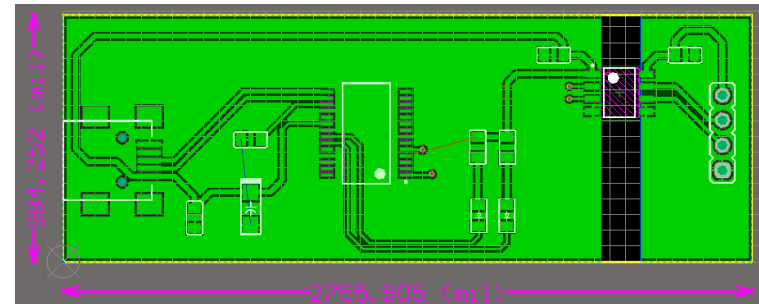
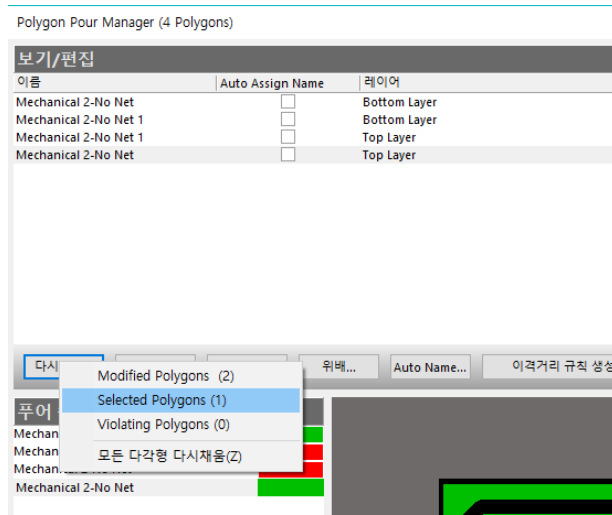
생성된 다각형 더블클릭하여 다각형 푸어 생성하고
우측의 다각형에 대해서도 동일하게 작업한다.



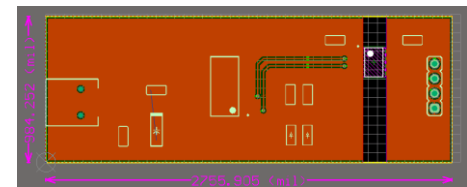
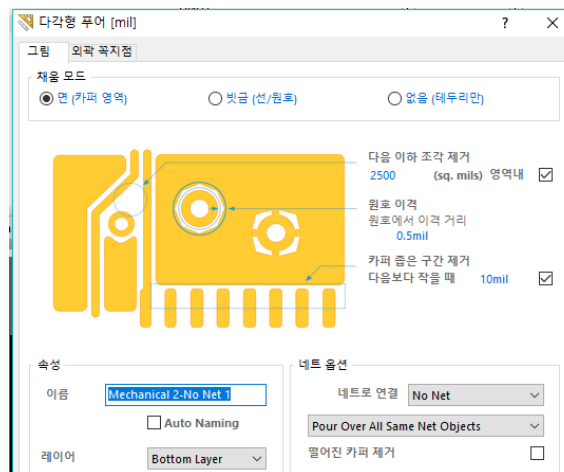
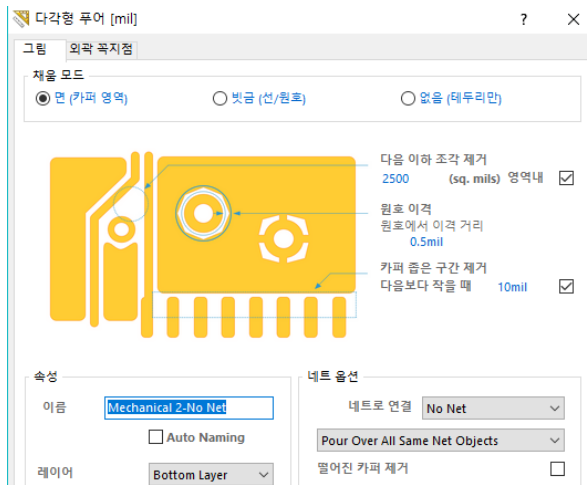
(*) '다각형 푸어' 기능으로
설계하고자 하는 동박면의
위치를 지정한 상태

이후, 동박을 덮는 작업을
추가하여야 카퍼 작업이 완료된다.

다각형 채움 → 동박이 씌워진 모습을 볼 수 있다.

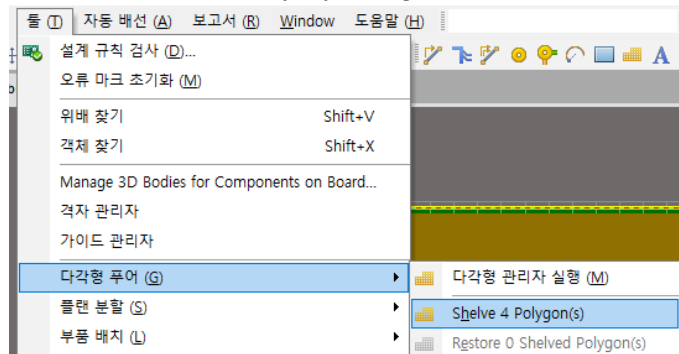


Bottom 영역에도 다음과 같이 다각형 푸어를 생성한다.



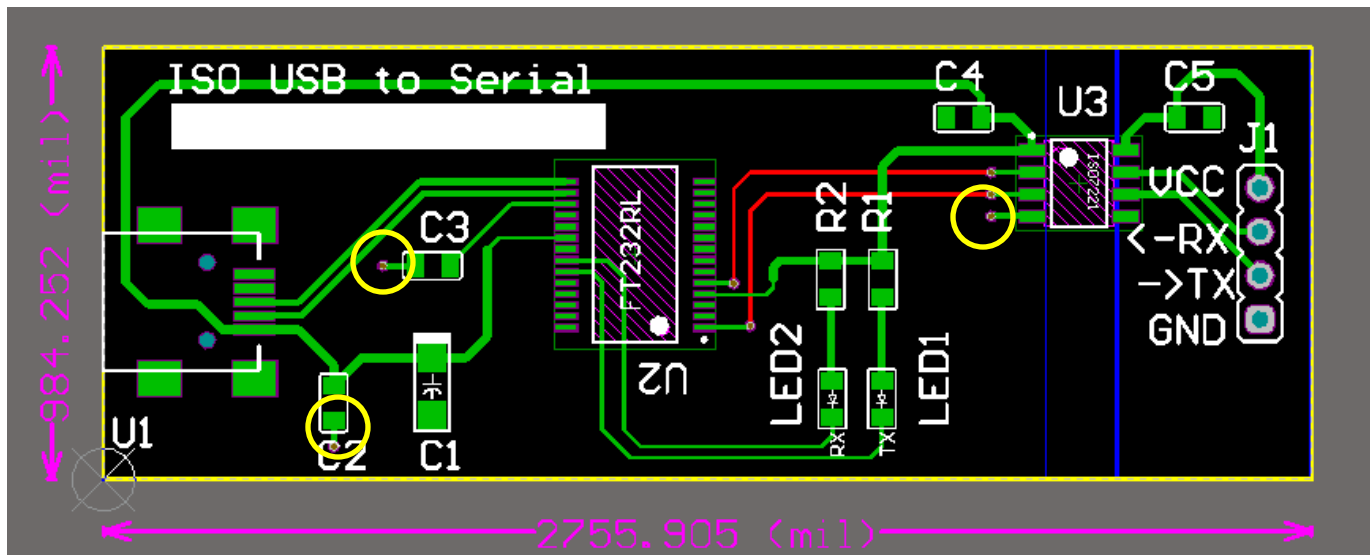
다각형 푸어를 해제하고, **비아**를 추가하여
Top, Bottom 다각형 푸어 영역이 연결되도록 한다.

:\tw1007_PCB1.PcbDoc * - 1007_PCB_Project.PrjPcb. Not signed in.

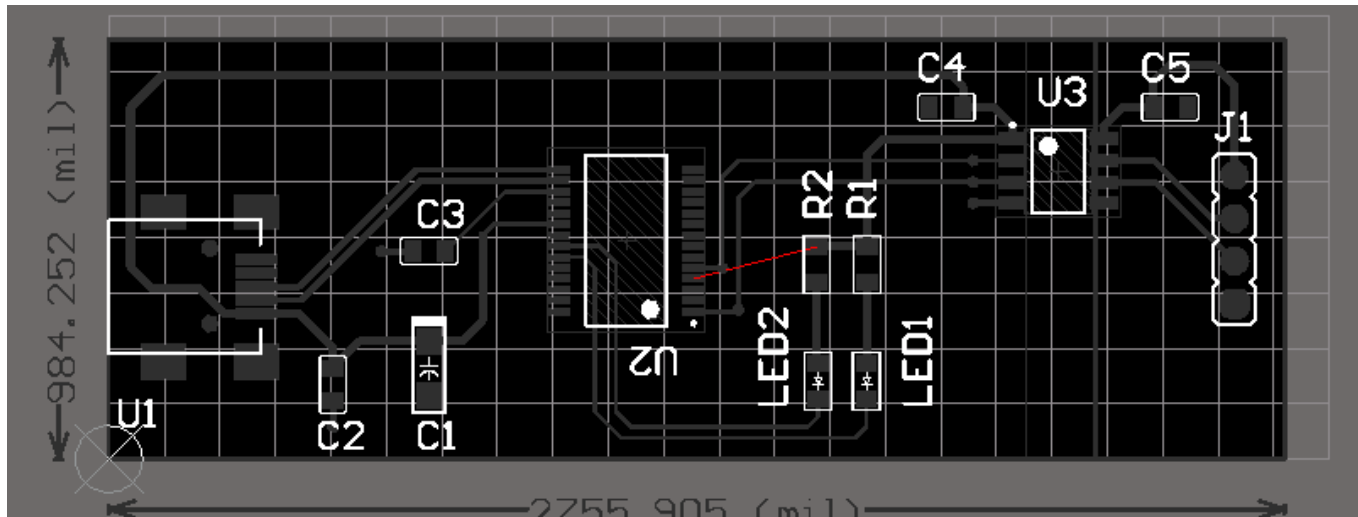


(*) 스티치 비아라고 한다.

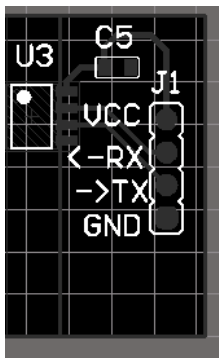
- copper층과 copper 층 사이에 비아로 뚫어서 연결을 해주는 비아로써 GND or PWR 보강을 위해 많이 사용된다.
- 서로 다른 층에 있는 더 큰 구리 영역을 함께 묶어 보드 구조를 통해 강력한 수직 연결을 만들어서 낮은 임피던스와 짧은 리턴 루프를 휴지하는데 사용 되는 기술
- Vía stitching을 하면 아날로그 회로에서 디지털 잡음이 더 적음



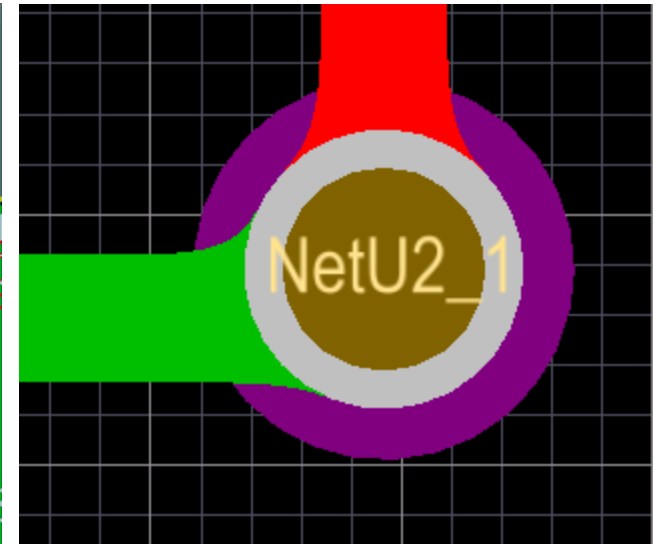
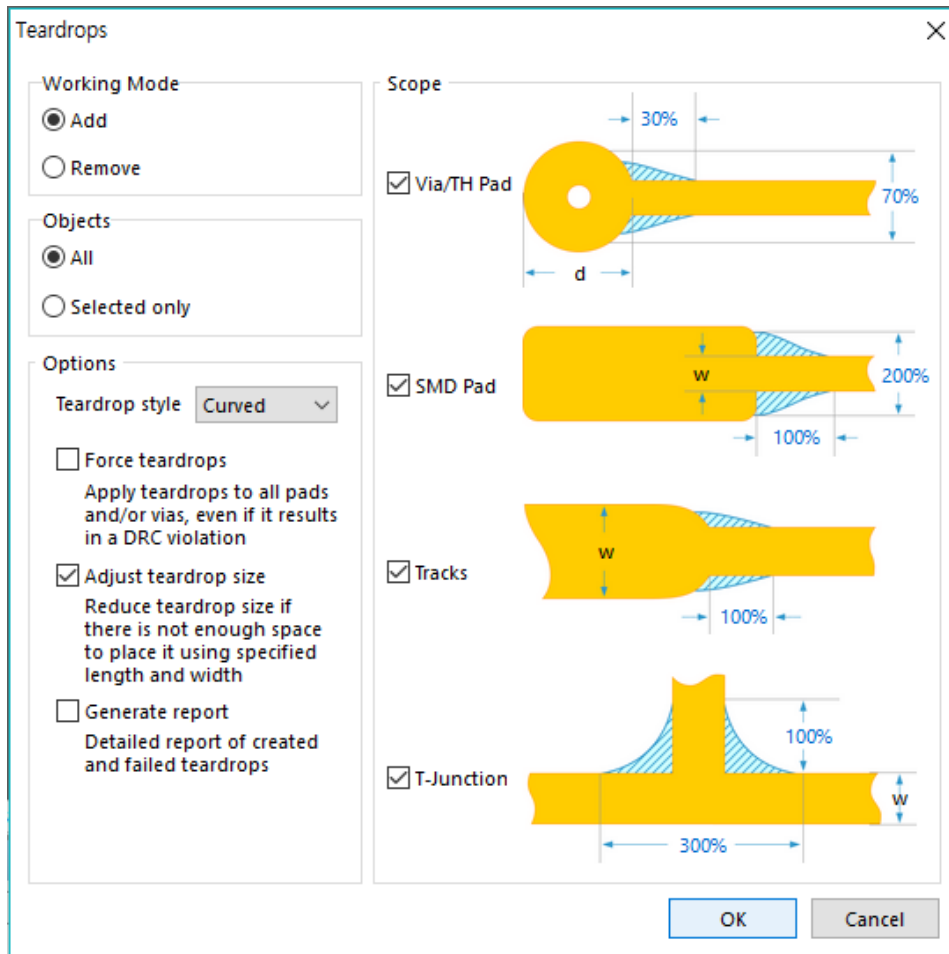
Top Overlay 에서 shift+S (레이어 선택)→ 문자 정렬



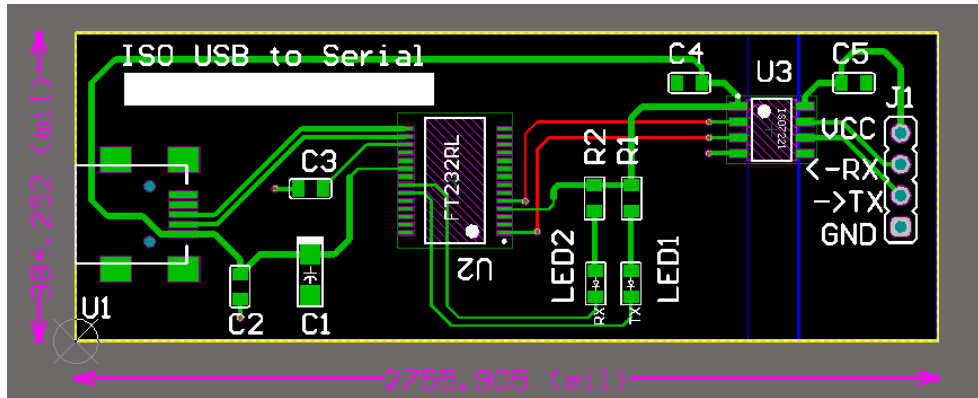
Place Text , 채움영역 설정



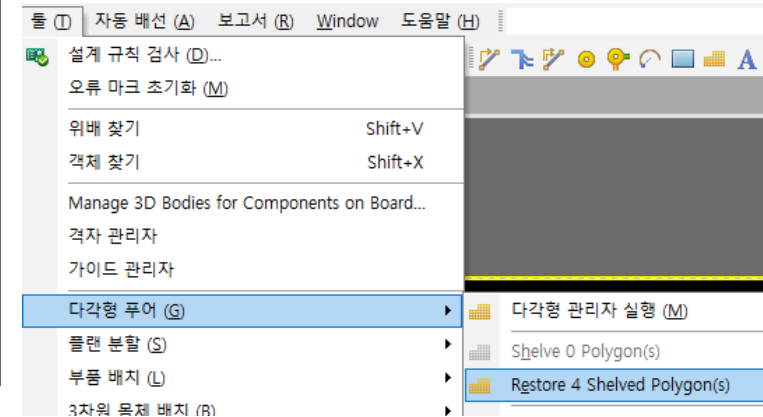
툴 > 패드보강 : Teardrop 관련 설정



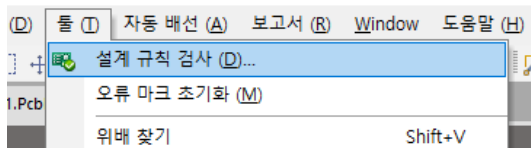
동박을 다시 씌우고 설계규칙검사를 시행



#1007_PCB1.PcbDoc + - 1007_PCB_Project.PrjPcb. Not signed in.



Project#1007_PCB1.PcbDoc + - 1007_PCB_Project.PrjPcb. Not signed



Altium Designer

Design Rule Verification Report

Date: 2018-10-08
Time: 2018-10-08 11:35:59
Elapsed Time: 00:00:01
Filename: C:\Workspace\Altium\Projects\1007_PCB_Project\1007_PCB1.PcbDoc

Warnings: 0
Rule Violations: 0

Summary

Warnings	Count
----------	-------

(*) 설계 규칙 변경 관련

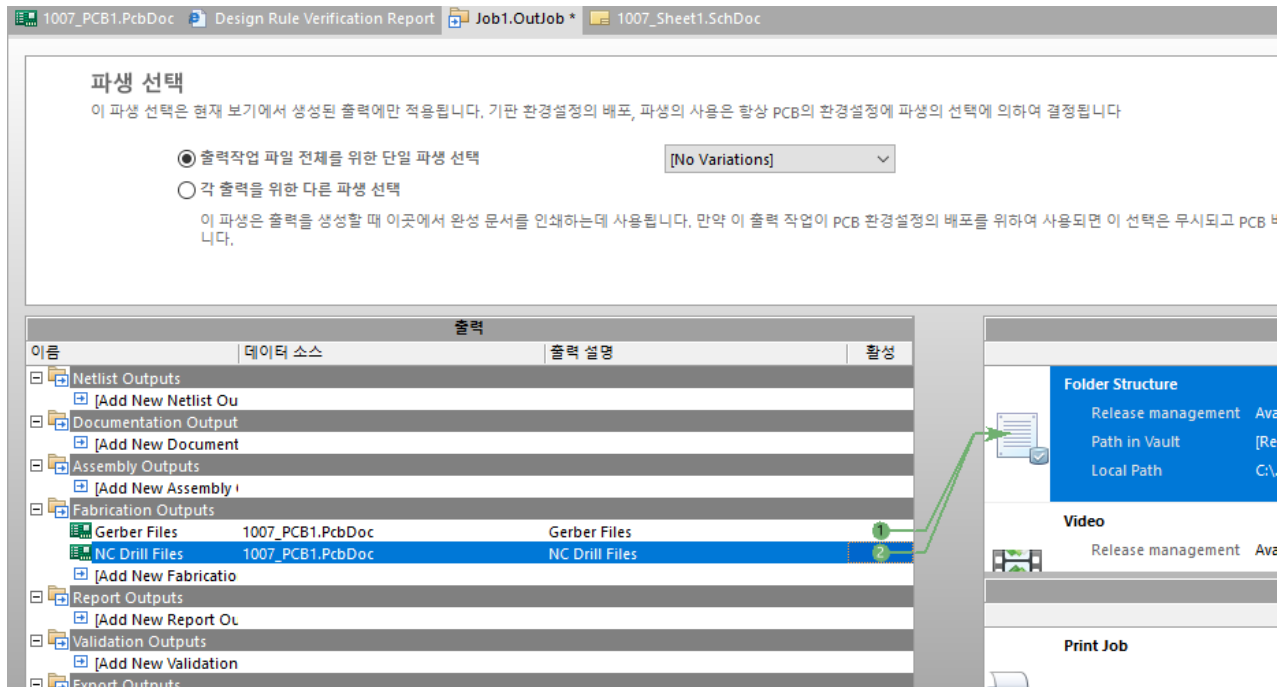
(설계 > PCB 규칙 및 조건편집기)

Minimum Solder Mask Sliver : 최소 솔더마스크 간격보다 솔더마스크가 가까이 있음
→minimum solder mask sliver 에서 최소간격을 10mil보다 작게

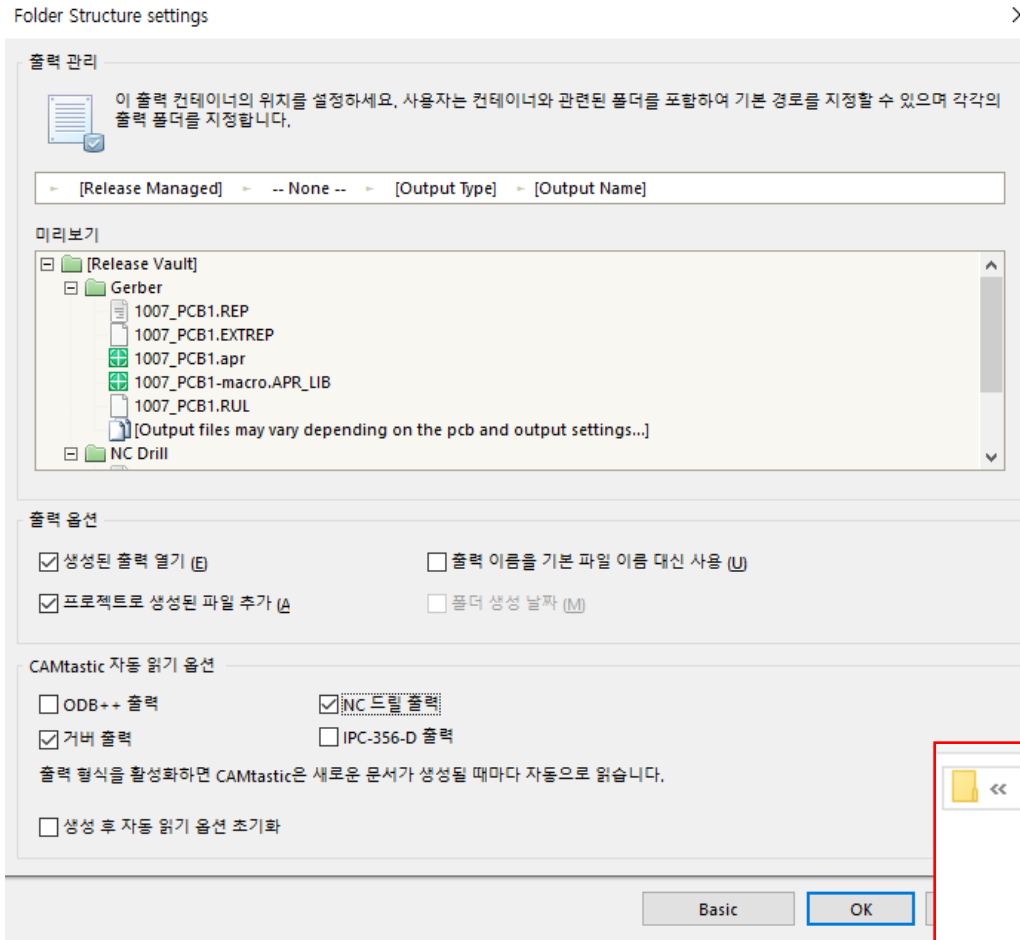
Silkscreen Over Component Pads : 패드에 실크가 올라가 있음
→Silkscreen Over Component pads 를 DRC체크를 빼시면 에러는 잡지 않겠지만 공정 시 패드 위에 실크가 올라가서 기판을 사용할 수 없게 된다

silkscreen to object minimum clearance : PCB에 부품 및 부품의 형상, 부품 레퍼런스 번호가 적히는 실크와 납땜 부분 사이의 거리가 너무 좁아 발생하는 설계 위배 사항

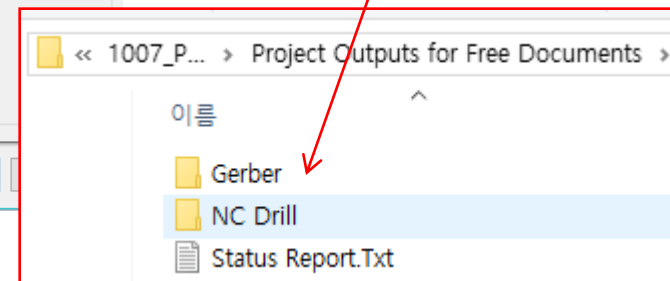
[4] Output Job 파일 생성



툴 > 작업옵션, 일괄실행

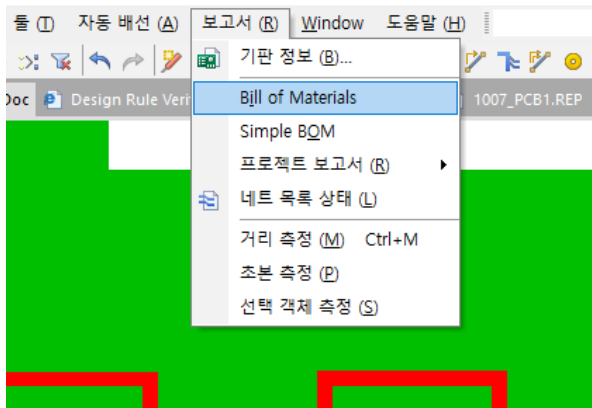


생성된 Gerber, Drill파일
을 압축하여 발주하
면 된다

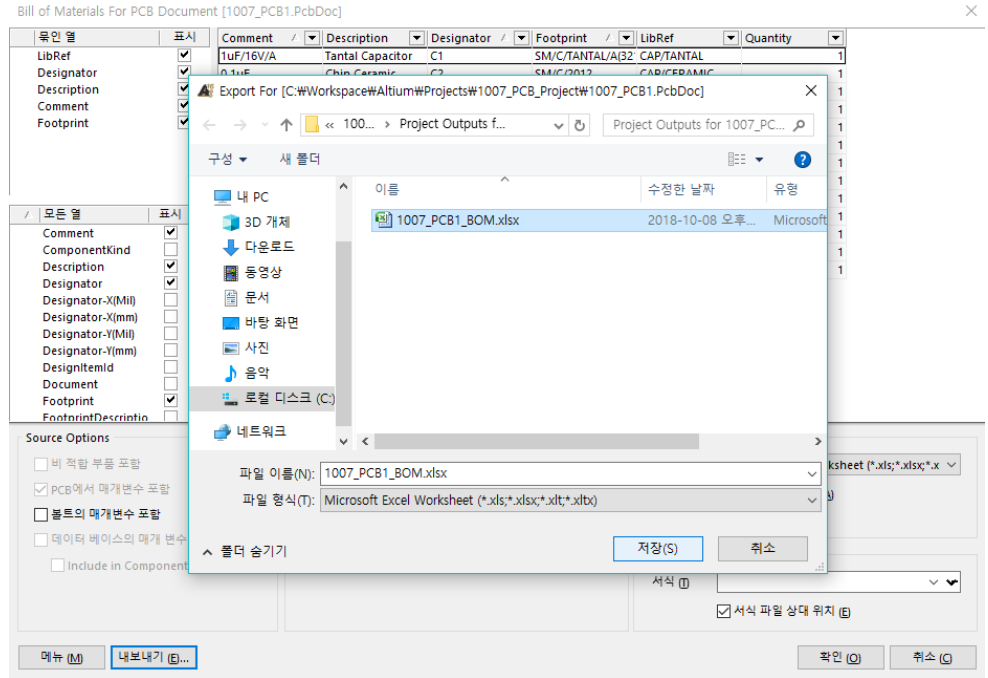


[5] BOM 출력

#1007_PCB1.PcbDoc - 1007_PCB_Project.PrjPcb. Not signed in.



	A	B	C	D	E	F
1	Comment	Description	Designator	Footprint	LibRef	Quantity
2	1uF/16V/A	Tantal Capacitor	C1	SM/C/TANTAL/A[32	CAP/TANTAL	1
3	0.1uF	Chip Ceramic	C2	SM/C/2012	CAP/CERAMIC	1
4	0.1uF	Chip Ceramic	C3	SM/C/2012	CAP/CERAMIC	1
5	0.1uF	Chip Ceramic	C4	SM/C/2012	CAP/CERAMIC	1
6	0.1uF	Chip Ceramic	C5	SM/C/2012	CAP/CERAMIC	1
7	04P	Pin Header, Pitch 2	J1	HL/HAD/P2.54/04P	HAD/P2.54/04P	1
8	LED		LED1	SM/LED/2012/GREE	LED	1
9	LED		LED2	SM/LED/2012/GREE	LED	1
10	330	1/4W Resistor	R1	SM/R/2012	RESISTOR	1
11	330	1/4W Resistor	R2	SM/R/2012	RESISTOR	1
12	Mini USB	Mini USB 05P, AB-T	U1	SM/CONT/MINIUSB	CONT/MINIUSB/AB	1
13	FT232RL	FT232 USB UART IC	U2	M/IC/SSOP/28P	IC/FT232RL	1
14	ISO7221	ISO722x Dual-Cha	U3	SM/IC/SOIC/08P	IC/ISO7221	1
15						



[6] PDF파일 생성

스마트 PDF

내보내기 대상 선택

스마트 PDF는 현재 보여진 문서 또는 전체 프로젝트를 내보낼 수 있습니다.

스마트 PDF는 현재 보여진 문서 또는 현재 프로젝트의 문서를 내보낼 수 있습니다.

- 현재 프로젝트 (P) (1007_PCB_Project.PrjPcb)
○ 현재 문서 (D) (1007_PCB1.PcbDoc)

다음과 같이 이음:

C:\Workspace\Altium\Projects\1007_PCB_Project\1007_PCB_Project.pdf

스마트 PDF

프로젝트 파일 선택

목록에서 내보내기 위하여 프로젝트에 있는 피

아래의 목록에서 내보내기 위하여 파일을 선택

C:\Workspace\Altium\Projects\1007_Po
C:\Workspace\Altium\Projects\1007_Po

스마트 PDF

자재 계산 내보내기

서식을 이용한 자재 계산 파일을 선택하세요.

☐ **자재 계산 내보내기**

「자재 계산 옵션」

파생품

[No Variations]

스마트 PDF

구조 설정

PDF에서 사용할 구조를 선택하세요.

구조

이 옵션을 체크시 회로도 도면에 물리적
네트 라벨, 포트, 도면 분기, 도면 번호, 도

☐ 물리적 구조 사용