

Xilinx

Zynq FPGA

TI DSP MCU 기반의

프로그래밍 및 회로 설계 전문가

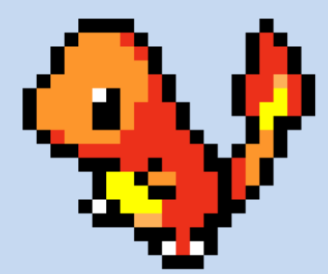
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New Project

Family: TMS570LS31x, TMS570LS21x, RM48x, TMS570LS12x, TMS570LS11x, RM46x, TMS570LS04x, TMS570LS03x, TMS570LS02x, RM42x, RM41x, TMS570LS09x_07x, RM44x, **TMS570LC43x**, RM57Lx

Device: TMS570LC4357ZWT, **TMS570LC4357ZWT_FREERTOS**

Name: Light_ADC_RTOS

Location: C:\Users\minking\Desktop\CCS pro\Light_ADC_RTOS

☐ Create directory for project

Project will be created at: C:\Users\minking\Desktop\CCS pro\Light_ADC_RTOS.

TMS570LC4357ZWT_FREERTOS OS PINMUX GIO ESM SCI1 SCI2 SCI3 SC

General Driver Enable R5-MPU-PMU Interrupts VIM General VIM RAM VIM Channel 0-31

Enable Driver Compilation

Click and mark the required modules for driver compilation from below:

☐ Enable RTI driver

☒ **Enable GIO driver ****

☐ Enable SCI drivers

☐ Enable LIN drivers

☐ Enable MIBSPI drivers

☒ **Enable CAN drivers**

☒ **Enable CAN1 driver**

☐ Enable CAN2 driver

☐ Enable CAN3 driver

☐ Enable CAN4 driver **

Turn signal RTOS_Setting

TMS570LC4357ZWT_FREERTOS OS PINMUX GIO ESM SCI1 SCI2 SCI3

Port A Port B

Bit 0

DOUT: 0 DIR: PDR: PSL: GIOB[0]

DIN:

TMS570LC4357ZWT_FREERTOS OS PINMUX GIO ESM SCI1 SCI2 SCI3 SCI4 LIN1 LI

General Driver Enable R5-MPU-PMU Interrupts VIM General VIM RAM VIM Channel 0-31

Module	Pin	Signal	IRQ	FIQ
13 : LIN1 High	13			
14 : ADC1 Event	14			
15 : ADC1 Group 1	15			
16 : CAN1 High	16		IRQ	FIQ
17 : MIBSPI2 High	17			
18 : FlexRay High	18			
19 : CRC 1	19			
20 : ESM Low	20			
21 : SSI	21			
22 : PMU TAP	22			
23 : GIO Low	23			
24 : HET1 Low	24			
25 : HET TU1 Low	25			
26 : MIBSPI1 Low	26			
27 : LIN1 Low	27			
28 : ADC1 Group 2	28			
29 : CAN1 Low	29		IRQ	FIQ

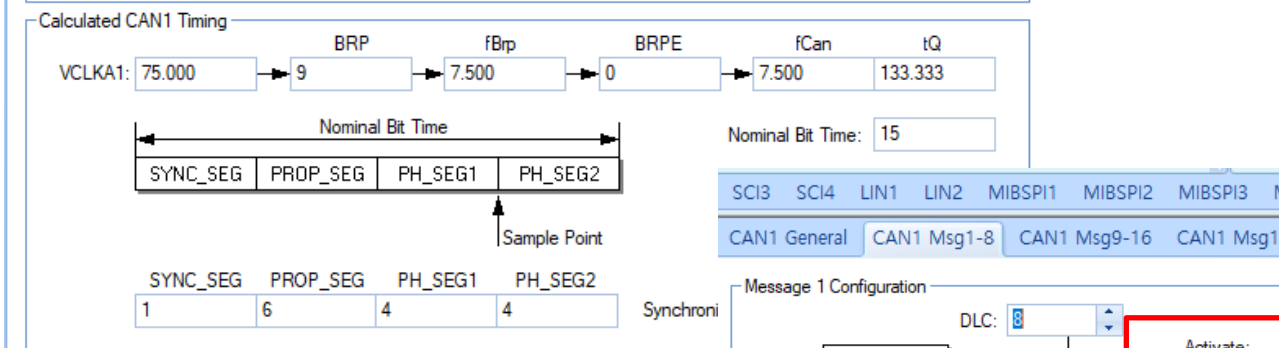
Turn signal RTOS_Setting



CAN1 Timing Configuration

Bit Rate: Propagation Delay:

SP Ref: Calculated Bit Rate:



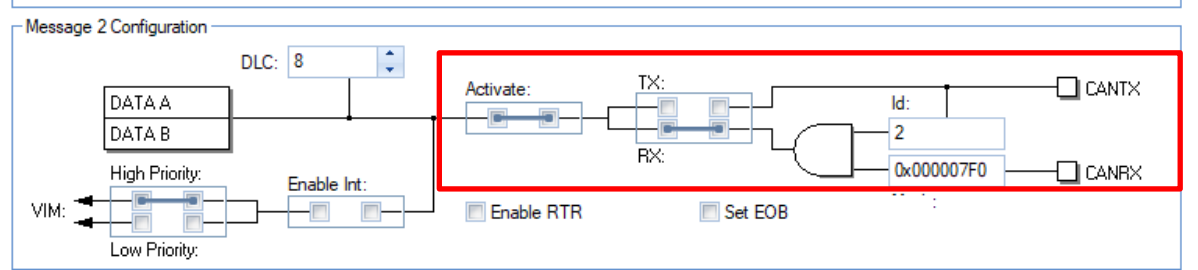
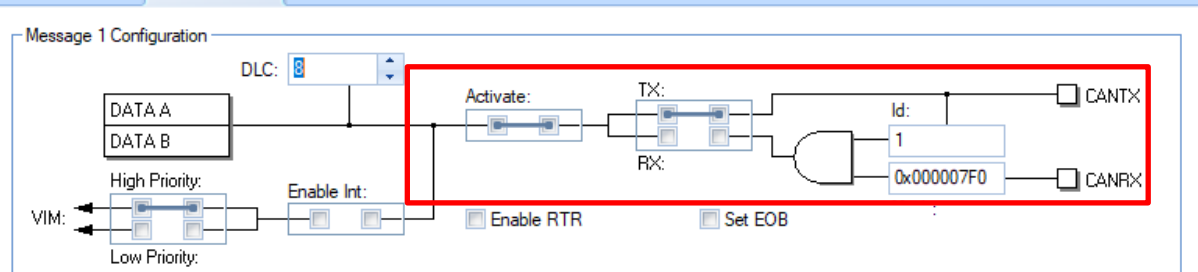
CAN1 Auto Bus On Configuration

☐ Enable Auto Bus On ABOTR: tAbo:

VCLK1: → ABO Counter → tAbo Nom

CAN1 General Configuration

☐ Disable Automatic Retransmission ☒ Enable Identifier Extension ☐ Enable R



```

#include <HL_can.h>
#include <HL_gio.h>
#include <HL_reg_can.h>
#include <HL_reg_gio.h>
#include <stdio.h>
#include <FreeRTOS.h>
#include <FreeRTOSConfig.h>
#include <HL_hal_stdtypes.h>
#include <os_mpu_wrappers.h>
#include <os_projdefs.h>
#include <os_semphr.h>
#include <os_task.h>
#include <string.h>

char num;
xTaskHandle xTask1Handle;
QueueHandle_t mutex;
void vTask1(void* pvParameters);

void delay(int num)
{
    int a;
    for (a = 0; a < num; a++)
        ;
}

int main()
{
    giolnit();
    canlnit();
    delay(10000);
    char num = 0;
    //vSemaphoreCreateBinary(mutex)
    if (xTaskCreate(vTask1, "Task1", configMINIMAL_STACK_SIZE*8, NULL,
1,&xTask1Handle) != pdTRUE)
    {
        while (1)
            ;
    }

    vTaskStartScheduler();
    while (1)
        ;
    return 0;
}

```

```

void vTask1(void *pbParameters)
{
    while (1)
    {
        canTransmit(canREG1, canMESSAGE_BOX1, &num);
        vTaskDelay(500);

        canIsRxMessageArrived(canREG1, canMESSAGE_BOX2);
        vTaskDelay(500);
        canGetData(canREG1, canMESSAGE_BOX2, &num);

        switch(num)
        {
            case 7:
                gioSetBit(gioPORTB, 0, 1);
                vTaskDelay(500);
                break;

            default:
                gioSetBit(gioPORTB, 0, 0);
                vTaskDelay(500);
                break;
        }
    }
}

```

Turn signal RTOS_CODE

Turn signal Circuit

Designer : 황수정 , 김민호

2018.08.12

Project AI CAR

