Xilinx Zynq FPGA, TI DSP, MCU 기반의 회로 설계 및 임베디드 전문가 과정

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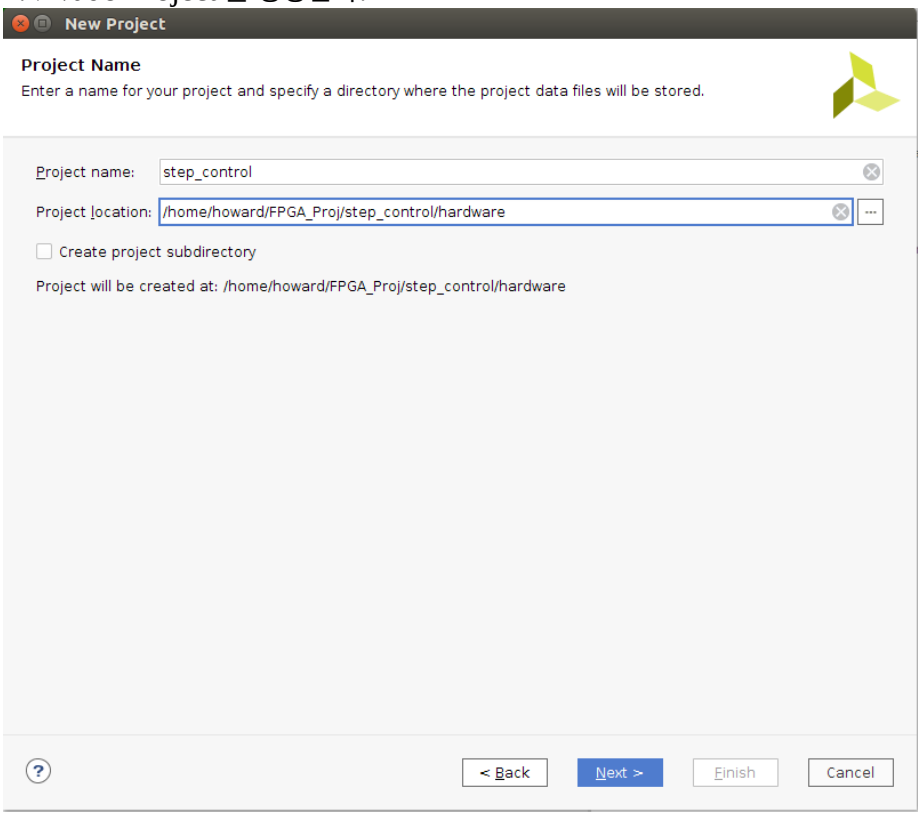
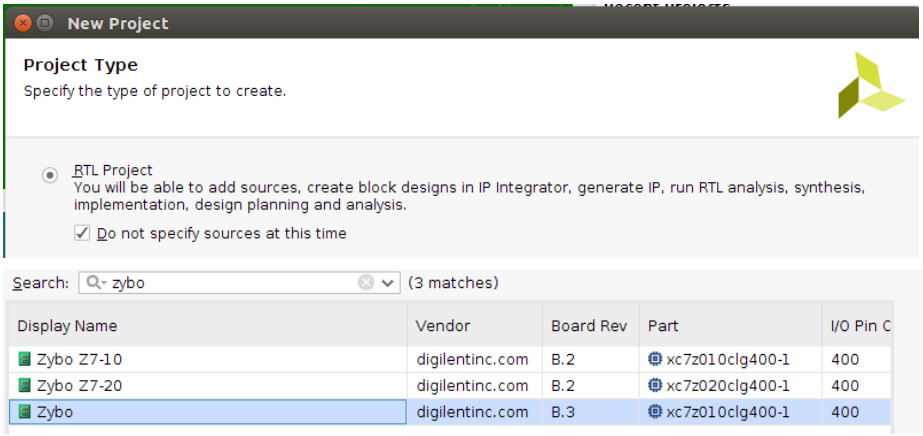
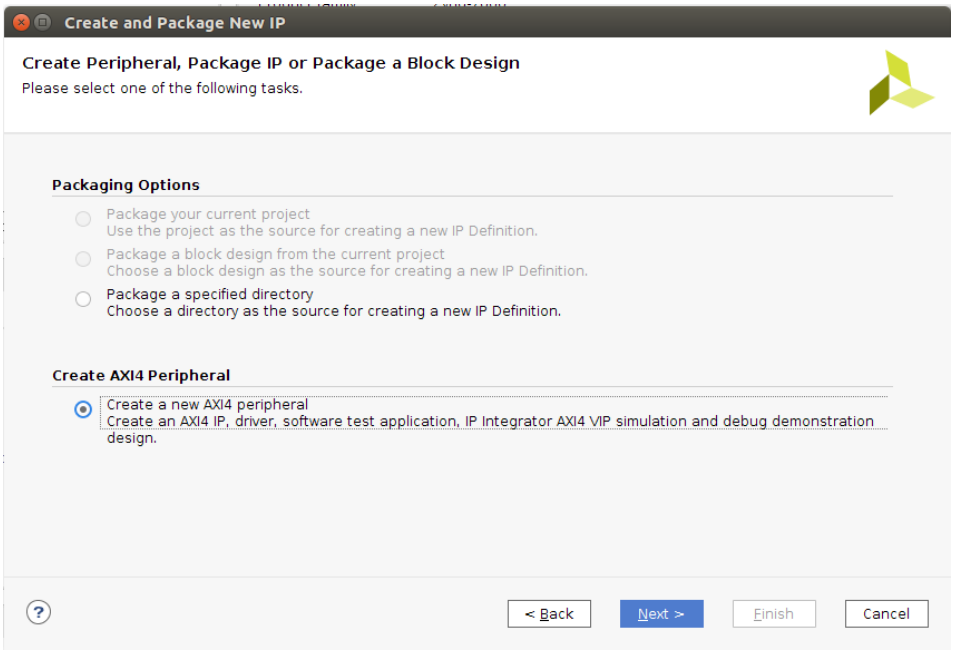
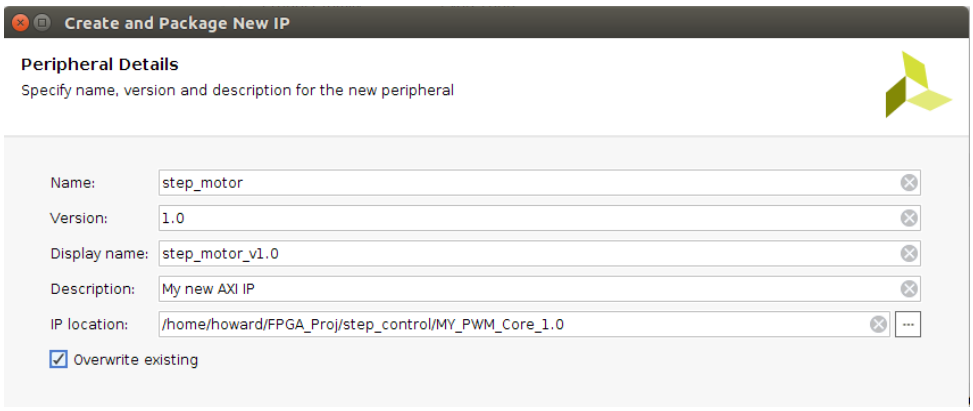
1.Vivado Project 를 생성한다.

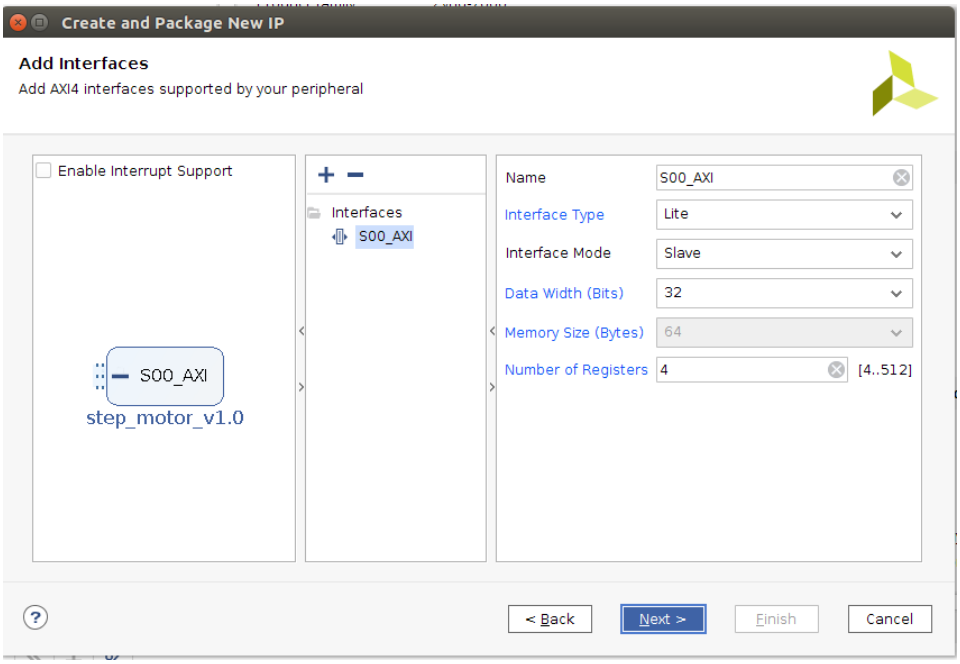




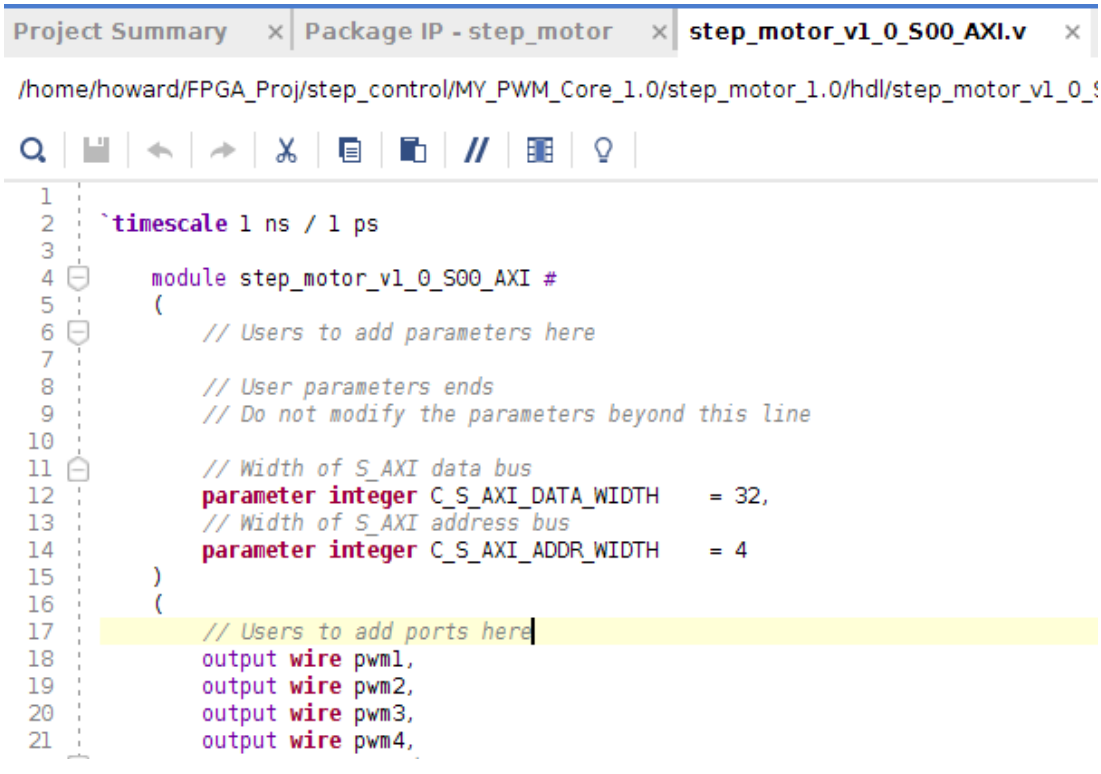
2. IP 를 설계한다. Tools → Create and Package New IP







3.하위 모듈에 출력 포트 4 개를 추가하고, pwm 로직을 설계한다.



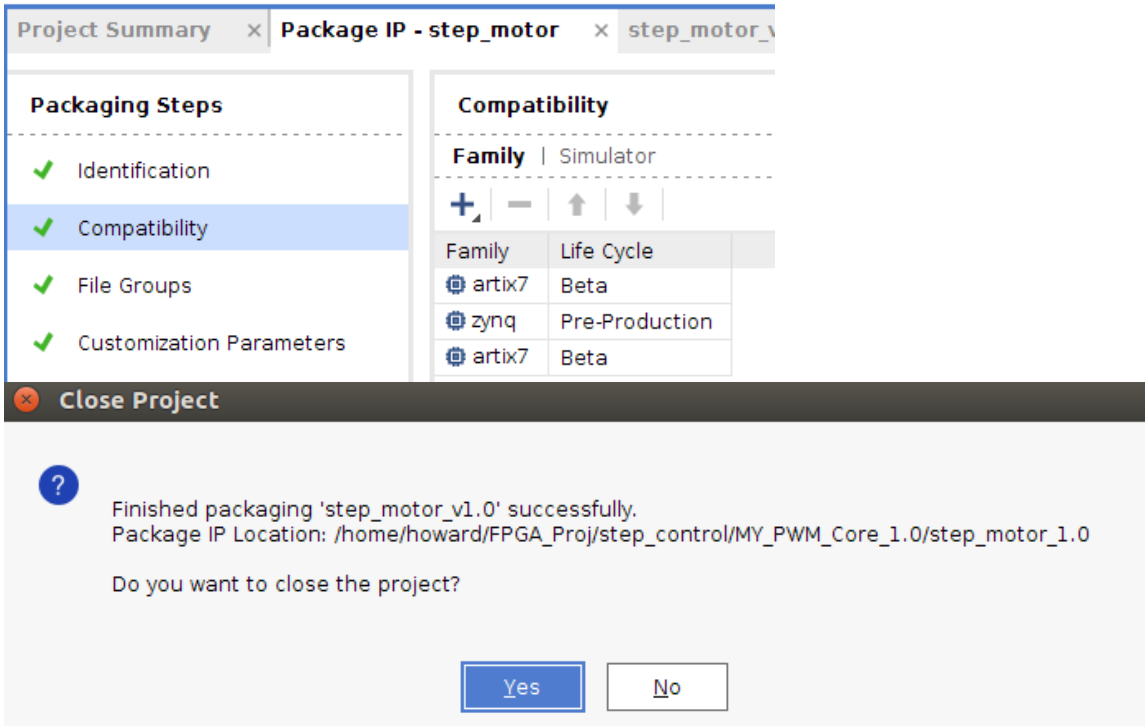
```
403     // Add user logic here
404     reg [31:0] counter;
405
406     always @( posedge S_AXI_ACLK)
407     begin
408        if(counter > slv_reg0 - 32'd1)
409            counter <= 32'd0;
410        else
411            counter <= counter + 32'd1;
412     end
413
414     assign pwm1 = counter > slv_reg0 / 5 && counter < slv_reg0 * 3 / 5 ? 1'b0 : 1'b1;
415     assign pwm2 = counter > slv_reg0 / 5 && counter < slv_reg0 * 3 / 5 ? 1'b1 : 1'b0;
416     assign pwm3 = counter > slv_reg0 * 2/ 5 && counter < slv_reg0 * 4 / 5 ? 1'b0 : 1'b1;
417     assign pwm4 = counter > slv_reg0 * 2/ 5 && counter < slv_reg0 * 4 / 5 ? 1'b1 : 1'b0;
418     // User logic ends
419
420     endmodule
421
```

4.상위 모듈에 출력 포트 4 개를 추가하고, 하위 모듈과 연결한다.

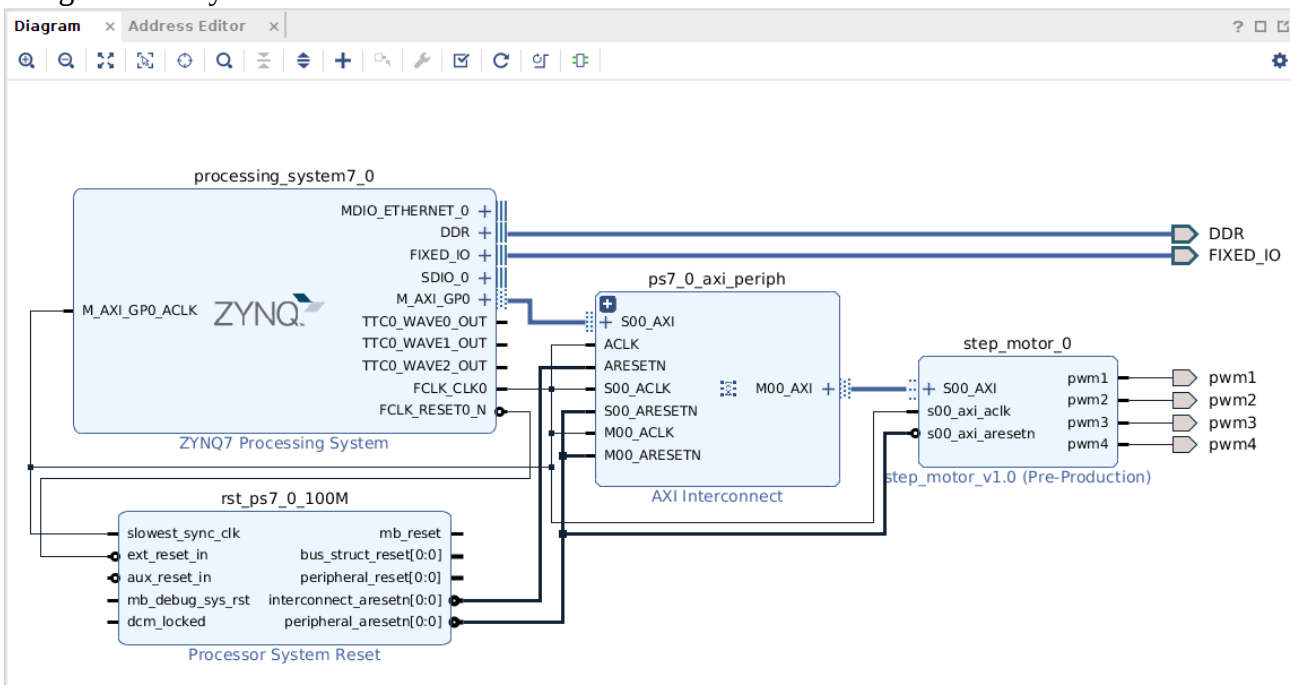
```
17          // Users to add ports here
18          output wire pwm1,
19          output wire pwm2,
20          output wire pwm3,
21          output wire pwm4,
22          // User ports ends
23          // Do not modify the ports beyond this line
```

```
49  // Instantiation of Axi Bus Interface S00_AXI
50      step_motor_v1_0_S00_AXI # (
51          .C_S_AXI_DATA_WIDTH(C_S00_AXI_DATA_WIDTH),
52          .C_S_AXI_ADDR_WIDTH(C_S00_AXI_ADDR_WIDTH)
53      ) step_motor_v1_0_S00_AXI_inst (
54          .pwm1(pwm1),
55          .pwm2(pwm2),
56          .pwm3(pwm3),
57          .pwm4(pwm4),
58          .S_AXI_ACLK(s00_axi_aclk),
```

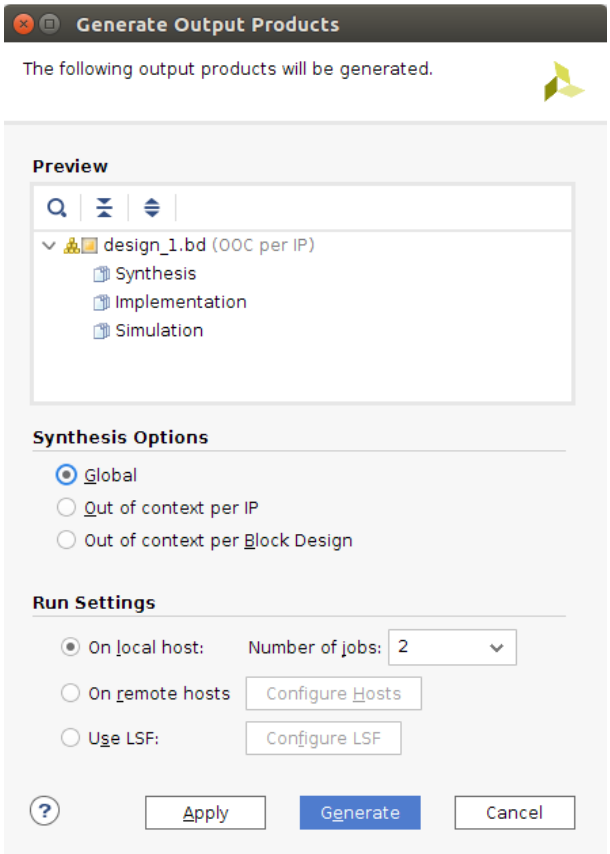
5.Package IP 에서 호환성 부분에 artix7 을 추가하고, ip 를 생성한다.



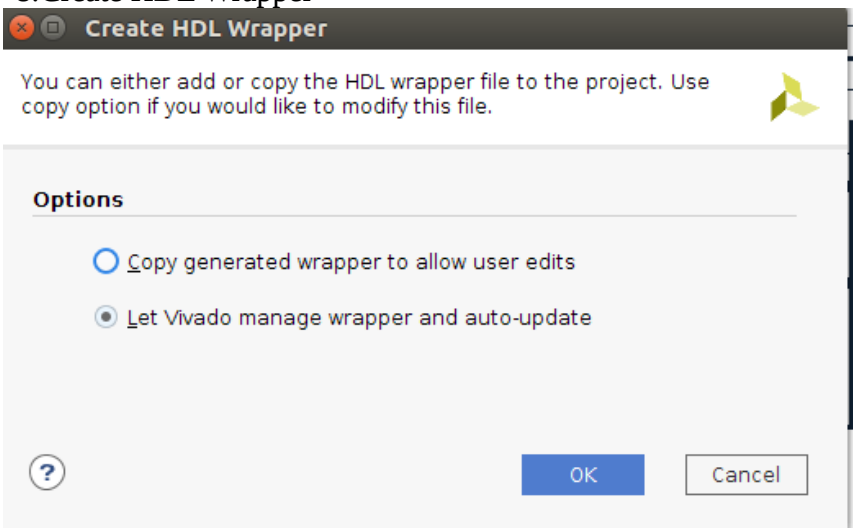
6.블록 다이어그램을 만들어 아래와 같이 구성한다.
- zynq 보드 추가
- 더블클릭 후 USB0 제거
- step_motor IP 추가
- 각 포트에 create port
- Run connection Automation
- Validate design
- Regenerate Layout



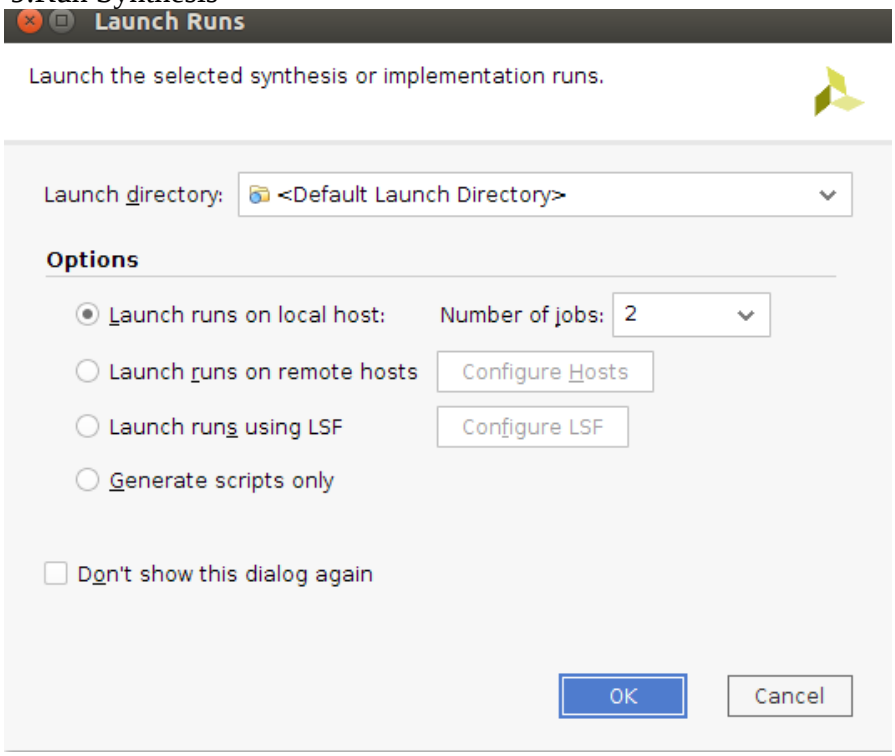
7.Generate Output Products



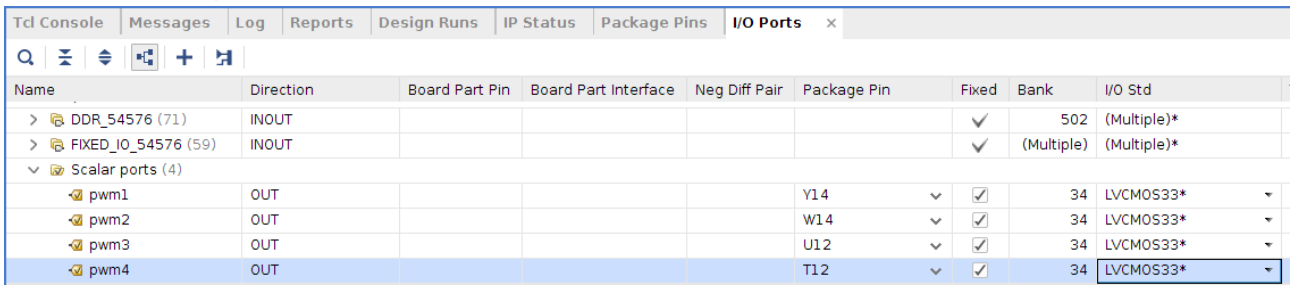
8.Create HDL Wrapper



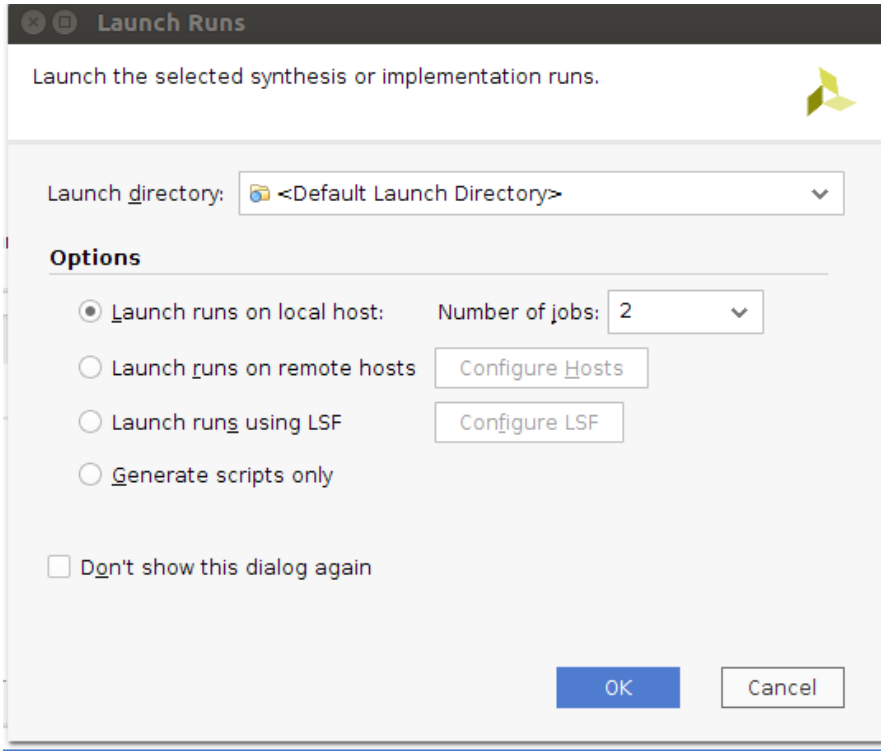
9.Run Synthesis



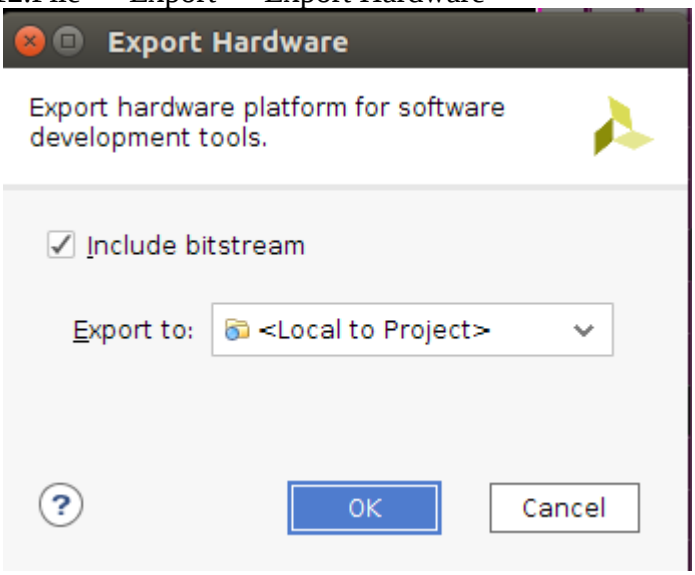
10. I/O Ports 설정



11.Generate Bitstream

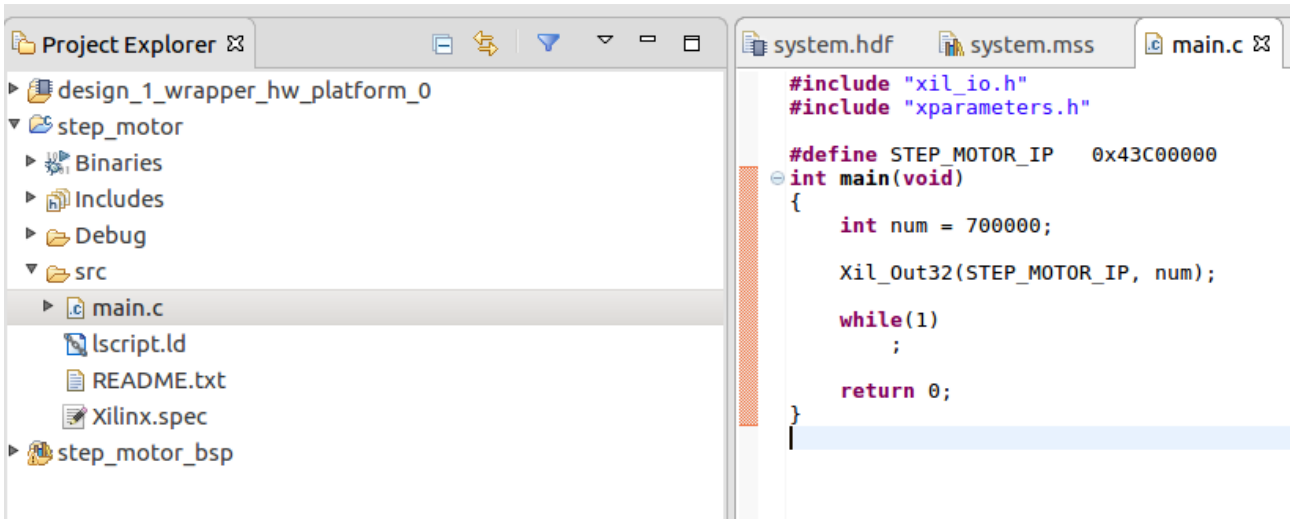


12.File → Export → Export Hardware

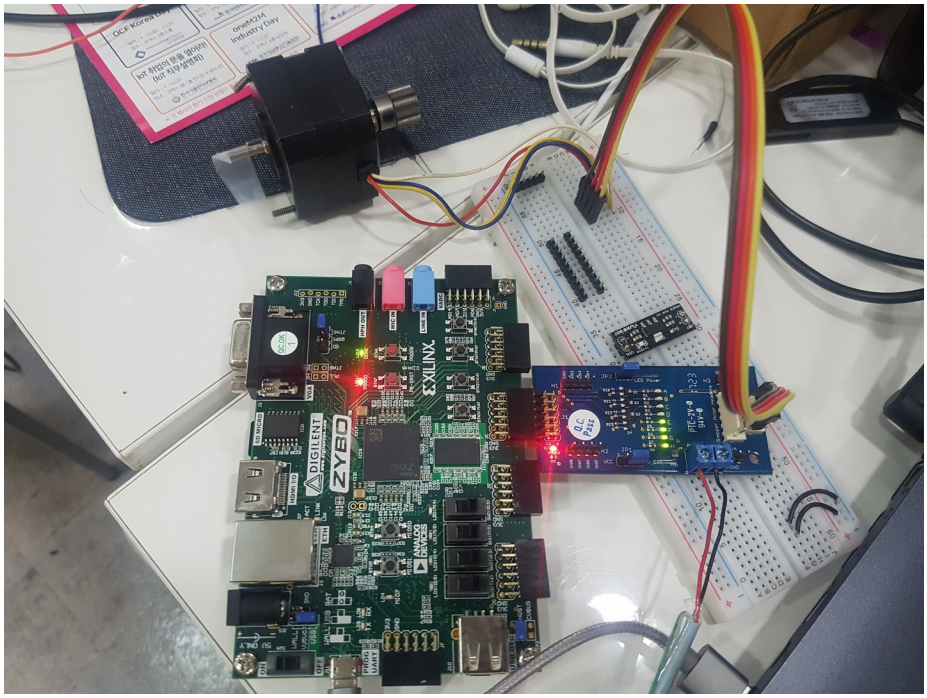


13.File → Launch SDK

14.main.c 에 아래와 같이 작성한다.



15.Program FPGA 후 Run as → Launch On Hardware(GDB)
16.결선은 아래와 같이 한다.
JC 에 연결하고, 스텝모터는 위쪽 순서대로 A 상,A-상,B 상,B-상이다.
외부 전원은 왼쪽이 +, 오른쪽이 -.



사용 모터 : 4017-875
스텝모터 드라이버 : Pmod Stepmotor driver
외부전원 : 5V1A(노트북 USB)