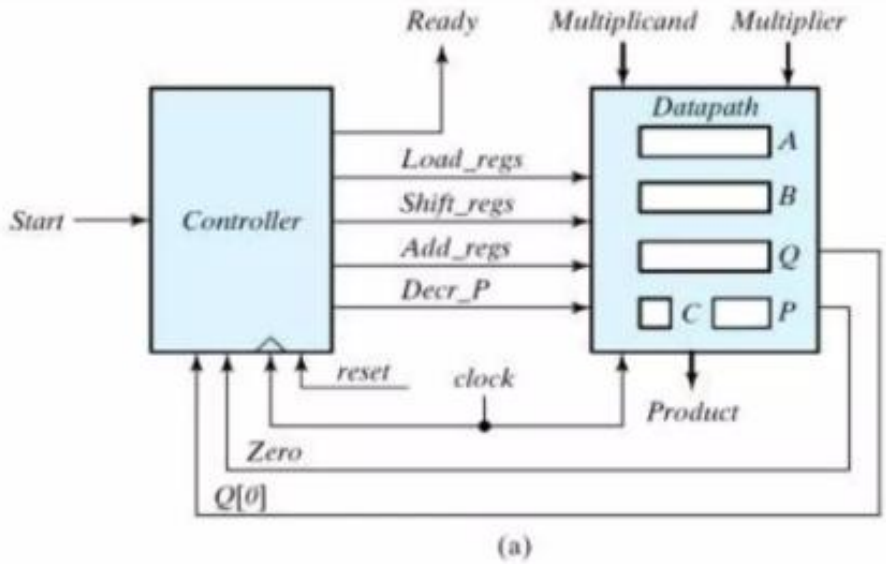
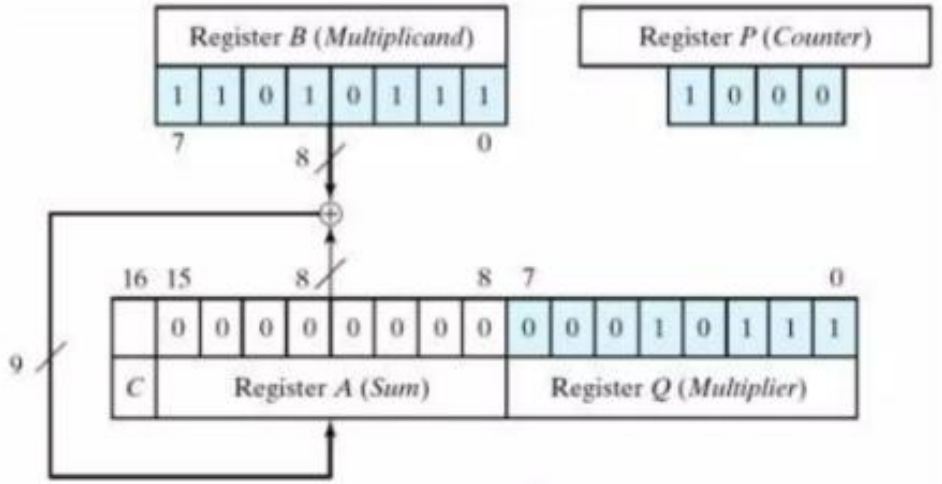
Binary Multiplier

Block diagram:



(a)

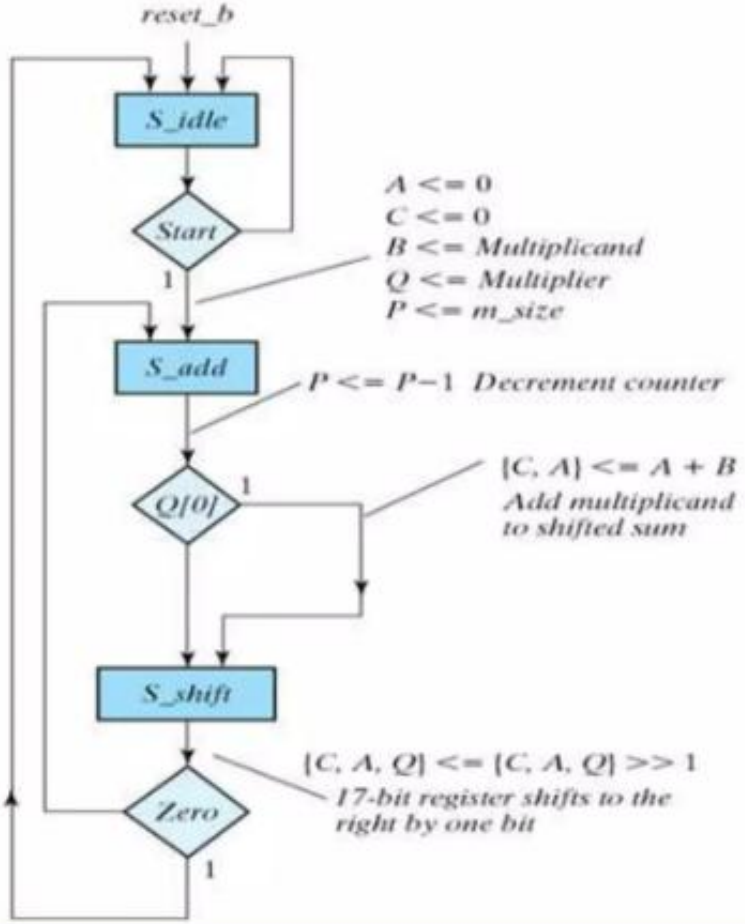
Datapath:



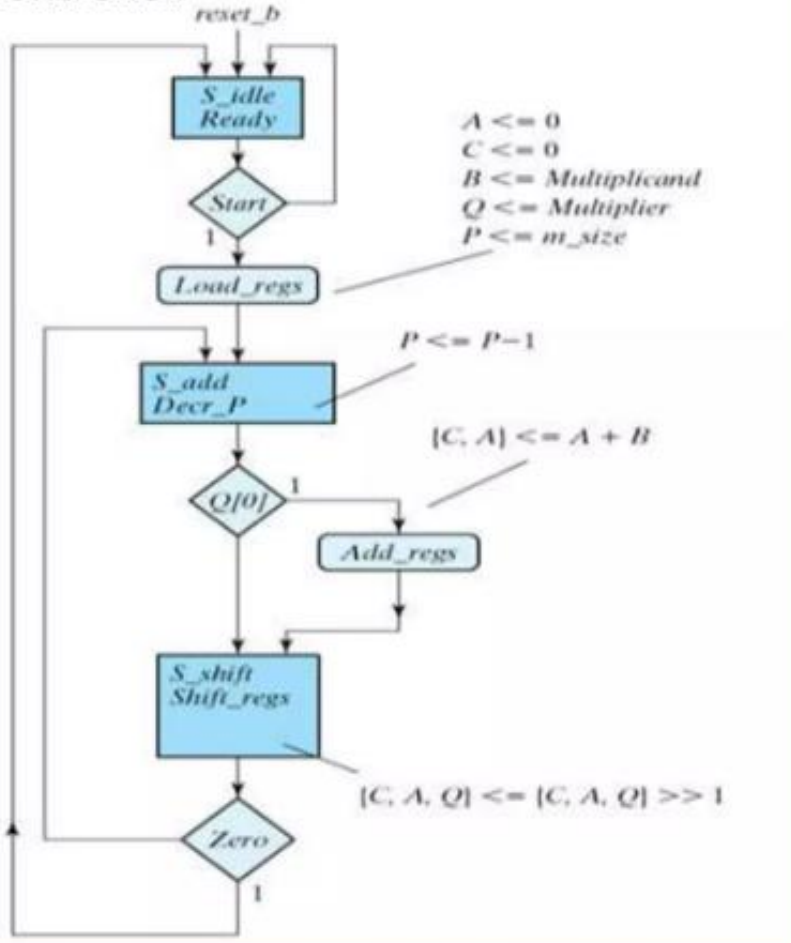
(b)

ASMD Chart for Binary Multiplier

The intermediate form annotates the ASM chart of the controller with the register operations.



The completed chart identifies the Moore and Mealy outputs of the controller.



Example

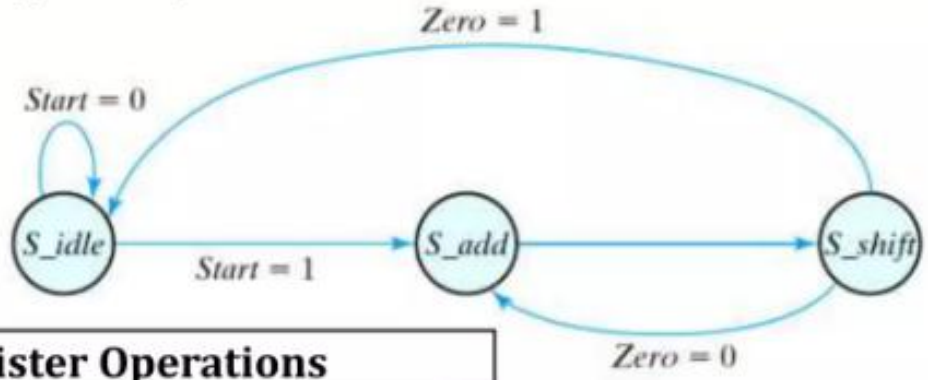
Multipicand $B = 10111_2 = 17_H = 23_{10}$	Multiplier $Q = 10011_2 = 13_H = 19_{10}$			
	C	A	Q	P
Multiplier in Q	0	00000	10011	101
$Q_0 = 1$; add B		10111		
First partial product	0	10111		100
Shift right CAQ	0	01011	11001	
$Q_0 = 1$; add B		10111		
Second partial product	1	00010		011
Shift right CAQ	0	10001	01100	
$Q_0 = 0$; shift right CAQ	0	01000	10110	010
$Q_0 = 0$; shift right CAQ	0	00100	01011	001
$Q_0 = 1$; add B		10111		
Fifth partial product	0	11011		
Shift right CAQ	0	01101	10101	000
Final product in $AQ = 0110110101_2 = 1b5_H$				

Control Logic

- Design of digital system
  - Register transfer in the datapath unit
  - Control logic of the control unit
- Must execute two steps when implementing the control logic:

(1) establish the required sequence of states, and

(2) provide signals to control the register operations.



State Transition		Register Operations
From	**To**	(a)
S_idle		Initial state
S_idle	*S_add*	$A <= 0, C <= 0, P <= dp\_width$
S_add	*S_shift*	$P <= P-1$
		if $(Q[0])$ then $(A <= A+B, C <= C_{out})$
S_shift		shift right $[CAQ]$, $C <= 0$

Sequence Register and Decoder

•Uses a register for the control states and a decoder to provide an output corresponding to each of the states.

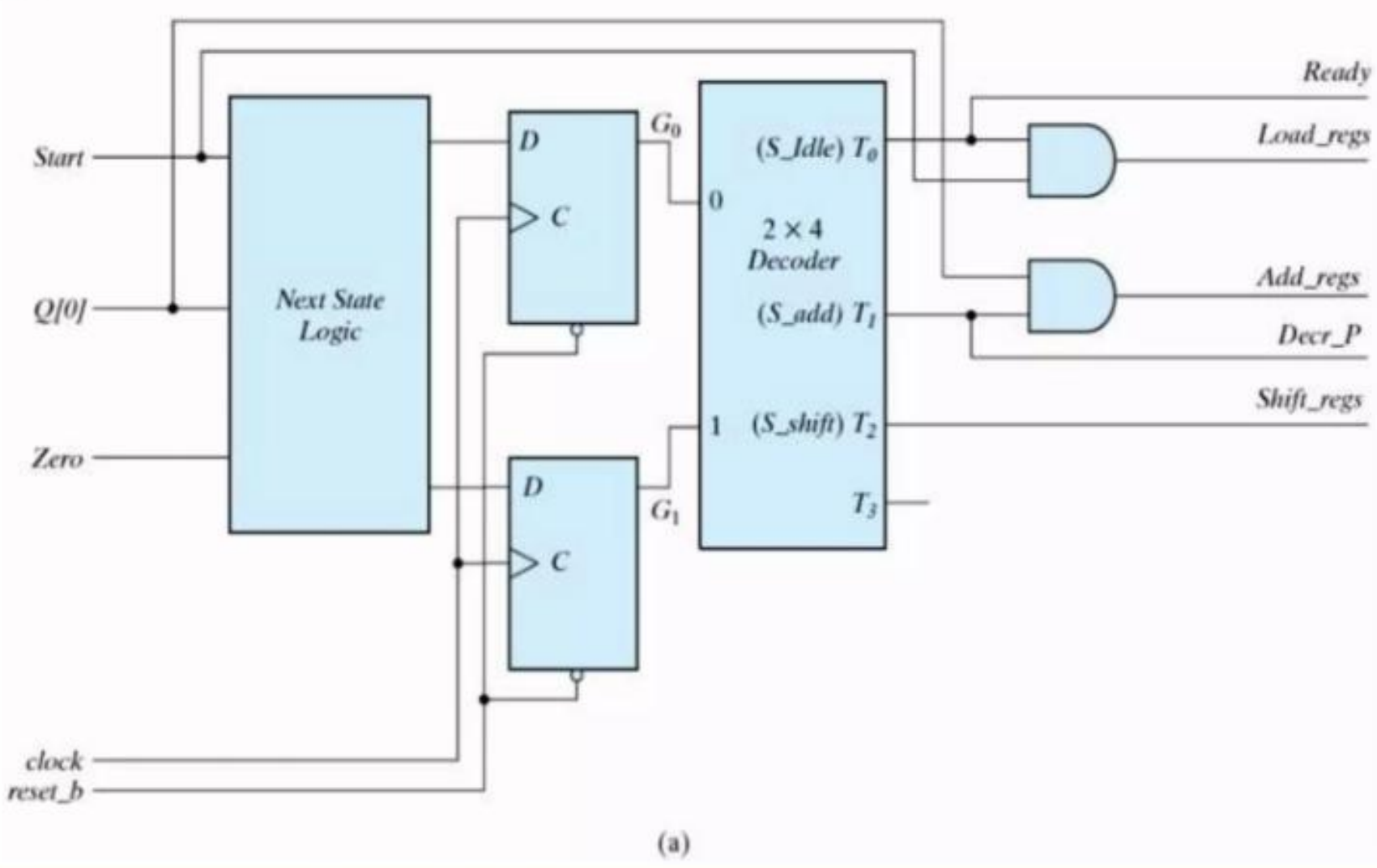
•A register with n flip- flops can have up to 2^n states, and an n -to- 2^n -line decoder has up to 2^n outputs.

•An n -bit sequence register is essentially a circuit with n flip-flops, together with the associated gates that effect their state transitions.

Present-State Symbol	Present State		Inputs			Next State		Ready	Load_regs	Decr_P	Add_regs	Shift_regs
	G_1	G_0	Start	Q[0]	Zero	G_1	G_0					
S_idle	0	0	0	X	X	0	0	1	0	0	0	0
S_idle	0	0	1	X	X	0	1	1	1	0	0	0
S_add	0	1	X	0	X	1	0	0	0	1	0	0
S_add	0	1	X	1	X	1	0	0	0	1	1	0
S_shift	1	0	X	X	0	0	1	0	0	0	0	1
S_shift	1	0	X	X	1	0	0	0	0	0	0	1

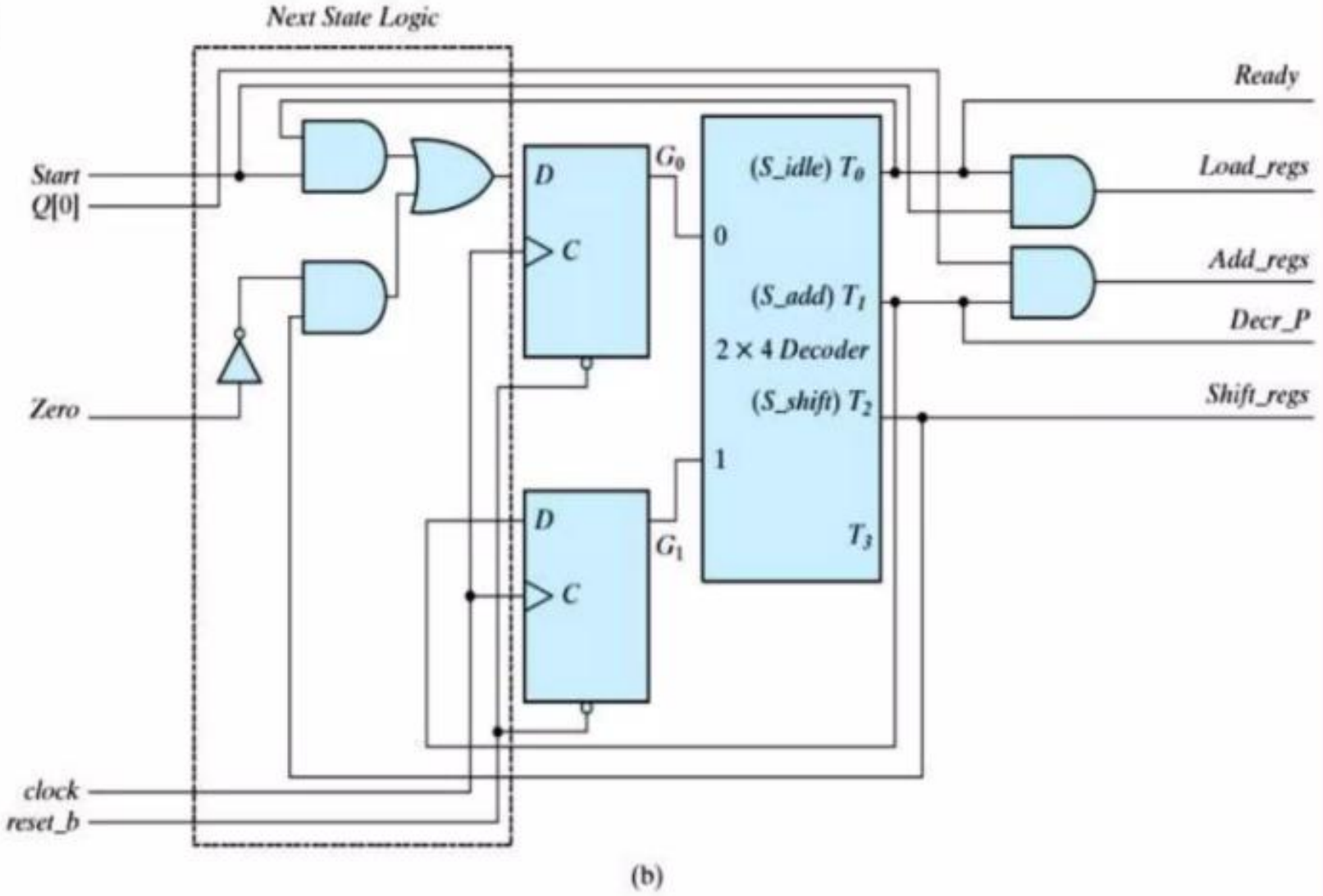
Logic Diagram

Logic diagram of control for binary multiplier using a sequence register and decoder



(a)

- $D_{G1} = G_0 Start + G_2 Zero'$
- $D_{G2} = G_1$



(b)