Z7-Nano Block Diagram

REV	DATE	PAGES	DESCRIPTION
1.0	13/03/2021	All	Rev 1.0 Release

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Title: Z7-Nano

Size: B | Document Number: Block Diagram | Rev: 2.0

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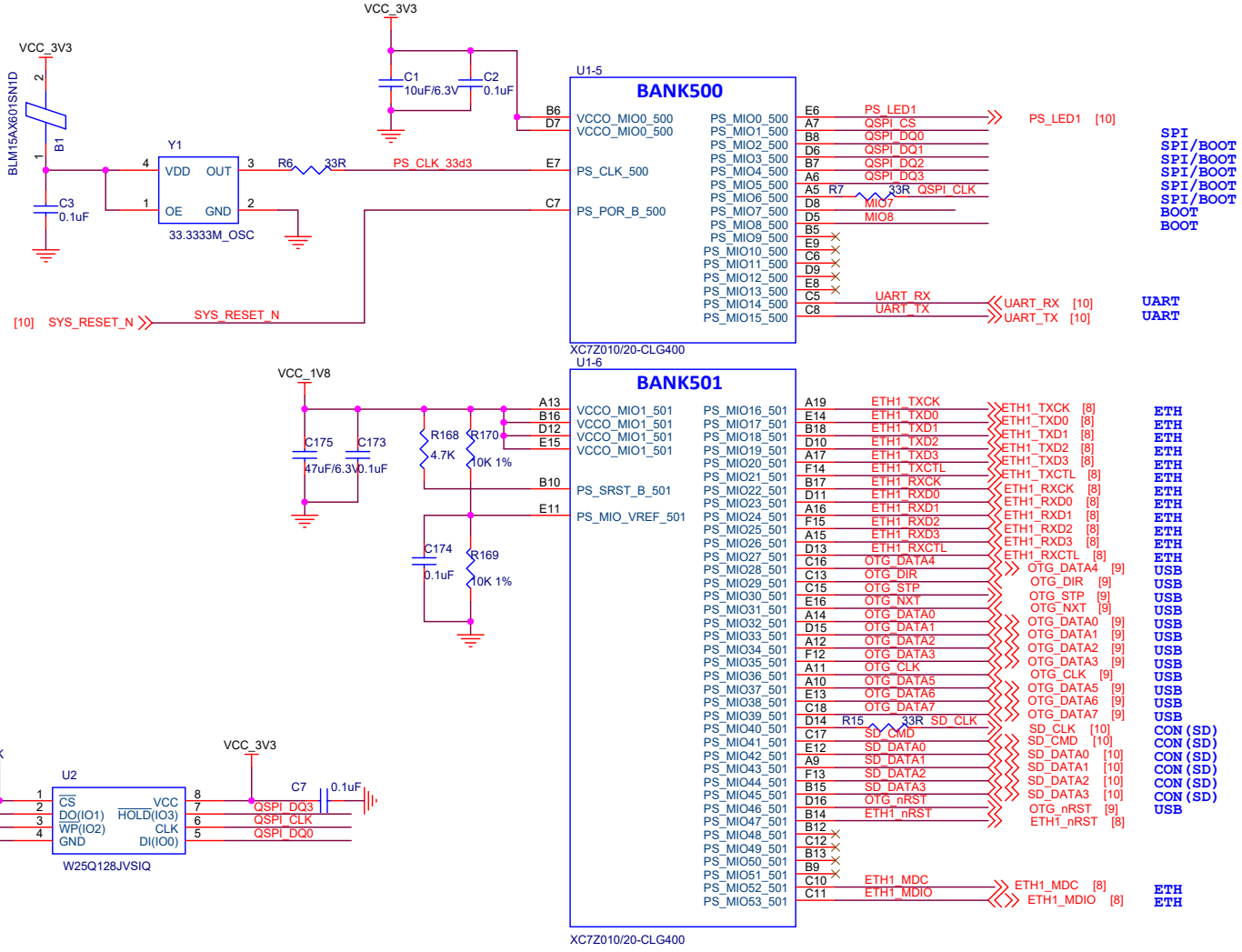
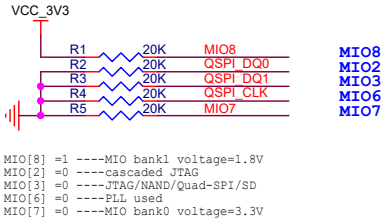
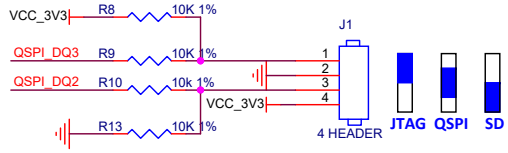
PS Bank 500 & 501







Boot Mode	MIO[5] (QSPI_DQ3)	MIO[4] (QSPI_DQ2)
JTAG	0	0
NAND	0	1
QSPI	1	0
SD Card	1	1

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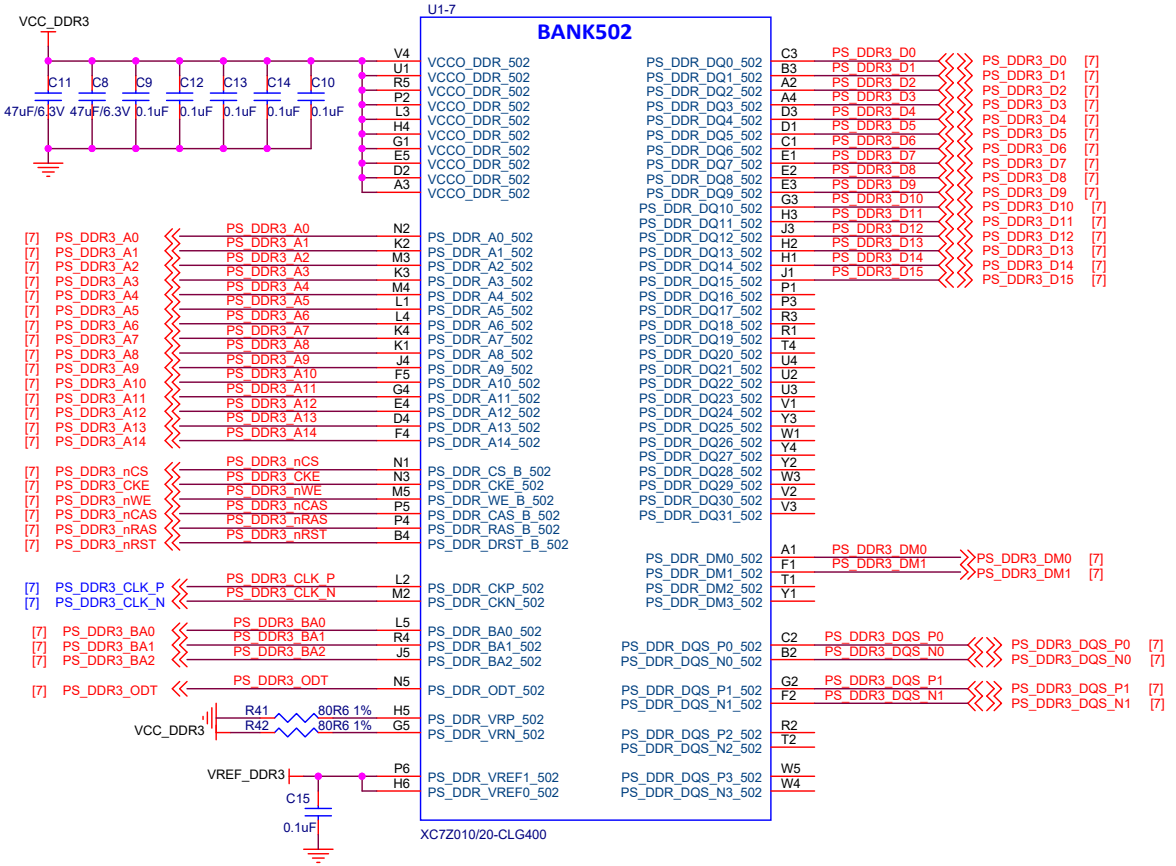
PS DDR Interface



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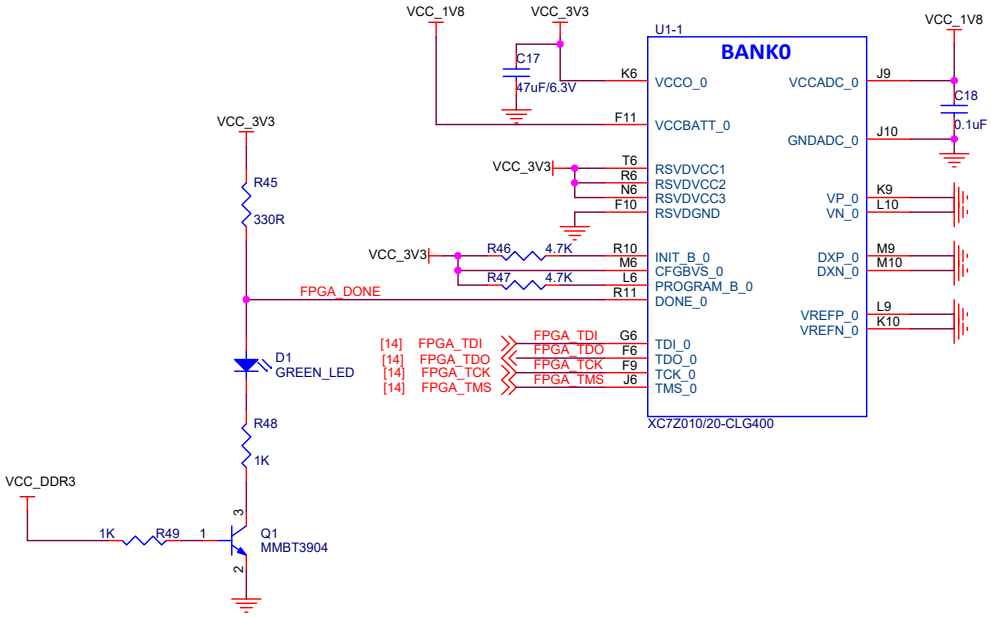
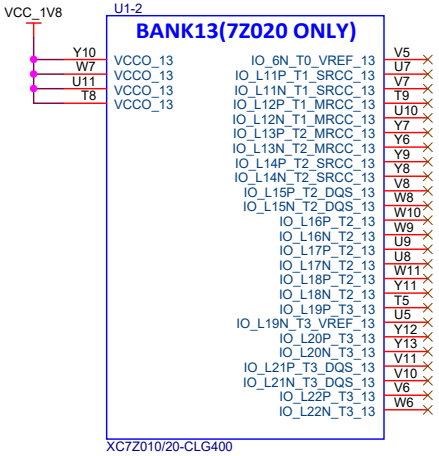
ZYNQ_CONFIG





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Title: Z7-Nano

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B	PL BANK0&13	2.0

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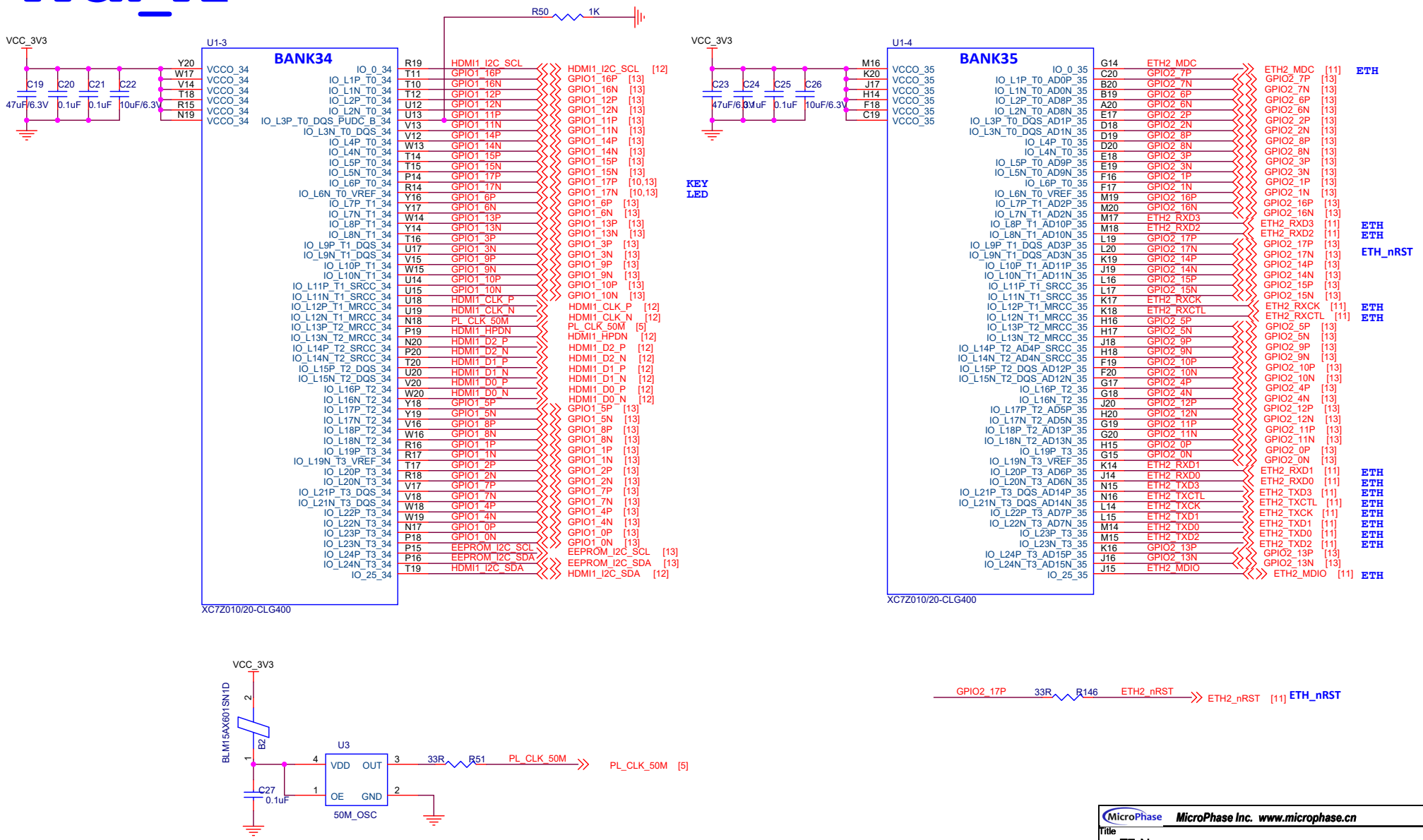
FPGA_PL



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Title	Z7-Nano	
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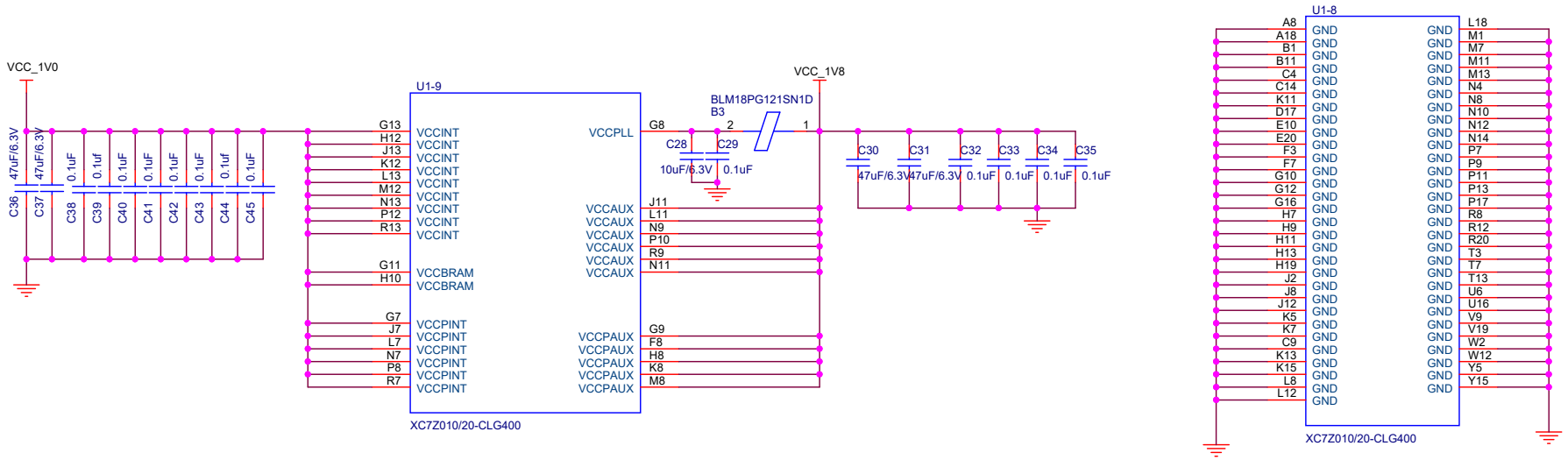
ZYNQ POWER



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Title: Z7-Nano		
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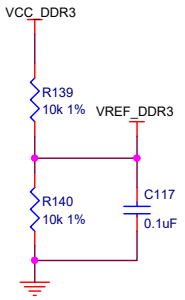
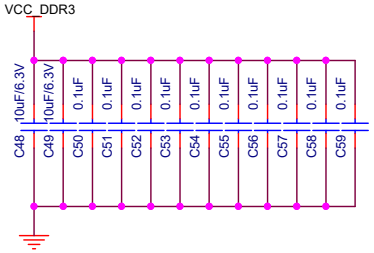
PS_DDR3





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B	DDR3 RAM	2.0

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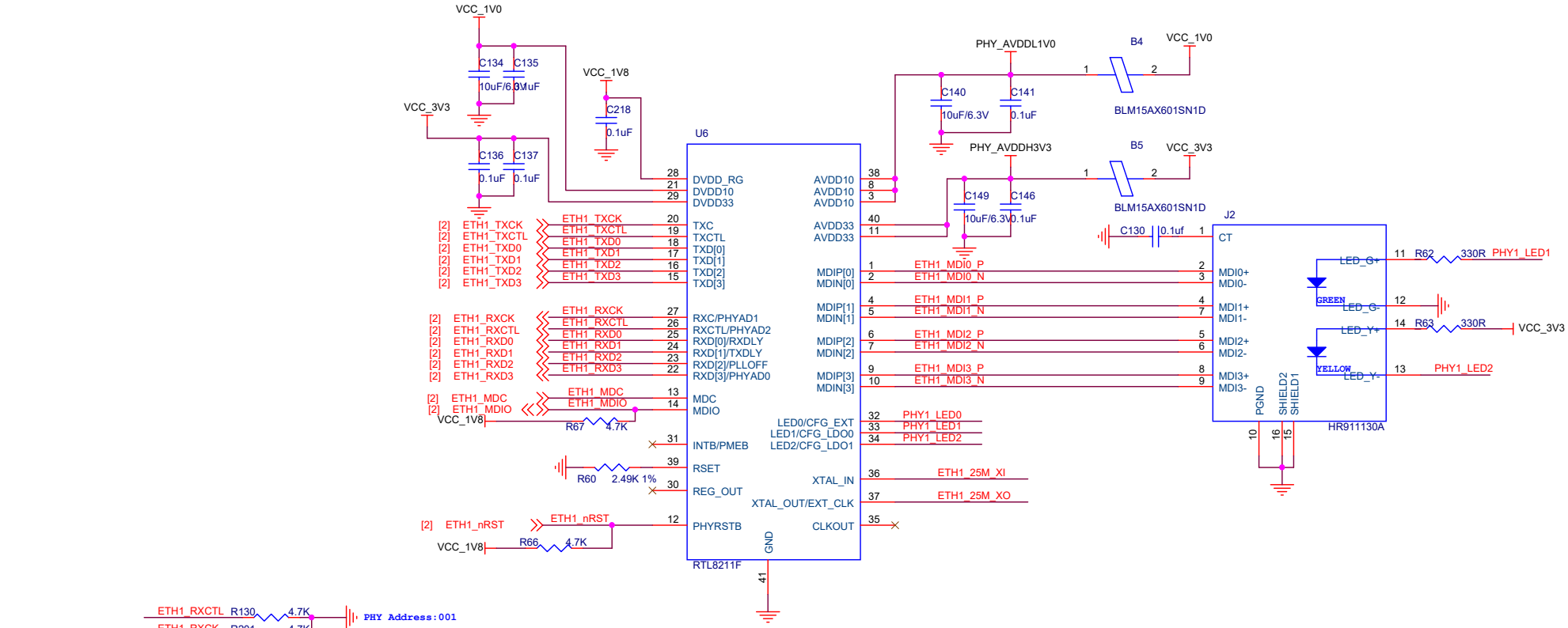
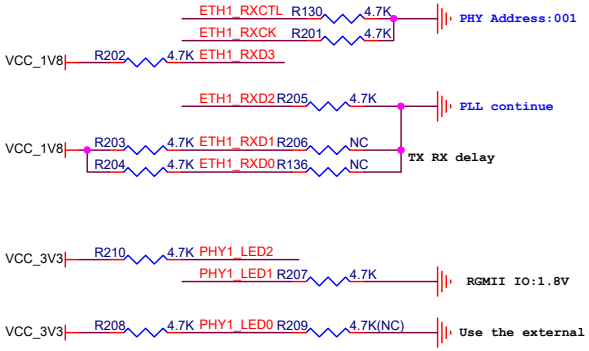
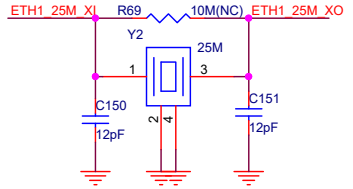
PS ETHERNET







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B	PS ETHERNET	2.0

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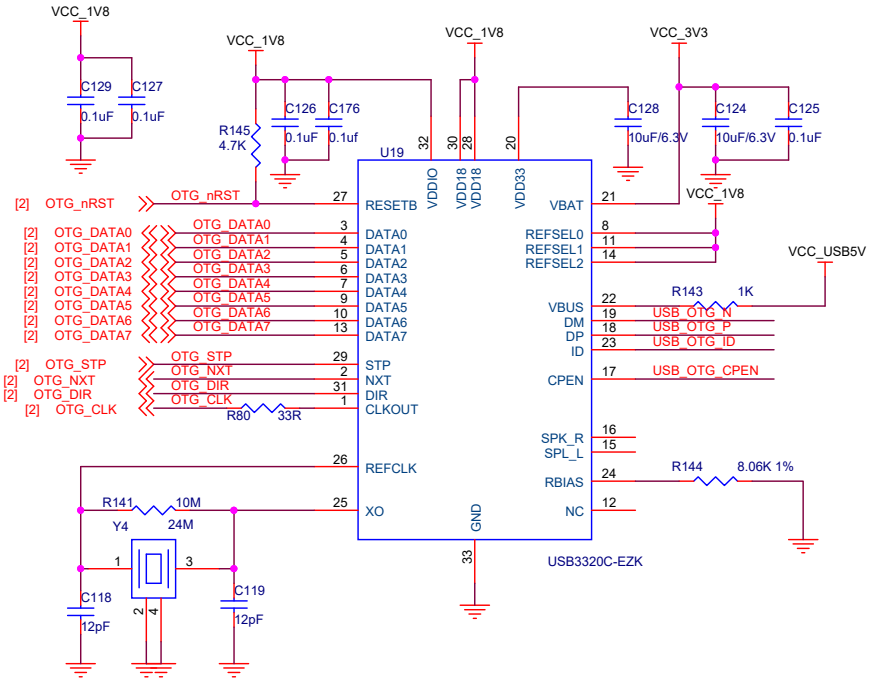
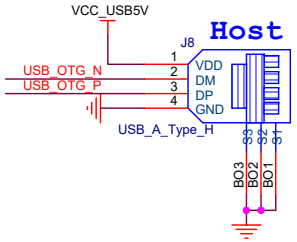
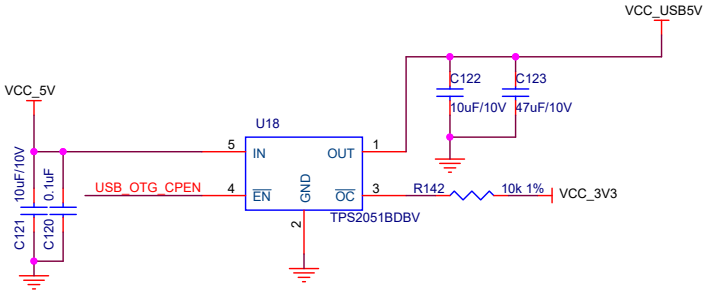
PS USB OTG







Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4 MHz
0	1	0	12 MHz
0	1	1	27 MHz
1	0	0	13 MHz
1	0	1	19.2 MHz
1	1	0	26 MHz
1	1	1	24 MHz

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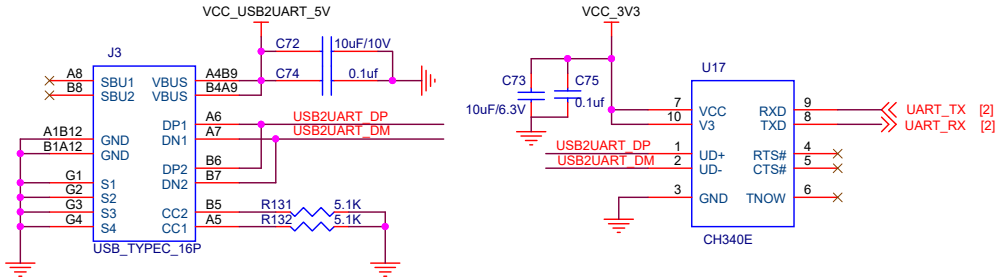
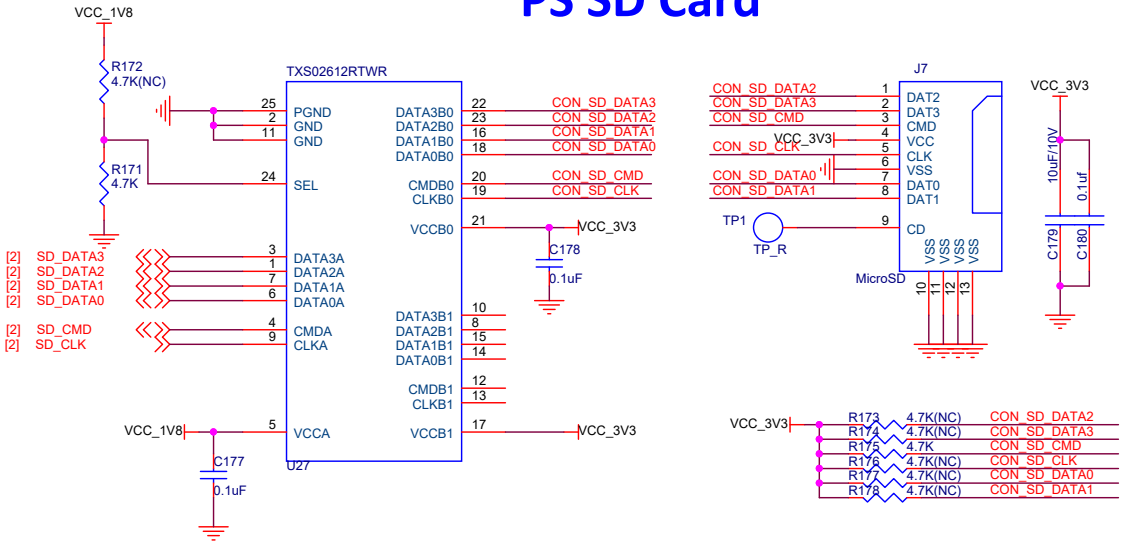
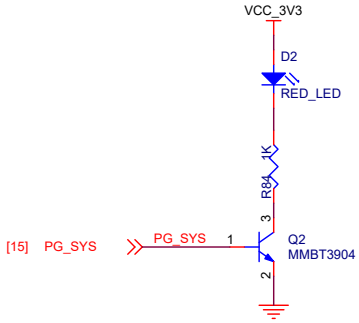
PS USB-UART

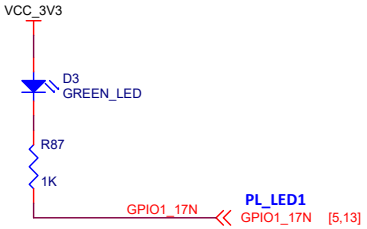


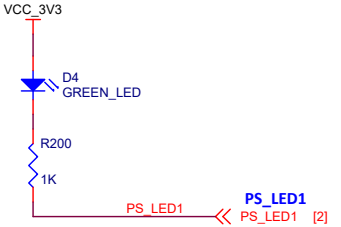
PS SD Card

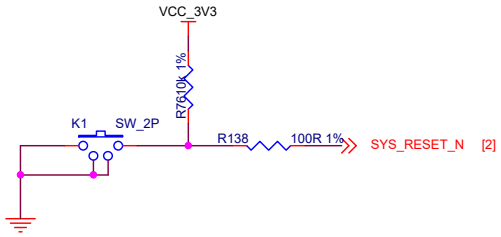


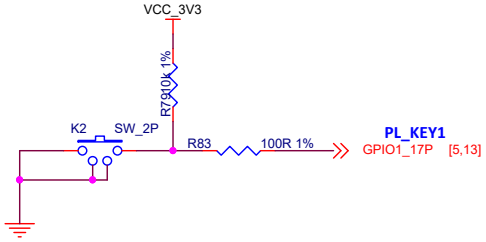
KEY & LED











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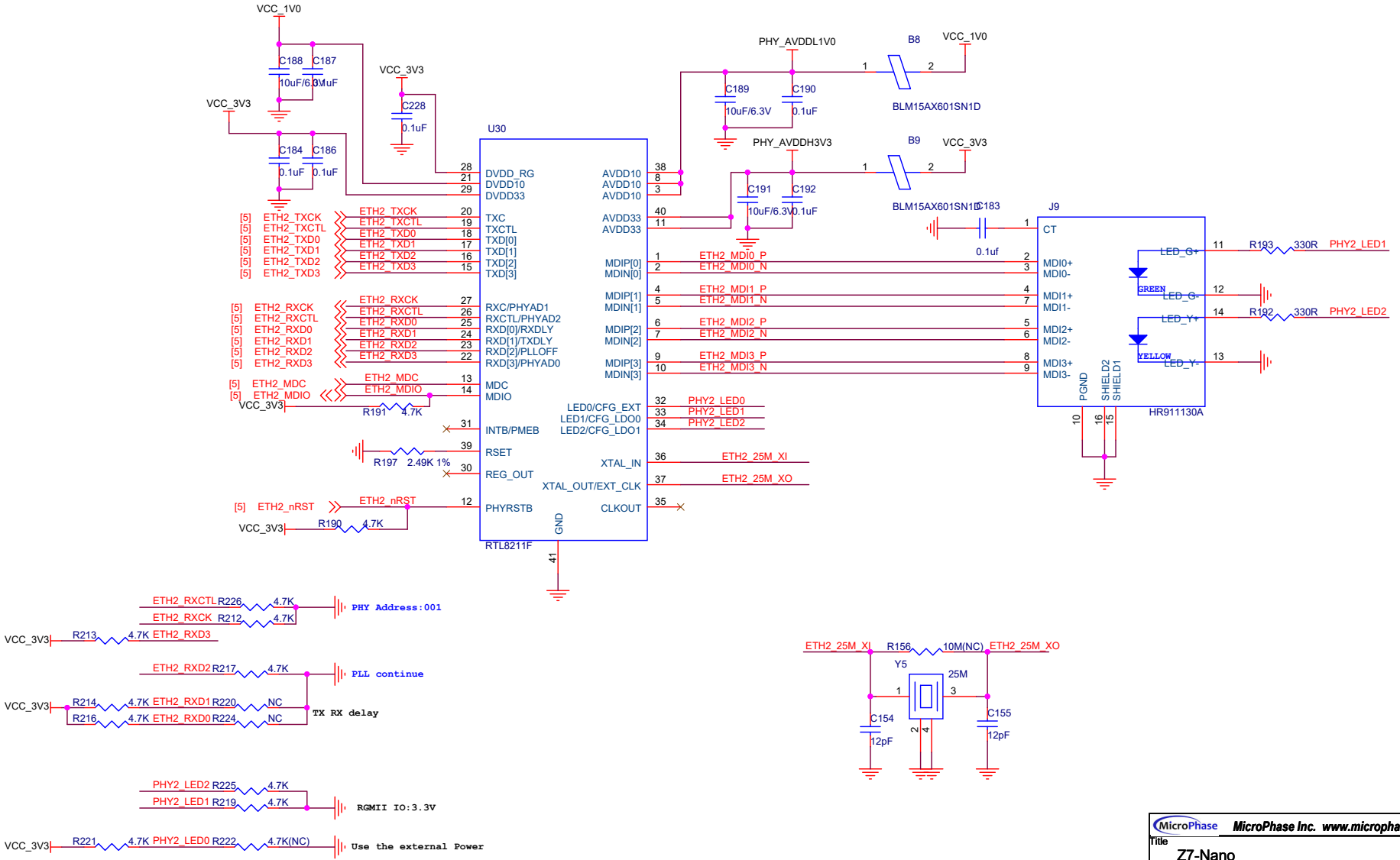
PL ETHERNET



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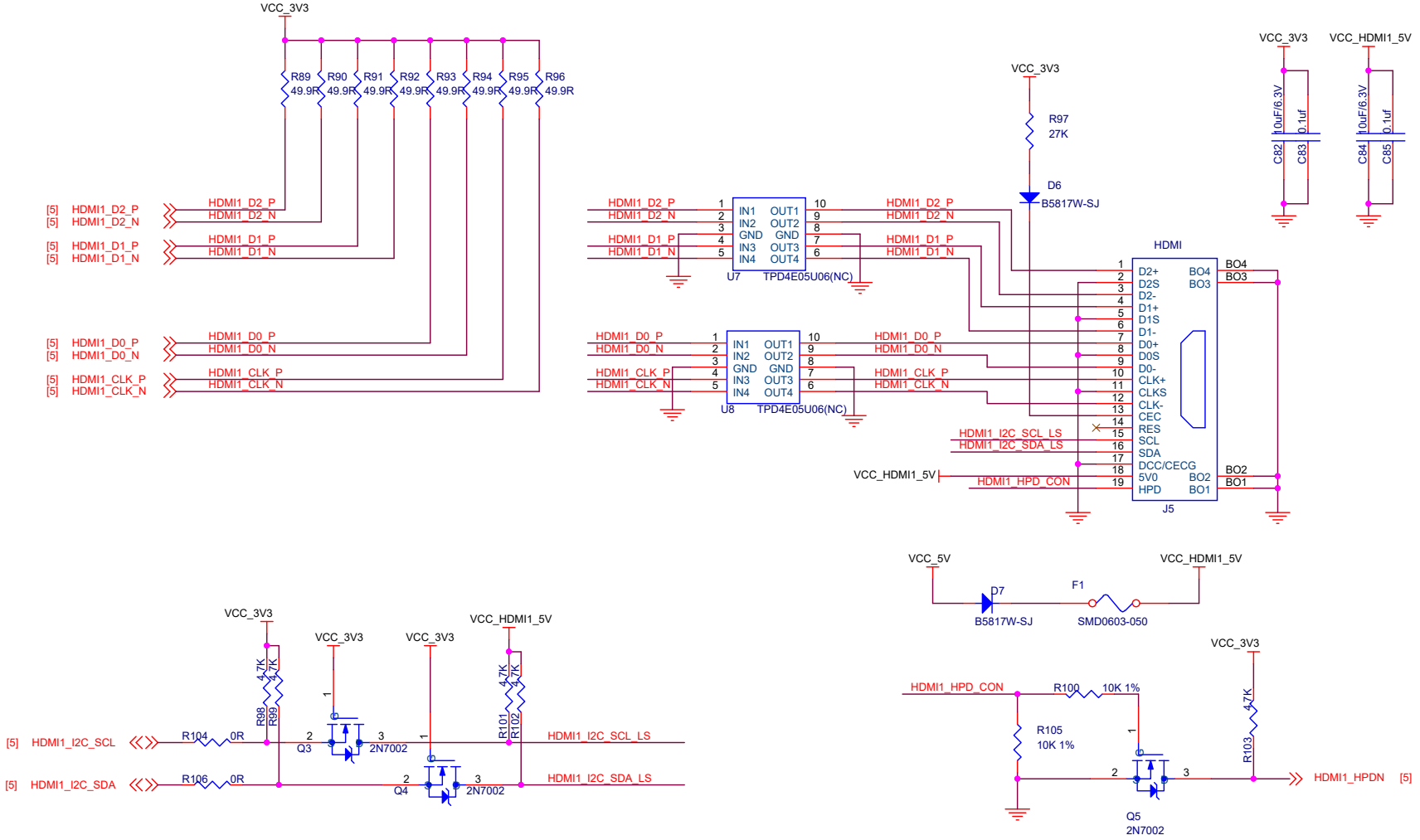
PL HDMI-TX



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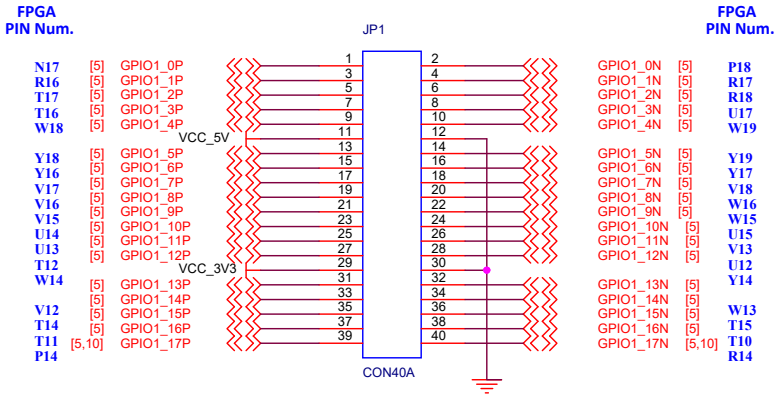
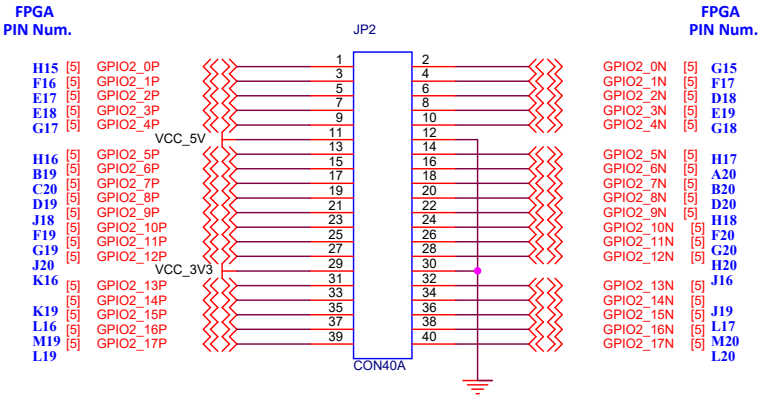
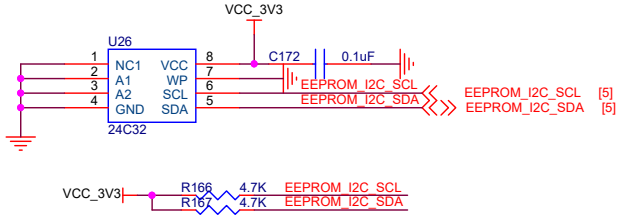
GPIO Interface





EEPROM



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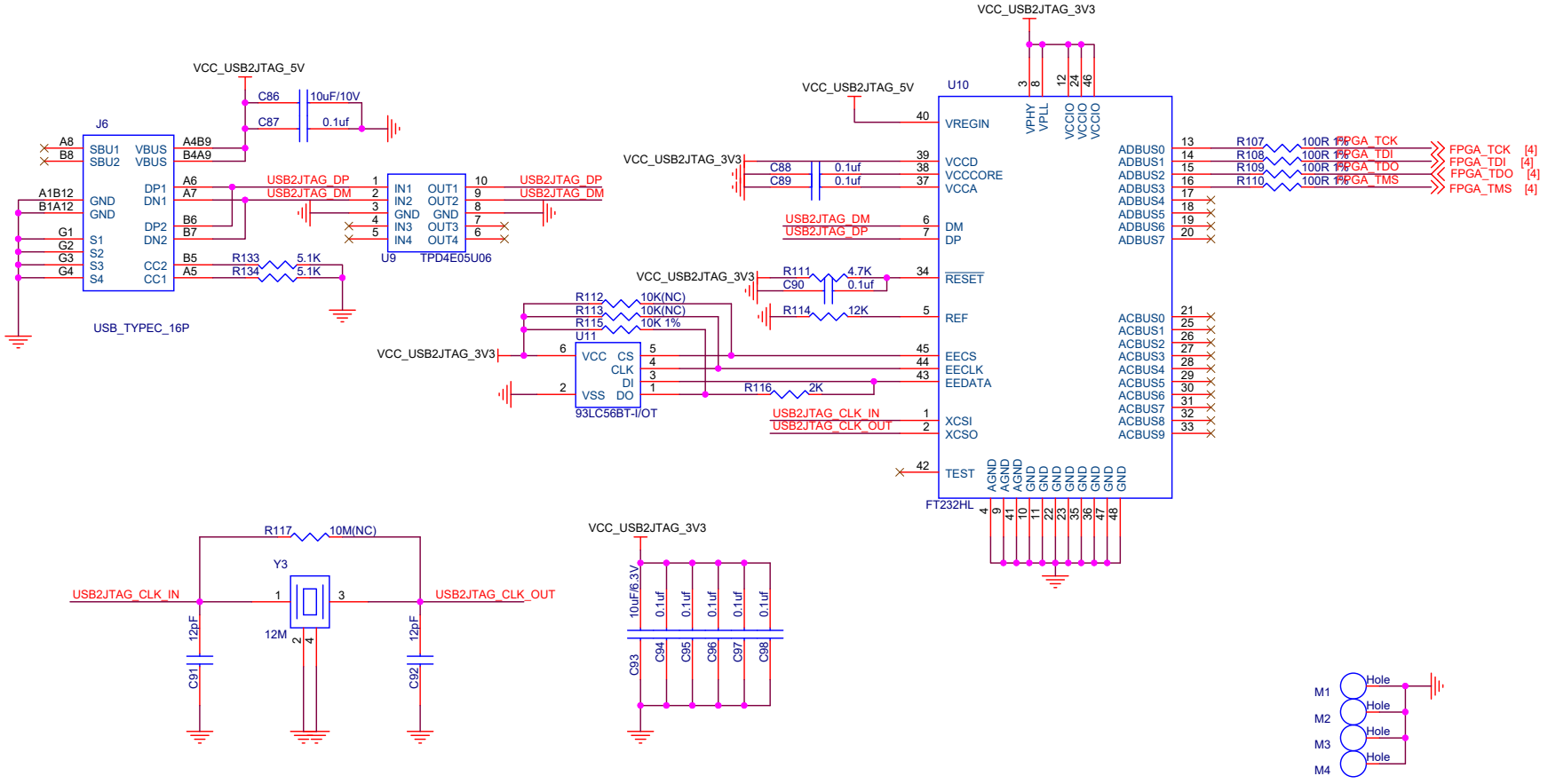
USB JTAG



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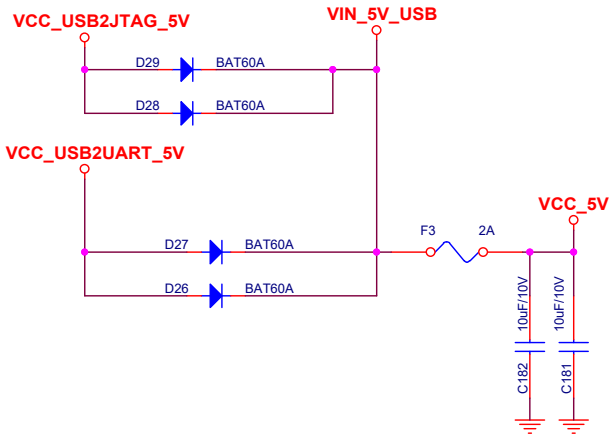
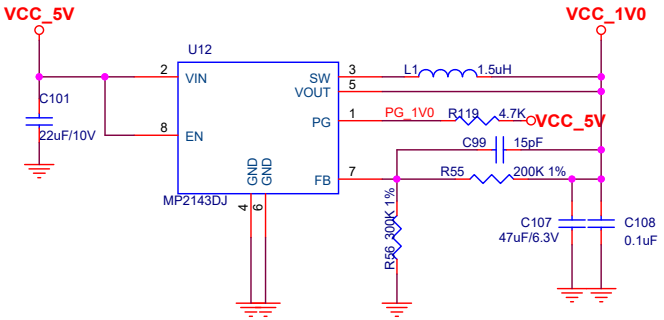
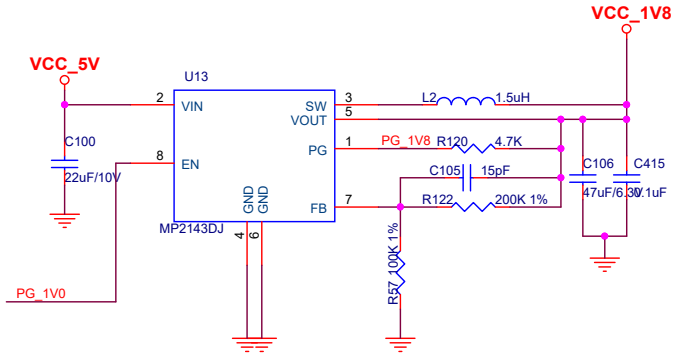
POWER

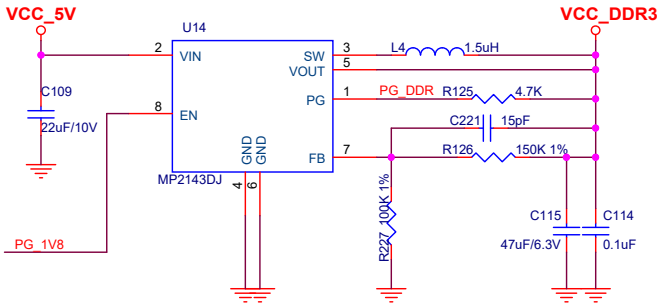




Vref = 0.6V VOUT = 1.0V



Vref = 0.6V VOUT = 1.8V



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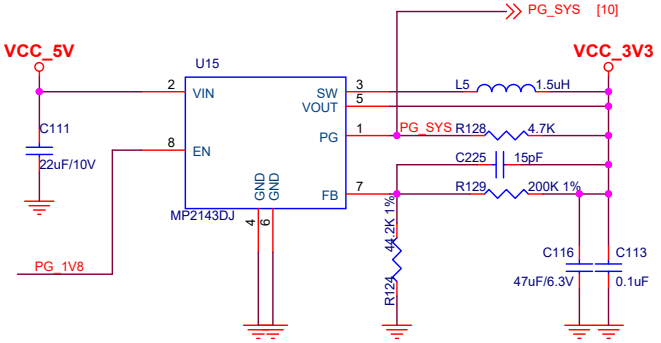

Vref = 0.6V VOUT = 3.3V

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