Stability Analysis of Quadratic Boost Converter with Different Controllers

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***Abstract*— DC-DC converters have played a key role in many applications. Such applications demand high gain without any change in voltage for any changes in line and load. Quadratic Boost Converter (QBC) provides a moderately high voltage gain compared to conventional boost topology. However, stability and closed-loop performance are difficult to achieve because of three RHP zeros. A stability analysis of QBC was conducted in this paper. The design of Type II and Type III controllers for QBC is discussed in this paper. A combination of Type II and Type III controllers is proposed for a stable operation of QBC. Performance is validated and compared with the conventional PI controller.**

Keywords—Quadratic Boost Converter, Type II controller, Type III Controller

I. INTRODUCTION

Nowadays, Renewable energy applications have come with significant penetration to provide a feasible alternative to rapidly depleting fossil reserves and to sustain growing energy demand. One of the limitation of renewable energy is its low output voltage. In the case of a PV system, we can increase the output voltage by connecting several PV modules in series, but this poses other issues due to partial shading conditions. DC-DC boost converters have been investigated as a solution to this problem.

The conventional DC-DC boost converter can provide limited voltage gain due to the losses associated with the inductor, filter capacitor, and main switch. Voltage stress across the switching device is also high and thus requires the switching device with a high voltage rating to be selected. The switching device with high-rated voltage has high on-state resistance (Rds.on), which results in high conduction losses. It also causes diode reverse recovery and high conduction losses [1,2].

Interleaved converters have the advantage of lower ripple in input current, have a limitation of low voltage gain, and many components requirements result in a complex control system, large size, and low efficiency [3,4]. Isolated converters can provide high voltage gain but are bulky due to the transformer. Also, leakage reactance causes voltage transient across the switch during its off condition. Clamp circuits are used to reduce this effect. It increases the complexity and cost of the network. Non-isolated converters are of two types coupled and non-coupled inductor converters. The Coupled inductors [5] are like isolated converters in which high voltage gain is achieved by increasing the voltage ratio of the transformer but suffer from the same demerits of a large size, bulky, and leakage inductor. To eliminate this leakage inductance, it uses a clamp circuit like in isolated converters to recycle the energy of the inductor. Non-coupled inductor based on these modifications is proposed in a classical boost converter. The modifications such as voltage multiplier converters [6] and switched inductors/switched capacitors [7,8] can provide high voltage gain without using coupled inductors or isolated transformers. Large multiplier stages require more components, increasing the complexity of the circuit. It also reduces the efficiency of the converter.

Out of the discussed converters, the Quadratic Boost Converter (QBC) provides moderate gain with limited disadvantages. Although QBC provides limited voltage gain in comparison to isolated converters but has higher power density which is one of the significant design parameters in compact and portable converters. N stage cascade boost converter with one active switch is proposed in [9]. The voltage gain of this converter is the same as the series connection of the N boost converter but with the use of a single switch only. The quadratic boost converter is the simplest form of N stage converter with N= 2 is discussed here in this paper.

The design of the controller for quad boost is discussed in [10, 11]. It used the current through the switch for feedback to change fourth-order dynamics to first-order. The author claims that the arrangement simplifies the controller design of the outer loop. A robust Fixed-Structure Cascade Controller for QBC based on a Genetic Algorithm is proposed in [12], but validation on actual QBC was missing. This paper presents a Type II controller design for QBC for its stable closed-loop operation. The operation of QBC with a Type II controller for the inner and outer loop can't provide stability. The presence of three RHP zeros which creates this non-minimum phase feature affects the stability. This non-minimum phase behaviour also results in unstable operation for a single Type III controller. A combination of type II and Type III controllers is proposed in this paper for the stable operation of QBC. The performance of QBC with this combination is compared with a conventional PI controller with the help of simulation.

The remainder of this paper is organized as follows. In Section II, a brief description of the operation of QBC is presented. The design parameters of QBC with the state space model are covered in Section III. Type II controller design is discussed in Section IV, and Type III controller design is discussed in Section V. Performance analysis of QBC with PI, Type II, and Type III controller is presented in Section VI. The paper concludes with some final remarks in Section VII.

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II. OPERATION OF QBC

Among all dc-dc converters, the selection of circuit is based on following criterion

1. Basic and derived converters
2. Isolated and Non isolated converters
3. Second order and Higher order converters

Quadratic boost is a fourth-order dc-dc converter. It is preferred over other converters mainly due to single switch control and maximum gain of up to four possible. It consists of one controlled switch, three diodes, and three energy storage elements: inductor L1, L2, and capacitor C1. Capacitor C2 is connected across the load and used for filtering. Fig.1 shows the circuit diagram of the Quadratic Boost Converter.

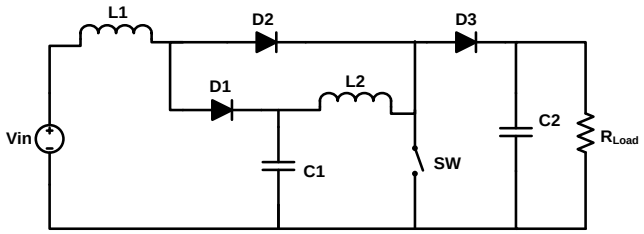

Fig.1. Schematic of QBC [13]

The operation of a converter is in two stages in one cycle of switching frequency

1. When the controlled switch is on,
2. When the controlled switch is off,

When the switch is on, inductors L1 and L2 charges through the dc source. C1 and C2 discharge through the load. Fig. 2 shows when the switch is in on condition.

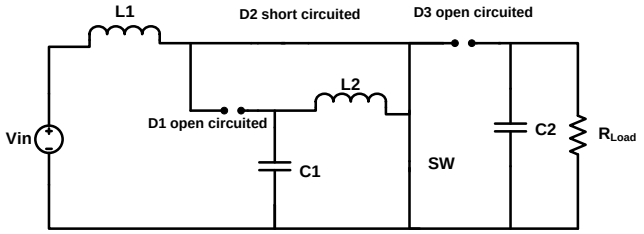

Fig.2. QBC with Switch ON condition [13]

When the switch is off, inductors L1 and L2 discharge through C1 and C2 also supply the load as shown in Fig. 3.

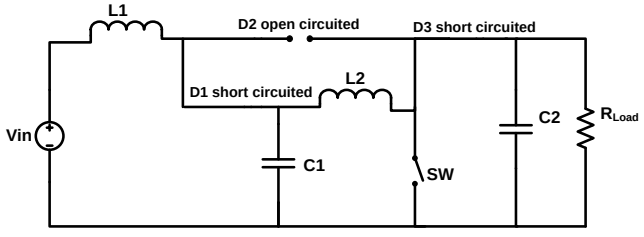

Fig.3. QBC with Switch OFF condition [13]

III. DESIGN OF QBC

The circuit is designed to get an output voltage of 48V from an input of 12V with a duty cycle of 0.5. The circuit parameters are as specified in Table I.

TABLE I. CIRCUIT PARAMETERS

Parameter	Specifications
Maximum input voltage, $V_{i,Max}$	13.2V
Minimum input voltage, $V_{i,Min}$	10.8V
Required output voltage, V_o	48V
Switching frequency f_s	18kHz
Minimum value of output current $I_{o,\,Min}$	0.25A
Maximum value of output current $I_{o,Max}$	1A

The current ripple is considered 20% of the total inductor current. The minimum and maximum values of inductor currents are as follows [14, 15].

$$I_{L1min} = \frac{I_{omin}}{(1-D)^2} = \frac{0.25}{(1-0.5)^2} = 1\ A \quad (1)$$

$$I_{L2min} = \frac{I_{omin}}{(1-D)} = \frac{0.25}{(1-0.5)} = 0.5\ A \quad (2)$$

$$I_{L1max} = \frac{I_{omax}}{(1-D)^2} = \frac{1}{(1-0.5)^2} = 4\ A \quad (3)$$

$$I_{L2max} = \frac{I_{omax}}{(1-D)} = \frac{1}{(1-0.5)} = 2\ A \quad (4)$$

Considering the CCM mode of conduction, the ripple currents are $\Delta I_{L1} = 20\% I_{L1}$ and $\Delta I_{L2} = 20\% I_{L2}$. Based on the ripple current and switching frequency, the minimum values of inductors are as follows,

$$L_{1min} = \frac{V_{in}.D}{\Delta I_{L1max}\, f_s} = \frac{12 \times 0.5}{0.2 \times 4 \times 18000} = 416.7\mu H$$

$$L_{1max} = \frac{V_{in}.D}{\Delta I_{L1min}\, f_s} = \frac{12 \times 0.5}{0.2 \times 1 \times 18000} = 1.67mH$$

$$L_{2min} = \frac{V_{in}.D}{\Delta I_{L2max}\,(1-D)\, f_s} = 1.67mH$$

$$L_{2max} = \frac{V_{in}.D}{\Delta I_{L2min}\,(1-D)\, f_s} = 6.67mH$$

$$L_1 = \frac{V_{in}\,D\,(1-D)^2}{2\,I_0\,f_s} = \frac{12 \times 0.5 \times 0.25}{2 \times 1 \times 18000} = 41.67\mu H$$

$$L_2 = \frac{V_{in}\,D}{2\,I_0\,f_s} = \frac{12 \times 0.5}{2 \times 1 \times 18000} = 166.67\mu H$$

$$C_{1min} = \frac{I_{omin}.D}{\Delta V_{C1}(1-D)\, f_s} = \frac{0.25 \times 0.5}{0.05 \times 24 \times 0.5 \times 18000} = 11.6\ \mu F$$

$$C_{1max} = \frac{I_{omax}\,D}{\Delta V_{C1}(1-D)\, f_s} = \frac{1 \times 0.5}{0.05 \times 24 \times 0.5 \times 18000} = 46.3\ \mu F$$

$$C_{2min} = \frac{I_{omin}.D}{\Delta V_{C2}\ f_s} = \frac{0.25 \times 0.5}{0.05 \times 48 \times 18000} = 2.89\mu F$$

$$C_{2max} = \frac{I_{omax}\ D}{\Delta V_{C2}\ f_s} = \frac{1 \times 0.5}{0.05 \times 48 \times 18000} = 11.6\mu F$$

$$C_1 = \frac{I_o.D}{\Delta V_{C1}(1-D)\ f_s} = \frac{1 \times 0.5}{0.05 \times 24 \times 0.5 \times 18000}$$

$$= 46.3\mu F$$

$$C_2 = \frac{I_o.D}{\Delta V_{C2}\ f_s} = \frac{1 \times 0.5}{0.05 \times 48\ \times 18000} = 11.6\mu F$$

The stability analysis is done using small signal analysis [16, 17]. State space matrices for the circuit, when the switch is in ON condition, are given as follows,

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & -1/L_2 & 0 \\ 0 & -1/C_1 & 0 & 0 \\ 0 & 0 & 0 & -1/RC_2 \end{bmatrix}$$

$$B_1 = \begin{bmatrix} 1/L_2 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad C_1 = [0 \quad 0 \quad 0 \quad 1]$$

Similarly, State space matrices for the circuit when switched in OFF condition are given as follows,

$$A_2 = \begin{bmatrix} 0 & 0 & 1/L_1 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 \\ 1/C_1 & -1/C_1 & 0 & 0 \\ 0 & 1/C_2 & 0 & -1/RC_2 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad C_2 = [0 \quad 0 \quad 0 \quad 1]$$

Based on the matrix under both the scenario, the final state space matrix is given as,

$$\dot{x} = Ax + Bu$$
$$y = Cx + Du$$

Where A, B, and C are the final matrix considering both switched ON and OFF conditions together

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & -1/L_2 & 0 \\ 0 & -1/C_1 & 0 & 0 \\ 0 & (1-d)/C_2 & 0 & -1/RC_2 \end{bmatrix}$$

$$B = \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad C = [0 \quad 0 \quad 0 \quad 1]$$

IV. TYPE II CONTROLLER DESIGN

Type II controller has a pole at the origin and is a kind of lead compensator. It provides a maximum phase boost of 90° with zero state error.

A. Mathemtical Model: Type II controller is a pair of pole-zero combinations with a pole at the origin [19, 21]. The expression of Type-II controller is given as

$$T_{C_{typeII}} = \frac{(1 + s/\omega_z)}{(s/\omega_{po})(1 + s/\omega_p)} \tag{5}$$

Where ω_p and ω_z are the frequency of the respective pole and zero location of the Type-II controller.

The magnitude of the transfer function is obtained by substituting *s* with $j\omega$,

$$\left|T_{C_{typeII}}\right| = \frac{|1 + j\omega/\omega_z|}{|j\omega/\omega_{po}||1 + j\omega/\omega_p|} = \frac{\sqrt{1 + (\omega/\omega_z)^2}}{(\omega/\omega_p)\sqrt{1 + (\omega/\omega_p)^2}} \tag{6}$$

The argument can be given as,

$$arg T_{C_{typeII}}(j\omega) = \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) - \frac{\pi}{2} \tag{7}$$

B. Derivation of K for Type II Controller

K type approach helps to design the controller to achieve desired phase margin at the desired cross-over frequency [18]. For the Type-II controller, the value of K is stated as "the ratio of the frequency at which the pole locate to the frequency at which zero locate". The combination of this pole and zero can give a phase boost up to 90° at the desired cross-over frequency. The value of K in terms of the phase boost of the controller [20, 21] is expressed as (8).

$$K = \tan\left(\frac{phase\ boost}{2} + \frac{\pi}{4}\right) \tag{8}$$

By using the relation, $K = f_p/f_z$ pole frequency and zero frequency will be derived. Assuming the cross-over frequency is less than the switching frequency proper locations of the pole, zero can be defined from (9) and (10).

C. Inner Loop Controller Design

The inner loop controller design is based on the sensing of the input current of the QBC. The key factor in designing such that the inner current loop is to be faster than that of the outer voltage loop. Bandwidth selection will be critical in such design methods. The frequency response of the inner loop controller is shown in Fig 4, which can provide a boost of 70° at the desired crossover frequency of 2.25 kHz.

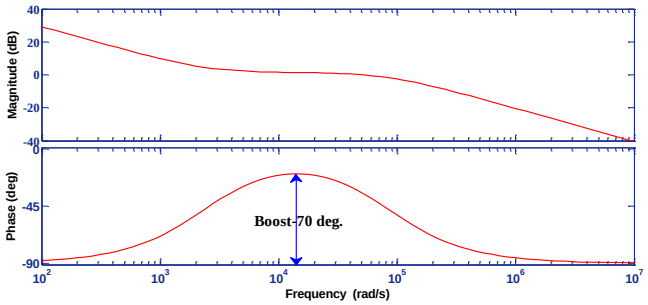

Fig.4. Frequency Response for Type II controller

Thus, from equations (9) and (10), the pole location for the inner loop Type II controller is given as,

$$f_{p_i} = tan\left(\frac{phase\ boost}{2} + \frac{\pi}{4}\right) f_{c_i}$$
$$= tan\left(\frac{70}{2} + \frac{\pi}{4}\right) \times 2250 = 12.76kHz \quad (9)$$

Also, zero is placed as,

$$f_{z_i} = \frac{f_{c_i}}{tan\left(\frac{phase\ boost}{2} + \frac{\pi}{4}\right)}$$
$$= \frac{2250}{tan\left(\frac{70}{2} + \frac{\pi}{4}\right)} = 396.7Hz \quad (10)$$

Hence the transfer function of the inner loop Type II controller is given as

$$T_{c_i} = \frac{I_{L1}}{D} = \frac{96000(s + 2493)}{s(s + 80173)} \quad (11)$$

D. Outer Loop Controller Design

The design process of the outer loop poses challenges, as the outer loop transfer function has three RHP zeros making the system a non-minimum phase system. The boost requirement at the cross-over frequency is more than 90° thus, to achieve this boost Type III controller is proposed for the outer voltage loop.

V. TYPE III CONTROLLER DESIGN

The Type-III controller is a lead-lead type controller able to furnish a maximum phase boost of 180° with zero steady-state error.

A. *Mathematical Model:*

Type III controller is a controller with pair of poles and zeros in addition to the pole at the origin [20, 21]. The transfer function of the Type III controller is given as,

$$T_{c_o}(s) = \frac{(1 + s/\omega_{z1})\,(1 + s/\omega_{z2})}{(s/\omega_{po})(1 + s/\omega_{p1})\,(1 + s/\omega_{p2})} \quad (12)$$

Assuming two zeros at the same location and two poles are at the same location. Hence, $\omega_{z1} = \omega_{z2} = \omega_z$ and $\omega_{p1} = \omega_{p2} = \omega_p$. Hence, the equation modifies as,

$$T_{c_o}(s) = \frac{(1 + s/\omega_z)^2}{(s/\omega_{po})\,(1 + s/\omega_p)^2} \quad (13)$$

The magnitude of the controller transfer function can be obtained by replacing $s = j\omega$

$$|T_{c_o}(j\omega)| = \frac{|1 + (j\omega/\omega_z)||1 + (j\omega/\omega_z)|}{|j\omega/\omega_{po}||1 + (j\omega/\omega_p)||1 + (j\omega/\omega_p)|}$$

Argument can be written as

$$arg T_{co}(j\omega) = 2\tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) - \frac{\pi}{2} \quad (14)$$

B. Derivation of K for Type II Controller

The value of K for the Type-III controller is stated as "the ratio of the frequency at which the double pole is located to the frequency at which double zero is located" [18]. Consolidation of these poles and zeros can furnish a maximum phase boost of 180° at the desired crossover frequency. The value of K in terms of the phase boost of the controller [20, 21] is expressed as (15).

$$K = \left\{\tan\left(\frac{phase\ boost}{4} + \frac{\pi}{4}\right)\right\}^2 \quad (15)$$

Hence two poles location and two zeros location for Type III controller is obtained as,

$$f_p = \sqrt{K}.f_c \ ; f_z = \frac{f_c}{\sqrt{K}} \quad (16)$$

The exact point where double zero and double pole reside can be determined from (16) if, the cross-over frequency is established, with the value of the necessary phase boost. The frequency response of the Type-III controller is plotted as shown in Fig.5, which has a phase boost at the desired cross-over frequency of 900 Hz.

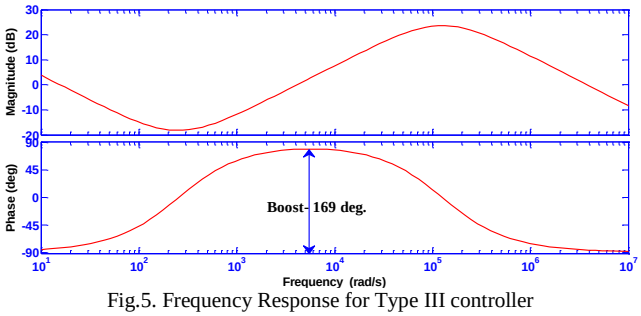

Fig.5. Frequency Response for Type III controller

Thus from equation (16), the pole location for the outer loop Type III controller is given as,

$$f_{p_o} = tan\left(\frac{phase\ boost}{4} + \frac{\pi}{4}\right) f_{c_o}$$

$$= tan\left(\frac{169}{4} + \frac{\pi}{4}\right) \times 900 = 18737$$

$$f_{z_o} = \frac{f_{c_o}}{tan\left(\frac{phase\ boost}{2} + \frac{\pi}{4}\right)}$$
$$= \frac{900}{tan\left(\frac{169}{2} + \frac{\pi}{4}\right)} = 43.23Hz$$

Hence, the transfer function of the Type-III controller is given as,

$$T_{C_o} = \frac{V_{c_2}}{I_{L1}} = 3.8 \times 10^6 \frac{(s+272)^2}{s\,(s+1.17\times10^5)^2}$$

VI. SIMULATION OF QBC

The closed-loop operation of QBC is simulated to validate the stability of the quadratic boost converter. It consists of two loops: the inner current loop and the outer voltage loop. The variation in the load is fast, which causes a rapid change in the current. The stability is ensured under rapid current changing conditions by keeping the cross-over frequency for the current loop lesser than the switching frequency. In the DC-DC converter, the output voltage variation is slow, so the voltage loop is selected as an outer loop whose operating frequency is lesser than the inner current loop frequency. Fig.6 shows the closed-loop quadratic boost converter, with the inductor current (IL_1) and the load voltage (V_o) sensed for closed-loop operation. These signals are then passed through low-pass filters to filter unwanted noise or harmonic contents. A comparator is used to compare these signals with the desired reference. The output of the comparator is passed through the controller to get the desired PWM pulses for controlling the switching device.

A. Simulation Performance with PI Controller

Simulation performance is validated for different configurations, as mentioned in Table II. For the PI controller, the performance of the circuit is validated for different values of K_p and K_i for both the inner loop and outer loop by the trial and error method. One which shows stable operation is considered for final validation in terms of load variation and source variation. Two scenarios of a 25% rise in load and a 25% rise in source voltage are considered to validate the performance of the PI controller. The output voltage under both scenarios is shown in Fig.7 and Fig.8

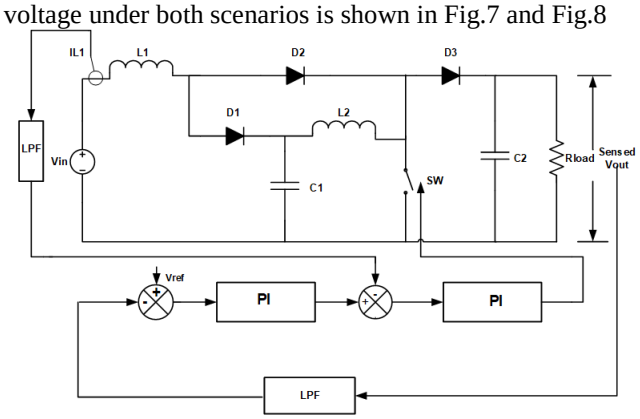

Fig.6. Closed Loop Operation of QBC

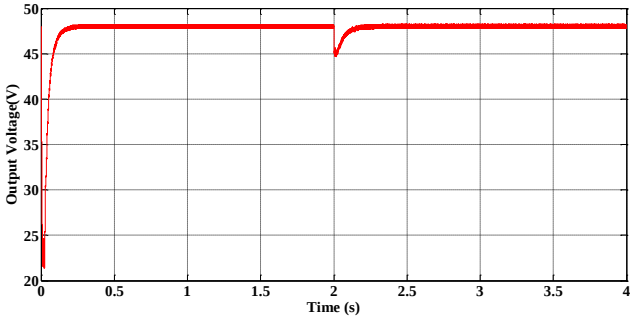

Fig.7. Load Voltage (V_o) under Load variation with PI controller

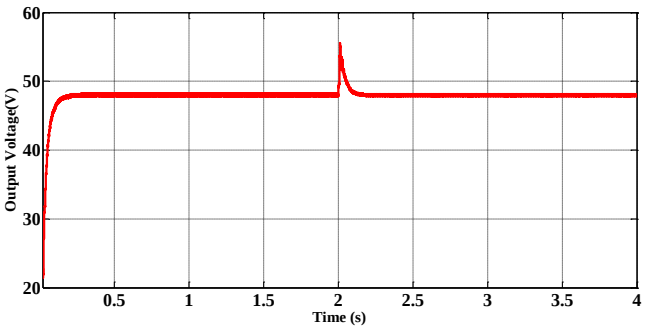

Fig.8. Load Voltage (Vo) under Source variation with PI controller

B. Simulation Performance with Type II Controller

Simulation performance is validated with a Type II controller. Type II controller is designed for the inner loop, as discussed in section IV. Outer-loop demands a boost of more than 90°, which is impossible to achieve from a Type II controller due to three RHP zeros. Desired boost requirement is possible to meet only with a Type III controller. Hence, the outer loop is designed, as discussed in section V. Type II controller is used in the inner loop and Type III controller is used in the outer loop as shown in Fig.6. Performance validation is conducted in a similar way as for PI controllers such as load variation and source variation of 25%. Output voltage response under load variation and source variation as shown in Fig. 9 and Fig. 10.

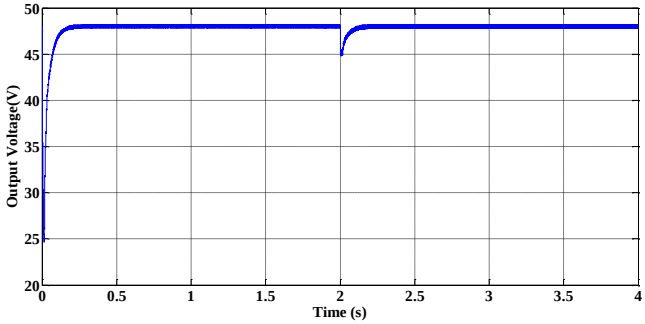

Fig.9. V_o under Load variation with Type II and Type III controller

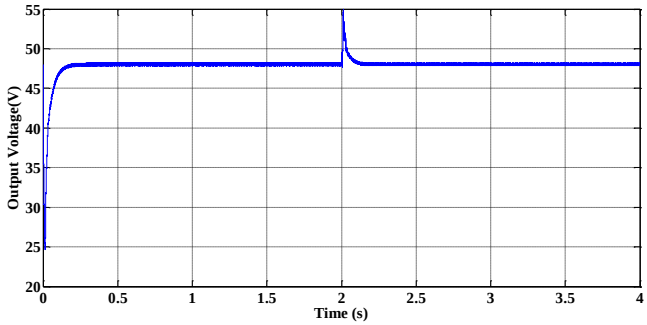

Fig.10. V_o under source variation with Type II and Type III controller

Following controller combinations are simulated to check the stability of the closed loop system.

Table II Selection of controller and their effect on stability

Inner loop controller	Outer loop controller	Remarks
PI	PI	Stable Operation
Type 2	Type 2	Oscillatory behaviour
Type 3	Type 3	Oscillatory behaviour
Type 2	Type 3	Stable Operation

Even though the PI controller shows stable operation, but characteristic behavior of 2 degrees of freedom (DOF) can't satisfy all the requirements of plant operation [22]. Thus, rigorous tuning efforts are required with the tradeoff between the various design criteria of the plant. The distinguishing feature of Type II and Type III controllers over PI controllers is the allocation of the pole at a higher frequency. It causes significant attenuation of the high-frequency harmonic content in the signal.

The oscillatory behavior of Only Type II and Type III is due to the matching of cross-over frequency to that of resonating frequency of energy storage elements. It required rigorous efforts while selecting cross-over frequency to optimize the oscillations.

VII. CONCLUSIONS

In this paper, the mathematical modeling of QBC is applied to design Type II and Type III controllers for the QBC. The Type II controller is used for the inner and outer loops of the QBC. However, stable operation cannot be achieved by using a Type II controller in both loops. This is due to the presence of three RHP zeros in the transfer function, which causes a high boost requirement. However, a single Type III controller can't provide a stable operation. A type II controller, for the Inner loop, and a Type III controller, for the outer loop, was implemented to achieve stability. This operation is endorsed by simulating QBC for load and source variation conditions. The effect of the parasitic component is ignored in this analysis which may affect the maximum gain and efficiency of the QBC. This effect will be addressed in a hardware implementation of QBC.

REFERENCES

[1] S. A. Ansari, J. S. Moghani, G. Gharehpetian, and M. R. Nasab, "A Novel High Efficiency Interleaved Flyback Inverter for Smart Home Applications," in 2018 Smart Grid Conference (SGC), 2018, pp. 1-7: IEEE.

[2] M. Changizian, S. Rezazade, A. Saleki, and M. T. Bina, "Application of Vienna Converter to a double-driven SRMs under one PFC compensator," in 2018 9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC), 2018, pp. 294-299: IEEE

[3] M. Changizian, A. Saleki, and S. Rezazade, "A novel FPGA control scheme to improve power factor and reduce the harmonic distortion in a three phase VIENNA rectifier," in *2017 32th International Power System Conference (PSC)*, 2017

[4] S. Arab Ansari, J. S. Moghani, and M. Mohammadi, "Analysis and implementation of a new zero current switching flyback inverter, "*International Journal of Circuit Theory and Applications*, vol. 47, no. 1, pp. 103-132, 2019.

[5] Wang, J., Dunford, W.G., and Mauch, K.: 'A comparison of modified boost converters with continuous inductor current mode and ripple free input current with conventional converters'. IEEE Industry Applications Conf., New York, NY, USA, 1996, pp. 878–885

[6] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," IEEE Transactions on Power Electronics, vol. 23, DOI 10.1109/TPEL.2007.915762, no. 2, pp. 871-887, Mar. 2008.

[7] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/ switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 55, DOI 10.1109/TCSI.2008.916403, no. 2, pp. 687-696, Mar. 2008.

[8] M. Forouzesh, K. Yari, A. Baghramian, and S. Hasanpour, "Single-switch high step-up converter based on coupled inductor and switched capacitor techniques with quasi-resonant operation," IET Power Electronics, vol. 10, DOI 10.1049/iet-pel.2015.0923, no. 2, pp. 240-250, Feb. 2017.

[9] Ramos, J. Leyva, M. G. Ortiz-Lopez, and J. A. Morales-Saldana. "Control of a cascade boost converter with a single active switch." In 2008 IEEE Power Electronics Specialists Conference, pp. 2383-2388. IEEE, 2008.

[10] Morales - Saldaña, Jorge Alberto, Rodrigo Loera - Palomo, Elvia Palacios - Hernández, and Jorge Luis González - Martínez. "Modelling and control of a DC‐DC quadratic boost converter with R2P2." IET Power Electronics 7, no. 1 (2014): 11-22.

[11] Morales-Saldana, Jorge Alberto, R. Galarza-Quirino, J. Leyva-Ramos, E. E. Carbajal-Gutierrez, and M. G. Ortiz-Lopez. "Multiloop controller design for a quadratic boost converter." IET Electric Power Applications 1, no. 3 (2007): 362-367.

[12] Srithongchai, Pitsanu, and Somyot Kaitwanidvilai. "Robust fixed-structure cascade controller for a quadratic boost converter." In Lecture Notes in Engineering and Computer Science: Proceedings of the International MultiConference of Engineers and Computer Scientists, IMECS, pp. 1030-1033. 2010.

[13] Tattiwong, K., and C. Bunlaksananusorn. "Analysis design and experimental verification of a quadratic boost converter." In TENCON 2014-2014 IEEE Region 10 Conference, pp. 1-6. IEEE, 2014.

[14] Yijie Wang,Yuping Qiu, Qing Bian, Yueshi Guan and Dianguo Xu, "A Single Switch Quadratic Boost High Step up DC-DC Converter," DOI 10.1109/TIE.2018.2860550, IEEETransactions on Industrial Electronics

[15] Boujelben, Nesrine, Ferdaous Masmoudi, Mohamed Djemel, and Nabil Derbel. "Design and comparison of quadratic boost and double cascade boost converters with boost converter." In 2017 14th International Multi-Conference on Systems, Signals & Devices (SSD), pp. 245-252. IEEE, 2017.

[16] Oswaldo Lopez-Santos, Luis Martinez-SalameroGermain Garcia, Hugo Valderrama-Blavi, and Tomás Sierra-Polanco, "Robust Sliding Mode Control Design for a Voltage Regulated Quadratic Boost Converter," DOI 10.1109/TPEL.2014.2325066, IEEE Transactions on Power Electronics IEEE transactions on power electronics, Vol. X, No. X, December 2014

[17] J. Leyva-Ramos, R. Mota-Varona, M. G. Ortiz-Lopez, L. H. Diaz-Saldierna, and D. Langarica-Cordoba, "Control Strategy of a Quadratic Boost Converter with Voltage Multiplier Cell for High Voltage Gain," DOI 10.1109/JESTPE.2017.2749311, IEEE Journal of Emerging and Selected Topics in Power Electronics

[18] Venable, H. Dean. "The K factor: A new mathematical tool for stability analysis and synthesis." In Proc. Powercon, vol. 10, no. 1, p. 1. Citeseer, 1983.

[19] Ghosh, Arnab, Subrata Banerjee, Mrinal Kanti Sarkar, and Priyanka Dutta. "Design and implementation of type - II and type - III controller for DC‐DC switched - mode boost converter by using K - factor approach and optimisation techniques." IET Power Electronics 9, no. 5 (2016): 938-950.

[20] Ghosh, Arnab, and Subrata Banerjee. "Design of Type-III controller for dc-dc switch-mode boost converter." In 2014 6th IEEE Power India International Conference (PIICON), pp. 1-6. IEEE, 2014.

[21] Basso, Christophe P. "Designing control loops for linear and switching power supplies: a tutorial guide." (2012).

[22] Mallik, Ayan, Jiangheng Lu, and Alireza Khaligh. "A comparative study between PI and type-II compensators for H-bridge PFC converter." *IEEE Trans. Ind. Appl* 54, no. 2 (2018): 1128-1135.