Motherboard
User's Manual
用户手册

SV3b-12N46 Series

Ver 0.0

Contents

1 Models and Attentions

1.1 Model

This manual is applied to following models:

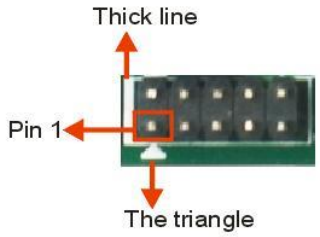
Model	CPU	COM	LAN	HDMI	eDP/ LVDS	USB	M.2 KEY-M	Mini-PCIe	SATA 3.0	B2B
SV3b-12N46-N95	N95	2	4	1	LVDS	6	SATA	PCIE+ USB2.0	1	1
SV3b-12N46-N97	N97	2	4	1	LVDS	6	SATA	PCIE+ USB2.0	1	1
SV3b-12N46-N100	N100	2	4	1	LVDS	6	SATA	PCIE+ USB2.0	1	1
SV3b-12N46-N305	i3-N305	2	4	1	LVDS	6	SATA	PCIE+ USB2.0	1	1

1.2 Attentions

1) **Notes under a table or figure indicate the difference of models, or alternative definition of specific pin of the header (jumper/connector).**

2) **How to identify the first pin of a header or jumper**

○ Usually, there is a thick line or a triangle near the header's or jumper's pin 1.



○ Square pad, which you can find on the back of the motherboard, is usually used for pin 1.

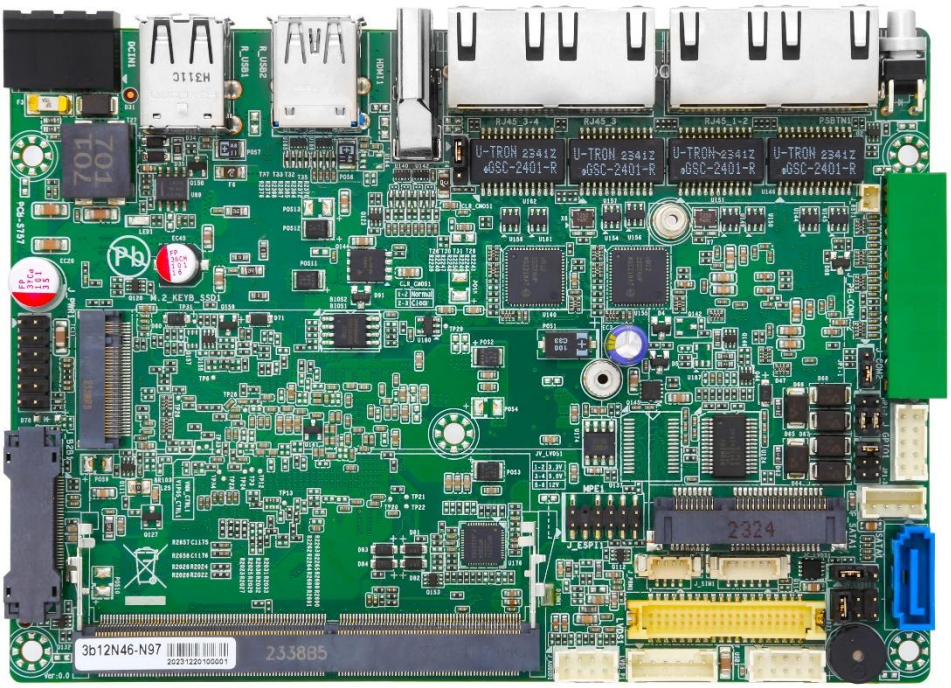
2 Specification

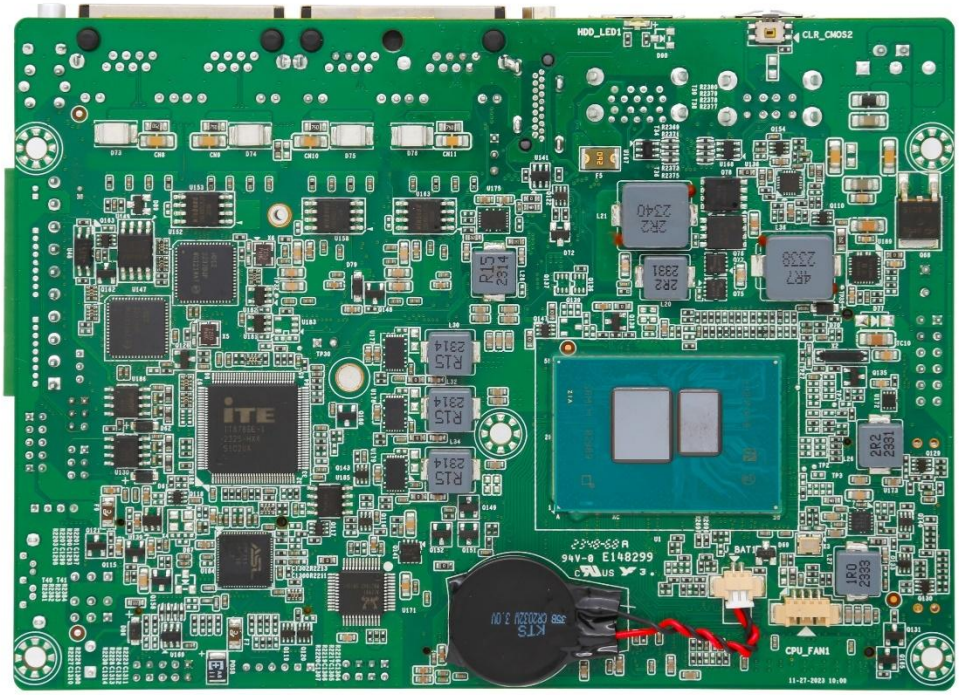
Specifications					
Model		**SV3b-12N46-N95**	**SV3b-12N46-N97**	**SV3b-12N46-N100**	**SV3b-12N46-N305**
Processor System	Processor	Intel® Alder Lake-N Series Processor			
		N95	N97	N100	i3-N305
	Clock Speed	up to 3.40GHz	up to 3.60GHz	up to 3.40GHz	up to 3.80GHz
	Multi-Core	4E-Core	4E-Core	4E-Core	8E-Core
	TDP	15W	12W	6W	15W
	BIOS	AMI UEFI BIOS (Support Watchdog Timer)			
Memory	Slot Type	1, DDR4 Non-ECC SO-DIMM			
	Memory Type	DDR4 3200MHz			
	Max Memory	16GB			
	Channels	Single			
Display	Graphics	Intel® UHD Graphics			
		up to 16 EUs, 1.20 GHz	up to 24 EUs, 1.20 GHz	up to 24 EUs, 750 MHz	up to 32 EUs, 1.25 GHz
	HDMI	1, HDMI, max 4096*2160@30Hz			
	eDP/LVDS	1, LVDS, max 1920*1200@60Hz			
		Notes: *: BOM optional support eDP, max 4096*2160@30Hz			
	Multi-Display	Dual			
Audio	Codec	Realtek Audio HDA codec			
	Audio	1, Line-Out + MIC			
Storage	M.2 SSD	1, M.2 M-Key 2280, PCIE 2x/SATA, Default SATA, Support SATA SSD			
		Notice: *: PCIE signal colay with SATA1 and M.2_KEYB_SSD1. When using SATA1, M.2_KEYB_SSD1 can only support SATA.			
	SATA	1, SATA Gen3 6Gbps			
Expansion Slot	Mini-PCIe	1, Mini-PCIe, PCIE+USB2.0, support WIFI+4G Module			
	SIM Card	1, SIM Crad			
	B2B	1, Expansion Card 1, Expansion Card Power Input			

Ethernet	Chipset	4, Intel® i210 GbE Ethernet Controller
USB	USB3.0	2, USB3.2 Gen1 5Gbps
	USB2.0	4, USB2.0
I/O	Serials	1, RS232/RS485, COM1, default RS232 selected by jumper 1, RS232/RS485, COM2, default RS232 selected by resistors
	Power on	2
	Reset	1
	HDD LED	1
	FAN	1, CPU FAN
	CMOS Clear	1
GPIO	GPIO	4* GPI, 4* GPO, non-isolated 5V
Power	Power in	1, DC 24V Power Input
		Notes: *: BOM optional support 12V.
OS	OS Supported	Windows 10/11 64bit, Linux
Environment	Temperature	Operation: 0 ~ 60˚C Storage: -40 ~ 85˚C
	Humidity	5 ~ 95%, non-condensing
Mechanical	Dimension	3.5 inch, 146mm*105mm
	Height	PCB: 1.6mm

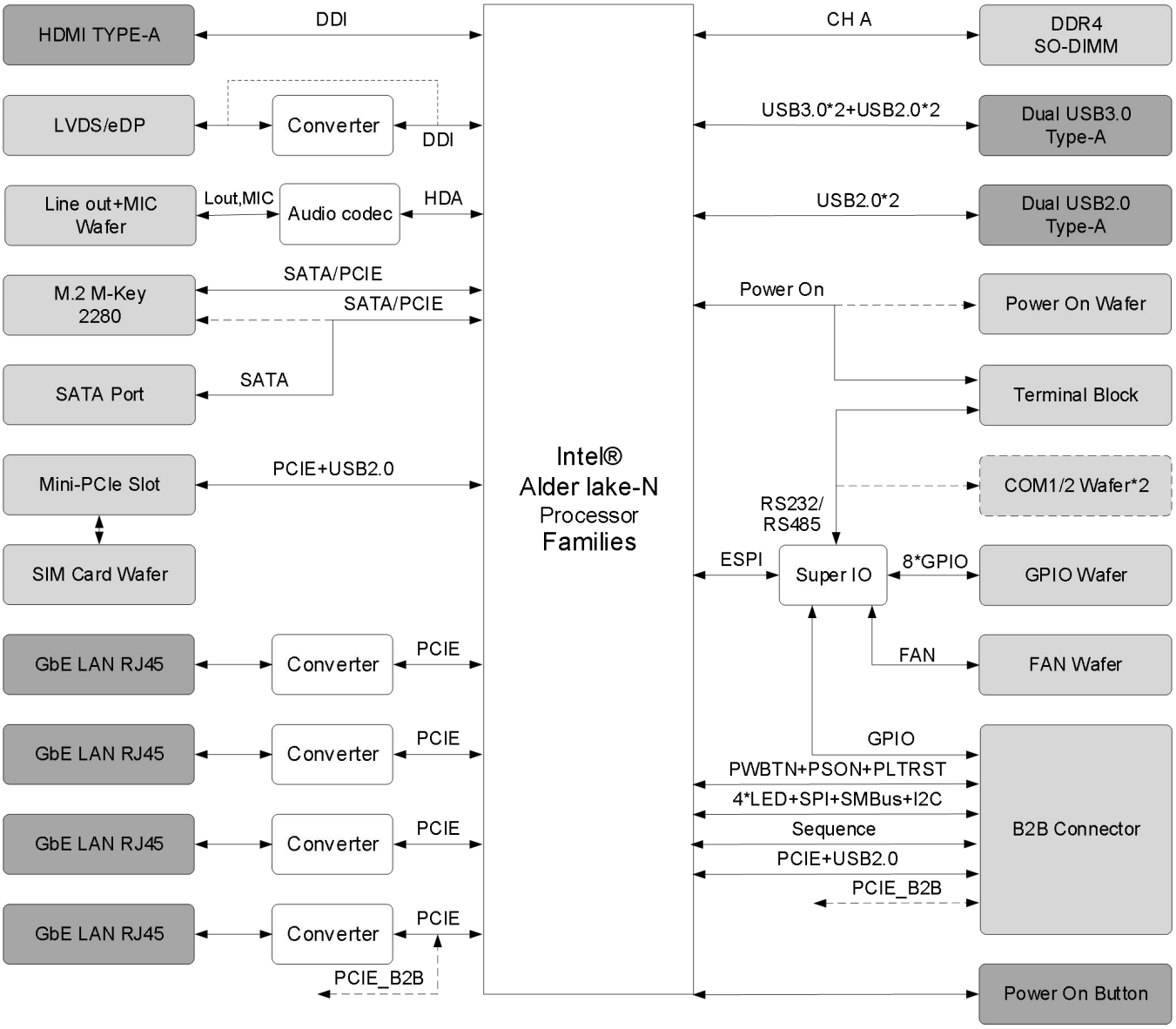
Interfaces

Model		SV3b-12N46-N95	SV3b-12N46-N97	SV3b-12N46-N100	SV3b-12N46-N305
Rear I/O	Power on	1, Button			
	Ethernet	4, GbE RJ45			
	HDMI	1, HDMI TYPE-A			
	USB2.0	2, USB3.0 TYPE-A			
	USB3.0	2, USB3.0 TYPE-A			
	Power In	1, 3P 5.08mm Terminal Block			
		Notes: *: BOM optional support 2P 3.5mm Terminal Block.			
Internal I/O	Display	1, DF13, eDP/LVDS, with Backlight Control Wafer			
	Audio	1, Wafer, Line-out+ MIC			
	Storage	1, SATA 7P Port, with Power supply Wafer 1, M.2 M-Key 2280, SATA, support SATA SSD			
	Expansion	1, Mini-PCIe Slot, PCIE+USB2.0, Support WIFI+4G 1, Wafer, SIM Card 1, Board to Board Connector, Expansion Card 1, Header, Expansion Card Power Input			
	USB2.0	2, Wafer			
	Serial	1, 10P Terminal Block, COM1+COM2+Power on			
		Notice *: COM1 wafer+COM2 wafer +Power on wafer optional.			
	GPIO	1, Wafer			
	Reset	1, Wafer			
	HDD LED	1, Blue light LED			
	FAN	1, Wafer, CPU FAN			
Others	Jumper	1, LVDS1 VDD Select 1, LVDS1 Blacklight Control Select 2, COM1 RS232/RS485 Select 1, COM1 RS485 Signal 120Ω Resistive termination Select 1, CMOS Clear Select			
	RTC	1, Wafer			
	Buzzer	1			

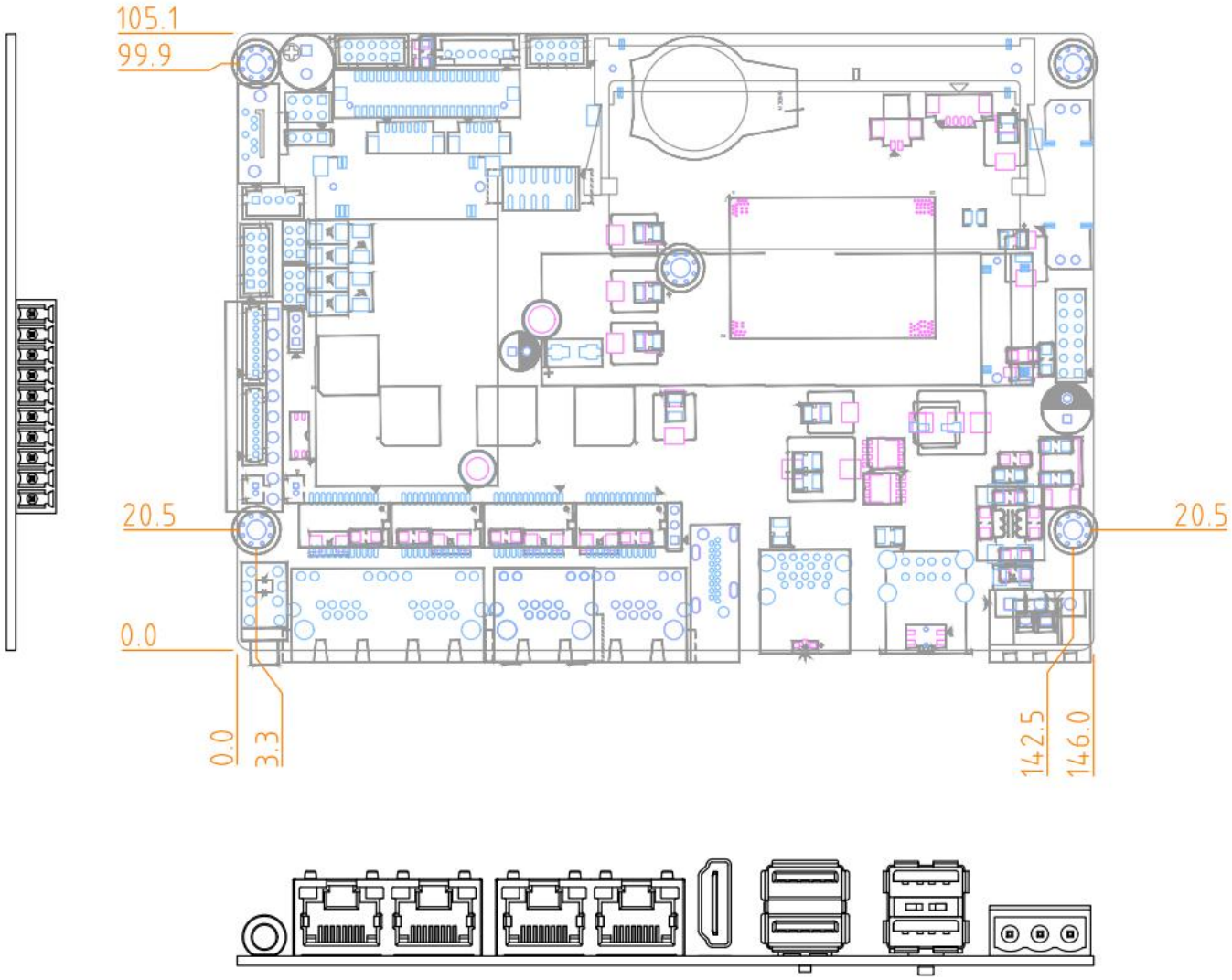

U-TRON 2341Z
GSC-2401-R
3b12N46-N97


HDD_LED1
CLR_CMOS2
CPU_FAN1

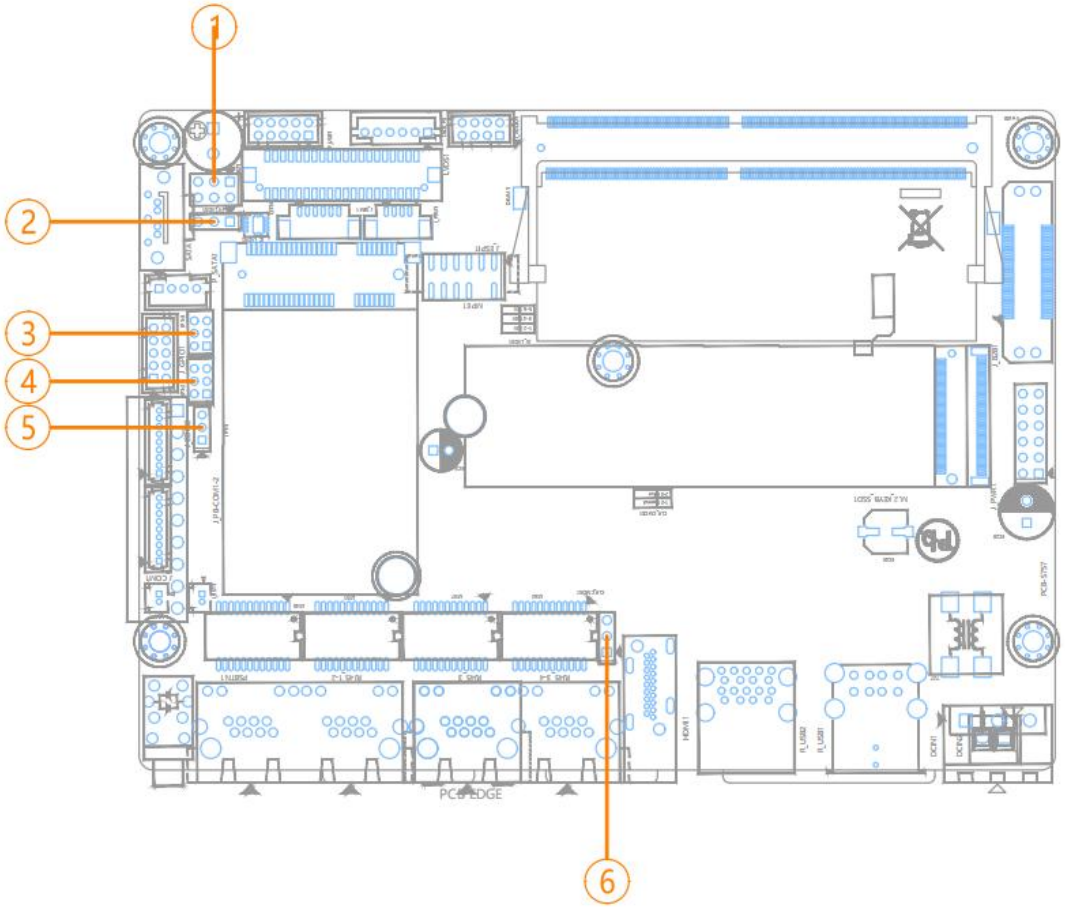
3 Block Diagram



4 Mechanical Drawing



5 Jumper



Jumpers / Headers and Connectors		
1	JV_LVDS1	LVDS1 VDD Select Jumper
2	JC_LVDS1	LVDS1 Blacklight Control Select Jumper
3	JP1-3	COM1 RS232/RS485 Select Jumper1
4	JP1-2	COM1 RS232/RS485 Select Jumper2
5	JP1-1	COM1 RS485 Signal 120Ω Resistive termination Select Jumper
6	CLR_CMOS1	CMOS Clear Select Jumper

6 Definition of Jumpers

6.1 LVDS VDD Select: Jumper, 3*1P, 2.54mm (Mark No.1, JV_LVDS1)

Graphic	Setting	Function
	1-2(Default)	VCC3.3
	3-4	VCC5
	5-6	VCC12

6.2 LVDS1 Blacklight Control Select Jumper, 3*2P, 2.54mm (Mark No.2, JC_LVDS1)

Graphic	Setting	Function
	1-2 (Default)	PWM
	2-3	CCFL/PWM#

Notice:

[1]: It can support CCFL/PWM#, CCFL by default. (resistor selectable)

6.3 COM1 RS232/RS485 Select Jumper, 3*2P, 2.00mm (Mark No.3/2, JP1-3/ JP1-2)

Graphic	Setting	Function
	JP1-3: 1-2(Default) JP1-2: 3-5, 4-6	COM1: RS232
	JP1-3: 5-6 JP1-2: 1-3, 2-4	COM1: RS485

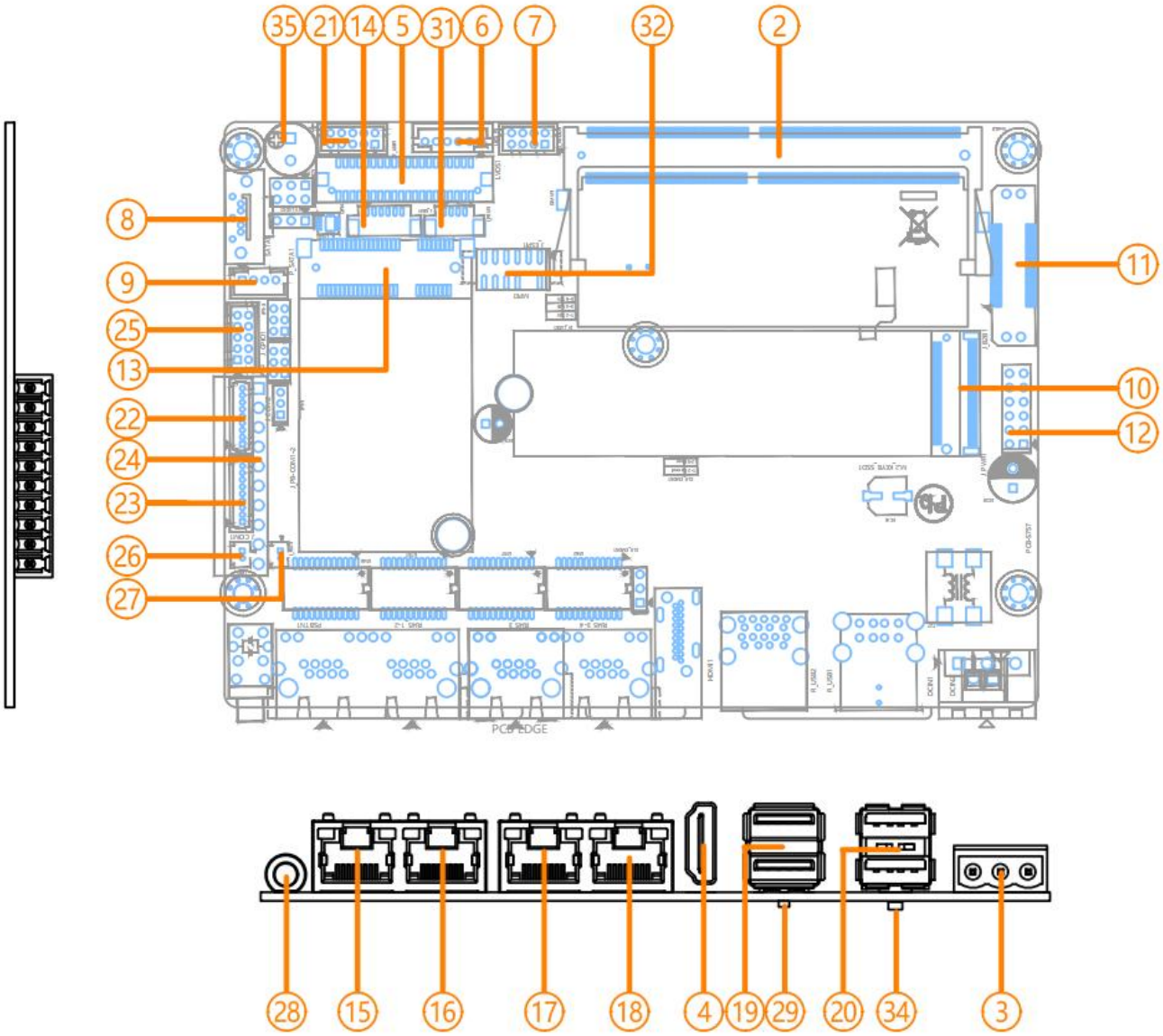
6.4 COM1 RS485 Signal 120Ω Resistive termination Select Jumper, 3*1P, 2.00mm (Mark No.5, JP1-1)

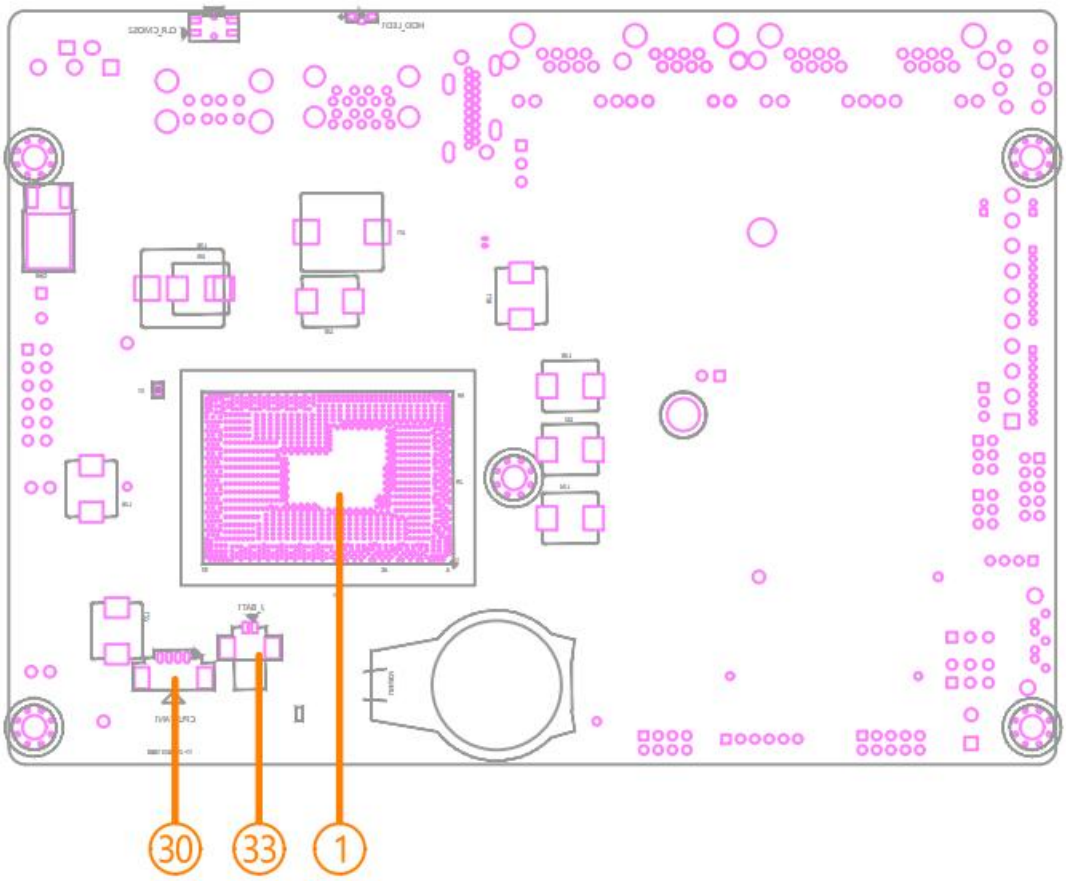
Graphic	Setting	Function
	1-2 (Default)	Disable
	2-3	Enable

6.5 CMOS Clear Select Jumper, 3*1P, 2.54mm (Mark No.6, CLR_CMOS1)

Graphic	Setting	Function
	1-2 (Default)	Normal
	2-3	Clear CMOS

7 Headers / Wafers and Connectors



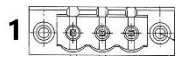


Headers / Wafers and Connectors		
①	U1	CPU
②	DIMM1	DDR4 SO-DIMM Slot
③	DCIN1 (DCIN2)	DC 12-24V Power Input 3P 5.08mm Terminal Block (DC 12-24V Power Input 2P 3.5mm Terminal Block)
④	HDMI1	HDMI TYPE-A Connector
⑤	LVDS1	eDP/LVDS Signal DF13 Connector
⑥	LVDS_P1	LVDS Backlight Control Wafer
⑦	J_AUDIO1	Front Audio Wafer
⑧	SATA1	SATA3.0 7P Connector
⑨	P_SATA1	SATA Power Wafer
⑩	M.2_KEYB_SSD1	M.2 M-Key-Slot (PCIE 2X/SATA, Support PCIE 2x NVMe/SATA SSD, 2280)
⑪	J_B2B1	Expansion Card Connector
⑫	J_PWR1	Expansion Card Power Supply Header
⑬	MPE1	Mini-PCIe Slot (PCIE+USB2.0, Support WIFI+4G)
⑭	J_SIM1	SIM Card Wafer
⑮	RJ45_1	GbE LAN RJ45 Connector
⑯	RJ45_2	GbE LAN RJ45 Connector
⑰	RJ45_3	GbE LAN RJ45 Connector
⑱	RJ45_4	GbE LAN RJ45 Connector

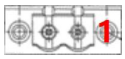
19	R_USB2	Dual USB3.0 TYPE-A Connector
20	R_USB1	Dual USB2.0 TYPE-A Connector
21	F_USB1	Front Dual USB2.0 Wafer
22	J_COM2	COM2 Wafer
23	J_COM1	COM1 Wafer
24	J_PB_COM1-2	COM1-2 + Power on Terminal Block
25	J_GPIO1	Front GPIO Wafer
26	J_PB1	Power on Wafer
27	J_RST1	Reset Wafer
28	PSBTN1	Power On Button
29	HDD_LED1	HDD LED
30	CPU_FAN1	CPU FAN Wafer
31	J_PRM1	Power Debug Wafer
32	J_ESPI1	ESPI Header
33	J_BAT1	CMOS Battery Wafer
34	CLR_CMOS2	CMOS Clear Jumper
35	BZ1	Buzzer

8 Definition of Connectors

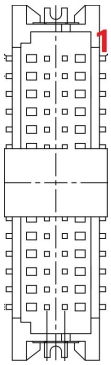
8.1 DC 12-24V Power Input: Terminal Block, 3*1P, 5.08mm (Mark No.3, DCIN1)

Graphic	Pin	Definition	Pin	Definition
	1	GND_EARTH	3	DC_IN
	2	GND		

8.2 DC 12-24V Power Input: Terminal Block, 3*1P, 5.08mm (Mark No.3, DCIN1)

Graphic	Pin	Definition	Pin	Definition
	1	GND	2	DC_IN

8.3 eDP/LVDS Signal DF13, 20*2P, 1.25mm (Mark No.5, LVDS1)

Graphic	Pin	Definition	Pin	Definition
	1	VDD_PANEL	2	VDD_PANEL
	3	LVDS_PRSNT	4	GND
	5	VDD_PANEL	6	VDD_PANEL
	7	LVDS_A_DATA0-	8	LVDS_B_DATA0- /EDP1_TX0- [2]
	9	LVDS_A_DATA0+	10	LVDS_B_DATA0+ /EDP1_TX0+ [2]
	11	GND	12	GND
	13	LVDS_A_DATA1-	14	LVDS_B_DATA1- /EDP1_TX1- [2]
	15	LVDS_A_DATA1+	16	LVDS_B_DATA1+ /EDP1_TX1+ [2]
	17	GND	18	GND
	19	LVDS_A_DATA2-	20	LVDS_B_DATA2- / EDP1_TX2- [2]
	21	LVDS_A_DATA2+	22	LVDS_B_DATA2+ / EDP1_TX2+ [2]
	23	GND	24	GND
	25	LVDS_A_CLK-	26	LVDS_B_CLK- /EDP1_TX3- [2]
	27	LVDS_A_CLK+	28	LVDS_B_CLK+ /EDP1_TX3+ [2]
	29	GND	30	GND
	31	N/C	32	EDP1_HPD_C
	33	GND	34	GND
	35	LVDS_A_DATA3-	36	LVDS_B_DATA3- /EDP1_AUX- [2]

	37	LVDS_A_DATA3+	38	LVDS_B_DATA3+ /EDP1_AUX+ [2]
	39	N/C	40	GND

Notes:

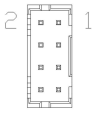
[1]: Panel Power VDD is 3.3V by default, 5V or 12V is selectable by “eDP/LVDS VDD Select Jumper”. (JV_LVDS1)

[2]: It supports LVDS by default and can support eDP if specified. (BOM selectable).

8.4 LVDS Backlight Control: Wafer ,6*1P, 2.00mm (Mark No.6, LVDS_P1)

Graphic	Pin	Definition	Pin	Definition
	1	GND	4	LVDS_EN_BKLT
	2	GND	5	VCC12
	3	LVDS_BKLTCTL	6	VCC12

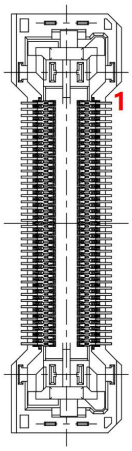
8.5 Front Audio: Wafer, 4*2P, 2.00mm (Mark No.7, J_AUDIO1)

Graphic	Pin	Definition	Pin	Definition
	1	MIC_R	2	Line out_R
	3	GND	4	GND
	5	GND	6	GND
	7	MIC_L	8	Line out_L

8.6 SATA Power: Wafer, 4*1P, 2.00mm (Mark No.9 P_SATA1)

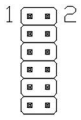
Graphic	Pin	Definition	Pin	Definition
	1	VCC12	3	GND
	2	GND	4	VCC5

8.7 Expansion Card: Wafer, 30*2P, 0.5mm (Mark No.11, J_B2B1)

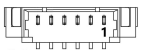
Graphic	Pin	Definition	Pin	Definition
	1	LED_PWR	31	LED_SSD
	2	LED_RUN/STOP	32	LED_ALM
	3	COM3_TXD	33	COM3_RXD
	4	COM4_TXD	34	COM4_RXD
	5	COM5_TXD	35	COM5_RXD
	6	COM6_TXD	36	COM6_RXD
	7	GND	37	GND
	8	PCIE_TX1-	38	PCIE_TX2-
	9	PCIE_TX1+	39	PCIE_TX2+
	10	PCIE_RX1-	40	PCIE_RX2-
	11	PCIE_RX1+	41	PCIE_RX2+

12	GND	42	GND
13	PCIE_CLK1+	43	N/C
14	PCIE_CLK1-	44	B2B_PECI
15	GND	45	GND
16	USB2.0-	46	SMB_SDA
17	USB2.0+	47	SMB_SCL
18	GND	48	GND
19	I2C_SDA	49	I2C_SCL
20	PANSWH_N	50	SYS_RESET_N
21	PLTRST	51	PCH_WAKE_N
22	EN_CB_PWROK	52	GND
23	RUNSTOP	53	FPGA_RST#
24	PWR_FAIL	54	CPU_EN_UPS
25	PWR_OK_CON	55	CPU_ALAM#
26	SIO_GP11	56	SIO_GP15
27	SIO_GP16	57	SIO_GP33
28	SIO_GP47	58	SIO_GP65
29	S_RTS#3	59	S_RTS#5
30	S_RTS#4	60	S_RTS#6

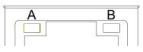
8.8 Expansion Card Power Supply: Header, 6*2P, 2.54mm (Mark No.12, J_PWR1)

Graphic	Pin	Definition	Pin	Definition
	1	DC_IN	2	DC_IN
	3	GND	4	GND
	5	VCC12	6	VCC12
	7	VCC12	8	VCC12
	9	GND	10	GND
	11	GND	12	GND

8.9 SIM Card: Wafer, 6*1P, 1.25mm (Mark No.14, J_SIM1)

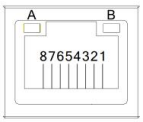
Graphic	Pin	Definition	Pin	Definition
	1	UIM1_PWR	4	UIM1_CLK
	2	UIM1_DATA	5	UIM1_RST
	3	GND	6	UIM1_VPP

8.10 GbE LAN: RJ45 Connector (Mark No.15, RJ45_1)

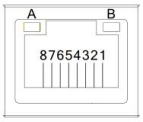
Graphic	Pin	Definition	Pin	Definition
	1	MDI0+	5	MDI2-

	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Green	B	Speed LED	1000M: Turn Green
			Only LINK: Lights On			100M: Turn Yellow
			Stop: Lights Off			10M: Lights Off

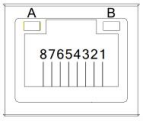
8.11 GbE LAN: RJ45 Connector (Mark No.16, RJ45_2)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0+		5	MDI2-	
	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Green	B	Speed LED	1000M: Turn Green
			Only LINK: Lights On			100M: Turn Yellow
			Stop: Lights Off			10M: Lights Off

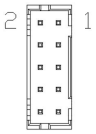
8.12 GbE LAN: RJ45 Connector (Mark No.17, RJ45_3)

Graphic	Pin	Definition		Pin	Definition	
	1	MDI0+		5	MDI2-	
	2	MDI0-		6	MDI1-	
	3	MDI1+		7	MDI3+	
	4	MDI2+		8	MDI3-	
	A	Active LED	ACT: Twinkling Green	B	Speed LED	1000M: Turn Green
			Only LINK: Lights On			100M: Turn Yellow
			Stop: Lights Off			10M: Lights Off

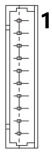
8.13 GbE LAN: RJ45 Connector (Mark No.18, RJ45_4)

<table>
<tr><th>Graphic</th><th>Pin</th><th colspan="2">Definition</th><th>Pin</th><th colspan="2">Definition</th></tr>
<tr><td rowspan="7"> 
</td><td>1</td><td colspan="2">MDI0+</td><td>5</td><td colspan="2">MDI2-</td></tr>
<tr><td>2</td><td colspan="2">MDI0-</td><td>6</td><td colspan="2">MDI1-</td></tr>
<tr><td>3</td><td colspan="2">MDI1+</td><td>7</td><td colspan="2">MDI3+</td></tr>
<tr><td>4</td><td colspan="2">MDI2+</td><td>8</td><td colspan="2">MDI3-</td></tr>
<tr><td rowspan="3">A</td><td rowspan="3">Active LED</td><td>ACT: Twinkling Green</td><td rowspan="3">B</td><td rowspan="3">Speed LED</td><td>1000M: Turn Green</td></tr>
<tr><td>Only LINK: Lights On</td><td>100M: Turn Yellow</td></tr>
<tr><td>Stop: Lights Off</td><td>10M: Lights Off</td></tr>
</table>

8.14 Front Dual USB2.0: Wafer, 5*2P, 2.00mm (Mark No.21, F_USB1)

Graphic	Pin	Definition	Pin	Definition
	1	VCC	2	VCC
	3	USB2.0_1-	4	USB2.0_2-
	5	USB2.0_1+	6	USB2.0_2+
	7	GND	8	GNE
	9	GND	10	N/C

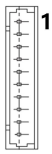
8.15 COM2: Wafer, 9*1P, 1.25mm (Mark No.22, J_COM2)

Graphic	Pin	Definition	Pin	Definition
	1	DCD	6	CTS
	2	DSR	7	DTR
	3	RXD	8	RI
	4	RTS	9	GND
	5	TXD		

Notice

*: When using COM2 Wafer, COM2 can support RS232.

8.16 COM1: Wafer, 9*1P, 1.25mm (Mark No.23, J_COM1)

Graphic	Pin	Definition	Pin	Definition
	1	DCD	6	CTS
	2	DSR	7	DTR
	3	RXD	8	RI
	4	RTS	9	GND
	5	TXD		

Notice

*: When using COM1 Wafer, COM1 can support RS232.

8.17 COM1-2 + Power on: Terminal Block, 10*1P, 3.50mm (Mark No.24, J_PB-COM1-2)

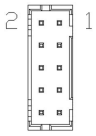
Graphic	Pin	Definition	Pin	Definition
	1	COM1_RXD/RS485+ [1]	6	GND
	2	COM1_TXD/RS485- [1]	7	UPS_OK+
	3	GND	8	UPS_OK-
	4	COM2_RXD/RS485+ [2]	9	GND
	5	COM2_TXD/RS485- [2]	10	PANSW_N

Notice

[1]: COM1 can support RS232 or RS485, selectable by “COM1 RS232/RS485 Select Jumper”. (JP1-2+ JP1-3)

[2]: COM2 can support RS232 or RS485, selectable by resistor.

8.18 Front GPIO: Wafer, 5*2P, 2.00mm (Mark No.25, J_GPIO1)

Graphic	Pin	Definition	Pin	Definition
	1	SIO_GPI81 (0xA07 Bit1, H [1])	2	SIO_GPI80 (0xA07 Bit0, H [1])
	3	SIO_GPI83 (0xA07 Bit3, H [1])	4	SIO_GPI82 (0xA07 Bit2, H [1])
	5	SIO_GPO85 (0xA07 Bit5, H [1])	6	SIO_GPO84 (0xA07 Bit4, H [1])
	7	SIO_GPO87 (0xA07 Bit7, H [1])	8	SIO_GPO86 (0xA07 Bit6, H [1])
	9	GND	10	VCC5

Notes:

[1]: “H” or “L” means the default voltage is High or Low level (5V GPIO).

8.19 Power on: Wafer, 2*1P, 1.25mm (Mark No.26, J_PB1)

Graphic	Pin	Definition	Pin	Definition
	1	Power on+	2	Power on-

8.20 Reset: Wafer, 2*1P, 1.25mm (Mark No.27, J_RST1)

Graphic	Pin	Definition	Pin	Definition
	1	SYS_RESET+	2	SYS_RESET-

8.21 CPU FAN: Wafer, 4*1P, 1.25mm (Mark No.30, CPU_FAN1)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	FAN Speed Detection
	2	VCC12 [1]	4	FAN Speed Control

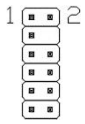
Notes:

[1]: Power on this Pin is 12V by default,12V/5V is available if specified. (resistor selectable)

8.22 Power Debug: Wafer, 4*1P, 1.25mm (Mark No.31, J_PRM1)

Graphic	Pin	Definition	Pin	Definition
	1	GND	3	VCCIN_SCL
	2	VCCIN_PE	4	VCCIN_SDA

8.23 ESPI: Header, 6*2P, 2.00mm (Mark No.32, J_ESPI1)

Graphic	Pin	Definition	Pin	Definition
	1	ESPI_IO0	2	VCC3.3
	3	ESPI_IO1		
	5	ESPI_IO2	6	ESPI_CLK
	7	ESPI_IO3	8	GND
	9	ESPI_CS0-	10	VCC3.3
	11	ESPI_ALERT0_N	12	PLTRST_N [1]

Notes:

[1]: Signal on this Pin is PLT_RST_N by default, ESPI_RST0_N is available if specified. (resistor selectable).

8.24 CMOS Battery: Wafer, 2*1P, 1.25mm (Mark No.33, J_BAT1)

Graphic	Pin	Definition	Pin	Definition
	1	VCC_BAT	2	GND

9 BIOS Setup

See “Alder Lake-N Platform BIOS User Guide” for detail information of BIOS setup.

【End】