Pin Name	Type	Note	Function
DOut1[0:6]	Output	7 bits output from benchmark design, which is the number of bits that different from the ideal result	
DOut2[0:6]	Output	7 bits output from proposed design, which is the number of bits that different from the ideal result	
Tout[0:6]	Output	7 bits output from the result of the test blocks	
BitOut1	Output	Decoded output from benchmark design	
BitOut2	Output	Decoded output from proposed design	
Start1	Output	Signal to indicates the beginning of each frame for benchmark design	Start=1, new frame begins
Start2	Output	Signal to indicates the beginning of each frame for proposed design	
KeepShift	Output	Signal to indicates the state of the shift registers	KeepShit=0, keep data; KeepShit=1, shift data
TestReady	Output	Signal to indicates the state of the test blocks	TestReady=1, data is ready, start to testing
Dclk	Output	Output of the divided clock signal	
In[0:6]	Input	7 bits input	
Mode	Input	Signal to select the working mode between decoder and testing	Mode=1, run decoder; Mode=0, run test blocks
S1 S2 S3	Input	Signals to select different blocks to be tested	[S1,S2,S3]=XX0, wire only; [S1,S2,S3]=001, benchmark; [S1,S2,S3]=101, proposed; [S1,S2,S3]=011, pipelined; [S1,S2,S3]=111, BTWC
Enable_f	Input	Signal to enable or disable clock dividing	Enable_f=0, no clock dividing; Enable_f=1, use clock dividing
Sel_f	Input	Signal to select the dividing clock between 1/2 or 1/4	Sel_f=0, Dclk=1/4 Clock; Sel_f=1, Dclk=1/2 Clock
Go	Input	Signal to enable the running of the whole system	Go=1, run system
Clock	Input	Input clock signal	
nReset	Input	Input nReset signal	