Computer Architecture (CSE511/ ECE 511) Assignment 1

1. Create a configuration script to simulate the system given in the figure below. Run a benchmark application, "qsort_small from MiBench benchmark suite [1]" in system emulation mode. Unless otherwise specified, the configuration of caches is as given; L1 Data Cache (size = 16kB, Associativity = 2, latencies = 2); L1 Inst Cache (size = 16kB, Associativity = 2, latencies = 2); L2 Cache (size = 256kB, Associativity = 4, latencies = 10).

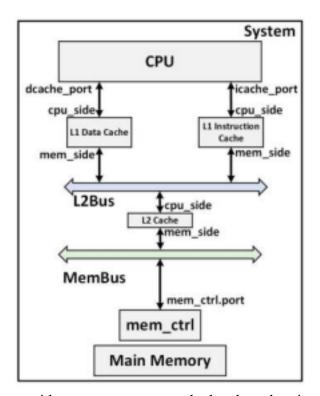
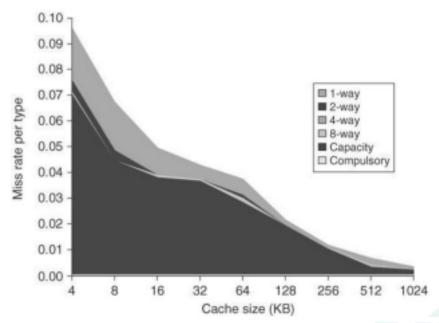


Fig. 1: A system architecture with a processor, two cache levels and main memory. The memory hierarchies are connected by buses.

2. Perform experimental simulations by changing L2 cache configurations on the above system with "qsort_small" benchmark to achieve a similar plot in Fig.2 below. For your convenience, we have provided a few sets of configurations in Table 1. You can extend the set of configurations to have a better understanding.



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Fig.2. Variation in Cache Miss Rate with different cache sizes and associativity.

L2 Configurations (size_associativity)	L2 Configurations(size_associativity)
64kB_2	1024kB_8
64kB_4	1024kB_2
256kB_2	32kB_4
256kB_4	64kB_8

Deliverables:

- 1. The assignment requires you to make observations on the L2 cache miss rate statistics report generated by each configuration as you change the cache configurations.
- 2. Submit the following:
 - a. Configuration script for the system given in question 1.
 - **b.** A graph (as shown in Figure 2) with the cache configurations you have considered and simulated on gem5. (list all the configurations in a table).
 - c. Explain your observations from the experiment performed in question 2.

Note: 2.b and 2.c should be uploaded in a single pdf. The python script should be kept separately in the same folder. All these should be zipped with folder name <your_name_roll_number_SA1> and uploaded in the classroom. Do not forget to "TURN IN" your assignment.