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14. ABSTRACT
Report developed under SBIR contract for topic A17-098. To address the Army's need for a squad-level system to detect and counter unmanned aircraft systems (UAS), during this Transition to Phase II period, Intellisense Systems, Inc. (ISI) advanced the development of the Portable Anti-UAS (PAN-UAS) device proven feasible in Phase I. The PAN-UAS device uses a new design that combines state-of-the-art high frame rate airspace monitoring technology utilizing the latest advances in radar, including digital beam-forming, all-digital scanning multiple-input, multiple-output (MIMO) radar with a machine learning micro-Doppler analysis algorithm for rapid identification of small UAS targets. PAN-UAS is able to automatically detect and counter multiple UAS targets using low-power, wide field-of-view scanning radar detection and a wide-beam RF jammer that uses low duty cycle and narrowband waveforms to achieve high peak power. Ruggedized, integrated components and solar-powered batteries allow PAN-UAS to operate continuously outdoors in a wide variety of weather and atmospheric conditions. During this Transition to Phase II period, ISI completed the architecture design and prepared a foundation for successful execution of Phase II. As a result, in Phase II, ISI will develop and produce a fully integrated prototype for use in live demonstration against UAS, reaching technology readiness level (TRL)-5.

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Portable Anti-UAS Device (PAN-UAS)

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1.0 SUMMARY

During the Transition period between Phase I and Phase II of the Portable Anti-UAS (PAN-UAS) device development, Intellisense Systems, Inc. (ISI) updated the system architecture and completed the high-level design of the radio frequency (RF) module. The radar was switched from the originally proposed S-band to C-band, which provides a more compact and accurate unmanned aircraft system (UAS) detection solution. This improvement enabled a more robust design of the multiple input, multiple output (MIMO) antenna array within the required volume of <100 $in.^3$.

Modeling of the radar digital signal processing (DSP) algorithm was completed in MATLAB® and Simulink®. This algorithm is based on ISI's proven MIMO radar algorithm, which was tested in autumn of 2018. Leveraging our experience in design of a vehicle-based counter-UAS radar system (see Appendix) will enable us to start development of the PAN-UAS device in Phase II without demonstrating the prototype as originally planned for the Transition period. Instead, ISI completed analysis of the computational throughput and storage requirements and confirmed the choice of a high-performance commercial off-the-shelf (COTS) module (based on Xilinx® Zynq® UltraScale+™ MPSoC) for digital processing. Our analysis shows that a single multi-processor system-on-chip (MPSoC) module will be able to support 4×16 MIMO digital processing of the radar and the system control operation.

The updated development plan for Phase II (see Figure 1) is based on concurrent development and incremental integration and testing of the PAN-UAS sub-systems, thus reducing the technical risks and enabling early validation and quick turnaround of the critical modules (e.g., antenna) prior to their integration in the system prototype.

These results provide a solid foundation for a successful launch of Phase II development immediately after completion of the Transition period.

2.0 INTRODUCTION

To address the Army's need for a squad-level system to detect and counter unmanned aerial systems (UASs), Intellisense Systems, Inc. (ISI) is developing a new Portable Anti-UAS (PAN-UAS) device that combines state-of-the-art airspace monitoring technology with novel UAS countermeasure approaches and packages them in a man-packable system. Innovations in power reduction, miniaturization, and ruggedization of radar detection and radio frequency (RF) jamming systems ensure the PAN-UAS device is self-contained in a very portable form factor and can detect and counter both individual and swarms of UASs, directly addressing Army requirements.

To facilitate the Phase II development, during the Transition period we refined the PAN-UAS system architecture and development plan. In the Transition period, ISI defined the PAN-UAS system architecture, developed a MATLAB®/Simulink® simulation model, and began development of the antenna and RF module. In Phase II, ISI will develop the PAN-UAS device prototype, including the electronic circuits, embedded software, and mechanical enclosure, evaluate its performance, and demonstrate its operation.

3.0 METHODS, ASSUMPTIONS, AND PROCEDURES

ISI reviewed the PAN-UAS system architecture defined in Phase I and applied lessons learned from relevant counter-UAS radar development projects. We optimized the system architecture to provide the specified functionality while meeting the size, weight, power, and cost (SWaP-C) requirements.

We prepared a high-level design of the critical system modules and interfaces. The detailed block diagrams of the RF module with selected main components will allow for rapid development of the RF printed circuit board (PCB) schematics.

To validate our assumptions for computation throughput and size of the radar signal processing module, we developed a detailed Simulink® model of the PAN-UAS radar digital signal processing (DSP) algorithm and mapped it into a field-programmable gate array (FPGA) system-on-chip (SoC).

We also updated the development approach and performance schedule to allow for incremental integration. In Phase II we will build and test 3-4 revisions of RF and antenna modules (the critical components) and two revisions of prototypes with the final revision in the target form factor ready for technology readiness level (TRL)-5 testing.

4.0 RESULTS AND DISCUSSION

During the Transition period, ISI completed Task 1, planned the activities of Tasks 2 and 3 (see Figure 1), and started Task 5. By defining the system architecture, we reached Milestone 1. The results of this effort are presented and discussed in the remainder of this section.

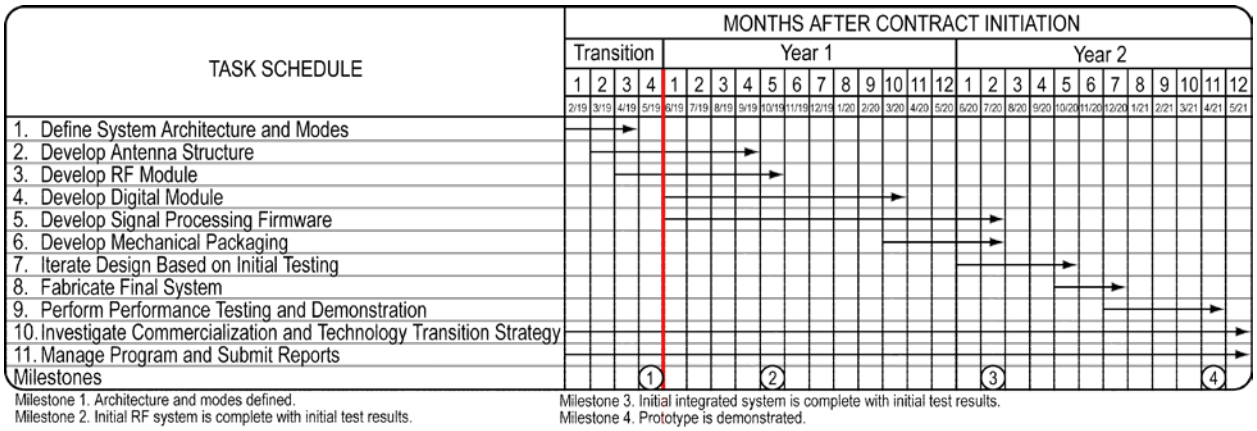


Figure 1: Milestone schedule

4.1 Frequency Band Selection (Task 1)

The PAN-UAS design approach is operation in the C-band, as it provides a more compact and accurate UAS detection solution than the originally proposed S-band. Table 1 compares these two bands for the multiple input, multiple output (MIMO) radar design. Fast frequency-modulated continuous wave (FMCW) radars operating at higher frequencies (X-band, Ku-band, etc.) have range-Doppler ambiguity problems and high complexity of planar antenna aperture designs. Physics dictates that lower frequencies (with longer wavelengths) do not allow for compact antenna designs that are necessary to meet the Army's requirements.

Table 1: PAN-UAS Radar Frequency Band Selection

Parameter	S-Band	C-Band	Notes
Aperture Size	Marginal for Compact Radar System	Compact MIMO Configuration	Longer wavelength S-Band and antenna aperture constraints result in a MIMO antenna design with very short distance between TX and RX antenna elements. This approach requires TX/RX leakage compensation and may result in antenna pattern distortion and higher power consumption.
MIMO Design Flexibility	Limited	Flexible	
Doppler Resolution for 0.1 s coherent time	0.41 m/s	0.26 m/s	Doppler resolution is very critical for detection of small UAS in cluttered environments.
Power Consumption	Low	Moderate	Larger receive antenna area allows for lower power transmitters for S-band. The higher power of C-band transmitters will be compensated by smart power management.

The selection of C-band has enabled us to redesign the 4×16 MIMO antenna array structure to increase the distance (and decrease the leakage) between the transmit (TX) and receive (RX) arrays. Figure 2 illustrates the 4×16 MIMO antenna design that will be implemented as a microstrip patch array and also incorporates a wide-beam jamming antenna. The wavelength for

the radar carriers at 5.7 GHz frequency is λ = 52.6 mm, which enables smaller antenna arrays and larger distance between TX and RX elements, minimizing the leakage.

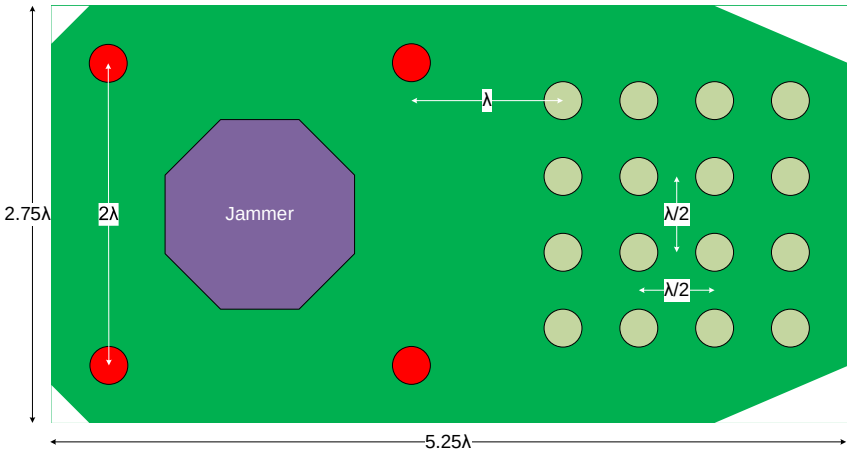


Figure 2: PAN-UAS 4×16 MIMO antenna array with the wideband jamming antenna

4.2 Requirements of Radar Antenna Array Design (Tasks 1 and 2)

The antenna requirements were defined as follows:

- Type: MIMO, 4×16 (4 transmit elements, 16 receive elements)
- Antenna element type: patch
- Feed: All antenna elements have individual via-type feeds
- PCB material, thickness: Capable of multilayer microstrip design (radar front-end surface-mount device (SMD) components are placed on the back side of the antenna board)
- Polarization: linear, horizontal
- Central frequency: 5.8 GHz
- Operational bandwidth: 200 MHz (T), 300 MHz (O)
- Return loss over the bandwidth: <-10 dB (T), -15 dB (O)
- Isolation between transmit and receive elements: more than 40 dB
- Single element gain: 5 dB or more
- -3 dB beamwidth for single element: 90° or more in horizontal and vertical planes
- -3 dB beamwidth for 16-element array: 30° or less in horizontal and vertical planes.

Based on the above requirements, in Phase II we will design the antenna using a high-frequency structure simulator (HFSS) antenna development tool. This task (#2) will include design, simulation, and optimization of transmit and receive elements of the MIMO antenna (Figure 2) to determine the element size and shape and the feed location.

We plan to use a consultant with whom we have collaborated in the past for executing antenna simulation task and we have requested the Army's approval for reallocating funds from external services to the consultant's fees.

4.3 Definition of Jamming Frequencies (Tasks 1 and 2)

Another improvement in the PAN-UAS design approach is the use of three different wideband antennas for jamming the following frequencies:

- 2.4 GHz (commonly used for small UAS communication and control) – dedicated jammer antenna integrated within the MIMO antenna aperture (purple octagon in Figure 2)
- 5.9 GHz – radar transmit antenna
- GPS (L1 – 1575.42 MHz, L2 – 1227.60 MHz), GLONASS (L1 – 1620 MHz, L2 – 1246 MHz), and GALLILEO (E1 – 1575.42 MHz, E5 – 1176.45/1207.14 MHz, E6 – 1278.75 MHz) frequencies – a single dedicated external wideband jammer antenna.

The PAN-UAS jammer design is discussed at the end of Section 4.4.

4.4 Development of System Architecture (Tasks 1 and 3)

ISI refined the system architecture by updating the RF module system diagram and selecting the main components. Figure 3 depicts the PAN-UAS radar sub-system architecture with main components and interfaces. The external monitor is optional and will be used in the PAN-UAS prototype test setup.

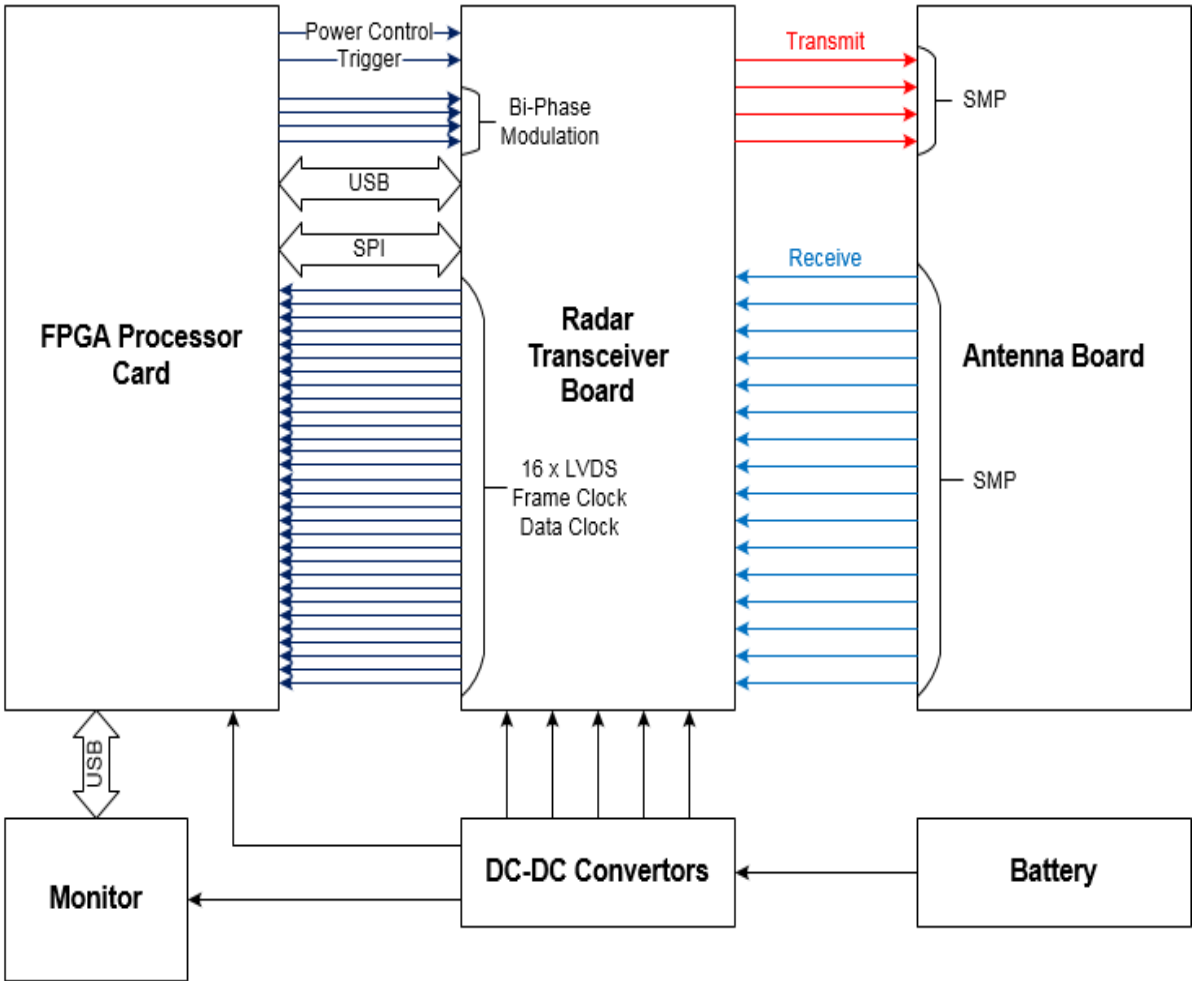


Figure 3: High-level architecture of the PAN-UAS radar sub-system

The RF transceiver module and the antenna array are the critical modules that will be developed by ISI. We prepared a detailed block diagram of these modules (see Figure 4).

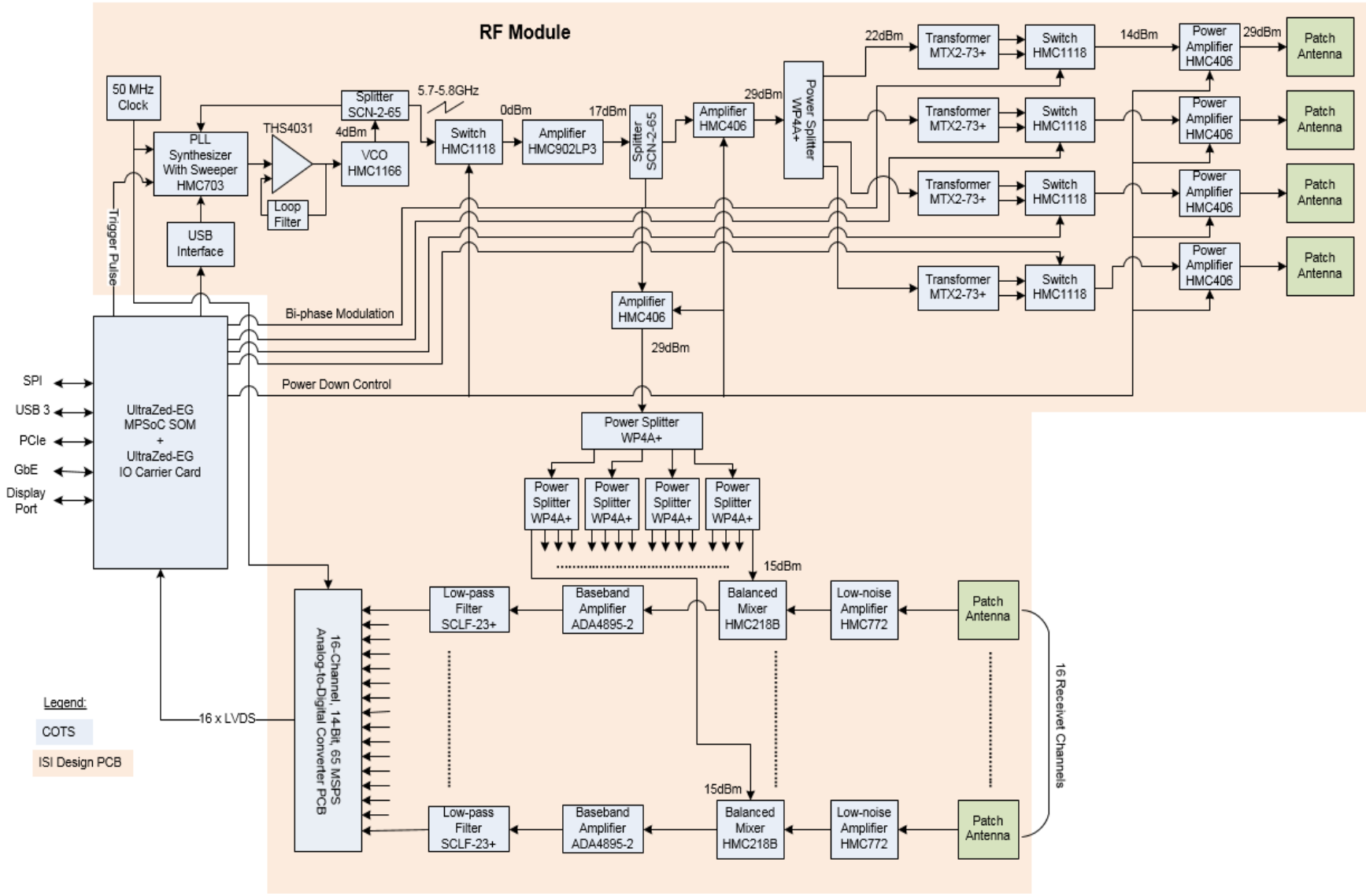


Figure 4: Block diagram of the RF module

The final prototype will have a single multilayer RF PCB with patch antenna arrays on the top side and transceiver components on the bottom side. Although using a single PCB would be more compact, less expensive, and more reliable, using separate antenna and RF PCBs in the first prototype during the radar development and optimization phase will enable us to reach full functionality faster and at lower development cost.

For the first radar prototype, we will implement separate boards for the patch antenna arrays and RF front-end. The two PCBs of similar size will be located in parallel with the gap of <1 in. (necessary for assembly with coax cables). We plan to use SMP Snap-On connectors (e.g. Amphenol SMP-MSLD-PCS) on the both RF boards. Twenty 3-in. coax cables with SMP right-angle 180°-rotated connectors (such as Mini-Circuits 047-SMPRC+) will connect antenna elements (4 TX and 16 RX) to the corresponding transceiver circuits (as shown in the floor plan in Figure 5).

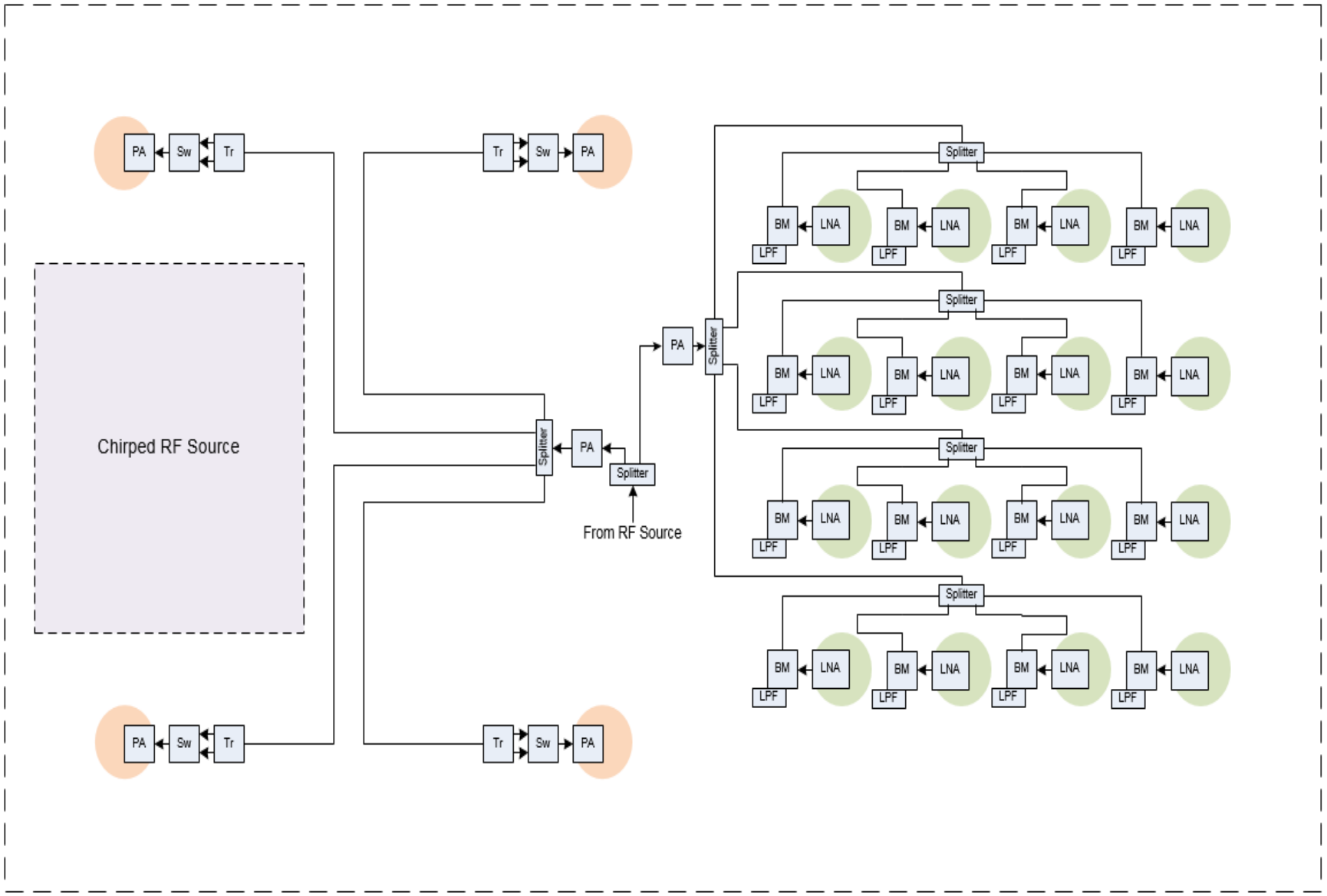


Figure 5: Radar antenna - RF transceiver plan

The PAN-UAS jammer will utilize its radar frequency (5.8 GHz) proximity to mobile Wi-Fi 5,850-5,925 MHz band (802.11p), which is likely used for drone control. In this jammer mode, the radar frequency will shift up 100 MHz and the radar will transmit a jamming signal.

To cover the GSM and Wi-Fi frequency bands used for UAS satellite navigation, communication and control, the PAN-UAS jammer will operate in 0.7-2.7 GHz band. We developed a concept block diagram for the jammer operating in this frequency band – see Figure 6.

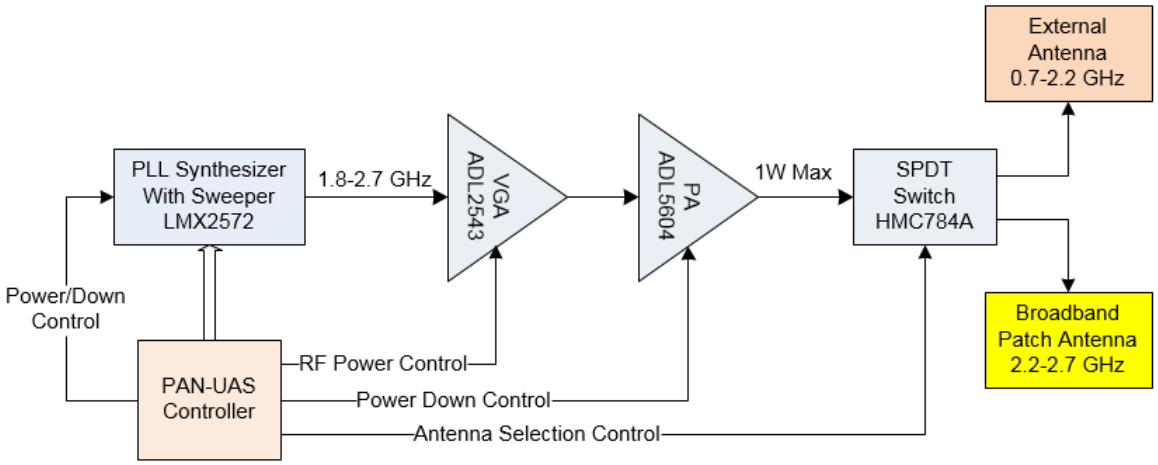


Figure 6: PAN-UAS jammer concept block diagram

The jammer frequency source is a lower power wideband LMX2572 PLL synthesizer with flexible frequency sweep capability in an ultra-wide frequency band: 12.5 MHz to 6,400 MHz. RF power is controlled by using the ADL2543 variable gain amplifier (VGA). The ADL5604 power amplifier (PA) provides up to 1 W output power in the 700-2,700 MHz bandwidth with excellent 50% PAE (power added efficiency). All the jammer components can be turned on or switched to power down mode in microseconds. We will place a broadband jammer antenna on the radar RF PCB (see Figure 2), which will cover the 2.2-2.7 GHz band used for control and communication by the majority of commercial small UAS. For lower frequencies (0.7-2.2 GHz) we will provide a port for an external broadband antenna designed specifically for 0.7-2.2 GHz bandwidth.

4.5 Development of DSP Algorithm (Task 1)

We developed the PAN-UAS simulation models. The MATLAB® DSP model is based on ISI's fast FMCW MIMO radar architecture, which has been adapted to the PAN-UAS requirements (Figure 7).

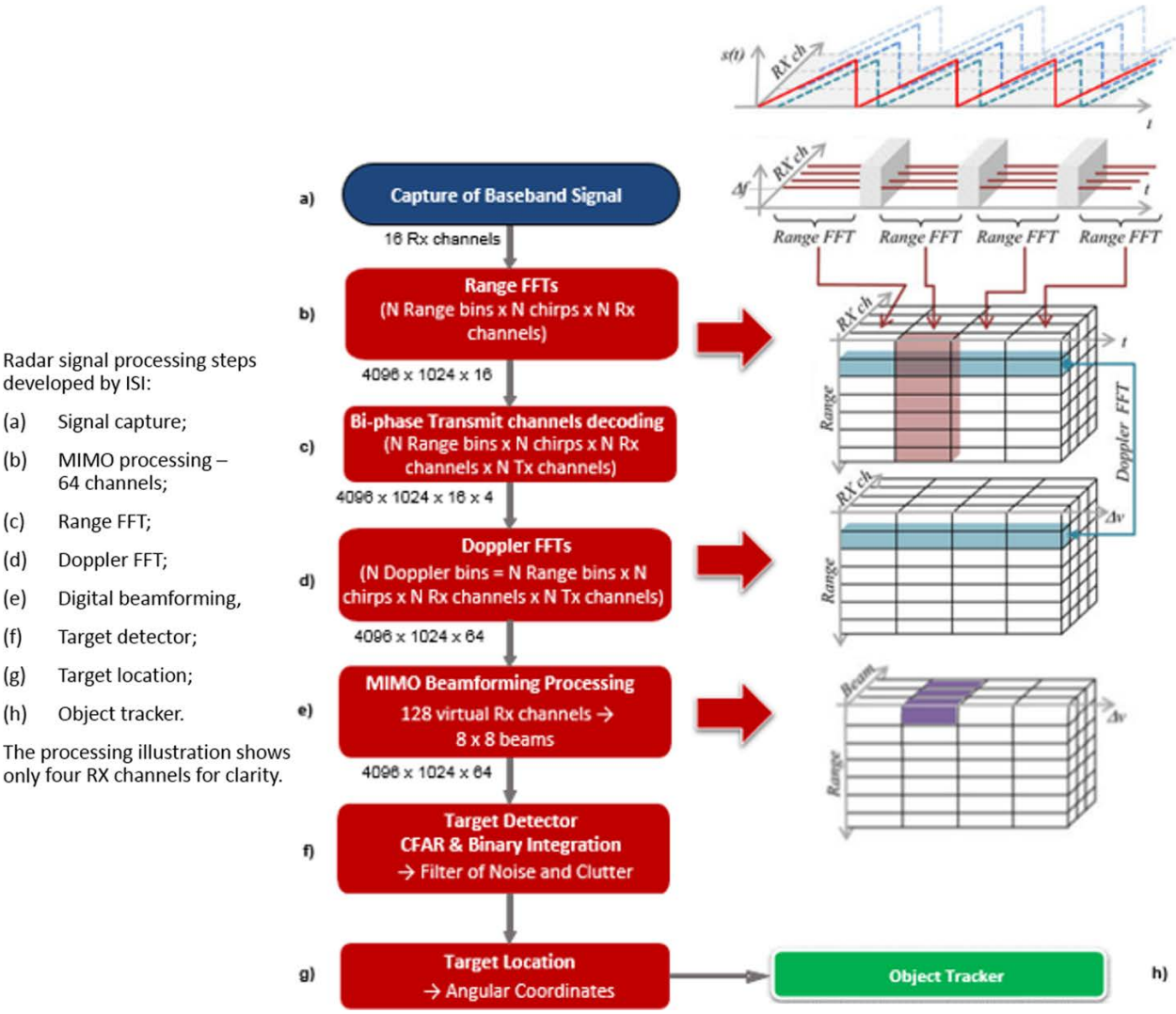


Figure 7: PAN-UAS DSP algorithm (illustration)

4.6 Development of Simulink Model (Tasks 1 and 5)

Unlike the MATLAB® algorithm model, the Simulink model is timing-accurate and enables analysis of computation throughput and latency as well as implementation tradeoffs. We developed the Simulink model of the PAN-UAS radar DSP algorithm. Figure 8 shows the partial Simulink model that includes processing of the digitized data and two Fast Fourier Transform (FFT) computations representing the range and Doppler stages.

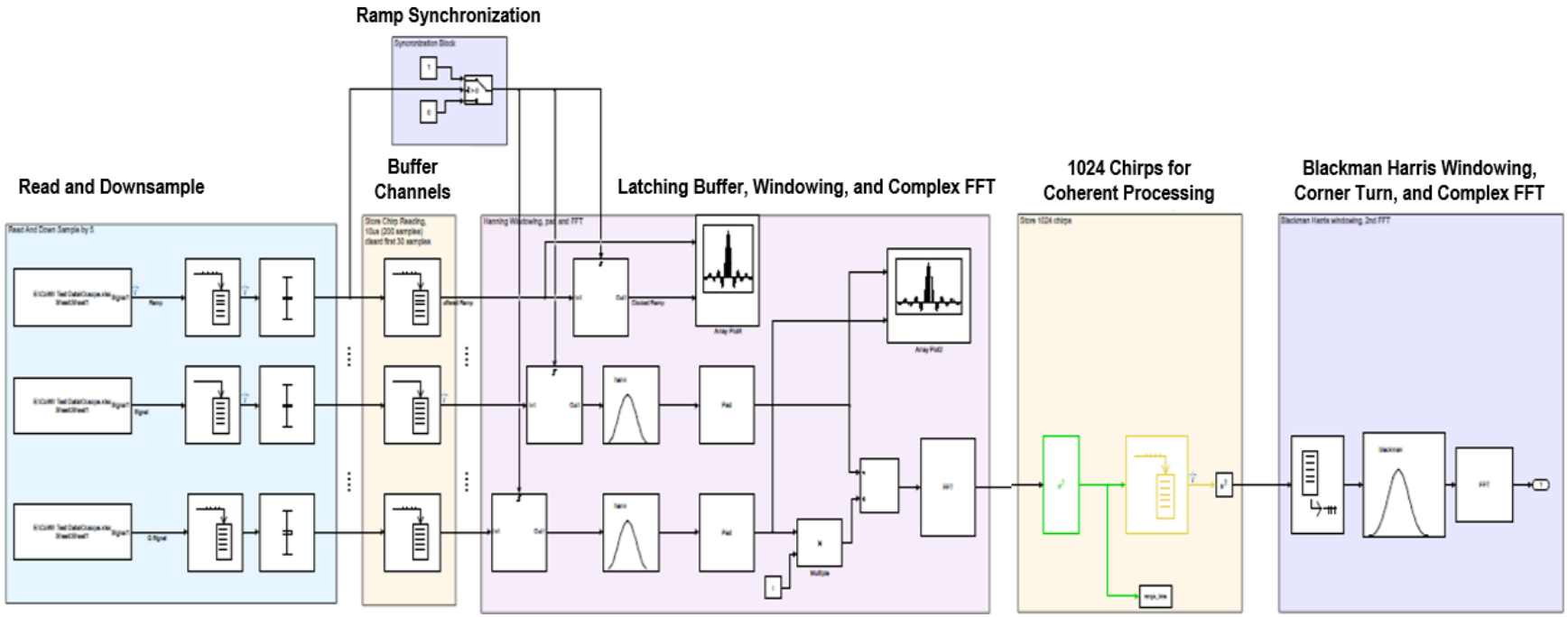


Figure 8: Partial Simulink model of the PAN-UAS DSP algorithm

In Task 5 we will map the optimized DSP algorithm into a Xilinx multi-processor system-on-chip (MPSoC) on a commercial off-the-shelf (COTS) system-on-module (SoM) in the Digital Module by using MathWorks® and Xilinx® tools. In the Transition period we mapped the partial algorithm in the MPSoC on the ZC706 Evaluation Board and received estimates of hardware acceleration engines' sizes and performance (see Section 4.8). In Phase II we will map the optimized DSP algorithm into a Zynq® UltraScale+™ MPSoC with more resources and circuits that operate at higher speeds. At 16 nm, the UltraScale+™ devices currently provide the highest performance and integration capability at reduced power consumption versus other products, and they are capable of supporting the PAN-UAS computation throughput.

In Phase II the Simulink model of the DSP algorithm will also serve as a bit-accurate reference model for verification of the FPGA-based implementation of this algorithm.

We completed the optimization of the partial Simulink® model and completed mapping of the DSP algorithm into the FPGA by using a MathWorks-Xilinx® tool flow. This methodology will shorten the development cycle of the FPGA-based Zynq® MPSoC and enable quick turn-around for refinement of the design in Phase II.

4.7 Analysis of Computation Precision (Task 1)

We performed an initial analysis of the required precision for the MIMO radar DSP computation. The DSP algorithm developed by ISI in MATLAB® uses floating-point arithmetic. Typical implementations of the DSP algorithms for high data throughput systems like radar use fixed-point arithmetic to enable high clock frequency that shortens the computation latency and minimizes the required hardware resources and power consumption. However, the standard 16-bit fixed-point arithmetic with block floating-point FFT implementation reduces the processing gain of the MIMO radar algorithm, decreasing the system's ability to detect targets in the presence of clutter.

Therefore, we determined that the PAN-UAS DSP algorithm should use 32-bit fixed-point arithmetic to achieve the required system performance. The Simulink® model that is being mapped into the MPSoC already includes the fixed-point 32-bit computation and memory blocks.

4.8 Computation and Storage Requirements (Task 1)

We estimated the memory and computation throughput requirements for implementation of the DSP algorithm (Table 2). The clock period corresponds to 105-123 MHz frequency, which is <¼ of the maximum frequency of DSP slices (500 MHz) in Zynq® UltraScale+™ devices. The number of DSP slices required to meet the computation throughput for 100 ms frame is <600, which is much lower than the ~2,000 for the largest Zynq® device that incorporates 8.8 MB of Block Random Access Memory (RAM).

Table 2: PAN-UAS DSP Computation and Storage Requirements (Preliminary)

	Number of Cycles	Clock Period	Storage
4096-point Real FFT (100 µs)	12,300	<8.2 ns	16 KB
Array 1024×2048 (100 ms)	10,500,000	<9.5 ns	16 MB
64 virtual channels × 16 MB			1 GB

The external memory used to store the frame data during processing will be at least 2 GB. An UltraZed-EG™ SoM has 2 GB and Trenz SoMs are available with 4 GB DDR4 SDRAM (see Figure 9).

Figure 9: UltraZed-EG™ SoM MPSoC module with Zynq® UltraScale+™ XCZU9EG-1FFVC900E, 4 GB DDR4, size 52×76 mm

4.9 UAS Identification (Tasks 1 and 5)

ISI defined the design approach to micro-Doppler signature analysis that will be used in the identification algorithm. We analyzed the most effective way to use machine learning for UAS identification and discrimination from birds using the latest research findings.

We studied the latest research in micro-Doppler signature analysis, specifically covering three main topics: classification, recognition, and identification. At this stage we focused on classification of signatures (see Figure 10).

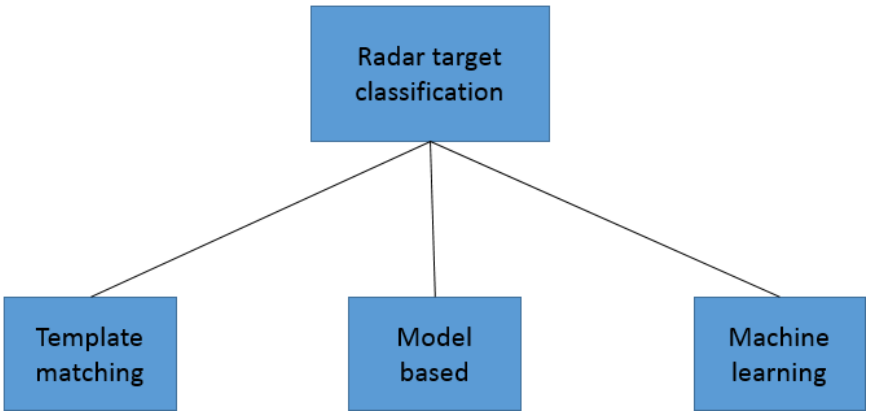


Figure 10: Radar target classification methods

We also compared clustering algorithms and identified Highly-Parallel Density-Based Spatial Clustering of Applications with Noise (HPDBSCAN). HPDBSCAN, deep (machine) learning, and a number of techniques for feature extraction will be used. We will also explore wavelet-based clustering. To evaluate these algorithms, we will need radar data that will be collected using the first prototype developed in Phase II. The defined approach to target classification and identification will enable us to develop the algorithm in Task 5. The algorithm will be executed by the ARM processor embedded in the MPSoC with potential use of hardware acceleration.

4.10 High-Level RF Module Design (Task 3)

ISI refined the system architecture by updating the RF module system diagram and selecting the main components. Figure 11 shows the latest high-level block diagram of the RF module that is integrated with the antenna. We added detailed high-level schematics of the chirped source (Figure 12), transmitter (Figure 13), and receiver (Figure 14). This resulted in the improved RF sub-system block diagram shown in Figure 11.

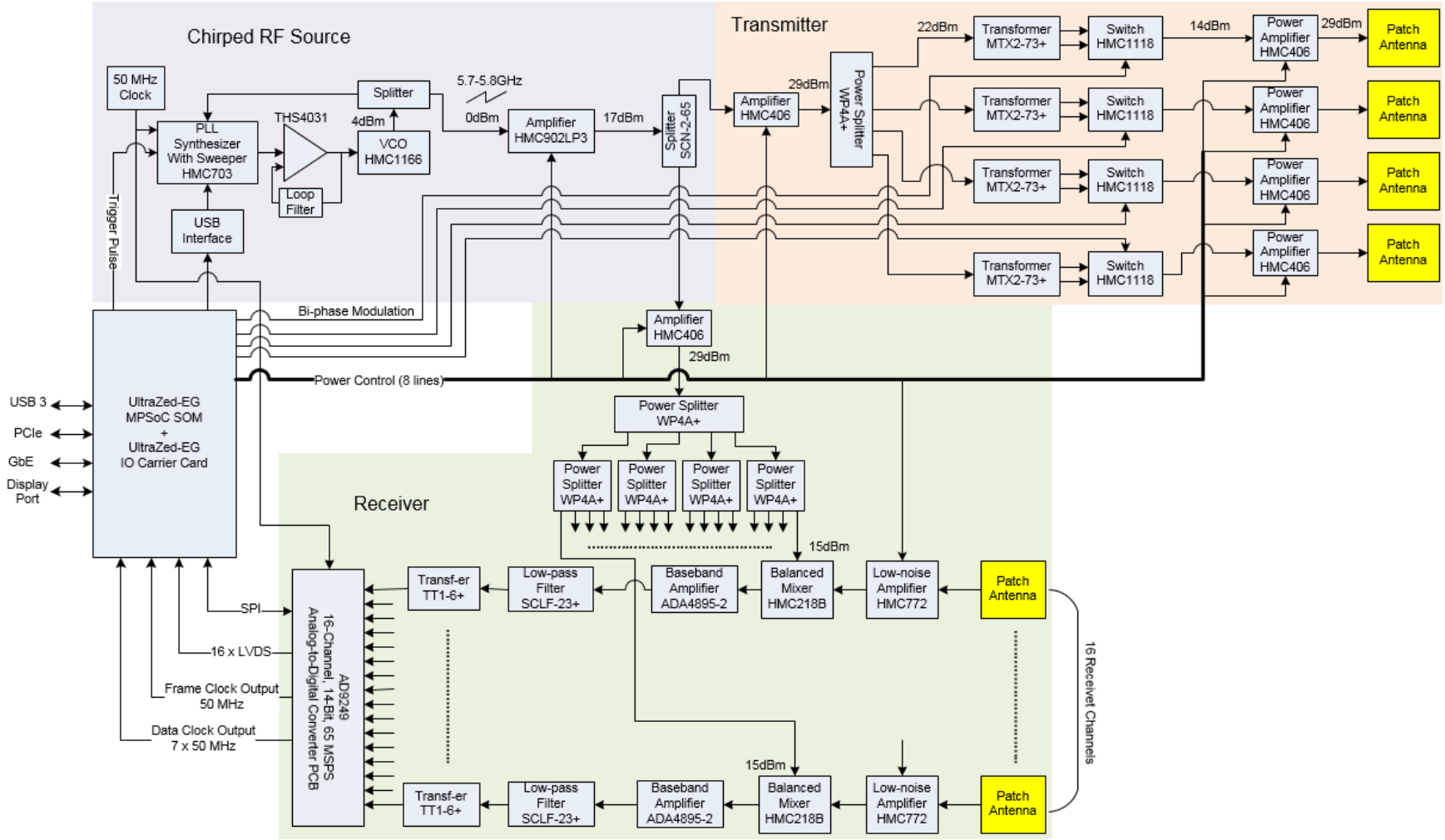


Figure 11: RF module block diagram

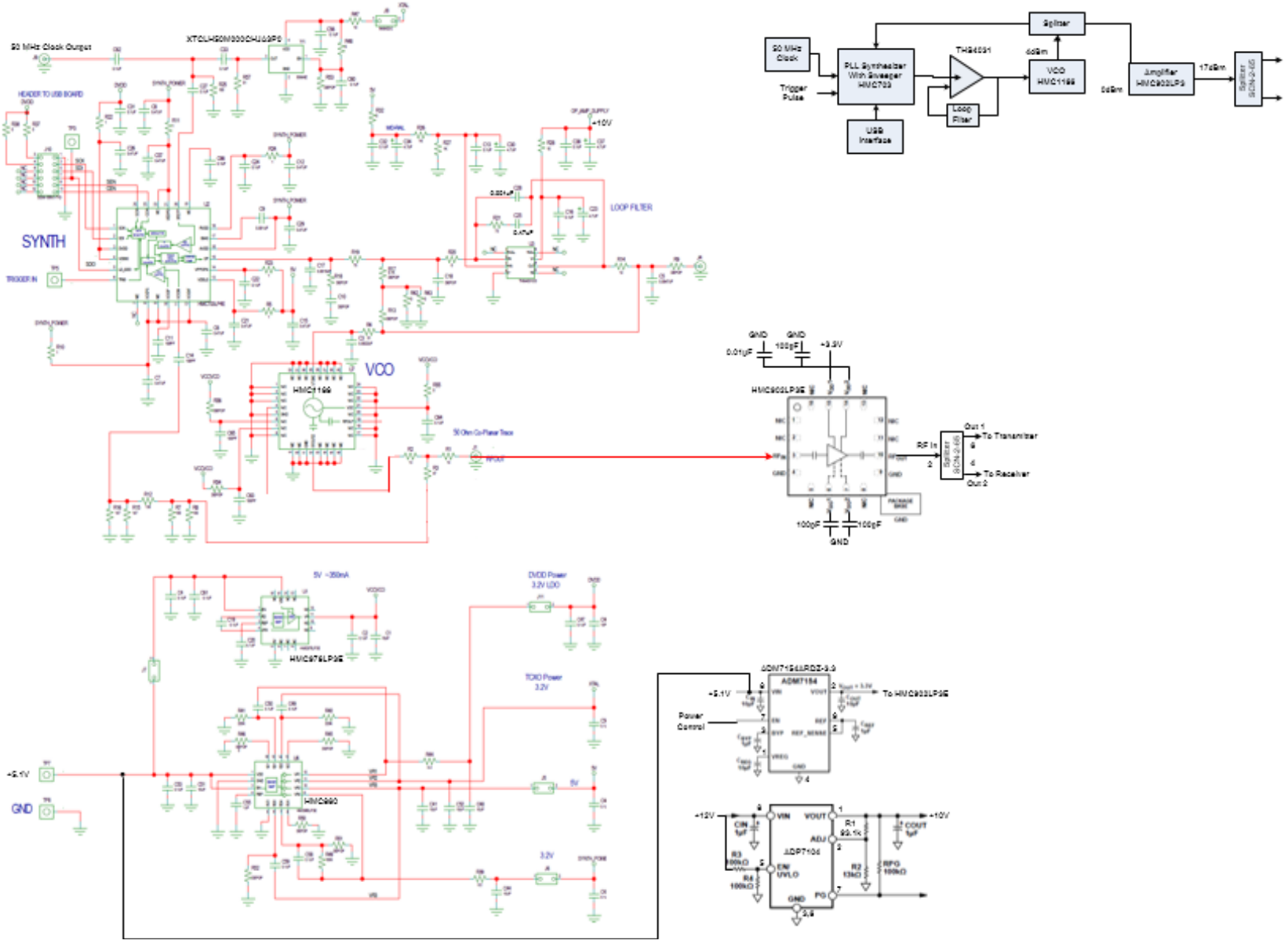


Figure 12: RF module – chirp RF source

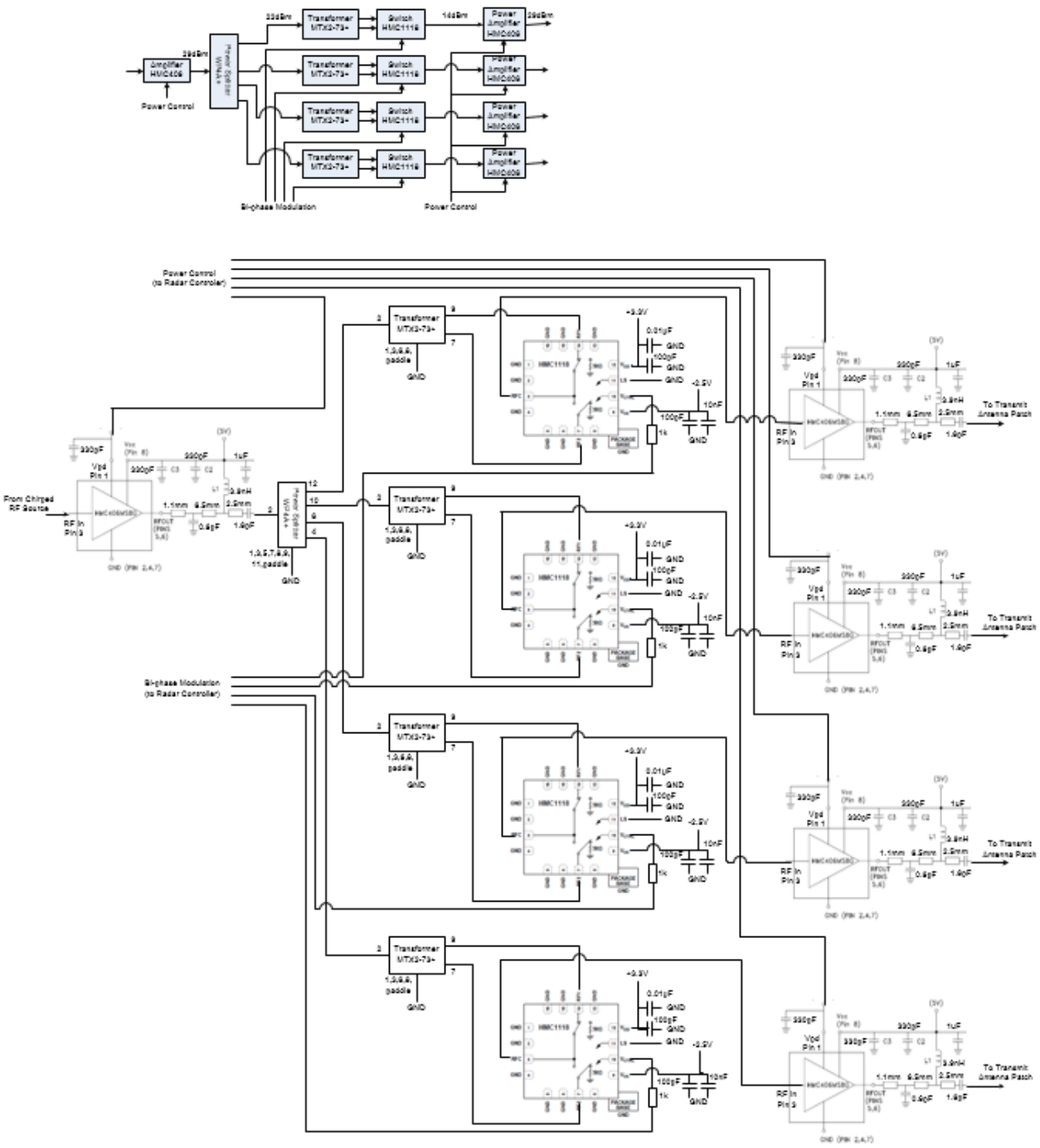


Figure 13: RF module – transmitter

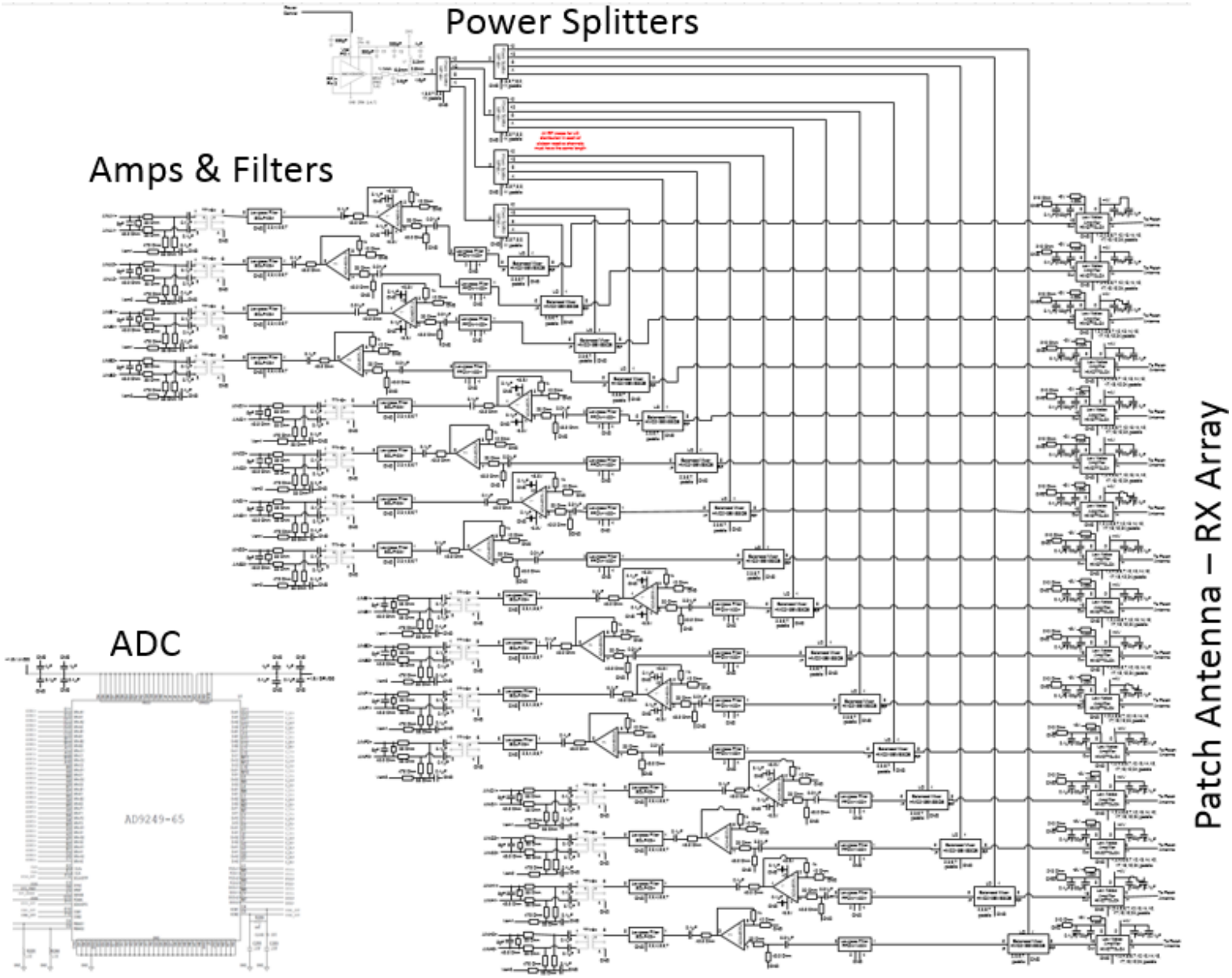


Figure 14: RF module – receiver

We also detailed the DC power distribution and control circuits. The DC power supply system includes a rechargeable lithium battery, high efficiency DC/DC convertors (Figure 15), and low dropout (LDO) linear regulators (Figures 16 and 17).

The compact (5.88×3.50×0.78 in.^{3}) DR202X lithium battery has a high enough voltage (11.1 V) to be directly connected with DC/DC (minimum input voltage is 9 V) and a sufficient capacity (7.8 Ah or 87 Wh) to feed the radar for >3 hours in continuous operation mode and >24 hours when operating with a typical optimized duty cycle (see Table 3). Using a low-power MIMO option (proposed in Section 6.0) would allow for 4.5 hours of continuous operation.

Table 3: Top-level Power Analysis of PAN-UAS System

Mode	Power Consumption	Frequency of Use
Low-Power Sentry	1 W	88%
Full-Rate Scanning	26 W	10%
Scanning and Jamming	32 W	2%
Weighted Average	**3.45 W**	

Four different DC/DC converter units from CUI, Inc. and X-Power provide five different output voltages (+12 V, +5.1 V, ±5 V, and 3.3 V), which are needed for the radar power supply. These voltages are supplied to the low noise LDO linear regulators placed on the radar transceiver board.

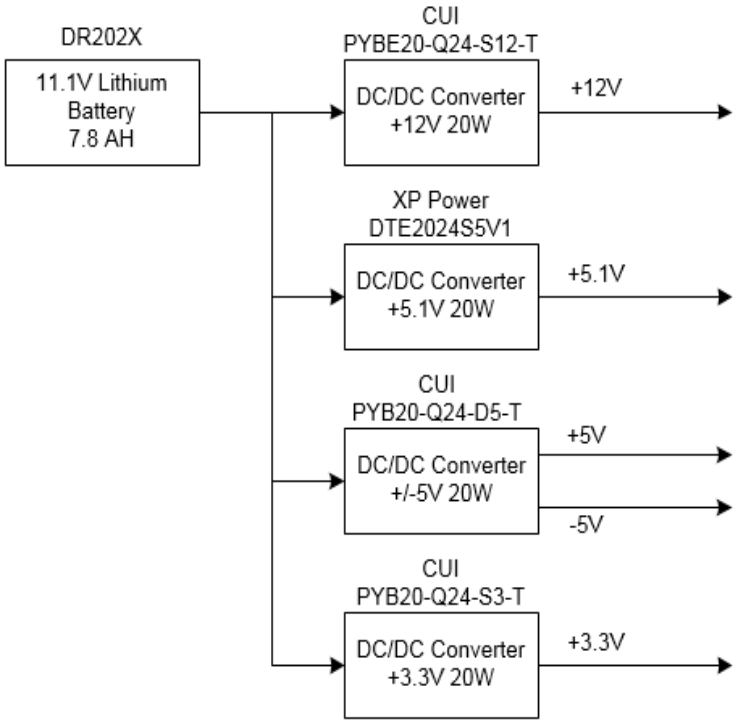


Figure 15: Block diagram of the power supply module

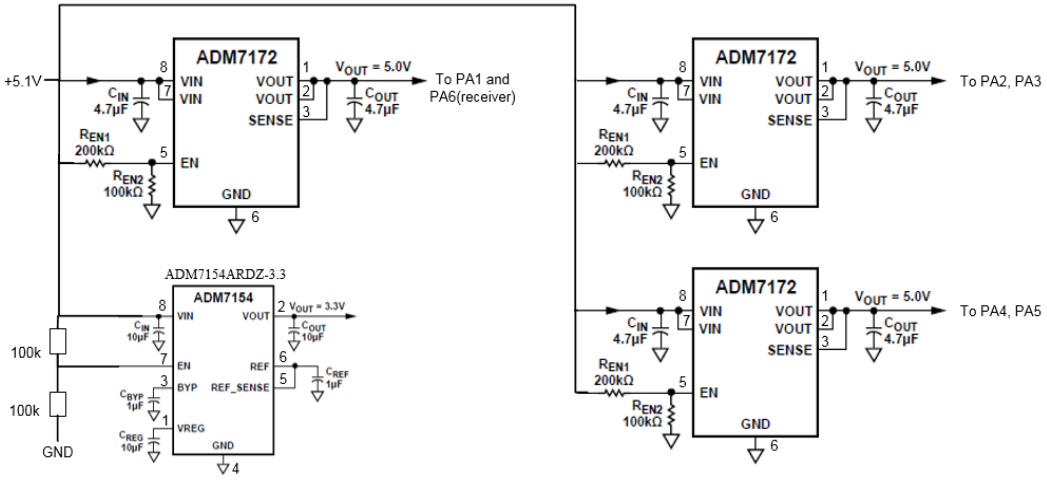


Figure 16: LDO linear regulator schematic for transmitter

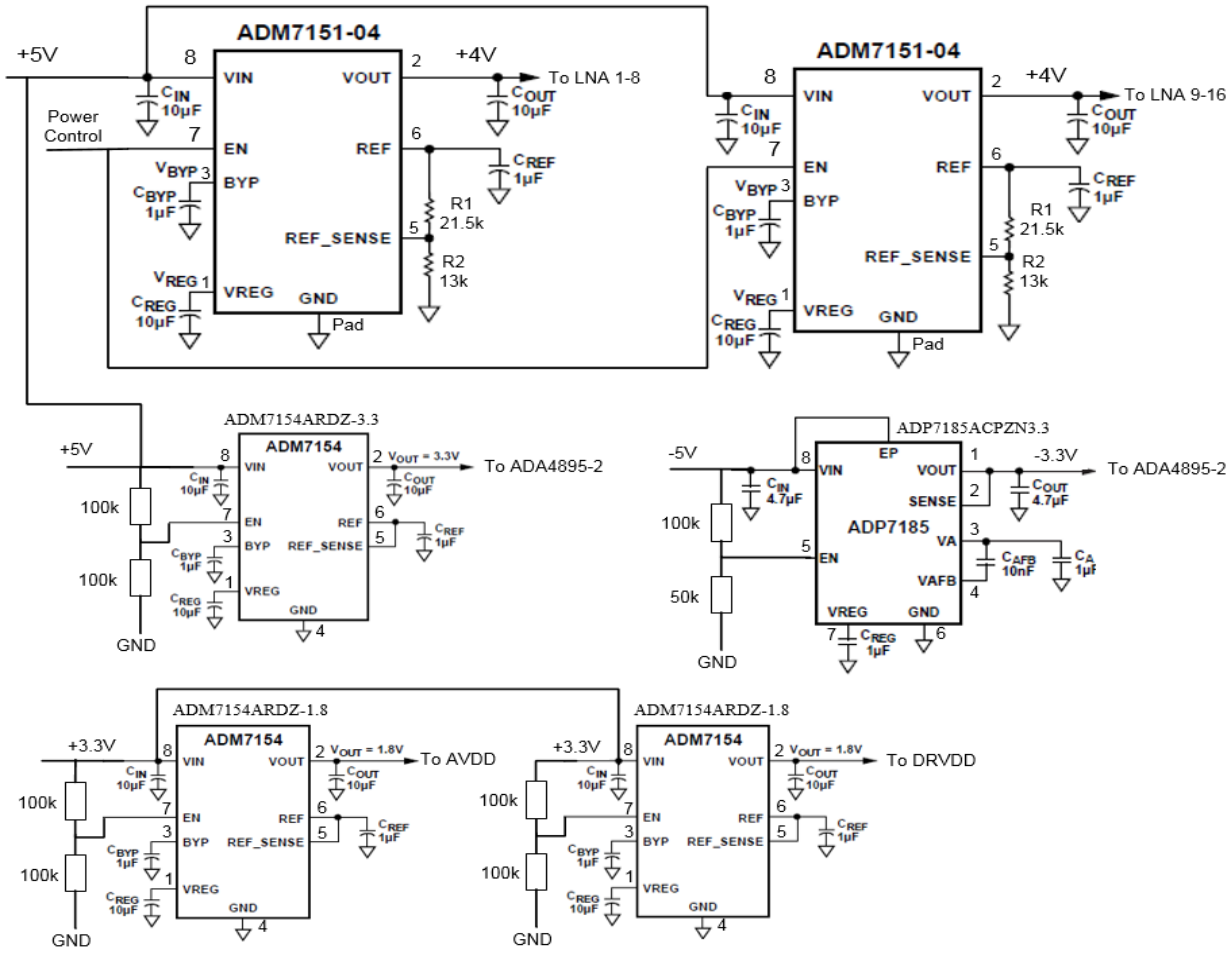


Figure 17: LDO linear regulator schematic for receiver

5.0 CONCLUSION

During this Transition period between Phase I and Phase II, ISI updated the Phase II development plan and schedule based on ISI's recent experience in developing counter-UAS MIMO radar systems. We reviewed and refined the PAN-UAS system architecture and completed high-level design of the radar RF module. We reviewed and updated the radar DSP algorithm, prepared MATLAB® and Simulink simulation models, and completed mapping of the partial DSP algorithm in a Xilinx® MPSoC. This effort validated the design methodology based on MathWorks and Xilinx® tools that enable a quick turnaround of the design and verification.

All of the findings and results of our analysis and development in the Transition period confirmed the feasibility of the proposed Phase II approach to implementing the PAN-UAS functionality while meeting the Army's SWaP-C requirements and addressing the concept of operations (CONOPS) as well as broader counter-UAS applications. The successful completion of the Transition period will enable ISI to execute development of the PAN-UAS during the Phase II performance period.

6.0 RECOMMENDATIONS

Based on our development of the PAN-UAS architecture, we recommend the following two topics for further analysis and potential optimization.

1. Phase Locked Loop (PLL) synthesizer selection.

   We identified a recently introduced LMX2572 – a 6.4 GHz PLL synthesizer with chirp capability from Texas Instruments that has an integrated VCO and consumes only 225 mW from a single 3 V power supply. On paper it looks like a better match for the PAN-UAS system, but the vendor information is insufficient to determine whether this device meets all of the functional and performance requirements. Therefore, we recommend procuring and testing the LMX2572 evaluation board.

2. MIMO options.

   Bi-phase coding of transmit channel signals was selected to separate the signals from the MIMO receiver. It represents a high computational load on the digital processing module. Also, bi-phase code-related Doppler side-lobes from static, highly reflective objects can mask a weak signal return from low radar cross section UAS. Therefore, in the initial part of Phase II development, we plan to apply the time division multiple access (TDMA) form of MIMO transmit channel separation to simplify the processing algorithm and avoid the Doppler side-lobe issue. However, eventually bi-phase coding will be implemented to achieve higher performance. We recommend development of an additional calibration procedure to suppress the bi-phase codes related to Doppler side-lobes.

   The TDMA operation of a MIMO transmitter reduces the power consumption in continuous operation mode by ~7.5 W and can be used to extend the operating time on battery power.

7.0 REFERENCES

Not applicable.

ADDENDUM

ISI has continued development of MIMO radar technology after PAN-UAS Phase I completion through a SOCOM effort and other related projects. We developed a simplified breadboard prototype of the FMCW MIMO radar operating in 3.5 GHz band – based on the PAN-UAS architecture described in Phase II proposal and adapted to a vehicle mounted use with longer range and greater size and power budget. This development included design, fabrication, and test of a simplified MIMO antenna array (Figure A-1) with 4 TX and 8 RX channels. We designed the RX antenna as two linear arrays with rectangular and circular elements in order to evaluate their performance and compare it to antenna model simulations in MATLAB. Selection of rectangular and circular patch shapes was based on simulations that showed superiority of these shapes to the originally proposed bow tie dipole antenna elements – see details in Section A.1. We will further explore it in Phase II using more accurate HFSS models of antenna elements than the MATLAB model and will select a material with lower ε and ensure the thickness and ε uniformity of the MIMO antenna panel PCB.

Figure A-1: Simplified MIMO antenna array: rectangular and circular 4-element receive antenna (vertical) linear arrays and four transmit elements in the corners; element side (left) and ground side with mounted SMA connectors (right)

We used a network vector analyzer to measure the antenna characteristics (see Figure A-2).

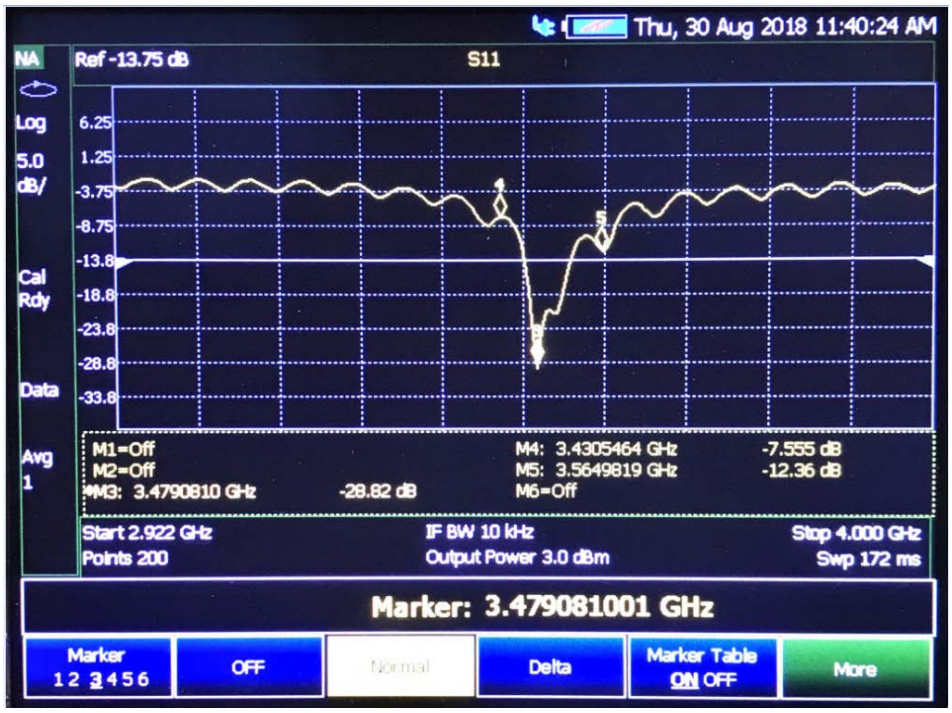


Figure A-2: Measured return loss characteristics for the circular antenna element, tested by ISI

To verify selected radar configuration capabilities, we made a breadboard assembly of the simplified version of the FMCW radar by using the simplified MIMO antenna, evaluation boards of the PLL synthesizer and ADC with FPGA interface board, and discrete RF components from the ISI lab stock with the exception for the power splitter and mixers. The breadboard diagram is shown in Figure A-3. The breadboard prototype uses two TX and four RX channels.

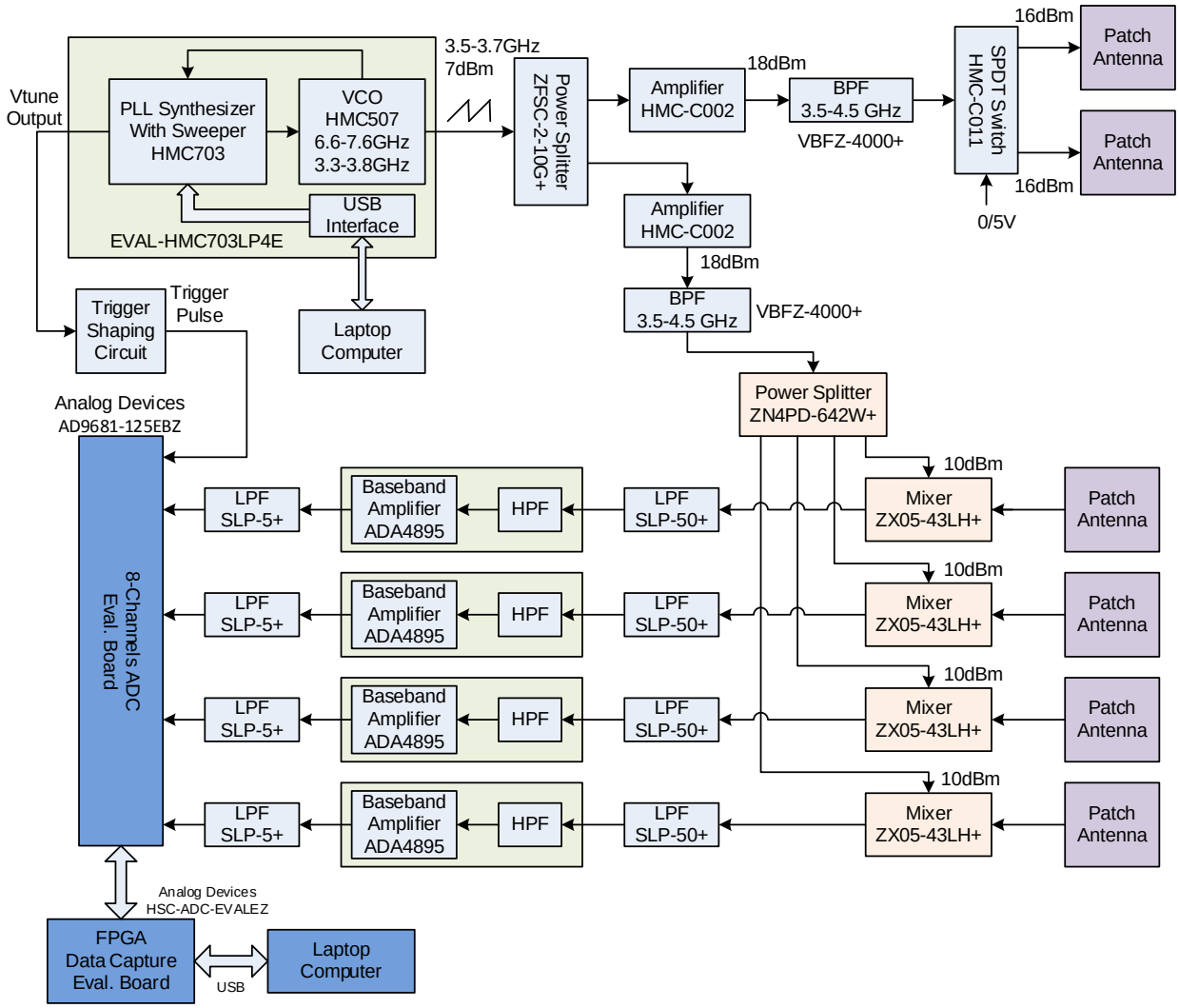


Figure A-3: Schematic diagram of the simplified radar breadboard developed by ISI

For fast FMCW signal generation, we used the evaluation board of the HMS703 PLL synthesizer with HMC507 VCO. While the VCO operates around 7 GHz, we used divide-by-two output to have the central frequency equal to 3.55 GHz. Modulation bandwidth at the 3.55 GHz carrier was set to 100 MHz, which corresponds to 1.5 m range resolution. The 500 kHz cutoff of the HPF on the ADC board forced us to reduce the time from 100 µs (200 µs period) to 20 µs (40 µs period) to avoid significant losses in measurements of closely located targets.

The oscilloscope screenshot in Figure A-4 depicts the VCO tune output of the PLL synthesizer (blue line), which corresponds to the frequency modulation response of the generator. We used symmetrical triangle modulation to simplify radar synchronization. A simple circuit provides double differentiation of the frequency response signal to get short synchronization pulses (shown in red in Figure A-4).

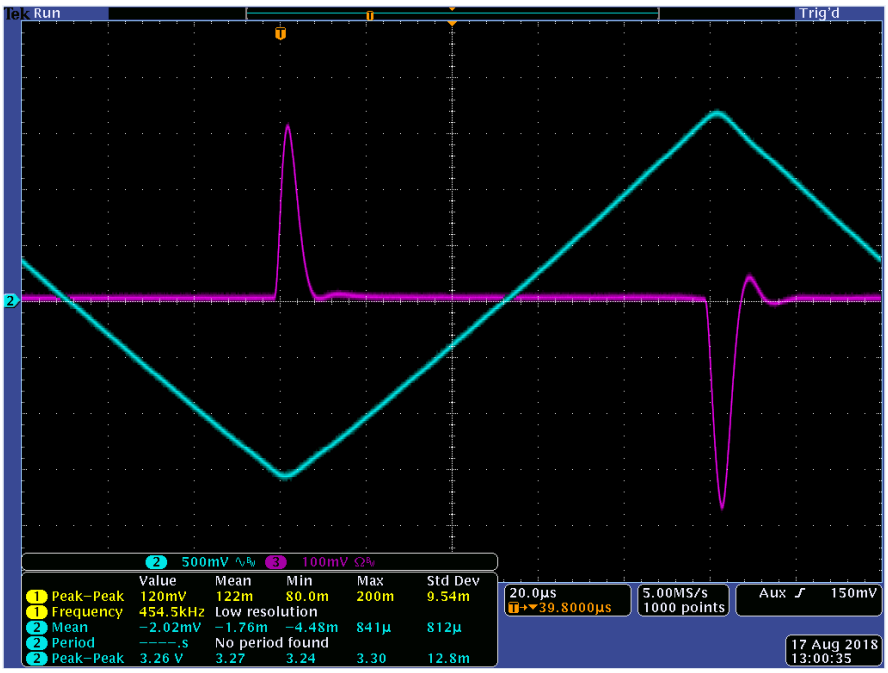


Figure A-4: Oscilloscope screenshot of PLL synthesizer VCO tune output signal (blue line) and synchronization signal (red line)

Because the breadboard prototype was intended to operate in close range, no power amplifiers were used in the transmit path and no low-noise amplifiers were used in the receive path. Two manually switchable transmit outputs have about 16 dBm on the antenna ports. Four receive channels can operate in parallel using four patch antennas, but the receiver's noise figure without amplifiers was too high for a modern radar—about 15 dB. Due to slow manual transmit channel switching, the MIMO processing could only be applied to still scenes. Without MIMO, a small 4-element linear antenna array provides FOV of about 30° in azimuth and about 120° in elevation directions. 2x4MIMO allows the azimuth resolution to decrease to 15°.

As the FPGA interface board (HSC-ADC-EVALEZ from Analog Devices), used for data capture, had the FIFO memory size limited to 256 Ksamples and the minimum applicable sampling rate of the ADC (AD9681-125EBZ) was 15.625 Msps, our coherent recording time was limited to 16.4 ms, which is about 6× less than the 100 ms dwell/frame time specified for the radar. This significantly reduced the breadboard radar detection capability, not only because the shorter frame time results in lower sensitivity (not critical in a close range test), but mostly because it adversely affects Doppler resolution: 2.7 m/s instead of specified 0.45 m/s.

A photograph of the RF frontend breadboard experimentation setup is shown in Figure A-4. As the RF breadboard is based on evaluation boards for the selected components, we reduced the frame duration from 100 ms to 15 ms. This limited the Doppler resolution of the RF breadboard and slightly reduced the sensitivity of the radar, which affected the experimentation results (but not the MIMO radar system performance). The signals received from the MIMO antenna are digitized and captured by the oscilloscope, which can store 250,000 samples per channel. The stored samples were uploaded to a PC for post-processing using the algorithm ISI developed in MATLAB. A photograph of the RF frontend breadboard experimentation setup is shown in Figure A-5.

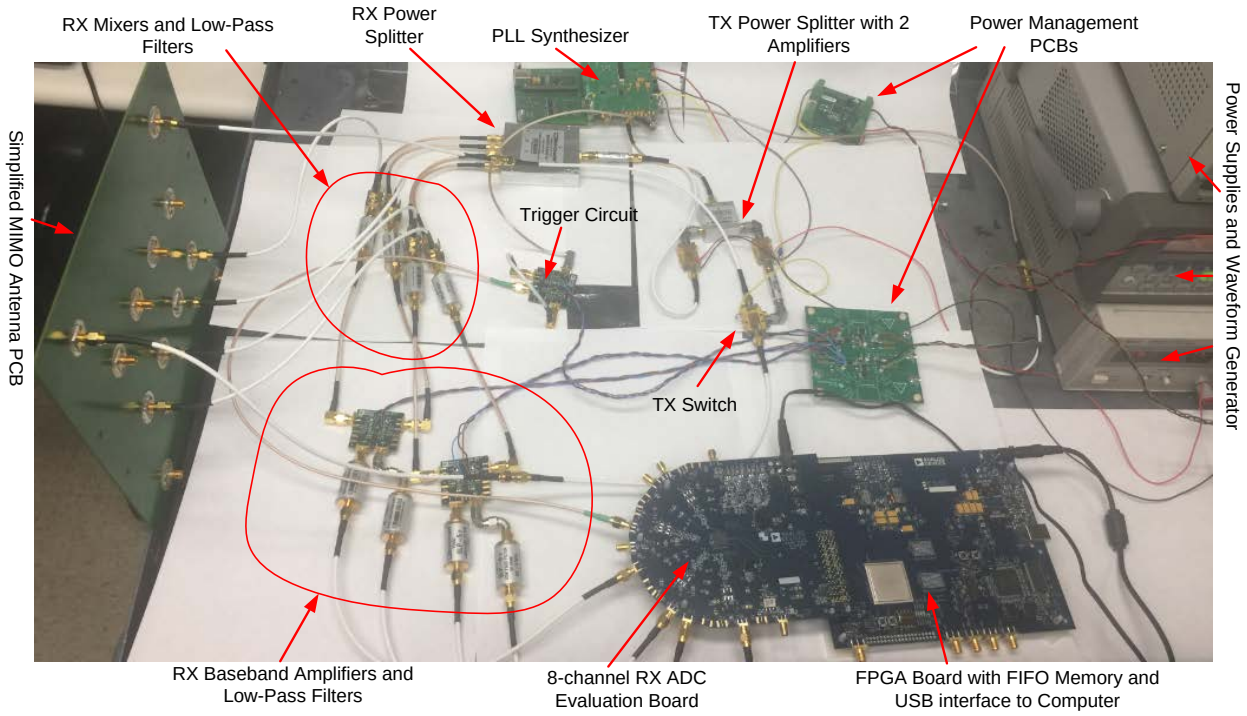


Figure A-5: Lab setup for MIMO radar breadboard experimentation at ISI

For the outdoor radar test, the breadboard assembly was put on a trolley and run out on the street close to ISI's building. Figure A-6 illustrates the radar location and measurement scene. We used moving cars as targets in this test.

Figure A-6: Street test of the radar breadboard

Recorded data were transferred to the laptop computer and processed using the 2D FFT Doppler processing of the fast FMCW radar data. The measurement results for a test with two cars moving on the street is presented in Figure A-7.

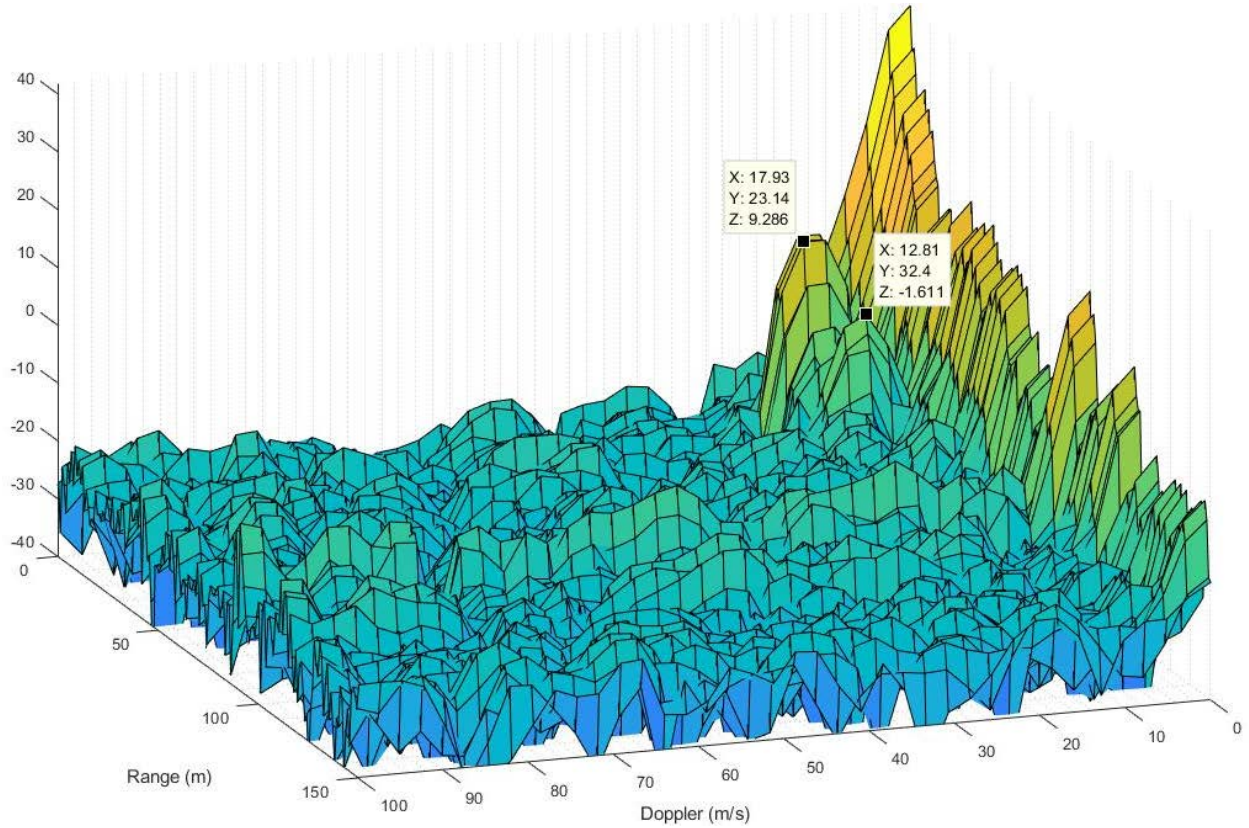


Figure A-7: Radar range-Doppler diagram with two moving cars

The 3D graph in Figure A-7 shows the magnitude of the radar return signals in dB (Z axis) versus range (Y axis: 0 to 150 meters) and velocity (X axis: 0 to 100 m/s). The high magnitude ridge with (close to) zero Doppler values, presented on the graph, is caused by reflection from the ground and still objects on the street (fences, buildings, parked cars, etc.). Two distinct peaks to the left from the ridge correspond to two cars. The first car was detected at the range of ~23 m from the radar and moving at ~18 m/s or 40 mph. The peak magnitude is 9.3 dB. The second car range and velocity were, respectively, measured at 32.4 m and 12.8 m/s or ~29 mph. The second car was partially blocked by the first car, which, combined with the longer range, resulted in the magnitude being lower by ~11 dB compared to the first car. As the average noise floor was about -30 dB, measurements for both cars were above the noise level. Also, the car velocities were high enough to be easily separated from the zero Doppler ridge.

In spite of multiple drawbacks (low number of antenna elements, low Doppler resolution, low transmit power, high noise figure, etc.) of the breadboard, we made an attempt to detect a small commercial quadcopter shown in Figure A-8. During the test, the quadcopter was flying over a trolley with radar breadboard prototype placed in the ISI parking lot. Figure A-9 is a photo of the "test site" that was taken by the flying drone.

Figure A-8: Quadcopter used for radar breadboard test

Figure A-9: Photo of the radar breadboard on a trolley taken by the flying quadcopter during the test in the parking lot

The MATLAB graph in Figure A-10 shows the processed radar data acquired during the drone test. As can be observed from the graph, the quadcopter-related peak at the 10.2 m range, 7.7 m/s velocity (close to the maximum speed of the quadcopter achieved in this test), and -0.7 dB magnitude is marginally distinguishable from the zero Doppler ridge. The reason for the quadcopter's poor resolution is not the low magnitude of the radar signal (the target SNR is high enough at about 30 dB), but the low Doppler resolution of the radar breadboard.

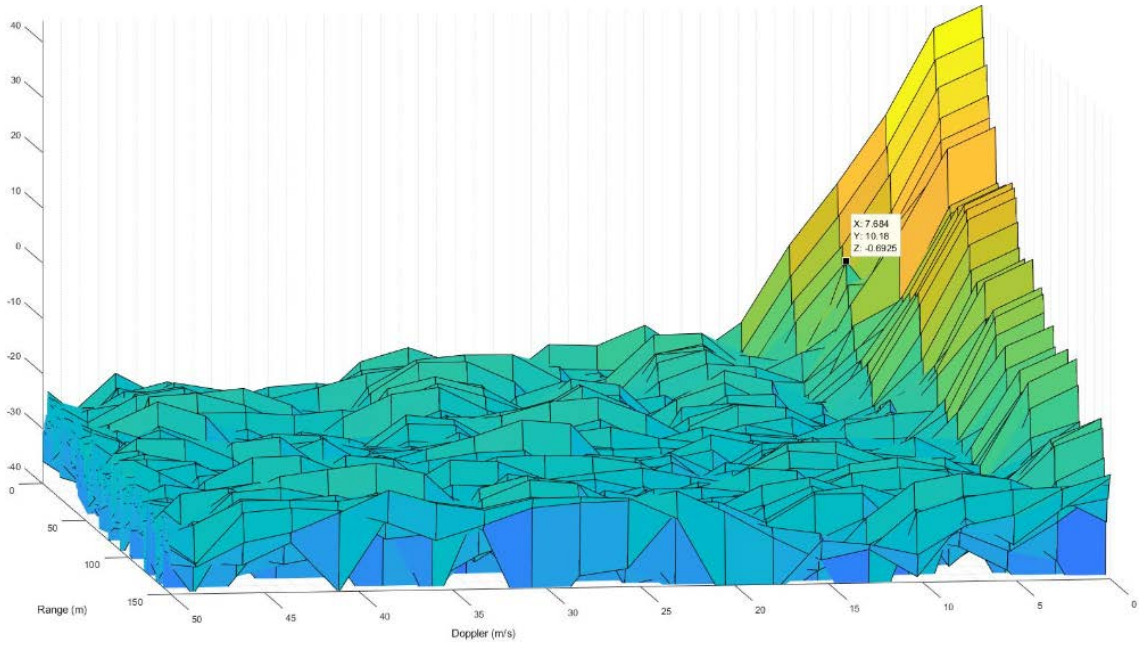


Figure A-10: Radar range-Doppler diagram with flying quadcopter

The quadcopter test demonstrated the critical importance of high Doppler resolution for an UAS detection radar. The high Doppler resolution is one of the advantages of the ISI's radar due to receiving radar returns from any directions in parallel. It allows significantly increased coherent dwell time and correspondingly improved Doppler resolution in the radar search mode. Unlike other available radars for small UAS detection, the ISI radar, due to its use of MIMO and fast FMCW technologies, provides a fine Doppler resolution during the search (not tracking!) within a hemispherical FOV and extremely short (100 ms) frame time.

A.1 MIMO Antenna Design

We designed the MIMO antenna array by modeling and simulating the antenna using the MATLAB® Antenna Toolbox™. The MIMO antenna acts as an array of independent antenna elements, so only the individual antenna element was simulated. Both the receive antenna elements and transmit antenna elements have the same configuration and size. First we analyzed a bow tie antenna element (see Figure A-11) positioned over the reflector plane and optimized for the frequency of 3.5 GHz. The feed (not shown) to the antenna element is connected to the center of the bow tie and is orthogonal to the bow tie and reflector plane to avoid beam distortions. The optimal reflector distance is $\lambda/4$ (quarter wavelength) or 21.4 mm. The length and angle of the flares were optimized to reduce the return loss and the VSWR (Voltage Standing Wave Ratio—the amount of reflected power expressed as a ratio), and set to 31 mm and 45°, respectively. Figure A-12 shows the radiation pattern of the bow tie antenna element with these properties. Its calculated gain is 7.31 dB.

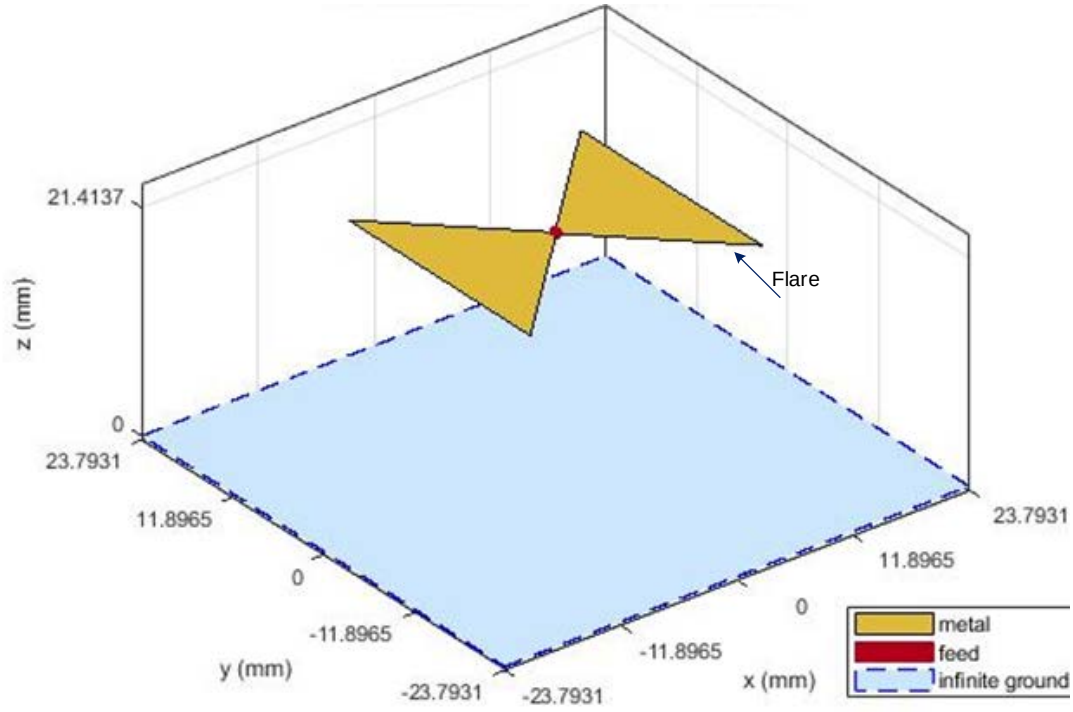


Figure A-11: Bow tie dipole antenna element simulation model with infinite ground plane

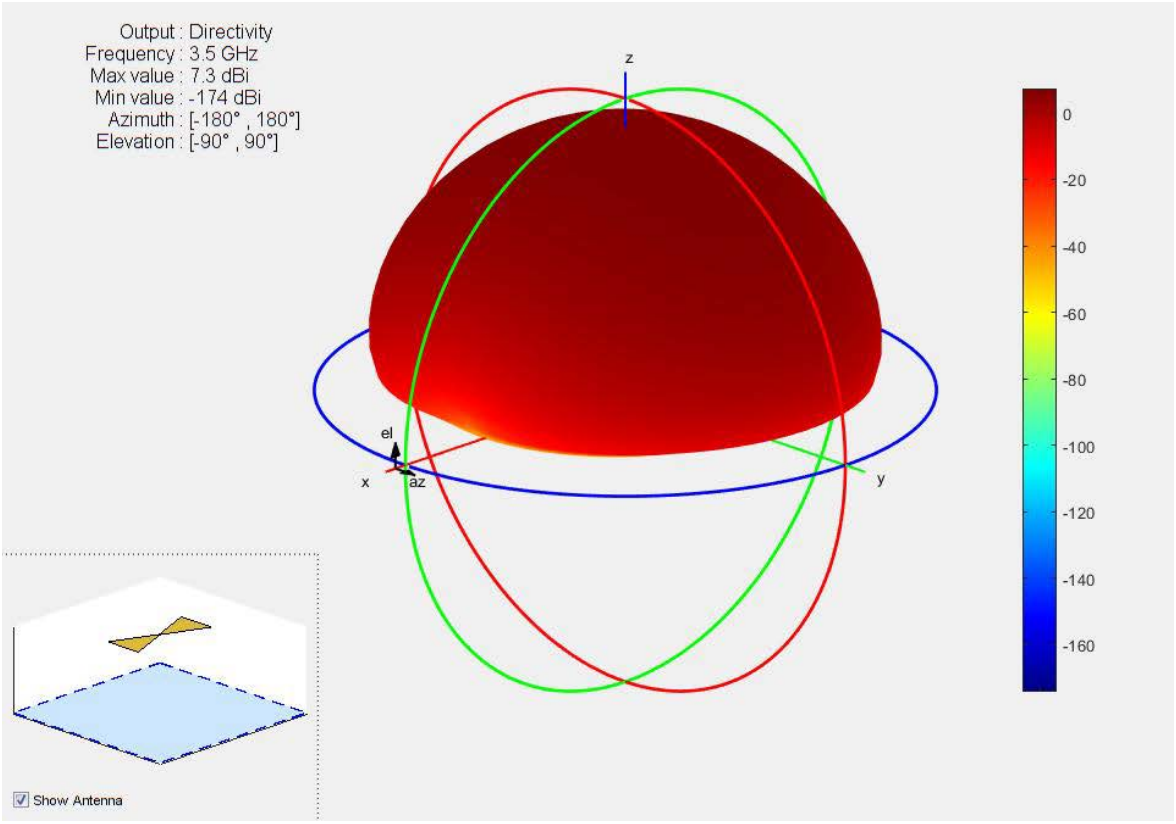
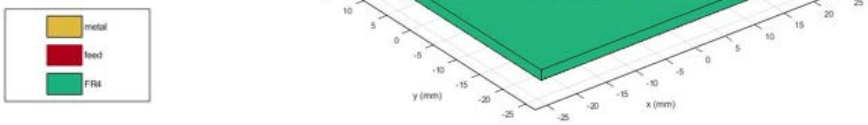


Figure A-12: Radiation pattern of the bow tie antenna with infinite reflector plane at 3.5 GHz, simulated by ISI

The bow tie antenna element is relatively large with a significant gap between the reflector and antenna element's planes, which requires a complex feed solution. An alternative design of an antenna array uses a microstrip patch antenna that can be implemented as a two-layer printed circuit board (PCB) only 64 mil (1.6 mm) thick (for a standard FR4 material). We compared circular (Table A-1 and Figures A-13 and A-14) and rectangular (Table A-2 and Figures A-15 and A-16) configurations of antenna elements. These simulations did not include the feed that was added later.

Table A-1: Circular Patch Antenna Element Designed by ISI

Parameter	
Substrate	FR4
Dielectric Constant (ε_R)	4.7
Substrate Thickness	64 mils
Radius	504 mils
Feed Offset	177 mils



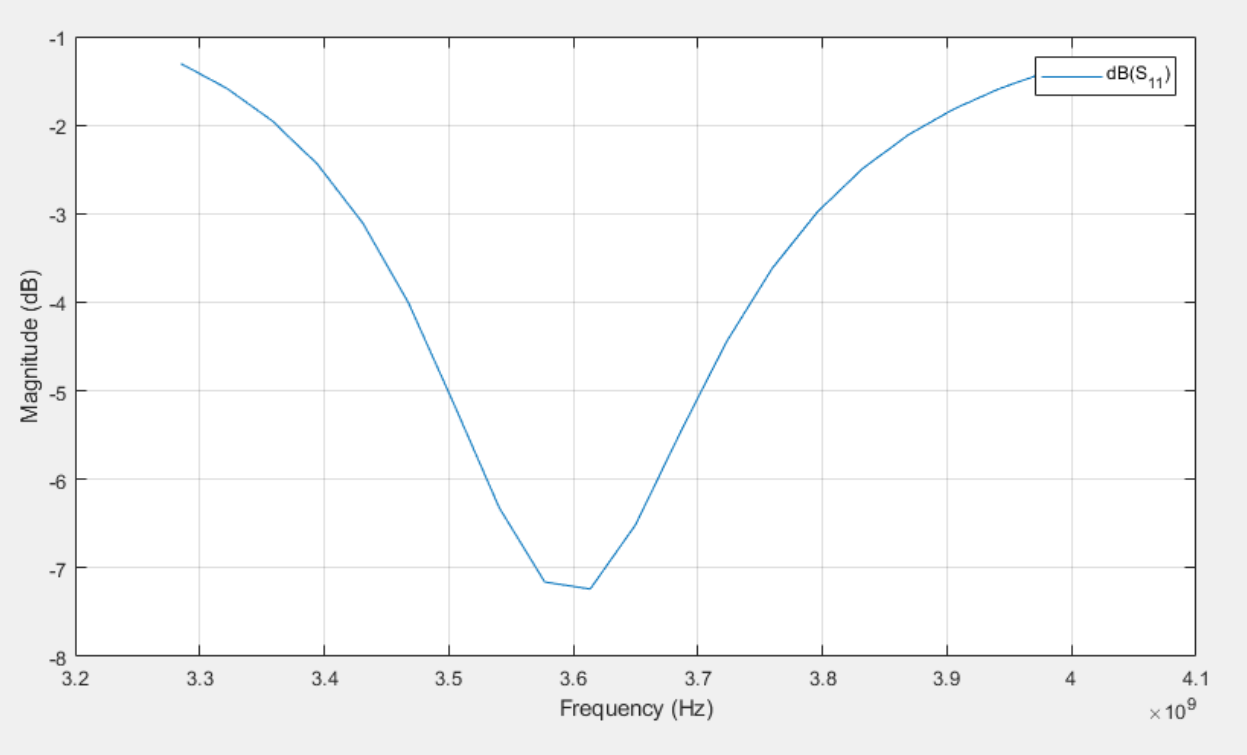


Figure A-13: Circular patch antenna simulation by ISI: S11 parameters

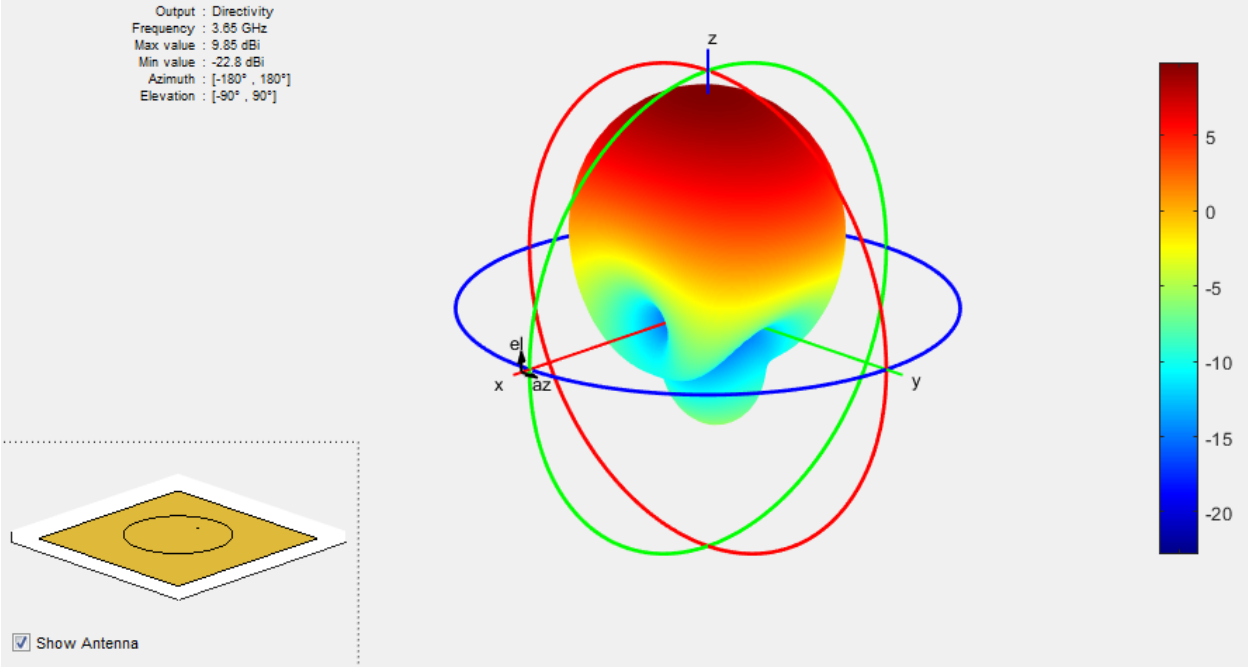
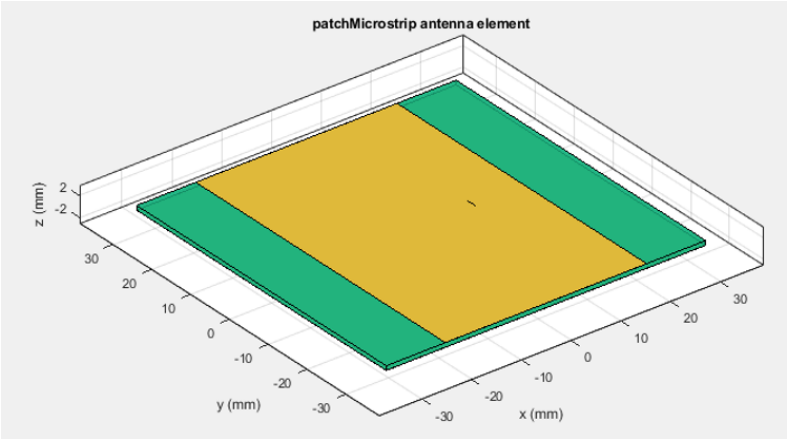


Figure A-14. Circular patch antenna simulation: pattern.

Table A-2: Rectangular Patch Antenna Element Designed by ISI

Parameter	
Substrate	FR4
Dielectric Constant (ε_R)	4.7
Substrate Thickness	64 mils
Width	1062 mils
Length	677 mils
Feed Offset	178 mils



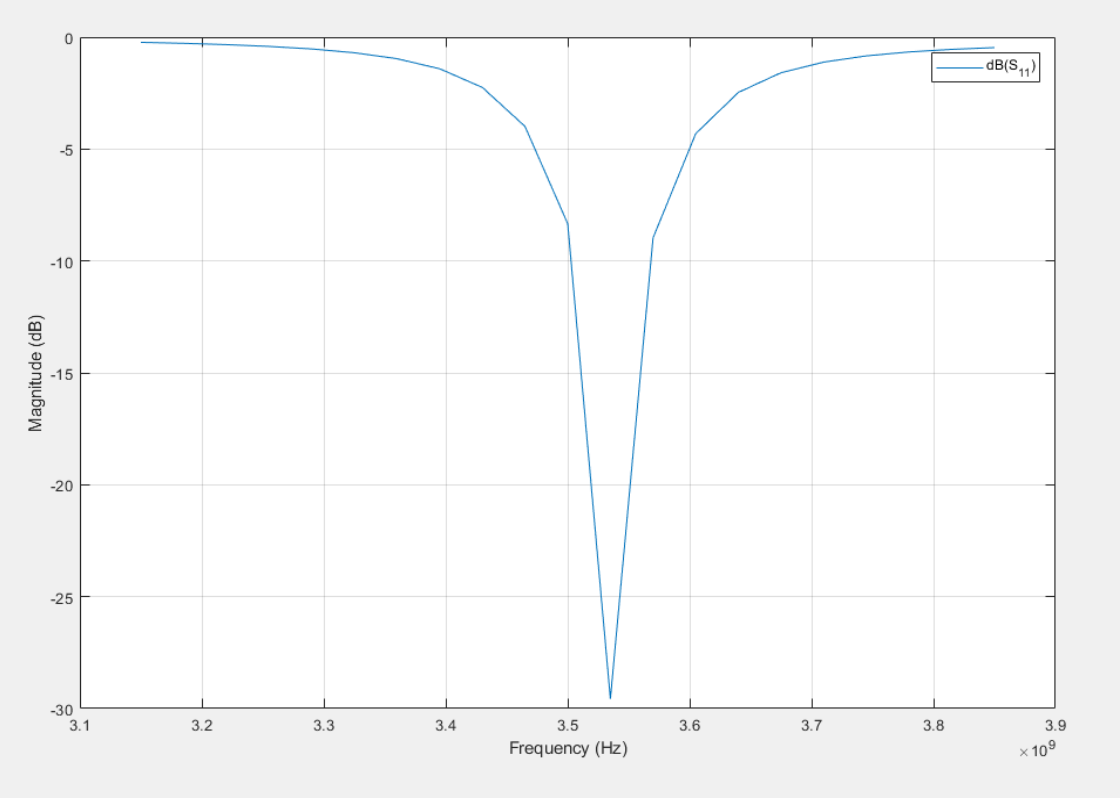


Figure A-15: Rectangular patch antenna simulation by ISI: S11 parameters

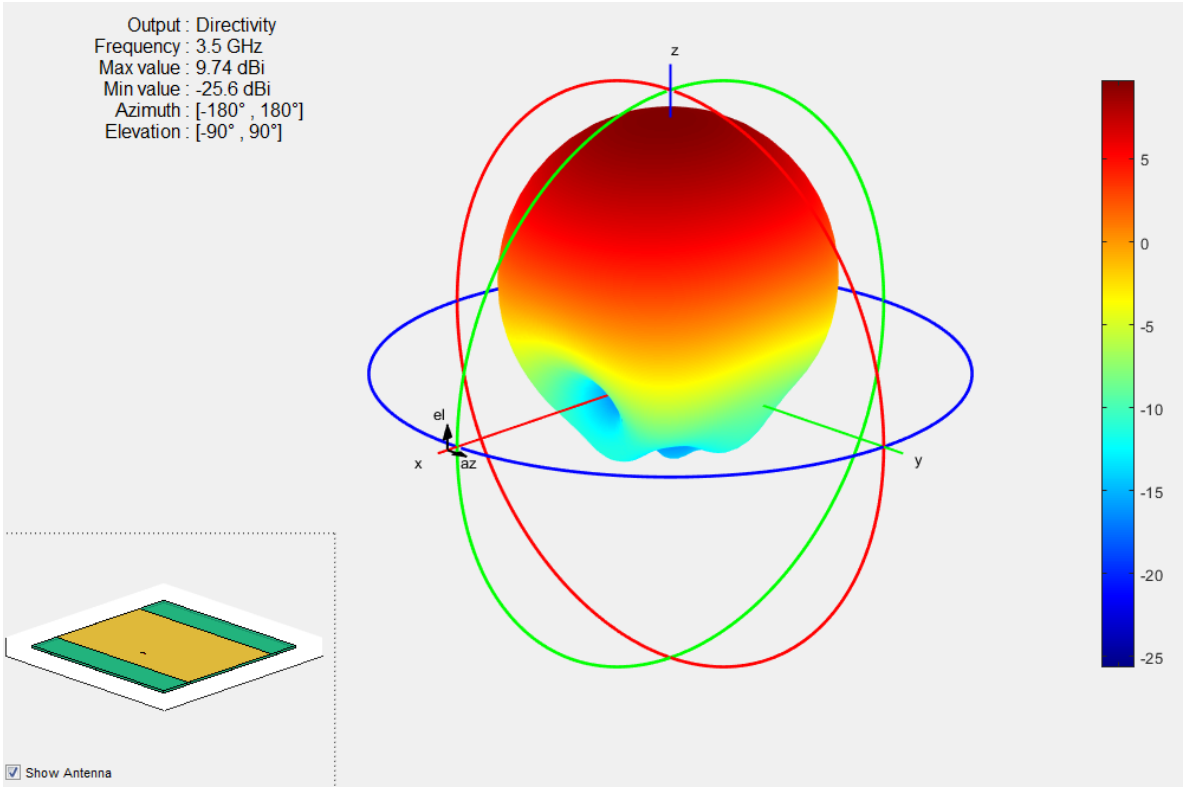


Figure A-16: Rectangular patch antenna simulation: pattern

We also analyzed a Planar Inverted F-type Antenna (PIFA) that is widely used in mobile devices operating in 2.4 GHz and 5 GHz bands. This L-shaped antenna (Figure A-17) is a variant of the rectangular patch antenna that is smaller in size and much better at radiating over the required frequency band (see Figures A-18 and A-19). The PIFA parameters used in simulations were automatically generated by the MATLAB® simulator. We will further explore PIFA applicability to PAN-UAS and optimize its design in Phase II.

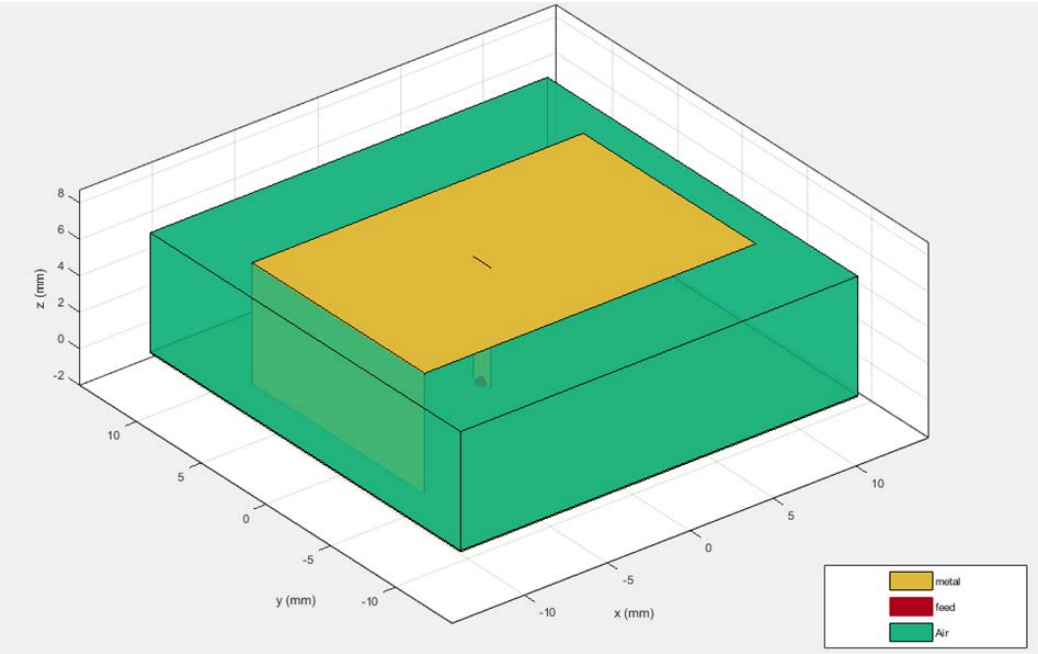


Figure A-17: PIFA antenna structure designed by ISI

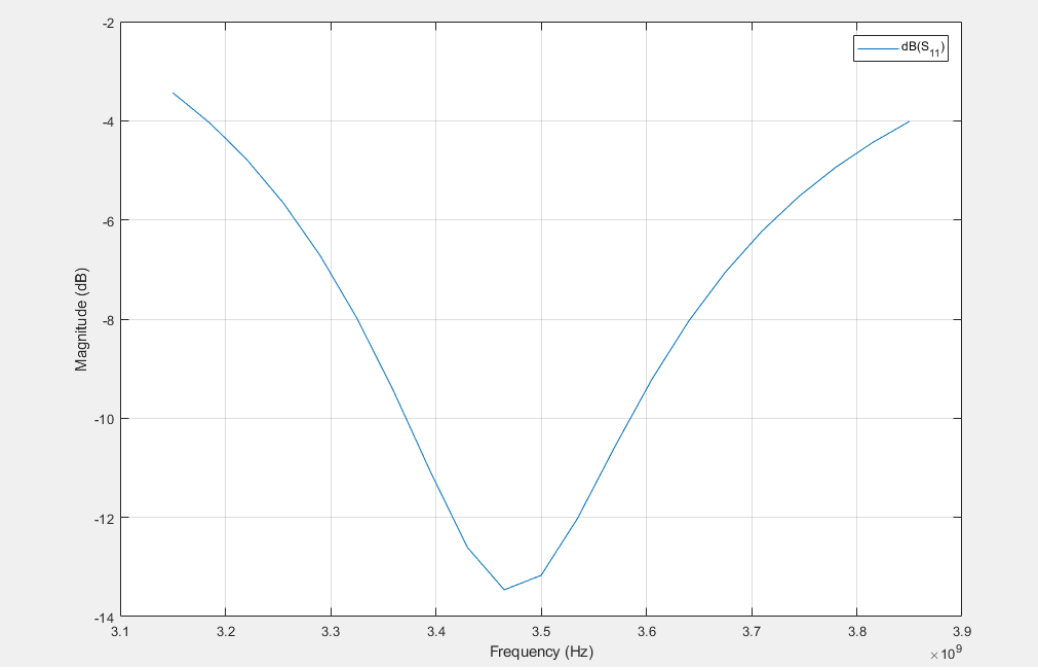


Figure A-18: PIFA antenna simulation: S11 parameters

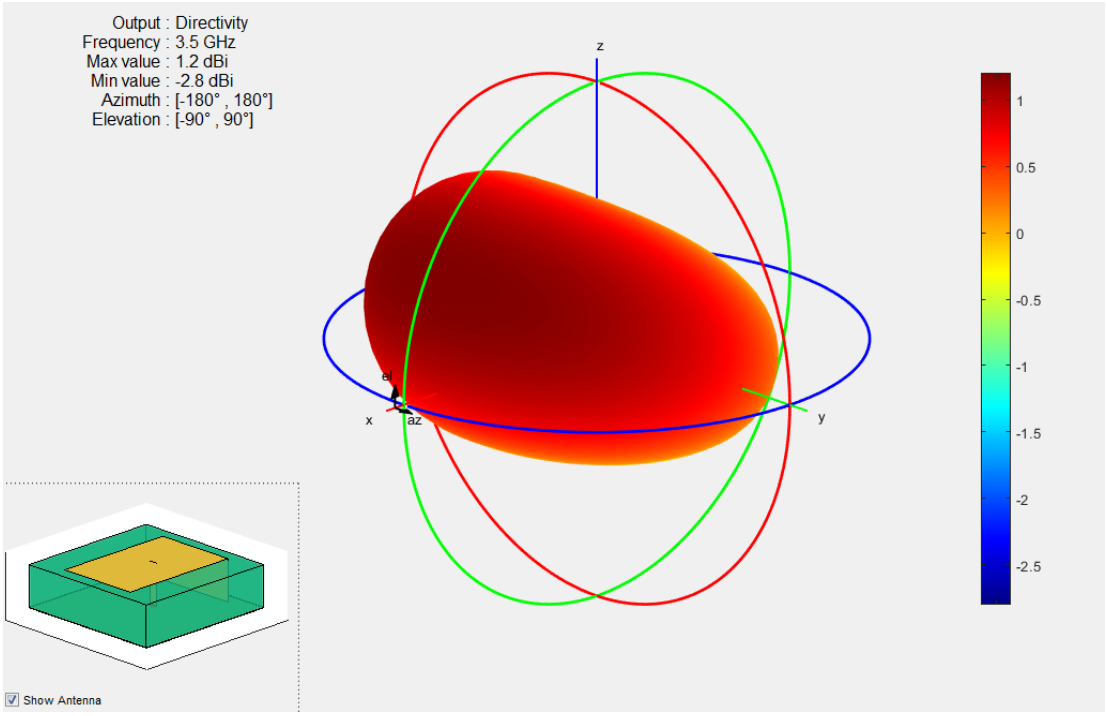


Figure A-19: PIFA antenna simulation: S11 parameters

Based on the geometry and simulation results, we decided to evaluate the circular and rectangular antenna elements and built a prototype antenna panel. The evaluation results are discussed above.

ACRONYMS AND ABBREVIATIONS

Acronym	Definition
CONOPS	concept of operations
COTS	commercial off-the-shelf
DSP	digital signal processing
FFT	Fast Fourier Transform
FMCW	frequency-modulated continuous wave
FPGA	field-programmable gate array
HFSS	high-frequency structure simulator
HPDBSCAN	Highly-Parallel Density-Based Spatial Clustering of Applications with Noise
ISI	Intellisense Systems, Inc.
LDO	low dropout
MIMO	multiple-inputs, multiple-outputs
MPSoC	multi-processor system-on-chip
PA	power amplifier
PAE	power added efficiency
PAN-UAS	Portable Anti-UAS (device)
PCB	printed circuit board
PLL	Phase Locked Loop
RAM	Random Access Memory
RF	radio frequency
RX	receive
SMD	surface-mount device
SoC	system-on-chip
SoM	system-on-module
SWaP-C	size, weight, power, and cost
TDMA	time division multiple access
TRL	technology readiness level
TX	transmit
UAS	unmanned aircraft system
VCO	voltage-controlled oscillator