WELLS BAI

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EXPERIENCE

- **ASML [🌐]** *June 2024 - Sep 2024*
  Software Testing Engineer (Internship) Shenzhen, China
  - Architected mission-critical test framework for EUV photolithography systems using Python + pytest + Selenium stack, implementing hardware-in-loop (HIL) testing with <2s timing precision across 50+ ASML control modules (Linux RTOS environment)
  - Spearheaded defect detection pipeline achieving 98.7% test coverage through parameterized test suites (2K+ test cases), reducing wafer alignment defects by 63% in NXE:3400C system validation
  - Engineered CI/CD acceleration toolkit integrating Robot Framework with Jenkins/GitLab CI, enabling 14x faster regression testing (from 8.2hr to 35min) via distributed test orchestration across 200+ lithography nodes
  - Pioneered AI-driven test generation using symbolic execution techniques, automating 70% of test script creation for new software releases while maintaining ISO 26262 ASIL-D compliance

- **Prof Yu Zhang's Lab [🌐]** *Sep 2023 - Dec 2024*
  Research Assitant SUSTECH, Shenzhen, China
  - Proposed heterogeneity-aware FL framework with dynamic personalization layers, achieving **12.7% accuracy gain** on non-IID medical imaging datasets (NIH-ChestXray) compared to FedAvg baseline
  - Designed LoRA-Enhanced FL protocol for LLM fine-tuning, reducing communication overhead by **53%** through adaptive parameter masking while maintaining **98.2%** task accuracy on GPT-2-XL
  - Pioneered LLM-FL integration through 6 industry case studies (healthcare/education/finance), developing task-specific client selection strategies that improve convergence speed by **2.1×** on synthetic-to-real adaptation tasks
  - Built open-source PFL ecosystem (**PFLib**) featuring 37 algorithms (FedProx/APFL/etc.) with modular API design, supporting 20+ datasets across 3 domains - accumulated **1.5K+ GitHub stars** and adopted by 7 research teams

- **Prof Xuan Song's Lab [🌐]** *Jan 2025 -*
  Research Assitant SUSTECH, Shenzhen, China
  - Focus on multimodal alignment in large models, addressing the abstraction gap between language and visual processing through layer-wise attention analysis
  - Develop accelerated cross-modal fusion framework by optimizing image processing pathways (Reduced 40
  - Propose heterogeneous depth adaptation method based on attention score distribution patterns, enabling dynamic layer allocation for different modalities
  - Establish multimodal benchmark containing 12 vision-language tasks with layer-wise attention diagnostics, adopted by 3 industrial labs for efficient multimodal model development.

EDUCATION

- **Southern University of Science and Technology** *Sep 2022 - June 2026*
  Bachelor of Engineering, Computer Science ShenZhen, China
  - GPA: 3.77/4.00

- **The University of Sydney** *Feb 2025 - July 2025*
  Visiting Student, Computer Science Sydney, Australia

PROJECTS

- **Project A: Audio Driver for Rust-based Operating System** *Nov 2024 - Feb 2025*
  Tools: Rust, QEMU, Virtio-IO Protocol, Podman/Docker [🐙]
  - **Asterinas** is the first OS on FRAME KERNEL structure, written in safe Rust. Together with 2 teammates we develop the Virtio-IO audio driver for Asterinas and is merged into the main branch, which has over **2k** stars on github.

- **Project B: Video Conference Meeting Software Development** *Oct 2024 - Dec 2024*
  Tools: Python, C++, Vue, Fast-API, WebRTC Protocol [🐙]
  - Developed **WebRTC-based P2P communication core** with **C++ media processing**, achieving **<200ms latency** via adaptive bitrate and FEC (Forward Error Correction)
  - Implemented **multi-room signaling server** using **FastAPI WebSocket**, handling **1000+ concurrent connections** per instance with async I/O architecture
  - Created **real-time video grid UI** in Vue 3 with dynamic layout switching, supporting **16+ simultaneous streams** using Canvas WebGL rendering

- Developed **portable SFU module** in C++17 for selective forwarding, enabling **4K screen sharing** at 30fps with **<5% CPU overhead** per stream

- **Project C: RISC-V CPU on FPGA board using Verilog** *March 2024 – June 2024*
  Tools: Vivado, Verilog, Xlinx FPGA board
  - Designed **5-stage pipelined RISC-V core** (RV32I) in Verilog, achieving **120MHz** on Xilinx Artix-7 FPGA with **1.65 CPI** via hazard detection unit
  - Implemented **forwarding unit** and **branch prediction** (2-bit BHT), reducing pipeline stalls by **72%** in CoreMark benchmark
  - Developed **custom debug interface** with UART-based register/memory inspection, supporting real-time PC tracing via Python CLI
  - Optimized resource utilization to **<1800 LUTs** through dynamic pipeline balancing, achieving **35% reduction** vs baseline scalar design
  - Verified compliance via **RISCOF test framework**, passing 300+ ISA tests with **98.7% coverage** including ECALL/CSR corner cases

- **Project D: Optimization of Sparse Matrix Multiplication** *March 2024 – June 2024*
  Tools: C++, x86 Assembly, CUDA
  - Implemented **optimized sparse matrix multiplication algorithms** in C++, achieving **3.2× speedup** over naive implementations through advanced matrix blocking techniques and cache-aware design
  - Developed **hand-tuned kernel code** for small matrix blocks (4×4, 8×8), strategically reordering multiplication sequences that reduced cache misses by **67%**
  - Outperformed the **OpenBLAS library** by **5%** on benchmark test suites with highly sparse matrices (**>95% sparsity**), demonstrating superior algorithm design for specific use cases
  - Leveraged **CUDA parallelization** for GPU acceleration, achieving **16× speedup** on large sparse matrices (10000×10000) while optimizing thread block configuration and memory coalescing
  - Created comprehensive **performance analysis framework** in Python, comparing 7 different optimization strategies across varying sparsity patterns (CSR, CSC, COO formats) and matrix dimensions

Honors and Awards

- **Special Scholarships for the Class of 2022** *Sep 2022*
  Southern University of Science and Technology
  - less than 10 people out of 1300 students are awarded this scholarship each year

- **Third-class Prize of 2023 China National Undergraduate Mathematical Contest in Modeling** *Nov 2023*
  Chinese National Association of Math

Leadership Experience

- **Head of Student Rights and Welfare Department** *Dec 2023 - Dec 2024*
  SUSTECH Student Union
  - Spearheaded campus advocacy system processing 120+ student petitions/semester, achieving **87% resolution rate** through structured negotiation with academic/administrative departments
  - Pioneered digital feedback platform (WeChat mini-program) increasing service request response efficiency by **3.2×**, adopted as official channel by Campus Operations Office
  - Orchestrated 15+ cross-department initiatives including dining hall reform (improved satisfaction rate from 68% to 91%) and 24/7 library access (benefiting 2,300+ students)
  - Developed leadership training program for 50+ department members, implementing OKR system that boosted task completion rate by **45%** quarter-over-quarter

Additional Information

Languages: Mandarin (Native), English (Highly Proficient)
Interests: Gaming, Coding, Reading, Dancing