AMD
XILINX

# Introduction to Embedded System Design Flow using Zynq

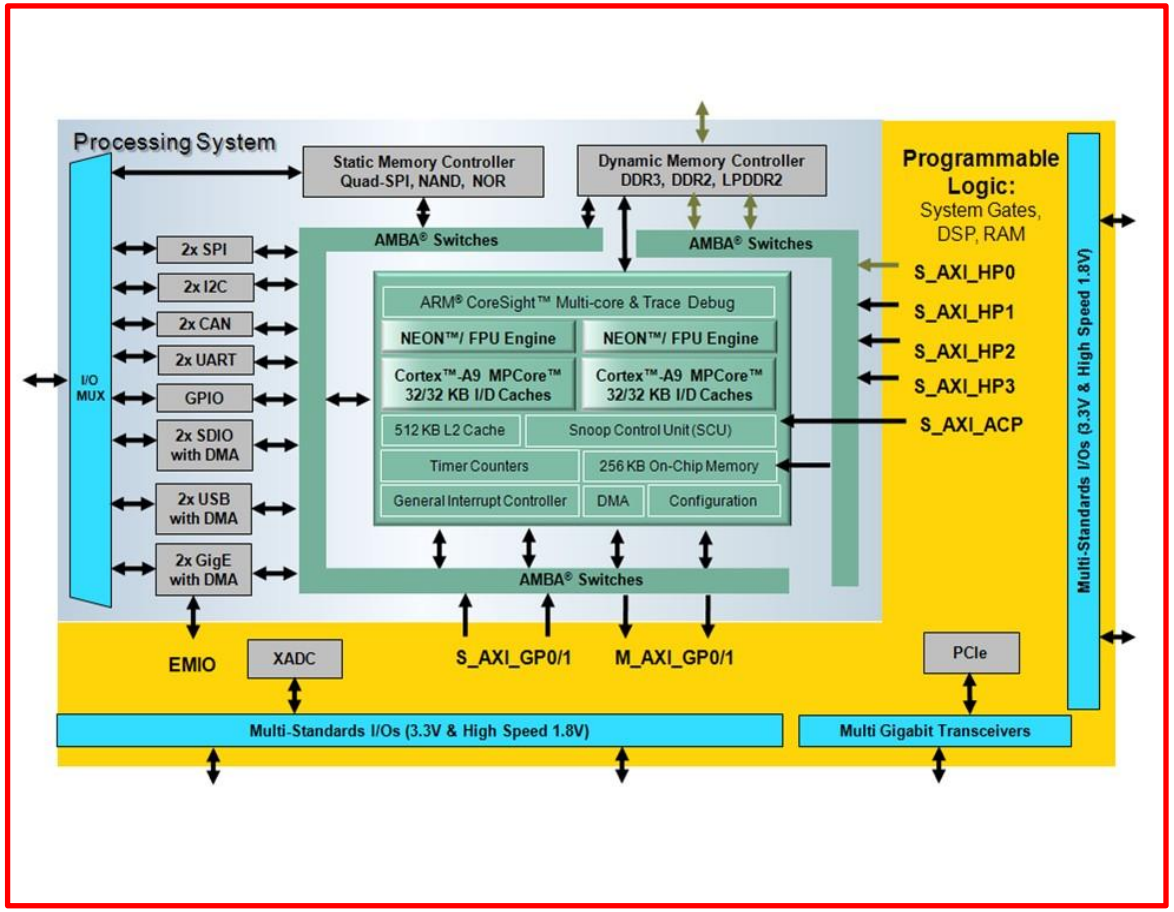
# Objectives

- After completing this module, you will be able to:
  - Define a Zynq SoC processor component
  - List the key aspects of the Zynq SoC processing system
  - Describe the embedded design flow
  - Understand the function of the IP Integrator tool
  - Indicate how the hardware design is linked to the software development environment

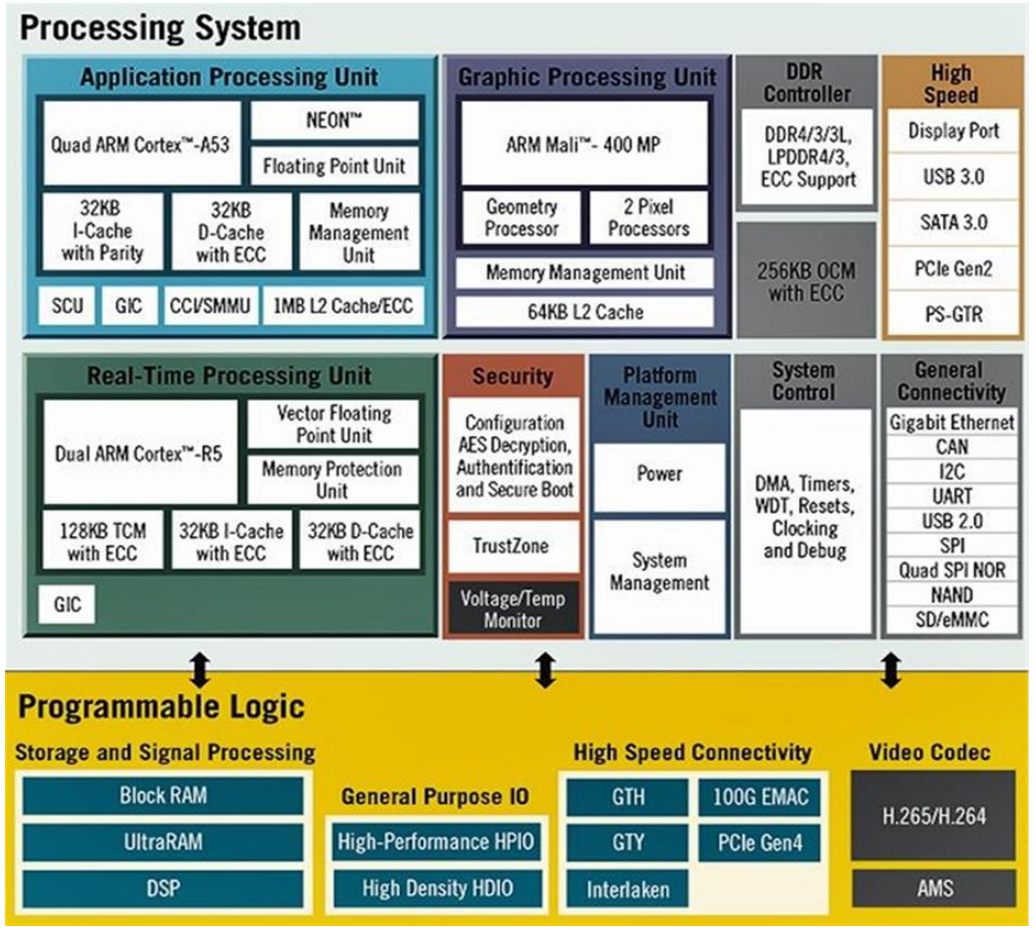
# Outline

- **Embedded Processor Component**
- Overview of Vivado for Embedded System Design
- Embedded System Development Flow
- Hardware Platform Creation
- Vitis IDE
- Summary

# Zynq-7000 & Zynq MPSoC




Zynq-7000 28nm




Zynq MPSoC 16nm





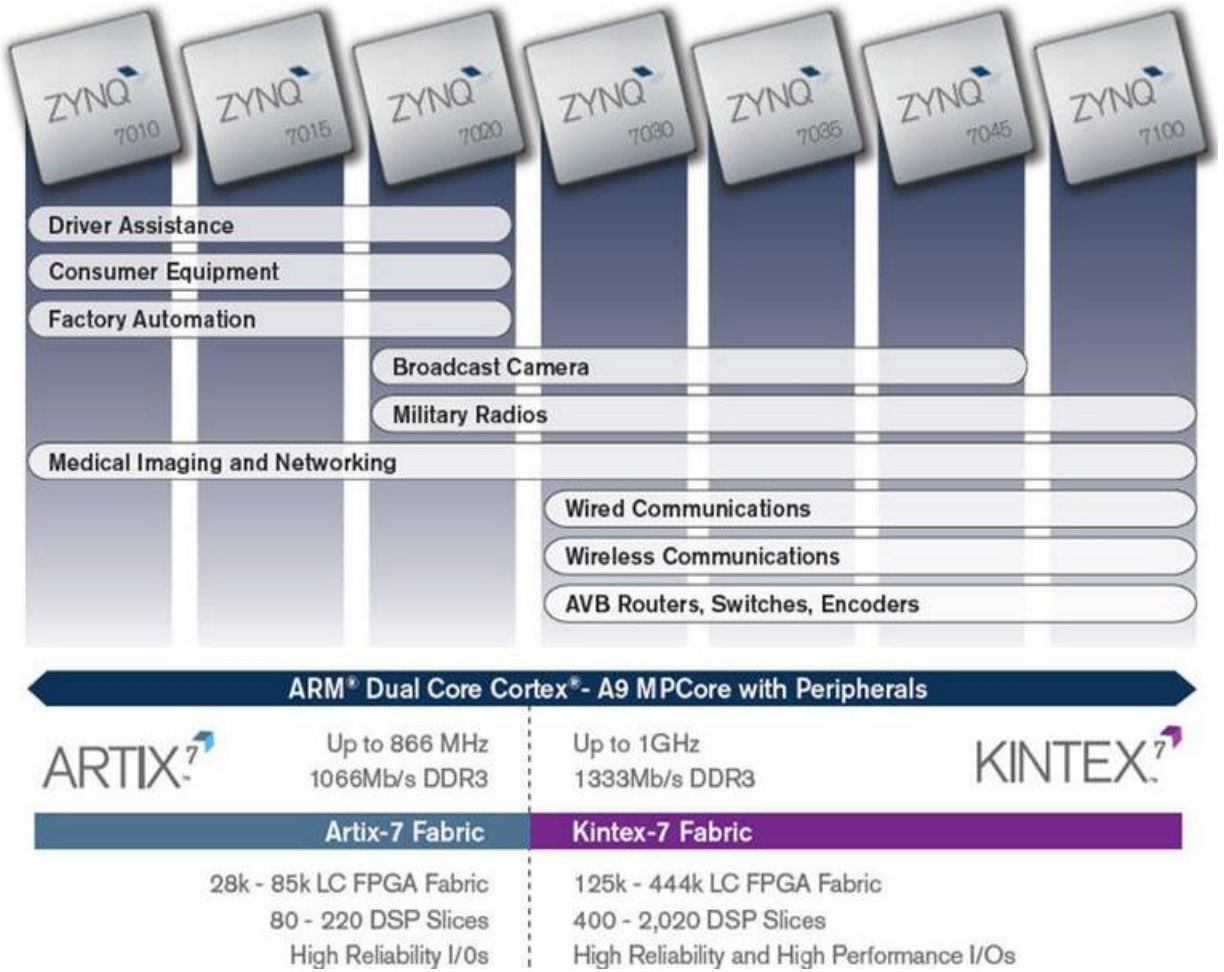
AMD XILINX

# Embedded Design Architecture in Zynq

- Embedded design with Zynq is based on:
  - Processor and peripherals
    - Dual ARM® Cortex™ -A9 processors of Zynq-7000 SoC
    - AXI interconnect
    - AXI component peripherals
    - Reset, clocking, debug ports
  - Software platform for processing system
    - Bare Metal Applications or OS's (e.g. Linux, FreeRTOS)
    - C language support
    - Processor services
    - C drivers for hardware
  - User application
    - Interrupt service routines (optional)

# The PS and the PL

- The Zynq-7000 SoC architecture consists of two major sections
  - PS: Processing system
    - Dual ARM Cortex-A9 processor based
      - Single core versions available
    - Multiple peripherals
    - Hard silicon core
  - PL: Programmable logic
    - Uses the same 7 series programmable logic
      - Artix™-based devices: Z-7010, Z-7015 and Z-7020 (high-range I/O banks only)
      - Kintex™-based devices: Z-7030, Z-7035, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)



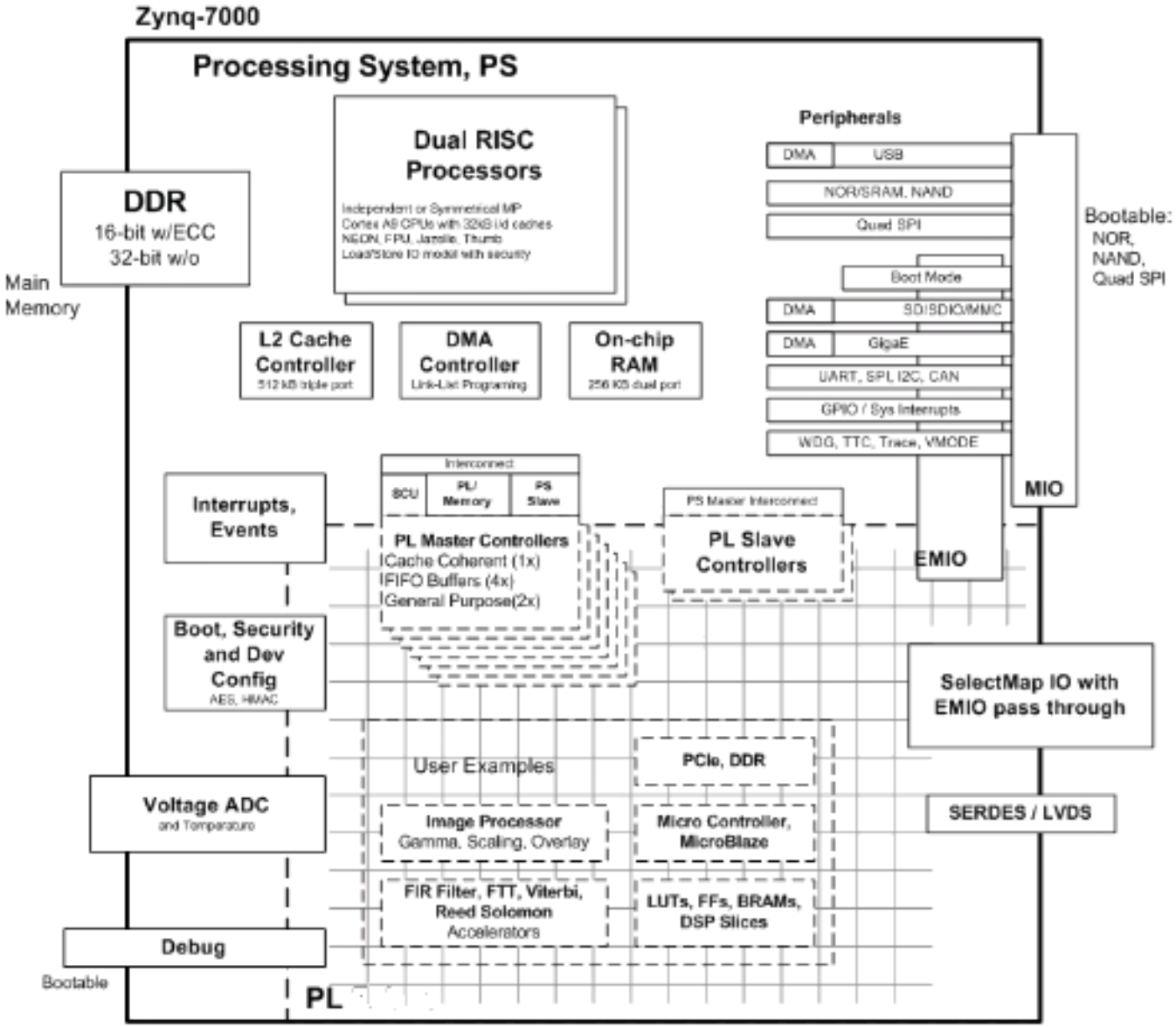





AMD XILINX

# PS Components

- The Zynq SoC processing system consists of the following blocks
  - Application processing unit (APU)
  - I/O peripherals (IOP)
    - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
  - Memory interfaces
  - PS interconnect
  - DMA
  - Timers
    - Public and private
  - General interrupt controller (GIC)
  - On-chip memory (OCM): ROM and RAM
  - Debug controller: CoreSight



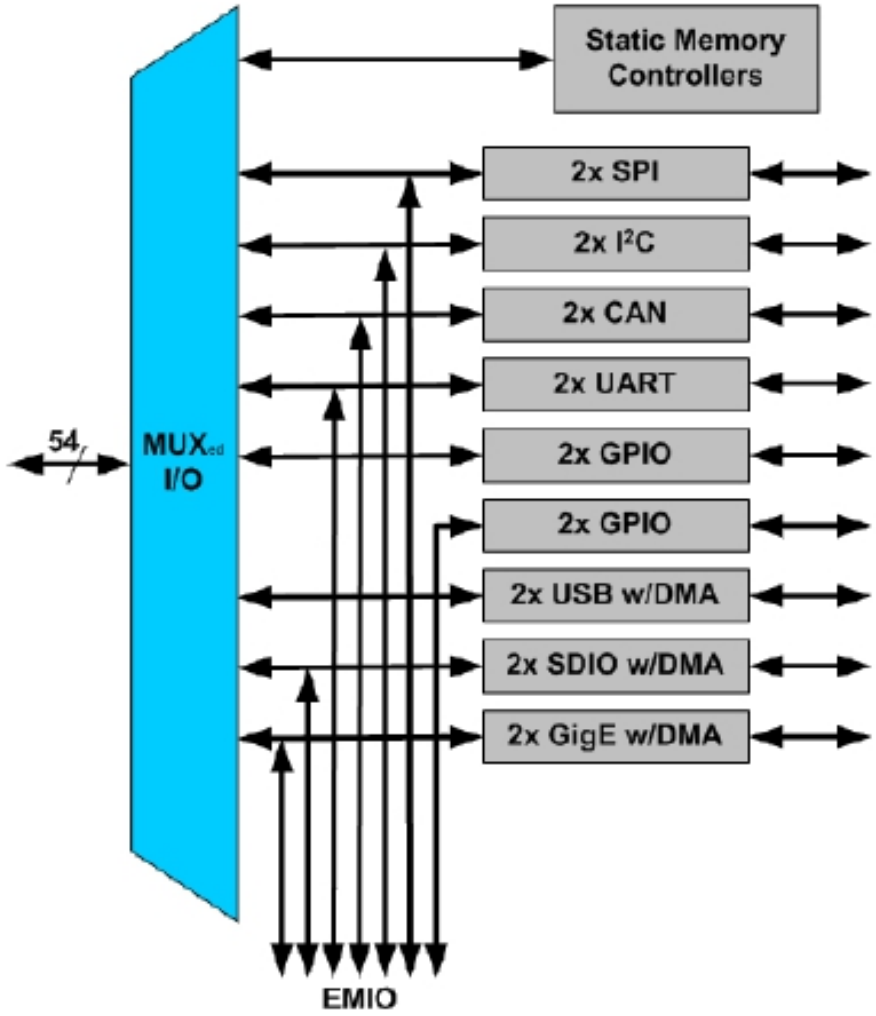





AMD XILINX

# Zynq Architecture Built-in Peripherals

- Two USB 2.0 OTG/Device/Host
- Two Tri- Mode GigE (10/100/1000)
- Two SD/SDIO interfaces
  - Memory, I/O and combo cards
- Two CAN 2.0Bs, SPIs , I2Cs, UARTs
- Four GPIO 32bit Blocks
  - 54 available through MIO; other available through EMIO
- Multiplexed Input/Output (MIO)
  - Multiplexed pinout of peripherals and static memories
- Extended MIO
  - Maps PS peripheral ports to the PL








AMD XILINX

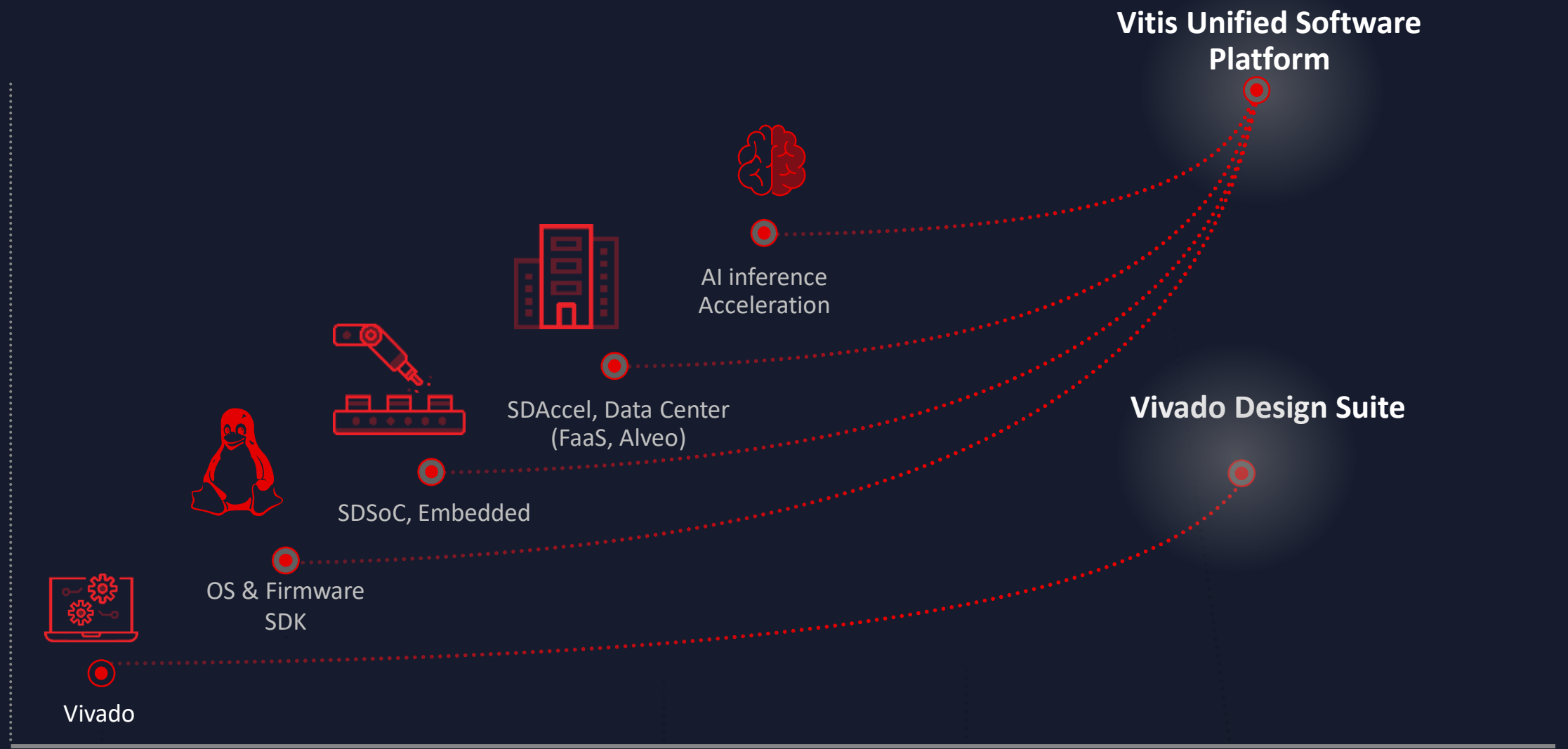
# Overview of Vivado & Vitis for Embedded Design



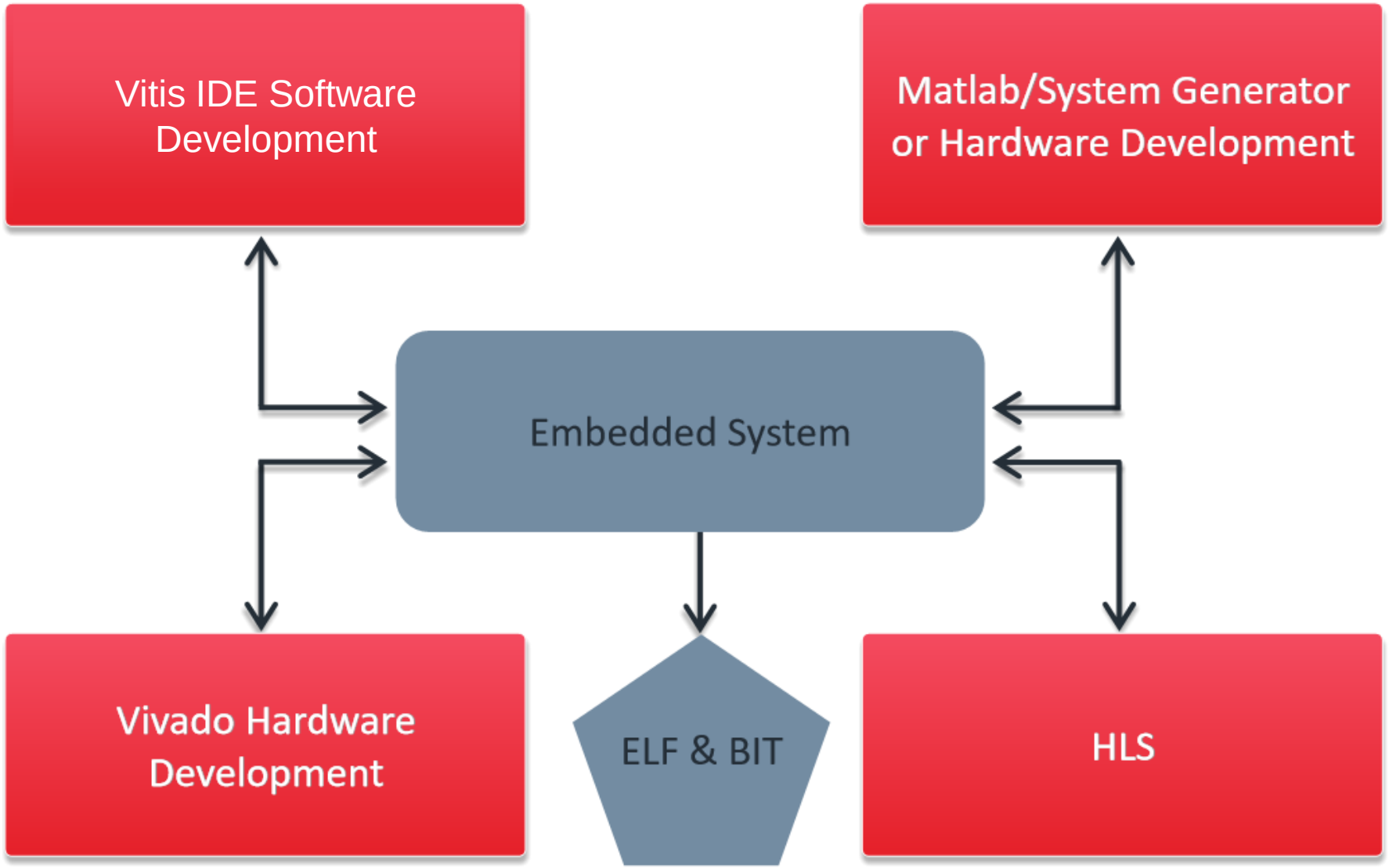


AMD
XILINX

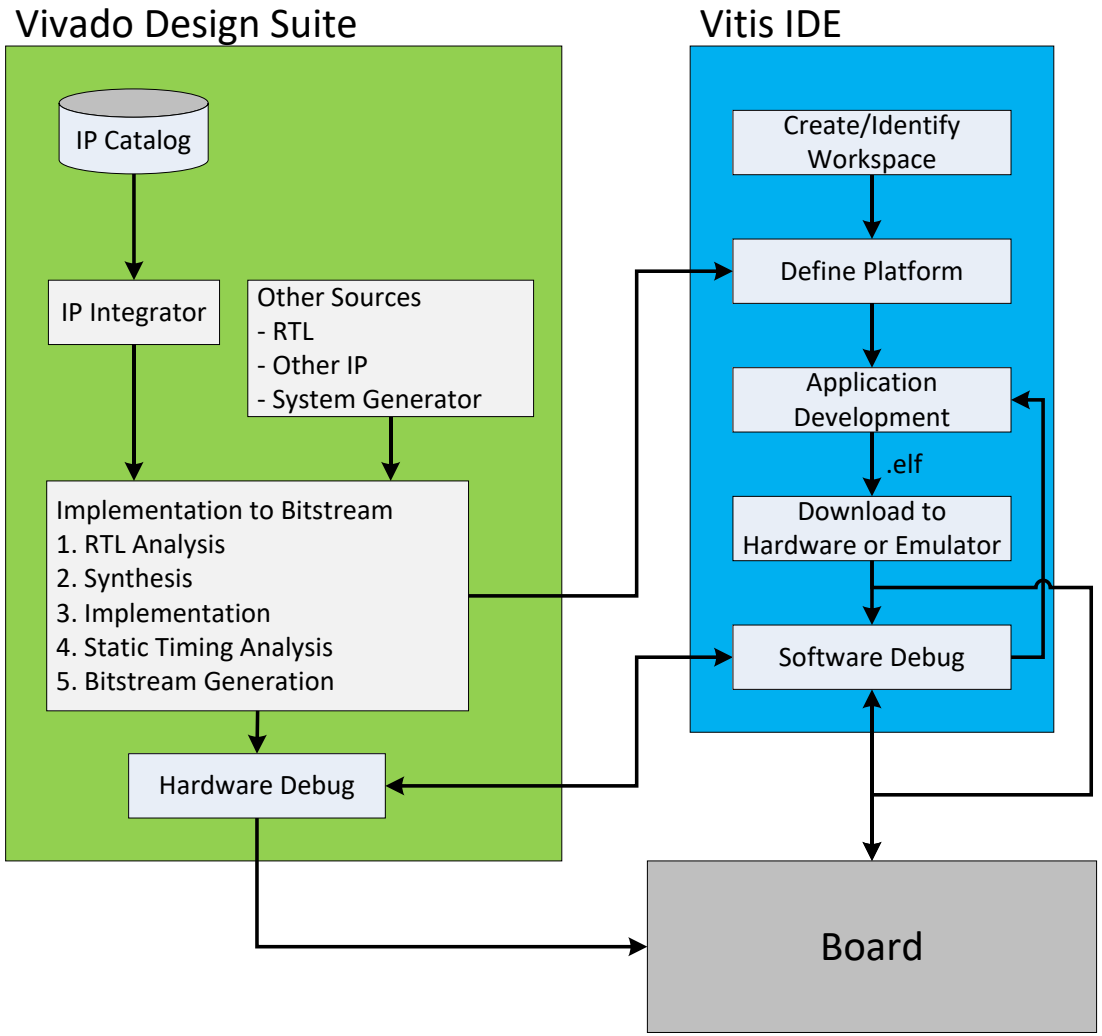
# Unifying Software Solutions: Vivado & Vitis



# Introduction to Embedded System Development



# Embedded System Design Flow for Zynq-7000 SoC



# Embedded System Tools: Hardware

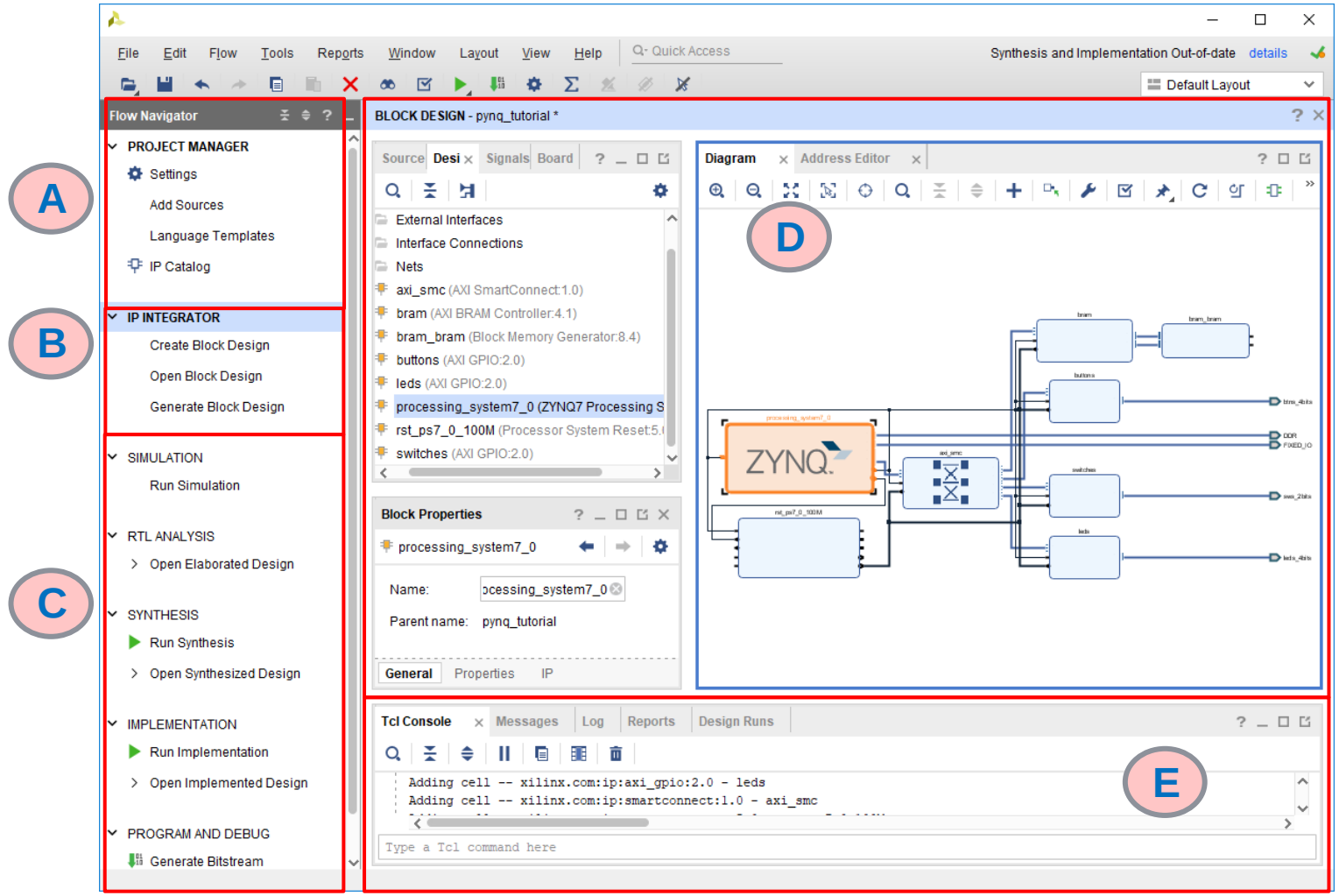
- **Hardware and software development tools**
  - IP Integrator
  - IP Packager
  - Hardware netlist generation
  - Simulation model generation
  - Hardware debugging using Vivado logic analyzer

# Embedded System Tools: Software

- **Eclipse IDE-based Software Development Kit (Vitis IDE)**
  - Board support package creation
  - GNU software development tools
  - C/C++ compiler for the ARM Cortex-A9 processors (gcc)
  - Debugger for the ARM Cortex-A9 processors (gdb)
  - TCF framework – multicore debug
- **Vitis Platform**
  - Stand-alone domain
    - Free basic device drivers and utilities from Xilinx
    - NOT an RTOS
    - Single-threaded
  - Operating system domain
    - Multi-threaded

# Vivado View

- **Customizable panels**
  - A: Project Management
  - B: IP Integrator
  - C: FPGA Flow
  - D: Project view/Preview Panel
  - E: Console, Messages, Logs



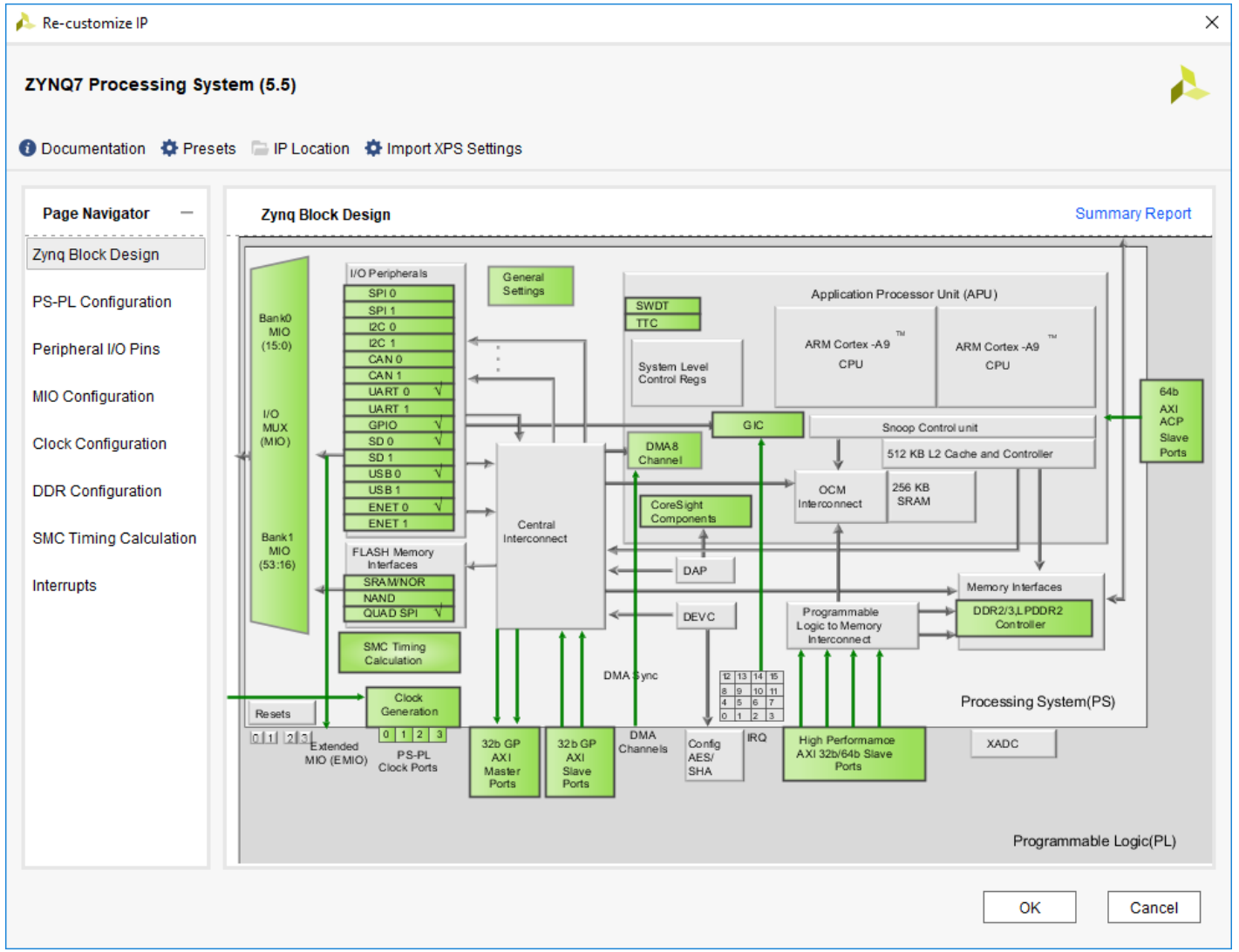





AMD XILINX

# Zynq Customization Processing System

- Zynq Block Design
- PS-PL Interface Configuration
- Peripheral I/O Pins
- MIO Configuration/Table View
- Clock Configuration
- DDR Configuration
- SMC Timing Calculation
- Interrupts

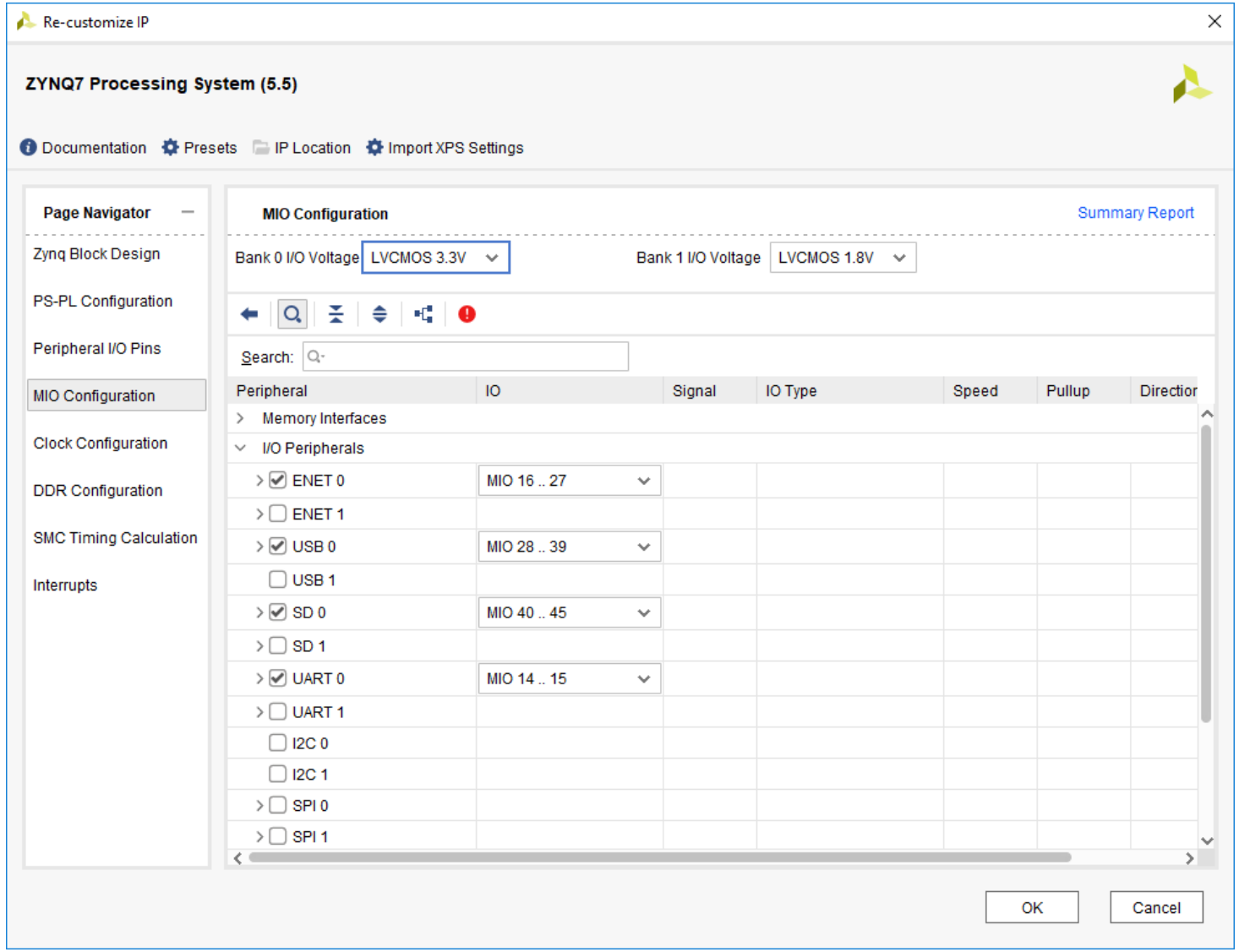




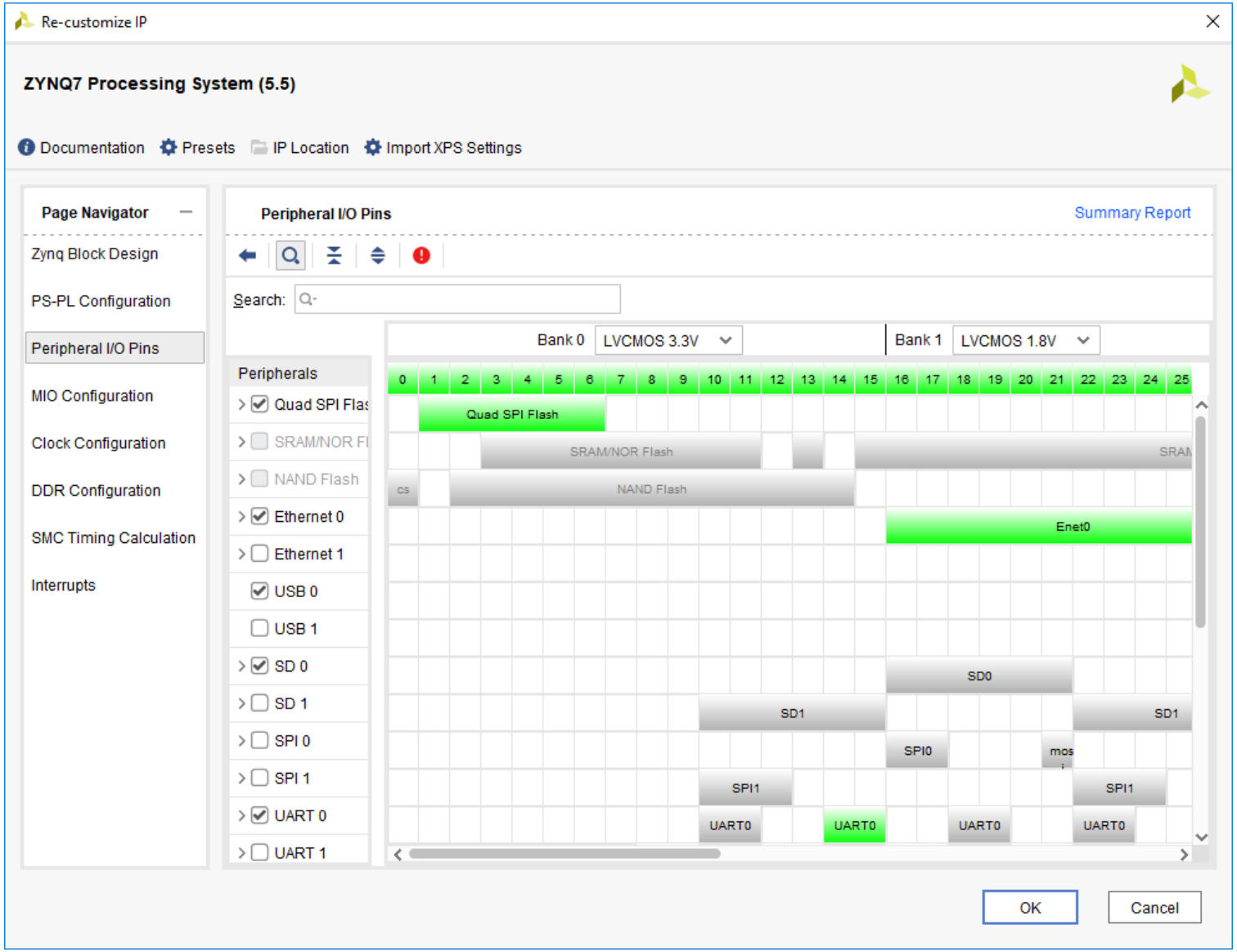



AMD XILINX

# MIO Configuration



# Peripheral I/O Pins



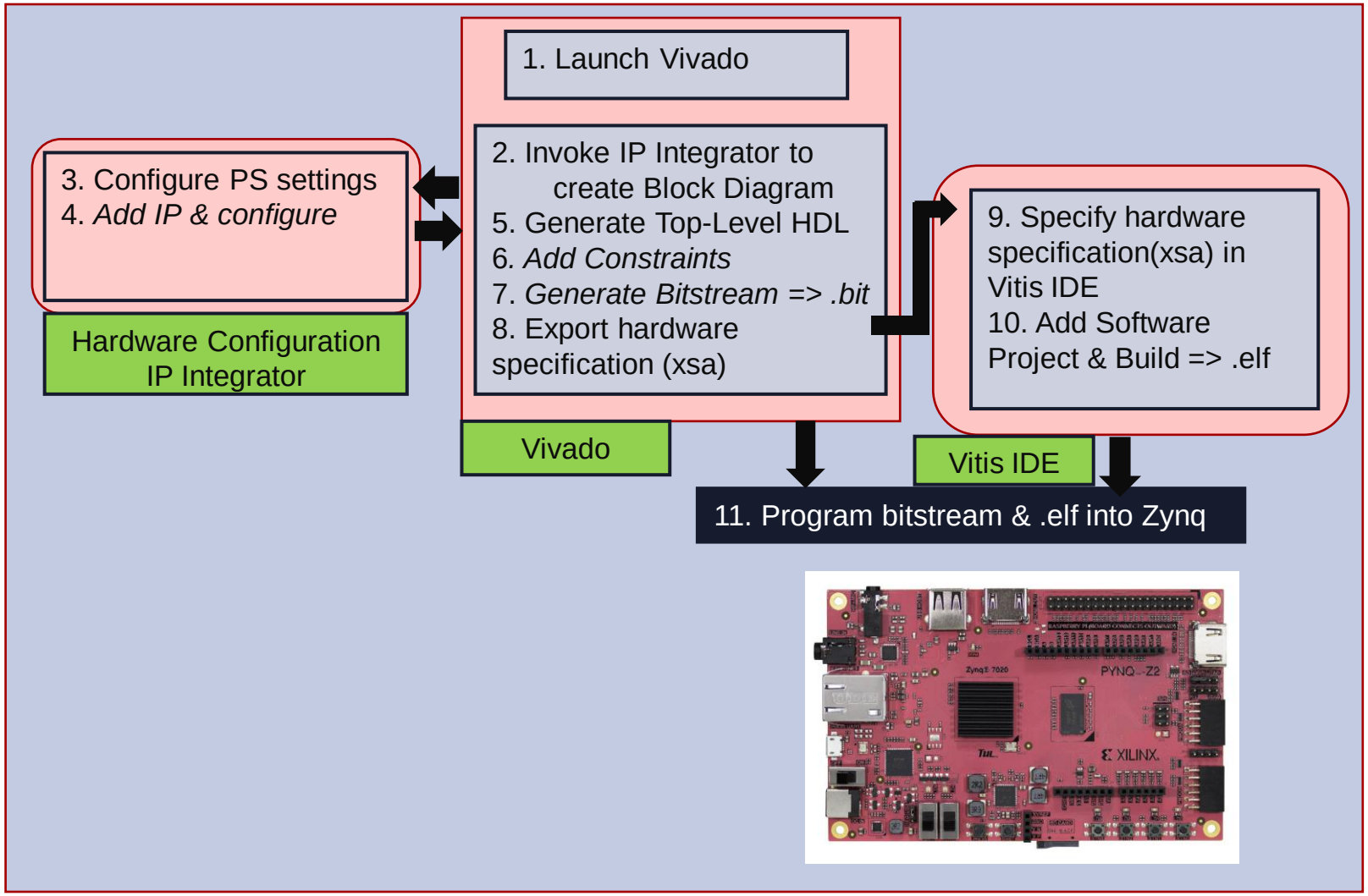





AMD XILINX

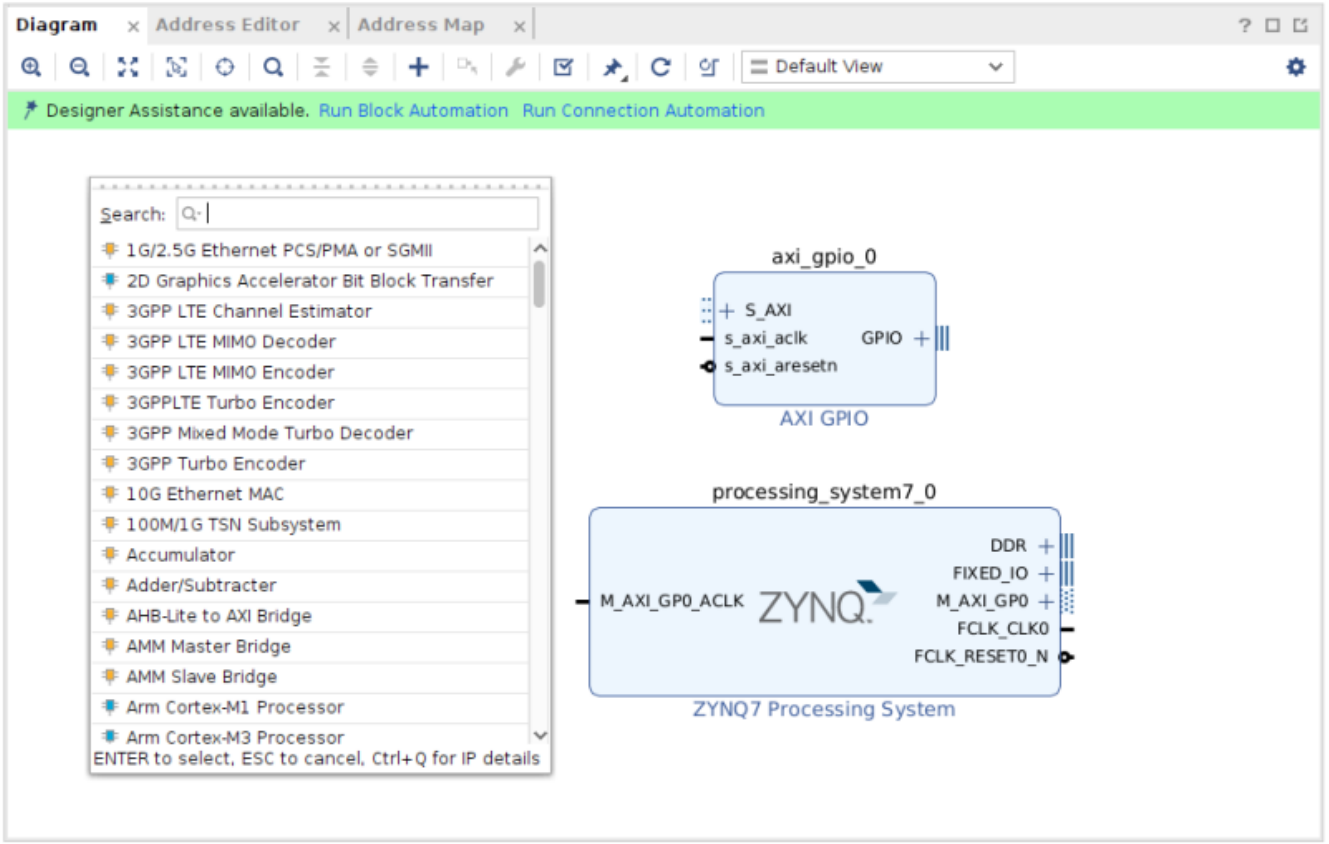
# Embedded System Development Flow

# Embedded System Design using Vivado



# Integrator Block Diagram

- IP Integrator Block Diagram opens a blank canvas
- IP can be added from the IP catalog
- Drag and drop interface
- Intelligent Design environment
  - Design Assistance
  - Connection automation
  - Highlights valid connections
  - Group, create hierarchal blocks
- Can create and import custom IP using IP Packager



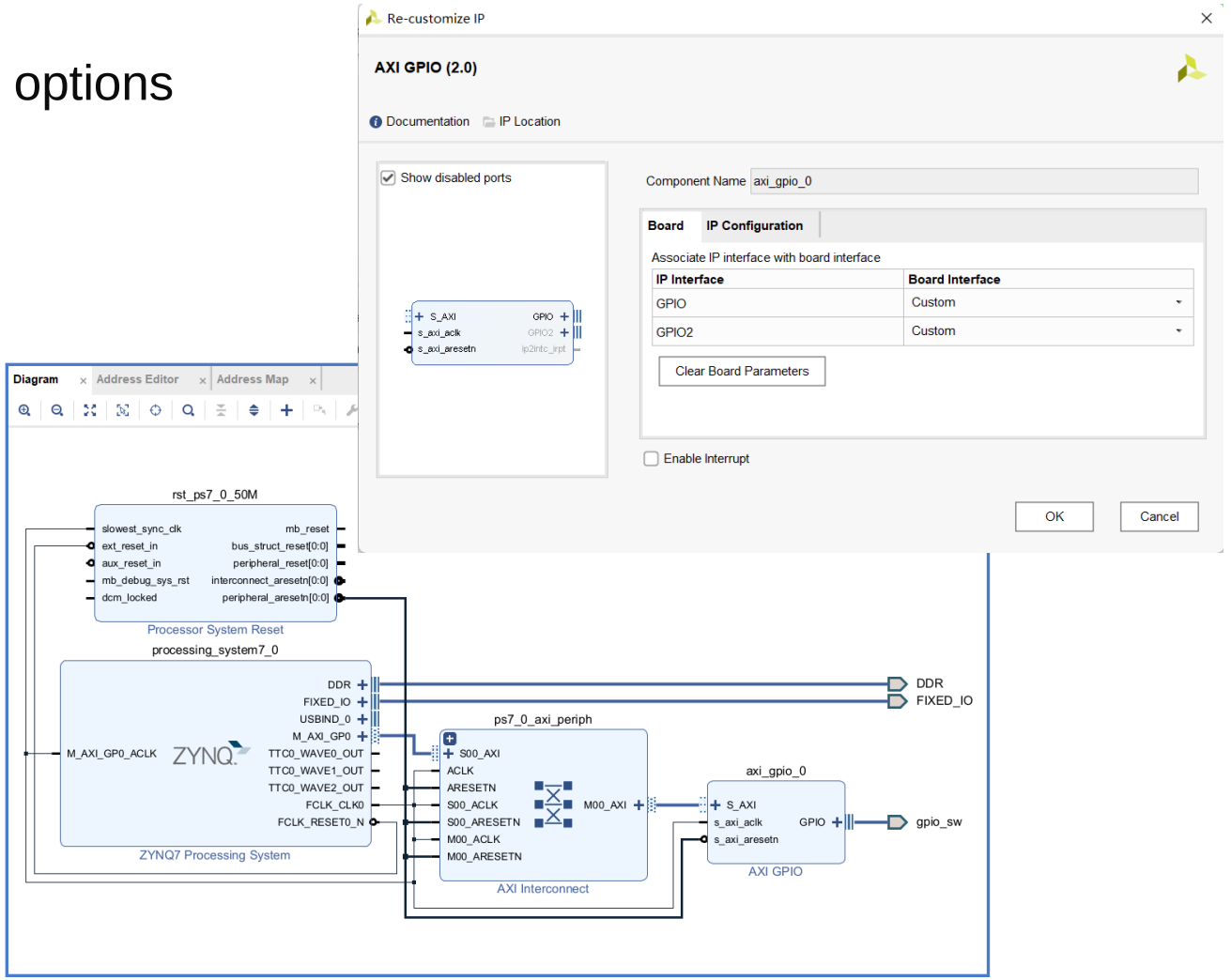





AMD XILINX

# Configuring Hardware in IP Integrator

- Double click blocks to access configuration options
- Drag pointer to make connections
  - Highlights valid connections
- Connection Automation
  - Automatically connect recognised interfaces
- Automatically Redraw system



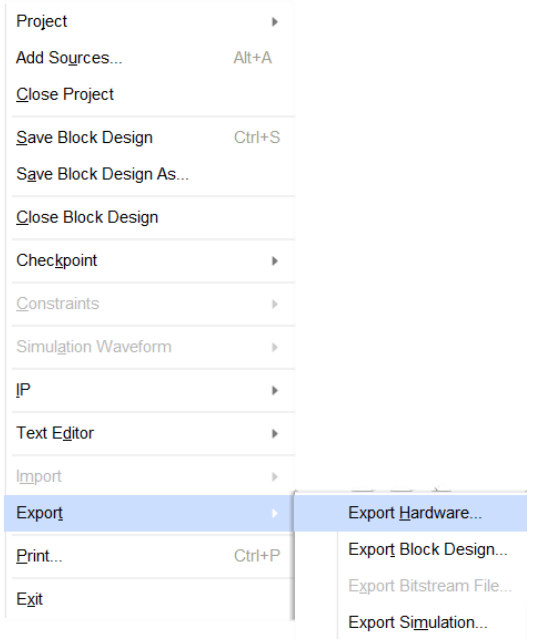


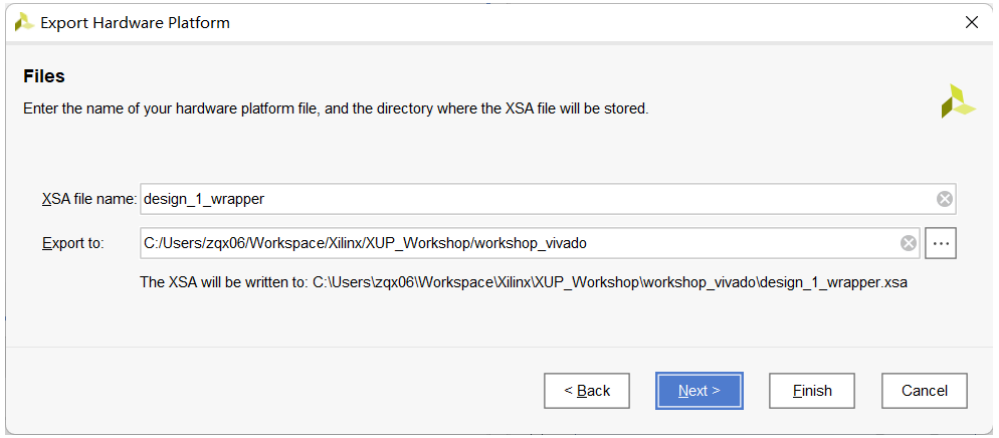



AMD XILINX

# Exporting to Vitis IDE

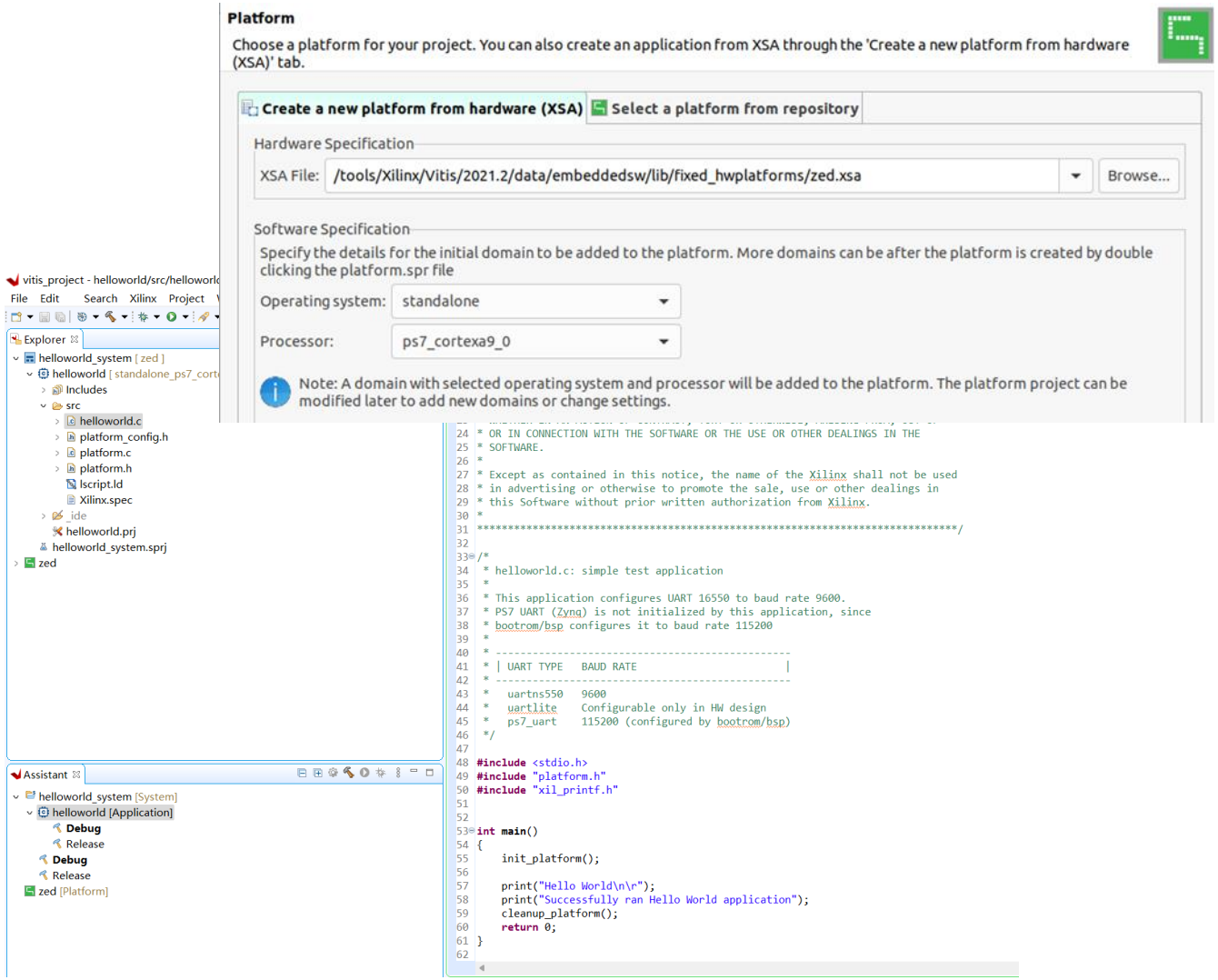
- Export hardware first
  - The Xilinx Shell Archive (XSA) is a container file that contains all the information needed to build a platform for a users target device
  - Include bitstream if generated
- Launch Vitis IDE
  - Software development is performed with the Vitis IDE



# Software Development Flow

- Create platform project
  - From XSA file
- Create system project
  - System software, board support package
- Create software application
- Create linker script
- Build project
  - compile, assemble, link output file *<app_project>.elf*



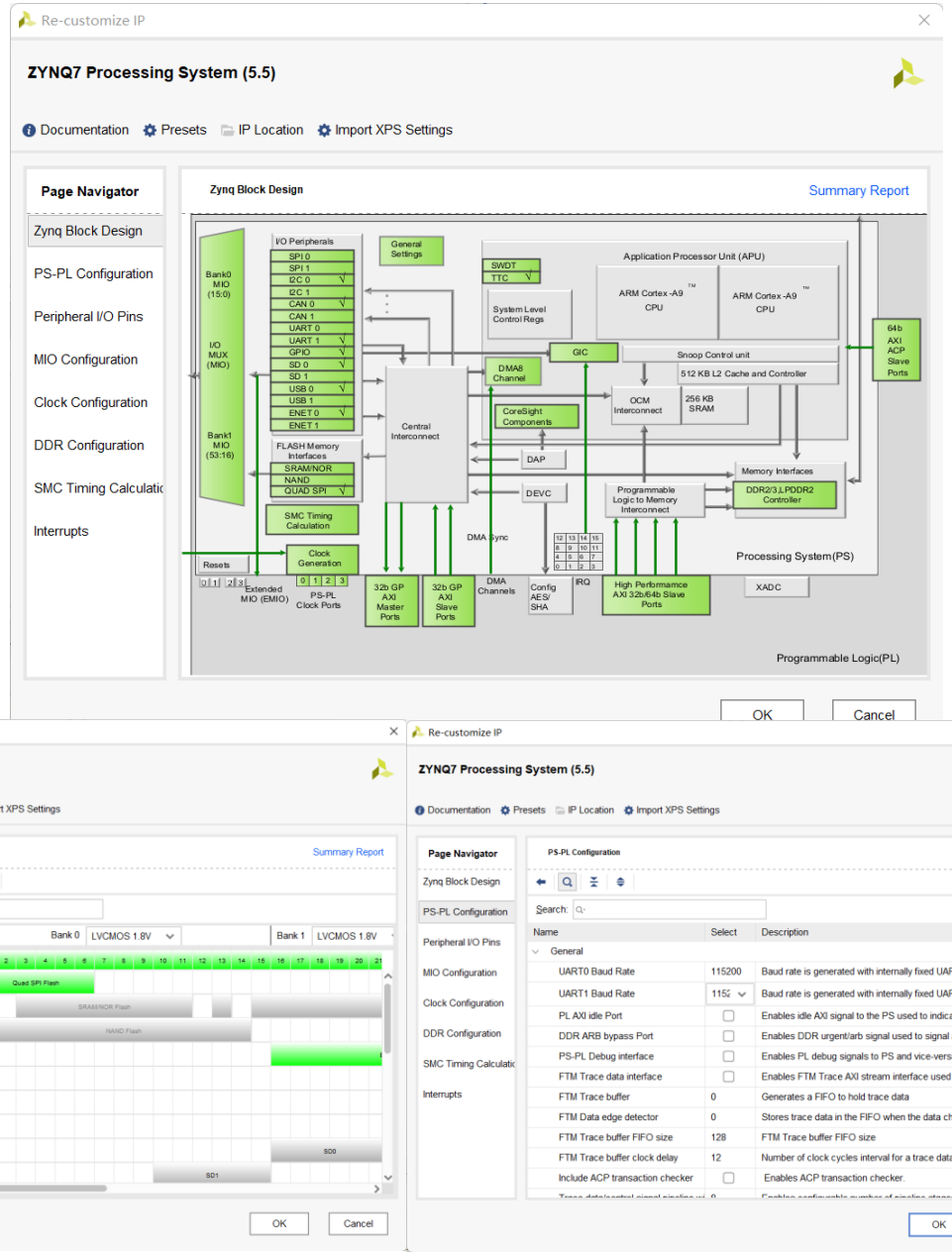
# Configuring FPGA and Downloading Application

- Download the bitstream
  - Only if PL is used
  - Input file <*top_name*>*.bit*
- The bitstream can be downloaded from either
  - Vivado
  - Vitis IDE
- Requires that the download cable is connected

# Hardware Platform

# Zynq Configuration GUI

- Provides a graphical view of the PS to configure
  - ARM cores
  - I/O peripherals
  - DDR controller
  - Memory systems
- I/O partitioning between dedicated PS pins and programmable logic I/O
- PS is configured via a set of memory-mapped configuration registers



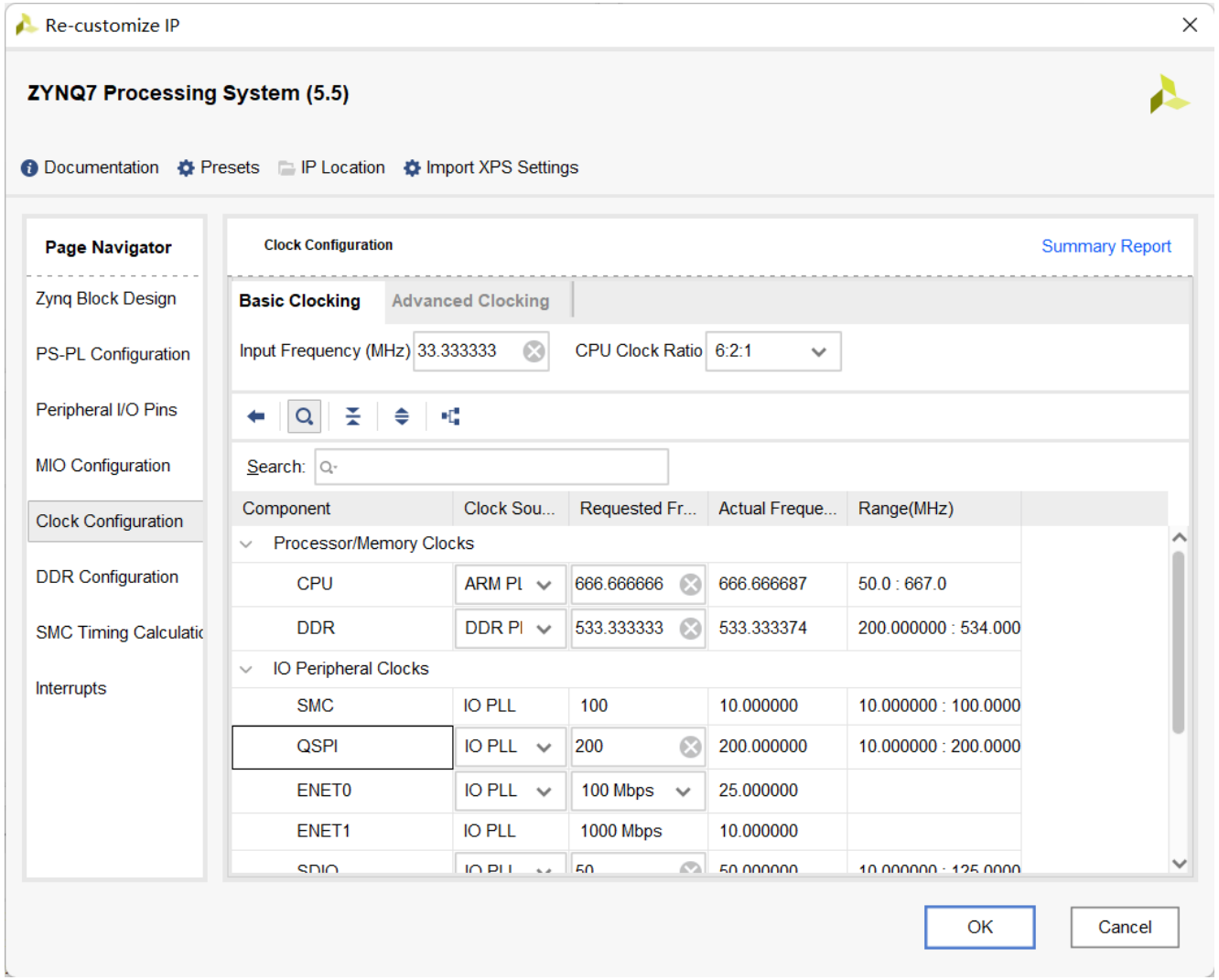





AMD XILINX

# Clock Configuration

- Clock Configuration
  - Input frequency can be set
    - Processor, DDR
  - All IOP clock frequencies can be set
  - PL fabric clocks can be enabled and configured
  - Set Timers



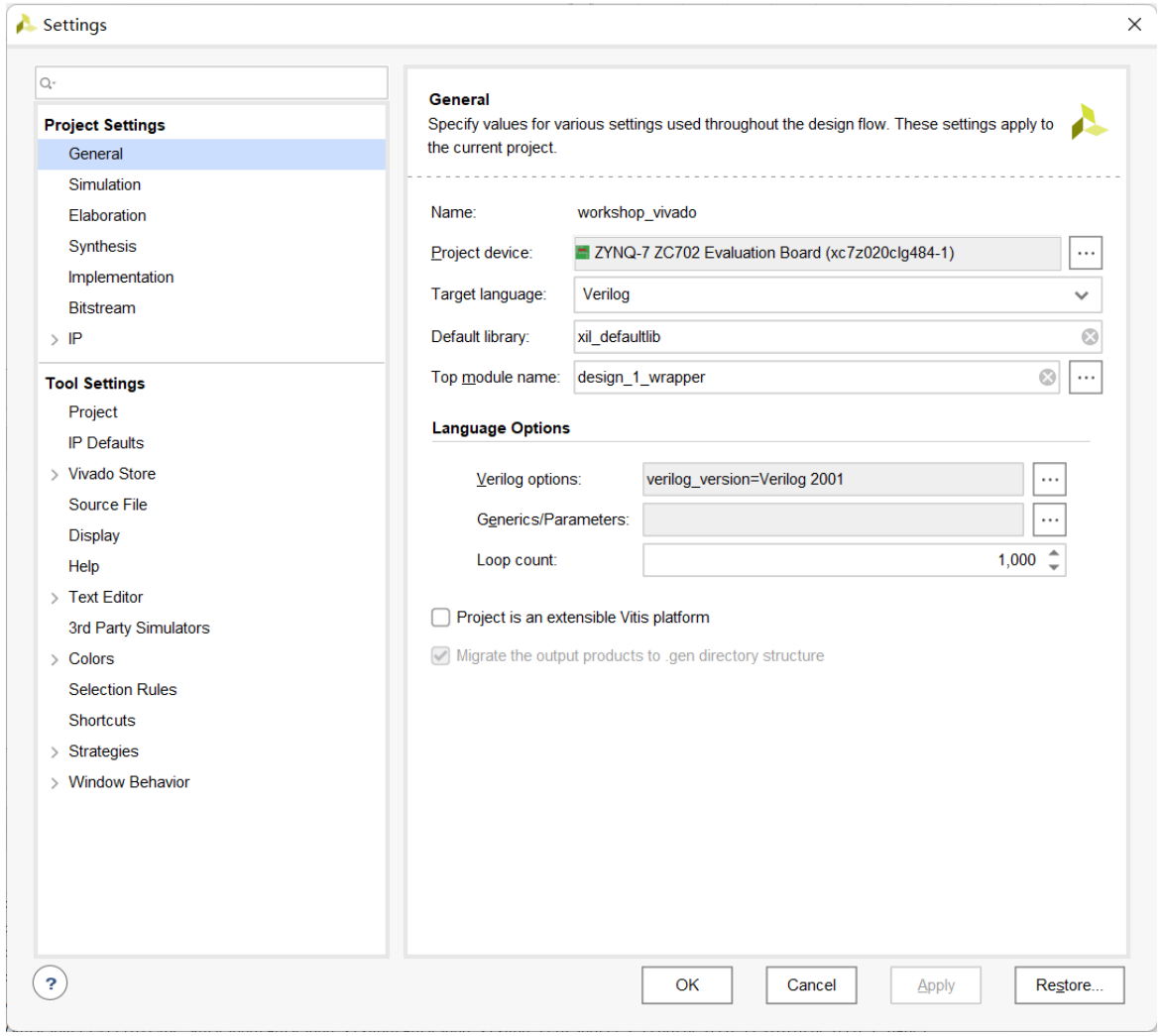





AMD XILINX

# Project Settings

- Accessed from flow navigator
- Default settings are typically used
- Set/change target device
  - Architecture, Device size, Package, Speed grade
- Simulation, Synthesis, Implementation, Bitstream options
- IP repository directory
  - Provide path to custom IP not present in the current project directory structure








AMD XILINX

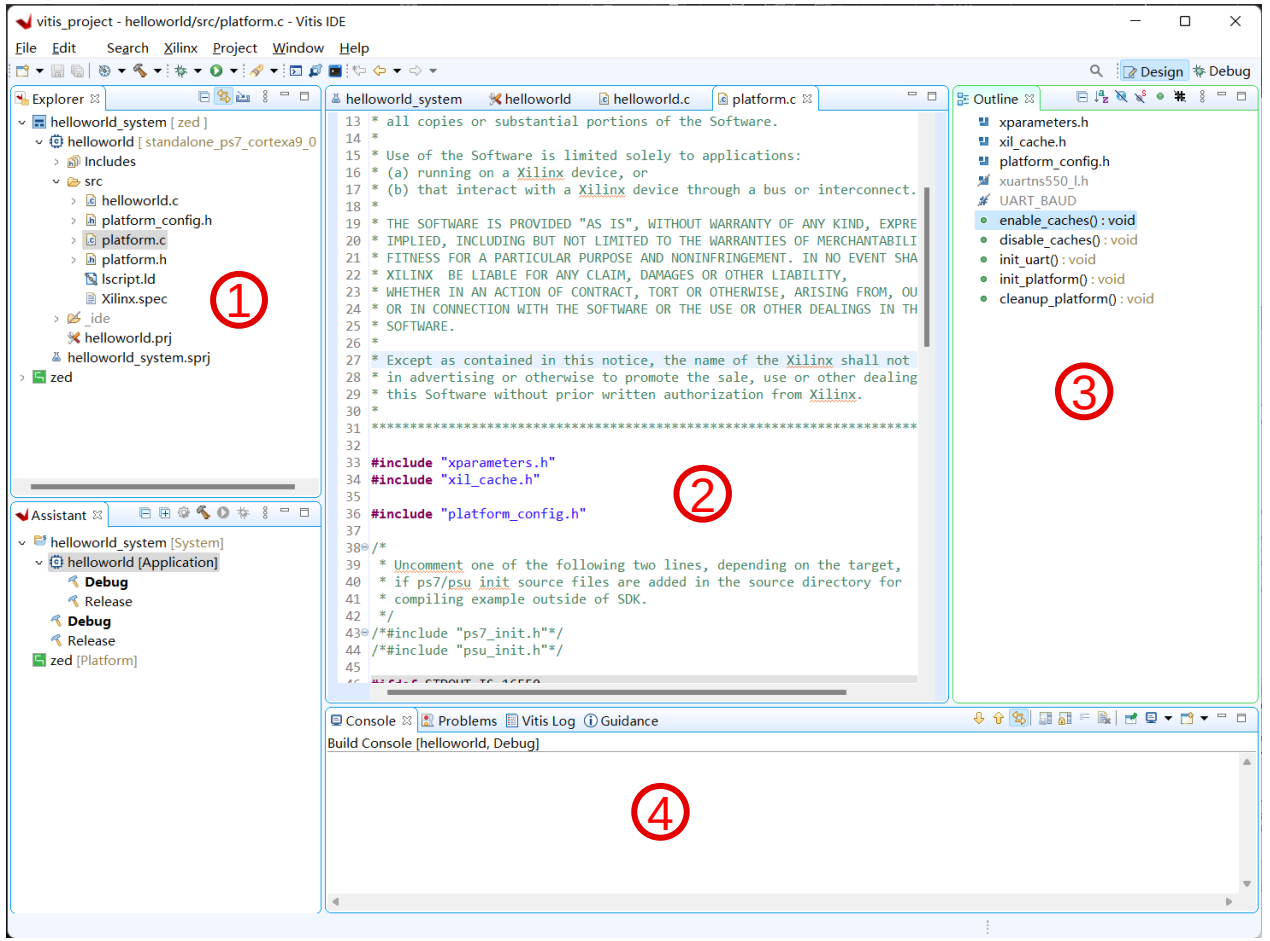
# Vitis IDE

# Vitis IDE

- The Vitis IDE is designed to be used for the development of embedded software applications targeted towards Xilinx embedded processors
- The Vitis IDE works with hardware designs created with the Vivado Design Suite
- The Vitis IDE is built upon the Eclipse open-source IDE, which is Java based—enabling the running under both Windows and Linux
- The Eclipse platform is extensible,  enabling Xilinx to add new capabilities to support the Vitis design environment, which makes developing code for the various SoC families much easier
  - Includes a collection of commonly used templates for first stage boot loaders, C, and C++ applications, specialized firmware, board support packages
  - These applications are automatically added to the platform and remove the need for the user to add these aspects manually
- Platform-oriented development enables the user to develop large and complex applications targeting specific processors or groups of processors within the hardware

# Vitis IDE Workbench Views

1. C/C++ project outline displays the elements of a project with file decorators (icons) for easy identification
2. C/C++ editor for integrated software creation
3. Code outline displays elements of the software file under development with file decorators (icons) for easy identification
4. Problems, Console, Properties views list output information associated with the software development flow



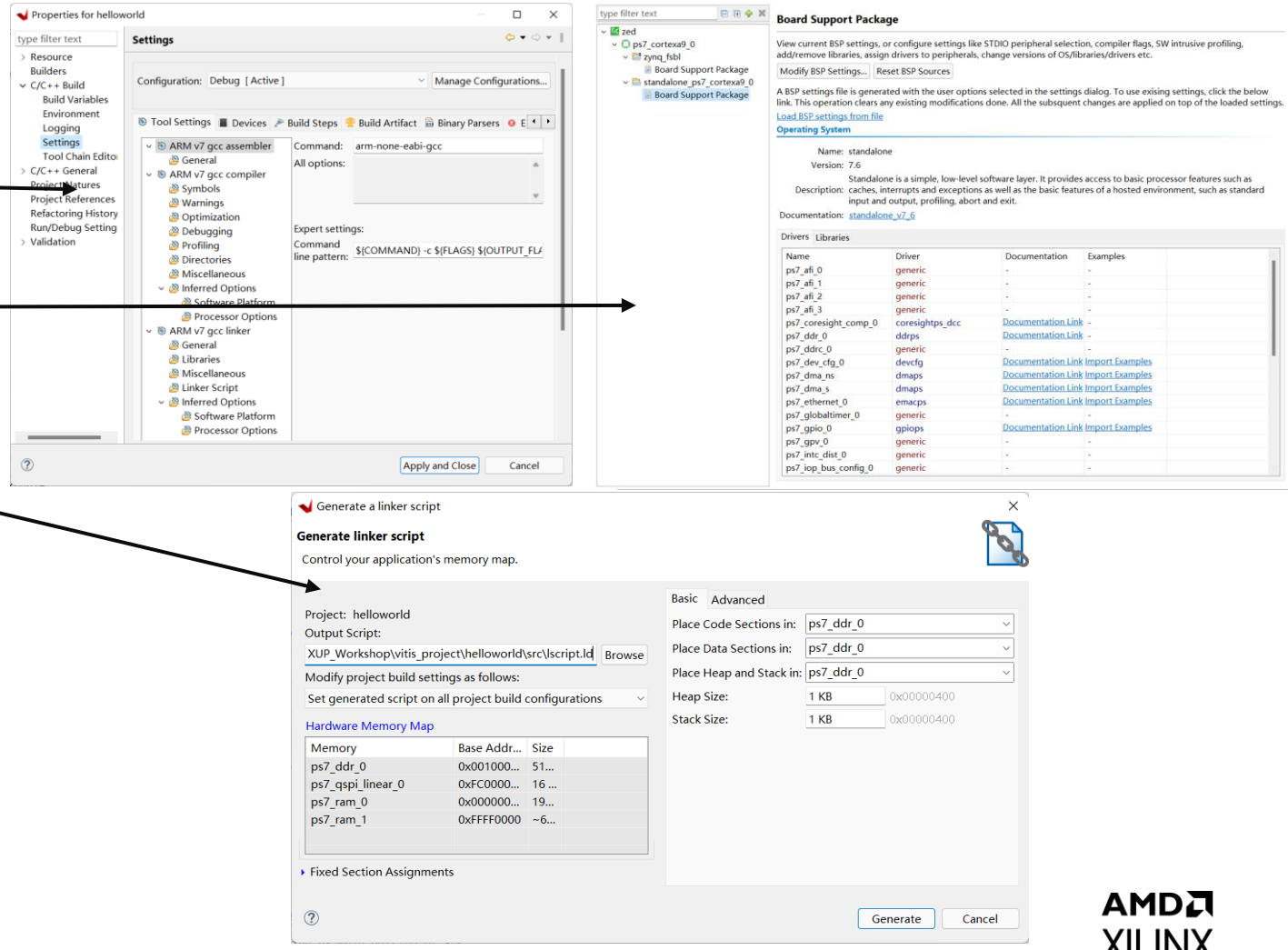





AMD XILINX

# Software Management Settings

- Software is managed in three major areas
  - Compiler/Linker Options
    - Application program
  - Software Platform Settings
    - Board support package
  - Linker Script Generation
    - Assigning software to memory resources
- Covered in more detail later








AMD XILINX

# Summary

# Summary

- Vivado includes all the tools, documentation, and IP necessary for building embedded systems
- IPI is a System Level design tool that increases productivity, allowing designs to be completed faster
- The Vitis IDE is a comprehensive software development environment for software applications
- An embedded processing system component is built with IP provided in the IP Catalog
  - Designers can also add their own custom IP to this catalog
- The PS Configuration wizard permits access to several configurable features of PS


# Thank You

# Disclaimer and Attribution



AMD
XILINX