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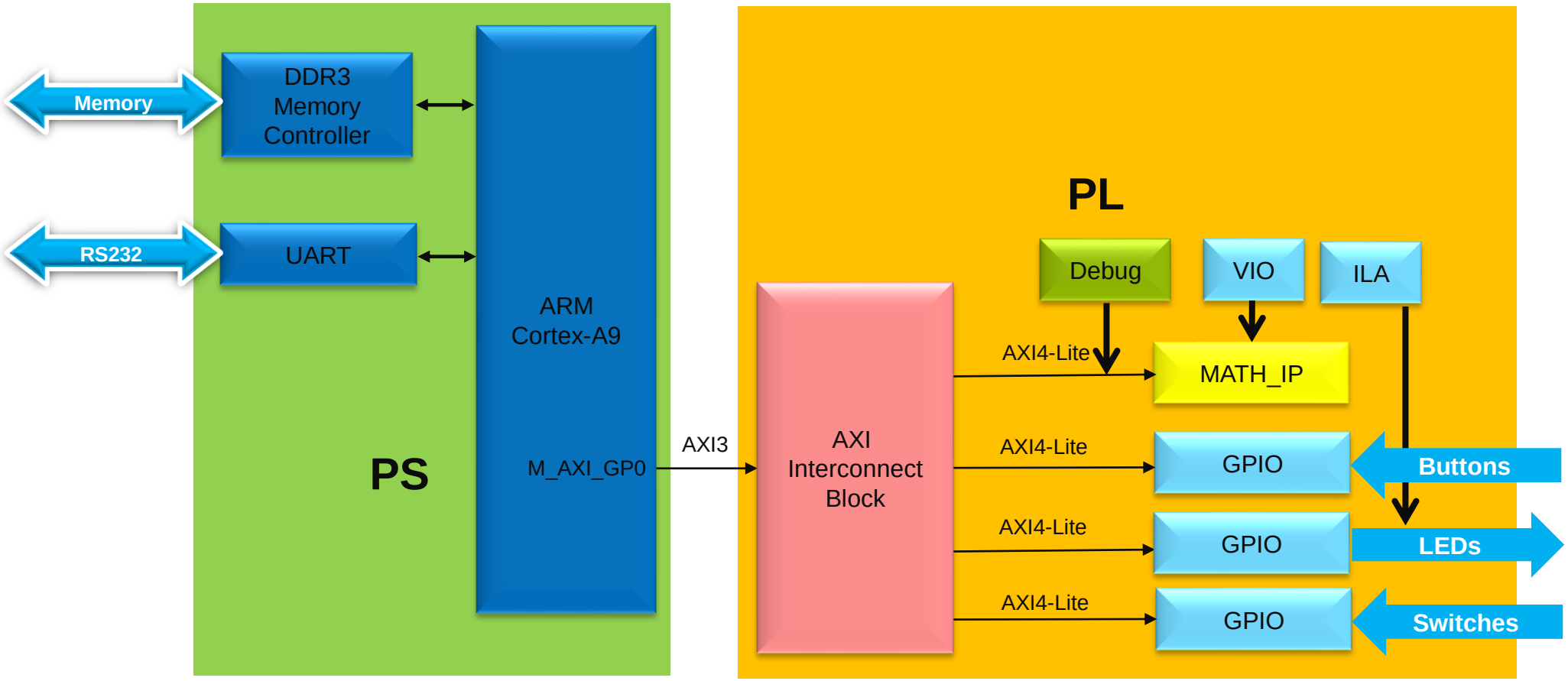
Lab6 Intro
Debugging Using Vivado Logic Analyzer

Introduction

- Software and hardware interact with each other in an embedded system.
- The Vitis includes System Debugger as software debugging tool.
- The Vivado logic analyzer tool allows for hardware debugging by providing access to the internal signals, using number of cores, without necessarily bringing them out via the package pins using several types of cores.
- These cores may reside in the programmable logic (PL) portion of the device and can be configured with several modes that can monitor signals within the design.
- Vivado provides capabilities of marking any net at several stages of the design flow. In this lab you will be introduced to various debugging cores.

ARM Cortex-A9 based Embedded System Design Debugging using Logic Analyzer Cores and Mark Debug



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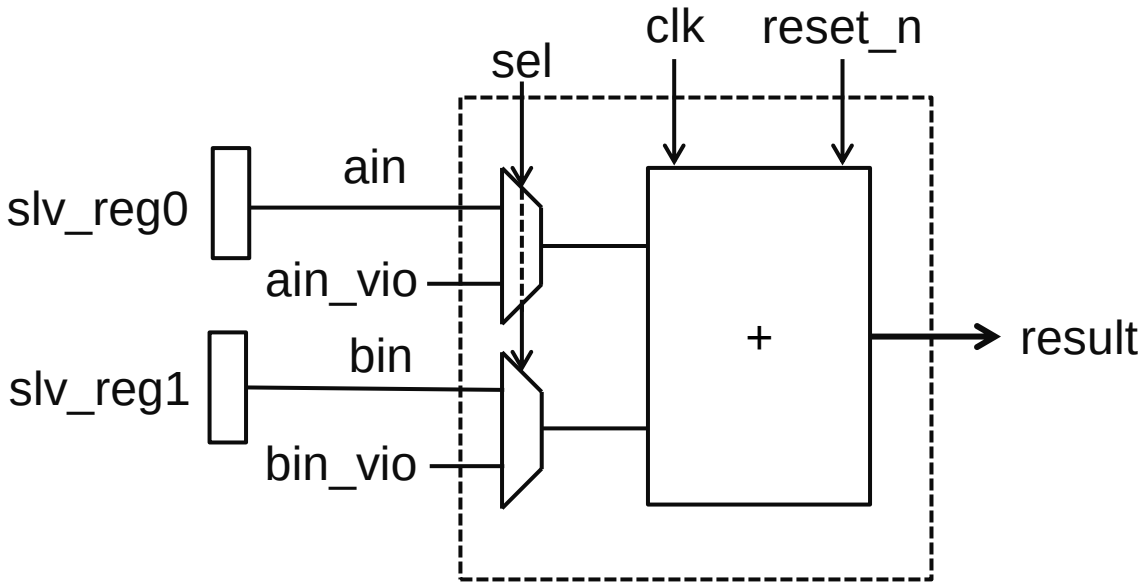
The Custom IP – MATH_IP



Procedure

- Open lab1 Vivado project and save as lab2
- Add the provided custom IP
- Add the VIO and ILA cores
- Synthesize the design and assign the S_AXI nets for debugging
- Generate the bitstream
- Generate the application in the Vitis IDE
- Test and debug in design in hardware

Summary

- In this lab, you added a custom core with extra ports so you can debug the design using the VIO core.
- You instantiated the ILA and the VIO cores into the design.
- You used Mark Debug feature of Vivado to debug the AXI transactions on the custom peripheral.
- You then opened the hardware session from Vivado, setup various cores, and verified the design and core functionality using Vitis and the logic analyzer.
- Finally, you carried out cross triggering between hardware and software.

Thank You

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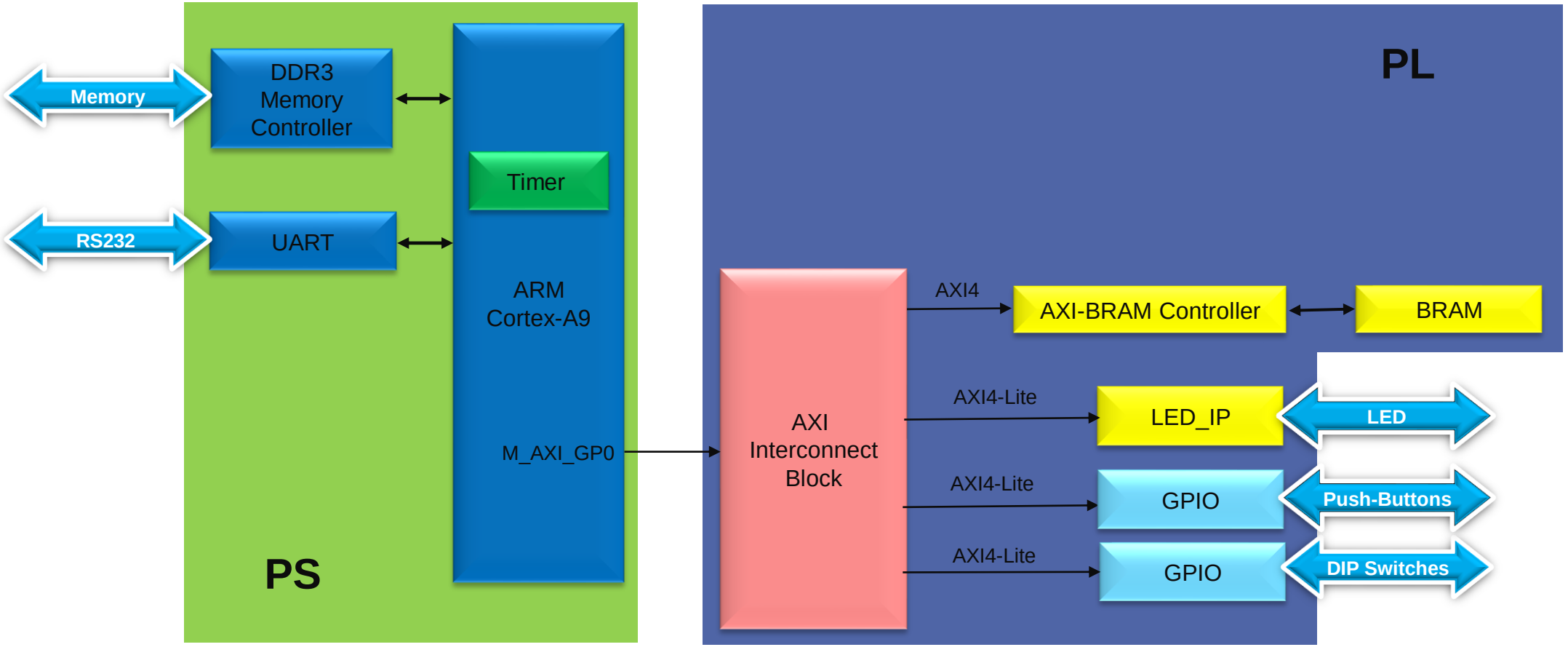
Introduction

- This lab guides you through the process of writing a software application that utilizes the private timer of the CPU.
- You will refer to the timer's API in Vitis to create and debug the software application.
- The application you will develop will monitor the dip switches settings and increment the count on LED.
- The application will exit when the center push button is pressed.

Lab5: Utilize system timer and perform software debugging



Procedure

- Open the project in Vivado
- Create an Vitis Software Project
- Verify Operation in Hardware
- Launch Debugger

Summary

- This lab led you through developing software that utilized the CPU's private timer.
- You studied the API documentation, used the appropriate function calls and achieved the desired functionality.
- You verified the functionality in hardware. Additionally, you used the Vitis debugger to view the content of variables and memory, and stepped through various part of the code.

Thank You

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