



Lab7 Intro

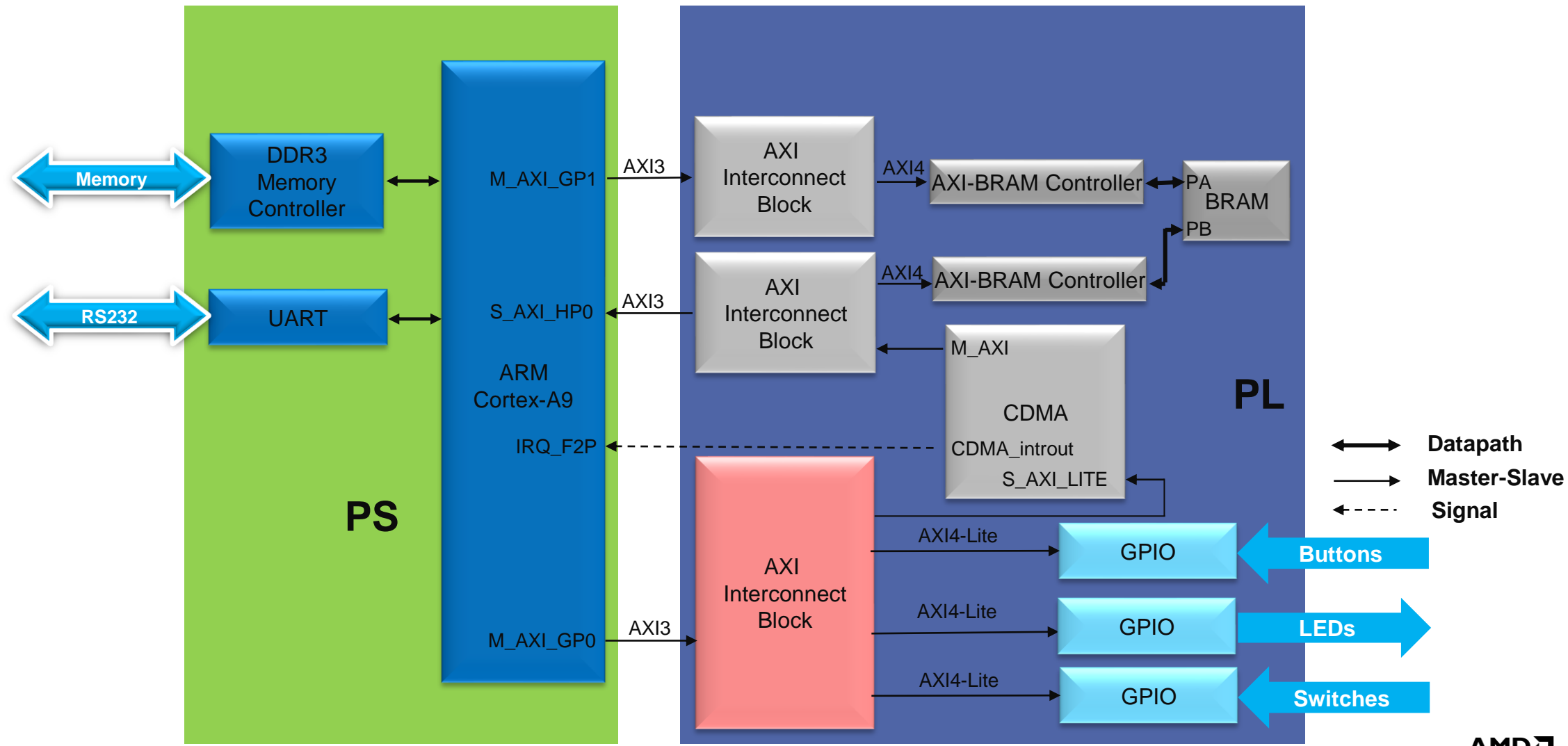
Direct Memory Access using CDMA

Introduction

- ▶ In Zynq, multiple interconnections are available between the PS and PL sections with different performance levels for data transfer between the two subsystems.
- ▶ General Purpose (GP) Master and Slave AXI interconnect
 - Intended for peripherals that do not have high bandwidth requirements.
 - E.g., switches, leds, keyboard, mouse.
- ▶ 4x High Performance PS slave to PL master AXI interfaces
 - For peripherals that need higher bandwidth
 - E.g., Video and image processing applications.
- ▶ This lab guides you through the process of enabling a High Performance AXI slave port in the PS, adding an AXI central DMA (CDMA) controller, and performing Direct Memory Access (DMA) operations between various memories.

ARM Cortex-A9 based Embedded System Design

Direct Memory Access using CDMA



Procedure

- ▶ Open the project
- ▶ Configure the processor to enable S_AXI_HP0 interface
- ▶ Add CDMA and BRAM
- ▶ Create the wrapper and generate the bitstream
- ▶ Generate an application in the Vitis IDE
- ▶ Test the design using the board

Summary

- ▶ This lab led you through adding a CDMA controller to the PS so that you can perform DMA transfers between various memories.
- ▶ You used the high-performance port so DMA could be done between the BRAM residing in the PL section and DDR3 connected to the PS.
- ▶ You verified the design functionality by creating an application and executing it from the DDR3 memory.



Thank You

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