AMD
XILINX

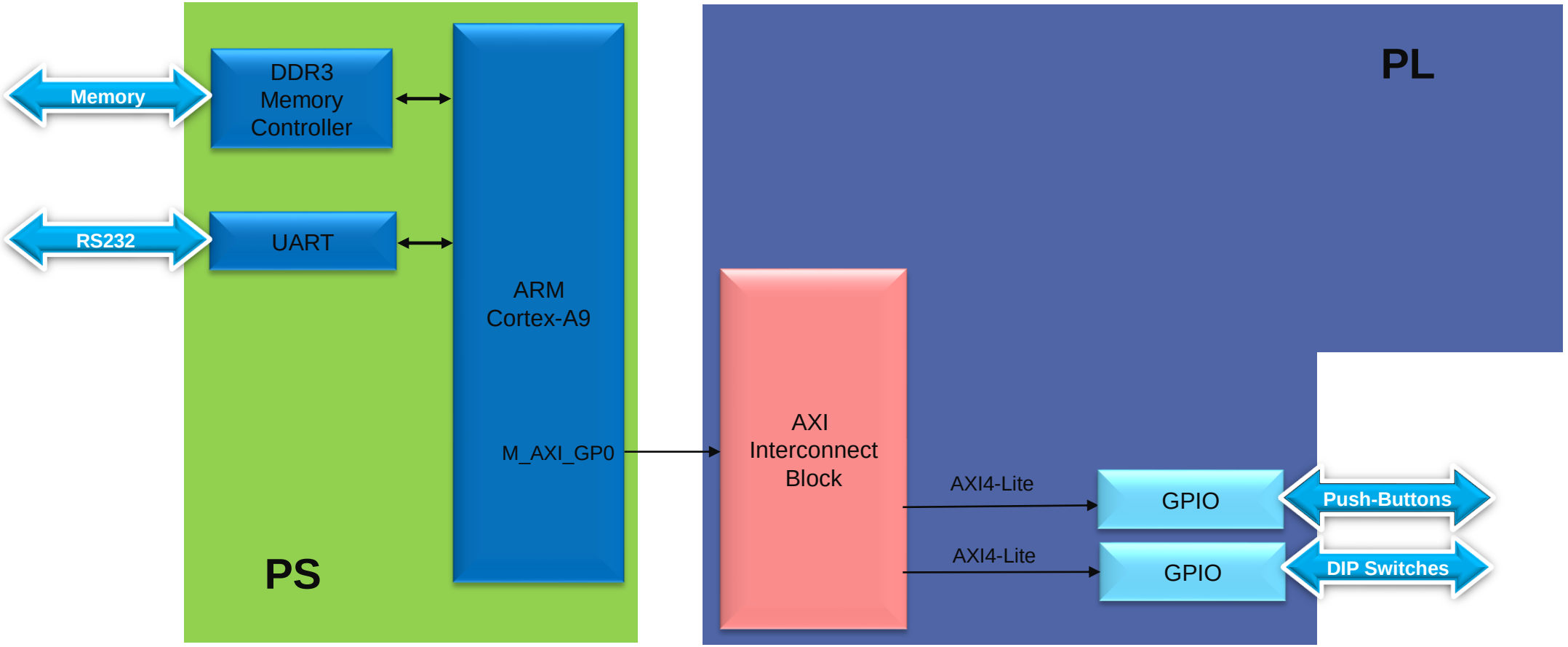
# Lab2 Intro
# Adding IP in PL

2021.2

# Introduction

- This lab guides you through the process of extending the processing system you created in the previous lab by adding two GPIO IPs in PL

# ARM Cortex-A9 based Embedded System Design
# Lab2: Adding IPs in PL








AMD
XILINX

# Procedure

- Open the project in Vivado
- Add and configure GPIO peripherals in the system in the IP Integrator
- Add external ports
- Generate the bitstream and export to Vitis
- Create a TestApp application in Vitis IDE
- Verify the functionality in hardware

# Summary

- The GP Master interface of the PS was enabled. GPIO peripherals were added from the IP catalog and connected to the Processing System through the 32b Master GP interface.
- The peripherals were configured and external FPGA connections were established.  Pin location constraints were made using IP Integrator Automation, and also manually, to connect the peripherals to push buttons and DIP switches.
- A TestApp application project was created and the functionality was verified after downloading the bitstream and executing the program.


# Thank You

# Disclaimer and Attribution



AMD
XILINX