



Embedded Systems Design Flow using Zynq

Course Objectives

- ▶ After completing this course, you will be able to:
 - Design the architecture of an embedded system targeting Zynq using Vivado IP Integrator
 - Extend the system by adding peripherals
 - Add Xilinx provided peripherals from the IP catalog
 - Create and add a custom peripheral using IP Integrator
 - Create and debug software applications using Vitis software development tool

Course Outline

Day 1

The course consists of the following modules:

- ▶ Introduction to Embedded System Design Flow using Zynq
- ▶ Lab 1: Simple Hardware Design
- ▶ Zynq Architecture
- ▶ Extending the Embedded System into PL
- ▶ Lab 2: Adding IPs in Programmable Logic
- ▶ Adding Your Own Peripheral
- ▶ Lab 3: Creating and Adding Custom IP

Course Outline

Day 2

- ▶ Software Development Environment
- ▶ Lab 4: Writing Basic Software Applications
- ▶ Software Development and Debugging
- ▶ Lab 5: Software Debugging Using Vitis

Prerequisites

- ▶ Familiarity with the FPGA design flow
- ▶ Basic C programming
- ▶ Basic understanding of processor-based system
- ▶ Basic HDL knowledge

Platform Support

- ▶ Vitis 2021.2 software development tool
- ▶ PYNQ-Z2 board
- ▶ Minimum System Requirements (UG1400)
 - Windows 10 Professional (64-bit)
 - Red Hat Enterprise Linux 8.48.3, 8.4 (64 Bit)
 - Cent OS 7.4, 7.5, 7.6, 7.7, 7.8, 7.9, 8.1, 8.2, 8.3 (64 Bit)
 - Ubuntu Linux 16.04.5 LTS, 16.04.6 LTS, 18.04.1 LTS, 18.04.2 LTS, 18.04.3 LTS, 18.04.4 LTS, 18.04.5 LTS, 20.04 LTS, 20.04.1 LTS, 20.04.2 LTS (64 Bit)
 - Amazon Linux 2 AL2 LTS (64-bit)
 - SUSE Linux Enterprise 11.4 and 12.3 (64 Bit)
 - 32 GB memory (64 GB recommended)



Thank You

Disclaimer and Attribution

The information contained herein is for informational purposes only and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale. GD-18

© Copyright 2022 Advanced Micro Devices, Inc. All rights reserved. Xilinx, the Xilinx logo, AMD, the AMD Arrow logo, Alveo, Artix, Kintex, Kria, Spartan, Versal, Vitis, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Advanced Micro Devices, Inc. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

