NEW GENERATION MOTORS CORPORATION

Washington, D.C. U.S.A

EVC402 Controller
OPERATING MANUAL

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Document Revision Record		
Rev:	Date:	Description of Change
-	2003-03-03	First Issue
A	2003-03-20	Removed all references to VC_Kt. Fixed erroneous mode switch commands in section 8.3. Changed description of VC_discrete bit 2. Some editing for clarity.
B	2003-11-12	Corrected factory setting of register 80B bit 5 (MF_mtrsensors) and register 80D (MF_pwmfreq). Added serial cable schematics section.
C	2004-05-14	Corrected description of FA2_threxcite and FA2_rgnexcite in section 5.1.3
D	2005-02-14	Changed number of stop bits in section 4.6

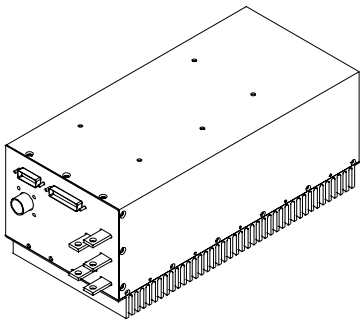
Table of Contents

1 Introduction

The New Generation Motors (NGM) EVC402 motor controller integrates years of advanced development and the latest in high-efficiency MOSFETs.

The EVC402 controller uses breakthrough technology to smoothly transition from trapezoidal control at low-speed to efficient sinusoidal control at higher speeds. Slew-rate control eliminates the noise and vibration associated with six-step control and reduces eddy-current losses. Advanced MOSFETs reduce conduction losses by over 40%.

Standard features include:



- ◊ *Environmentally sealed to IP65 when properly connected.*
- ◊ *Mechanically and electrically interchangeable with the EV-C200 (software changes needed for serial port interface).*
- ◊ *Designed especially for the SCM150 wheel motor.*
- ◊ *Efficient fixed-frequency space-vector control.*
- ◊ *Motor Current Limiting (MCL) logic limits battery charge and discharge current based on battery voltage.*
- ◊ *High-speed over-voltage detection protects controller against instantaneous battery disconnection, even under regenerative braking.*
- ◊ *State-Of-Charge tracking with programmable battery profile.*
- ◊ *Flexible battery current measurement circuit utilizes external high or low-side current shunt.*
- ◊ *Serial Interface for configuration, control, and data acquisition.*

1.1 SPECIFICATIONS

Dimensions are without fans and connectors.

	EVC402-092
Peak RMS Phase Current (Amps)	145
Peak Phase Current, Trapezoidal Mode (Amps)	175
Nominal Bus Voltage (Volts)	66-108
Min./Max. Operating Voltage (Volts)	50/135
Maximum Withstand Voltage (Volts)	160
Input Capacitance (uF)	12,000
Peak Efficiency %	99
Height (mm/in.)	135/5.29
Width (mm/in.)	156/6.13
Length (mm/in.)	332/13.06
Weight (kg/lbs)	4.9/10.75

1.2 KEY FEATURES OF THE EVC402 CONTROLLER

- Full I/O isolation from batteries
- Ultra high efficiency
- Synchronous switching
- Fixed-frequency space vector control
- Regenerative braking
- Active discharge circuit
- Instrumentation data available through serial port:
  - Battery voltage
  - Battery current
  - State-Of-Charge
  - Motor speed and temperature
  - Controller temperature
  - Drive state
  - Hours of operation
  - Throttle position
  - Brake position
- Programmable torque or speed control
- Programmable thermostatic fan control with internal power supply
- Low power sleep mode when disabled
- Built-in protection features:
  - Extreme over/under voltage protection
  - Motor interface connection verification
  - Thermal limiting protection
  - Over- and under- voltage limiting with soft shutdown
  - Abrupt start-up inhibition
  - Programmable Battery Protection
  - User configurable Throttle input based on speed
  - Speed Governor
  - Reverse Speed Limiting

1.3 FRONT PANEL INTERFACE OF THE EVC402 CONTROLLER

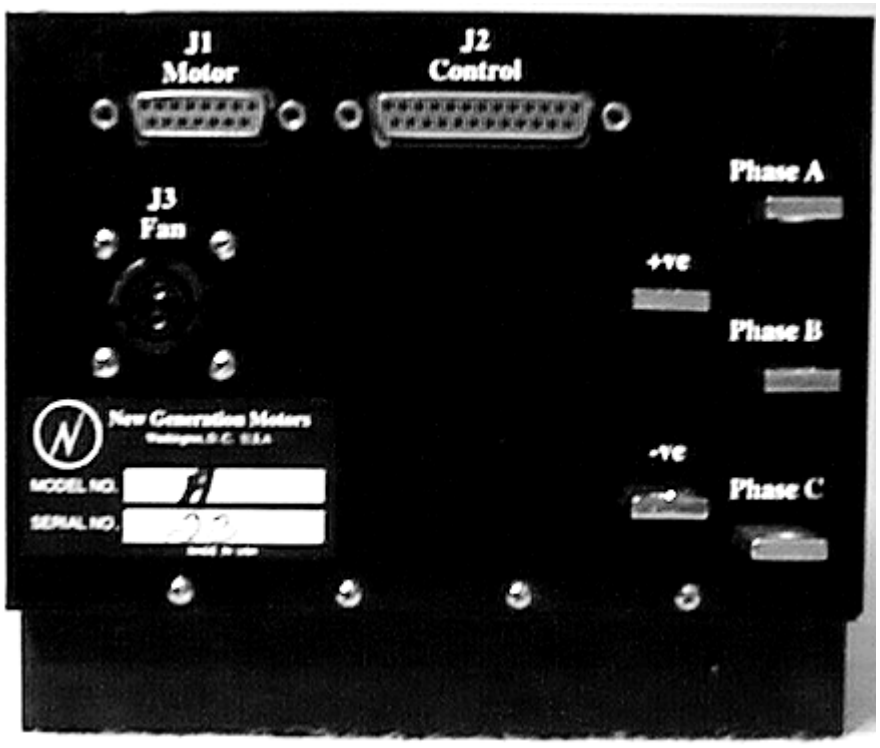


Figure 1-1

Controller connections:

J1 – Motor communication link,
15 pin female D-Sub. connector

J2 – Control signals (vehicle)
25 pin female D-Sub. connector

J3 – Fan power for cooling
AMP Series 1 CPC 11-4, reversed sex
(*mating connector provided*)

+ve & -ve – Positive & negative power
bus bar with ¼ in. diameter through hole

Phase A,B,C – Phase lead connections for the motor
bus bar with ¼ in. diameter through hole

2 Mechanical Installation

2.1 Physical Mounting

The Controller should be mounted by a method that minimizes the vibration and protects it from the elements during operation. High impact loads or excessive moisture and dirt could shorten the life span of the controller. There are several 4-40 UNC screw holes on the side of the controller that may be used for mounting. *Do not remove* any of the existing screws.

There are five types of connections that must be performed before operation of the controller:

- motor phase
- motor sense
- control
- fan power
- power

It is recommended that they be performed in the order as listed.

> ***Safety* Note**: The controller can retain a charge due to its high capacitance. Check the voltage before servicing the controller. **DO NOT** short the positive and negative buses together

2.2 Motor Phase Connection

This unit has three phase bus bars located on the right hand side; phase A, phase B and phase C. These phases must be properly connected to the corresponding phases of the motor. These connections must be made with *no less than* AWG 6 gage (4.1 mm) wire, although AWG 4 (5.18mm) is preferred. The connections can be made using properly sized ring terminals for the corresponding wire width and inner diameter of 0.25 in. Low head bolts, ¼ in. UNC no longer than 0.625in. should be used. They must be securely fastened with lock nuts and washers. Rubber boots should then be placed over each connection point to ensure no shorts between phases (a set of hardware is provided). *Visually check the spacing between connections and ensure the leads can not be rotated.* There should be a minimum of 3/16in. between connection points. Great care should be taken in applying proper strain relief for these cables. Additionally, ensure there exists enough slack in the cables for movement, especially for those connected to "in the wheel" motors.

In combination with NGM-SC-M100 & NGM-SC-M150 motors, RED corresponds to Phase A, GREEN to Phase B and BLACK to Phase C.

2.3 MOTOR SENSE CONNECTOR J1

The motor sense connection requires a 15 pin D-sub male to be inserted into *J1* on the front of the controller and secured tightly. Take care to strain-relieve this cable properly on both ends to prevent any damage. (See Appendix A for pin out information)

Most NGM motors have a pre-installed cable for connection to the controller. However the NGM-SC-M100 motor, requires the *rotor retrofit package* to have been installed. For further information, contact NGM. Once the retrofit package is installed, the connection is similar to the others.

2.4 CONTROLLER INPUT CONNECTOR J2

The control cable must be plugged into *J2,* a DB25F connector. See appendix A for pin information.

2.5 FAN CONNECTOR J3

Fan power should be connected to *J3*. A series 1 CPC Amp 11-4 plug and two pins are provided with the controller. Splice the ground of each fan wire (Black) into one single wire long enough to reach the front panel of the controller. Do the same with the positive (Red) wires of each fan. Crimp the pins (CPC, series 1) on to the end of the positive and negative leads of this cable. The positive must be placed into position 1 of the plug and the negative into position 4 (See Fig. 2-1). Then mate the plug to *J3* on the controller's front panel.

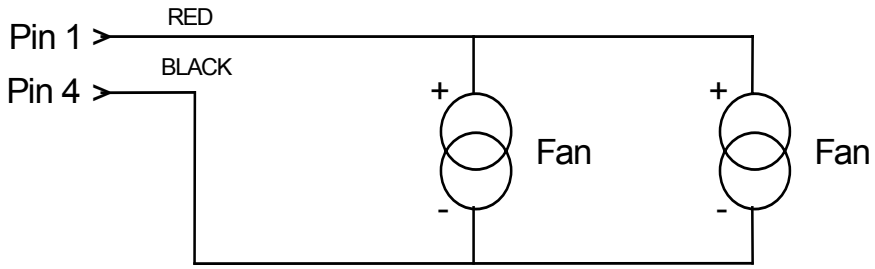


Figure 2-1, Fan power circuit

2.6 POWER CONNECTION

A pre-charge circuit *(see Fig. 2-2) must* be used to connect the motor controller to the power system. Resistor R1 and switch S3 form a "pre-charge" for the motor controller. The input capacitance of the controller is very high, large in-rush currents will eventually destroy the controller and switch S2. R1 should have a resistance such that the current through it at turn-on is at most 30A. Resistor R2 is an optional high current shunt for measuring the battery current. The DC ratings of all components must exceed the maximum bus voltage.

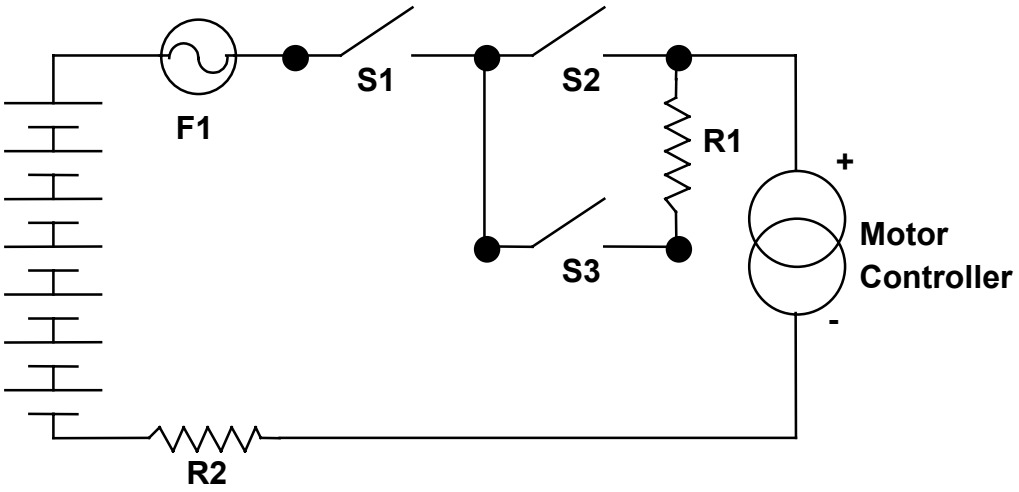


Figure 2-2, Pre-Charge Circuit Schematic

Low head bolts ¼ in. UNC with a lock nut and washer (provided) should be used to connect to the positive and negative posts of the controller. A *minimum* of AWG 6 gage (4.1 mm) or larger should be used (AWG 4 (5.2mm) preferred). Visually check the spacing between connections and ensure that the leads can not be rotated. After connection, each post should have a rubber boot covering it. Take care to strain-relieve each wire properly to ensure that no damage is done by the force on the connections.

3 Basic Operation

When shipped, the EVC402 controller is configured for "discrete torque" control using external switches and potentiometers. Connection of these signals is straightforward, as shown in the diagram below. In this mode of operation, the direction input sets the operating direction, and the ignition input enables motoring operation. The controller operates in torque control mode, whereby the motor phase current, which is proportional to output torque, is determined by the throttle and regen inputs and the motor speed.

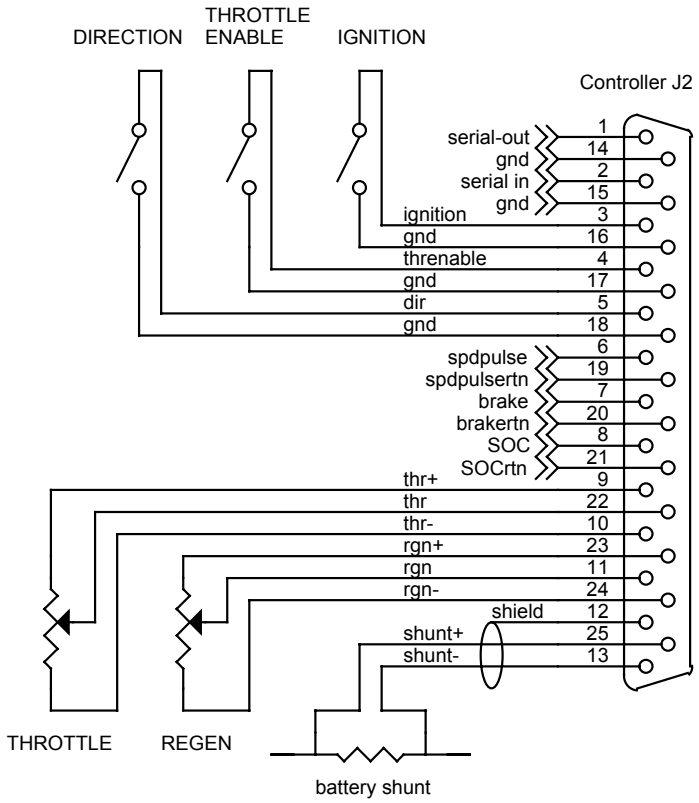


Figure 3-1, Input Signals

3.1 DIRECTION INPUT

The *for/rev* input and its corresponding *gnd,* use pins 5 and 18, respectively, on *J2*. Forward corresponds to open circuit and reverse to closed. It is recommended that the direction signal be wired directly to a switch for maximum safety and reliability.

3.2 IGNITION

The *ignition* input signal (pin 3 on *J2*) must be connected to *gnd* (pin 16, on *J2*) for the controller to enable. An open circuit immediately disables all torque production, and reduces the controller's quiescent power consumption.

3.3 THROTTLE ENABLE

The *threnable* signal (pin 4 on *J2*) must be connected to *gnd* (pin 17 on *J2*) for the controller to produce accelerating torque. When open-circuited, the maximum throttle current is set to zero, but the controller can still operate in regen. It is suggested that this input be wired to a switch on the brake pedal.

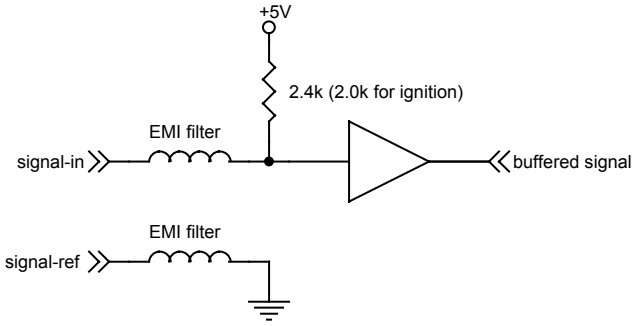


Figure 3-2, Electrical equivalent of *ignition*, *direction*, and *throttle enable* inputs

3.4 THROTTLE INPUT

The *thr* signal (pin 22 on *J2*) has an associated ground, *thr*- (pin 10 on *J2*), and excitation signal, *thr*+ (pin 9 on *J2*). These signals should be connected to a linear (i.e. non-audio) potentiometer having a minimum resistance of at least 4.0k Ohms, and a maximum resistance of at most 12.0k Ohms. The wiper should be connected to *thr*, with *thr*- connected to the end of the potentiometer nearest the rest position and *thr*+ connected to the opposite end. The excitation signal is a 5V reference with an internal 1.00kOhm series resistor. The ratio *thr* / *thr*+ determines the measured throttle position.

The controller measures the excitation voltage to verify proper connection of the potentiometer. If the excitation voltage *thr*+ falls below 3.9V or rises above 4.7V, or if the *thr* signal exceeds *thr*+, the throttle input is disabled and the FA2_threxcite bit is set in SV_fault2 (see section 5.1.3 for more details). Furthermore, if the throttle input is greater than zero when the ignition is closed, the controller will enter the interlock state to prevent the vehicle from accelerating unexpectedly. An electrical equivalent of the controller's throttle interface circuit is shown below.

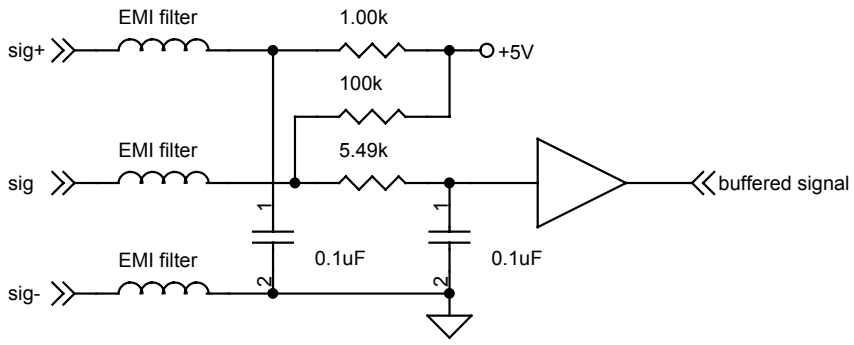


Figure 3-3, Throttle & regen internal circuit schematic

By default, *thr* = 0V is scaled to -5% pedal position, and *thr* = *thr*+ is scaled to 105% pedal position. This ensures that somewhat less than full travel of the throttle potentiometer still allows operation from zero to 100% and allows for voltage drops in the wiring.

3.4.1 Support for Reduced Potentiometer Input Range

It is common for the throttle or regen mechanism to produce less than full travel of the potentiometer. The controller has configurable gain and bias settings and 0.1% resolution of the *thr* and *rgn* signals, allowing the full control range from a reduced input range. Because of the high signal resolution, reducing the total pedal travel to as little as 1/10 of full-scale allows 1% resolution of the pedal position, and experience suggests that 3% resolution is sufficient for vehicle applications. Refer to the Configuration section for details on these configuration settings.

3.4.2 Support for Potentiometers with Higher Resistances

To utilize a potentiometer with a maximum resistance greater than 12k Ohms, a 10k Ohm resistor must be wired across the ends of the potentiometer. When this is done, the controller will not detect an open-circuit that is in series with the potentiometer but not the 10k Ohm resistor, so the resistor should be wired directly to the potentiometer, as shown below. This resistor has minimal effect on the resolution of the signal measurement, and there is no need to adjust the signal gain and bias if the full travel of the potentiometer is utilized.

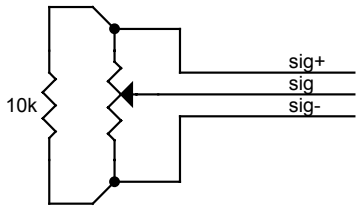


Figure 3-4, Utilizing Potentiometers With Resistances Greater Than 12kOhms

3.4.3 Support for Potentiometers with Lower Resistances

To utilize a potentiometer with a minimum resistance less than 4k Ohms, a resistor must be wired in series with the positive excitation signal. This resistor should be selected to bring the minimum total resistance between the excitation and reference signals to between 4.0k and 5.0k Ohms. For example, a 3.6k, 5% resistor could be used in series with a 1.0k, 20% potentiometer, since the minimum total resistance would be 3.6 * 0.95 + 1.0 * 0.8 = 4.2k Ohm. Detection of open-circuits is not affected by this configuration, but short-circuits between terminals of the potentiometer may not be detected. Should such a short-circuit occur, the effect will be either a throttle input that is stuck at zero, or a highly sensitive throttle that rapidly transitions from zero to a high value.

Full-travel of the potentiometer will not produce a full-scale signal voltage, so it is necessary to adjust the signal gain and bias as described in the Configuration section.

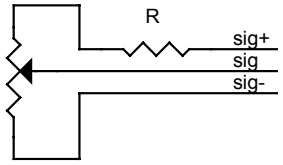


Figure 3-5, Utilizing Potentiometers With Resistances Less Than 4kOhms

3.5 REGEN INPUT

The *rgn* signal (pin 11 on *J2*) has an associated ground, *rgn-* (pin 24 on *J2*), and excitation signal, *rgn+* (pin 23 on *J2*). These signals should be connected to a linear potentiometer having a minimum resistance of at least 4.0k Ohms, and a maximum resistance of at most 12.0k Ohms. The wiper should be connected to *rgn*, with *rgn-* connected to the end of the potentiometer nearest the rest position and *rgn+* connected to the opposite end. The excitation signal is a 5V reference with an internal 1.00kOhm series resistor. The ratio *rgn* / *rgn+* determines the measured regen position.

The controller measures the excitation voltage to verify proper connection of the potentiometer. If the excitation voltage *rgn+* falls below 3.9V or rises above 4.7V, or if the *rgn* signal exceeds *rgn+*, the regen input is disabled and the FA2_rgnexcite bit is set in SV_fault2 (see section 5.1.3 for more details). The interface circuit is identical to the throttle interface circuit.

By default, *rgn* = 0V is scaled to -5% regen position, and *rgn* = *rgn+* is scaled to 205% regen position. This ensures that somewhat less than full travel of the regen potentiometer still allows operation from zero to 200% and allows for voltage drops in the wiring. Setting the full-scale range to 200% ensures that full regen in available when the throttle is also at its maximum value.

3.6 BATTERY CURRENT MEASUREMENT INPUT

The battery current measurement utilizes an external current shunt in series with the battery pack. This current shunt may be placed at the positive or negative end of the pack, or between any two batteries. The only requirements are that the entire battery current flow through the current shunt, and that current that charges the battery produce a positive voltage from *shunt+* to *shunt-*. Thus, if the current shunt is placed at the negative end of the battery pack, the *shunt+* signal should be wired to the battery side of the current shunt, and the *shunt-* signal should be wired to the load/controller side of the shunt.

Shielded twisted pair wire should be used for the current sense lines *shunt+* (pin 25 on *J2*) and *shunt-* (pin 13 on *J2*). The shield drain wire should be connected to *shield* (pin 12 on *J2*) for maximum noise immunity.

The recommended value for the current shunt is 100A, 50mV. This corresponds to 2000 A/V, the default gain setting for this measurement. The input range of the current measurement circuit is ±115mV, allowing the use of 50 or 100mV shunts. A voltage in excess of 120mV disables the current measurement. This will occur if there is an open circuit in either of the sense signals.

3.7 SPEED PULSE OUTPUT

Speed pulse (pins 6 and 19 on *J2*) is an isolated open-drain pulse stream output that is proportional to the commutation rate, and thus the rotational velocity. The output changes state every two consecutive commutations (i.e. never after forward and backward movement), producing a 50% duty cycle. Unlike the EV-C200 series controllers, this output has a very low output impedance (max. 0.25 Ohm). The electrical equivalent of the speed pulse output is shown below.

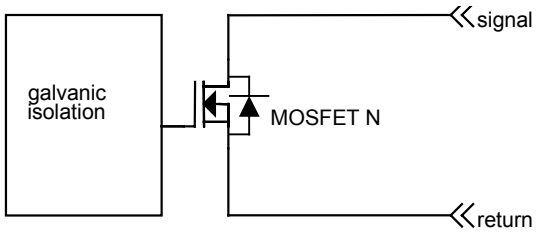


Figure 3-6, Speed Pulse and Brake Outputs

The output frequency f_{out} equals (3*P)/4 * f_{motor}, where P equals the motor pole count and f_{motor} equals the motor's revolutions per second.

3.8 STATE-OF-CHARGE (SOC) OUTPUT

SOC (pins 8 and 21 on *J2*) is a fixed 3,906Hz, pulse-width modulated 0-5V output with a duty cycle proportional to the calculated state-of-charge. This can be converted to an analog voltage using an RC low pass filter, or the duty cycle or pulse width can be measured using external circuitry.

3.9 REGENERATIVE BRAKING OUTPUT

Brake (pins 7 and 20 on *J2*) can be used as an activating switch that corresponds to the controller when in a "braking" mode. It is on (conducting) when the regen input is positive, even if the controller is not in a regenerative braking mode.

> *NOTE:* The *speed pulse* and *brake* pins can sustain a maximum of 40V and 100mA.

4 Introduction to the Serial Interface

Communication to the controller is based on the concept of the register, a single memory location identified by number. Some registers are used for instrumentation, and thus are read-only, while others are used for control or configuration and may be read or written. All registers are 16 bit integers.

The registers are organized by function into pages. Pages may be read/write, read-only, or read/write when selected. The "write when selected" feature prevents accidental changes to configuration values. All pages are initialized at power up by reading from the controller's nonvolatile memory. The pages are defined as follows:

Page	Description	Access
0_H	Control	read/write
1	Instrumentation	read-only
2	Development	read-only
3	Vehicle Configuration	read/write when selected
4	Battery Configuration	read/write when selected
5	reserved	read-only
6	Motor configuration	read/write when selected
7	Motor calibration	read/write when selected
8	Motor factory settings	read/write when selected
9	Controller Configuration	read/write when selected
A	reserved	read-only
B	Controller factory settings	read-only
C	Integrations	read-only

Figure 4-1, Register Pages

Pages 3 and 4 are the only pages needed to configure the drive system for a new vehicle platform. Page 1 and perhaps portions of page 2 are the only pages needed for instrumentation. Page 0 is the only page needed for control, except for feedback from page 1. The remaining pages are not described in detail in this document, but are listed in Appendix C.

Registers are identified by three digit hexadecimal numbers, and the first digit is the page number.

The communication format was designed to simplify external configuration, data acquisition, and control utilities while still allowing commands to be sent through a terminal emulation program. Communication over the serial interface is done using simple text strings terminated with carriage return [CR] and/or line feed [LF] characters. Each character is echoed as it is received, with two exceptions: the first ASCII [CR] or [LF] character received is echoed back as [CR][LF], and [CR] and [LF] characters are ignored when the previous character was a [CR] or [LF]. There are five types of serial input messages: commands, queries, assignments, bit queries, and bit assignments.

4.1 COMMANDS

Commands are used to instruct to the controller to perform a basic operation, such as storing configuration values to nonvolatile memory.

XXX![CR]

where XXX is a hexadecimal command number and [CR] is a carriage return character.

The controller replies with **#XX[CR][LF]** where XX is a two digit hexadecimal error number. The number for no error is 00. The leading # character identifies the number as an error code.

A list of commands is outlined in Section 7.2.

4.2 QUERIES

Queries are used for instrumentation or to read configuration values. There are two query commands, as follows:

Query with Decimal Reply:

XXX?[CR]

Query with Hexadecimal Reply:

XXX>[CR]

In both cases XXX is the register number to be queried. The controller replies with a text string of the decimal or hexadecimal value of the variable terminated by a [CR][LF] combination. Decimal replies are signed integers in the standard 16 bit range –32768 to 37267. Hexadecimal replies represent negative numbers in two's complement form. For example, –1 is sent as FFFF.

An entire page may be queried with a single command by replacing the register number with **. Specifically:

Page Query with Decimal Reply:

P?[CR]**

Page Query with Hexadecimal Reply:

P>[CR]**

The response to a page query is a tab-delimited string of register values terminated by a [CR][LF] combination. Using these commands, a data acquisition system could operate by simply saving the response string to the "1**?" query directly to disk.

4.3 ASSIGNMENTS

Assignments are used for control over the serial port and for configuration. There are two assignment commands, as follows:

Assignment of a Decimal Value:

XXX=#[CR]

Assignment of a Hexadecimal Value:

XXX<H[CR]

Here, # is a decimal text string and H is a hexadecimal text string of the value to be assigned. Hexadecimal numbers should be in two's complement form. The controller replies with **#XX[CR][LF]** where XX is a two digit hexadecimal error number. The number for no error is 00.

WARNING: Range checking is not performed on most registers. Out-of-range settings can cause erratic and unexpected operation.

4.4 BIT QUERIES

Bit queries are used to read individual bits in the instrumentation and configuration registers. The format of a bit query is:

XXX.Y?[CR]

where XXX is the hexadecimal register number and Y is the hexadecimal bit digit (0 is the least significant bit, F is the most significant). The controller replies with N[CR][LF] where N is either 0 or 1.

4.5 BIT ASSIGNMENTS

Bit assignments are a simple means to set and clear individual bits in the configuration registers. The format of a bit assignment is:

XXX.Y=N[CR]

where XXX is the hexadecimal register number, Y is the hexadecimal bit digit (0 is the least significant bit, F is the most significant), and N is 0 or 1. No other bits in the register are affected by a bit assignment.

4.6 SETTINGS

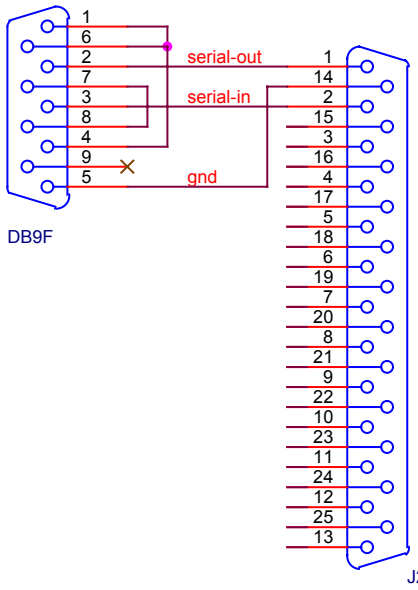
The serial interface operates at 19200 baud, 8 data bits, 1 start bit, 1 stop bit, no parity, no flow control.

4.7 Error Codes

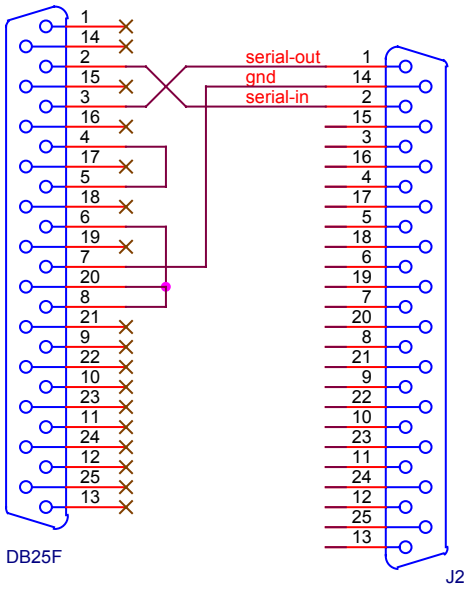
Code	Message	Description
00_H	Ok	Assignment made or command executed
01	reserved	
02	Invalid command	The action character is not one of !,?,=,<, or > or the command number in a command is not valid.
03	Serial overflow	24 consecutive characters received without a carriage return or line-feed. Additional characters are ignored.
04	Invalid input	The message was less than the minimum four characters or the three register characters are not a valid number.
05	Command failed	A coast command (0F0!) failed because the discrete throttle input is enabled.
06	Can't program	assignment: The specified page is not write-enabled. command: The controller must be disabled to allow a page operation command.
07-0B	reserved	
0C	Bad register number	The specified register number in an assignment or query is greater than the number of registers on the specified page.
0D-FF	reserved	

4.8 Cable Schematics

9-pin RS-232 Connector



25-pin RS-232 Connector



5 Instrumentation

The recommended method for reading instrumentation values from the controller is the use of the "1**?[CR]" serial command. The controller responds to this command with all 19 tab-delimited signed integers from the instrumentation page, page 1. This string is followed by a carriage-return and line-feed [CR][LF]. Note that future controller enhancements may increase the size of the instrumentation page. Alternatively, the registers may be queried one at a time as described in Section 4.2

5.1 Instrumentation Registers (Page 1)

5.1.1 Analog Measurements

All analog measurements reside in page one, and utilize a AM_ prefix.

Register AM_velocity Definition (100)

Bits 15-0
Motor speed in RPM. Negative values are used for reverse. This calculation uses the pole pair setting MF_polepairs. The definition of forward takes into account the reverse-direction bit VC_discrete.12.

Register AM_supplyV Definition (101)

Bits 15-0
Supply Voltage in deci-V. (10 deci-V = 1.0 V)

Register AM_supplyI Definition (102)

Bits 15-0
Supply or battery current, in deci-A (10 deci-A = 1.0 A). Specifically, the current through the external shunt. Positive current is defined to be charging current.

Register AM_baseplateT Definition (103)

Bits 15-0
Controller baseplate temperature in deci-°C (10 deci-°C = 1.0 °C).

Register AM_ambientT Definition (104)

Bits 15-0
Controller internal ambient temperature in deci-°C.

Register AM_motorT Definition (105)

Bits 15-0
Motor temperature in deci-°C.

Register AM_soc Definition (106)

Bits 15-0
Measured state-of-charge 0-1, with 1 corresponding to fully charged. This number is stored in Q8 format, whereby 1.00 = 256 and 0.50 = 128.

Register AM_thr Definition (107)

Bits 15-0
Measured throttle position 0-1, stored in Q8 format.

Register AM_rgn Definition (108)

Bits 15-0
Measured regen position 0-1, stored in Q8 format.

5.1.2 State Variables

State variables are input values, status bits, and fault codes. They are identified with an SV_ prefix.

Register SV_desiredphaseI Definition (109)

Bits 15-0
The input phase current regardless of the control or input modes, in deci-A. Negative values are used for negative torque. Positive torque is defined as accelerating torque in the positive direction, and decelerating torque in the reverse direction.

Register SV_desiredspd Definition (10A)

Bits 15-0
The input speed regardless of the input mode, in RPM. Negative values are used for reverse. This register is only set when the controller is in speed control.

Register SV_targetphaseI Definition (10B)

Bits 15-0
The target phase current, in deci-A rms. Negative values are used for negative torque. This is the input value to the space-vector PWM algorithm. Its magnitude is the lesser of SV_desiredphaseI and the maximum throttle (DV_maxthrI) or braking (DV_maxrgnI) phase current, as appropriate.

The motor controller top-level software structure is a state machine. The register SV_drivestate stores the current state and other important status bits. These bits are defined as follows.

Register SV_drivestate Definition (10C)

Bit 15	Bit 14	Bit 13	Bit 12
reserved	BIT_initialized	BIT_charging	BIT_motornotready

Bit 11	Bit 10	Bit 9	Bit 8
BIT_interlock	BIT_enabled	BIT_active	BIT_standby

Bit 7	Bit 6	Bit 5	Bit 4
BIT_transition	reserved	reserved	reserved

Bit 3	Bit 2	Bit 1	Bit 0
BIT_INdisable	BIT_limiting	BIT_spdctrl	BIT_reverse

Bit 15 **Reserved**. Always reads zero.

Bit 14 **BIT_initialized**. This bit is set once the controller has completed its power-up initialization.

0 Initialization in progress, reported analog values may be inaccurate.
1 Initialization complete.

Bit 13 **BIT_charging**. This bit is set when the charging input is asserted.

0 Not charging.
1 Charging.

Bit 12 **BIT_motornotready**.

0 A motor sense cable is detected and the motor settings have been read.
1 The motor settings have not been read.

Bit 11 **BIT_interlock**. The controller has entered the interlock state due to a fault. The controller's phase outputs are disabled in this state.

0 Normal operation.
1 Interlock state. All faults must be cleared and the controller must be disabled to leave this state.

Bit 10 **BIT_enabled**.

0 The phase current outputs are disabled.
1 The phase current outputs are enabled.

Bit 9 **BIT_active**.

0 The phase outputs are zero or disabled.
1 The phase outputs are nonzero.

Bit 8 **BIT_standby**.

0 The ignition input is asserted.
1 The ignition input is off. The controller is in a power saving mode with many internal circuits powered down.

Bit 7 **BIT_transition**. This bit is set briefly when BIT_active is set (the controller is operating), and a fault occurs, the target phase current is zero, or the target phase current changes sign.

0 Normal operation.
1 Transition in progress.

Bits 6-4 **Reserved**. Always read 0.

Bit 3 **BIT_INdisable**.

0 No disable inputs are asserted.
1 At least one disable input is asserted.

Bit 2 **BIT_limiting**.

0 Normal operation.
1 The output phase current is being limited by the phase-current limiting module.

Bit 1 **BIT_spdctrl**.

0 The controller is operating in torque control.
1 The controller is operating in speed control.

Bit 0 **BIT_reverse**.

0 The controller is operating in forward.
1 The controller is operating in reverse.

Not all combinations of the high-order bits are possible. In fact, ten drive states are defined based on the state of bits 14-7. These drive states are as follows:

Drive state	(bits 14-7)	Description
DS_startup	1000_H	The controller is performing its initialization
DS_standby	5100_H	The controller is in low-power standby mode
DS_nomotor	5000_H	Initialized, but no motor sense cable is connected
DS_charging	7100_H	Charger is plugged in and the ignition is off
DS_charging2	7000_H	Charger is plugged in and ignition is on
DS_shutdown	4000_H	Normal powered-down mode
DS_interlock	4800_H	A disable input must be asserted to leave this state
DS_enabled	4400_H	The controller is enabled, but the phase current input is zero
DS_active	4600_H	The drive system is producing accelerating torque
DS_transition	4680_H	The controller is leaving the DS_active state

5.1.3 Fault Indication

There are a total of four fault registers that organize fault conditions into logical groups. The most serious faults are stored in SV_fault1. These faults disable or prevent operation of the motor. When bits in this register are set, they also set in the SV_fault1latch register. Once the fault is cleared, the corresponding bit in SV_fault1 is also cleared, but SV_fault1latch remains set until the controller enters the DS_enabled drivestate (i.e. when the controller is enabled). This allows spurious faults to be read through the serial interface.

Register SV_fault1latch(10D) and SV_fault1 Definition (10E)

Bits 15-10	Bit 9	Bit 8
reserved	FA1_stuckthr	reserved

Bit 7	Bit 6	Bit 5	Bit 4
reserved	FA1_PDPINT	FA1_lostcomm	FA1_SCItimeoutzero

Bits 3-0
reserved

Bits 15-10 **Reserved**. Always read zero.

Bit 9 **FA1_stuckthr**.

0 No fault.
1 The throttle input was non-zero when the controller was first enabled.

Bits 8,7 **Reserved**. Always read zero.

Bit 6 **FA1_PDPINT**.

0 No fault.
1 An internal over-voltage or over-current fault has occurred.

Bit 5 **FA1_lostcomm**.

0 No fault.
1 Too much time has elapsed since the last message was received from the serial port, and the serial timeout function is enabled (See VC_SCI).

Bit 4 **FA1_SCItimeoutzero**.

0 No fault.
1 The discrete throttle input is disabled (VC_discrete.7 is zero) and the serial timeout duration is zero (bits 7-0 of VC_SCI are zero).

Bits 3-0 **Reserved**. Always read zero.

SV_fault2 consists of sensor and communication fault bits.

Register SV_fault2 Definition (10F)

Bit 15	Bit 14	Bit 13	Bit 12
reserved	reserved	FA2_rgnexcite	FA2_threxcite

Bits 11-8	Bit 5	Bit 4
reserved	FA2_SOClost	FA2_SCInoise

Bit 3	Bit 2	Bit 1	Bit 0
reserved	FA2_supplyI	reserved	reserved

Bits 15-14 Reserved. Always read zero.

Bit 13 **FA2_rgnexcite**

0 No fault.
1 The *rgn*+ signal is less than 3.9V, greater than 4.7V, or less than *rgn*.

Bit 12 **FA2_threxcite**

0 No fault.
1 The *thr*+ signal is less than 3.9V, greater than 4.7V, or less than *thr*.

Bits 11-8 **Reserved**. Always read zero.

Bit 5 **FA2_SOClost**

0 No fault.
1 The state-of-charge was lost due to corruption of the nonvolatile memory.

Bit 4 **FA2_SCInoise**.

0 No fault.
1 Parity or framing error in serial communication.

Bit 3 **Reserved**. Always reads zero.

Bit 2 **FA2_supplyI**.

0 No fault.
1 The voltage on current sense signal *shunt*+ is greater than 120mV. This is most likely due to an open-circuit on *shunt*+ or *shunt*-.

Bits 1,0 **Reserved**. Always read zero.

SV_fault3 consists of miscellaneous warning bits. These warnings can affect controller operation.

Register SV_fault3 Definition (110)

Bits 15-8
reserved

Bit 7	Bit 6	Bit 5	Bit 4
reserved	FA3_limphome	FA3_dirlatcherror	FA3_softstart

Bits 3-0
reserved

Bits 15-7 **Reserved**. Always read zero.

Bit 6 **FA3_limphome**.

0 Normal operation.
1 The controller is in limp-home mode, and the limp-home mode phase and battery discharge currents are being applied.

Bit 5 **FA3_dirlatcherror**.

0 Normal operation.
1 The input direction has been changed while the vehicle speed is greater than VC_spdthreshold. Accelerating torque is disabled.

Bit 4 **FA3_softstart**.

0 Normal operation.
1 The controller is soft-starting after being enabled with a non-zero input torque.

Bits 3-0 **Reserved**. Always read zero.

The final two status registers identify the dominant current limit for throttle and braking, respectively. The content of each register is a numeric code which corresponds to a current limit as follows:

Code	Name	Current limit:
0	FA4_motorT	motor temperature limit
1	FA4_baseplateT	controller baseplate temperature limit
2	FA4_undervolt	factory low voltage phase current limit
3	FA4_overvolt	factory high voltage phase current limit
4	FA4_abslim	factory motor or controller phase current limit
5	FA4_softlimit	serial phase current limit, SI_thrphaseIlimit, or SI_rgnphaseIlimit
6	FA4_thrdisabled	throttle disable input asserted
7	reserved	
8	FA4_spdgovernor	speed governor phase current limit
9	FA4_batIlimit	vehicle battery current limit
10	FA4_batIsoftlimit	serial battery current limit, SI_dischargeIlimit or SI_chargeIlimit
11	FA4_limphomebatI	limp-home mode battery current limit, VC_limphomesupplyI
12	FA4_limphomephaseI	limp-home mode phase current limit, VC_limphomephaseI
13	FA4_vehsoftlimit	vehicle regen current limit, VC_rgnphaseIlimit
14	reserved	
15	FA4_clutch	clutch input asserted
16	FA4_revgovernor	reverse-speed governor
17	FA4_dirlatcherror	input direction changed while vehicle speed is greater than VC_spdthreshold

Several codes are only applicable to one of the registers

Register SV_thrIlimit Definition (111)

Bits 15-0
The throttle current limit code.

Register SV_rgnIlimit Definition (112)

Bits 15-0
The braking current limit code.

5.2 DEVELOPMENT REGISTERS (PAGE 2)

The development page consist of registers which may simplify debugging a new system or understanding controller operation, but are not normally needed for instrumentation. These registers use a DV_ prefix.

The estimated temperature registers hold temperature calculations of the motor hot spot and controller power transistor junctions. In the EVC402 controller, these temperatures are equal to the measured temperatures.

Register DV_motorTest Definition (200)

Bits 15-0
Estimated motor temperature in deci-°C.

Register DV_baseplateTest Definition (201)

Bits 15-0
Estimated power transistor junction temperature in deci-°C.

Register IN_rgnphaseIlimit Definition (202)

Bits 15-0
When in discrete speed control, the regen phase current limit set by the regen input, in deci-A. Otherwise, set to maximum value.

Register IN_status consists of the digital control inputs to the controller, after arbitration between the discrete and serial inputs.

Register IN_status Definition (203)

Bit 15	Bit 14	Bit 13	Bit 12
reserved	IN_disable	reserved	reserved

Bit 11	Bit 10	Bit 9	Bit 8
IN_noignition	IN_nocbl	IN_pdfault	reserved

Bit 7	Bit 6	Bit 5	Bit 4
reserved	IN_spdctrl	IN_neutral	IN_thrdisable

Bit 3	Bit 2	Bit 1	Bit 0
IN_reverse	IN_forward	IN_charger	IN_clutch

Bit 15 **Reserved**. Always read zero.

Bit 14 **IN_disable.**

0 No disable inputs are asserted.
1 One or more disable inputs are asserted.

Bits 13-12 **Reserved**. Always read zero.

Bit 11 **IN_noignition.**

0 The ignition input is asserted.
1 The ignition input is not asserted.

Bit 10 **IN_nocbl.**

0 The motor cable detection input is asserted.
1 The motor cable detection input is not asserted, no motor is detected.

Bit 9 **IN_pdfault.**

0 Normal operation.
1 Internal power-drive fault asserted.

Bits 8,7 **Reserved**. Always read zero.

Bits 6-0 **IN_[INPUT].**

0 The corresponding input is not asserted.
1 The corresponding input is asserted.

Registers DV_DIstatus and DV_SIstatus hold the state of the discrete and serial digital inputs, respectively. These are used to calculate DV_status, along with VC_discrete. Note that the bits in DV_DIstatus and DV_SI_status are not affected by the enable bits in the VC_discrete register.

Register DV_DIstatus Definition (204)

Bits 15-12
reserved

Bit 11	Bit 10	Bit 9	Bit 8
DI_noignition	DI_nocbl	DI_pdfault	reserved

Bit 7	Bit 6	Bit 5	Bit 4
reserved	reserved	reserved	DI_thrdisable

Bit 3	Bit 2	Bit 1	Bit 0
DI_reverse	reserved	reserved	reserved

Bits 15-12 **Reserved**. Always read zero.

Bit 11 **DI_noignition.**

0 The ignition input is asserted.
1 The ignition input is not asserted.

Bit 10 **DI_nocbl.**

0 The motor cable detection input is asserted.
1 The motor cable detection input is not asserted, no motor is detected.

Bit 9 **DI_pdfault.**

0 Normal operation.
1 Internal power-drive fault asserted.

Bits 8-5 **Reserved**. Always read zero.

Bits 4,3 **DI_[INPUT].**

0 The corresponding discrete input is not asserted.
1 The corresponding discrete input is asserted.

Bits 2-0 **Reserved**. Always read zero.

Register DV_SIstatus Definition (205)

Bits 15-8
reserved

Bit 7	Bit 6	Bit 5	Bit 4
reserved	reserved	SI_disable (SI_neutral)	SI_thrdisable

Bit 3	Bit 2	Bit 1	Bit 0
SI_reverse	SI_forward	SI_charger	SI_clutch

Bits 15-6 **Reserved**. Always read zero.

Bits 5-0 **SI_[INPUT].** These bits are set and cleared using the 0XX! commands (see the section on serial control). It is possible to simulate the digital inputs through the serial port by setting these bits.

0 The corresponding serial input is not asserted.
1 The corresponding serial input is asserted.

The remaining development registers hold status values for the current-limiting logic.

Register DV_thermallimitmtr Definition (206)

Bits 15-0
The maximum motor phase current, in deci-A, based on the motor temperature.

Register DV_baseplateTderating Definition (207)

Bits 15-0
The derating coefficient (0-1 in Q8 format) of the phase current due to the controller temperature. This value is multiplied by the maximum phase current for the current supply voltage to calculate the maximum phase current of the controller due to temperature.

Register DV_maxphaseIthr Definition (208)

Bits 15-0
The maximum accelerating phase current, in deci-A, due to the most restrictive current-limiting constraint.

Register DV_maxphaseIrgn Definition (209)

Bits 15-0
The maximum decelerating phase current, in deci-A, due to the most restrictive current-limiting constraint.

Register DV_batmaxphIthr Definition (20A)

Bits 15-0
The maximum accelerating phase current, in deci-A, due to limits on the battery discharge current.

Register DV_batmaxphIrgn Definition (20B)

Bits 15-0
The maximum decelerating phase current, in deci-A, due to limits on the battery charge current.

6 Configuration

6.1 PROCESS

Configuration can be done via the serial interface at any time. However, configuration changes can only be stored to nonvolatile memory while the controller is disabled. Furthermore, in order to prevent unintentional changes to the configuration registers, the page to be written to must be write-enabled before new values are assigned. Configuration values are stored on pages 3 and 4.

A control register, SI_writeenable, (register 008) is used to set which pages are write-enabled, or to read the current write-enable status.

Register SI_writeenable Definition (008)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
reserved, always 0	reserved, always 0	reserved, always 0	reserved, always 0	Page B write enable, always 0	Page A write enable, always 0	Page 9 write enable	Page 8 write enable

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Page 7 write enable	Page 6 write enable	Page 5 write enable, always 0	Page 4 write enable	Page 3 write enable	Page 2 write enable, always 0	Page 1 write enable, always 0	Page 0 write enable, always 1

In addition, there are two serial commands to set or clear the write enable bits:

0F2! write disable (clears bits 1-15 in SI_writeenable)
0F3! write enable (sets all bits in SI_writeenable, except for read-only pages)

For example, the following serial commands all allow access to the battery configuration page (page 4):

008.4=1
008<10 ($2^4 = 10_H$)
008=16 ($2^4 = 16_D$)
008<FFFF
0F3!

Note that the last two commands enable all pages to be written to (except for read-only pages).

Once a page is enabled, any writes to registers in that page take effect immediately. This allows the effect of the change to be noticed immediately. For example, to set the threshold voltage for detecting full charge of the batteries to 55.0V, send the following command:

401=550[CR] (Register 401 is BC_fullchargeV, and the units are deci-V).

This value can be immediately changed to 53.5V by sending:

401=535[CR]

After all changes are complete, it is necessary to copy the page(s) to non-volatile memory. To discard all changes to a page, the power-up values can be restored. There are two commands for these functions:

- 0F4! Save all write-enabled pages except page 0 to non-volatile memory, the controller must be disabled.
- 0F5! Restore power-up values for all enabled pages.

The controller must be disabled for these commands to take effect, this is best done by turning off the ignition. Alternatively, the controller can be disabled through the serial port using the serial disable command (see the Serial Control section).

NOTE: If the configuration changes are not saved to non-volatile memory, the controller will revert to the old settings when it is power-cycled.

Summary of Configuration Commands:

- 0F2! write disable (clears bits 1-15 in SI_writeenable)
- 0F3! write enable (sets all bits in SI_writeenable)
- 0F4! Save all write-enabled pages except page 0 to non-volatile memory, the controller must be disabled.
- 0F5! Restore power-up values for all enabled pages, the controller must be disabled.
- 0FA! reset controller

6.2 VEHICLE CONFIGURATION (PAGE 3)

All vehicle configuration registers use a VC_ prefix.

6.2.1 Battery Current Shunt

The EVC402 controller supports a wide range of external current shunts. The controller uses the shunt conductance to calculate the battery current from the shunt voltage. A bias setting is provided for completeness, but it should be set to zero for most applications.

Register VC_SCsupplyI Definition (300)

Bits 15-0
The value of the external supply current shunt, in A/V.

Register VC_OFsupplyI Definition (301)

Bits 15-0
Supply current bias in deci-A, normally set to zero.

6.2.2 Switch Inputs

Each switch, or binary, input to the motor controller may be enabled or disabled, and the polarity (assert when open-circuited vs. assert when short-circuited) of several inputs may be inverted.

> *NOTE:* It is strongly recommended that the ignition input remain enabled at all times, and that it be within easy reach of the driver. This will allow the controller to be readily disabled. In addition, should the controller enter the interlock state, the ignition can be toggled to clear the interlock..

Register VC_discrete Definition (302)

Bit 15	Bit 14	Bit 13	Bit 12
reserved	reserved	BIT_defaultspdctrl	BIT_invertdir

Bit 11	Bit 10	Bit 9	Bit 8
EN_discreteignition	reserved, set to 1	reserved, set to 1	reserved

Bit 7	Bit 6	Bit 5	Bit 4
EN_discretethr	reserved	reserved	EN_discretethrdisable

Bit 3	Bit 2	Bit 1	Bit 0
EN_discretereverse	EN_discretereverse	reserved	reserved

Bits 15,14 Reserved. Always set these bits to zero.

Bit 13 BIT_defaultspdctrl. This bit determines the control mode at power up.

0 The controller powers up in torque control.
1 The controller powers up in speed control.

Bit 12 BIT_invertdir.

0 Forward is clockwise rotation of the phase currents.
1 Forward is counter-clockwise rotation of the phase currents.

Bit 11 EN_discreteignition.

0 The ignition input is disabled.
1 The ignition input is enabled.

Bits 10,9 Reserved. Always set these bits to one.

Bit 8 **Reserved**. Always set this bit to zero.

Bit 7 **EN_discretethr**.

0 The discrete throttle and regen inputs are disabled.
1 The discrete throttle and regen inputs are enabled

Bits 6,5 **Reserved**. Always set these bits to zero.

Bits 4-2 **EN_discrete[INPUT]**.

0 The corresponding discrete input is disabled.
1 The corresponding discrete input is enabled

NOTE: Bits 3 and 2 (both EN_discretereverse) must always be set to the same value.

Bits 1-0 **Reserved**. Always set these bits to zero.

Register VC_invert Definition (303)

Bits 15-12
reserved

Bit 11	Bit 10	Bit 9	Bit 8
reserved	BIT_strictwrongdir	BIT_softstuckthr	reserved

Bit 7	Bit 6	Bit 5	Bit 4
reserved	reserved	reserved	INV_discretethrdisable

Bit 3	Bit 2	Bit 1	Bit 0
INV_discretereverse	reserved	reserved	reserved

Bits 15-11 Reserved. Always set these bits to zero.

Bit 10 **BIT_strictwrongdir**. This bit sets the behavior of the FA3_dirlatcherror bit. Regenerative braking is not affected by this setting or the FA3_dirlatcherror bit.

0 The FA3_dirlatcherror bit is cleared when the input direction matches the motor direction. As a result, it is not necessary to slow or stop the motor to enable operation in the current direction.
1 The FA3_dirlatcherror bit is cleared when the motor speed is less than VC_spdthreshold. If the input direction is changed while the speed is above

VC_spdthreshold, it is necessary to slow the motor below VC_spdthreshold to enable driving torque.

Bit 9 **BIT_softstuckthr**. This bit sets the behavior of the controller when the throttle is nonzero when the controller is enabled.

0 The stuck throttle interlock is only cleared by disabling the controller, using either the ignition or neutral inputs.
1 The stuck throttle interlock is cleared when the controller is disabled or the throttle input is zero.

Bits 8-5 **Reserved**. Always set these bits to zero.

Bits 4,3 **INV_discrete[INPUT]**. These bits may be set to one in order to invert the corresponding discrete input. As a result, switch inputs that are normally asserted when open circuit are instead asserted when short-circuited.

0 The corresponding discrete input is not inverted.
1 The corresponding discrete input is inverted.

Bits 2-0 **Reserved**. Always set these bits to zero.

Register VC_spdthreshold Definition (315)

Bits 15-0
The maximum speed for direction reversal, in RPM.

6.2.3 Throttle and Regen Inputs

The analog throttle and regen inputs are conditioned to produce a per unit value from zero to one. First, a gain and bias is applied, with each input having its own coefficients. Next, the reading is filtered using an exponential filter with programmable cut-off frequency. The filtered value is the measured position, AM_thr and AM_rgn. These registers are in Q8 format, meaning that there is an implied decimal point to the right of the 8th least-significant binary digit. In this format, a value of 256 corresponds to 1.00. Ignoring the Q8 convention, the calculations of AM_thr and AM_rgn can be summarized as:

```
AM_thr = filter(position * VC_thringain + VC_thrdeadband);
AM_rgn = filter(position * VC_rgningain + VC_rgndeadband);
```

Register VC_thringain Definition (304)

Bits 15-0
Discrete throttle input gain, in Q8 format.

Register VC_rgningain Definition (305)

Bits 15-0
Discrete regen input gain, in Q8 format.

Register VC_thrdeadband Definition (306)

Bits 15-0
Discrete throttle input bias, in Q8 format

Register VC_rgndeadband Definition (307)

Bits 15-0
Discrete regen input bias, in Q8 format.

Register VC_thrfilter Definition (308)

Bits 15-0
Discrete throttle input filter coefficient, in Q8 format

Register VC_rgnfilter Definition (309)

Bits 15-0
Discrete regen input filter coefficient, in Q8 format.

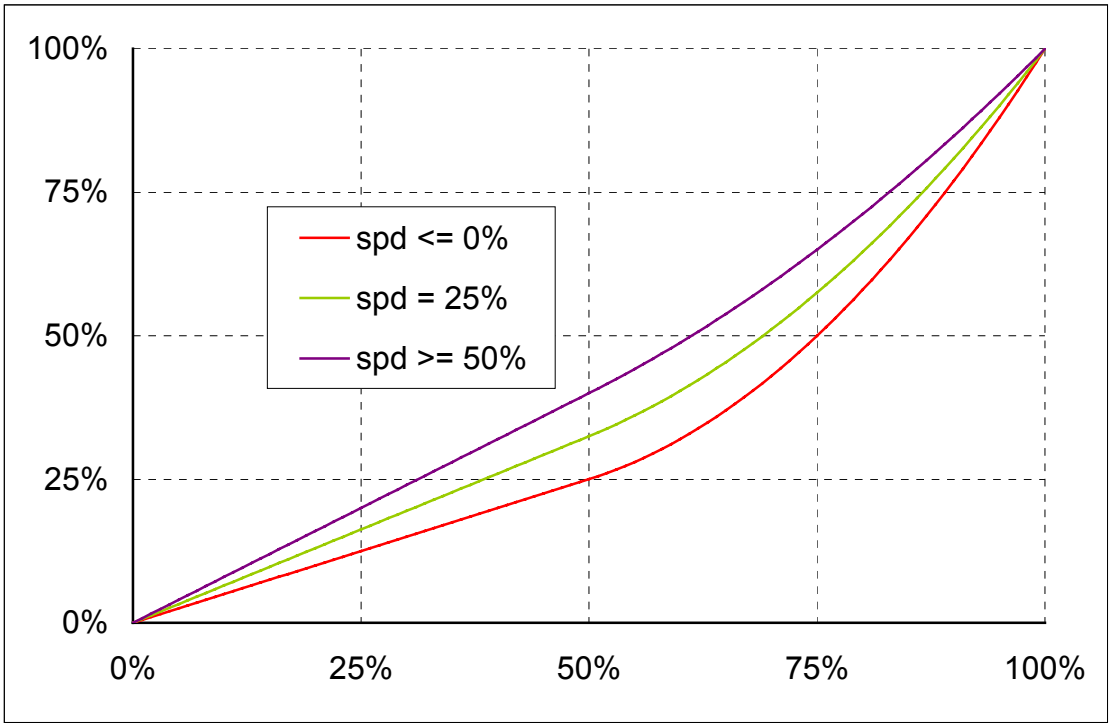
Given a desired cut-off frequency *f*, the filter coefficient can be computed as:

$$VC\_\_\_filter = 256e^{-\pi f/100}$$

The filter coefficients must be set between 0 and 252 to prevent nonsensical results and round-off errors.

The translation from the measured throttle and regen positions to the desired output torque is a three step process: shaping, arbitration, and scaling and differencing. The shaping step applies the throttle position to a torque map, shown below. The mapping has the following characteristics:

- The curve has a linear and quadratic section.
- The linear section is defined by a total width and the desired slope.
- The quadratic section is constrained to provide continuity and first derivative continuity with the linear section and to allow full torque at full input travel.



As a result of this mapping the following is achieved:

- Increased input sensitivity at low torque levels and low speeds
- Full throttle capability at any speed
- No discontinuities or corners (first derivative discontinuities)
- Configuration constants with physical meaning. Specifically, the values to be set are:
  - The linear to quadratic throttle position point
  - The low-speed output at the transition point.
  - The full-speed output at the transition point.
  - The low-speed and full-speed speeds (0 and 50% of top speed in the graph above)

Register VC_Xt Definition (30A)

Bits 15-0
The linear to quadratic throttle position point, in Q8 format.

Register VC_Yt0 Definition (30D)

Bits 15-0
Throttle shaping Y value at X=VC_Xt when the speed is <= VC_spd0, Q8 format

Register VC_Yt1 Definition (30E)

Bits 15-0
Throttle shaping Y value at X=VC_Xt when the speed is >= VC_spd1, Q8 format

Register VC_spd0 Definition (30F)

Bits 15-0
Throttle shaping and engine braking minimum speed, in RPM

Register VC_spd1 Definition (310)

Bits 15-0
Throttle shaping and engine braking maximum speed, in RPM

The arbitration step is responsible for determining the relative weight of the throttle and regen inputs when the regen input is non-zero. The goals of this step are: to allow full throttle when the vehicle is stopped and regen is applied, to allow zero throttle when the vehicle is moving quickly, and to transition smoothly between these two conditions. In addition, regenerative braking is disabled below a set speed to prevent torque oscillations at low speeds.

Lastly, the throttle is scaled to the nominal maximum throttle current, the regen is scaled to its maximum, and the difference between the two values is taken. In order to prevent acceleration jerk, the positive derivative is limited by a programmable amount.

Register VC_spddeadband Definition (33B)

Bits 15-0
Below this speed, the discrete regen input is disabled, in RPM..

Register VC_lowspdxfrslope Definition (311)

Bits 15-0
Throttle-vs.-regen arbitration coefficient, 1 / RPM in Q15 format.

Given that it is desired to weight the regen input at 100% for speeds of S RPM and above,
VC_lowspdxfrslope = 32768 / (S – VC_spddeadband).
The maximum value of VC_lowspdxfrslope (and all other registers) is 32767.

Register VC_phaseIposramp Definition (312)

Bits 15-0
The maximum positive derivative of the phase current when the phase current is positive and the discrete throttle input is enabled. The units are A/s.

6.2.4 Engine Damping

The drag of an idling internal combustion engine is simulated by adding regenerative braking in proportion to the motor speed between VC_spd0 and VC_spd1.

Register VC_enginedamping0 Definition (30B)

Bits 15-0
The amount of simulated engine braking to be applied when the speed is <= VC_spd0, in Q8 format. **This register should always be set to zero**.

Register VC_enginedamping1 Definition (30C)

Bits 15-0
The amount of simulated engine braking to be applied when the speed is >= VC_spd1, in Q8 format.

6.2.5 State-of-Charge Output

The state-of-charge output is calculated by scaling AM_soc by a programmable scaling coefficient, VC_K_soc. This register should normally be set to 4096_D, corresponding to 1.0 in Q12 format. If it is desired to reduce the maximum duty cycle of the state-of-charge output, this register may be set to a lower value.

Register VC_K_soc Definition (314)

Bits 15-0
The gain coefficient for the state-of-charge output in Q12 format.

6.2.6 Soft-start

When the controller is enabled in serial control and the input phase current is non-zero, the controller will ramp-up to the input level during a soft-start period. The length of this period is VC_softstart. During this time, the FA3_softstart bit will be set

Register VC_softstart Definition (316)

Bits 15-0
The soft-start duration in ms.

6.2.7 Limp-Home Mode

Limp-home mode is activated when the state of charge falls below a programmed threshold, and is only cleared by disabling the vehicle and recharging. Thus there is no possibility of regenerative braking taking the system out of limp-home mode. In this operating state, the maximum battery current draw is reduced to limit energy consumption and the maximum phase current (torque) is reduced to improve operating efficiency. These actions will reduce the acceleration, gradeability, and top-speed of the vehicle in exchange for increased range.

Register VC_limphomeSOC Definition (317)

Bits 15-0
The threshold state-of-charge in Q8 format.

Register VC_limphomesupplyI Definition (318)

Bits 15-0
The maximum battery discharge current when in limp-home mode, in deci-A.

Register VC_limphomephaseI Definition (319)

Bits 15-0
The maximum throttle phase current when in limp-home mode, in deci-A.

6.2.8 Regen Current Limit

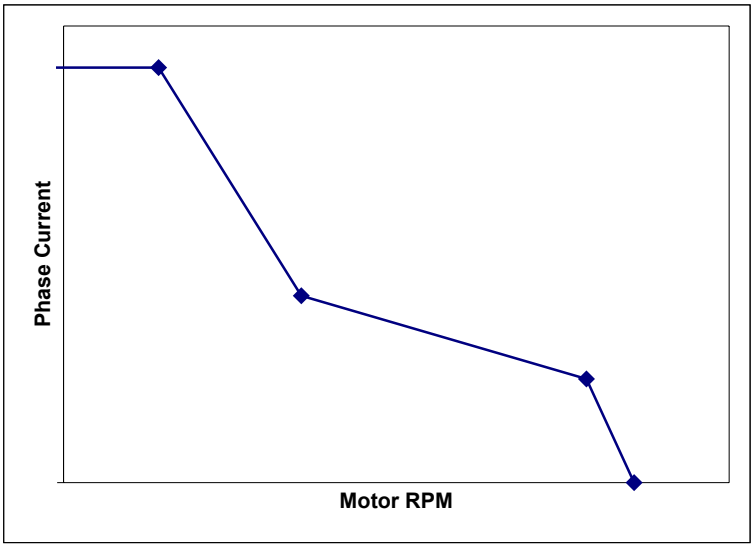
The maximum regent current limit may be reduced from its factory-set maximum by setting VC_rgnphaseIlimit.

Register VC_rgnphaseIlimit Definition (31A)

Bits 15-0
The vehicle maximum regen phase current, in deci-A. This register determines the vehicle's maximum regenerative deceleration.

6.2.9 Speed Governor

In certain applications it may be desirable to limit the maximum speed, or to limit the torque as the speed is increased. This can be for safety reasons and/or regulations and can be achieved by adjusting the Phase current vs. Speed envelope. It is also possible to improve range without sacrificing low speed gradeability. The envelope is altered by adjusting four points on a piecewise-linear function. The first is the maximum speed allowed to utilize 100% of the phase current and the last point is the speed at which the phase current drops to 0%. This limit is not applied to the braking torque.



The points are stored as an array of motor speeds and an array of phase currents in sequential registers.

Register Array VC_spdSpts[0-3] Definition (31C-31F)

31C-31F Bits 15-0
The speed (in RPM) points for the speed governor. These must be in ascending order, VC_spdSpts[0] < VC_spdSpts[1] < VC_spdSpts[2] < VC_spdSpts[3].

Register Array VC_spdIpts[0-3] Definition (320-323)

320-323 Bits 15-0
The phase current (in deci-A) points for the speed governor. All points must be greater than or equal to zero, but there are no restrictions on the relative magnitude of each point.

A simple reverse governor is implemented to limit the maximum speed in reverse. It has the same structure as the speed governor, but with only two points. By setting VC_revSpts[0] < VC_spdSpts[0] it is possible to reduce the maximum reverse torque as well.

Register Array VC_revSpts[0-1] Definition (33C-33D)

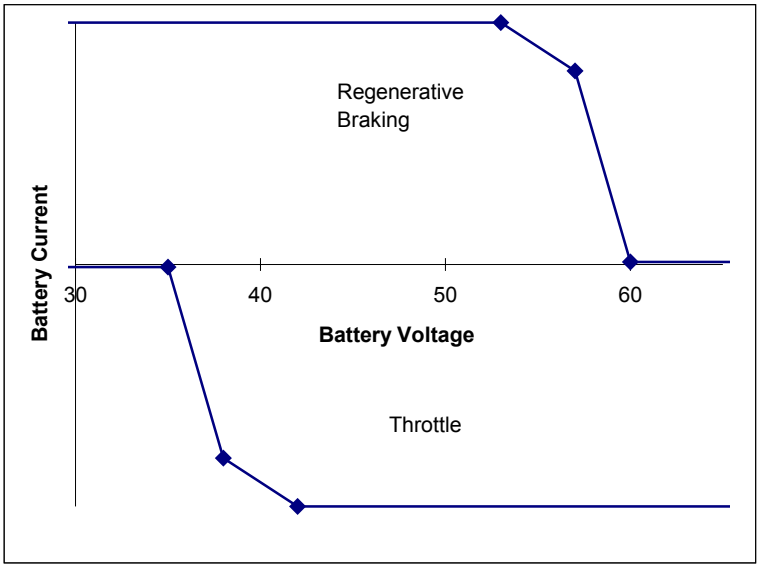
33C-33D Bits 15-0
The speed (in RPM) points for the reverse governor. These must be positive and in ascending order, VC_revSpts[0] < VC_revSpts[1]

Register Array VC_revIpts[0-1] Definition (33E-33F)

33E-33F Bits 15-0
The phase current (in deci-A) points for the reverse governor. Both points must be greater than or equal to zero, but there are no restrictions on their relative magnitude.

6.2.10 Battery Current Limits

In order to protect the batteries or extend range by limiting the maximum power draw, the battery current is constrained to be within an envelope of the form shown below. The six points allow configuration to the specific battery module and number of cells used. Note that positive battery current corresponds to energy entering the battery, i.e. under regenerative braking.



Register Array VC_dischargeVpts[0-2] Definition (324-326)

324-326 Bits 15-0
The supply voltage (in deci-V) points for the discharge current governor. These must be in ascending order, VC_dischargeVpts [0] < VC_dischargeVpts [1] < VC_dischargeVpts [2]

Register Array VC_dischargeIpts[0-2] Definition (327-329)

327-329 Bits 15-0
The battery current (in deci-A) points for the discharge current governor. All points must be greater than or equal to zero, but there are no restrictions on the relative magnitude of each point.

Register Array VC_chargeVpts[0-2] Definition (32A-32C)

32A-32C Bits 15-0
The supply voltage (in deci-V) points for the charge current governor. These must be in ascending order, VC_chargeVpts [0] < VC_chargeVpts [1] < VC_chargeVpts [2]

Register Array VC_chargeIpts[0-2] Definition (32D-32F)

32D-32F Bits 15-0
The battery current (in deci-A) points for the charge current governor. All points must be greater than or equal to zero, but there are no restrictions on the relative magnitude of each point.

Register VC_FIbatIlim Definition (330)

Bits 15-0
The filter setting for the supply current regulators, should be set to 0. Higher settings will decrease the response rate of the supply current regulators. Never set above 252.

6.2.11 Speed Control Coefficients

The EVC402 controller can be operated in speed control from either the discrete or serial inputs. The speed control algorithm is a PI controller with programmable coefficients and automatic anti-windup. To promote smooth operation of the vehicle, a programmable speed error clamp is provided.

Register VC_maxspderror Definition (331)

Bits 15-0
The maximum speed error (RPM) for the speed control PI regulator.

Register VC_Kp Definition (332)

Bits 15-0
The proportional coefficient for the speed control PI regulator, in deci-A / RPM in Q8 format.

Register VC_Ki Definition (333)

Bits 15-0
The integral coefficient for the speed control PI regulator, in deci-A / (RPM-s) in Q8 format.

6.2.12 Fan Thermostat

The EVC402 controller has a fan power output. This is thermostatically controlled based on the measured controller baseplate temperature. The turn-on threshold is programmable. Once on, the fan power outputs remain on until the measured temperature has dropped two degrees Celsius below this setting.

Register VC_hsfantemp Definition (336)

Bits 15-0
The baseplate temperature at which the controller fan is turned on, in deci-°C.

6.2.13 Serial Communication Watchdog

In order to ensure that the motor is disabled in the event of a loss of communication, the EVC402 controller implements a programmable watchdog function. See section 7.3.

Register VC_SCI Definition (339)

Bits 15-8
reserved

Bits 7-0
VC_maxSCIidle

Bits 15-8 Reserved. Always set these bits to zero.

Bits7-0 VC_maxSCIidle The maximum time (centi-s) between received characters to prevent a SCI timeout fault, 0 disables. Must be non-zero to operate in serial control.

6.3 BATTERY CONFIGURATION (PAGE 4)

All battery configuration registers use a BC_ prefix.

6.3.1 State-of-Charge Calculation

The State-of-Charge (SOC) is calculated using a weighted amp-hour calculation. To conserve memory, the weighing coefficients are defined by a piecewise linear equation. The nominal battery capacity is programmable in order to scale the measured amp-hours. A reset to 100% SOC will be initiated when, for a few programmable duration, both the battery voltage remains above a voltage threshold and the charging current remains below a current threshold. In addition, the state-of-charge can be set to an arbitrary value, as described in section 8.1.

Register BC_initbatcapacity Definition (400)

Bits 15-0
The nominal battery capacity in deci-Ahrs. This value corresponds to 100% state-of-charge.

Register BC_fullchargeV Definition (401)

Bits 15-0
The minimum voltage (in deci-V) for detecting when the batteries have been fully charged.

Register BC_fullchargeI Definition (402)

Bits 15-0
The maximum charge current (in deci-A) for detecting when the batteries have been fully charged.

Register BC_fullchargeT Definition (403)

Bits 15-0
The time (in deci-seconds) that the supply voltage must remain above VC_fullchargeV and the charging current must remain below BC_fullchargeI in order to set the state-of-charge at 100%.

The points for the weighted amp-hour integration are stored in an array of battery currents and an array of scaling coefficients. The points should be selected so that the piecewise linear function has a value of 1.0 (256 in Q8) when the battery current corresponds to the discharge rate for the specified nominal capacity. I.e., if the battery has a rating of 200A-hrs at a 50A discharge rate, BC_initbatterycapacity should be set to 2000 deci-A-hrs, and one of the scaling points should be set to 500 deci-A and K = Q8(1.0) = 256. If the same battery has a capacity of 100A-hrs at a 200A discharge rate, an addition point can be placed at 2000 deci-A and K = Q8(2.0) = 512.

Register Array BC_ahrIpts[0-7] Definition (404-40B)

404-40B Bits 15-0
The battery current (in deci-A) points for the weighted amp-hour integration. Negative values are used for discharge current. These must be in ascending order, BC_ahrIpts[0] < BC_ahrIpts [1] < BC_ahrIpts [2] < …

Register Array BC_ahrKpts[0-7] Definition (40C-413)

40C-413 Bits 15-0
The weighting coefficients (in Q8 format) for the weighted amp-hour integration. All points must be greater than or equal to zero, but there are no restrictions on the relative magnitude of each point.

WARNING:
The accuracy of the state-of-charge calculation is dependent on the accuracy of these weighting coefficients, the battery capacity register, and correct initialization of the state-of-charge. Errors in these settings will lead to erroneous and misleading state-of-charge calculations.

7 Serial Control

Serial control is achieved using register set commands to set registers in page 0. In addition, several commands exist to set and clear bits in the DV_SIstatus register. Control through the serial port must first be enabled by proper setting of the configuration registers in order to prevent contention between the serial and discrete interfaces. The discrete throttle input must be disabled. It may also be desirable to disable the discrete direction and throttle enable inputs. This is done by setting and clearing bits in the VC_discrete register. Refer to the configuration section for more details.

It is also possible to use the serial port to limit the maximum phase or battery current while in discrete control.

7.1 Serial Control Registers (Page 0)

Serial control can utilize either torque or speed control. Bit set and clear commands are used to set the control mode, see the following section. For each control mode, there is a ramp-rate register that limits the input rate of change. Thus, when in speed control, the controller can be commanded to accelerate at a constant rate with only two commands: an assignment to the SI_spdramp register and an assignment to the SI_desiredspd register. Likewise, an assignment to the SI_phIramp can prevent jerk when assigning new values to the SI_desiredphaseI register.

When in serial control, a coast command is available to quickly set the desired phase current (SI_desiredphaseI) to zero, independent of the SI_phIramp input. In speed control this command zeroes the speed control loop's integral component but does not change the target speed.

0F0! Coast

Register SI_desiredphaseI Definition (000)

Bits 15-0
The serial phase-current control register. Units are deci-A. Negative values are used for negative torque (regen when turning forward, accelerating torque when in reverse). This register is ignored when the EN_discretethr bit, VC_discrete.7, is 1, or when the controller is in speed control. Set to zero at power-up.

Register SI_desiredspd Definition (001)

Bits 15-0
The serial speed control register. Units are RPM. Negative values are used for reverse. This register is ignored unless the controller is in speed control and the EN_discretethr bit, VC_discrete.7, is zero. Set to zero at power-up. The definition of forward takes into account the reverse-direction bit VC_discrete.12. The reverse and forward bits in DV_SIstatus are ignored when in serial speed control.

Register SI_phIramp Definition (002)

Bits 15-0
The serial phase-current ramp-rate input. Units are A/s. This input does not affect the discrete throttle and regen inputs. This register is ignored when the EN_discretethr bit, VC_discrete.7, is 1, or when the controller is in speed control. Set to maximum value at power-up.

Register SI_spdramp Definition (003)

Bits 15-0
The serial speed ramp-rate input. Units are RPM/s. This input does not affect the discrete throttle and regen inputs. This register is ignored unless the controller is in speed control and the EN_discretethr bit, VC_discrete.7, is zero. Set to maximum value at power-up.

The soft-limit feature is implemented using four registers. These registers correspond to throttle and regen current limits, as well as battery charge and discharge limits.

Register SI_thrphaseIlimit Definition (004)

Bits 15-0
The serial throttle current limit register. Units are deci-A rms. Set to maximum value at power-up.

Register SI_rgnphaseIlimit Definition (005)

Bits 15-0
The serial regen current limit register. Units are deci-A rms. This is the magnitude of the limit, so it is a positive number. Set to maximum value at power-up.

Register SI_dischargeIlimit Definition (006)

Bits 15-0
The serial battery discharge current limit register. Units are deci-A. This is the magnitude of the limit, so it is a positive number. Set to maximum value at power-up.

Register SI_chargeIlimit Definition (007)

Bits 15-0
The serial battery charge current limit register. Units are deci-A. Set to maximum value at power-up.

7.2 SERIAL CONTROL COMMANDS

In addition to the coast command mentioned above (0F0!), several commands exist to set the operating direction, enable or disable the controller, change operating modes, or similar tasks:

Bit Set and Clear Commands:

000! clear SI_clutch
001! set SI_clutch, disable regenerative braking
002! clear SI_charger
003! set SI_charger, enter charging mode
005! set SI_forward and clear SI_reverse and SI_disable
007! set SI_reverse and clear SI_forward and SI_disable
008! clear SI_thrdisable
009! set SI_thrdisable, disable accelerating torque
00A! clear SI_disable
00B! set SI_disable and clear SI_forward and SI_reverse
00C! clear SI_spdcontrol, enter torque control
00D! set SI_spdcontrol, enter speed control
080! clear EN_discretethr and SI_spdcontrol, enter serial torque control
082! clear EN_discretethr and set SI_spdcontrol, enter serial speed control
084! set EN_discretethr and clear SI_spdcontrol, enter discrete torque control
086! set EN_discretethr and SI_spdcontrol, enter discrete speed control

Note that the SI_disable bit is always in effect, independent of the VC_discrete register. Therefore, if a 00B! command is sent (which sets SI_disable), the controller will remain disabled until a 00A!, 005!, or 007! command is sent. If one of these commands is not sent, then the vehicle can not be driven. The same hazard exists with the SI_clutch , SI_charger, and SI_thrdisable bits. The SI_forward, SI_reverse, and SI_spdcontrol bits, however, are only enabled when the corresponding discrete input is disabled in the VC_discrete register.

The 08x! commands will change the value of the EN_discretethr bit (VC_discrete.7) independent of the value of the page 3 write enable bit (SI_writeenable.3). This change will be to the current value only. The non-volatile memory is unaffected and the bit will revert to the saved value after a reset or power cycle.

7.3 THE SERIAL WATCHDOG

In order to prevent the vehicle from accelerating out of control in the event of a loss of serial communication, the controller firmware incorporates a watchdog function on the serial port. If, while active, the controller fails to receive a character in an allotted time, the controller will interlock. If desired, this functionality can be enabled even when the controller is in discrete control.

The duration of the timeout period is stored in the lower eight bits of VC_SCI, in the units of centi-seconds. For example, setting VC_SCI to 25 will set the timeout period to 0.25s. The maximum timeout period is 2.55s. If the lower eight bits of VC_SCI are zero, this function is disabled. Setting the timeout period to zero while EN_discretethr(VC_discrete.9) is zero will create a type 1 fault, FA1_SCItimeoutzero.

8 Application Tips

8.1 Adjusting the State-of-Charge

The state-of-charge may be set to an arbitrary value by first enabling writes to the battery configuration page (page 4), and then writing the new state-of-charge to AM_SOC. Note that this is a special case, since the instrumentation page is normally read-only. As an example, to reset the SOC to 100%, send the following two commands:

008.4=1
106=256

The first command enables writes to the battery configuration page, and the second sets the SOC to 100%. Recall that the AM_SOC is in Q8 format, so 100% corresponds to $1.00 * 2^8 = 256$.

8.2 Configuring the EVC402 Controller for Discrete Speed Control

If desired, the EVC402 controller can be configured to control the output speed in proportion to the magnitude of the *thr* input. In this configuration, an internal P^2I control loop is used to adjust the motor torque to match the input speed from the *thr* input. When the vehicle speed is greater than the set point, the controller will use regenerative braking to decelerate the vehicle. The *rgn* input is used to set the maximum amount of regenerative braking to use to decelerate the vehicle. If *rgn* is equal to *rgn-*, no regenerative braking will be applied, and the motor will coast until the speed is below the target speed.

The serial command 00D! is used to enter speed control. Sending this command while the *thr* input is enabled (VC_discrete.7 set) will cause the controller to immediately interpret the *thr* input as the desired speed. For this reason, it is recommended that the enter speed control command only be sent when the throttle is released and either the vehicle is stationary or the *rgn* input is zero, disabling regenerative braking.

To configure the controller to always operate in speed control, send the following commands through the serial interface:

disable the controller	00B!
enable writes to the configuration page (page 3)	008.3=1
set BIT_defaultspdctrl (VC_discrete.13)	302.D=1
save the configuration page	0F4!
disable writes to all pages	008=0
immediately switch to speed control	00D!
enable the controller	00A!

Once this procedure is complete, the controller will operate in speed control without further need of the serial interface.

The controller can be reset to operate in torque control by default by using the above procedure to set BIT_defaultspdctrl to zero, and sending the torque control command 00C! in place of the speed control command.

When in discrete speed control, full pedal travel (AM_thr ≥ 256 or 1.0 in Q8 format) sets the desired speed to the value stored in VC_spdSpts[3] (register 31F). This value can be set to the desired top speed of the motor. The throttle shaping function is used to scale the throttle input between 0 and 100%, so it is possible to provide increased throttle sensitivity at low speeds by appropriate configuration of the throttle shaping registers.

8.3 Switching Between Discrete Torque Control and Serial Speed Control

It is often desired to implement some form of cruise control similar to passenger vehicles whereby the controller switches between operating in discrete torque control and fixed speed operation. This can be readily accomplished with the EVC402 controller and an external microcontroller or embedded computer wired to the EVC402 controller's serial port.

To operate in this fashion, the controller is configured in discrete torque control (VC_discrete.7 set, VC_discrete.13 clear). The controller can be switched to serial speed control at any time, independent of the motor speed. To disable the throttle input and switch to speed control, send the following command to the controller:

switch to serial speed control	082!

Note that this command will clear the EN_discretethr bit, independent of the page 3 write enable bit. This change will be to the current value only. The non-volatile memory is unaffected so the bit will revert to the saved value after a reset or power cycle.. The speed control command will set SI_desiredspd to the current motor speed, AM_velocity. The target speed can then be adjusted in response to driver inputs to the external computer by adjusting SI_desiredspd.

A similar procedure is used to resume discrete torque control:

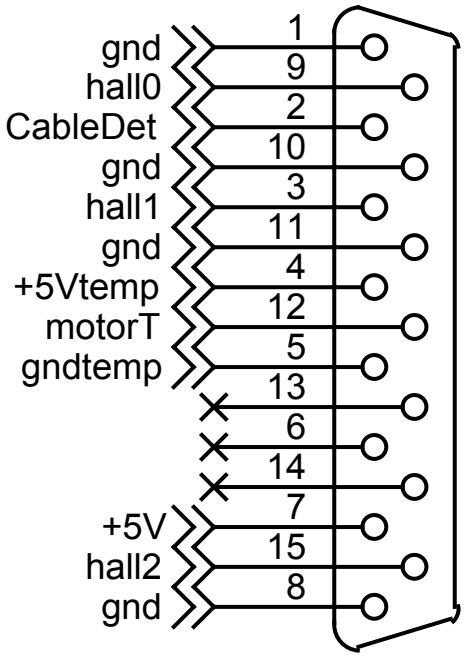
switch to discrete torque control	084!

This command will set the EN_discretethr bit, independent of the page 3 write enable bit. The nonvolatile memory is unaffected.

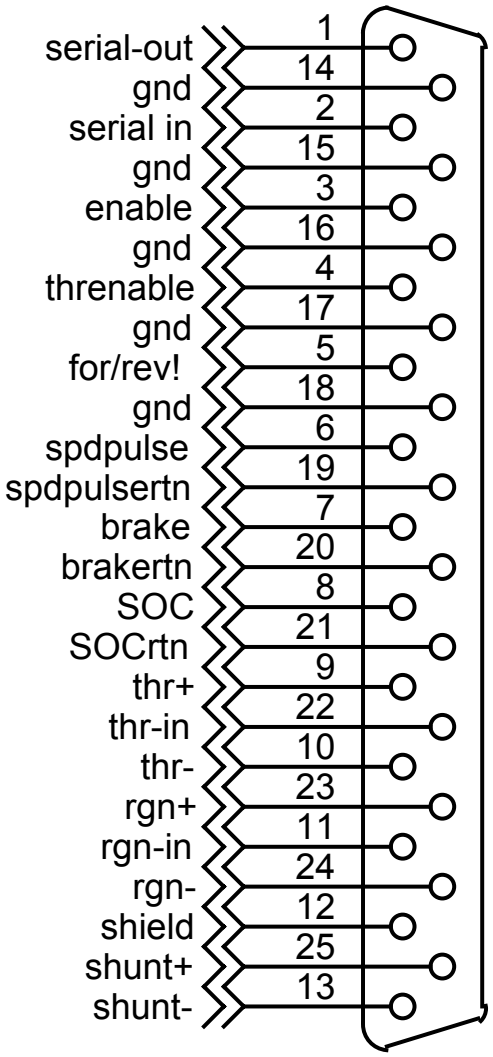
If it is desired to return to discrete torque control when the brake is pressed, connect the *threnable* signal to a switch on the brake pedal so that it opens when the brake is pressed. Then, by regularly querying the DI_thrdisable bit (using, for example, the bit query 204.4?), the external computer can determine that the brake has been pressed, and switch back to discrete control. Furthermore, by enabling the throttle enable input (EN_discretethrdisable set to 1, VC_discrete.4), accelerating torque will immediately be disabled by pressing the brake.

9 Appendix A: Connector Pinouts

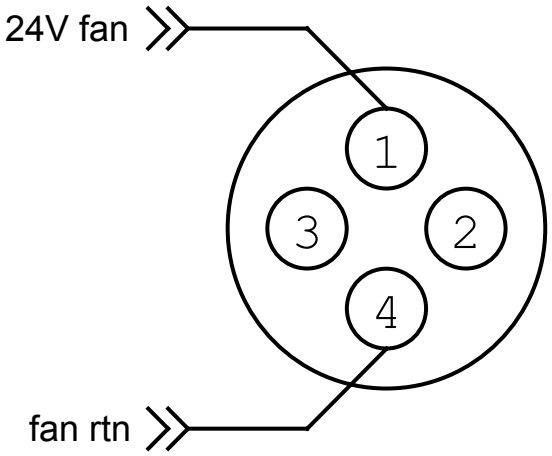
Motor Interface J1



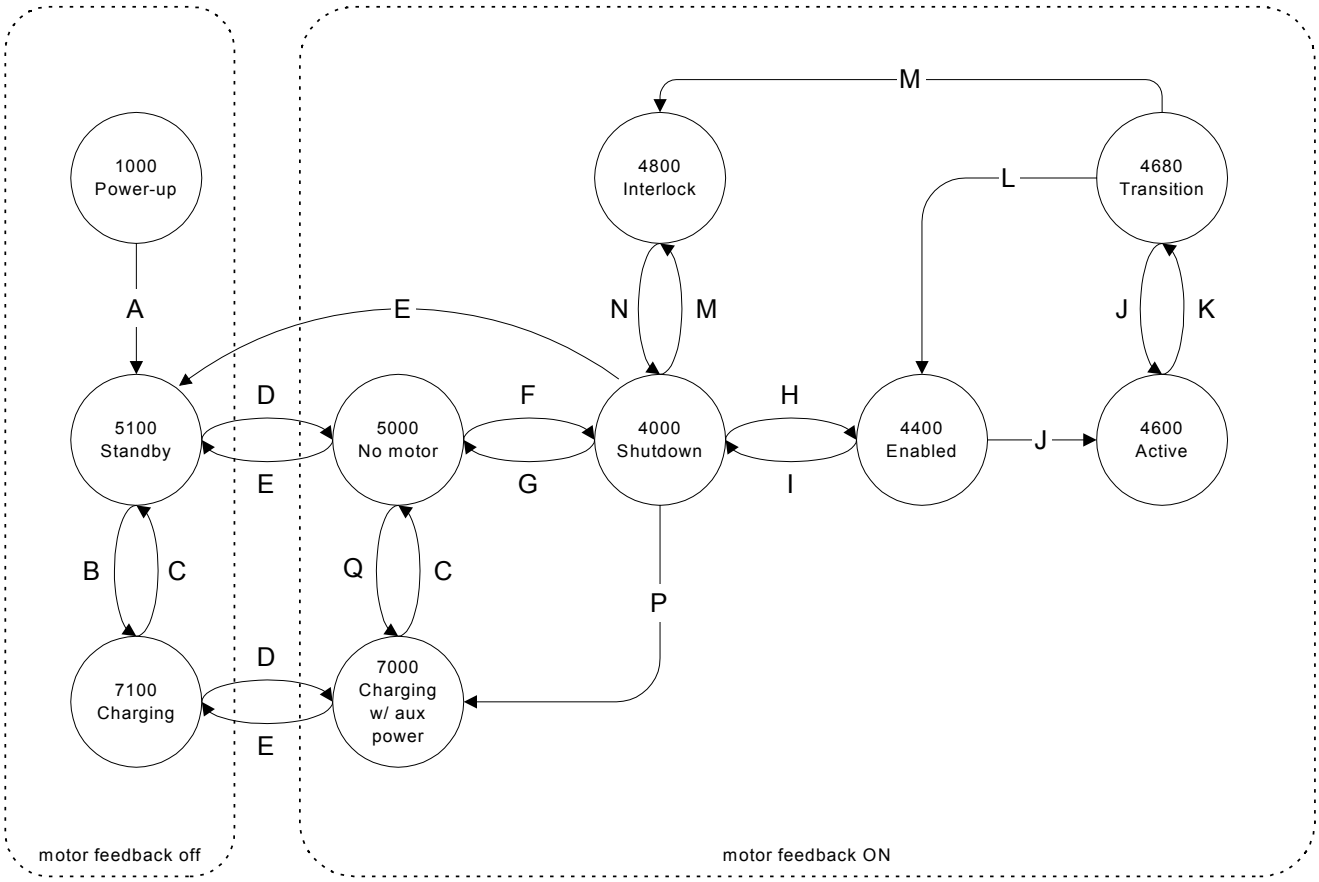
Vehicle Interface J2



Fan Power J3



10 Appendix B: Controller State Diagram



Transitions:

A	Power-up initialization is complete
B	Supply current is greater than 1/128th of VC_SCsupplyI or charger input is asserted
C	Supply current is less than 1/128th of VC_SC_supplyI and charger input is not asserted
D	Ignition input is asserted
E	Ignition input is not asserted
F	A motor has been detected and 100ms have passed since entering the no motor state
G	No motor is detected
H	No disable inputs are asserted and no SV_fault1 bits are set
I	At least one disable input is asserted
J	The target phase current SV_targetphaseI is nonzero, and no disable or SV_fault1 bits are set
K	The target phase current is zero, or a SV_fault1 or disable bit is set, or the target phase current has changed sign.
L	No SV_fault1 bits are set and either the target phase current is zero or a disable bit is set
M	An SV_fault1 bit is set
N	A disable bit is set and no SV_fault1 bits set
P	Charger input is asserted

11 Appendix C: Software Register Compilation

Page 0: Control

Register	Description
SI_desiredphaseI 000	The serial phase-current control register. Units are deci-A. Negative values are used for negative torque (regen when turning forward, accelerating torque when in reverse). This register is ignored when the EN_discretethr bit, VC_discrete.7, is 1, or when the controller is in speed control. Set to zero at power-up.
SI_desiredspd 001	The serial speed control register. Units are RPM. Negative values are used for reverse. This register is ignored unless the controller is in speed control. Set to zero at power-up. The definition of forward takes into account the reverse-direction bit VC_discrete.12.
SI_phIramp 002	The serial phase-current ramp-rate input. Units are A/s. This input does not affect the discrete throttle and regen inputs. Set to maximum value at power-up.
SI_spdramp 003	The serial speed ramp-rate input. Units are RPM/s. This input does not affect the discrete throttle and regen inputs. Set to maximum value at power-up.
SI_thrphaseIlimit 004	The serial throttle current limit register. Units are deci-A rms. Set to maximum value at power-up.
SI_rgnphaseIlimit 005	The serial regen current limit register. Units are deci-A rms. This is the magnitude of the limit, so it is a positive number. Set to maximum value at power-up.
SI_dischargeIlimit 006	The serial battery discharge current limit register. Units are deci-A. This is the magnitude of the limit, so it is a positive number. Set to maximum value at power-up.
SI_chargeIlimit 007	The serial battery charge current limit register. Units are deci-A. Set to maximum value at power-up.
SI_writeenable 008	The bits in this register correspond to the controller pages. In order to write to a given page, its corresponding bit must be set.

Page 1: Instrumentation

Register	Description
AM_velocity 100	Measured speed in RPM. Negative values are used for reverse. This calculation uses the pole pair setting MF_polepairs, and the line count MF_linecount. The definition of forward takes into account the reverse-direction bit VC_discrete.12.
AM_supplyV 101	Supply Voltage in deci-V.

AM_supplyI 102	Supply or battery current, in deci-A. Specifically, the current through the external shunt. Positive current is defined to be charging current.
AM_baseplateT 103	Controller baseplate temperature in deci-°C.
AM_ambientT 104	Controller internal temperature in deci-°C.
AM_motorT 105	Motor temperature in deci-°C.
AM_SOC 106	Measured state-of-charge 0-1, with 1 corresponding to fully charged. This number is stored in Q8 format.*
AM_thr 107	Measured throttle position 0-1, stored in Q8 format.*
AM_rgn 108	Measured regen position 0-1, stored in Q8 format.*
SV_desiredphaseI 109	The input phase current regardless of the control or input modes, in deci-A. Negative values are used for negative torque.
SV_desiredspd 10A	The input desired speed in RPM.
SV_targetphaseI 10B	The target phase current, in deci-A rms. Negative values are used for negative torque. Positive torque is defined as accelerating torque in the forward direction. This is the input value to the space-vector PWM algorithm.

*Q-format is the binary equivalent of the metric prefixes used elsewhere. Qn format means that there is an implied decimal point to the right of the n-th bit, where the least-significant bit is bit 0. Equivalently, there is an implied denominator of 2^n. Thus, Q8 format implies “divide by 256,”, so 1.0 in Q8 format is 256, and 0.5 in Q8 is 128.

SV_drivestate 10C

Status bits that relate to the operating state of the controller. These bits are as follows:

Bit	Name	Set to 1 when:
15	reserved	always 0
14	BIT_initialized	the controller has completed its power-up initialization
13	BIT_charging	the charging input is asserted
12	BIT_motornotready	no motor sense cable is plugged in.
11	BIT_interlock	a fault has occurred while the phase current is non-zero
10	BIT_enabled	no disable inputs are asserted
9	BIT_active	the output phase current is non-zero
8	BIT_standby	the controller is in low-power standby mode
7	BIT_transition	the controller is transitioning out of torque production
6-4	reserved	always 0
3	BIT_INdisable	a disable input is asserted
2	BIT_limiting	the output phase current is being limited by the MCL module
1	BIT_spdctrl	the controller is in speed control mode
0	BIT_reverse	the controller is in reverse (CCW rotation of the phase currents)

Bit 15 is the most-significant bit, and bit 0 is the least-significant.

Nine drive states are defined based on the state of bits 14-8. These drive states are as follows:

Drive state	(bits 14-8)	Description
DS_startup	1000_H	The controller is performing its initialization
DS_standby	5100_H	The controller is in low-power standby mode
DS_nomotor	5000_H	Initialized, but no motor sense cable is connected
DS_charging	7100_H	Charger is plugged in and the ignition is off
DS_charging2	7000_H	Charger is plugged in and ignition is on
DS_shutdown	4000_H	Normal powered-down mode
DS_interlock	4800_H	A disable input must be asserted to leave this state
DS_enabled	4400_H	The controller is enabled, but the phase current input is zero
DS_active	4600_H	The drive system is producing accelerating torque
DS_transition	4680_H	The controller is leaving the DS_active state

<table>
<tr><td>SV_fault1latch
10D</td><td>Bits in this status register are set whenever the corresponding bits in the SV_fault1 register are set. They are cleared upon entering the DS_enabled drive state.</td></tr>
<tr><td>SV_fault1
10E</td><td>This status register consists of fault bits that prevent motoring operation. These bits are as follows:

<table>
<tr><th>Bit</th><th>Name</th><th>Set to 1 when:</th></tr>
<tr><td>15-10</td><td>reserved</td><td>always 0</td></tr>
<tr><td>9</td><td>FA1_stuckthr</td><td>the throttle input is nonzero when the forward or reverse input is first asserted</td></tr>
<tr><td>8-7</td><td>reserved</td><td>always 0</td></tr>
<tr><td>6</td><td>FA1_PDPINT</td><td>an internal over-voltage or over-current fault occurs</td></tr>
<tr><td>5</td><td>FA1_lostcomm</td><td>too much time has elapsed since the last message was received from the serial port, and the serial timeout function is enabled (See VC_SCI)</td></tr>
<tr><td>4</td><td>FA1_SCItimeoutzero</td><td>The discrete throttle input is disabled (VC_discrete.9 is zero) and the serial timeout duration is zero (bits 7-0 of VC_SCI are zero).</td></tr>
<tr><td>3-0</td><td>reserved</td><td>always 0</td></tr>
</table></td></tr>
<tr><td>SV_fault2
10F</td><td>This status register consists of sensor error fault bits. These bits are as follows:

<table>
<tr><th>Bit</th><th>Name</th><th>Set to 1 when:</th></tr>
<tr><td>15-14</td><td>reserved</td><td>always 0</td></tr>
<tr><td>13</td><td>FA2_rgnexcite</td><td>rgn+ signal is out of range</td></tr>
<tr><td>12</td><td>FA2_threxcite</td><td>thr+ signal is out of range</td></tr>
<tr><td>11-6</td><td>reserved</td><td>always 0</td></tr>
<tr><td>5</td><td>FA2_SOClost</td><td>state-of-charge lost due to corruption of the non-volatile memory</td></tr>
<tr><td>4</td><td>FA2_SCInoise</td><td>parity or framing error in serial communication</td></tr>
<tr><td>3</td><td>reserved</td><td>always 0</td></tr>
<tr><td>2</td><td>FA2_supplyI</td><td>The voltage on current sense signal shunt+ is greater than 120mV. This is most likely due to an open-circuit on shunt+ or shunt-.</td></tr>
<tr><td>1,0</td><td>reserved</td><td>always 0</td></tr>
</table></td></tr>
</table>

SV_fault3 110	This status register consists of miscellaneous warning messages. These bits are as follows:
SV_thrlimit 111 SV_rgnlimit 112	These status registers identify the dominant current limit for throttle and regen, respectively. The content of each register is a numeric code which corresponds to a current limit as follows: Code Name Current limit: 0 FA4_motorT motor temperature limit 1 FA4_baseplateT controller baseplate temperature limit 2 FA4_undervolt factory low voltage phase current limit 3 FA4_overvolt factory high voltage phase current limit 4 FA4_abslim factory motor or controller phase current limit 5 FA4_softlimit serial phase current limit, SI_thrphaseIlimit, or SI_rgnphaseIlimit 6 FA4_thrdisabled throttle disable input asserted 7 FA4_rgnphaseIlimit discrete regen current limit input (not implemented) 8 FA4_spdgovernor speed governor phase current limit 9 FA4_batIlimit vehicle battery current limit 10 FA4_batIsoftlimit serial battery current limit, SI_dischargeIlimit or SI_chargeIlimit 11 FA4_limphomebatI limp-home mode battery current limit, VC_limphomesupplyI 12 FA4_limphomephaseI limp-home mode phase current limit, VC_limphomephaseI 13 FA4_vehsoftlimit VC_thrphaseIlimit or VC_rgnphaseIlimit 14 FA4_lowspdregen abs(AM_velocity)*VC_rgnslope when in torque control 15 FA4_clutch clutch input asserted 16 FA4_revgovernor reverse-speed governor 17 FA4_dirlatcherror

Page 2: Development

Register	Description
DV_motorTest 200	Estimated motor temperature in deci-C.
DV_baseplateTest 201	Estimated motor temperature in deci-C.
IN_rgnphaseIlimit 202	When in discrete speed control, the regen phase current limit set by the regen input, in deci-A. Otherwise, set to maximum value.
IN_status 203	The digital control inputs to the controller, as follows: Bit — Name — Description: 15 — reserved — always 0 14 — IN_disable — set when any of the disable inputs are asserted 13,12 — reserved — always 0 11 — IN_noignition — ignition input 10 — IN_nocbl — motor cable detection 9 — IN_pdfault — internal fault 8,7 — reserved — always 0 6 — IN_spdctrl — speed control input 5 — IN_neutral — neutral input 4 — IN_thrdisable — throttle disable input 3 — IN_reverse — reverse 2 — IN_forward — forward input input 1 — IN_charger — charger detection input 0 — IN_clutch — clutch input
DV_DIstatus 204	The state of the discrete digital inputs, as follows: Bit — Name — Description: 15-12 — reserved — always 0 11 — DI_noignition — ignition input 10 — DI_nocbl — motor cable detection 9 — DI_pdfault — internal fault 8-5 — reserved — always 0 4 — DI_thrdisable — throttle disable input 3 — DI_reverse — reverse input 2-0 — reserved — always 0

DV_SIstatus 205	The state of the serial digital inputs (set and reset by 00X! commands), as follows: Bit — Name — Description: 15-7 — reserved — always 0 6 — SI_spdctrl — speed control input 5 — SI_disable — disable input 4 — SI_thrdisable — throttle disable input 3 — SI_reverse — reverse input 2 — SI_forward — forward input 1 — SI_charger — charger input 0 — SI_clutch — regen disable input
DV_thermallimitmtr 206	The maximum motor current, in deci-A, due to the motor temperature.
DV_baseplateTderating 207	The derating (0-1 in Q8 format*) of the phase current due to the controller temperature. This value is multiplied by the maximum phase current for the current supply voltage to calculate the maximum phase current of the controller due to temperature.
DV_maxphaseIthr 208	The maximum accelerating phase current, in deci-A, due to all current-limiting constraints
DV_maxphaseIrgn 209	The maximum decelerating phase current, in deci-A, due to all current-limiting constraints
DV_batmaxphIthr 20A	The maximum accelerating phase current, in deci-A, due to limits on the battery discharge current.
DV_batmaxphIrgn 20B	The maximum decelerating phase current, in deci-A, due to limits on the battery charge current.
reserved 20C	reserved
reserved 20D	reserved

Page 3: Vehicle Configuration

Register	Description
VC_SCsupplyI 300	The value of the external supply current shunt, in A at 1V. This can also be computed as 1/R, where R is the resistance in Ohms.
VC_OFsupplyI 301	Offset calibration in deci-A.

VC_discrete 302	Discrete input enable bits and other discrete configuration bits as follows: Bit Name Description: 15,14 reserved should be set to 0 13 BIT_defaultspdctrl set to one to have the controller power-up into speed control 12 BIT_invertdir set to one to define forward as counter-clockwise rotation of the phase currents. 11 EN_discreteignition 10 reserved should be set to 1 9 reserved should be set to 1 8 reserved should be set to 0 7 EN_discretethr set to one to enable the discrete *thr* and *rgn* inputs. 6,5 reserved should be set to 0 4 EN_discretethrdisable 3 EN_discretereverse 2 EN_discretereverse should be set to match bit 3 1-0 reserved should be set to 0
VC_invert 303	Bits 3-4 of this register may be set to 1 in order to invert the corresponding discrete input. Bit Name Description: 15-11 reserved should be set to 0 10 BIT_strictwrongdir when set, the motor speed must be less than VC_spdthreshold in order to clear the FA3_dirlatcherror bit 9 BIT_softstuckthr when set, the stuck throttle interlock is cleared when AM_thr is zero 8-5 reserved should always be set to 0 4 INV_discretethrdisable 3 INV_discretereverse 2-0 reserved should be set to 0
VC_thringain 304	Discrete throttle input gain, in Q8 format
VC_rgningain 305	Discrete regen input gain, in Q8 format
VC_thrdeadband 306	Discrete throttle input bias, in Q8 format
VC_rgndeadband 307	Discrete regen input bias, in Q8 format
VC_thrfilter 308	Discrete throttle input filter value, 0-252

VC_rgnfilter 309	Discrete regen input filter value, 0-252
VC_Xt 30A	Throttle shaping X transition point, in Q8 format
VC_enginedamping0 30B	amount of simulated engine braking to be applied when the speed is <= VC_spd0, in Q8 format. Should always be set to zero.
VC_ enginedamping1 30C	amount of simulated engine braking to be applied when the speed is >= VC_spd1, in Q8 format
VC_Yt0 30D	Throttle shaping Y value at X=VC_Xt when the speed is <= VC_spd0, Q8 format
VC_Yt1 30E	Throttle shaping Y value at X=VC_Xt when the speed is >= VC_spd1, Q8 format
VC_spd0 30F	Throttle shaping and engine braking minimum speed, in RPM
VC_spd1 310	Throttle shaping and engine braking maximum speed, in RPM
VC_lowspdxfrslope 311	Throttle-vs.-regen arbitration coefficient, 1 / RPM in Q15 format.
VC_phaseIposramp 312	The maximum positive derivative of the phase current when the phase current is positive and the discrete throttle input is enabled. The units are A/s. This register limits the vehicle jerk.
reserved 313	reserved
VC_K_soc 314	The gain coefficient for the state-of-charge output in Q12 format.
VC_spdthreshold 315	The maximum speed for direction reversal, in RPM.
VC_softstartT 316	The soft-start duration in ms.
VC_limphomeSOC 317	The threshold state-of-charge in Q8 format. Once AM_soc has dropped below this value, the controller will remain in limp-home mode until the batteries are charged above this value.
VC_limphomesupplyI 318	The maximum battery discharge current when in limp-home mode, in deci-A.
VC_limphomephaseI 319	The maximum throttle phase current when in limp-home mode, in deci-A.
VC_rgnphaseIlimit 31A	The vehicle maximum regen phase current, in deci-A. This register determines the vehicle's maximum regenerative deceleration.
VC_rgnslope 31B	The maximum regen current vs. speed when in torque control. The units are deci-A/RPM in Q8 format
VC_spdSpts[0-3] 31C-31F	The speed (RPM) and phase current (deci-A) points for the speed governor. Below the lowest speed VC_spdSpts[0], the maximum phase current is VC_spdIpts[0], and likewise for speeds above the highest speed.
VC_spdIpts[0-3] 320-323	

VC_dischargeVpts[0-2] 324-326	The voltage (deci-V) and discharge(deci-A) points for the battery discharge current regulator.
VC_dischargeIpts[0-2] 327-329	
VC_chargeVpts[0-2] 32A-32C	The voltage (deci-V) and charge(deci-A) points for the battery charge current regulator.
VC_chargeIpts[0-2] 32D-32F	
VC_FIbatlim 330	The filter setting for the supply current regulators.
VC_maxspderror 331	The maximum speed error (RPM) for the speed control PI regulator.
VC_Kp 332	The proportional coefficient for the speed control PI regulator, in deci-A / RPM in Q8 format
VC_Ki 333	The integral coefficient for the speed control PI regulator, in deci-A / (RPM-s) in Q8 format
reserved 334	reserved
reserved 335	reserved
VC_hsfantemp 336	The baseplate temperature at which the controller fan is turned on, in deci-°C. The fan will stay on until the temperature has dropped two degrees C below this setting.
reserved 337	reserved
reserved	reserved
VC_SCI 339	The serial configuration register. Bits are as follows: Bit — Name — Description: 15-8 — reserved — should be set to 0 7-0 — VC_maxSCIidle — the maximum time (centi-s) between received characters to prevent a SCI timeout fault, 0 disables.
reserved 33A	reserved
VC_spddeadband 33B	below this speed, the discrete regen input is disabled, in RPM.
VC_revSpts[0-1] 33C-33D	The speed (RPM) and phase current (deci-A) points for the reverse speed governor. Below the lowest speed VC_revSpts[0], the maximum phase current in reverse is VC_revIpts[0], and likewise for speeds above the highest speed.
VC_revIpts[0-1] 33E-33F	

Page 4: Battery Configuration

Register	Description
BC_initbatcapacity 400	The nominal battery capacity in deci-Ahrs.
BC_fullchargeV 401	The threshold voltage (deci-V) and charge current (deci-A) for detecting when the batteries have been fully charged. Once the battery voltage has been above BC_fullchargeV and the charge current has been less than BC_fullchargeI for BC_fullchargeT deci-seconds, the state-of-charge is reset to 100%
BC_fullchargeI 402	
BC_fullchargeT 403	
BC_ahrIpts[0-7] 404-40B	The battery current (deci-A, negative for discharge current) and weighting coefficients (Q8 format) for the weighted amp-hour integration state-of-charge algorithm.
BC_ahrKpts[0-7] 40C-413	

Page 5: Reserved

Page 6: Motor Configuration

Register	Description
MC_FI_motorT 600	The filtering time constant for the motor temperature sensor, 0-255. Zero corresponds to no filtering, 255 to maximum filtering. Values outside this range give invalid measurements, and values between 253 and 255 can cause significant rounding errors.
MC_user_mtr[0-1] 601-602	User values can be stored in these unused registers.

Page 7: Motor Calibration

Register	Description
MA_Kimpts[0-1] 700-701	The integral and integral coefficients for current regulation (in engineering units) vs. motor speed, in RPM.
MA_Kpmpts[0-1] 702-703	
MA_spdpts[0-1] 704-705	
MA_SCmotorT 706	The scale coefficient for the motor temperature sensor. Set this to 100/(V per deg C).
MA_OFmotorT 707	The offset coefficient for the motor temp sensor, deci-C. Set this to -10*(V at 0 °C)/(V per °C).

MA_motorITcoeff 708	The scaling coefficient for the I^2t temperature estimation calculation.
MA_motortimeC 709	The time constant for the I^2t temperature estimation calculation.
reserved 70A	reserved, set to -1
reserved 70B	reserved, set to -1
MA_OFutateangle 70C	The angular offset of the commutation signals, where the angle is expressed 0-4095. An offset of 0 corresponds to commutations occurring at 0,60…300° electrical.
MA_maxerror 70D	the maximum per-unit error for current regulation

Page 8: Motor Factory Settings

Register	Description
MF_maxmotorI 800	The maximum motor phase current in deci-A RMS.
MF_defaultmtrT 801	The default motor temperature in deci °C, used when the temp sensor has failed.
MF_tempTpts[0-3] 802–805	The temperature (deci °C) and current (deci-A) points for the motor temperature governor. The estimated temperature DV_motorTest is used for this calculation.
MF_tempIpts[0-3] 806–809	
MF_polepairs 80A	The number of pole-pairs, one-half the pole count.

MF_mtrsensors 80B	The motor sensor configuration register. The bits are assigned as follows: Bit Name Description: 15-9 reserved should be set to 0 8-7 reserved should be set to 1 6 reserved should be set to 0 5 reserved should be set to 1 4-3 reserved should be set to 0 2 MTR_invertcom2 when set to 1, the polarity of commutation bit 2 is inverted. 1 MTR_invertcom1 (as above) 0 MTR_invertcom0 (as above). Bits 2-0 should be set so that the resulting commutation codes correspond to the following sequence: 210 Angle (electrical) 000 x° 001 x+60° 011 x+120° 111 x+180° 110 x+240° 100 x+300° where x is an arbitrary offset. MA_OFutateangle should be set to -4096*x/360.
reserved 80C	reserved
MF_pwmfreq 80D	The PWM frequency, set to 8,000Hz.
MF_pherrfilter 80E	The time constant for the phase error correction algorithm in engineering units.

Page 9: Controller Configuration

Register	Description
CC_FI_supplyV 900	The filtering time constants for the analog inputs, 0-255. Zero corresponds to no filtering, 255 to maximum filtering. Values outside this range give invalid measurements, and values between 253 and 255 can cause rounding errors.
CC_FI_supplyI 901	
CC_FI_baseplateT 902	
CC_FI_ambientT 903	

CC_FI_motorT2 904	A placeholder. The controller copies the motor temperature time constant to this location.
CC_user[0-1] 905-906	User values can be stored in these unused registers.

Page A: Reserved

Page B: Controller Factory Settings

Register	Description
CF_thrVpts[0-4] B00-B04	The voltage (deci-V) and phase current (deci-A RMS) throttle phase-current governor points.
CF_thrIpts[0-4] B05-B09	
CF_rgnVpts[0-4] B0A-B0E	The voltage (deci-V) and phase current (deci-A RMS) regen phase-current governor points.
CF_rgnIpts[0-4] B0F-B13	
CF_default_hsinkT B14	The baseplate temperature to use when the sensor fails, deci-°C.
CF_tempTpts[0-3] B15-B18	The temperature (deci-°C) and phase current (deci-A RMS) baseplate governor points. The estimated baseplate temperature DV_baseplateTest is used for this calculation.
CF_tempIpts[0-3] B19-B1C	
CF_spdrate B1D	The rate at which speed measurements are made in Hz.
reserved B1E -B1F	reserved
CF_SN1 B20	The controller serial number, SN1 is the least significant word.
CF_SN2 B21	
CF_swbuild B22	The software build number.
CF_swbuilddate B23	The software build date expressed as YYWW.

Page C: Integrations

Register	Description
NV_hours[0-1] C00-C01	The number of milli-hours that the controller has been powered. The lower address is the least significant word.
NV_revs[0-1] C02-C03	1/1000 of the number of motor revolutions for motors connected to the controller.
NV_activehours[0-1] C04-C05	The number of milli-hours that the BIT_active bit has been set in the controller.
NV_amphours[0-1] C06-C07	The number of weighted milli-A-hours in the vehicle traction battery.
NV_chargehours[0-1] C08-C09	The number of milli-hours that the vehicle has spent on charge.
NV_batcapacity C0A	The battery capacity in deci-A hours. This value is adjusted by the aging calculation
NV_checksum C0B	A checksum for the Integration registers.

12 Appendix D: Warranty

NGM Warranty

New Generation Motors Corporation warrants that its EVC402 motor controller will be free from defects in title, materials, and manufacturing workmanship for one (1) year. If an EVC402 motor controller is found to be defective, then, as your sole remedy and as the manufacturer's only obligation, New Generation Motors Corporation will repair or replace the product. This warranty is exclusive and is limited to the EVC402 motor controller.

This warranty shall not apply to EVC402 motor controllers that have been subjected to abuse, misuse, abnormal electrical or environmental conditions, or any condition other than what can be considered normal use (including, but not limited to, opening of the controller for any purpose).

Warranty Disclaimers

New Generation Motors Corporation makes no other warranties, express, implied, or otherwise, regarding EVC402 motor controllers, and specifically disclaims any warranty for merchantability or fitness for a particular purpose.

The exclusion of implied warranties is not permitted in some States and countries thus exclusions specified herein may not apply to you. This warranty provides you with specific legal rights. There may be other rights that you have which vary from State to State.

Limitation of Liability

The liability of New Generation Motors Corporation arising from this warranty and sale shall be limited to the replacement of defective parts. In no event shall New Generation Motors Corporation be liable for costs of procurement of substitute products or services, or for any lost profits, or for any consequential, incidental, direct or indirect damages, however caused and on any theory of liability, arising from this warranty and sale. These limitations shall apply not withstanding any failure of essential purpose of any limited remedy.