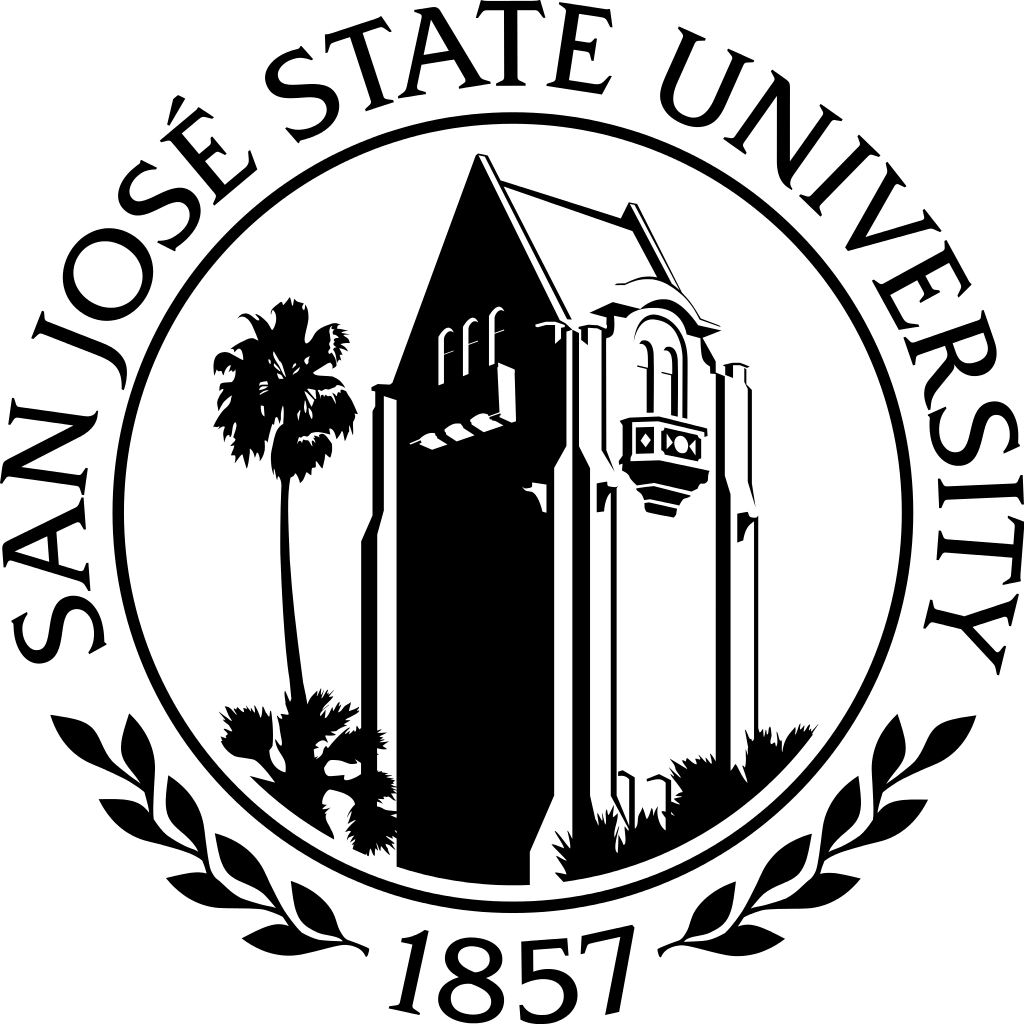
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**CmpE Internship Summer 2018**

**Design Document**

***LPC40xx SSP Driver***

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**Revision History:**

|  |  |  |
| --- | --- | --- |
| **Revision** | **Date** | **Description** |
| **A.1** | **xx/6/18** | **Initial Design Documentation Draft** |

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# **Objective**

The objective of this driver is to provide a generic SSP template for the LPC40xx series of microcontrollers. The template must allow the user to configure any of the three SSP ports as needed.

# **Background**

Various Issues Regarding input devices for vendors:

<https://blogs.msdn.microsoft.com/oldnewthing/20050112-00/?p=36723>

Coca Cola Machines Patents

<https://patents.google.com/patent/US7161494>

# **Overview**

One page-ish high level description of what you are doing. Should be understandable by other engineers.

The PMOD 16-button input device allows for a specified input to be run into the machine before outputting to the output module PMOD Character LCD display.

# 

# **Detailed Design**

Detailed description of what you are designing and how.

In order to design this project, the user must be able to have prior knowledge of state machines. By having state machines, the project will be able to produce an a valid output. Now, a valid input is determined from the Pmod 16-button module device which will detect if two subsequent values are correct. The two subsequent values will consist of a number and a letter. During the wait state if the two values are given, the output device will indicate to the user that it will work.

The signal assignment convention for the Pmod devices will be as followed:

|  |  |  |
| --- | --- | --- |
| Pin | Signal | Direction |
| 1 | IO1 | In/Out |
| 2 | IO2 | In/Out |
| 3 | IO3 | In/Out |
| 4 | IO4 | In/Out |
| 5 | GND |  |
| 6 | VCC |  |

# 

# **Caveats**

List any caveats to the design choices if there are any. Really thing about this section.

Before starting this project the user must have access to both Pmod Devics. Without these, the program will not be set out to be intended.

# **Testing Plan**

### **Unit testing scheme**

Describe how you will go about writing unit tests on your host machine.

### **Integration Testing**

Describe how you will go about doing integration testing (ie testing on the SJTwo board).

### **Demonstration Project**

To demonstrate that your library can **do the thing** we would like you to have some code that demonstrates the capabilities of your library.