

Hyper-Kamiokande Outer Detector Light Injector System Technical Note

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September 26, 2025

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⁴⁶ **0 Version history**

- ⁴⁷ • v0.99 - First release by Balint circulated to Liverpool group for internal review
- ⁴⁸ • v1 - [Sam]: Ported over to github for continued development, as we hit compilation
⁴⁹ time on overleaf. Initial pass through to fix wording and rewrite some sections. Also
⁵⁰ integrating Warwick TN on OD diffuser. Will add Liz's saturation studies as soon as
⁵¹ these are available. Some reordering of structure to make it flow better.

52 **1 Introduction**

53 Hyper-Kamiokande is a large scale water Cherenkov detector with two main sections, an
54 inner detector (ID) and an outer detector (OD). The OD volume of Hyper-K is a one meter
55 wide annular ring on the circumference of the detector. This space is designed to tag charged
56 particles, such as cosmic ray muons or particles from interactions in the surrounding rock,
57 entering the detector. In addition, the OD volume will be used as working space for instal-
58 lation activities. Once complete, it will be optically separated from the ID volume, and will
59 be instrumented with 3,600 outward facing 8 cm photomultipliers tubes (PMTs). These will
60 each surrounded by wavelength shifting (WLS) plates to increase photocoverage.

61 In order to achieve the precision measurements Hyper-K aims to make, precise calibration
62 of the detector is required. For the OD, a light injection (LI) system will be employed,
63 allowing for known quantities of light to be injected into the detector region. This will
64 consist of 122 diffusers and 12 collimators. The diffuser system, which is described in this
65 technical note, will be used to measure gain and timing properties of the OD PMTs, and
66 will be powered by dedicated pulsed LED sources. The 12 OD collimators are identical to
67 those uses in the ID system, and will be integrated into the ID laser system. Full details on
68 that system, along with investigations of the fibre optics that will be employed for the OD
69 system, can be found in [1].

70 **2 Light Injection System Overview and Requirements**

71 The OD diffuser system will be composed of 122 bare diffusers, installed on the outward
72 facing side of the PMT support structure. The diffuser design is discussed in Section 4.
73 These will each be illuminated by individual LED pulser boards, with 365 nm LEDs. This
74 will require at least 122 dedicated LED pulsers, and spares should be readily available for hot-
75 swapping should a board encounter issues. Full details of the pulser board design are given
76 in Section 6. The pulser boards will be powered and controlled by commercially-available
77 Field Programmable Grid Array (FPGA) boards. The control system architecture for these
78 consists of three primary components:

- 79 • **Blade:** Interfaces directly with the FPGA, distributing all differential signals into the
80 crate system.
- 81 • **Backplane:** Routes differential signals to the pulser boards and provides the primary
82 power distribution, accepting 12 V and ± 5 V inputs.
- 83 • **Eurocards:** Host the pulser boards, receive power and differential signals from the
84 backplane, and incorporate the necessary circuitry for laser triggering.

85 Further details on the control system and individual electronics crate components are given
86 in Sections 9 and 10 respectively.

87 Light will be transported between the pulsers and diffusers by a series of fibre optic
88 cables; following the investigations in [1] the Thorlabs FP400URT [2] is targeted for this.
89 Due to production limitations, it is not possible to keep all fibre path lengths the same.
90 Instead there will be five different lengths: 50 m, 80 m, 106 m, 124 m and 168 m. The
91 light output after signal attenuation and dispersion in these fibres should be as consistent
92 as possible, which will require fine tuning given the different amounts of attenuation and
93 dispersion which pulses will experience based on fibre length.

94 The initial design requirements for the system are to produce pulse widths out of the
95 diffuser of between 1–10 ns, with a photon yield in the range 1–15 million photons per pulse
96 (ppp). The 10 ns limit is driven by the timing resolution of the WLS plates. The photon

yield target here is more of a goal than a requirement, and saturation studies were performed using numbers motivated by system performance. These are summarised in Section 3.

The below paragraph should split up. The first half has been rewritten into the above paragraph, the second should be fleshed out for the photon yield test section.

Pulse width should ideally be between 1-10 ns and the photon count from 1-15 million photons, but higher limits are preferable. The lower limits are not possible to achieve, as the fibre dispersion will create a minimum pulse width, which is 4.5 ns at 180 metres, and if we try to achieve large light output it will compromise our lower light output, so we can only achieve around 100,000 photons per pulse at minimum. While these compromises are not ideal, the fibre selection limits our capabilities on hitting the required theoretical targets.

3 OD PMT Saturation Studies

4 Diffuser Design

4.1 ID Diffuser Hemisphere Design

4.1.1 Inner Detector Diffuser Design

The diffusers used to scatter input laser light in the inner detector volume are 2.54 cm half-spheres fabricated from PTFE. This is used as it

- is unaffected by immersion in water
- acts as a excellent diffuser
- is a good transmitter of UV light
- is easy to machine and clean

A mechanical drawing of the inner detector diffuser hemispheres is shown in Figure 1

4.1.2 Diffuser Profile Measurement System

A scanning system was built to measure the output characteristics of diffuser hemispheres. Enclosed in a dark box, the diffuser is mounted onto two rotary stages which gives the freedom to rotate the diffuser around the nominal axis linking the diffuser with the photosensor. This scanner only takes scans in an air medium, and the setup is illustrated in Figure 2.

A laser powered from a wall plug is used to illuminate the diffuser with light at a wavelength of 450 nm. It is triggered by a function generator with 1000 triggers per burst at a frequency of 2 kHz. The open beam is directed via a mirror, a circulator, and a lens to the fibre launch stage, and then via an optical fibre towards the diffuser. The diffuser enclosure is fixed with three screws on the double-rotation stage. Measurements of bare diffuser profiles, i.e. without enclosure, are conducted with the bare fibre end positioned in the centre of the rotation stage using a 3D printed frame. The bare fibre end is kept in place due to friction on the connection point with the diffuser hemisphere. A photograph of the rotation stage with a bare diffuser hemisphere is shown in Figure 3.

A PMT measures the diffuser spectrum at a fixed position, with 62 cm distance to the diffuser enclosure and a 3 mm pinhole aperture, restricting the solid angle viewed by the PMT to $2 \cdot 10^{-5}$ sr. For comparison, a single 50 cm PMT in the HK far detector receives light from a point source at the other side of the tank over a solid angle of approximately $2.2 \cdot 10^{-4}$ sr. The PMT signal is digitised at a sampling rate of 2500 MHz over 1000 cycles, allowing to

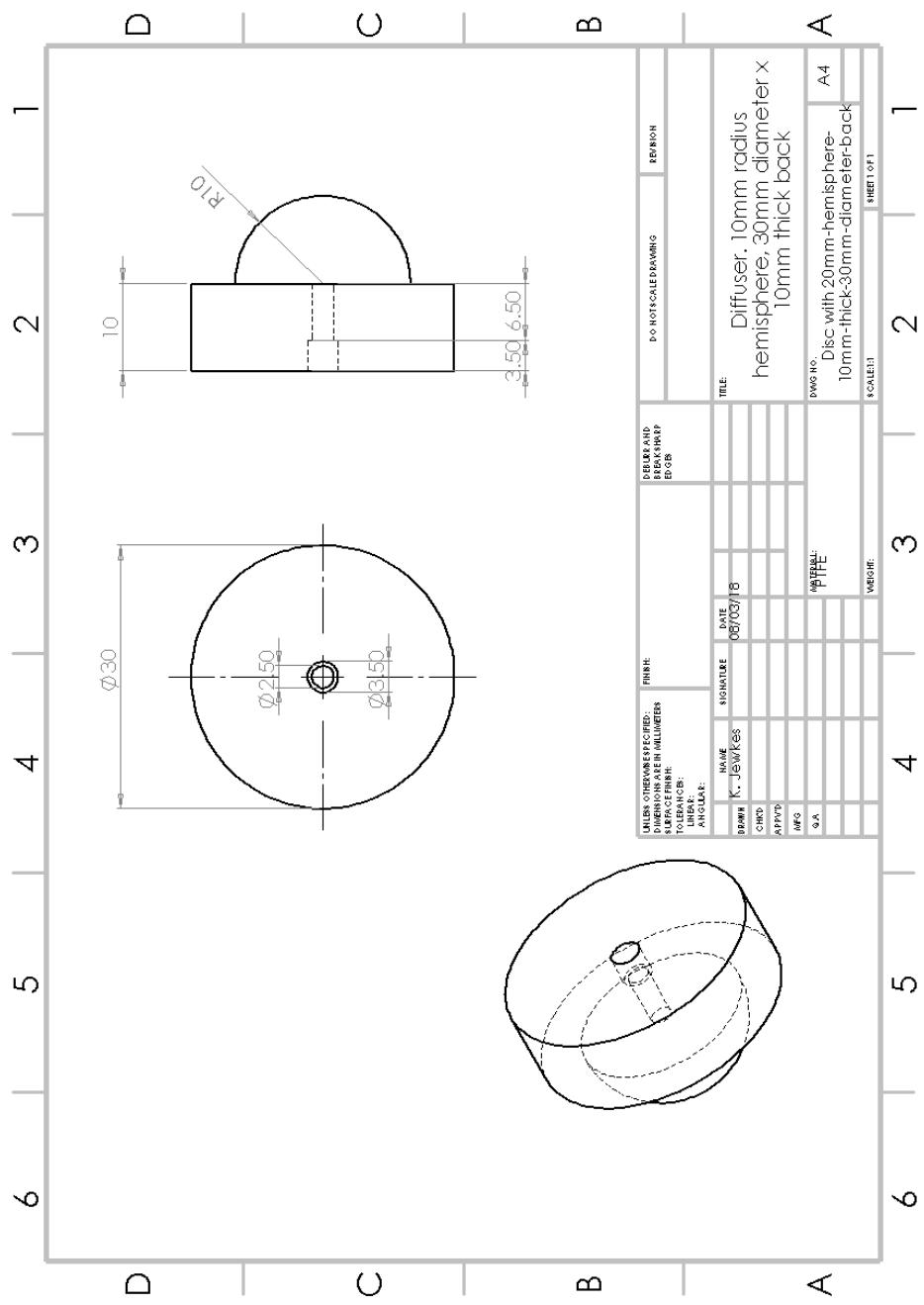


Figure 1: Bare Diffuser Mechanical Drawing

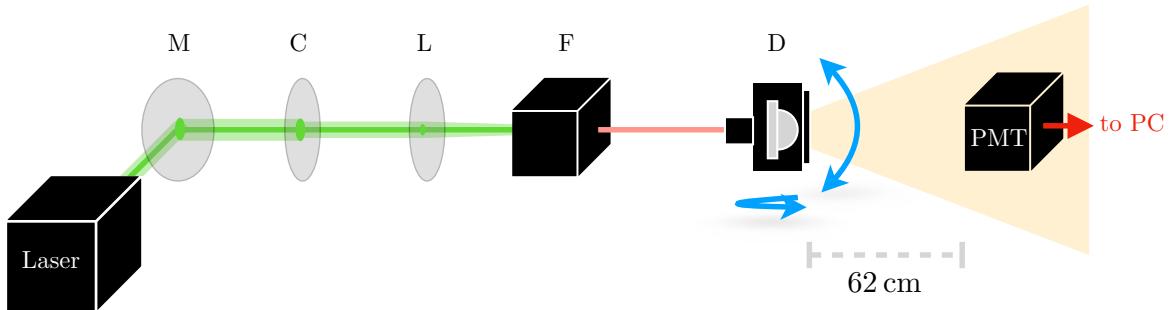


Figure 2: Setup for diffuser scans: light from the laser is directed via a mirror (M), a circulator (C), and a lens (L) to the fibre launch stage (F). From there, the light goes via an optical fibre to the diffuser (D) on the rotation stage.

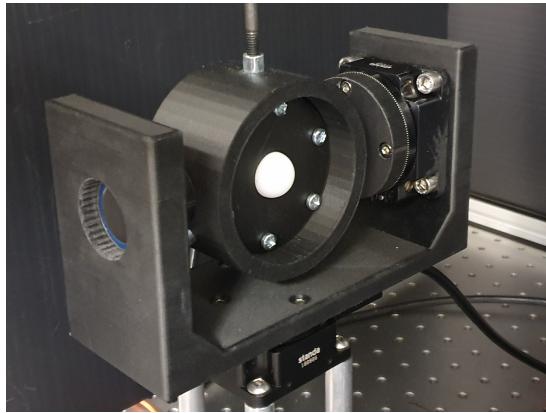


Figure 3: Rotation stage with bare diffuser hemisphere mounted using a 3D-printed frame.

137 resolve the shape of each single signal waveform. The light yield at each coordinate is then
 138 obtained as the average waveform area across all digitised signals.

139 The diffuser profile measurement system is discussed in detail in [3].

140 4.1.3 Diffuser Power Measurement System

141 In addition to the profile measurement functionality, the integrated power output from the
 142 diffuser was measured using an integrating sphere from Ophir. This sphere provides an
 143 unbiased measurement of the total light output power of any light source, regardless of the
 144 shape of the emission profile. A bespoke diffuser holder suitable for connection to one of the
 145 integrating sphere ports was 3D-printed, as was a holder for the optical fibre from the laser
 146 source.

147 A bare PTFE hemisphere was mounted into this holder and connected into the integrating
 148 sphere port. The bare end is inserted into the connection point in the same manner as for
 149 a bare profile scan. Tape was used to prevent light leaking out of the back
 150 of the hemisphere during the measurement, which also helped to keep the fibre in place.
 151 The hemisphere was then illuminated with light from the same laser, this time running on
 152 a continuous rather than burst setting. On the continuous setting light is supplied in a
 153 sinusoidal manner at a frequency of 1 kHz. Power measurements were taken once per second
 154 for a period of ten seconds to account for small fluctuations in laser intensity, the mean of
 155 which served as the final power measurement for that hemisphere.

156 In order to calculate a power ratio, a measurement of power for the bare fibre also needed
 157 to be obtained. This was done in a similar manner to a power measurement for a hemisphere,

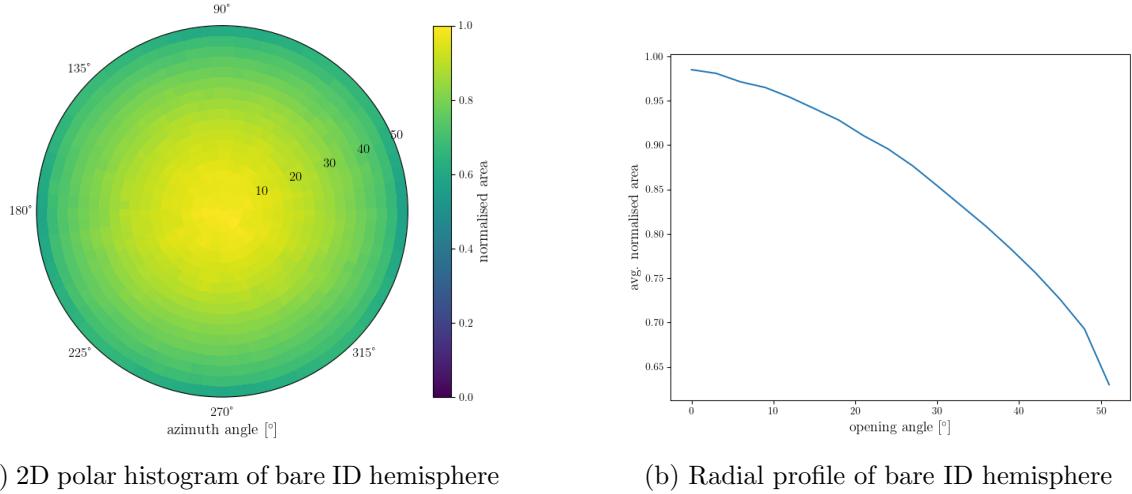


Figure 4: Profile scan of a standard bare ID diffuser hemisphere

158 using the same laser and data acquisition settings. To make the comparison between fibre and
 159 hemisphere measurement as accurate as possible, a special hemisphere was created with the
 160 fibre connection point extended into a hole that runs through the length of the hemisphere.
 161 The bare fibre can then be inserted all the way through until it pokes out of the front,
 162 allowing a power measurement for the bare fibre to be taken with the conditions inside the
 163 integrating sphere as close as possible to hemisphere measurements. The ratio of hemisphere
 164 power to fibre power can then be taken to determine the amount of light lost.

165 A table of systematics for the power ratio measurement is shown in Table I. Rotation
 166 refers to changing the orientation at which the diffuser is placed into the holder, and dif-
 167 fuser re-insertion refers to removing the diffuser from the holder and replacing it. Fibre
 168 re-insertions refers to disconnecting and re-connecting the fibre into the diffuser, while bare
 169 fibre refers to dis- and re-connecting the fibre when taking bare fibre measurements. This
 170 results in a total systematic of 5.3% for a diffuser measurement and 1.8% for a fibre mea-
 171 surement, and therefore an uncertainty of 5.6% in a power ratio measurement.

Systematic	Std. dev. (%)
Rotation	1.4
Diffuser re-insertion	1.0
Fibre re-insertion	5.0
Bare fibre re-insertion	1.8

Table I: Integrating sphere systematics for the power ratio measurement.

172 4.2 OD Diffuser Design

173 The original intention was to use the same diffuser hemisphere design for the OD diffusers
 174 as will be used for the ID diffusers. However, the standard diffuser emits less than 20% of
 175 the power delivered by an optical fibre. As there are a number of interfaces in the optical
 176 pathway between the light source and the diffuser, and as the light source for the OD will be
 177 LEDs, this was considered too low to be able to effectively illuminate the OD space. Neither
 178 the number of interfaces in the optical chain, nor the light source can be changed easily, but
 179 it is possible that an alternate design of the diffuser hemisphere could yield more light.

180 Light is lost to two mechanisms in the standard diffuser; absorption by the PTFE and



Figure 5: A prototype of the OD diffuser with a 2 mm top hat.

181 backscattering. Both loss mechanisms would be minimised if there were less PTFE in the
 182 light path. The design for the OD diffuser section was modified to be the shape of a top
 183 hat, as shown in Figure 5. The optimal depth was studied by taking profile and power
 184 ratio measurements using the same diffuser, but at smaller and smaller depths; after each
 185 measurement was completed, 2.0 mm was cut from the top-hat, and the measurements were
 186 re-taken. This procedure was repeated until the top-hat was 2.0 mm high.

Top-hat depth (mm)	Power ratio (%)
10.0	19.2
8.0	32.4
6.0	31.5
4.0	42.1
2.0	55.2

Table II: Power ratio measurements for each depth of the top-hat

187 Results of the power ratio measurements are shown in Table II. As expected, power ratio
 188 increases with decreasing top-hat depth, making the optimum depth 2.0 mm. The profile as
 189 shown in Figure 6 confirms that the shape of the profile is still suitable.

190 Based on these studies, we propose to change the OD diffuser design from a hemisphere
 191 to a top-hat with a 2.0 mm height above the base. The diffuser will still be fabricated from
 192 PTFE, but this new design (i) emits more light at higher emission angles (ii) doubles the
 193 amount of light that is emitted for a given LED power setting and (iii) is significantly easier
 194 to fabricate in bulk.

195 5 OD Diffuser Mounting System and Installation

196 The OD space will be illuminated by a total of 122 OD diffusers, 19 on each of the top and
 197 bottom caps, and 84 in the barrel. The barrel diffusers are distributed in 7 vertical layers
 198 each consisting of 12 OD diffusers. Due to the numbers and cost, the mounting system must
 199 be relatively small, easy to fabricate and easy to install. Installation will be carried out by
 200 workers on the gondola in the OD space after the Tyvek has been installed and as the fibres
 201 are being installed. The gondola worker will install the fibre in the OD diffuser, and fix the
 202 mount to the HK frame, oriented into the OD space. Since this is being done on the gondola,
 203 the mount needs to be small, easy to store, and straightforward to install.

204 Drawings for the OD diffuser prototype mount can be seen in Figure 7 and pictures of the

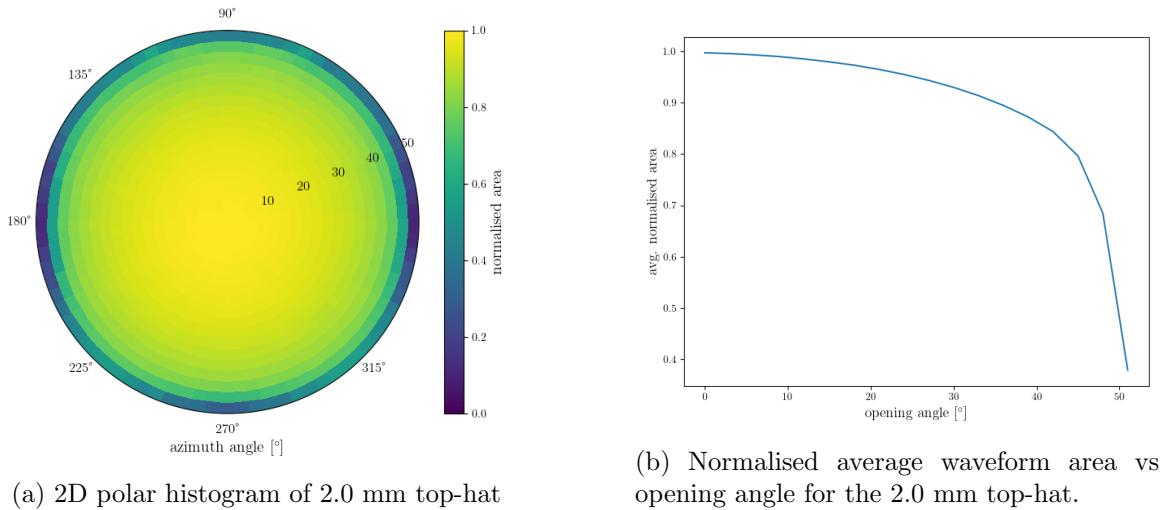


Figure 6: Profile scan of the 2.0 mm top-hat



Figure 7: (left) Front view of the prototype of the OD diffuser mount and (right) rear view of the prototype of the OD diffuser mount.

205 prototype can be seen in Figure 8. The mount is made from stainless steel and is designed
206 to hook over a horizontal frame bar, and screw in from the bottom. The PTFE mount is
207 approximately 5 cm on a side. The fibre will be installed from the back and is held in place
208 by a T-shaped component that is screwed down by the gondola worker.

209 6 Pulser Board

210 6.1 Pulser Board Overview

211 The pulser board was designed to be a more efficient and compact version compared to
212 Super-Kamiokande UK Light Injection system, improving on efficiency, functionality, and
213 light output. The pulser board is a rather simple board designed for low cost production.
214 This section explains each circuit, component selection and design decision. As of writing,
215 the board development is v0.9. v1.0 will be ready by September and will have only minor
216 changes and adjustments compared to v0.9, mostly centered on refinement and removing the
217 prototyping circuit.

218 6.2 Physical dimensions and construction

219 The dimensions of the Printed Circuit Board (PCB) were selected to be as compact as prac-
220 ticable, while still providing sufficient area for the secure mounting of a fibre coupler and for

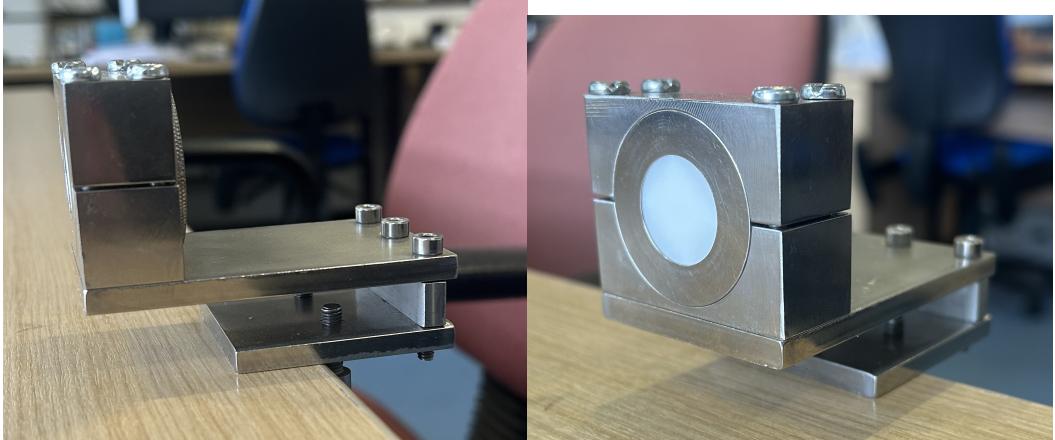


Figure 8: (left) Side view of the prototype holder and (right) front view of the prototype holder.

the components. The final board size is 50 mm × 30 mm. This configuration permits electrically noisy components, such as switching power supplies and the Low Voltage Differential Signal to Transistor Transistor Logic (LVDS-to-TTL) converter to be positioned at a maximum distance from the switching circuitry, thereby minimising potential electromagnetic interference.

Although it is technically feasible to further reduce the board size, preliminary design studies and practical build indicated no substantial benefit in doing so. The board density cannot be significantly increased inside the crate due to FPGA LVDS count and Eurocard dimension, and cost analyses revealed negligible differences associated with a smaller PCB footprint. Furthermore, the chosen dimensions provide an adequate area for the fibre coupler and the necessary mounting holes to affix the pulser board onto the Eurocard, thereby ensuring reliable optical alignment and mechanical stability. The PCB is fabricated as a four-layer FR4 [4] board with a thickness of 0.8 mm, in accordance with the standard construction offered by PCB Train/Newbury Electronics¹, see Figure 9. Refer to Figure 10 for the 3D model of the pulser board. The Top Layer and Inner Top Layer are shown in Figure 11, and the Inner Bottom Layer and Bottom Layer are likewise illustrated in Figure 12. A combined view of all PCB layers is provided in Figure 13.

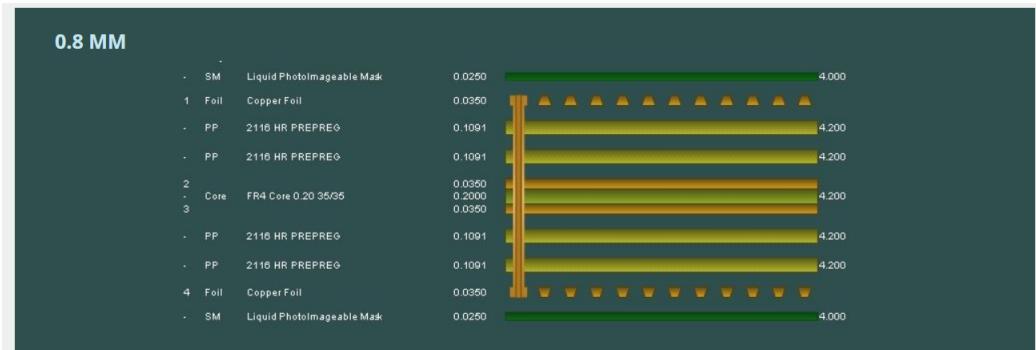


Figure 9: PCB Train's 4 Layer 0.8mm Layer Stack

¹These are trading names of the same manufacturer.

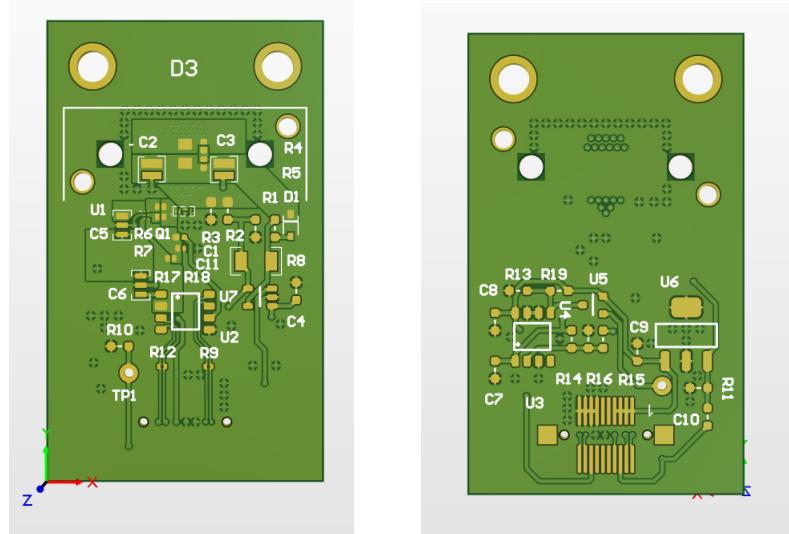


Figure 10: Pulser Board's 3D view Top and Bottom

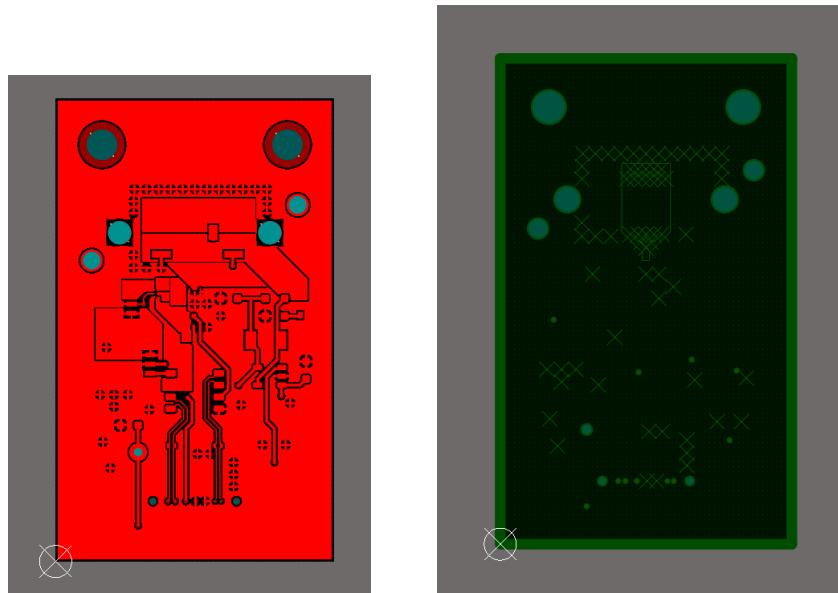


Figure 11: Pulser Board Top and Inner Top Layer

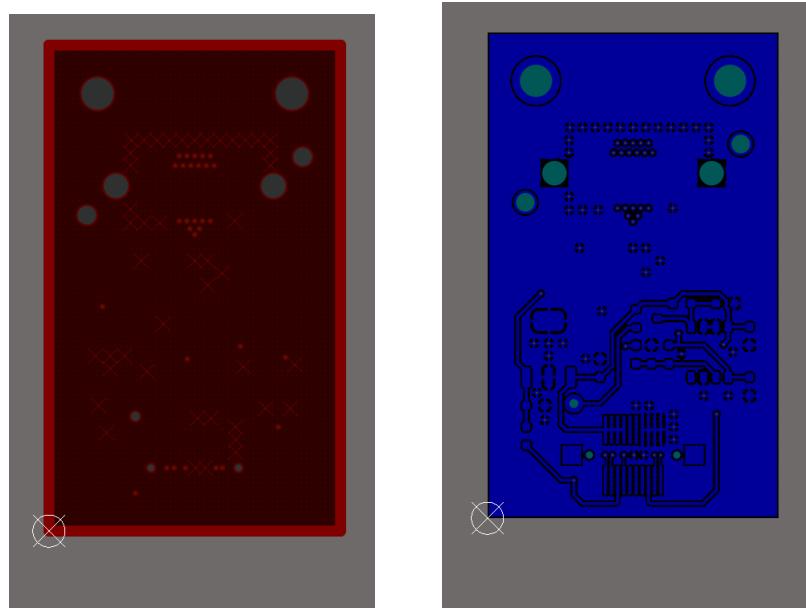


Figure 12: Pulser Board Inner Bottom and Bottom Layer

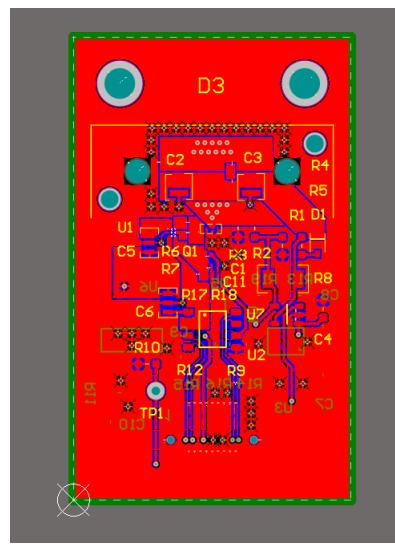


Figure 13: Pulser Board Layer Overview

238 6.3 LED

239 6.3.1 Overview

The LEDs are the most crucial component in the system as the characteristics of these primarily determine the light output, regardless of electronics. LEDs are usually not rated for such high-speed applications, which meant LEDs had to be tested and validated in-house, as datasheets do not provide the required information. The specification required was a 1–10 ns clean single pulse, sub-400 nm wavelength, small surface mount package, narrow output beam so it can be coupled to a fibre with reduced losses and a good range of photon output. Several LED packages were purchased from Kingbright and LC-LED, and their performance tested. The results of these tests are given in Section 6.3.4.

248 6.3.2 Switching Circuit

The redesign process provided a valuable opportunity to evaluate a revised layout and new components for the switching circuit. Several enhancements have since been implemented in the revised switching circuit. Most importantly, the switching side of the layout has been rerouted. In contrast to the previous configuration, where current would flow through the limiting resistor regardless of the LED state, the updated design only allows current flow when the LED is active (refer to Figure 14). This modification reduces both thermal dissipation and the overall power consumption of the system. To modulate light intensity, a variable power supply is now employed to adjust the voltage supplied to the LED. This method has proven highly effective. Tests were conducted at various voltage levels using the full 181 m length of optical fibre—the maximum expected in Hyper-K at the time of testing—and the resulting photon output ranged from approximately 1×10^5 to 2×10^7 photons per pulse. Refined testing results are shown in Section 6.3.4. Further discussion regarding the implementation and performance of the variable voltage supply is provided in Section 6.5.

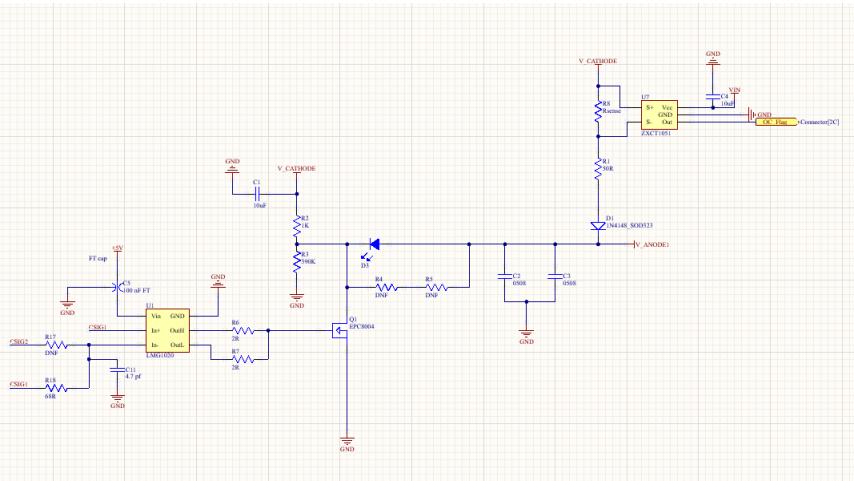


Figure 14: Switching Circuit Layout with LMG1020 and over current IC, R4 is 6.8 nH inductor and R5 is 3R3 resistor

263 6.3.3 Switch Selection

The previous iteration of the pulser board utilised a BFR92 [5] high-speed RF NPN switching transistor which was directly driven by a LVDS-to-TTL converter. In the redesign phase,

266 alternative circuit topologies were explored—particularly those suitable for generating (sub-
267)nanosecond pulses. This investigation led to the adoption of gate driver circuits. Gate
268 drivers are advantageous not only because they can power switches with challenging drive
269 requirements, but also because sub-nanosecond electrical pulses can be achieved by modu-
270 lating the enable pin with slight timing offsets.

271 The fastest commercially available gate driver identified was the Texas Instruments
272 LMG1020 [6]. This device supports pulse widths down to 1 ns, with typical rise and fall
273 times of 400 ps. Additionally, it features an enable pin that allows for precise nanosecond
274 pulse shaping ². The LMG1020 is compatible with both Gallium Nitride Field Effect Tran-
275 sistor (GaN) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) switches,
276 broadening the scope for future component integration and experimentation. It is widely
277 available and priced at £1.97 per unit in the quantities we will require for full production.

278 For the switching element, enhancement-mode GaN transistors manufactured by EPC
279 were selected due to their superior switching characteristics. This recommendation origi-
280 nated from Nick Braam, an engineer at the University of Victoria, who contributed to the
281 pulser board design for the mPMT system **TN52**. Two EPC devices were shortlisted: the
282 EPC2012 [7] and EPC8004 [8]. The EPC2012 offers a simpler footprint, which could re-
283 duce manufacturing defects. However, the EPC8004 features lower parasitic capacitance,
284 see Figure 15 for the EPC2012 values and Figure 16 for EPC8004 values, leading to better
285 high-speed performance.

286 To evaluate optical output performance, a 40 m length of FP400URT [2] optical fibre, a
287 Mouser-sourced 385 nm LED (ATS2012UV385 [9]), and a Hamamatsu H10721-210 [10] PMT
288 were used. The EPC-based configurations exhibited nearly identical pulse shapes, whereas
289 the BFR92-based circuit’s pulse shape was less sharp at identical pulse widths, as shown in
290 Figure 17. Consequently, the EPC8004 (Figure 18) was chosen for implementation. Opti-
291 mal performance of the EPC GaN switches required careful layout considerations. A layout
292 was developed in accordance with EPC’s design guidelines [11], targeting minimal parasitic
293 inductance and capacitance. The design employs two layers placed directly above one an-
294 other, utilising large copper planes and multiple vias to ensure uniform current distribution.
295 The PCB will be fabricated and assembled by PCB Train, using their 0.8 mm thick, four-
296 layer stack-up, which offers minimal inter-layer separation for optimal electrical performance
297 (Figure 9). This same layout strategy was applied to the BFR92 circuit to provide a fair
298 performance comparison.

299 A significant challenge at low pulse widths is the presence of a trailing edge or “tail” in
300 the LED output. This effect arises due to charge accumulation and the intrinsic capacitance
301 of the LED, resulting in extended decay times and pulse broadening (see Figure 19). To
302 mitigate this, a parallel modified snubber circuit was implemented, consisting of a 6.8 nH
303 inductor and a 3.3 Ω current-limiting resistor. Upon LED turn-off, the inductor generates an
304 electromotive force (EMF) that actively extracts residual charge from the LED, accelerating
305 its shutdown. The effectiveness of this approach is illustrated in Figure 20. Additionally,
306 two 0508 reverse-topology 100 nF capacitors have been incorporated. Their role is to act as
307 local energy reservoirs, providing rapid current delivery to the LED during pulse operation,
308 surpassing the response time of the main power supply.

309 6.3.4 Testing

310 For testing purposes, the previous-generation United Kingdom Light Injection (UKLI) moth-
311 erboard and associated software were utilised in conjunction with a prototype of the next-
312 generation pulser board. This prototype consisted of four distinct circuit variants: one

²See page 12 and 13 in [6].

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)					
C_{ISS}	$V_{\text{DS}} = 100\text{ V}, V_{\text{GS}} = 0\text{ V}$		128	145	pF
C_{OSS}			73	95	
C_{RSS}			3.3	4.4	

Figure 15: EPC2012 Capacitance Values IC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics[#] ($T_j = 25^\circ\text{C}$ unless otherwise stated)					
C_{ISS}	$V_{\text{GS}} = 0\text{ V}, V_{\text{DS}} = 20\text{ V}$		45	52	pF
C_{OSS}			23	34	
C_{RSS}			0.8	1.3	

Figure 16: EPC8004 Capacitance Values IC

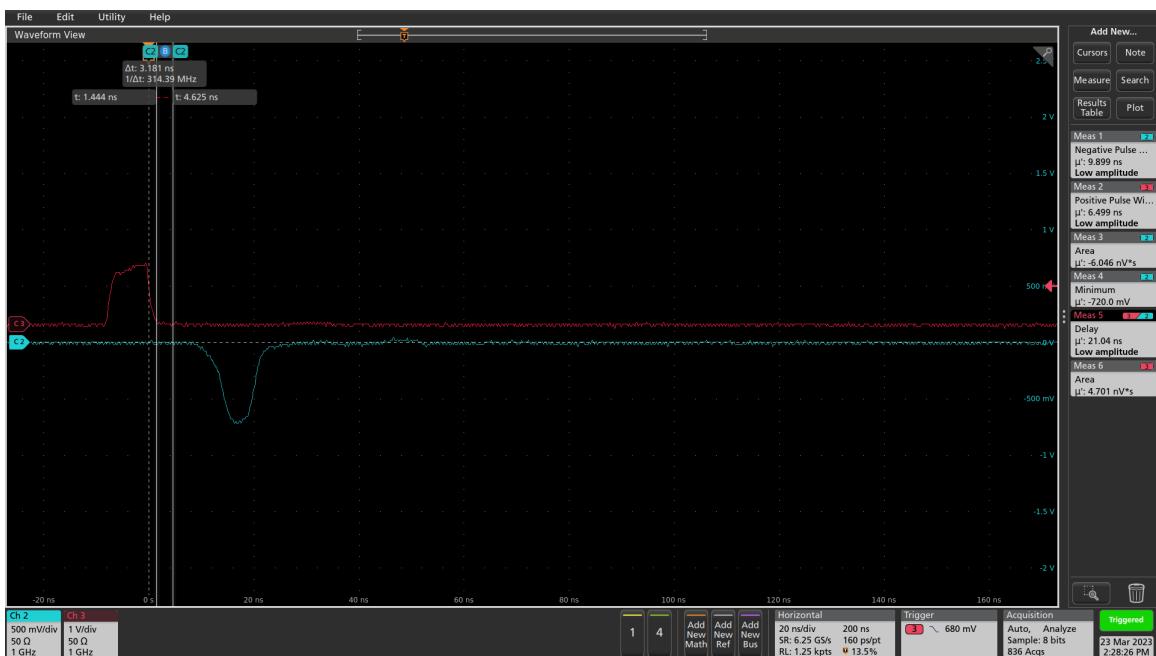


Figure 17: BFR92 Pulse Shape

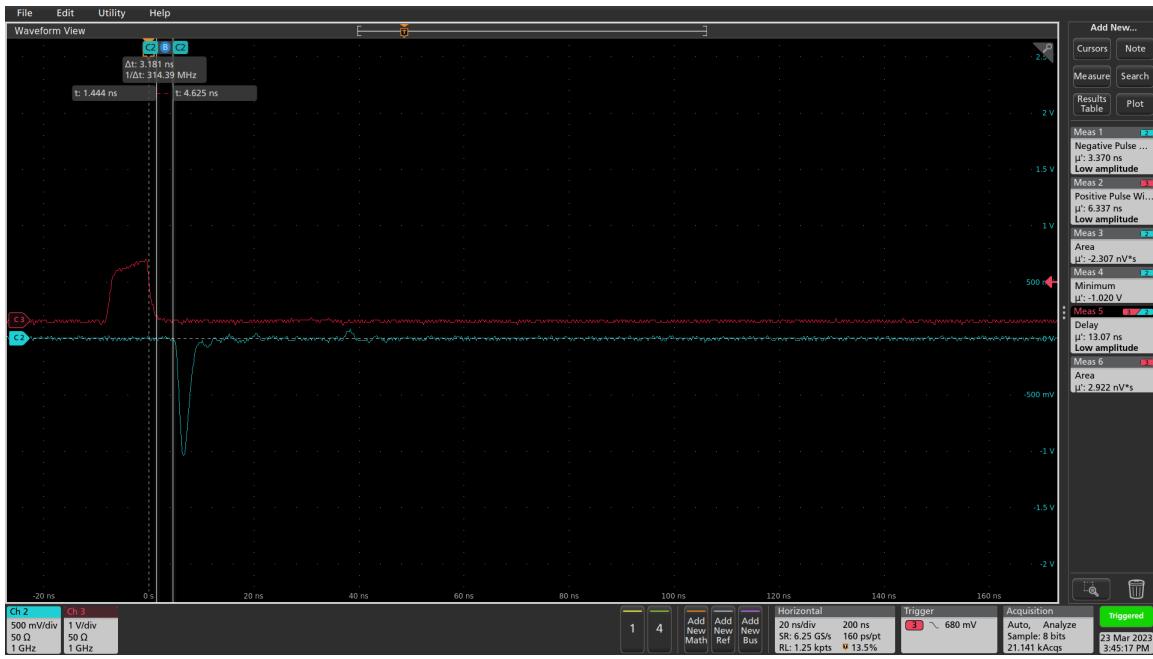


Figure 18: EPC8004 Pulse Shape

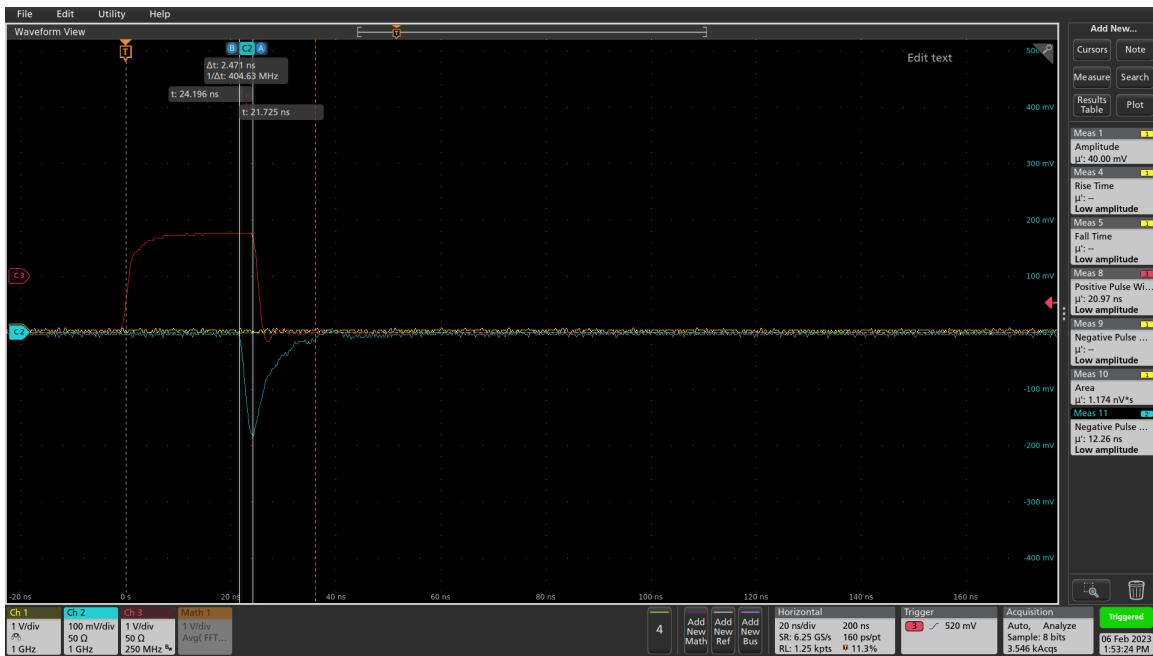


Figure 19: Pulsing Circuit With No Inductor and Resistor

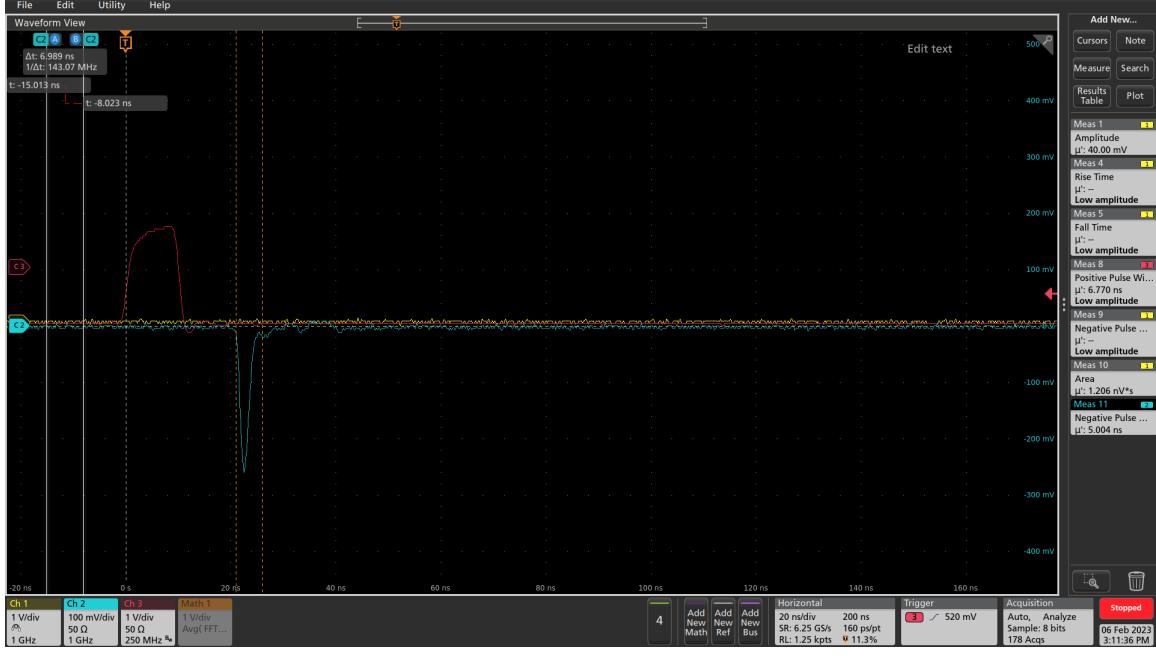


Figure 20: Pulsing Circuit With Inductor and Resistor

313 employing the EPC8004 switch, another utilising the EPC2012 switch, a third using the
 314 same high-speed transistor (BFR92) as implemented in the legacy system, and a fourth vari-
 315 ant incorporating an EPC2012 gate in a through-hole package instead of the standard 0805
 316 surface-mount footprint. Further evaluation was also performed using the latest pulser board
 317 prototype once they had arrived.

318 Following comparative performance evaluations, the configuration using the EPC8004
 319 switch was selected for continued use. While both the EPC8004 and EPC2012 switches
 320 exhibited similar electrical characteristics, the EPC8004 offered superior performance due to
 321 its lower parasitic capacitance, without any additional cost. The pulser board assembly was
 322 housed within a dark box during testing, and a 3D-printed fibre coupler was employed to
 323 facilitate light delivery. The initial focus of the evaluation was on the shape of the generated
 324 optical pulse. During component selection, it was observed that the LED previously sourced
 325 from Mouser (ATS2012UV385 by Kingbright) provided acceptable performance in terms of
 326 electrical characteristics, but the optical output was suboptimal, as it was showing a strange
 327 “double pulsing”, which can be seen in Figure 21. Additionally, this LED was found to be
 328 out of stock and obsolete at the time after testing, precluding further procurement.

Figure 21: Double pulse observed from the Kingbright ATS2012UV385 LED.

329 Subsequently, four ultraviolet LEDs from LC LED were assessed—two emitting at 365 nm
 330 and two at 395 nm—each in both 0805 and 0603 surface-mount packages. Results demon-
 331 strated that the 0805 package LEDs provided significantly better optical coupling efficiency
 332 with the FP400URT optical fibre. Furthermore, the 365 nm variant exhibited superior opti-
 333 cal power output relative to the 395 nm counterparts. Based on these findings, the LC LED
 334 UT-67UV365P [12] 365 nm LED was selected as the most suitable LED for this application.
 335 Tests showed the LED was behaved well, providing an optical pulse of 2.8 ns width, with
 336 3.3 ns elelctrical signal, as shown as Figure 22. The pulse width deviation is 60.218 ps, or
 337 2.12% , and the histogram shows the pulse distribution.

338 **check this** A long torture test took place over the Christmas break as well. The pulser

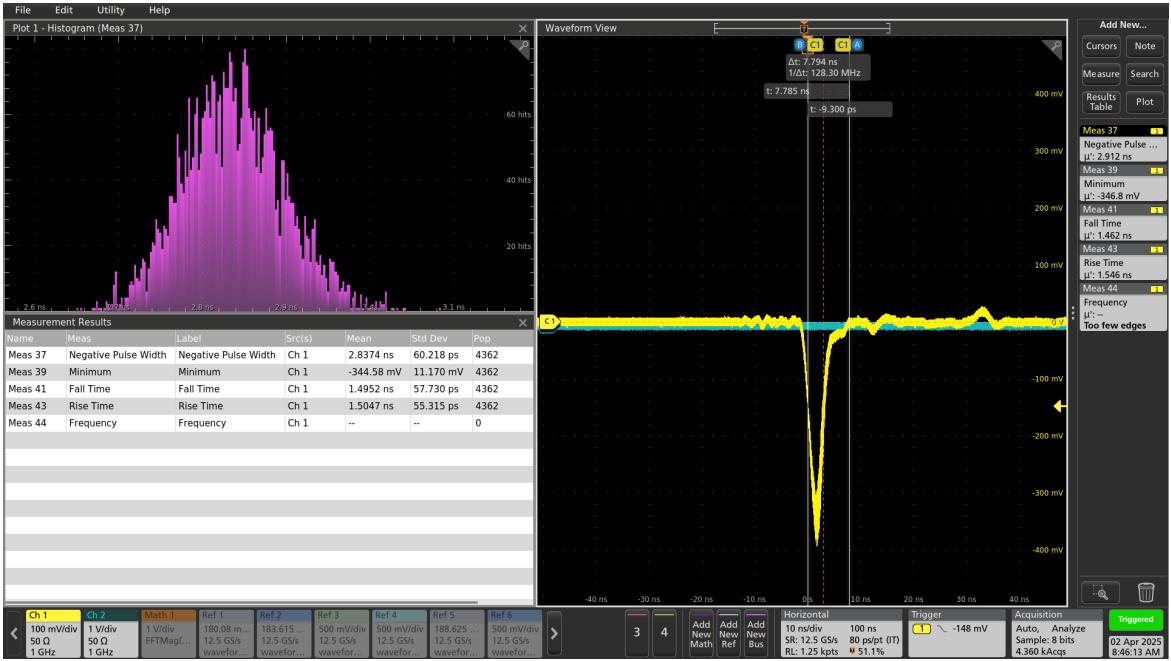


Figure 22: Scope trace and pulse width histogram for a 3.3 ns input signal, through a 1 m FP400URT fibre.

339 system was placed in a small dark box, and a new 365nm LED was soldered onto the
 340 pulser board. The pulse frequency was set to 30,000 Hz, and the pulse width was set to
 341 2.8ns pulse width, which is effectively 6.8ns pulse after 180m of fibre. The system was
 342 running continuously for 13 days, while we took power and air temperature measurement
 343 every 10 seconds. The air temperature was measured at the power meter, using the Thorlab
 344 PM100USB. We are expecting to run the system at around 0.0082 Hz, as autocalib will pulse
 345 a channel at 1 Hz rate and there are 122 active channels. This means that pulsing the LED
 346 at 30 KHz for 13 days is equivalent of 106 849 years of normal running, not including the
 347 1 KHz shorting calibration sessions. While we have not calibrated the temperature gain, we
 348 are estimating a 1.5 percent loss if we compare the same temperature from the beginning of
 349 the experiment to the end.

350 6.4 LVDS to TTL Converter

351 The DS90C402 [13] from Texas Instruments was selected as the LVDS-to-TTL conversion
 352 solution. This device is a dual-channel converter, chosen primarily for its fast switching
 353 characteristics—offering both rise and fall times of approximately 500 ps. It operates at
 354 5 V and provides 5 V TTL output levels, which aligns well with the requirements of the
 355 downstream switching circuitry. The inclusion of two channels is particularly advantageous,
 356 as it enables the generation of sub-nanosecond differential pulses by precisely offsetting the
 357 channels, as described in Switch Selection. Among commercially available devices with
 358 these specifications, the DS90C402 is the fastest and is readily available through multiple
 359 distributors.

360 The associated circuit was implemented in accordance with the manufacturer's recom-
 361 mendations provided in the datasheet. A decoupling capacitor was placed in close proximity
 362 to the power supply pin to minimise voltage ripple. Output traces were routed using polygon
 363 fills to reduce impedance and enhance signal integrity, and a continuous ground plane was
 364 placed beneath the signal layers to improve shielding and minimise electromagnetic interfer-

ence. The schematic for this is given in Figure 23.

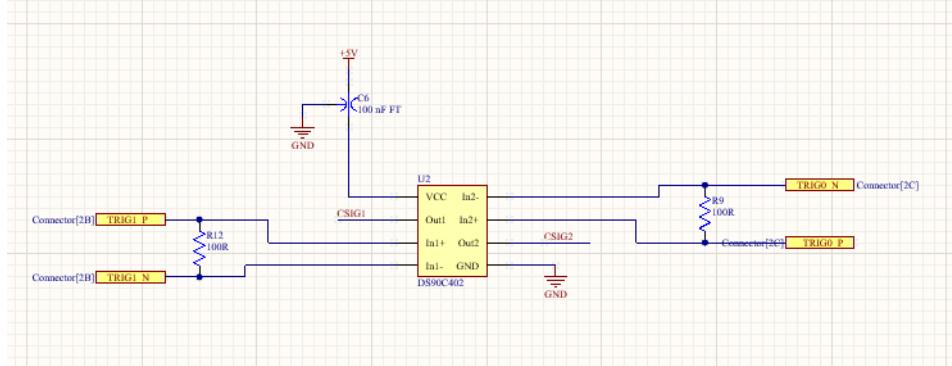


Figure 23: LVDS-TTL Converter Schematic

6.5 Power Supplies

Each pulser board is required to incorporate a variable voltage power supply dedicated to driving the LED, with an adjustable output range from 3 V to 12 V. This supply is used exclusively to modulate the LED’s light output by varying the forward voltage, and consequently the current. The design specification also necessitates that the power supply be remotely controllable—i.e., capable of being switched on or off via a simple logic-level signal.

For this purpose, the LT1963A [14] adjustable low-dropout linear regulator was selected. This regulator has demonstrated reliable performance in previous pulser board iterations and offers a favourable balance of cost-effectiveness and controllability. The implementation includes standard filtering and decoupling, with layout details provided in Figure 24. The schematic provided in Figure 25 is an early version used for prototyping; the adjustable circuit has been simulated and will be tested shortly, and the enable circuit has been tested, modified and simplified. Updated schematics will be provided with v1.0 circuit. There will be overcurrent protection built in to the system as well. A ZXCT1051 (Reference!) is used to monitor the current and if it senses larger than normal current then it send a signal to the FPGA to turn the damaged board off. A surface mounted fuse will be added in line as well to make sure there is a second line of defense as well.

In addition to the variable LED supply, each board requires a stable 5 V supply to power both the DS90C402 LVDS-to-TTL converter and the LMG1020 gate driver. Unlike the LED supply, this rail remains continuously powered. The 5 V supply is provided by an LM2937-5 [15], a fixed-output linear voltage regulator, which has been successfully employed in various high-speed and low-noise applications within the laboratory. The associated circuit schematic and layout and schematic are shown in Figures 26 and 27 respectively.

To meet system-level design constraints, each pulser board is equipped with its own independent 12 V input supply, ensuring that LED output intensity can be individually controlled on a per-board basis. However, the 5 V supply is common across all boards and derived locally on each pulser module. This approach allows for localised filtering and minimal power distribution path lengths, reducing the risk of noise coupling and voltage drop considerations that are particularly critical in high-speed circuit applications.

Power is supplied to each board via the Eurocard backplane. The 12 V input from the Eurocard simultaneously feeds both the variable (LED) and fixed (logic) power regulators on the pulser board. The LED enable function is controlled via a 5 V logic signal originating from the Eurocard’s GPIO interface. Additionally, a DAC output from the Eurocard provides

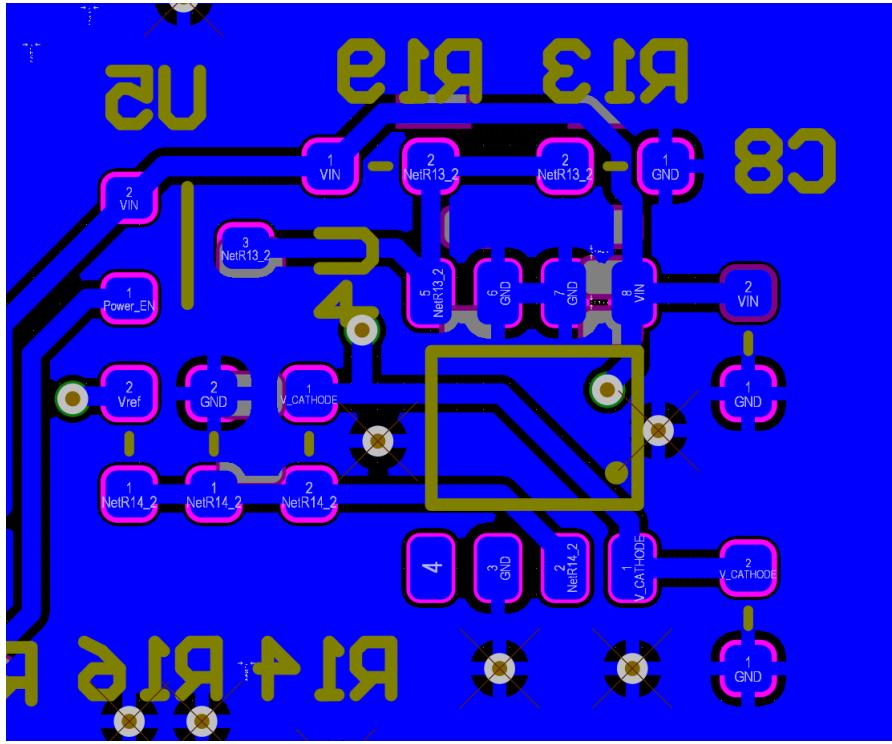


Figure 24: LT1963 Layout

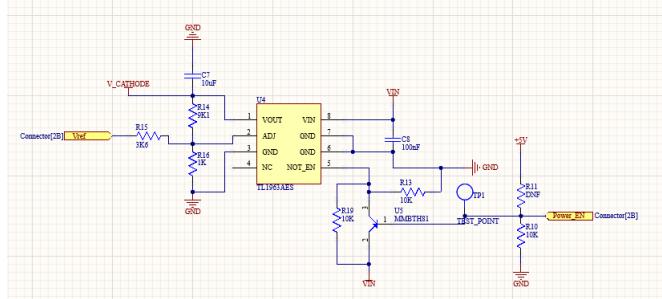


Figure 25: 12V Circuit Schematics

400 a voltage control signal to the adjustment pin of the LT1963A regulator on each pulser board,
401 thereby allowing precise, programmable control of light intensity.

402 6.6 Connector

403 The previous board connector was deemed too bulky and expensive for the larger number
404 of channels needed in this system, leading to the process of finding a more suitable alterna-
405 tive. Following an evaluation of commercially available options, the Phoenix Contact female
406 connector 1331962 [16] was selected. This connector offers several advantageous specifi-
407 cations: it is rated for 500 V, features a low contact resistance of $40\text{ m}\Omega$, supports a maximum
408 current of 0.5 A, and is capable of signal transmission up to 20 Gbit s^{-1} . In addition, it is
409 cost-effective, priced at approximately £0.50 per unit, with wide availability ensuring ease
410 of procurement. Multiple height variants are available within the same series, facilitating
411 flexible mechanical integration within the Eurocard crate system. The compact footprint of
412 the connector allows for a reduced PCB form factor. Electrically, the high-frequency perfor-
413 mance supports reliable LVDS signal transmission. Additionally, the compact footprint of

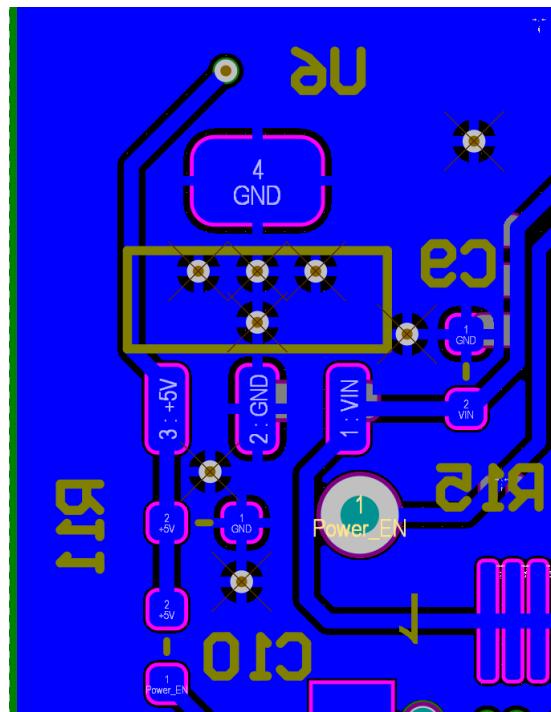


Figure 26: LM2937-5 Layout

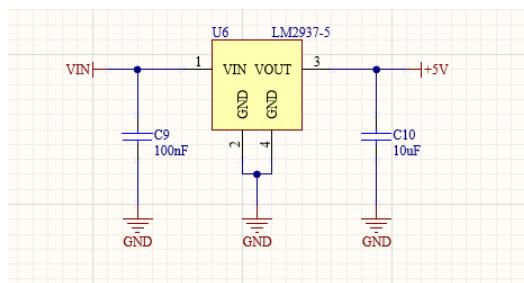


Figure 27: 5V circuit schematics

414 the connector is well-suited to space-constrained PCB layouts.

415 An illustration showing the connector and corresponding circuit layout is provided in
416 Figure 28.

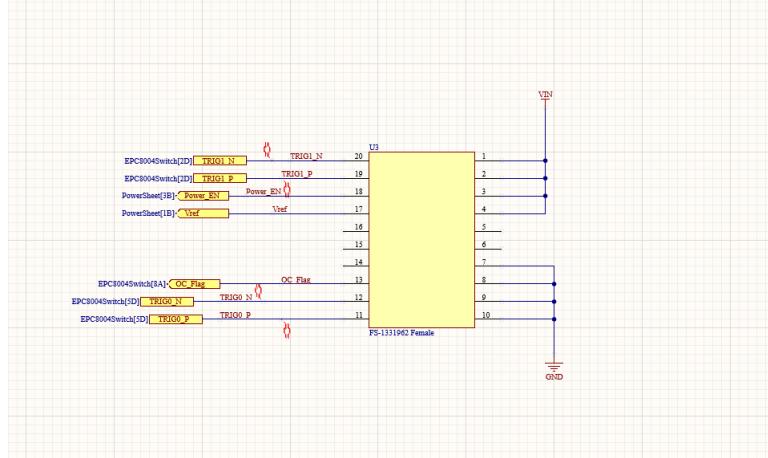


Figure 28: Connector Schematics

417 6.7 Fibre Coupler

418 During the prototyping phase, improvements were made to the PCB layout to better ac-
419 commodate a fibre coupler. As a result, the current design includes provisions for precise
420 mechanical mounting and alignment. Specifically, two mounting holes for M2 screws have
421 been incorporated, enabling the 3D-printed coupler to be firmly secured to the board (see
422 Figure 29). In addition, two dowel holes have been added to guide the coupler into posi-
423 tion, ensuring accurate alignment over the LED. Given the tolerances associated with PCB
424 fabrication and 3D printing, an alignment accuracy of approximately 100 μm is expected.



Figure 29: Old Fibre Coupler Design

425 To optimise the electrical path, capacitors have been repositioned as close as possible to
426 the LEDs. This minimises parasitic inductance and resistance, while enabling a centralised
427 layout of larger components. The resulting configuration creates a compact chamber housing
428 both the LEDs and associated capacitors.

429 An earlier design for the fibre coupler, which assumed uniform fibre lengths for all chan-
430 nels, has since been abandoned. The current approach for the LED light injection system

431 adopts five different fibre lengths, necessitating individual light attenuation for each channel.
 432 This attenuation will be implemented within the coupler itself, allowing the LED output to
 433 remain within the electronically controlled dynamic range.

434 The proposed design is modular, consisting of three components: a base section mounted
 435 to the pulser PCB, a top section into which the fibres will be epoxied, and an intermediate
 436 attenuator element. The latter will serve to space the fibre from the LED and thereby adjust
 437 the optical coupling efficiency to achieve the required attenuation. While an initial prototype
 438 will be developed in the near term for functional testing, the full design and validation of the
 439 fibre coupler will be undertaken later, once the required fibre lengths are fixed and unlikely
 440 to change. Should the project timeline require faster iteration, this can be pursued.

441 The fibre coupler will be fabricated via stereolithography (SLA) using a black resin to
 442 minimise light transmission through the material. Additional light-tight testing will be
 443 conducted, and black paint may be applied if further sealing is required. Furthermore, laser-
 444 cut rubber gaskets will be introduced at interface points to ensure optimal optical isolation
 445 and mechanical sealing.

446 6.8 Photon Yield Tests

447 tests on maximising photon yield and available dynamic range should be fully described here

448 6.9 Production

449 Production will be carried out using PCB Train as they are local and competitively priced,
 450 and known to produce boards of good quality. Estimated cost is £12.27 per board, which
 451 equates to £1,496.94 for 122 units or £1,840.5 for 150 units, and production is £4073.48 for
 452 122 units for 15 days lead time, or £3985 for 150 units at 25 days lead time. The full cost
 453 breakdown is shown in Figure 30

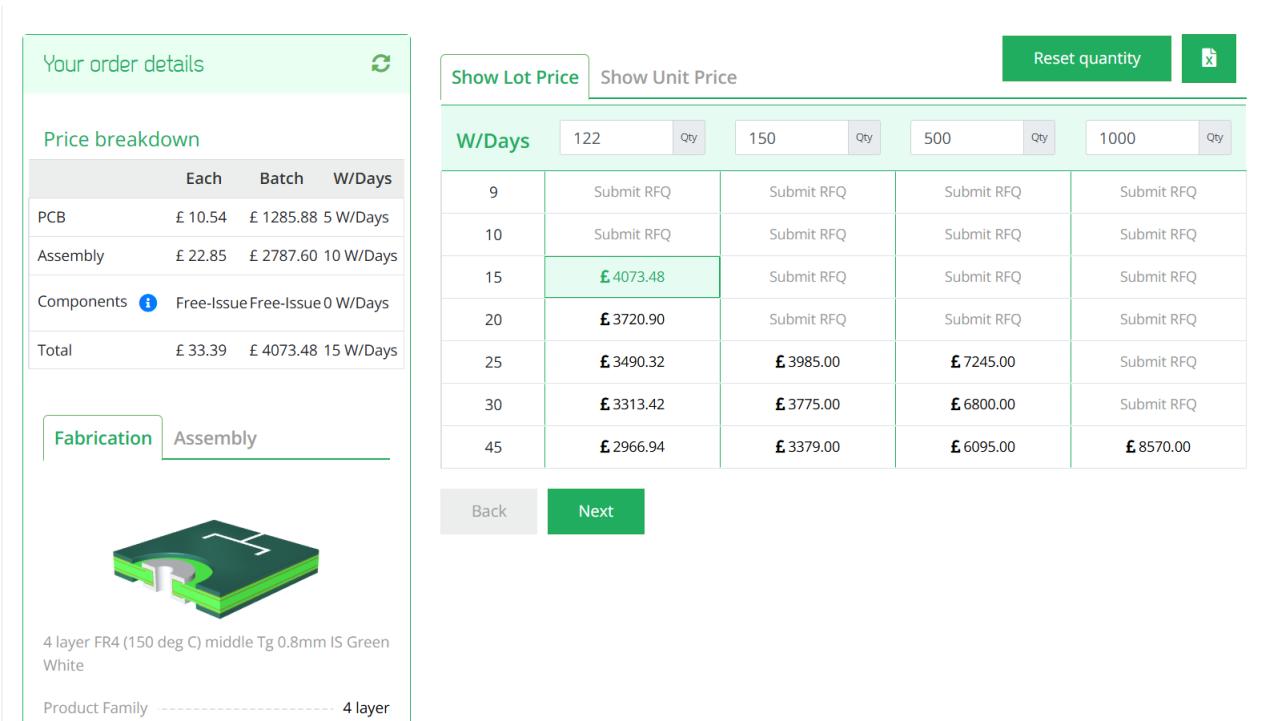


Figure 30: PCBTrain PCB production and assembly costs

454 **6.10 Changes Expected from v0.9 to v1.0**

455 **6.10.1 LED and Switching Circuit**

456 There will be minimal changes to the LED and switching circuit. Changes will be made to
457 the position of the switching devices, placing them slightly closer to each other to reduce
458 transmission line length. The LED will likely remain as the LC LED UT-67UV365P 365nm
459 0805 LED, but further LED tests will be performed. This takes a short amount of time, and
460 may lead to discovering better LEDs in the future which would be easy to swap in due to
461 standardised footprints.

462 **6.10.2 LVDS-to-TTL converter**

463 No changes are expected to this circuit.

464 **6.10.3 Power supplies**

465 Reverse voltage bias will be removed as no difference between normal and reverse bias was
466 observed photon output. The overcurrent protection and power enable circuit will be re-
467 worked.

468 **6.10.4 Connector**

469 No changes are expected to this.

470 **6.10.5 Fibre coupler**

471 A brand new fibre coupler will be designed due to the recent requirement changes regarding
472 the different fibre lengths.

473 **7 Server Rack and Cooling**

474 To house the electronics for the LI systems, two 42U server racks with 800 mm depth will
475 be used. The front of the server rack will be used for electrical connections and displays,
476 and the reverse/internal will be used only for fibre routing. The server racks will include
477 Uninterruptible Power Supplies (UPS) for safe power delivery and for power processing, to
478 avoid issues with potential instabilities in the main power supply. Each rack will include an
479 air conditioning unit to have a controlled temperature and remove humidity from the air,
480 as the relative humidity in the air is expected to be above 70%. Although specific tests on
481 running the LED electronics in humid conditions have not been carried out, it is known that
482 the optical switches for the laser calibration system requires lower humidity levels. In order
483 to simplify things and remove the potential of humidity issues with the LED electronics,
484 both server racks will be air conditioned. These systems are widely available and will be
485 chosen closer to installation.

486 **8 LED Monitoring**

487 To monitor the light output from the LEDs before attenuation by fibres and convolution
488 with water parameters, PMTs will be placed near to the LED sources. This is a similar
489 design to what is currently used in the Super-K UKLI system. Each LED connector will
490 feature a second fibre to take light to a series of PMTs, which are expected to be Hamamatsu
491 H10721-210. Due to the 8 mm diameter of the PMT window, up to 16 fibres can be attached,

492 meaning one PMT can monitor up to 16 LED boards at once. Each PMT will be powered
493 by a unique low cost power supply developed for the SK UKLI system. These will be housed
494 in a small 2–3 U server rack. The signals from the PMTs will then go to the dedicated HK
495 electronics channels that are set up for monitoring.

496 9 Control System for LEDs

497 The LEDs are driven by a differential LVDS signal originating from the FPGA. The FPGA
498 in use is the Genesys 2 [17] development board, which operates a pulsing VHDL module
499 clocked at 300 MHz. Pulses are generated on the rising edge of this clock, and toggling the
500 output (i.e., asserting and then deasserting the trigger) requires a minimum of two clock
501 cycles. Consequently, the shortest achievable pulse duration in this configuration is 3.3 ns.

502 One of the main limitations of this setup is the coarse time resolution: pulse durations
503 are effectively constrained to integer multiples of 3.3 ns. To achieve a broader and more
504 finely resolved spectrum of optical injection into the detector, improved temporal precision
505 is necessary. This is accomplished using the Xilinx `IODELAY` primitive, originally designed for
506 high-speed interface timing alignment. The `IODELAY` module permits fine-tuning of signal
507 timing to account for PCB trace mismatches, and in this application, it is repurposed to
508 introduce controlled delays between pulses.

509 To generate shorter pulses, two identical signals are created, one of which is delayed
510 using `IODELAY`. These signals are then combined using a logical AND operation, producing
511 a narrower pulse. Since the `IODELAY` module requires one clock cycle to process the input,
512 both signals—regardless of whether they are delayed—must pass through an `IODELAY` stage
513 to ensure temporal synchronisation.

514 Conversely, to produce longer pulses, the same methodology is applied, but the signals are
515 combined using a logical OR gate instead. This approach extends the pulse width beyond the
516 base clock resolution, enabling pulse durations ranging from approximately 1.5 ns to 4.5 ns
517 in 49 discrete steps. The lower bound is determined by the threshold of the LVDS-to-TTL
518 converter, which does not respond to pulses shorter than approximately 1.5 ns .

519 For channels using the longest optical fibres, this extended range is sufficient, given
520 the intrinsic dispersion in the fibre optics of around 5 ns. However, shorter fibres require
521 additional pulse shaping. To this end, an additional mechanism is implemented using a `for`
522 loop structure within the FPGA logic. This allows the pulse to persist for multiple clock
523 cycles, effectively producing longer pulses by repetition. However, due to FPGA architecture
524 constraints, each iteration of the loop consumes a clock cycle, necessitating careful timing
525 control. For instance, to produce a 6.6 ns pulse, the loop must be configured for two cycles,
526 accounting for the loop overhead.

527 Further refinement is under investigation through the daisy-chaining of multiple `IODELAY`
528 modules. This would enable sub-nanosecond granularity by introducing additional intermediate
529 delay steps. While promising, this technique requires further validation and testing.

530 The pulse control data structure is currently under development. There are two types
531 of pulse description considered. In the first option, the software interface would require two
532 parameters per channel: a *coarse* step and a *fine* step, reflecting the approach used in the SK
533 system. The other option would be just a single variable and then simple logic turning that
534 variable into the *coarse* and *fine* step that the internal logic requires. Two hardware modules
535 are planned: one for generating the single shortest possible pulse (to minimise latency), and
536 another for multi-cycle pulses using programmable duration. A selection logic will assess the
537 input and route it to the appropriate module based on the desired pulse characteristics.

538 Each LED channel will be controlled independently, allowing for unique pulse configurations
539 across channels. The global trigger will be derived from the system clock, and each

540 channel will pulse in a predefined sequence while triggered from the global trigger. This
541 architecture also supports simultaneous pulsing of multiple channels. Should asynchronous
542 behaviour be required, additional per-channel delay logic can be implemented. Given the
543 five distinct fibre lengths used in the system, each channel group will also include a config-
544 urable delay offset to compensate for propagation time differences. These group delays will
545 be calibrated and fixed, with the option of fine-tuning individual channels post-deployment
546 if necessary.

547 The repetition rate can be adjusted as well, including a single pulse, using external
548 trigger, from 0.001Hz through 1 KHz to multiple megahertz if needed, but the system was
549 only tested up to 30 KHz, as that was a high enough rate to illuminate the power monitor's
550 sensor.

551 The FPGA programming remains in active development. Inter-crate communication
552 protocols and synchronisation are currently under integration and testing.

553 10 Crate Electronics

554 10.1 Overview

555 The system specification calls for control of up to 122 LED channels, significantly exceeding
556 the channel counts used in current systems such as Super-Kamiokande or LUX-ZEPLIN,
557 which the previous generation of pulser boards are used for. To manage this complexity, the
558 design prioritises ease of use, maintainability, and straightforward deployment, particularly
559 given that the server racks will accommodate hundreds of optical fibres.

560 To achieve this, a system concept originally developed by ATLAS collaborators (specifi-
561 cally by Ashley Greenal) has been adapted. The original design utilises a Genesys 2 FPGA
562 integrated into a half-width Verotec KM6-2 [18] Eurocard-compatible crate for testing pur-
563 poses. This concept has been extended to a full 19-inch rack width, enabling the integration
564 of up to 36 pulser boards within a single crate.

565 Each FPGA is capable of interfacing with up to 38 pulser boards, thereby maximising
566 the utilisation of available LVDS differential pairs, with an additional pair reserved for the
567 laser trigger signal. This configuration ensures full use of the Genesys 2's I/O capacity while
568 maintaining flexibility for future expansion.

569 The system architecture consists of three primary components: the Blade (Section 10.2),
570 Backplane (Section 10.3) and Eurocard (Section 10.4). This modular approach ensures
571 scalability and facilitates debugging, replacement, and upgrades. It also provides a robust
572 foundation for managing high channel counts while maintaining signal integrity and synchro-
573 nisation across the system.

574 We will have 4 crates in the system, which allows us to have up to 144 pulser boards
575 while the system only requires 122 to run. This means we will have 22 spare boards, which
576 will allow us to have 5 sets of 4 boards, a set of four for each fibre length, that can be used for
577 hot swapping. A local technician can remove the signal and monitor fibre from the broken
578 pulser board, attach it to a spare board and reconfigure the software to use the spare board
579 for running, all with an expert guidance. Next time an expert is on site they can do further
580 maintenance or repair if needed.

581 10.2 Blade

582 The Blade is a simple, eight layer board, that has a SEAM-40-06.5-L-10-2-A-K-TR [19]
583 connector which is a direct fit for the Genesys 2's FMC connector. It features a PCIE 16X
584 connector at the edge for connectivity to the Backplane. The PCIE was selected by Ashley

585 Greenal as it is a well documented standard connector and there are a large amount of
586 connectors available that can be bought easily. While PCIE connectors are being used, the
587 PCIE standards for communication are not. This is a very dense PCB with all the differential
588 tracks on it, so buried vias and multiple layers will be used. See Figure 31 for a work in
589 progress version.

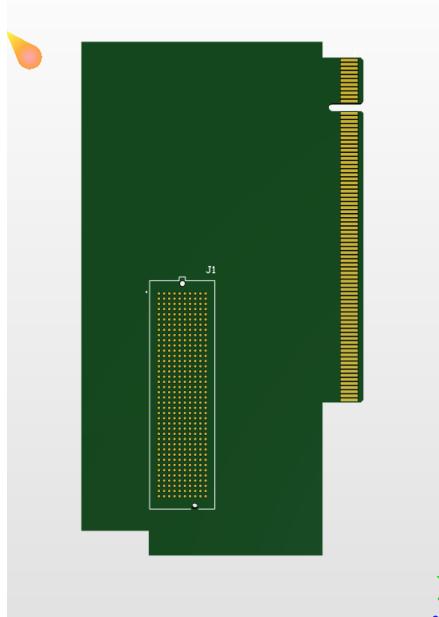


Figure 31: Blade Work in Progress

590 10.3 Backplane

591 The Backplane serves two primary functions: the distribution of differential signals from the
592 Blade to the Eurocards, and the reception and distribution of power throughout the crate
593 system. It accepts external power inputs of 12 V and ± 5 V, and includes a basic regulation
594 circuit to stabilise these supply voltages for downstream use.

595 Given the mechanical constraints and routing complexity, the Backplane is implemented
596 as a four-layer PCB with impedance-controlled traces to ensure signal integrity across all
597 differential pairs. It features a single PCIe x16 connector to interface with the Blade, and
598 three PCIe x8 connectors to interface with the Eurocards.

599 The Eurocards are positioned at slots 2, 8, and 64 within the crate. This arrangement
600 creates two symmetrical chambers with 48 units spacing between cards, ensuring adequate
601 space to accommodate the minimum long-term bend radius of the FP400URT optical fibres.
602 This layout balances mechanical reliability with signal routing efficiency and supports long-
603 term maintainability of the system. See Figure 32 for a work in progress version.

604 10.4 Eurocard

605 The Eurocard format defines the physical and electrical standard for the crate system, hence
606 the naming convention. Each Eurocard is equipped with a PCIe x8 connector for interfacing
607 with the Backplane, and is designed to host up to 18 pulser boards—nine mounted on each
608 face. Pulser boards connect via FS-1332120 Male[20] connectors, and each socket includes
609 two mounting holes for mechanical standoffs.

610 The board layout on each side consists of two staggered rows: five sockets in the back
611 row and four in the front. The two faces are laterally offset by approximately 10 mm to

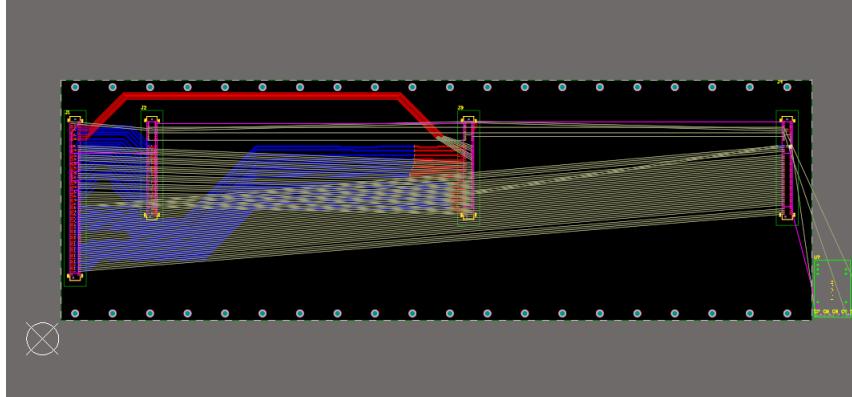


Figure 32: Backplane Work in Progress

612 prevent interference or fibre clashes when the system is fully populated and enclosed within
 613 the crate chamber. This offset ensures smooth fibre routing and accommodates the bend
 614 radius requirements of FP400URT fibres.

615 Power distribution within each Eurocard is handled by a THD 12-1212 [21] 12 V DC-DC
 616 regulator. This regulator provides local power isolation for the pulser boards and includes
 617 a control pin connected to a PCA9698 [22] 40-pin GPIO expander. This allows for system-
 618 level control, enabling or disabling all pulser boards on a card—an essential feature during
 619 power-up, especially when the FPGA may inadvertently drive all differential outputs high
 620 during reprogramming.

621 The GPIO expander is responsible for enabling the local 12 V regulator and for selectively
 622 powering individual pulser boards. This facilitates fault isolation and power savings in
 623 channels that are inactive or disconnected. Additional GPIO pins are assigned to monitor
 624 output voltage levels via the overcurrent sensing circuitry.

625 To provide per-channel LED power control, an AD5673 [23] DAC is included. It out-
 626 puts analogue control voltages to the onboard adjustable regulators on each pulser board,
 627 allowing for independent LED drive voltage per channel. Both the GPIO and DAC devices
 628 communicate with the system over the I²C protocol.

629 For laser synchronisation, the Eurocard includes a differential-to-NIM conversion stage.
 630 This consists of an LVDS-to-TTL converter identical to that used on the pulser boards,
 631 followed by a TTL-to-NIM converter. This ensures compatibility with legacy NIM-based
 632 timing systems used in external laser triggering. See Figure 33 for a work in progress version.

633 11 Conclusions

634 Write this

635 References

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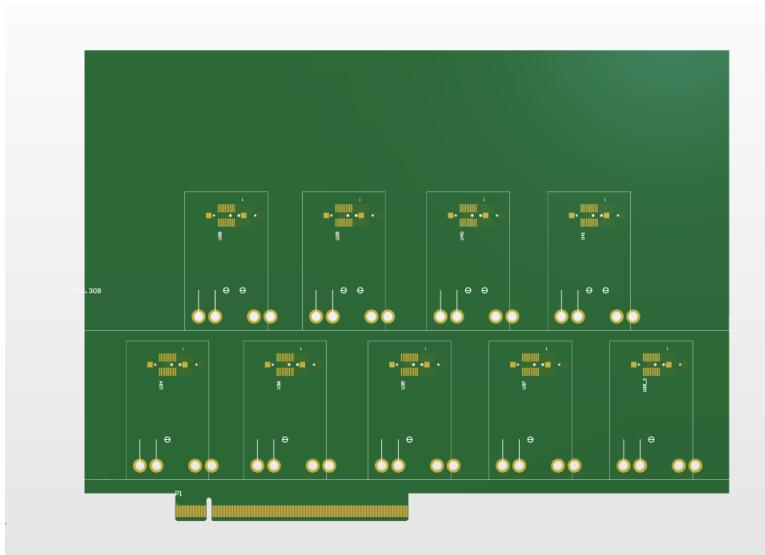


Figure 33: Eurocard Work in Progress

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