

1 Hyper-Kamiokande Outer Detector Light Injector System
2 Technical Note

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50 **0 Version history**

- 51 • v0.99 - First release by Balint circulated to Liverpool group for internal review
52 • v1 - [Sam]: Ported over to github for continued development, as we hit compilation
53 time on overleaf. Initial pass through to fix wording and rewrite some sections. Also
54 integrating Warwick TN on OD diffuser, and Liz's work on the OD saturation studies.
55 Some reordering of structure to make it flow better.

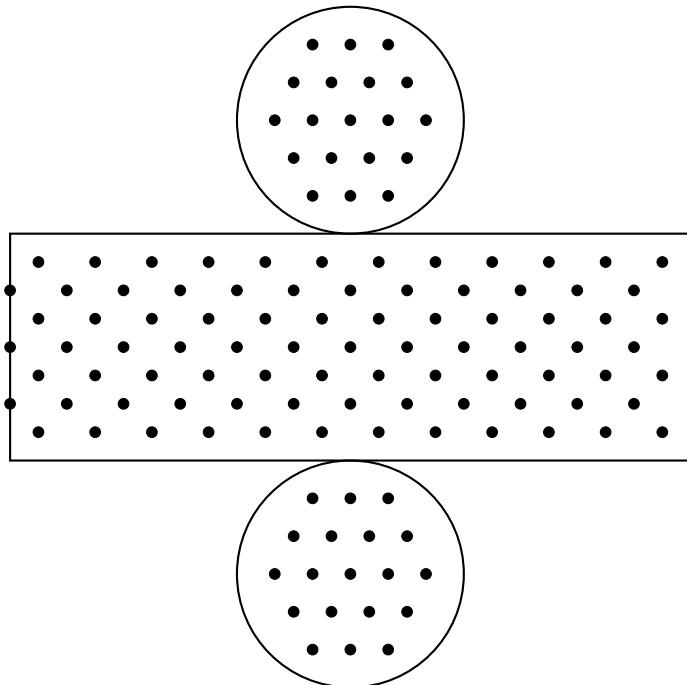
56 **1 Introduction**

57 Hyper-Kamiokande is a large scale water Cherenkov detector with two main sections, an
58 inner detector (ID) and an outer detector (OD). The OD volume of Hyper-K is a one meter
59 wide annular ring on the circumference of the detector. This space is designed to tag charged
60 particles, such as cosmic ray muons or particles from interactions in the surrounding rock,
61 entering the detector. In addition, the OD volume will be used as working space for instal-
62 lation activities. Once complete, it will be optically separated from the ID volume, and will
63 be instrumented with 3,600 outward facing 8 cm photomultipliers tubes (PMTs). These will
64 each surrounded by wavelength shifting (WLS) plates to increase photocoverage.

65 In order to achieve the precision measurements Hyper-K aims to make, precise calibration
66 of the detector is required. For the OD, a light injection (LI) system will be employed,
67 allowing for known quantities of light to be injected into the detector region. This will
68 consist of 122 diffusers and 12 collimators. The diffuser system, which is described in this
69 technical note, will be used to measure gain and timing properties of the OD PMTs, and
70 will be powered by dedicated pulsed LED sources. The 12 OD collimators are identical to
71 those uses in the ID system, and will be integrated into the ID laser system. Full details on
72 that system, along with investigations of the fibre optics that will be employed for the OD
73 system, can be found in [1].

74 **2 Light Injection System Overview and Requirements**

75 The OD diffuser system will be composed of 122 bare diffusers, installed on the outward facing
76 side of the PMT support structure. The proposed layout for this is shown in Figure 1, though
77 in actuality there will be minor differences from this regular arrangement due to restrictions
from other systems. These are arranged such that they illuminate roughly an equal amount



78
79 Figure 1: Injector location map for OD diffuser positions. Locations are approximate and
dependent on PMT/WLS plate locations.

of OD PMTs. One of the primary goals of the system is to inject enough light to saturate the

80 OD PMTs. This goal drives a large part of the photon output optimisation, and Monte Carlo
81 (MC) studies to evaluate the amount of photons required to do this are shown in Section 3.
82 The diffuser design is discussed in Section 4. These will each be illuminated by individual
83 LED pulser boards with 365 nm LEDs. This will require at least 122 dedicated LED pulsers,
84 and spares should be readily available for hot-swapping should a board encounter issues. Full
85 details of the pulser board design are given in Section 6. The pulser boards will be powered
86 and controlled by commercially-available Field Programmable Grid Array (FPGA) boards.
87 The control system architecture for these consists of three primary components:

- 88 • **Blade:** Interfaces directly with the FPGA, distributing all differential signals into the
89 crate system.
- 90 • **Backplane:** Routes differential signals to the pulser boards and provides the primary
91 power distribution, accepting 12 V and ± 5 V inputs.
- 92 • **Eurocards:** Host the pulser boards, receive power and differential signals from the
93 backplane, and incorporate the necessary circuitry for laser triggering.

94 Further details on the control system and individual electronics crate components are given
95 in Sections 9 and 10 respectively.

96 Light will be transported between the pulsers and diffusers by a series of fibre optic
97 cables; following the investigations in [1] the Thorlabs FP400URT [2] is targeted for this.
98 Due to production limitations, it is not possible to keep all fibre path lengths the same.
99 Instead there will be five different lengths: 50 m, 80 m, 106 m, 124 m and 168 m. The
100 light output after signal attenuation and dispersion in these fibres should be as consistent
101 as possible, which will require fine tuning given the different amounts of attenuation and
102 dispersion which pulses will experience based on fibre length.

103 The initial design requirements for the system are to produce pulse widths out of the
104 diffuser of no more than 10 ns, with a photon yield in the range 1–15 million photons per
105 pulse (ppp). The 10 ns limit is driven by the timing resolution of the WLS plates. The
106 wavelength of light used is also partially dictated by the WLS plates, which will not activate
107 for light above 400 nm. The photon yield target here is more of a goal than a requirement,
108 and saturation studies were performed using numbers motivated by system performance.
109 These are summarised in Section 3.

110 The below paragraph should split up. The first half has been rewritten into the above
111 paragraph, the second should be fleshed out for the photon yield test section.

112 Pulse width should ideally be between 1–10 ns and the photon count from 1–15 million
113 photons, but higher limits are preferable. The lower limits are not possible to achieve, as the
114 fibre dispersion will create a minimum pulse width, which is 4.5 ns at 180 metres, and if we
115 try to achieve large light output it will compromise our lower light output, so we can only
116 achieve around 100,000 photons per pulse at minimum. While these compromises are not
117 ideal, the fibre selection limits our capabilities on hitting the required theoretical targets.

118 3 OD PMT Saturation Study

119 The light injection system in the OD will use collimated and diffuse light injection to calibrate
120 the PMTs and to measure the optical properties (scattering and attenuation) of water, as
121 well as any degradation in Tyvek reflectivity over the course of operation.

122 Diffuse light sources will be used for in-situ calibration of the PMT charge response.
123 Light will be injected at very low levels to measure the single-photoelectron charge response,
124 and the requirement to achieve single-photoelectron coverage across all PMTs was used to
125 determine the number of light injectors required for the light injection calibration system, as

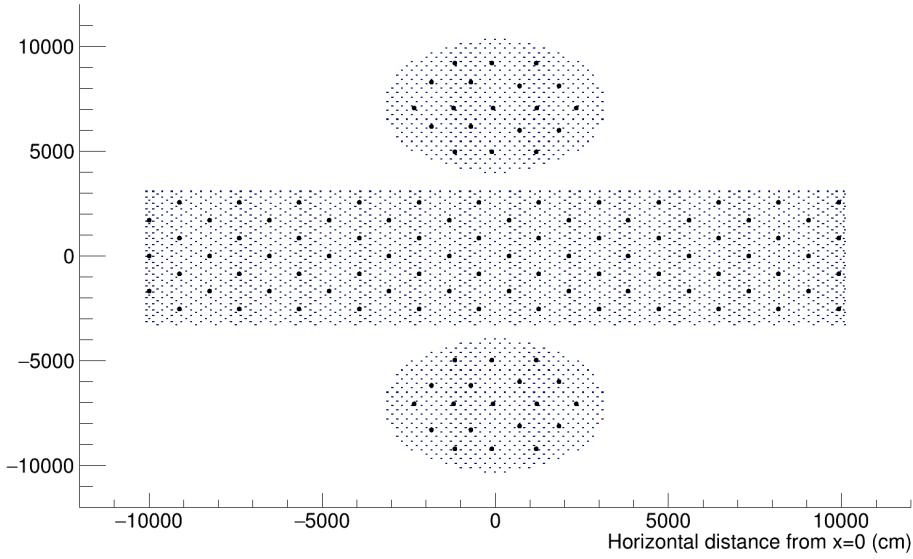


Figure 2: Positions of the OD PMTs and diffuser positions used in the calibration simulations. Note that the positions of PMTs in the top and bottom rows of the barrel have changed in the design, and as such the results presented in this tech note reflect these changes. This differs from the most recent version of WCSim (1.12.26) [4] that has been used as a basis for the simulation, and the changes are reflected in pull request #525.

126 reported in the Outer Detector Technical Report [3]. In order to calibrate the PMTs across
 127 their entire range, the light injection system must also be capable of illuminating PMTs to
 128 saturation, to understand the change in their response as they approach saturation.

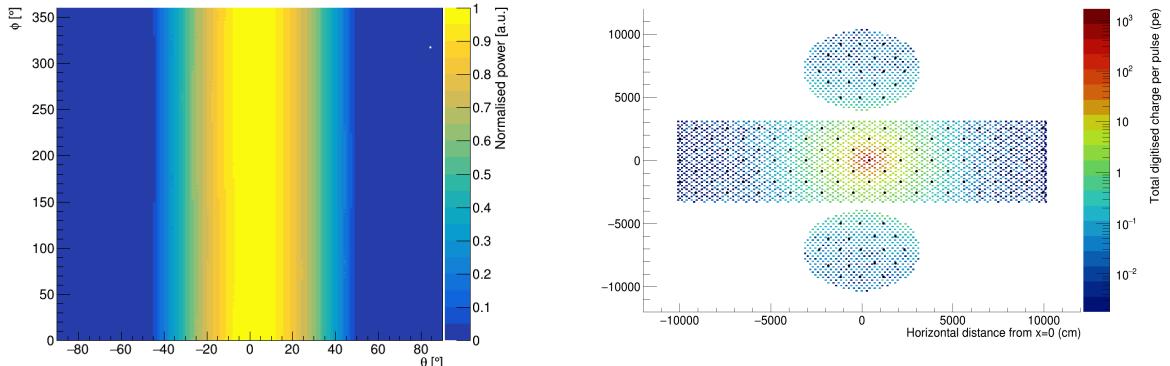
129 This section describes the use of diffuse light injection to evaluate the suitability of light
 130 sources for in-situ measurements of the PMT saturation response. Section 3.1 describes the
 131 diffuser simulation, Section 3.2 gives details of the OD geometry and diffuser parameters
 132 used, and Sections 3.3 and 3.4 describe the scope, analysis and results of the saturation
 133 study.

134 3.1 Light Injector Simulation

135 The planned light injection calibration system will consist of 122 sources, as determined by
 136 maximising the single-photoelectron coverage of all of the OD PMTs [3]. The division of
 137 sources between the endcaps and barrels, and their positions in terms of the overall geometry,
 138 has been altered since [3], following an update of the design and geometry in the simulation.
 139 Figure 2 shows the updated diffuse light injector (LI) with respect to OD PMT positions.
 140 The diffusers have been positioned as close to equidistant as possible from the surrounding
 141 PMTs, next to a strut in an empty cell.

142 A new LI generator has been written within the framework of WCSim [4]. This allows
 143 the user to define the characteristics of the LI within a data file input to the simulation. The
 144 following characteristics can be defined:

- 145 • Global position within the detector geometry,
- 146 • Direction of the LI axis,
- 147 • Wavelength of the optical photons



(a) ID diffuser profile measured in water, used for the diffuser simulations described in this technical report. A measured profile for each diffuser will be stored in the database for OD calibration.

(b) Charge in photoelectrons on each PMT produced when the profile in (a) is used to simulate optical photons from a diffuser pointing outwards in the barrel OD. The size of the PMT + WLS plates has been increased only in the plot for improved visualisation.

Figure 3: Diffuser profile measured in water, and the resulting charge map from this profile.

- 148 • Pulse width
- 149 • Photons per pulse
- 150 • LI profile in the form of arrays of θ , ϕ and measured light intensity, where θ is the
151 angle made with the axis of the LI and ϕ is the rotation around the axis.

152 The LI profile opening angle and intensity can reflect either a flat angular distribution
153 of photons within the desired angular range of the light injector (-opening angle, +opening
154 angle), or can be drawn from the measured profile for that injector, in which case the LI
155 generator accurately models the variation across the profile, and in particular the drop-off
156 in the frequency of photons towards the edge of the LI profile. For each pulse, the generator
157 samples the specified number of photons per pulse, each with an energy calculated from the
158 wavelength set in a database currently stored within WCSim, and a time sampled from a
159 Gaussian distribution around the mean, with a variance equal to the pulse width specified
160 in the database. Each photon is also assigned a global direction, which is sampled with a
161 distribution corresponding to the LI profile.

162 The profile of each diffuser will be measured and stored in the database as a function
163 of the diffuser identifier number in the final simulation. For the purposes of the diffuser
164 simulations presented in this tech note, a single profile taken from the measurement of a
165 diffuser profile in water has been used. This diffuser profile corresponds to an opening angle
166 of around 40°. Since the OD diffuser profiles have not yet been measured in water, an ID
167 diffuser profile has been used to approximate a realistic OD diffuser profile. Although the
168 design of the OD diffusers has been modified from the ID diffuser design in order to increase
169 the diffuser efficiency, the design has been shown to maintain the desired profile and as such
170 the ID diffuser profile is expected to be a reasonable approximation. The diffuser profile
171 used, and the resulting charge map from a diffuser in the barrel is shown in Figure 3.

172 3.2 Diffuser and OD Parameters

173 The characteristics of diffusers simulated in the saturation study are summarised in Table I.
174 The number of photons per pulse used in the simulation was based on measurements made

175 from the LED pulser setup, using a chain of fibre optic cables equating to 181 m in length.
 176 The simulations described here use a maximum photon yield from the fibre optic chain of
 177 11×10^6 photons per pulse. This was modified to account for an assumed diffuser efficiency
 178 of 50%. As such, the simulated number of photons per pulse is 5.5×10^6 .

Parameter	Assumed value
Photons per pulse	11×10^6
Wavelength	365 nm
Pulse width	10 ns
Diffuser efficiency	50%

Table I: The LI configuration used in the diffuser simulations for the saturation study presented in Section 3.3.

179 The OD geometry parameters that have been used in the simulations for the saturation
 180 study are shown in Table II.

Parameter	Assumed value
PMT radius	8 cm
PMT dark rate	0.4 kHz
OD lateral water depth	1 m
OD height water depth	2 m
OD dead space	60 cm
Tyvek sheet thickness	1 mm
WLS plate thickness	6 mm
WLS plate length	30 cm

Table II: The OD configuration used for the saturation study presented in Section 3.3 using WCSim version 1.12.26.

181 3.3 Saturation Study

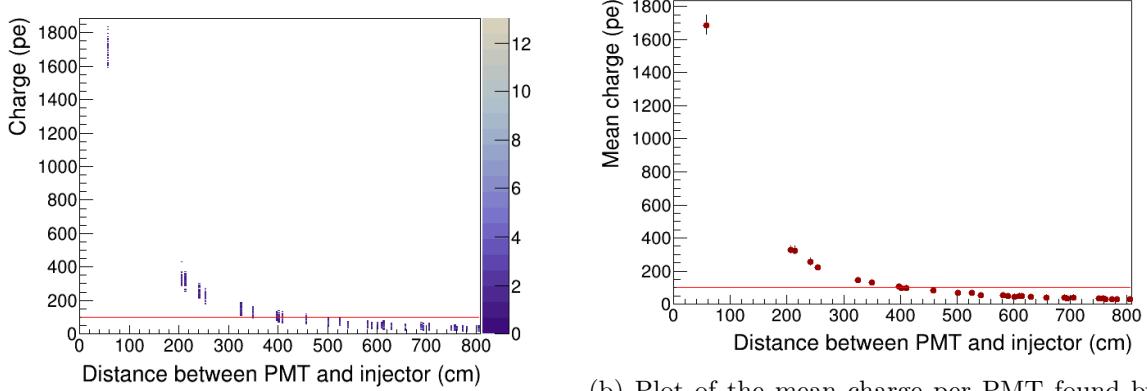
182 The limit of the PMT range is governed by the electronics response, which is expected to
 183 fully saturate at around 100 photoelectrons (pe) in a 16 ns time window. The simulation
 184 of the PMT charge response in WCSim does not currently handle the saturation, but it is
 185 expected that the linearity of the charge response will break down between 80 pe and 100 pe.
 186 Saturation measurements aim to measure the PMTs over the full range of this breakdown
 187 in linearity. The saturation level for the purposes of this study has been taken to be 100 pe
 188 in 16 ns, but the analysis has been designed to take into account the need to measure across
 189 the entirety of this range.

190 The saturation of OD PMTs has been evaluated in the top endcap, barrel and bottom
 191 endcap. The diffuser simulations are intensive, requiring millions of tracked photons to
 192 simulate a single flash. As such, only two diffusers in each of the top endcap, barrel and
 193 bottom endcap have been simulated for this current study.

194 Two values have been used as figures of merit to determine the PMT saturation coverage:

- 195 • Mean saturation distance - the distance from the nearest diffuser at which the mean
 196 charge per PMT is greater than saturation level.
- 197 • Saturation limit - the greatest distance from the nearest diffuser at which the charge
 198 on any PMT reaches the saturation level.

199 For each configuration, the charge per PMT was plotted as a function of the distance
 200 from the nearest diffuser, to give the saturation limit (Figure 4a). The mean saturation
 201 distance was then found by taking the mean of the same plot (Figure 4b). The plot showing
 202 the saturation limit is particularly useful in understanding the range of distances over which
 203 it is possible to see the expected range of breakdown of linearity.



(a) Plot of the charge per PMT as a function of the distance from the nearest diffuser. The saturation limit is the greatest distance at which saturation is achieved i.e. 5.0 m in this case.

(b) Plot of the mean charge per PMT found by taking the mean of the left-hand plot. The mean saturation distance is the greatest distance at which the mean charge per PMT is greater than the saturation level i.e. 4.0 m.

Figure 4: Sample plots showing the mean saturation distance and saturation limit used as figures of merit for the saturation study. The red, horizontal lines mark the assumed saturation level of 100 pe.

204 Since only six diffuser locations have been simulated, the percentage of PMTs within
 205 the mean saturation distance and saturation limit is calculated assuming symmetry both of
 206 the detector and of the diffuser positions with respect to the PMTs. However, for practical
 207 reasons, the diffusers have to be positioned off-centre in the empty cells between PMTs, next
 208 to the struts on the PMT support structure. As such, a full simulation of all diffusers should
 209 be performed in future, once the OD geometry and LI specifications have been finalised, for
 210 an accurate evaluation of the percentage saturation across the whole detector.

211 3.4 Results

212 The mean saturation distance and saturation limit were evaluated for two OD diffuser loca-
 213 tions in each of the top endcap, barrel and bottom endcap. These are shown in Table III,
 214 along with the percentage of PMTs within the mean saturation distance and saturation limit.
 215 Table IV shows the mean charge at the calculated saturation distance and the mean charge
 216 at the saturation limit at the six diffuser positions.

217 Figure 5 shows the PMT charge map for the Barrel 1 diffuser, with the saturation distance
 218 and saturation limits marked around the barrel PMTs.

219 Due to the differing geometry the mean saturation distance in the barrel (4.0 m) is
 220 slightly higher than in the endcaps (e.g. 3.6 m), and the percentage of PMTs within the
 221 mean saturation distance in the barrel is higher at 31% than in the endcaps (22-27%).
 222 Similarly, the percentage of PMTs within the saturation limit in the barrel is higher than in
 223 the endcaps, with the exception of the bottom endcap 2 diffuser, with 66% of PMTs within
 224 the saturation limit of 6.1 m. It should be noted that changes to the OD geometry, including
 225 the addition of PMTs in the endcaps, are possible, and have not been taken into account in
 226 this simulation.

OD location	Mean saturation distance	% PMTs within saturation distance	Saturation limit	% PMTs within saturation limit
Barrel 1	4.0 m	31%	5.0 m	50%
Barrel 2	4.0 m	31%	5.0 m	50%
Top endcap 1	3.7 m	27%	3.9 m	30%
Top endcap 2	3.6 m	24%	4.3 m	37%
Bottom endcap 1	3.6 m	24%	4.3 m	37%
Bottom endcap 2	3.5 m	22%	6.1 m	66%

Table III: Results for PMT saturation using the diffuser configuration detailed in Table I.

OD location	Diffuser position	Mean charge (pe) at saturation distance	Mean charge (pe) at saturation limit $\pm 2\sigma$.
Barrel 1	(395.65,-3281.50,8.75 cm)	108	68 ± 12
Barrel 2	(3281.50,395.65,1705.55 cm)	105	67 ± 11
Top endcap 1	(-70.7,-97.3,3350.82 cm)	106	96 ± 14
Top endcap 2	(-707,-968.2,3350.82 cm)	108	77 ± 13
Bottom endcap 1	(-707,-968.2,-3350.82 cm)	108	77 ± 14
Bottom endcap 2	(707,-1157.8,-3350.82 cm)	114	42 ± 11

Table IV: Results for PMT saturation using the diffuser configuration detailed in Table I.

227 The diffuser position with respect to the surrounding PMTs has an observable effect
 228 on the saturation levels achieved. Where the diffuser positions with respect to surrounding
 229 PMTs are equivalent, as in the case of the two barrel diffusers, as well as the Bottom Endcap 1
 230 and Top Endcap 2 diffusers, saturation levels are largely the same. However, the positions of
 231 the Top Endcap 1 and Bottom Endcap 2 diffuser each differ from all other diffusers simulated,
 232 resulting in different saturation distances and saturation limits. Again, a full simulation of
 233 all diffuser positions should be carried out to fully evaluate achievable saturation across the
 234 whole detector, once all parameters and geometries have been finalised.

235 4 Diffuser Design

236 4.1 ID Diffuser Hemisphere Design

237 4.1.1 Inner Detector Diffuser Design

238 The diffusers used to scatter input laser light in the inner detector volume are 2.54 cm
 239 half-spheres fabricated from PTFE. This is used as it

- 240 • is unaffected by immersion in water
- 241 • acts as a excellent diffuser
- 242 • is a good transmitter of UV light
- 243 • is easy to machine and clean

244 A mechanical drawing of the inner detector diffuser hemispheres is shown in Figure 6

245 4.1.2 Diffuser Profile Measurement System

246 A scanning system was built to measure the output characteristics of diffuser hemispheres.
 247 Enclosed in a dark box, the diffuser is mounted onto two rotary stages which gives the freedom

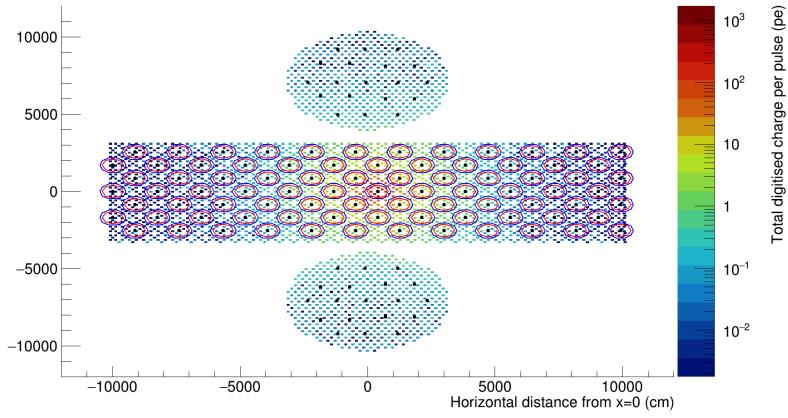


Figure 5: Charge in pe on each PMT as a result of illumination with the Barrel 1 diffuser. The mean saturation distance and saturation limit around each PMT in the barrel are marked in red (smaller circles) and blue (larger circles) respectively.

248 to rotate the diffuser around the nominal axis linking the diffuser with the photosensor. This
249 scanner only takes scans in an air medium, and the setup is illustrated in Figure 7.

250 A laser powered from a wall plug is used to illuminate the diffuser with light at a wave-
251 length of 450 nm. It is triggered by a function generator with 1000 triggers per burst at a
252 frequency of 2 kHz. The open beam is directed via a mirror, a circulator, and a lens to the
253 fibre launch stage, and then via an optical fibre towards the diffuser. The diffuser enclosure is
254 fixed with three screws on the double-rotation stage. Measurements of bare diffuser profiles,
255 i.e. without enclosure, are conducted with the bare fibre end positioned in the centre of the
256 rotation stage using a 3D printed frame. The bare fibre end is kept in place due to friction
257 on the connection point with the diffuser hemisphere. A photograph of the rotation stage
258 with a bare diffuser hemisphere is shown in Figure 8.

259 A PMT measures the diffuser spectrum at a fixed position, with 62 cm distance to the
260 diffuser enclosure and a 3 mm pinhole aperture, restricting the solid angle viewed by the PMT
261 to $2 \cdot 10^{-5}$ sr. For comparison, a single 50 cm PMT in the HK far detector receives light from
262 a point source at the other side of the tank over a solid angle of approximately $2.2 \cdot 10^{-4}$ sr.
263 The PMT signal is digitised at a sampling rate of 2500 MHz over 1000 cycles, allowing to
264 resolve the shape of each single signal waveform. The light yield at each coordinate is then
265 obtained as the average waveform area across all digitised signals.

266 The diffuser profile measurement system is discussed in detail in [5].

267 4.1.3 Diffuser Power Measurement System

268 In addition to the profile measurement functionality, the integrated power output from the
269 diffuser was measured using an integrating sphere from Ophir. This sphere provides an
270 unbiased measurement of the total light output power of any light source, regardless of the
271 shape of the emission profile. A bespoke diffuser holder suitable for connection to one of the
272 integrating sphere ports was 3D-printed, as was a holder for the optical fibre from the laser
273 source.

274 A bare PTFE hemisphere was mounted into this holder and connected into the integrating
275 sphere port. The bare end is inserted into the connection point in the same manner as for
276 a bare profile scan. Tape was used to prevent light leaking out of the back
277 of the hemisphere during the measurement, which also helped to keep the fibre in place.
278 The hemisphere was then illuminated with light from the same laser, this time running on

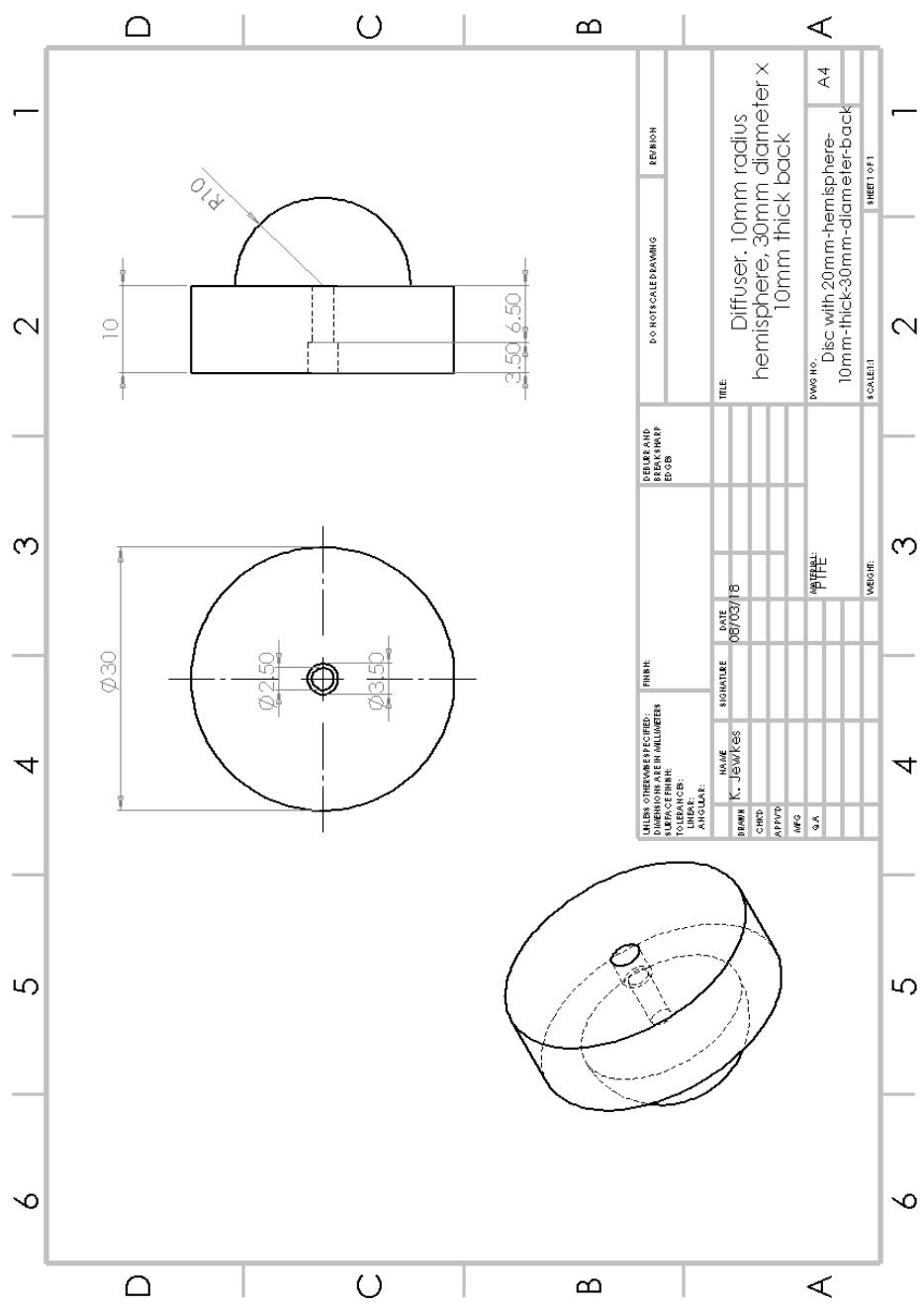


Figure 6: Bare Diffuser Mechanical Drawing

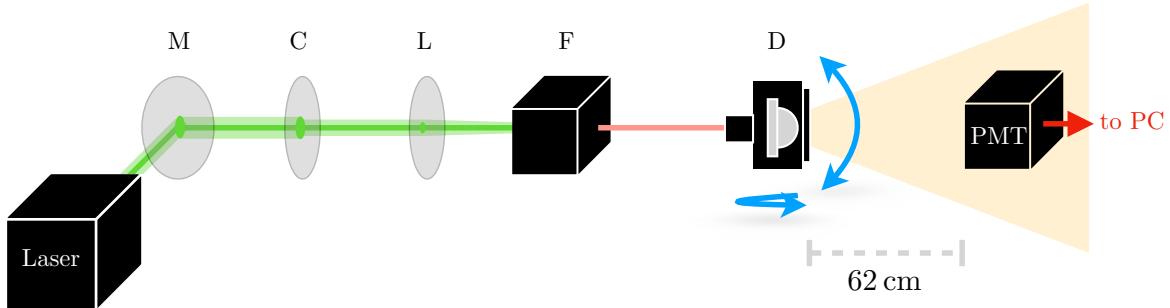


Figure 7: Setup for diffuser scans: light from the laser is directed via a mirror (M), a circulator (C), and a lens (L) to the fibre launch stage (F). From there, the light goes via an optical fibre to the diffuser (D) on the rotation stage.

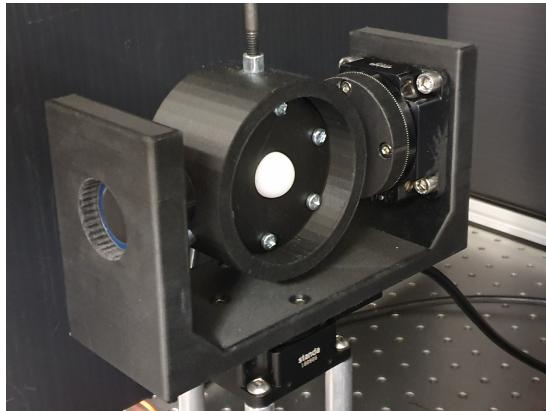


Figure 8: Rotation stage with bare diffuser hemisphere mounted using a 3D-printed frame.

279 a continuous rather than burst setting. On the continuous setting light is supplied in a
 280 sinusoidal manner at a frequency of 1 kHz. Power measurements were taken once per second
 281 for a period of ten seconds to account for small fluctuations in laser intensity, the mean of
 282 which served as the final power measurement for that hemisphere.

283 In order to calculate a power ratio, a measurement of power for the bare fibre also needed
 284 to be obtained. This was done in a similar manner to a power measurement for a hemisphere,
 285 using the same laser and data acquisition settings. To make the comparison between fibre and
 286 hemisphere measurement as accurate as possible, a special hemisphere was created with the
 287 fibre connection point extended into a hole that runs through the length of the hemisphere.
 288 The bare fibre can then be inserted all the way through until it pokes out of the front,
 289 allowing a power measurement for the bare fibre to be taken with the conditions inside the
 290 integrating sphere as close as possible to hemisphere measurements. The ratio of hemisphere
 291 power to fibre power can then be taken to determine the amount of light lost.

292 A table of systematics for the power ratio measurement is shown in Table V. Rotation
 293 refers to changing the orientation at which the diffuser is placed into the holder, and dif-
 294 fuser re-insertion refers to removing the diffuser from the holder and replacing it. Fibre
 295 re-insertions refers to disconnecting and re-connecting the fibre into the diffuser, while bare
 296 fibre refers to dis- and re-connecting the fibre when taking bare fibre measurements. This
 297 results in a total systematic of 5.3% for a diffuser measurement and 1.8% for a fibre mea-
 298 surement, and therefore an uncertainty of 5.6% in a power ratio measurement.

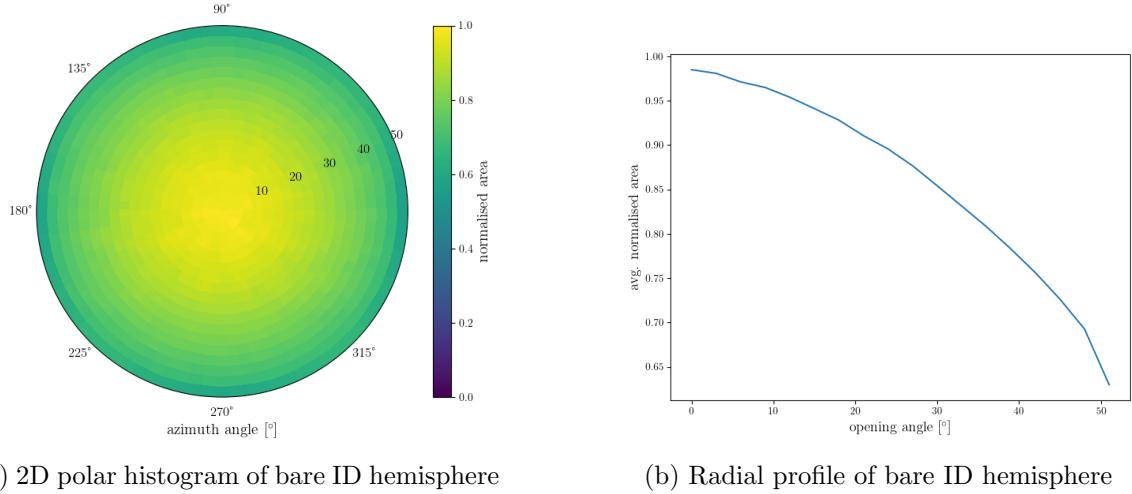


Figure 9: Profile scan of a standard bare ID diffuser hemisphere

Systematic	Std. dev. (%)
Rotation	1.4
Diffuser re-insertion	1.0
Fibre re-insertion	5.0
Bare fibre re-insertion	1.8

Table V: Integrating sphere systematics for the power ratio measurement.

299 4.2 OD Diffuser Design

300 The original intention was to use the same diffuser hemisphere design for the OD diffusers
 301 as will be used for the ID diffusers. However, the standard diffuser emits less than 20% of
 302 the power delivered by an optical fibre. As there are a number of interfaces in the optical
 303 pathway between the light source and the diffuser, and as the light source for the OD will
 304 be LEDs, this was considered too low to be able to effectively saturate PMTs in the OD
 305 space, which is one of the primary design requirements of the system. Neither the number of
 306 interfaces in the optical chain, nor the light source can be changed easily, but it is possible
 307 that an alternate design of the diffuser hemisphere could yield more light.

308 Light is lost to two mechanisms in the standard diffuser; absorption by the PTFE and



Figure 10: A prototype of the OD diffuser with a 2 mm top hat.

309 backscattering. Both loss mechanisms would be minimised if there were less PTFE in the
 310 light path. The design for the OD diffuser section was modified to be the shape of a top
 311 hat, as shown in Figure 10. The optimal depth was studied by taking profile and power
 312 ratio measurements using the same diffuser, but at smaller and smaller depths; after each
 313 measurement was completed, 2.0 mm was cut from the top-hat, and the measurements were
 314 re-taken. This procedure was repeated until the top-hat was 2.0 mm high.

Top-hat depth (mm)	Power ratio (%)
10.0	19.2
8.0	32.4
6.0	31.5
4.0	42.1
2.0	55.2

Table VI: Power ratio measurements for each depth of the top-hat

315 Results of the power ratio measurements are shown in Table VI. As expected, power ratio
 316 increases with decreasing top-hat depth, making the optimum depth 2.0 mm. The profile as
 317 shown in Figure 11 confirms that the shape of the profile is still suitable.

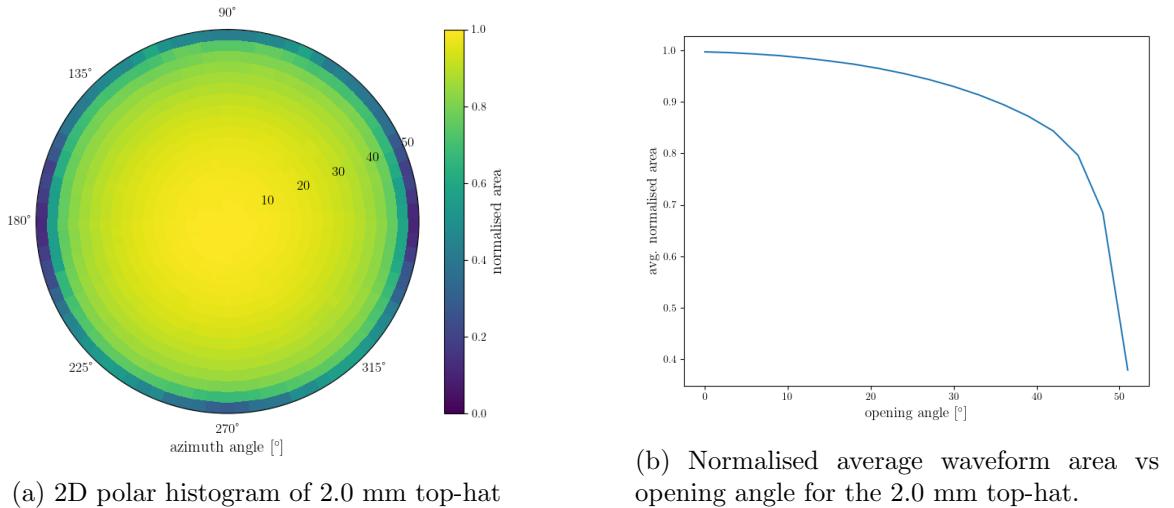


Figure 11: Profile scan of the 2.0 mm top-hat

318 Based on these studies, we propose to change the OD diffuser design from a hemisphere
 319 to a top-hat with a 2.0 mm height above the base. The diffuser will still be fabricated from
 320 PTFE, but this new design (i) emits more light at higher emission angles (ii) doubles the
 321 amount of light that is emitted for a given LED power setting and (iii) is significantly easier
 322 to fabricate in bulk.

323 5 OD Diffuser Mounting System and Installation

324 The OD space will be illuminated by a total of 122 OD diffusers, 19 on each of the top and
 325 bottom caps, and 84 in the barrel. The barrel diffusers are distributed in 7 vertical layers
 326 each consisting of 12 OD diffusers. Due to the numbers and cost, the mounting system must
 327 be relatively small, easy to fabricate and easy to install. Installation will be carried out by
 328 workers on the gondola in the OD space after the Tyvek has been installed and as the fibres
 329 are being installed. The gondola worker will install the fibre in the OD diffuser, and fix the



Figure 12: (left) Front view of the prototype of the OD diffuser mount and (right) rear view of the prototype of the OD diffuser mount.

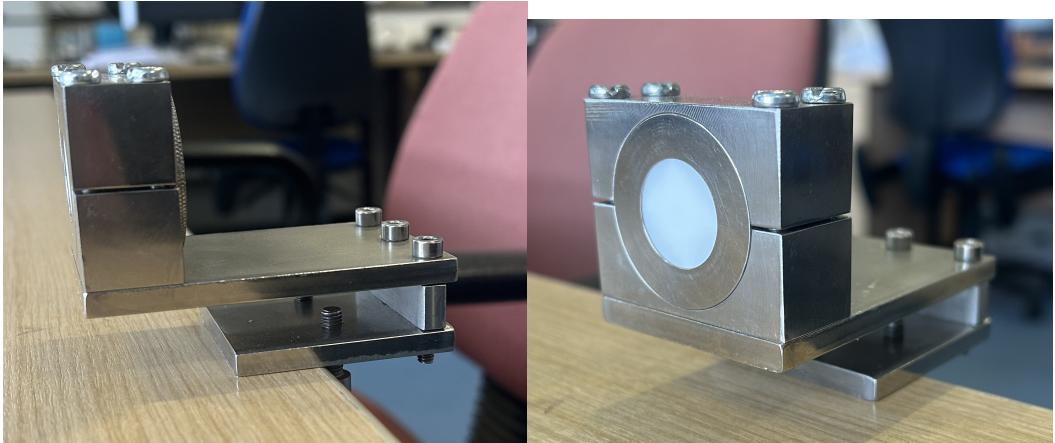


Figure 13: (left) Side view of the prototype holder and (right) front view of the prototype holder.

330 mount to the HK frame, oriented into the OD space. Since this is being done on the gondola,
331 the mount needs to be small, easy to store, and straightforward to install.

332 Drawings for the OD diffuser prototype mount can be seen in Figure 12 and pictures
333 of the prototype can be seen in Figure 13. The mount is made from stainless steel and is
334 designed to hook over a horizontal frame bar, and screw in from the bottom. The PTFE
335 mount is approximately 5 cm on a side. The fibre will be installed from the back and is held
336 in place by a T-shaped component that is screwed down by the gondola worker. An image of
337 the prototype housing installed on the PMT support structure mockup next to a mechanical
338 OD PMT and WLS plate is given in Figure 14.

339 6 Pulser Board

340 6.1 Pulser Board Overview

341 The pulser board was designed to be a more efficient and compact version compared to
342 Super-Kamiokande UK Light Injection system, improving on efficiency, functionality, and
343 light output. The pulser board is a rather simple board designed for low cost production.
344 This section explains each circuit, component selection and design decision. Minor changes
345 are expected from the current design, mostly centred on removing prototyping circuitry.
346 More details on the expected changes are given in Section 6.10.



Figure 14: OD diffuser housing installed at the RAL mockup frame, next to an OD PMT and WLS plate.

347 6.2 Physical dimensions and construction

348 The dimensions of the Printed Circuit Board (PCB) were selected to be as compact as practicable, while still providing sufficient area for the secure mounting of a fibre coupler and for
 349 the components. The final board size is 50 mm × 30 mm. This configuration permits electrically noisy components, such as switching power supplies and the Low Voltage Differential
 350 Signal to Transistor Transistor Logic (LVDS-to-TTL) converter to be positioned at a maximum
 351 distance from the switching circuitry, thereby minimising potential electromagnetic
 352 interference.
 353

354 Although it is technically feasible to further reduce the board size, preliminary design
 355 studies and practical build indicated no substantial benefit in doing so. The board density
 356 cannot be significantly increased inside the crate due to FPGA LVDS count and Eurocard
 357 dimension, and cost analyses revealed negligible differences associated with a smaller PCB
 358 footprint. Furthermore, the chosen dimensions provide an adequate area for the fibre coupler
 359 and the necessary mounting holes to affix the pulser board onto the Eurocard, thereby
 360 ensuring reliable optical alignment and mechanical stability. The PCB is fabricated as a four-
 361 layer FR4 [6] board with a thickness of 0.8 mm, in accordance with the standard construction
 362 offered by PCB Train/Newbury Electronics¹, see Figure 15. Refer to Figure 16 for the 3D
 363 model of the pulser board. The Top Layer and Inner Top Layer are shown in Figure 17, and
 364 the Inner Bottom Layer and Bottom Layer are likewise illustrated in Figure 18. A combined
 365 view of all PCB layers is provided in Figure 19.

¹These are trading names of the same manufacturer.

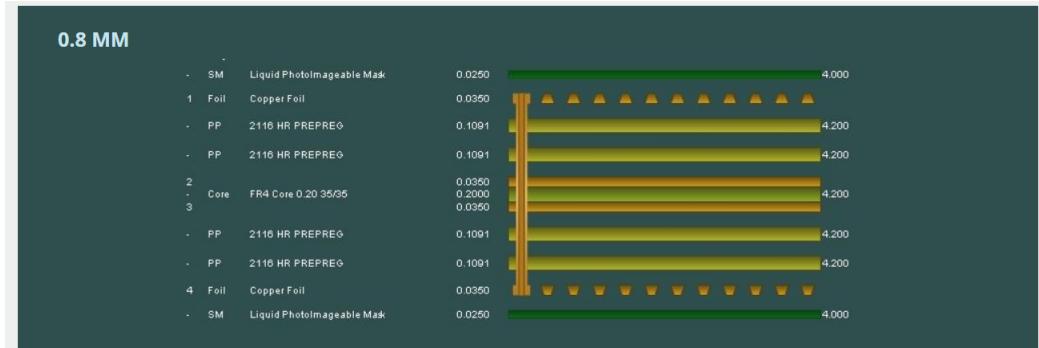


Figure 15: PCB Train's 4 Layer 0.8mm Layer Stack

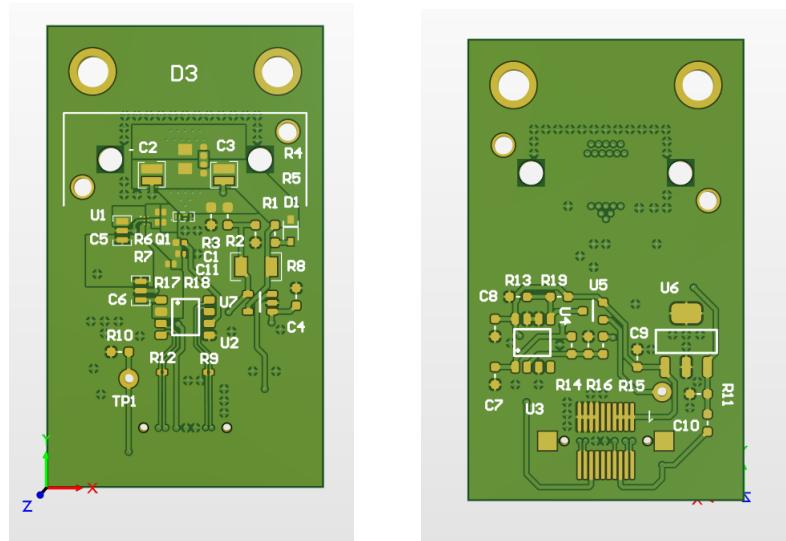


Figure 16: Pulser Board's 3D view Top and Bottom

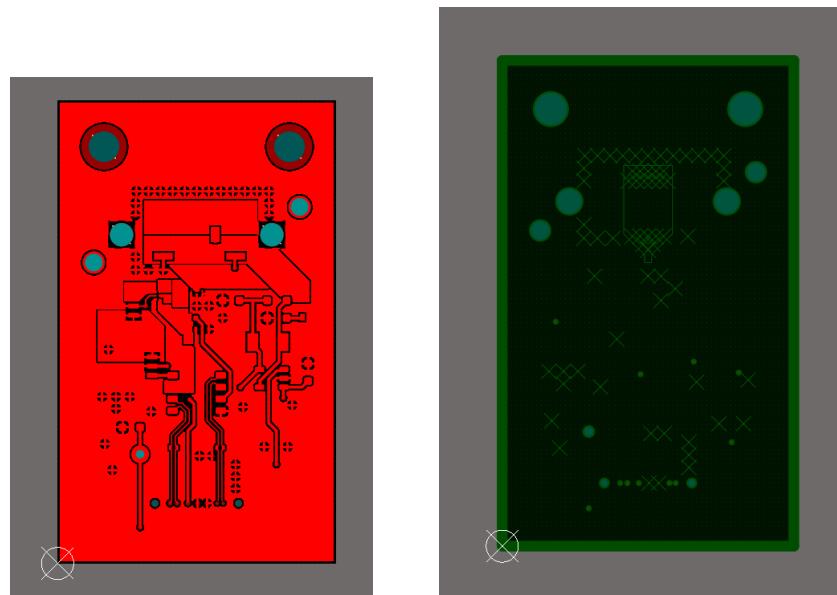


Figure 17: Pulser Board Top and Inner Top Layer

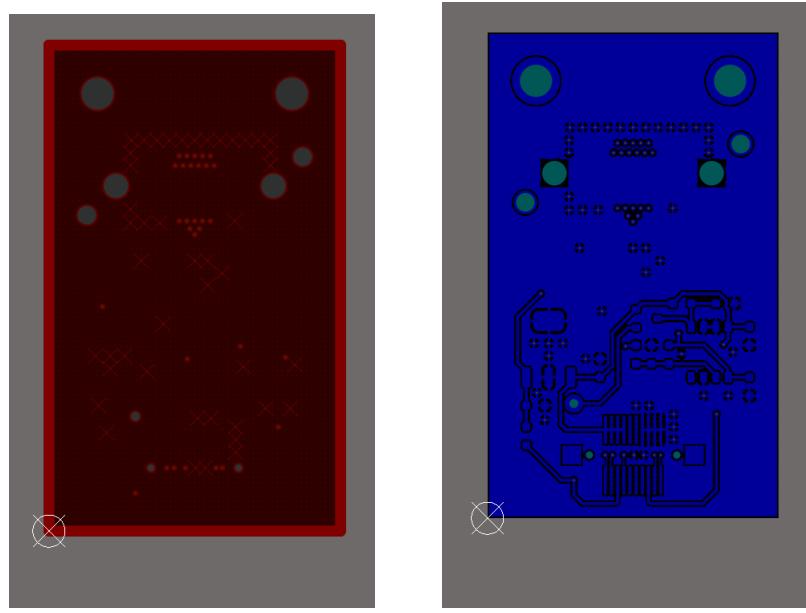


Figure 18: Pulser Board Inner Bottom and Bottom Layer

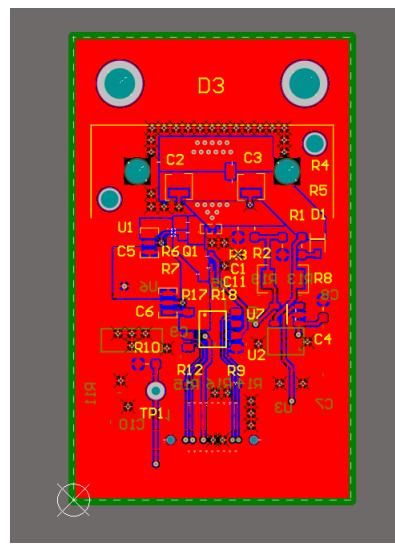


Figure 19: Pulser Board Layer Overview

367 6.3 LED

368 6.3.1 Overview

The LEDs are the most crucial component in the system as the characteristics of these primarily determine the light output, regardless of electronics. LEDs are usually not rated for such high-speed applications, which meant LEDs had to be tested and validated in-house, as datasheets do not provide the required information. The specification required was a 1–10 ns clean single pulse, sub-400 nm wavelength, small surface mount package, narrow output beam so it can be coupled to a fibre with reduced losses and a good range of photon output. Several LED packages were purchased from Kingbright and LC-LED, and their performance tested. The results of these tests are given in Section 6.3.4.

377 6.3.2 Switching Circuit

The redesign process provided a valuable opportunity to evaluate a revised layout and new components for the switching circuit. Several enhancements have since been implemented in the revised switching circuit. Most importantly, the switching side of the layout has been rerouted. In contrast to the previous configuration, where current would flow through the limiting resistor regardless of the LED state, the updated design only allows current flow when the LED is active (refer to Figure 20). This modification reduces both thermal dissipation and the overall power consumption of the system. To modulate light intensity, a variable power supply is now employed to adjust the voltage supplied to the LED. This method has proven highly effective. Tests were conducted at various voltage levels using the full 181 m length of optical fibre—the maximum expected in Hyper-K at the time of testing—and the resulting photon output ranged from approximately 1×10^5 to 2×10^7 photons per pulse. Refined testing results are shown in Section 6.3.4. Further discussion regarding the implementation and performance of the variable voltage supply is provided in Section 6.5.

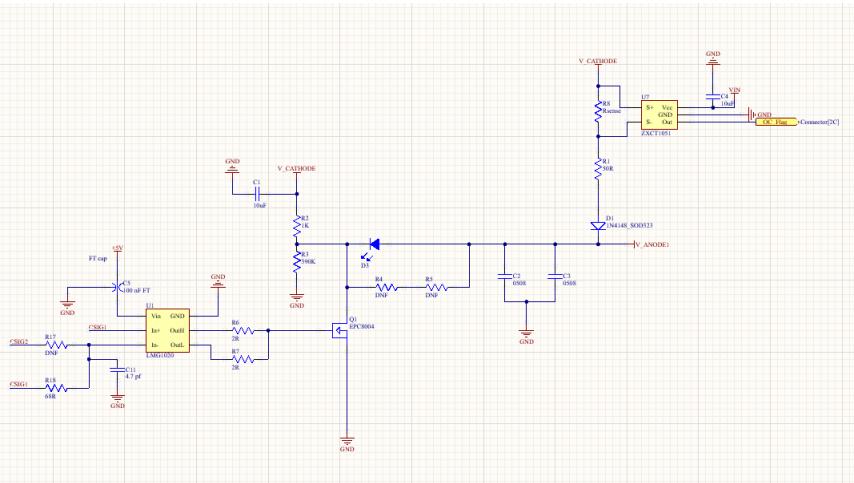


Figure 20: Switching Circuit Layout with LMG1020 and over current IC, R4 is 6.8 nH inductor and R5 is 3R3 resistor

392 6.3.3 Switch Selection

393 The previous iteration of the pulser board utilised a BFR92 [7] high-speed RF NPN switching
 394 transistor which was directly driven by a LVDS-to-TTL converter. In the redesign phase,

395 alternative circuit topologies were explored—particularly those suitable for generating (sub-
396)nanosecond pulses. This investigation led to the adoption of gate driver circuits. Gate
397 drivers are advantageous not only because they can power switches with challenging drive
398 requirements, but also because sub-nanosecond electrical pulses can be achieved by modu-
399 lating the enable pin with slight timing offsets.

400 The fastest commercially available gate driver identified was the Texas Instruments
401 LMG1020 [8]. This device supports pulse widths down to 1 ns, with typical rise and fall
402 times of 400 ps. Additionally, it features an enable pin that allows for precise nanosecond
403 pulse shaping ². The LMG1020 is compatible with both Gallium Nitride Field Effect Tran-
404 sistor (GaN) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) switches,
405 broadening the scope for future component integration and experimentation. It is widely
406 available and priced at £1.97 per unit in the quantities we will require for full production.

407 For the switching element, enhancement-mode GaN transistors manufactured by EPC
408 were selected due to their superior switching characteristics. This recommendation origi-
409 nated from Nick Braam, an engineer at the University of Victoria, who contributed to the
410 pulser board design for the mPMT system [9]. Two EPC devices were shortlisted: the
411 EPC2012 [10] and EPC8004 [11]. The EPC2012 offers a simpler footprint, which could re-
412 duce manufacturing defects. However, the EPC8004 features lower parasitic capacitance,
413 see Figure 21 for the EPC2012 values and Figure 22 for EPC8004 values, leading to better
414 high-speed performance.

415 To evaluate optical output performance, a 40 m length of FP400URT [2] optical fibre,
416 a Mouser-sourced 385 nm LED (ATS2012UV385 [12]), and a Hamamatsu H10721-210 [13]
417 PMT were used. The EPC-based configurations exhibited nearly identical pulse shapes,
418 whereas the BFR92-based circuit’s pulse shape was less sharp at identical pulse widths, as
419 shown in Figure 23. Consequently, the EPC8004 (Figure 24) was chosen for implementation.
420 Optimal performance of the EPC GaN switches required careful layout considerations. A
421 layout was developed in accordance with EPC’s design guidelines [14], targeting minimal
422 parasitic inductance and capacitance. The design employs two layers placed directly above
423 one another, utilising large copper planes and multiple vias to ensure uniform current dis-
424 tribution. The PCB will be fabricated and assembled by PCB Train, using their 0.8 mm
425 thick, four-layer stack-up, which offers minimal inter-layer separation for optimal electrical
426 performance (Figure 15). This same layout strategy was applied to the BFR92 circuit to
427 provide a fair performance comparison.

428 A significant challenge at low pulse widths is the presence of a trailing edge or “tail” in
429 the LED output. This effect arises due to charge accumulation and the intrinsic capacitance
430 of the LED, resulting in extended decay times and pulse broadening (see Figure 25). To
431 mitigate this, a parallel modified snubber circuit was implemented, consisting of a 6.8 nH
432 inductor and a 3.3 Ω current-limiting resistor. Upon LED turn-off, the inductor generates an
433 electromotive force (EMF) that actively extracts residual charge from the LED, accelerating
434 its shutdown. The effectiveness of this approach is illustrated in Figure 26. Additionally,
435 two 0508 reverse-topology 100 nF capacitors have been incorporated. Their role is to act as
436 local energy reservoirs, providing rapid current delivery to the LED during pulse operation,
437 surpassing the response time of the main power supply.

438 6.3.4 Testing

439 For testing purposes, the previous-generation United Kingdom Light Injection (UKLI) moth-
440 erboard and associated software were utilised in conjunction with a prototype of the next-
441 generation pulser board. This prototype consisted of four distinct circuit variants: one

²See page 12 and 13 in [8].

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)					
C_{ISS}	$V_{\text{DS}} = 100\text{ V}, V_{\text{GS}} = 0\text{ V}$		128	145	pF
C_{OSS}			73	95	
C_{RSS}			3.3	4.4	

Figure 21: EPC2012 Capacitance Values IC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics[#] ($T_j = 25^\circ\text{C}$ unless otherwise stated)					
C_{ISS}	$V_{\text{GS}} = 0\text{ V}, V_{\text{DS}} = 20\text{ V}$		45	52	pF
C_{OSS}			23	34	
C_{RSS}			0.8	1.3	

Figure 22: EPC8004 Capacitance Values IC

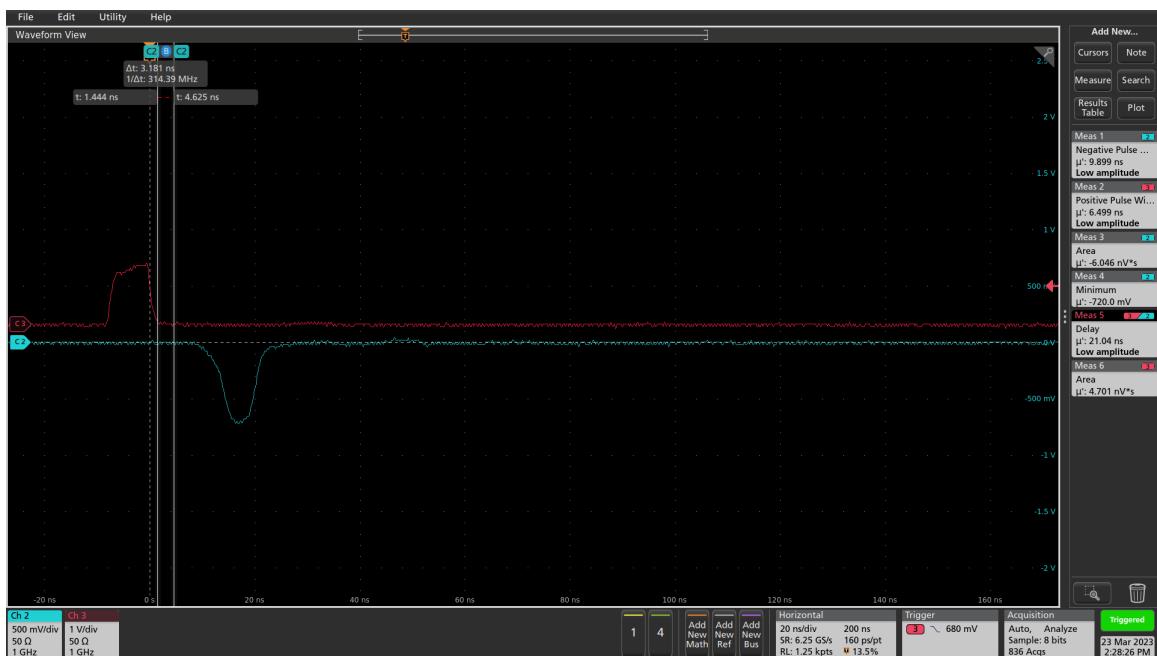


Figure 23: BFR92 Pulse Shape

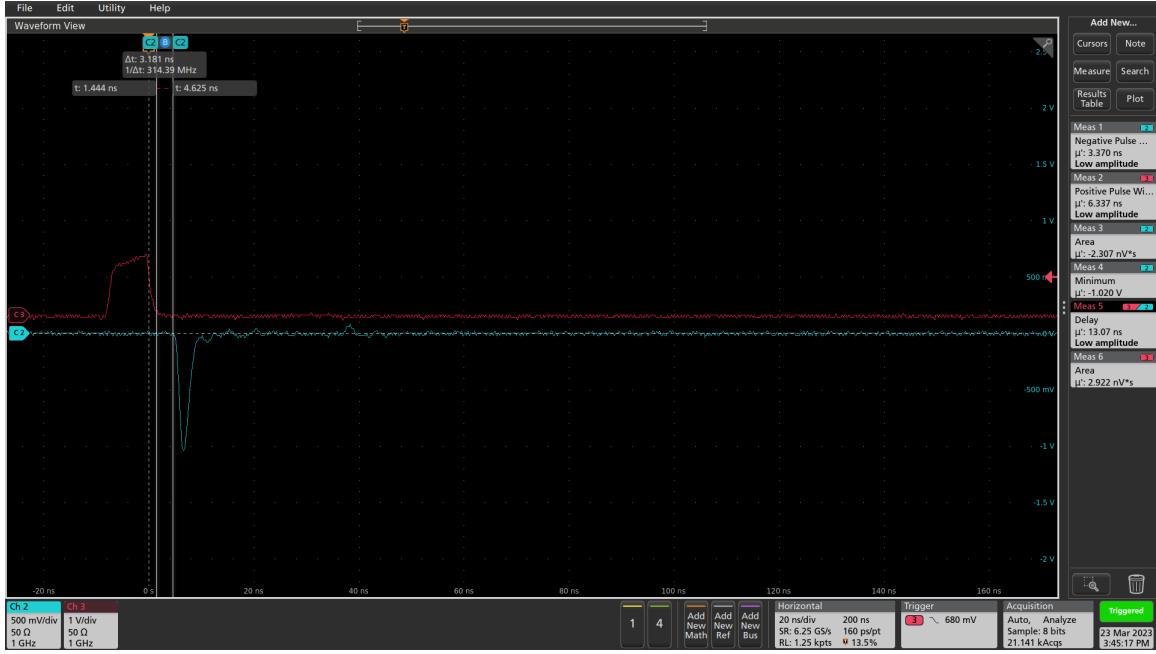


Figure 24: EPC8004 Pulse Shape

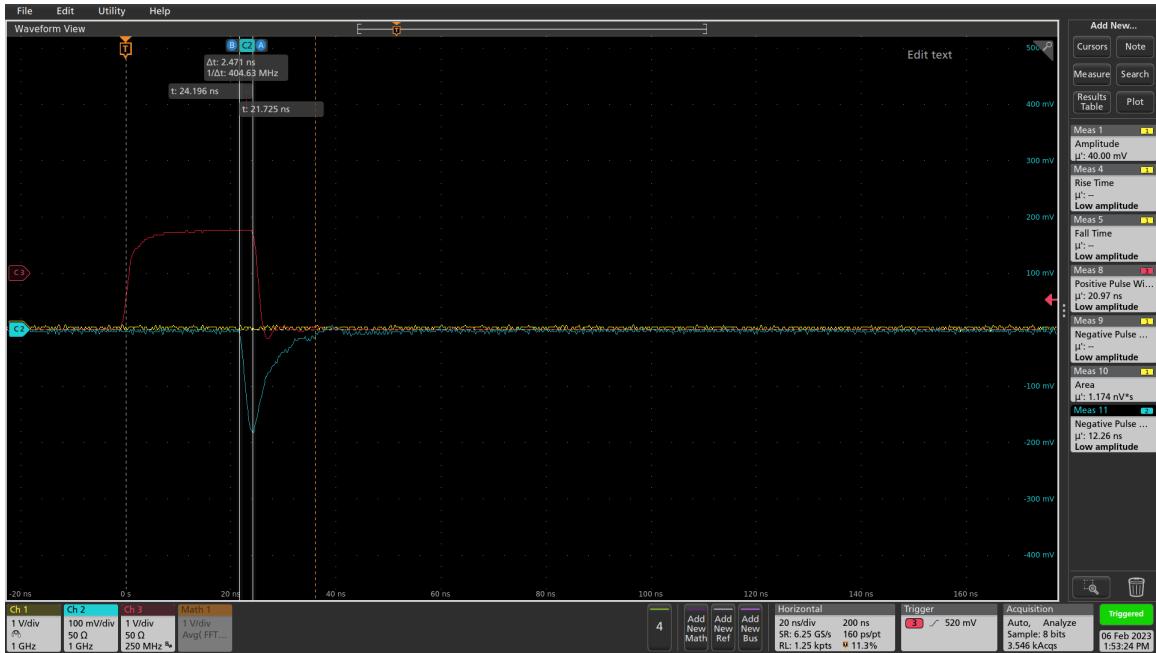


Figure 25: Pulsing Circuit With No Inductor and Resistor

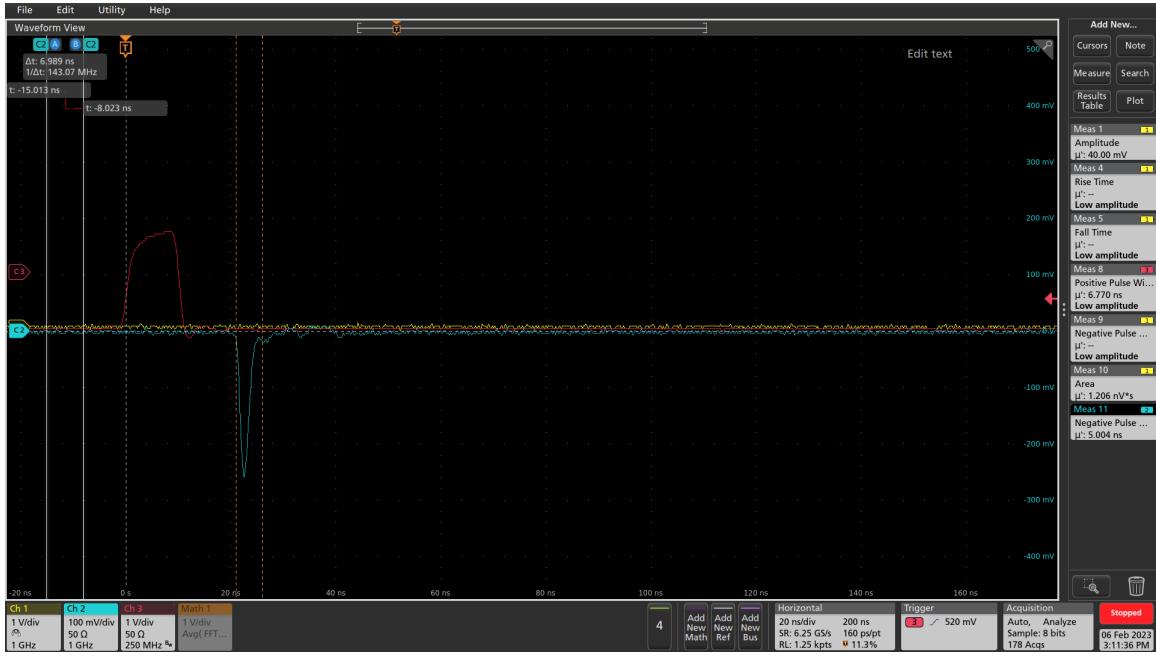


Figure 26: Pulsing Circuit With Inductor and Resistor

442 employing the EPC8004 switch, another utilising the EPC2012 switch, a third using the
 443 same high-speed transistor (BFR92) as implemented in the legacy system, and a fourth vari-
 444 ant incorporating an EPC2012 gate in a through-hole package instead of the standard 0805
 445 surface-mount footprint. Further evaluation was also performed using the latest pulser board
 446 prototype once they had arrived.

447 Following comparative performance evaluations, the configuration using the EPC8004
 448 switch was selected for continued use. While both the EPC8004 and EPC2012 switches
 449 exhibited similar electrical characteristics, the EPC8004 offered superior performance due to
 450 its lower parasitic capacitance, without any additional cost. The pulser board assembly was
 451 housed within a dark box during testing, and a 3D-printed fibre coupler was employed to
 452 facilitate light delivery. The initial focus of the evaluation was on the shape of the generated
 453 optical pulse. During component selection, it was observed that the LED previously sourced
 454 from Mouser (ATS2012UV385 by Kingbright) provided acceptable performance in terms of
 455 electrical characteristics, but the optical output was suboptimal, as it was showing a strange
 456 “double pulsing”, which can be seen in Figure 27. Additionally, this LED was found to be
 457 out of stock and obsolete at the time after testing, precluding further procurement.

458 Subsequently, four ultraviolet LEDs from LC LED were assessed—two emitting at 365 nm
 459 and two at 395 nm—each in both 0805 and 0603 surface-mount packages. Results demon-
 460 strated that the 0805 package LEDs provided significantly better optical coupling efficiency
 461 with the FP400URT optical fibre. Furthermore, the 365 nm variant exhibited superior opti-
 462 cal power output relative to the 395 nm counterparts. Based on these findings, the LC LED
 463 UT-67UV365P [15] 365 nm LED was selected as the most suitable LED for this application.
 464 Tests showed the LED was behaved well, providing an optical pulse of 2.8 ns width, with
 465 3.3 ns eletrical signal, as shown as Figure 28. The pulse width deviation is 60.218 ps, or
 466 2.12% , and the histogram shows the pulse distribution.

467 A long-term stress test was also performed for this LED. The pulser system was placed
 468 in a small dark box, and a new 365 nm LED was soldered onto the pulser board. The pulse
 469 frequency was set to 30,000 Hz, and the pulse width was set to 2.8 ns pulse width, which
 470 yielded a 6.8 ns pulse after dispersion through 180 m of fibre. The system was running

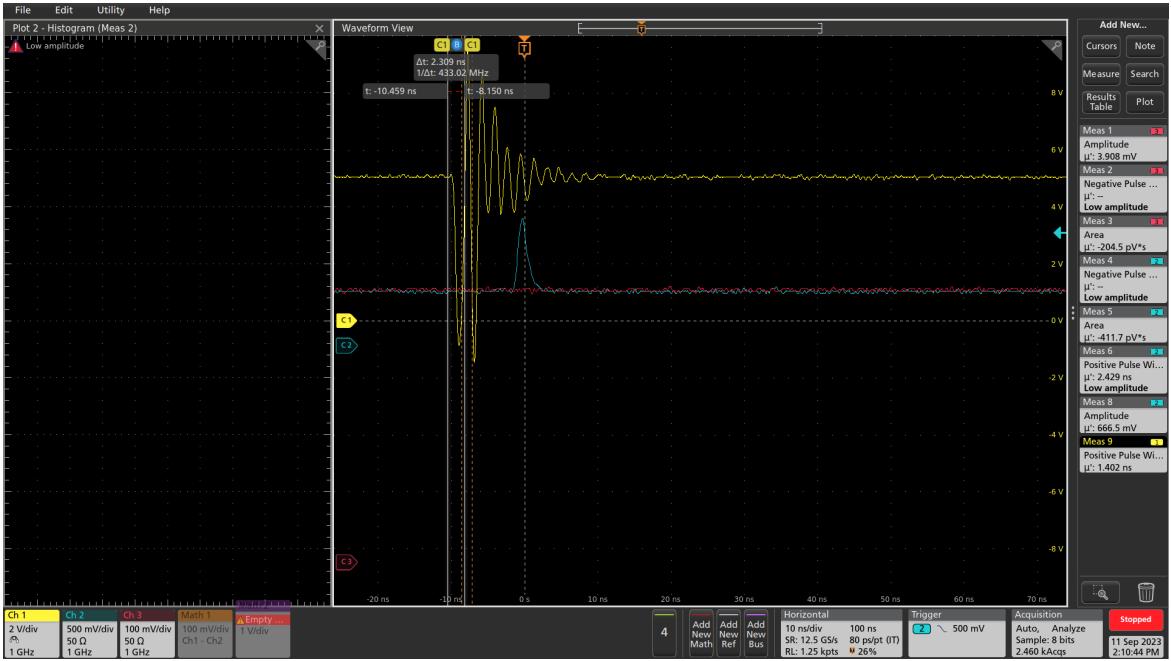


Figure 27: Double pulse observed from the Kingbright ATS2012UV385 LED.

471 continuously for 13 days, during which power and air temperature measurements were made
 472 every 10 seconds. The air temperature was measured at the power meter, using the Thorlabs
 473 PM100USB. Each individual LED is expected to run at around 0.0082 Hz, as the auto-calib
 474 process is expected to pulse any channel at 1 Hz rate and there are 122 active channels. This
 475 means that pulsing the LED at 30 KHz for 13 days is equivalent to 106,849 years of normal
 476 running, not including the short dedicated calibration runs where the system will run at
 477 1 kHz. While we have not calibrated the temperature gain, we are estimating a 1.5% loss if
 478 we compare the same temperature from the beginning of the experiment to the end. **ADD**
 479 **PLOT FOR THIS**

480 6.4 LVDS to TTL Converter

481 The DS90C402 [16] from Texas Instruments was selected as the LVDS-to-TTL conversion
 482 solution. This device is a dual-channel converter, chosen primarily for its fast switching
 483 characteristics—offering both rise and fall times of approximately 500 ps. It operates at
 484 5 V and provides 5 V TTL output levels, which aligns well with the requirements of the
 485 downstream switching circuitry. The inclusion of two channels is particularly advantageous,
 486 as it enables the generation of sub-nanosecond differential pulses by precisely offsetting the
 487 channels, as described in Switch Selection. Among commercially available devices with
 488 these specifications, the DS90C402 is the fastest and is readily available through multiple
 489 distributors.

490 The associated circuit was implemented in accordance with the manufacturer’s recom-
 491 mendations provided in the datasheet. A decoupling capacitor was placed in close proximity
 492 to the power supply pin to minimise voltage ripple. Output traces were routed using polygon
 493 fills to reduce impedance and enhance signal integrity, and a continuous ground plane was
 494 placed beneath the signal layers to improve shielding and minimise electromagnetic interfer-
 495 ence. The schematic for this is given in Figure 29.

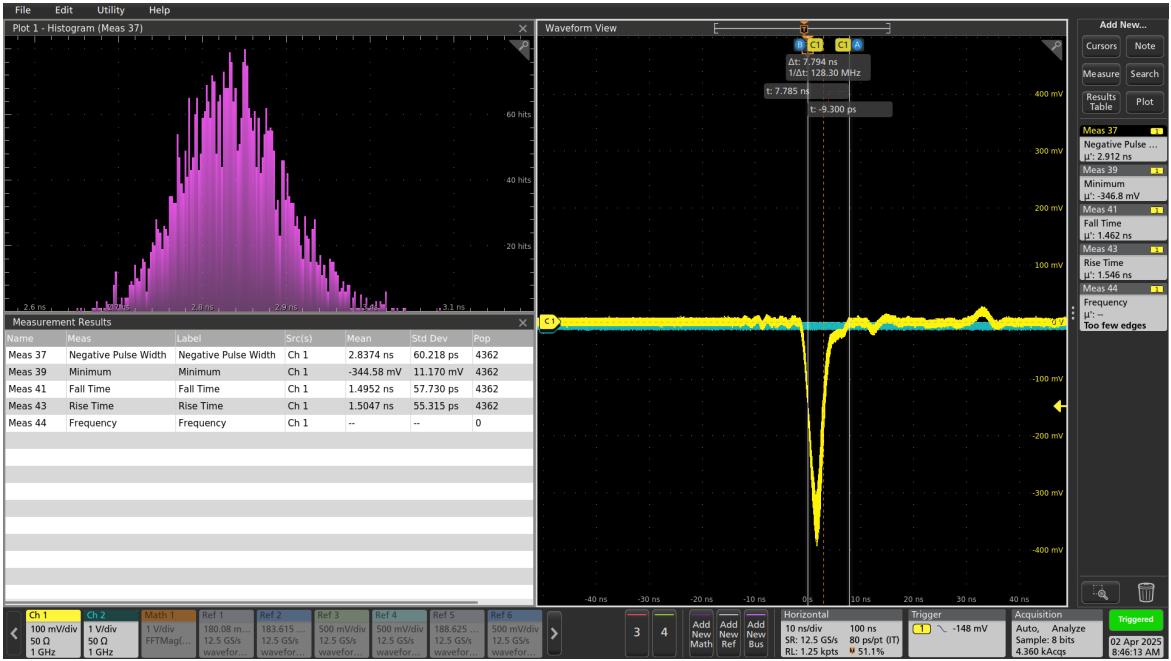


Figure 28: Scope trace and pulse width histogram for a 3.3 ns input signal, through a 1 m FP400URT fibre.

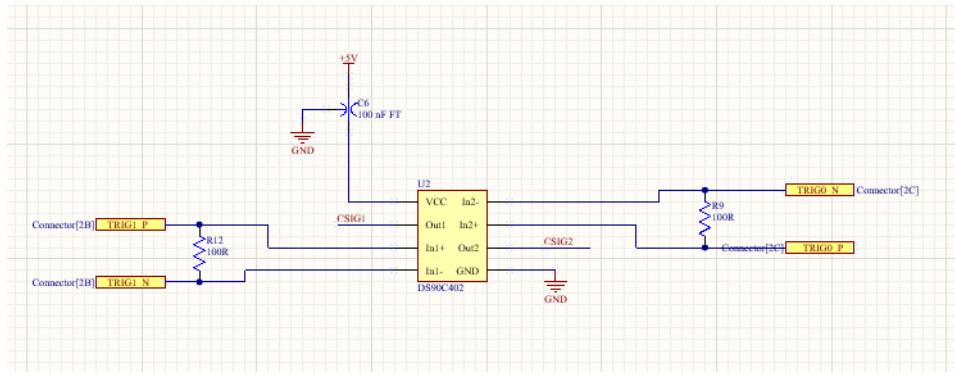


Figure 29: LVDS-TTL Converter Schematic

496 6.5 Power Supplies

497 Each pulser board is required to incorporate a variable voltage power supply dedicated
 498 to driving the LED, with an adjustable output range from 3 V to 12 V. This supply is
 499 used exclusively to modulate the LED’s light output by varying the forward voltage, and
 500 consequently the current. The design specification also necessitates that the power supply
 501 be remotely controllable—i.e., capable of being switched on or off via a simple logic-level
 502 signal.

503 For this purpose, the LT1963A [17] adjustable low-dropout linear regulator was selected.
 504 This regulator has demonstrated reliable performance in previous pulser board iterations
 505 and offers a favourable balance of cost-effectiveness and controllability. The implementation
 506 includes standard filtering and decoupling, with layout details provided in Figure 30. The
 507 schematic provided in Figure 31 is an early version used for prototyping; the adjustable
 508 circuit has been simulated and will be tested shortly, and the enable circuit has been tested,
 509 modified and simplified. Updated schematics will be provided with v1.0 circuit. There will
 510 be overcurrent protection built in to the system as well. A ZXCT1051 (Reference!) is used

511 to monitor the current and if it senses larger than normal current then it send a signal to
 512 the FPGA to turn the damaged board off. A surface mounted fuse will be added in line as
 513 well to make sure there is a second line of defense as well.

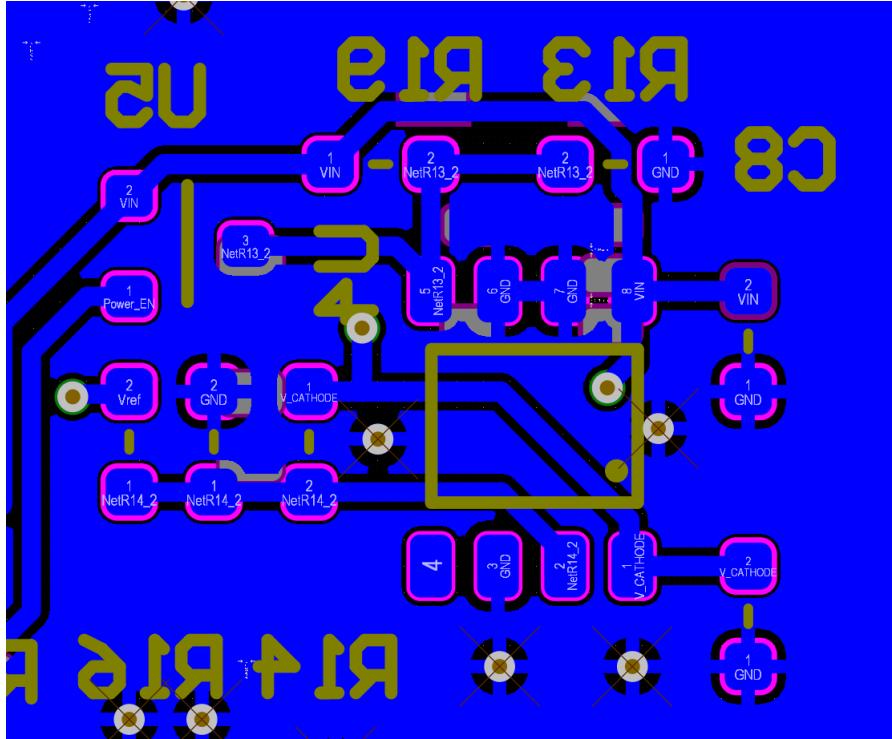


Figure 30: LT1963 Layout

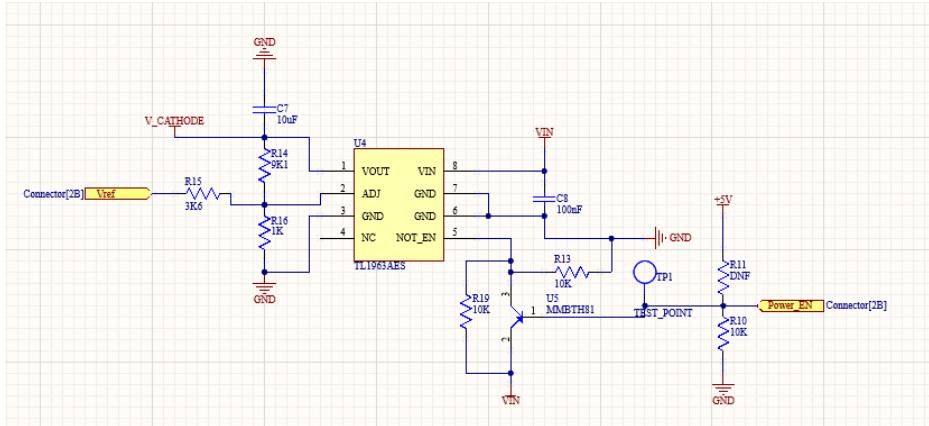


Figure 31: 12V Circuit Schematics

514 In addition to the variable LED supply, each board requires a stable 5 V supply to power
 515 both the DS90C402 LVDS-to-TTL converter and the LMG1020 gate driver. Unlike the LED
 516 supply, this rail remains continuously powered. The 5 V supply is provided by an LM2937-5
 517 [18], a fixed-output linear voltage regulator, which has been successfully employed in various
 518 high-speed and low-noise applications within the laboratory. The associated circuit schematic
 519 and layout and schematic are shown in Figures 32 and 33 respectively.

520 To meet system-level design constraints, each pulser board is equipped with its own
 521 independent 12 V input supply, ensuring that LED output intensity can be individually

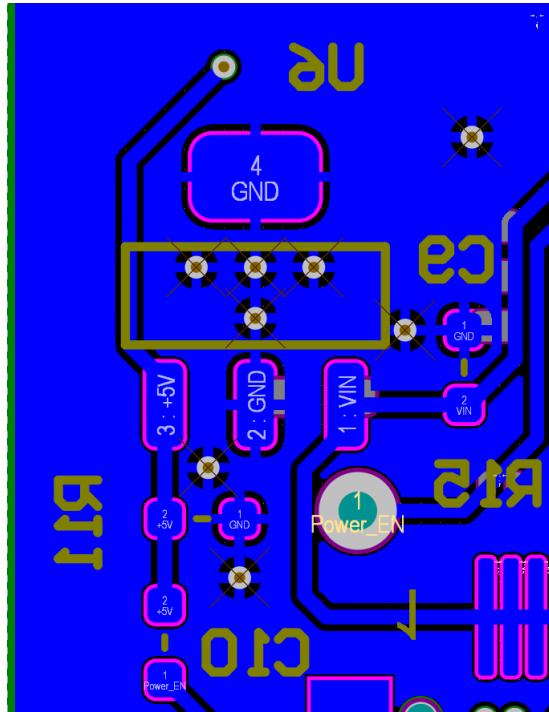


Figure 32: LM2937-5 Layout

controlled on a per-board basis. However, the 5 V supply is common across all boards and derived locally on each pulser module. This approach allows for localised filtering and minimal power distribution path lengths, reducing the risk of noise coupling and voltage drop considerations that are particularly critical in high-speed circuit applications.

Power is supplied to each board via the Eurocard backplane. The 12 V input from the Eurocard simultaneously feeds both the variable (LED) and fixed (logic) power regulators on the pulser board. The LED enable function is controlled via a 5 V logic signal originating from the Eurocard's GPIO interface. Additionally, a DAC output from the Eurocard provides a voltage control signal to the adjustment pin of the LT1963A regulator on each pulser board, thereby allowing precise, programmable control of light intensity.

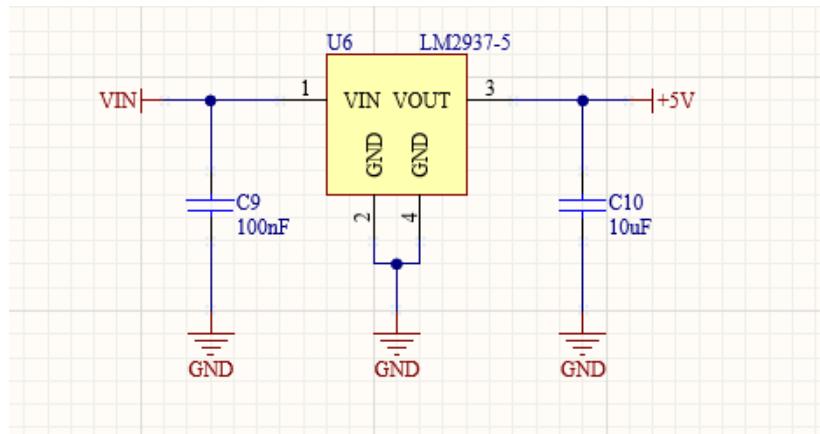


Figure 33: 5V circuit schematics

532 6.6 Connector

533 The previous board connector was deemed too bulky and expensive for the larger number
 534 of channels needed in this system, leading to the process of finding a more suitable alterna-
 535 tive. Following an evaluation of commercially available options, the Phoenix Contact female
 536 connector 1331962 [19] was selected. This connector offers several advantageous specifica-
 537 tions: it is rated for 500 V, features a low contact resistance of $40\text{ m}\Omega$, supports a maximum
 538 current of 0.5 A, and is capable of signal transmission up to 20 Gbit s^{-1} . In addition, it is
 539 cost-effective, priced at approximately £0.50 per unit, with wide availability ensuring ease
 540 of procurement. Multiple height variants are available within the same series, facilitating
 541 flexible mechanical integration within the Eurocard crate system. The compact footprint of
 542 the connector allows for a reduced PCB form factor. Electrically, the high-frequency perfor-
 543 mance supports reliable LVDS signal transmission. Additionally, the compact footprint of
 544 the connector is well-suited to space-constrained PCB layouts.

545 An illustration showing the connector and corresponding circuit layout is provided in
 546 Figure 34.

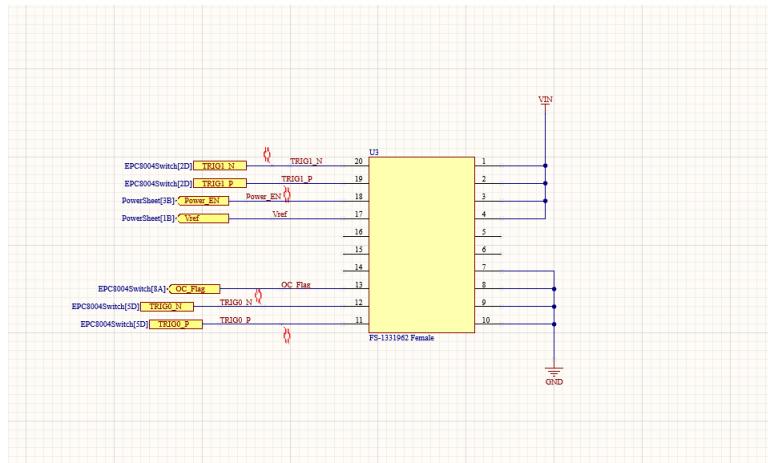


Figure 34: Connector Schematics

547 6.7 Fibre Coupler

548 During the prototyping phase, improvements were made to the PCB layout to better ac-
 549 commodate a fibre coupler. As a result, the current design includes provisions for precise
 550 mechanical mounting and alignment. Specifically, two mounting holes for M2 screws have
 551 been incorporated, enabling the 3D-printed coupler to be firmly secured to the board (see
 552 Figure 35). In addition, two dowel holes have been added to guide the coupler into posi-
 553 tion, ensuring accurate alignment over the LED. Given the tolerances associated with PCB
 554 fabrication and 3D printing, an alignment accuracy of approximately $100\text{ }\mu\text{m}$ is expected.

555 To optimise the electrical path, capacitors have been repositioned as close as possible to
 556 the LEDs. This minimises parasitic inductance and resistance, while enabling a centralised
 557 layout of larger components. The resulting configuration creates a compact chamber housing
 558 both the LEDs and associated capacitors.

559 The design for the fibre coupler is modular, consisting of three components: a base
 560 section mounted to the pulser PCB, a top section into which the fibres will be epoxied, and
 561 an intermediate attenuator element. The latter part will be added to the current design to
 562 space the fibre from the LED and thereby adjust the optical coupling efficiency to achieve
 563 required attenuation, accounting for the different lengths of fibre in the system. This means



Figure 35: Fibre Coupler Design

564 the attenuation will be implemented within the coupler itself, allowing the LED output to
565 remain within the electronically controlled dynamic range.

566 The fibre coupler will be fabricated via stereolithography (SLA) using a black resin to
567 minimise light transmission through the material. Additional light-tight testing will be
568 conducted, and black paint may be applied if further sealing is required. Furthermore, laser-
569 cut rubber gaskets will be introduced at interface points to ensure optimal optical isolation
570 and mechanical sealing.

571 **6.8 Photon Yield Tests**

572 tests on maximising photon yield and available dynamic range should be fully described here

573 **6.9 Production**

574 Production will be carried out using PCB Train as they are local and competitively priced,
575 and known to produce boards of good quality. Estimated cost is £12.27 per board, which
576 equates to £1,496.94 for 122 units or £1,840.5 for 150 units, and production is £4073.48 for
577 122 units for 15 days lead time, or £3985 for 150 units at 25 days lead time. The full cost
578 breakdown is shown in Figure 36

579 **6.10 Changes Expected from v0.9 to v1.0**

580 **6.10.1 LED and Switching Circuit**

581 There will be minimal changes to the LED and switching circuit. Changes will be made to
582 the position of the switching devices, placing them slightly closer to each other to reduce
583 transmission line length. The LED will likely remain as the LC LED UT-67UV365P 365nm
584 0805 LED, but further LED tests will be performed. This takes a short amount of time, and
585 may lead to discovering better LEDs in the future which would be easy to swap in due to
586 standardised footprints.

587 **6.10.2 LVDS-to-TTL converter**

588 No changes are expected to this circuit.

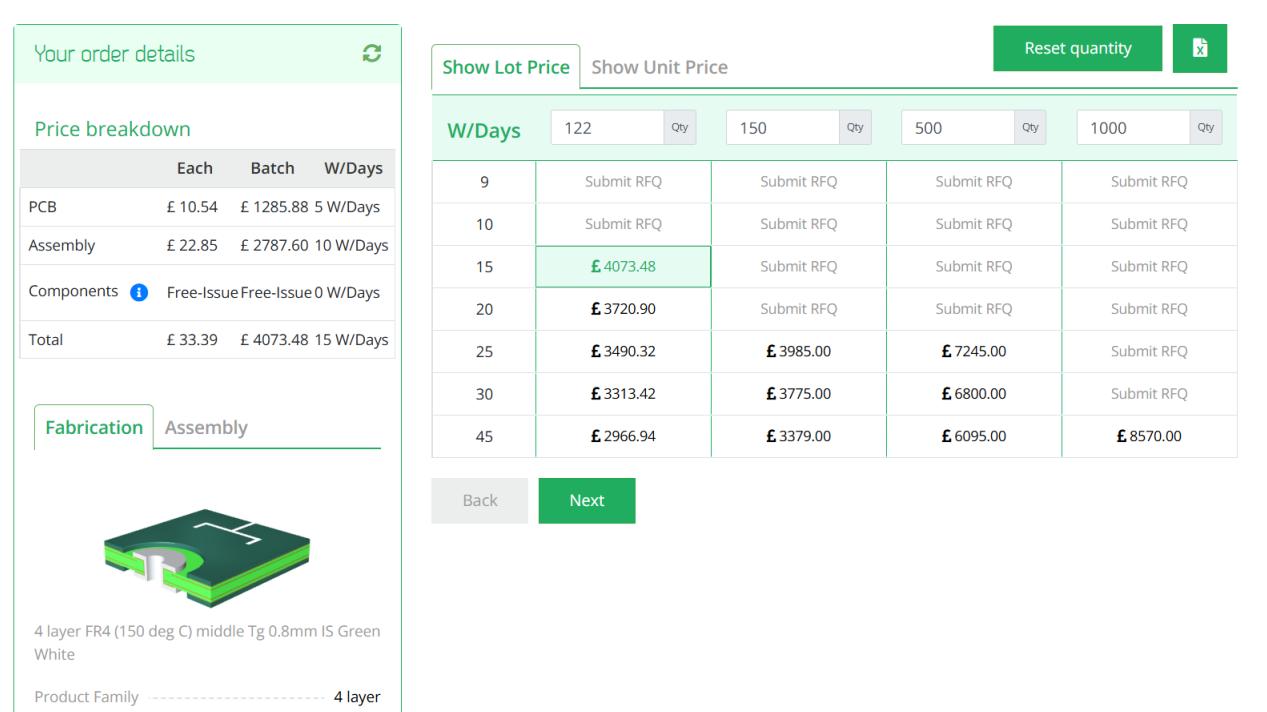


Figure 36: PCBTrain PCB production and assembly costs

589 6.10.3 Power supplies

590 Reverse voltage bias will be removed as no difference between normal and reverse bias was
 591 observed photon output. The overcurrent protection and power enable circuit will be re-
 592 worked.

593 6.10.4 Connector

594 No changes are expected to this.

595 6.10.5 Fibre coupler

596 A brand new fibre coupler will be designed due to the recent requirement changes regarding
 597 the different fibre lengths.

598 7 Server Rack and Cooling

599 To house the electronics for the LI systems, two 42U server racks with 800 mm depth will
 600 be used. The front of the server rack will be used for electrical connections and displays,
 601 and the reverse/internal will be used only for fibre routing. The server racks will include
 602 Uninterruptible Power Supplies (UPS) for safe power delivery and for power processing, to
 603 avoid issues with potential instabilities in the main power supply. Each rack will include an
 604 air conditioning unit to have a controlled temperature and remove humidity from the air,
 605 as the relative humidity in the air is expected to be above 70%. Although specific tests on
 606 running the LED electronics in humid conditions have not been carried out, it is known that
 607 the optical switches for the laser calibration system requires lower humidity levels. In order
 608 to simplify things and remove the potential of humidity issues with the LED electronics,

609 both server racks will be air conditioned. These systems are widely available and will be
610 chosen closer to installation.

611 8 LED Monitoring

612 To monitor the light output from the LEDs before attenuation by fibres and convolution
613 with water parameters, PMTs will be placed near to the LED sources. This is a similar
614 design to what is currently used in the Super-K UKLI system. Each LED connector will
615 feature a second fibre to take light to a series of PMTs, which are expected to be Hamamatsu
616 H10721-210. Due to the 8 mm diameter of the PMT window, up to 16 fibres can be attached,
617 meaning one PMT can monitor up to 16 LED boards at once. Each PMT will be powered
618 by a unique low cost power supply developed for the SK UKLI system. These will be housed
619 in a small 2–3 U server rack. The signals from the PMTs will then go to the dedicated HK
620 electronics channels that are set up for monitoring.

621 9 Control System for LEDs

622 The LEDs are driven by a differential LVDS signal originating from the FPGA. The FPGA
623 in use is the Genesys 2 [20] development board, which operates a pulsing VHDL module
624 clocked at 300 MHz. Pulses are generated on the rising edge of this clock, and toggling the
625 output (i.e., asserting and then deasserting the trigger) requires a minimum of two clock
626 cycles. Consequently, the shortest achievable pulse duration in this configuration is 3.3 ns.

627 One of the main limitations of this setup is the coarse time resolution: pulse durations
628 are effectively constrained to integer multiples of 3.3 ns. To achieve a broader and more
629 finely resolved spectrum of optical injection into the detector, improved temporal precision
630 is necessary. This is accomplished using the Xilinx **IODELAY** primitive, originally designed for
631 high-speed interface timing alignment. The **IODELAY** module permits fine-tuning of signal
632 timing to account for PCB trace mismatches, and in this application, it is repurposed to
633 introduce controlled delays between pulses.

634 To generate shorter pulses, two identical signals are created, one of which is delayed
635 using **IODELAY**. These signals are then combined using a logical **AND** operation, producing
636 a narrower pulse. Since the **IODELAY** module requires one clock cycle to process the input,
637 both signals—regardless of whether they are delayed—must pass through an **IODELAY** stage
638 to ensure temporal synchronisation.

639 Conversely, to produce longer pulses, the same methodology is applied, but the signals are
640 combined using a logical **OR** gate instead. This approach extends the pulse width beyond the
641 base clock resolution, enabling pulse durations ranging from approximately 1.5 ns to 4.5 ns
642 in 49 discrete steps. The lower bound is determined by the threshold of the LVDS-to-TTL
643 converter, which does not respond to pulses shorter than approximately 1.5 ns .

644 For channels using the longest optical fibres, this extended range is sufficient, given
645 the intrinsic dispersion in the fibre optics of around 5 ns. However, shorter fibres require
646 additional pulse shaping. To this end, an additional mechanism is implemented using a **for**
647 loop structure within the FPGA logic. This allows the pulse to persist for multiple clock
648 cycles, effectively producing longer pulses by repetition. However, due to FPGA architecture
649 constraints, each iteration of the loop consumes a clock cycle, necessitating careful timing
650 control. For instance, to produce a 6.6 ns pulse, the loop must be configured for two cycles,
651 accounting for the loop overhead.

652 Further refinement is under investigation through the daisy-chaining of multiple **IODELAY**
653 modules. This would enable sub-nanosecond granularity by introducing additional interme-
654 diate delay steps. While promising, this technique requires further validation and testing.

655 The pulse control data structure is currently under development. There are two types
656 of pulse description considered. In the first option, the software interface would require two
657 parameters per channel: a *coarse* step and a *fine* step, reflecting the approach used in the SK
658 system. The other option would be just a single variable and then simple logic turning that
659 variable into the *coarse* and *fine* step that the internal logic requires. Two hardware modules
660 are planned: one for generating the single shortest possible pulse (to minimise latency), and
661 another for multi-cycle pulses using programmable duration. A selection logic will assess the
662 input and route it to the appropriate module based on the desired pulse characteristics.

663 Each LED channel will be controlled independently, allowing for unique pulse configura-
664 tions across channels. The global trigger will be derived from the system clock, and each
665 channel will pulse in a predefined sequence while triggered from the global trigger. This
666 architecture also supports simultaneous pulsing of multiple channels. Should asynchronous
667 behaviour be required, additional per-channel delay logic can be implemented. Given the
668 five distinct fibre lengths used in the system, each channel group will also include a config-
669 urable delay offset to compensate for propagation time differences. These group delays will
670 be calibrated and fixed, with the option of fine-tuning individual channels post-deployment
671 if necessary.

672 The repetition rate can be adjusted as well, including a single pulse, using external
673 trigger, from 0.001Hz through 1 KHz to multiple megahertz if needed, but the system was
674 only tested up to 30 KHz, as that was a high enough rate to illuminate the power monitor's
675 sensor.

676 The FPGA programming remains in active development. Inter-crate communication
677 protocols and synchronisation are currently under integration and testing.

678 10 Crate Electronics

679 10.1 Overview

680 The system specification calls for control of up to 122 LED channels, significantly exceeding
681 the channel counts used in current systems such as Super-Kamiokande or LUX-ZEPLIN,
682 which the previous generation of pulser boards are used for. To manage this complexity, the
683 design prioritises ease of use, maintainability, and straightforward deployment, particularly
684 given that the server racks will accommodate hundreds of optical fibres.

685 To achieve this, a system concept originally developed by ATLAS collaborators (specifi-
686 cally by Ashley Greenal) has been adapted. The original design utilises a Genesys 2 FPGA
687 integrated into a half-width Verotec KM6-2 [21] Eurocard-compatible crate for testing pur-
688 poses. This concept has been extended to a full 19-inch rack width, enabling the integration
689 of up to 36 pulser boards within a single crate.

690 Each FPGA is capable of interfacing with up to 38 pulser boards, thereby maximising
691 the utilisation of available LVDS differential pairs, with an additional pair reserved for the
692 laser trigger signal. This configuration ensures full use of the Genesys 2's I/O capacity while
693 maintaining flexibility for future expansion.

694 The system architecture consists of three primary components: the Blade (Section 10.2),
695 Backplane (Section 10.3) and Eurocard (Section 10.4). This modular approach ensures
696 scalability and facilitates debugging, replacement, and upgrades. It also provides a robust
697 foundation for managing high channel counts while maintaining signal integrity and synchro-
698 nisation across the system.

699 The system will consist of four crates, which allows for up to 144 pulser boards. The
700 OD diffuser system required 122 boards to run, and the auto-Xenon calibration system is
701 expected to use one or two of the additional boards. This means there will be 20 spare boards

702 available for hot-swapping. These can be further grouped into five sets of four, to have four
703 spare boards for each of the five different fibre lengths. Should issues arise, a local technician
704 can remove the signal and monitor fibres from the broken pulser board, attach them to a
705 spare board, and reconfigure the software to use the spare board for running, all with remote
706 expert guidance. Next time an expert is on site they can do further maintenance or repair
707 if needed.

708 **10.2 Blade**

709 The Blade is a simple, eight layer board, that has a SEAM-40-06.5-L-10-2-A-K-TR [22]
710 connector which is a direct fit for the Genesys 2's FMC connector. It features a PCIE 16X
711 connector at the edge for connectivity to the Backplane. The PCIE was selected by Ashley
712 Greenal as it is a well documented standard connector and there are a large amount of
713 connectors available that can be bought easily. While PCIE connectors are being used, the
714 PCIE standards for communication are not. This is a very dense PCB with all the differential
715 tracks on it, so buried vias and multiple layers will be used. See Figure 37 for a work in
716 progress version.

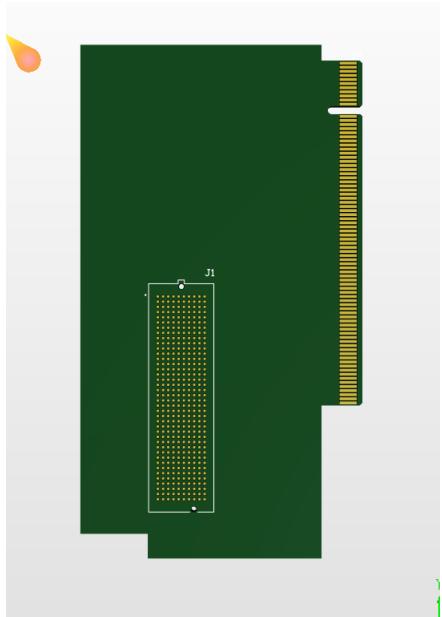


Figure 37: Blade Work in Progress

717 **10.3 Backplane**

718 The Backplane serves two primary functions: the distribution of differential signals from the
719 Blade to the Eurocards, and the reception and distribution of power throughout the crate
720 system. It accepts external power inputs of 12 V and ± 5 V, and includes a basic regulation
721 circuit to stabilise these supply voltages for downstream use.

722 Given the mechanical constraints and routing complexity, the Backplane is implemented
723 as a four-layer PCB with impedance-controlled traces to ensure signal integrity across all
724 differential pairs. It features a single PCIe x16 connector to interface with the Blade, and
725 three PCIe x8 connectors to interface with the Eurocards.

726 The Eurocards are positioned at slots 2, 8, and 64 within the crate. This arrangement
727 creates two symmetrical chambers with 48 units spacing between cards, ensuring adequate

728 space to accommodate the minimum long-term bend radius of the FP400URT optical fibres.
729 This layout balances mechanical reliability with signal routing efficiency and supports long-
730 term maintainability of the system. See Figure 38 for a work in progress version.

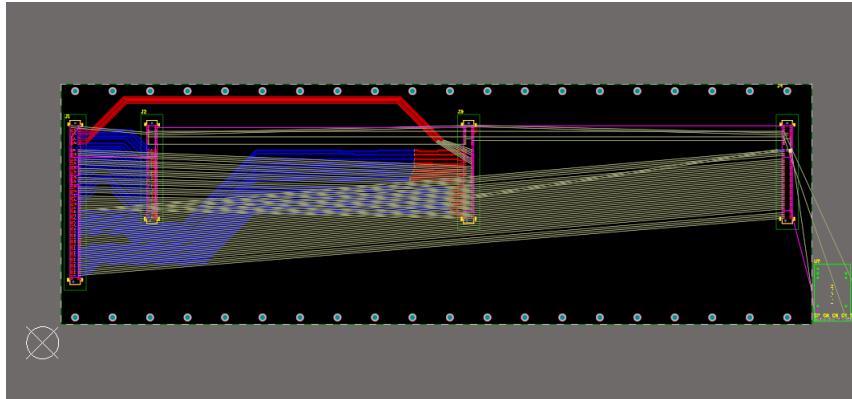


Figure 38: Backplane Work in Progress

731 10.4 Eurocard

732 The Eurocard format defines the physical and electrical standard for the crate system, hence
733 the naming convention. Each Eurocard is equipped with a PCIe x8 connector for interfacing
734 with the Backplane, and is designed to host up to 18 pulser boards—nine mounted on each
735 face. Pulser boards connect via FS-1332120 Male[23] connectors, and each socket includes
736 two mounting holes for mechanical standoffs.

737 The board layout on each side consists of two staggered rows: five sockets in the back
738 row and four in the front. The two faces are laterally offset by approximately 10 mm to
739 prevent interference or fibre clashes when the system is fully populated and enclosed within
740 the crate chamber. This offset ensures smooth fibre routing and accommodates the bend
741 radius requirements of FP400URT fibres.

742 Power distribution within each Eurocard is handled by a THD 12-1212 [24]12 V DC-DC
743 regulator. This regulator provides local power isolation for the pulser boards and includes
744 a control pin connected to a PCA9698 [25] 40-pin GPIO expander. This allows for system-
745 level control, enabling or disabling all pulser boards on a card—an essential feature during
746 power-up, especially when the FPGA may inadvertently drive all differential outputs high
747 during reprogramming.

748 The GPIO expander is responsible for enabling the local 12 V regulator and for selectively
749 powering individual pulser boards. This facilitates fault isolation and power savings in
750 channels that are inactive or disconnected. Additional GPIO pins are assigned to monitor
751 output voltage levels via the overcurrent sensing circuitry.

752 To provide per-channel LED power control, an AD5673 [26] DAC is included. It out-
753 puts analogue control voltages to the onboard adjustable regulators on each pulser board,
754 allowing for independent LED drive voltage per channel. Both the GPIO and DAC devices
755 communicate with the system over the I²C protocol.

756 For laser synchronisation, the Eurocard includes a differential-to-NIM conversion stage.
757 This consists of an LVDS-to-TTL converter identical to that used on the pulser boards,
758 followed by a TTL-to-NIM converter. This ensures compatibility with legacy NIM-based
759 timing systems used in external laser triggering. See Figure 39 for a work in progress version.

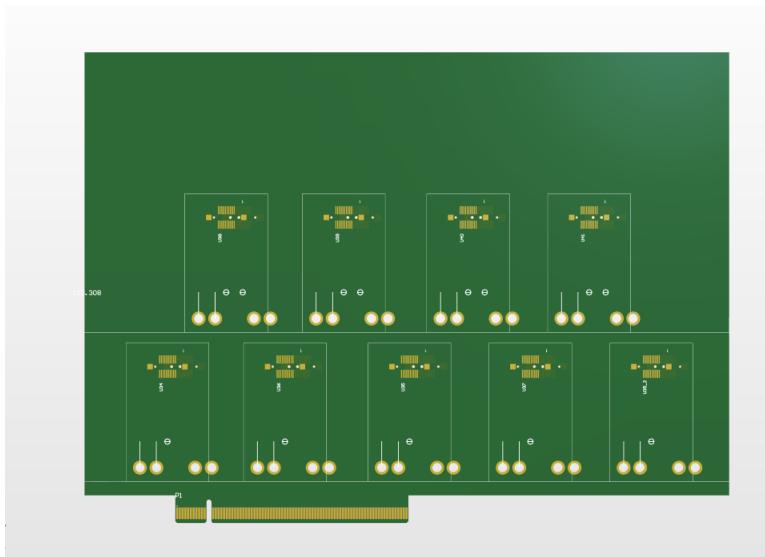


Figure 39: Eurocard Work in Progress

760 11 Conclusions

761 Write this

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