

Hyper-Kamiokande Outer Detector Light Injector System Technical Note

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⁴⁶ **0 Version history**

- ⁴⁷ • v0.99 - First release by Balint circulated to Liverpool group for internal review
- ⁴⁸ • v1 - [Sam]: Ported over to github for continued development, as we hit compilation
⁴⁹ time on overleaf. Initial pass through to fix wording and rewrite some sections. Also
⁵⁰ integrating Warwick TN on OD diffuser. Will add Liz's saturation studies as soon as
⁵¹ these are available. Some reordering of structure to make it flow better.

52 **1 Introduction**

53 Hyper-Kamiokande is a large scale water Cherenkov detector with two main sections, an
54 inner detector (ID) and an outer detector (OD). The OD volume of Hyper-K is a one meter
55 wide annular ring on the circumference of the detector. This space is designed to tag charged
56 particles, such as cosmic ray muons or particles from interactions in the surrounding rock,
57 entering the detector. In addition, the OD volume will be used as working space for instal-
58 lation activities. Once complete, it will be optically separated from the ID volume, and will
59 be instrumented with 3,600 outward facing 8 cm photomultipliers tubes (PMTs). These will
60 each surrounded by wavelength shifting (WLS) plates to increase photocoverage.

61 In order to achieve the precision measurements Hyper-K aims to make, precise calibration
62 of the detector is required. For the OD, a light injection (LI) system will be employed,
63 allowing for known quantities of light to be injected into the detector region. This will
64 consist of 122 diffusers and 12 collimators. The diffuser system, which is described in this
65 technical note, will be used to measure gain and timing properties of the OD PMTs, and
66 will be powered by dedicated pulsed LED sources. The 12 OD collimators are identical to
67 those uses in the ID system, and will be integrated into the ID laser system. Full details on
68 that system, along with investigations of the fibre optics that will be employed for the OD
69 system, can be found in [1].

70 **2 Light Injection System Overview and Requirements**

71 The OD diffuser system will be composed of 122 bare diffusers, installed on the outward facing
72 side of the PMT support structure. The proposed layout for this is shown in Figure 1, though
73 in actuality there will be minor differences from this regular arrangement due to restrictions
from other systems. These are arranged such that they illuminate roughly an equal amount

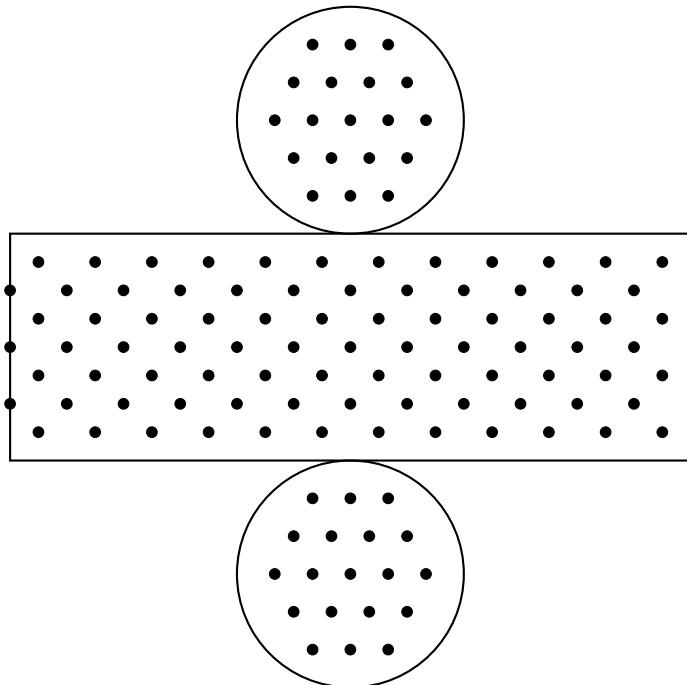


Figure 1: Injector location map for OD diffuser positions. Locations are approximate and
dependent on PMT/WLS plate locations.

74
75 of OD PMTs. One of the primary goals of the system is to inject enough light to saturate the

76 OD PMTs. This goal drives a large part of the photon output optimisation, and Monte Carlo
77 (MC) studies to evaluate the amount of photons required to do this are shown in Section 3.
78 The diffuser design is discussed in Section 4. These will each be illuminated by individual
79 LED pulser boards with 365 nm LEDs. This will require at least 122 dedicated LED pulsers,
80 and spares should be readily available for hot-swapping should a board encounter issues. Full
81 details of the pulser board design are given in Section 6. The pulser boards will be powered
82 and controlled by commercially-available Field Programmable Grid Array (FPGA) boards.
83 The control system architecture for these consists of three primary components:

- 84 • **Blade**: Interfaces directly with the FPGA, distributing all differential signals into the
85 crate system.
- 86 • **Backplane**: Routes differential signals to the pulser boards and provides the primary
87 power distribution, accepting 12 V and ± 5 V inputs.
- 88 • **Eurocards**: Host the pulser boards, receive power and differential signals from the
89 backplane, and incorporate the necessary circuitry for laser triggering.

90 Further details on the control system and individual electronics crate components are given
91 in Sections 9 and 10 respectively.

92 Light will be transported between the pulsers and diffusers by a series of fibre optic
93 cables; following the investigations in [1] the Thorlabs FP400URT [2] is targeted for this.
94 Due to production limitations, it is not possible to keep all fibre path lengths the same.
95 Instead there will be five different lengths: 50 m, 80 m, 106 m, 124 m and 168 m. The
96 light output after signal attenuation and dispersion in these fibres should be as consistent
97 as possible, which will require fine tuning given the different amounts of attenuation and
98 dispersion which pulses will experience based on fibre length.

99 The initial design requirements for the system are to produce pulse widths out of the
100 diffuser of no more than 10 ns, with a photon yield in the range 1–15 million photons per
101 pulse (ppp). The 10 ns limit is driven by the timing resolution of the WLS plates. The
102 wavelength of light used is also partially dictated by the WLS plates, which will not activate
103 for light above 400 nm. The photon yield target here is more of a goal than a requirement,
104 and saturation studies were performed using numbers motivated by system performance.
105 These are summarised in Section 3.

106 The below paragraph should split up. The first half has been rewritten into the above
107 paragraph, the second should be fleshed out for the photon yield test section.

108 Pulse width should ideally be between 1–10 ns and the photon count from 1–15 million
109 photons, but higher limits are preferable. The lower limits are not possible to achieve, as
110 the fibre dispersion will create a minimum pulse width, which is 4.5 ns at 180 metres, and
111 if we try to achieve large light output it will compromise our lower light output, so we can
112 only achieve around 100,000 photons per pulse at minium. While these compromises are not
113 ideal, the fibre selection limits our capabilities on hitting the required theoretical targets.

114 3 OD PMT Saturation Studies

115 4 Diffuser Design

116 4.1 ID Diffuser Hemisphere Design

117 4.1.1 Inner Detector Diffuser Design

118 The diffusers used to scatter input laser light in the inner detector volume are 2.54 cm
119 half-spheres fabricated from PTFE. This is used as it

- is unaffected by immersion in water
- acts as a excellent diffuser
- is a good transmitter of UV light
- is easy to machine and clean

A mechanical drawing of the inner detector diffuser hemispheres is shown in Figure 2

4.1.2 Diffuser Profile Measurement System

A scanning system was built to measure the output characteristics of diffuser hemispheres. Enclosed in a dark box, the diffuser is mounted onto two rotary stages which gives the freedom to rotate the diffuser around the nominal axis linking the diffuser with the photosensor. This scanner only takes scans in an air medium, and the setup is illustrated in Figure 3.

A laser powered from a wall plug is used to illuminate the diffuser with light at a wavelength of 450 nm. It is triggered by a function generator with 1000 triggers per burst at a frequency of 2 kHz. The open beam is directed via a mirror, a circulator, and a lens to the fibre launch stage, and then via an optical fibre towards the diffuser. The diffuser enclosure is fixed with three screws on the double-rotation stage. Measurements of bare diffuser profiles, i.e. without enclosure, are conducted with the bare fibre end positioned in the centre of the rotation stage using a 3D printed frame. The bare fibre end is kept in place due to friction on the connection point with the diffuser hemisphere. A photograph of the rotation stage with a bare diffuser hemisphere is shown in Figure 4.

A PMT measures the diffuser spectrum at a fixed position, with 62 cm distance to the diffuser enclosure and a 3 mm pinhole aperture, restricting the solid angle viewed by the PMT to $2 \cdot 10^{-5}$ sr. For comparison, a single 50 cm PMT in the HK far detector receives light from a point source at the other side of the tank over a solid angle of approximately $2.2 \cdot 10^{-4}$ sr. The PMT signal is digitised at a sampling rate of 2500 MHz over 1000 cycles, allowing to resolve the shape of each single signal waveform. The light yield at each coordinate is then obtained as the average waveform area across all digitised signals.

The diffuser profile measurement system is discussed in detail in [3].

4.1.3 Diffuser Power Measurement System

In addition to the profile measurement functionality, the integrated power output from the diffuser was measured using an integrating sphere from Ophir. This sphere provides an unbiased measurement of the total light output power of any light source, regardless of the shape of the emission profile. A bespoke diffuser holder suitable for connection to one of the integrating sphere ports was 3D-printed, as was a holder for the optical fibre from the laser source.

A bare PTFE hemisphere was mounted into this holder and connected into the integrating sphere port. The bare end is inserted into the connection point in the same manner as for a bare profile scan. Tape was used to prevent light leaking out of the back of the hemisphere during the measurement, which also helped to keep the fibre in place. The hemisphere was then illuminated with light from the same laser, this time running on a continuous rather than burst setting. On the continuous setting light is supplied in a sinusoidal manner at a frequency of 1 kHz. Power measurements were taken once per second for a period of ten seconds to account for small fluctuations in laser intensity, the mean of which served as the final power measurement for that hemisphere.

In order to calculate a power ratio, a measurement of power for the bare fibre also needed to be obtained. This was done in a similar manner to a power measurement for a hemisphere,

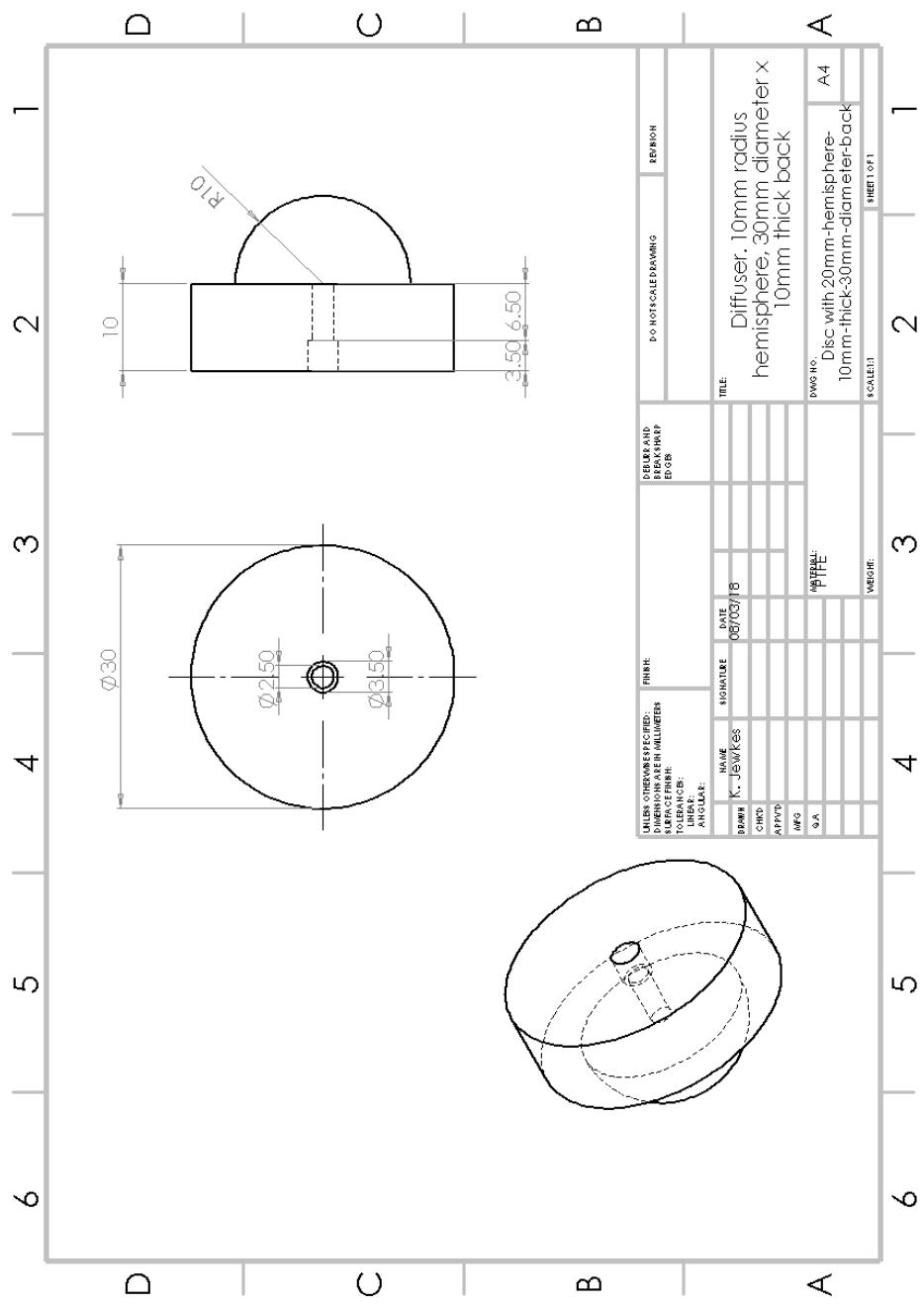


Figure 2: Bare Diffuser Mechanical Drawing

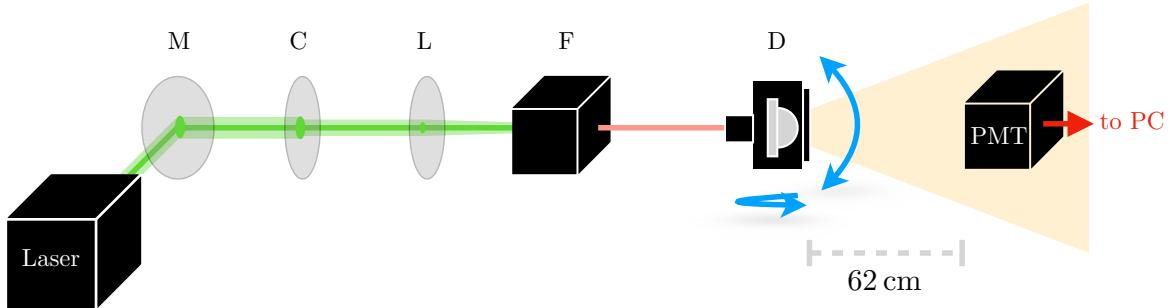


Figure 3: Setup for diffuser scans: light from the laser is directed via a mirror (M), a circulator (C), and a lens (L) to the fibre launch stage (F). From there, the light goes via an optical fibre to the diffuser (D) on the rotation stage.

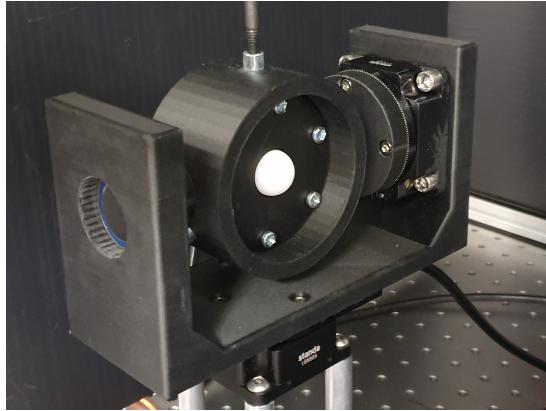


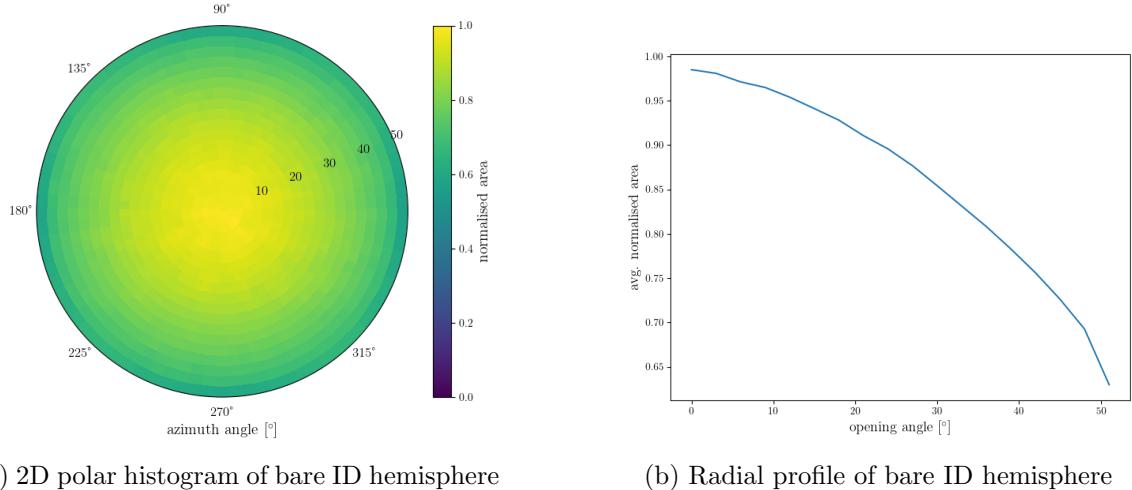
Figure 4: Rotation stage with bare diffuser hemisphere mounted using a 3D-printed frame.

165 using the same laser and data acquisition settings. To make the comparison between fibre and
 166 hemisphere measurement as accurate as possible, a special hemisphere was created with the
 167 fibre connection point extended into a hole that runs through the length of the hemisphere.
 168 The bare fibre can then be inserted all the way through until it pokes out of the front,
 169 allowing a power measurement for the bare fibre to be taken with the conditions inside the
 170 integrating sphere as close as possible to hemisphere measurements. The ratio of hemisphere
 171 power to fibre power can then be taken to determine the amount of light lost.

172 A table of systematics for the power ratio measurement is shown in Table I. Rotation
 173 refers to changing the orientation at which the diffuser is placed into the holder, and dif-
 174 fuser re-insertion refers to removing the diffuser from the holder and replacing it. Fibre
 175 re-insertions refers to disconnecting and re-connecting the fibre into the diffuser, while bare
 176 fibre refers to dis- and re-connecting the fibre when taking bare fibre measurements. This
 177 results in a total systematic of 5.3% for a diffuser measurement and 1.8% for a fibre mea-
 178 surement, and therefore an uncertainty of 5.6% in a power ratio measurement.

Systematic	Std. dev. (%)
Rotation	1.4
Diffuser re-insertion	1.0
Fibre re-insertion	5.0
Bare fibre re-insertion	1.8

Table I: Integrating sphere systematics for the power ratio measurement.



(a) 2D polar histogram of bare ID hemisphere

(b) Radial profile of bare ID hemisphere

Figure 5: Profile scan of a standard bare ID diffuser hemisphere



Figure 6: A prototype of the OD diffuser with a 2 mm top hat.

179 4.2 OD Diffuser Design

180 The original intention was to use the same diffuser hemisphere design for the OD diffusers
 181 as will be used for the ID diffusers. However, the standard diffuser emits less than 20% of
 182 the power delivered by an optical fibre. As there are a number of interfaces in the optical
 183 pathway between the light source and the diffuser, and as the light source for the OD will
 184 be LEDs, this was considered too low to be able to effectively saturate PMTs in the OD
 185 space, which is one of the primary design requirements of the system. Neither the number of
 186 interfaces in the optical chain, nor the light source can be changed easily, but it is possible
 187 that an alternate design of the diffuser hemisphere could yield more light.

188 Light is lost to two mechanisms in the standard diffuser; absorption by the PTFE and
 189 backscattering. Both loss mechanisms would be minimised if there were less PTFE in the
 190 light path. The design for the OD diffuser section was modified to be the shape of a top
 191 hat, as shown in Figure 6. The optimal depth was studied by taking profile and power
 192 ratio measurements using the same diffuser, but at smaller and smaller depths; after each
 193 measurement was completed, 2.0 mm was cut from the top-hat, and the measurements were
 194 re-taken. This procedure was repeated until the top-hat was 2.0 mm high.

195 Results of the power ratio measurements are shown in Table II. As expected, power ratio
 196 increases with decreasing top-hat depth, making the optimum depth 2.0 mm. The profile as
 197 shown in Figure 7 confirms that the shape of the profile is still suitable.

Top-hat depth (mm)	Power ratio (%)
10.0	19.2
8.0	32.4
6.0	31.5
4.0	42.1
2.0	55.2

Table II: Power ratio measurements for each depth of the top-hat

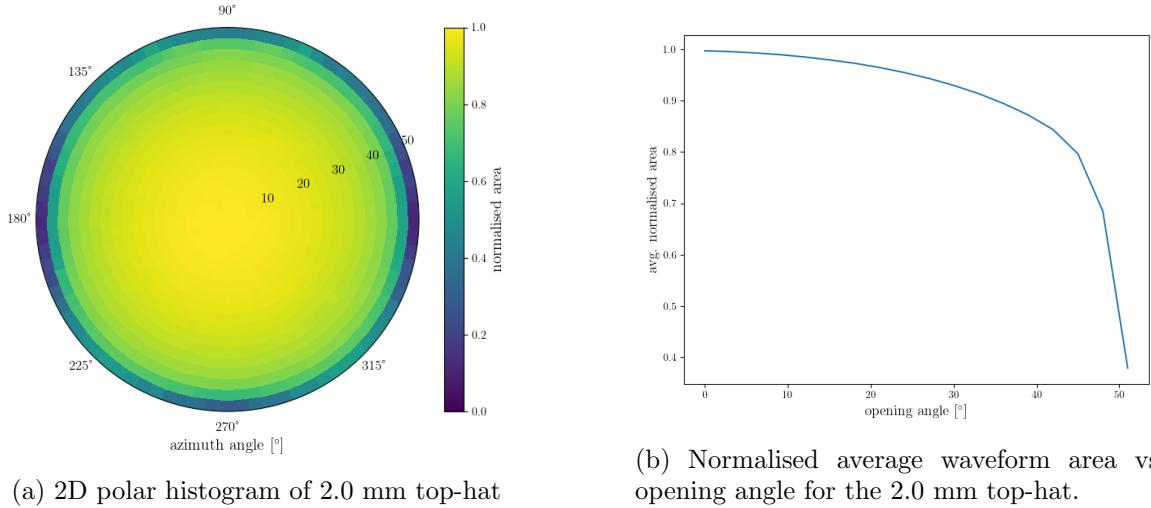


Figure 7: Profile scan of the 2.0 mm top-hat

198 Based on these studies, we propose to change the OD diffuser design from a hemisphere
 199 to a top-hat with a 2.0 mm height above the base. The diffuser will still be fabricated from
 200 PTFE, but this new design (i) emits more light at higher emission angles (ii) doubles the
 201 amount of light that is emitted for a given LED power setting and (iii) is significantly easier
 202 to fabricate in bulk.

203 5 OD Diffuser Mounting System and Installation

204 The OD space will be illuminated by a total of 122 OD diffusers, 19 on each of the top and
 205 bottom caps, and 84 in the barrel. The barrel diffusers are distributed in 7 vertical layers
 206 each consisting of 12 OD diffusers. Due to the numbers and cost, the mounting system must
 207 be relatively small, easy to fabricate and easy to install. Installation will be carried out by
 208 workers on the gondola in the OD space after the Tyvek has been installed and as the fibres
 209 are being installed. The gondola worker will install the fibre in the OD diffuser, and fix the
 210 mount to the HK frame, oriented into the OD space. Since this is being done on the gondola,
 211 the mount needs to be small, easy to store, and straightforward to install.

212 Drawings for the OD diffuser prototype mount can be seen in Figure 8 and pictures of the
 213 prototype can be seen in Figure 9. The mount is made from stainless steel and is designed
 214 to hook over a horizontal frame bar, and screw in from the bottom. The PTFE mount is
 215 approximately 5 cm on a side. The fibre will be installed from the back and is held in place
 216 by a T-shaped component that is screwed down by the gondola worker. An image of the
 217 prototype housing installed on the PMT support structure mockup next to a mechanical OD
 218 PMT and WLS plate is given in Figure 10.



Figure 8: (left) Front view of the prototype of the OD diffuser mount and (right) rear view of the prototype of the OD diffuser mount.

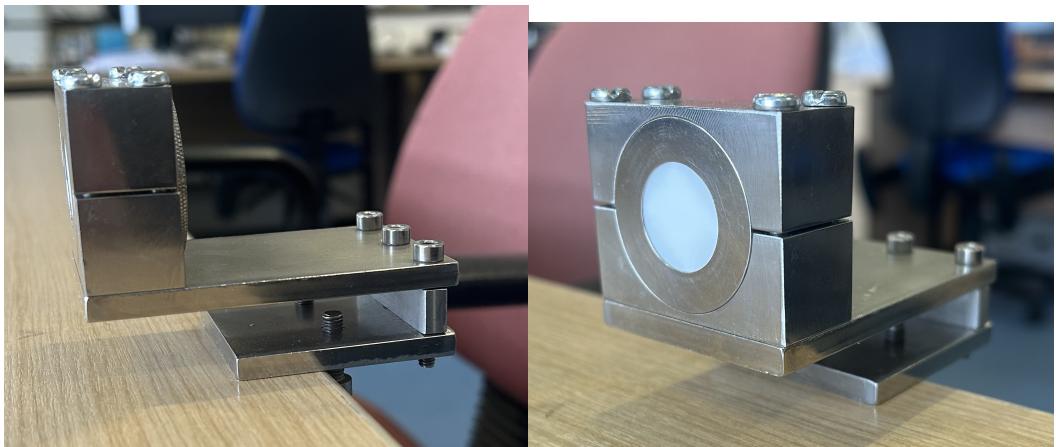


Figure 9: (left) Side view of the prototype holder and (right) front view of the prototype holder.



Figure 10: OD diffuser housing installed at the RAL mockup frame, next to an OD PMT and WLS plate.

219 **6 Pulser Board**

220 **6.1 Pulser Board Overview**

221 The pulser board was designed to be a more efficient and compact version compared to
222 Super-Kamiokande UK Light Injection system, improving on efficiency, functionality, and
223 light output. The pulser board is a rather simple board designed for low cost production.
224 This section explains each circuit, component selection and design decision. Minor changes
225 are expected from the current design, mostly centred on removing prototyping circuitry.
226 More details on the expected changes are given in Section 6.10.

227 **6.2 Physical dimensions and construction**

228 The dimensions of the Printed Circuit Board (PCB) were selected to be as compact as practicable,
229 while still providing sufficient area for the secure mounting of a fibre coupler and for
230 the components. The final board size is 50 mm × 30 mm. This configuration permits electrically
231 noisy components, such as switching power supplies and the Low Voltage Differential
232 Signal to Transistor Transistor Logic (LVDS-to-TTL) converter to be positioned at a maximum
233 distance from the switching circuitry, thereby minimising potential electromagnetic
234 interference.

235 Although it is technically feasible to further reduce the board size, preliminary design
236 studies and practical build indicated no substantial benefit in doing so. The board density
237 cannot be significantly increased inside the crate due to FPGA LVDS count and Eurocard
238 dimension, and cost analyses revealed negligible differences associated with a smaller PCB
239 footprint. Furthermore, the chosen dimensions provide an adequate area for the fibre coupler
240 and the necessary mounting holes to affix the pulser board onto the Eurocard, thereby
241 ensuring reliable optical alignment and mechanical stability. The PCB is fabricated as a four-layer
242 FR4 [4] board with a thickness of 0.8 mm, in accordance with the standard construction
243 offered by PCB Train/Newbury Electronics¹, see Figure 11. Refer to Figure 12 for the 3D
244 model of the pulser board. The Top Layer and Inner Top Layer are shown in Figure 13, and
245 the Inner Bottom Layer and Bottom Layer are likewise illustrated in Figure 14. A combined
246 view of all PCB layers is provided in Figure 15.

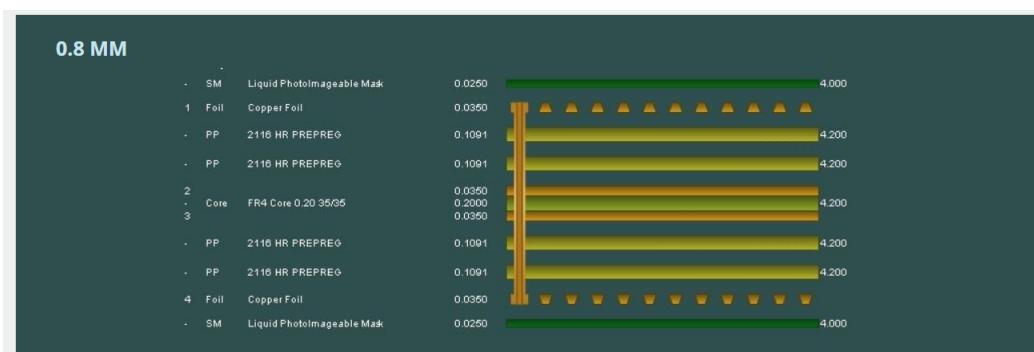


Figure 11: PCB Train's 4 Layer 0.8mm Layer Stack

¹These are trading names of the same manufacturer.

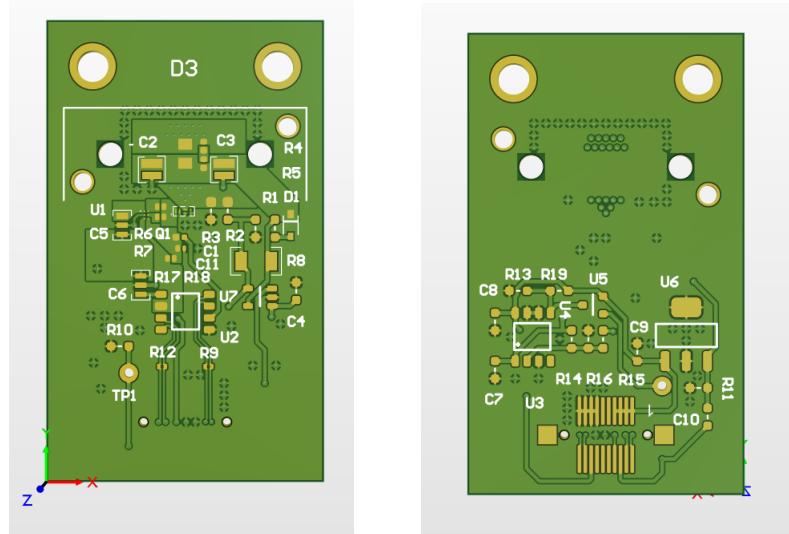


Figure 12: Pulser Board's 3D view Top and Bottom

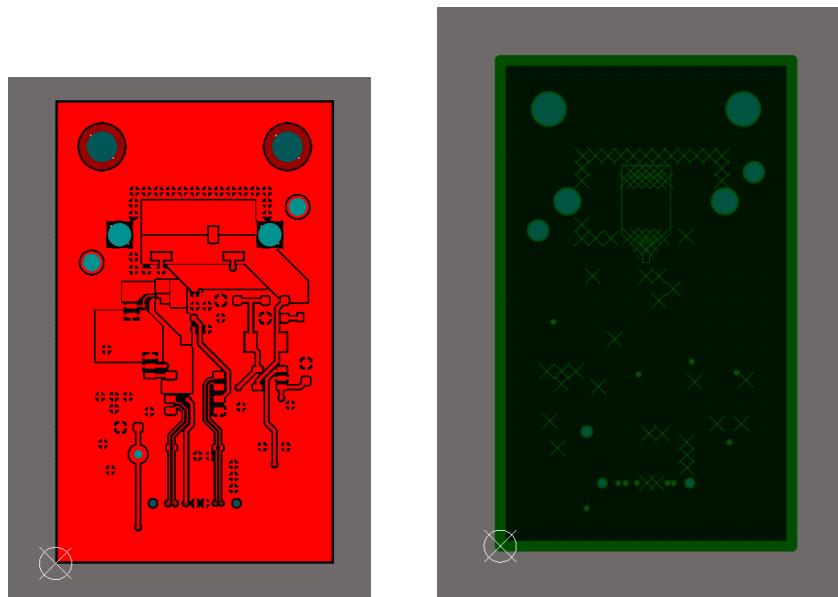


Figure 13: Pulser Board Top and Inner Top Layer

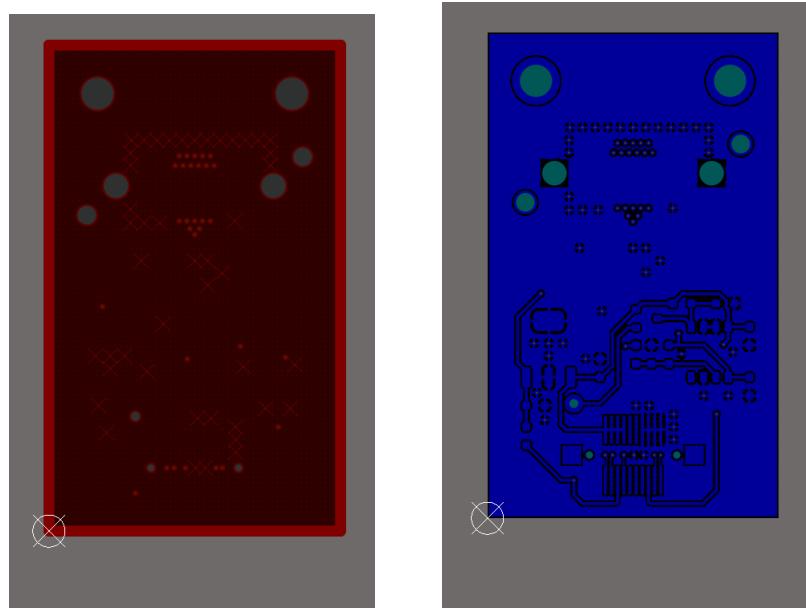


Figure 14: Pulser Board Inner Bottom and Bottom Layer

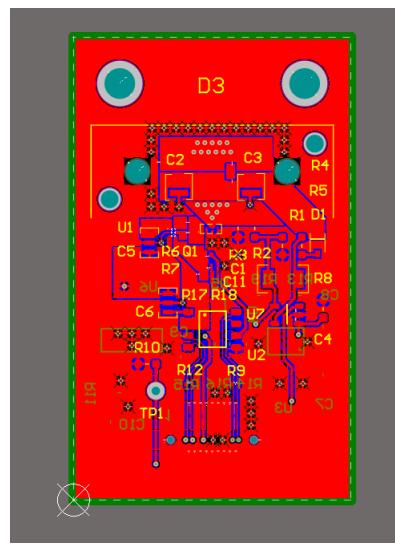


Figure 15: Pulser Board Layer Overview

247 **6.3 LED**

248 **6.3.1 Overview**

249 The LEDs are the most crucial component in the system as the characteristics of these
 250 primarily determine the light output, regardless of electronics. LEDs are usually not rated
 251 for such high-speed applications, which meant LEDs had to be tested and validated in-house,
 252 as datasheets do not provide the required information. The specification required was a 1–
 253 10 ns clean single pulse, sub-400 nm wavelength, small surface mount package, narrow output
 254 beam so it can be coupled to a fibre with reduced losses and a good range of photon output.
 255 Several LED packages were purchased from Kingbright and LC-LED, and their performance
 256 tested. The results of these tests are given in Section 6.3.4.

257 **6.3.2 Switching Circuit**

258 The redesign process provided a valuable opportunity to evaluate a revised layout and new
 259 components for the switching circuit. Several enhancements have since been implemented
 260 in the revised switching circuit. Most importantly, the switching side of the layout has
 261 been rerouted. In contrast to the previous configuration, where current would flow through
 262 the limiting resistor regardless of the LED state, the updated design only allows current
 263 flow when the LED is active (refer to Figure 16). This modification reduces both thermal
 264 dissipation and the overall power consumption of the system. To modulate light intensity,
 265 a variable power supply is now employed to adjust the voltage supplied to the LED. This
 266 method has proven highly effective. Tests were conducted at various voltage levels using
 267 the full 181 m length of optical fibre—the maximum expected in Hyper-K at the time of
 268 testing—and the resulting photon output ranged from approximately 1×10^5 to 2×10^7
 269 photons per pulse. Refined testing results are shown in Section 6.3.4. Further discussion
 270 regarding the implementation and performance of the variable voltage supply is provided in
 271 Section 6.5.

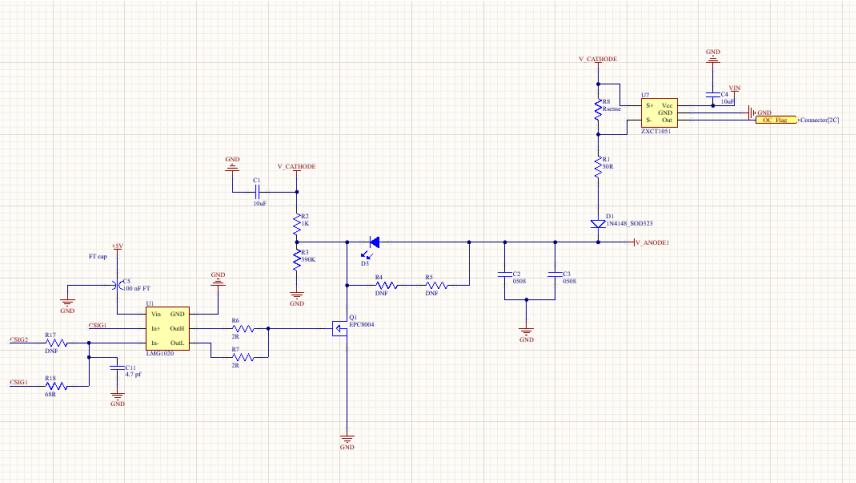


Figure 16: Switching Circuit Layout with LMG1020 and over current IC, R4 is 6.8 nH inductor and R5 is 3R3 resistor

272 **6.3.3 Switch Selection**

273 The previous iteration of the pulser board utilised a BFR92 [5] high-speed RF NPN switching
 274 transistor which was directly driven by a LVDS-to-TTL converter. In the redesign phase,

275 alternative circuit topologies were explored—particularly those suitable for generating (sub-
276)nanosecond pulses. This investigation led to the adoption of gate driver circuits. Gate
277 drivers are advantageous not only because they can power switches with challenging drive
278 requirements, but also because sub-nanosecond electrical pulses can be achieved by modu-
279 lating the enable pin with slight timing offsets.

280 The fastest commercially available gate driver identified was the Texas Instruments
281 LMG1020 [6]. This device supports pulse widths down to 1 ns, with typical rise and fall
282 times of 400 ps. Additionally, it features an enable pin that allows for precise nanosecond
283 pulse shaping ². The LMG1020 is compatible with both Gallium Nitride Field Effect Tran-
284 sistor (GaN) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) switches,
285 broadening the scope for future component integration and experimentation. It is widely
286 available and priced at £1.97 per unit in the quantities we will require for full production.

287 For the switching element, enhancement-mode GaN transistors manufactured by EPC
288 were selected due to their superior switching characteristics. This recommendation originated
289 from Nick Braam, an engineer at the University of Victoria, who contributed to the pulser
290 board design for the mPMT system. Two EPC devices were shortlisted: the EPC2012 [7] and
291 EPC8004 [8]. The EPC2012 offers a simpler footprint, which could reduce manufacturing
292 defects. However, the EPC8004 features lower parasitic capacitance, see Figure 17 for the
293 EPC2012 values and Figure 18 for EPC8004 values, leading to better high-speed performance.

294 To evaluate optical output performance, a 40 m length of FP400URT [2] optical fibre,
295 a Mouser-sourced 385 nm LED (ATS2012UV385 [9]), and a Hamamatsu H10721-210 [10]
296 PMT were used. The EPC-based configurations exhibited nearly identical pulse shapes,
297 whereas the BFR92-based circuit’s pulse shape was less sharp at identical pulse widths, as
298 shown in Figure 19. Consequently, the EPC8004 (Figure 20) was chosen for implementation.
299 Optimal performance of the EPC GaN switches required careful layout considerations. A
300 layout was developed in accordance with EPC’s design guidelines [11], targeting minimal
301 parasitic inductance and capacitance. The design employs two layers placed directly above
302 one another, utilising large copper planes and multiple vias to ensure uniform current dis-
303 tribution. The PCB will be fabricated and assembled by PCB Train, using their 0.8 mm
304 thick, four-layer stack-up, which offers minimal inter-layer separation for optimal electrical
305 performance (Figure 11). This same layout strategy was applied to the BFR92 circuit to
306 provide a fair performance comparison.

307 A significant challenge at low pulse widths is the presence of a trailing edge or “tail” in
308 the LED output. This effect arises due to charge accumulation and the intrinsic capacitance
309 of the LED, resulting in extended decay times and pulse broadening (see Figure 21). To
310 mitigate this, a parallel modified snubber circuit was implemented, consisting of a 6.8 nH
311 inductor and a 3.3 Ω current-limiting resistor. Upon LED turn-off, the inductor generates an
312 electromotive force (EMF) that actively extracts residual charge from the LED, accelerating
313 its shutdown. The effectiveness of this approach is illustrated in Figure 22. Additionally,
314 two 0508 reverse-topology 100 nF capacitors have been incorporated. Their role is to act as
315 local energy reservoirs, providing rapid current delivery to the LED during pulse operation,
316 surpassing the response time of the main power supply.

317 6.3.4 Testing

318 For testing purposes, the previous-generation United Kingdom Light Injection (UKLI) moth-
319 erboard and associated software were utilised in conjunction with a prototype of the next-
320 generation pulser board. This prototype consisted of four distinct circuit variants: one
321 employing the EPC8004 switch, another utilising the EPC2012 switch, a third using the

²See page 12 and 13 in [6].

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)					
C_{ISS}	$V_{\text{DS}} = 100\text{ V}, V_{\text{GS}} = 0\text{ V}$		128	145	pF
C_{OSS}			73	95	
C_{RSS}			3.3	4.4	

Figure 17: EPC2012 Capacitance Values IC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics[#] ($T_j = 25^\circ\text{C}$ unless otherwise stated)					
C_{ISS}	$V_{\text{GS}} = 0\text{ V}, V_{\text{DS}} = 20\text{ V}$		45	52	pF
C_{OSS}			23	34	
C_{RSS}			0.8	1.3	

Figure 18: EPC8004 Capacitance Values IC

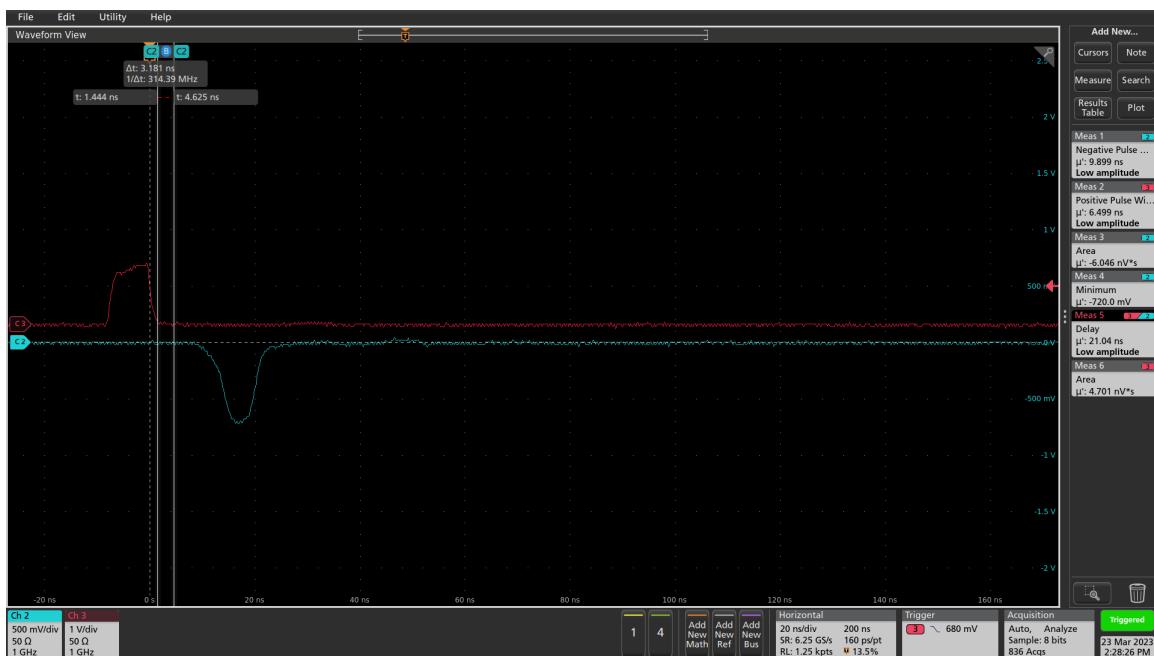


Figure 19: BFR92 Pulse Shape

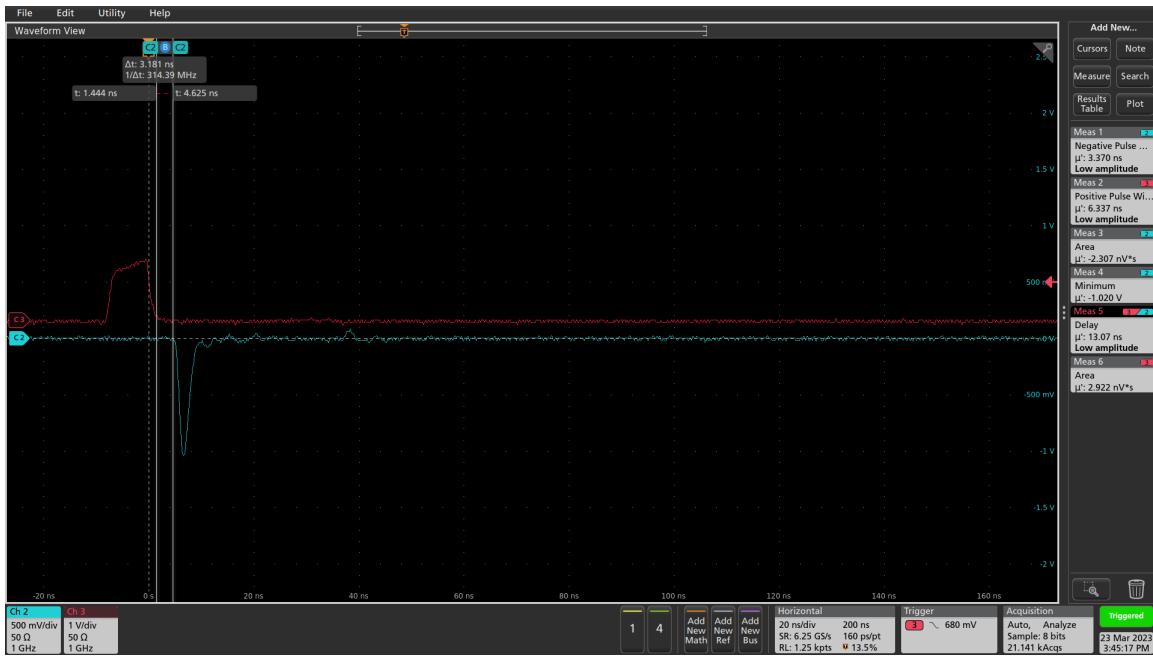


Figure 20: EPC8004 Pulse Shape

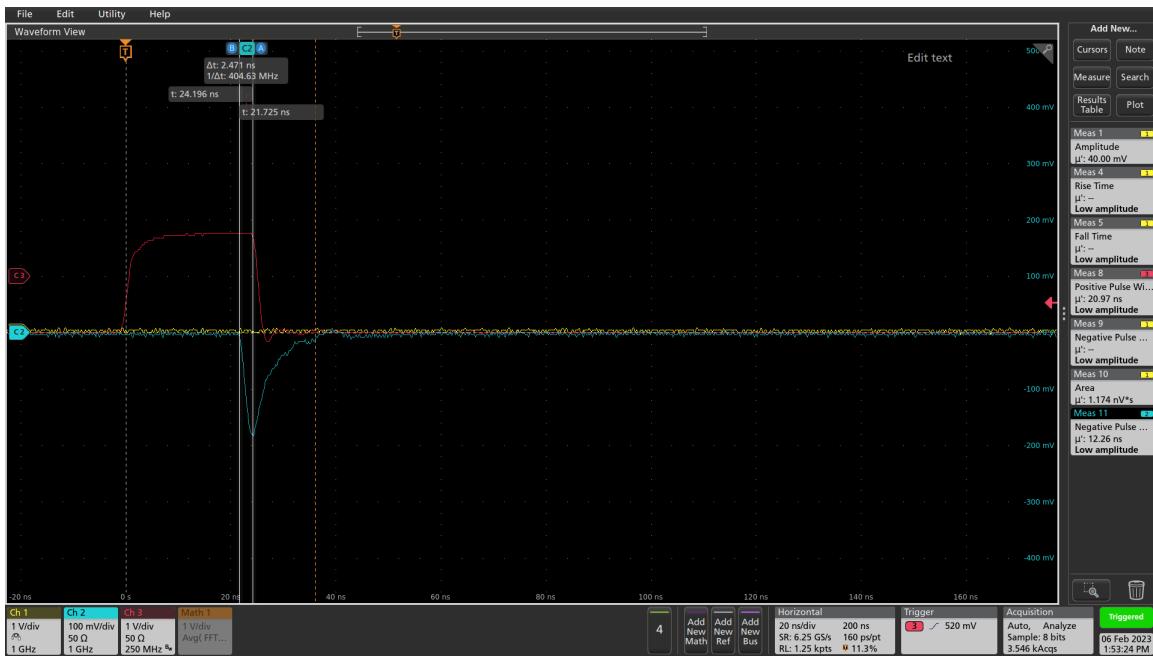


Figure 21: Pulsing Circuit With No Inductor and Resistor

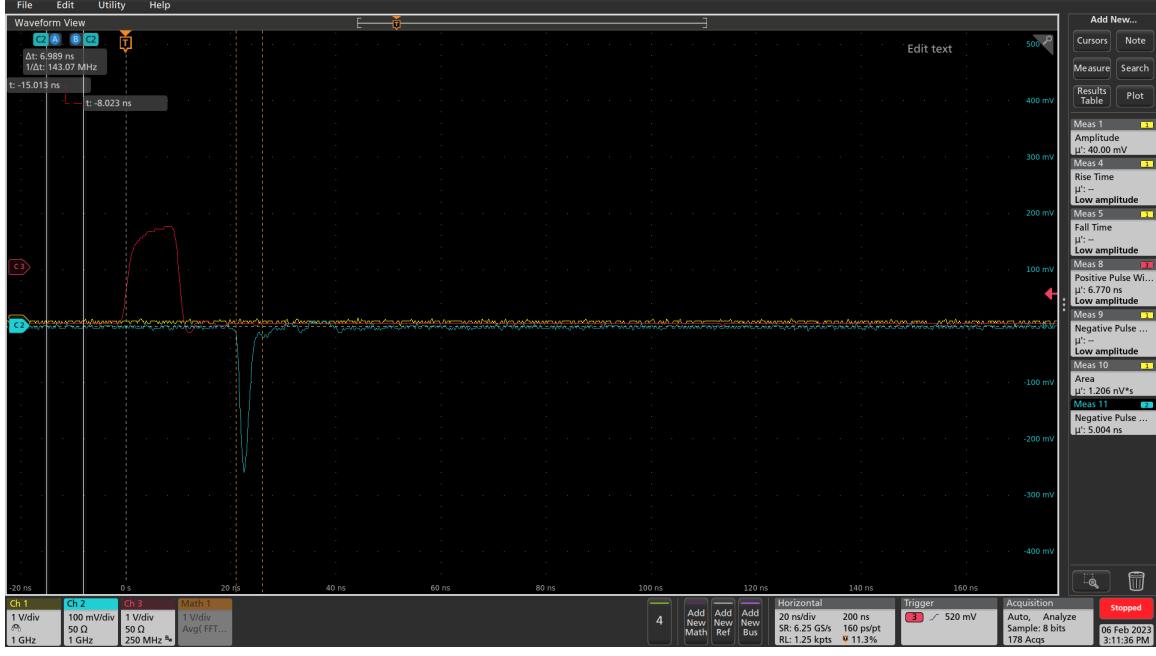


Figure 22: Pulsing Circuit With Inductor and Resistor

322 same high-speed transistor (BFR92) as implemented in the legacy system, and a fourth vari-
 323 ant incorporating an EPC2012 gate in a through-hole package instead of the standard 0805
 324 surface-mount footprint. Further evaluation was also performed using the latest pulser board
 325 prototype once they had arrived.

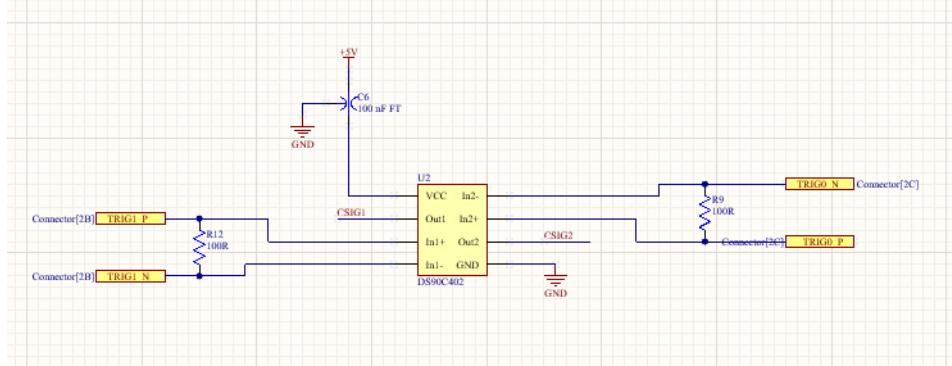
326 Following comparative performance evaluations, the configuration using the EPC8004
 327 switch was selected for continued use. While both the EPC8004 and EPC2012 switches ex-
 328 hibited similar electrical characteristics, the EPC8004 offered superior performance due to
 329 its lower parasitic capacitance, without any additional cost. The pulser board assembly was
 330 housed within a dark box during testing, and a 3D-printed fibre coupler was employed to
 331 facilitate light delivery. The initial focus of the evaluation was on the shape of the gener-
 332 ated optical pulse. During component selection, it was observed that the LED previously
 333 sourced from Mouser (ATS2012UV385 by Kingbright) provided acceptable performance in
 334 terms of electrical characteristics, but the optical output was suboptimal. Additionally, this
 335 LED was found to be out of stock and obsolete at the time after testing, precluding further
 336 procurement. Subsequently, four ultraviolet LEDs from LC LED were assessed—two emit-
 337 ting at 365 nm and two at 395 nm—each in both 0805 and 0603 surface-mount packages.
 338 Results demonstrated that the 0805 package LEDs provided significantly better optical cou-
 339 pling efficiency with the FP400URT optical fibre. Furthermore, the 365 nm variant exhibited
 340 superior optical power output relative to the 395 nm counterparts. Based on these findings,
 341 the LC LED UT-67UV365P [12] 365 nm LED was selected as the most suitable LED for this
 342 application.

343 6.4 LVDS to TTL Converter

344 The DS90C402 [13] from Texas Instruments was selected as the LVDS-to-TTL conversion
 345 solution. This device is a dual-channel converter, chosen primarily for its fast switching
 346 characteristics—offering both rise and fall times of approximately 500 ps. It operates at
 347 5 V and provides 5 V TTL output levels, which aligns well with the requirements of the
 348 downstream switching circuitry. The inclusion of two channels is particularly advantageous,

as it enables the generation of sub-nanosecond differential pulses by precisely offsetting the channels, as described in Switch Selection. Among commercially available devices with these specifications, the DS90C402 is the fastest and is readily available through multiple distributors.

The associated circuit was implemented in accordance with the manufacturer's recommendations provided in the datasheet. A decoupling capacitor was placed in close proximity to the power supply pin to minimise voltage ripple. Output traces were routed using polygon fills to reduce impedance and enhance signal integrity, and a continuous ground plane was placed beneath the signal layers to improve shielding and minimise electromagnetic interference. The schematic for this is given in Figure 23.



6.5 Power Supplies

Each pulser board is required to incorporate a variable voltage power supply dedicated to driving the LED, with an adjustable output range from 3 V to 12 V. This supply is used exclusively to modulate the LED's light output by varying the forward voltage, and consequently the current. The design specification also necessitates that the power supply be remotely controllable—i.e., capable of being switched on or off via a simple logic-level signal.

For this purpose, the LT1963A [14] adjustable low-dropout linear regulator was selected. This regulator has demonstrated reliable performance in previous pulser board iterations and offers a favourable balance of cost-effectiveness and controllability. The implementation includes standard filtering and decoupling, with layout details provided in Figure 24. The schematic provided in Figure 25 is an early version used for prototyping; the adjustable circuit has been simulated and will be tested shortly, and the enable circuit has been tested, modified and simplified. Updated schematics will be provided with v1.0 circuit.

In addition to the variable LED supply, each board requires a stable 5 V supply to power both the DS90C402 LVDS-to-TTL converter and the LMG1020 gate driver. Unlike the LED supply, this rail remains continuously powered. The 5 V supply is provided by an LM2937-5 [15], a fixed-output linear voltage regulator, which has been successfully employed in various high-speed and low-noise applications within the laboratory. The associated circuit schematic and layout and schematic are shown in Figures 26 and 27 respectively.

To meet system-level design constraints, each pulser board is equipped with its own independent 12 V input supply, ensuring that LED output intensity can be individually controlled on a per-board basis. However, the 5 V supply is common across all boards and derived locally on each pulser module. This approach allows for localised filtering and minimal power distribution path lengths, reducing the risk of noise coupling and voltage

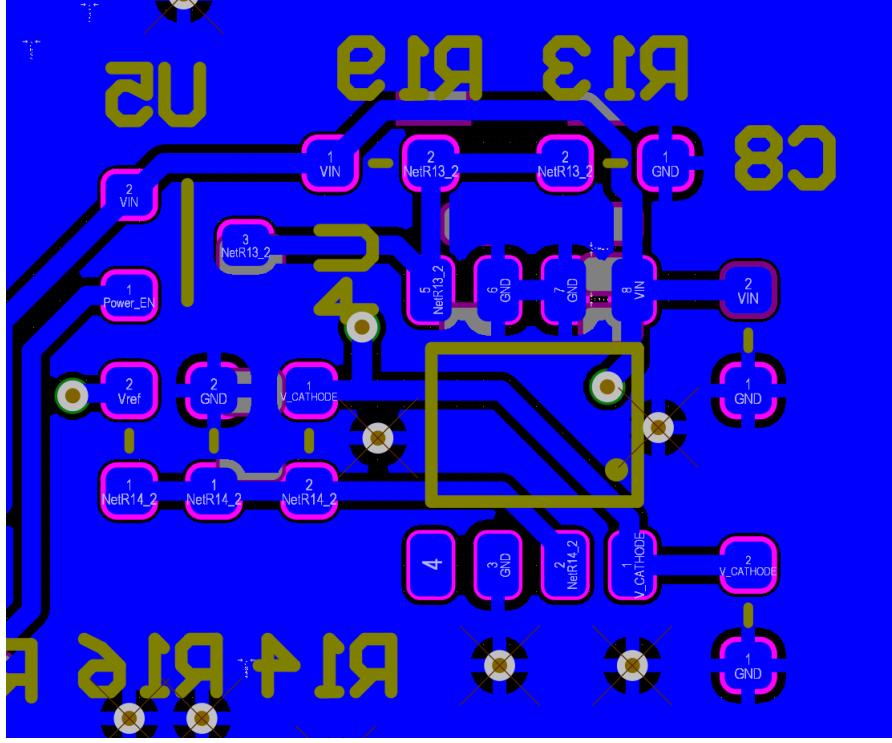


Figure 24: LT1963 Layout

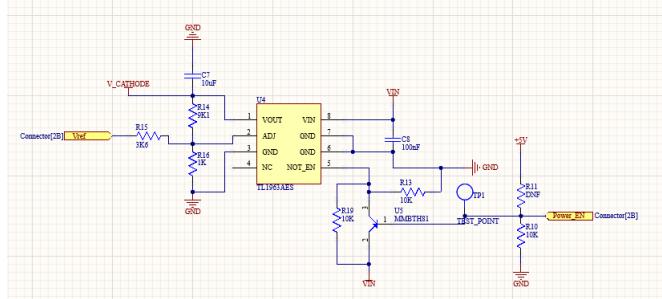


Figure 25: 12V Circuit Schematics

drop considerations that are particularly critical in high-speed circuit applications.

Power is supplied to each board via the Eurocard backplane. The 12 V input from the Eurocard simultaneously feeds both the variable (LED) and fixed (logic) power regulators on the pulser board. The LED enable function is controlled via a 5 V logic signal originating from the Eurocard's GPIO interface. Additionally, a DAC output from the Eurocard provides a voltage control signal to the adjustment pin of the LT1963A regulator on each pulser board, thereby allowing precise, programmable control of light intensity.

6.6 Connector

The previous board connector was deemed too bulky and expensive for the larger number of channels needed in this system, leading to the process of finding a more suitable alternative. Following an evaluation of commercially available options, the Phoenix Contact female connector 1331962 [16] was selected. This connector offers several advantageous specifications: it is rated for 500 V, features a low contact resistance of $40\text{ m}\Omega$, supports a maximum current of 0.5 A, and is capable of signal transmission up to 20 Gbit s^{-1} . In addition, it is

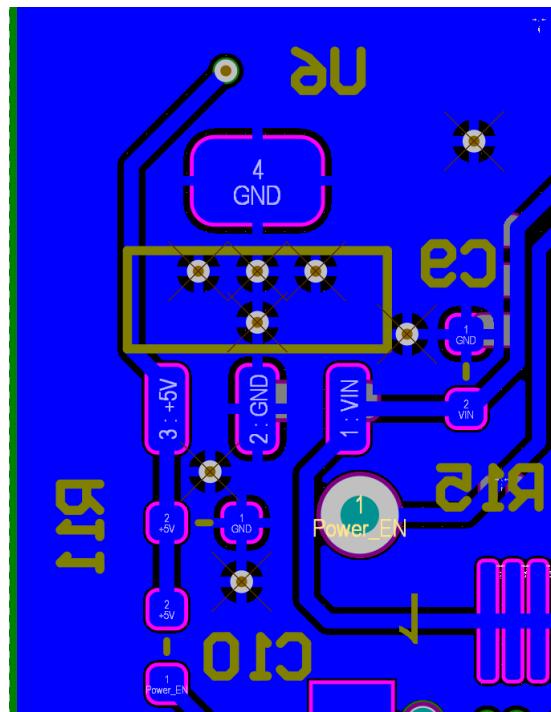


Figure 26: LM2937-5 Layout

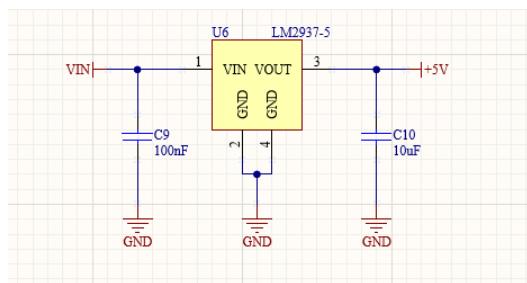


Figure 27: 5V circuit schematics

cost-effective, priced at approximately £0.50 per unit, with wide availability ensuring ease of procurement. Multiple height variants are available within the same series, facilitating flexible mechanical integration within the Eurocard crate system. The compact footprint of the connector allows for a reduced PCB form factor. Electrically, the high-frequency performance supports reliable LVDS signal transmission. Additionally, the compact footprint of the connector is well-suited to space-constrained PCB layouts.

An illustration showing the connector and corresponding circuit layout is provided in Figure 28.

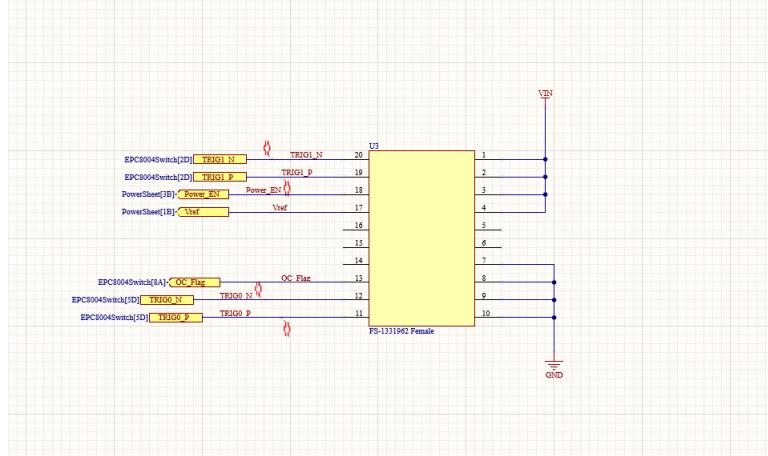


Figure 28: Connector Schematics

6.7 Fibre Coupler

During the prototyping phase, improvements were made to the PCB layout to better accommodate a fibre coupler. As a result, the current design includes provisions for precise mechanical mounting and alignment. Specifically, two mounting holes for M2 screws have been incorporated, enabling the 3D-printed coupler to be firmly secured to the board (see Figure 29). In addition, two dowel holes have been added to guide the coupler into position, ensuring accurate alignment over the LED. Given the tolerances associated with PCB fabrication and 3D printing, an alignment accuracy of approximately 100 µm is expected.

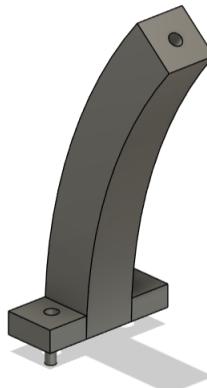


Figure 29: Fibre Coupler Design

To optimise the electrical path, capacitors have been repositioned as close as possible to

415 the LEDs. This minimises parasitic inductance and resistance, while enabling a centralised
 416 layout of larger components. The resulting configuration creates a compact chamber housing
 417 both the LEDs and associated capacitors.

418 The design for the fibre coupler is modular, consisting of three components: a base
 419 section mounted to the pulser PCB, a top section into which the fibres will be epoxied, and
 420 an intermediate attenuator element. The latter part will be added to the current design to
 421 space the fibre from the LED and thereby adjust the optical coupling efficiency to achieve
 422 required attenuation, accounting for the different lengths of fibre in the system. This means
 423 the attenuation will be implemented within the coupler itself, allowing the LED output to
 424 remain within the electronically controlled dynamic range.

425 The fibre coupler will be fabricated via stereolithography (SLA) using a black resin to
 426 minimise light transmission through the material. Additional light-tight testing will be
 427 conducted, and black paint may be applied if further sealing is required. Furthermore, laser-
 428 cut rubber gaskets will be introduced at interface points to ensure optimal optical isolation
 429 and mechanical sealing.

430 6.8 Photon Yield Tests

431 tests on maximising photon yield and available dynamic range should be fully described here

432 6.9 Production

433 Production will be carried out using PCB Train as they are local and competitively priced,
 434 and known to produce boards of good quality. Estimated cost is £12.27 per board, which
 435 equates to £1,496.94 for 122 units or £1,840.5 for 150 units, and production is £4073.48 for
 436 122 units for 15 days lead time, or £3985 for 150 units at 25 days lead time. The full cost
 437 breakdown is shown in Figure 30

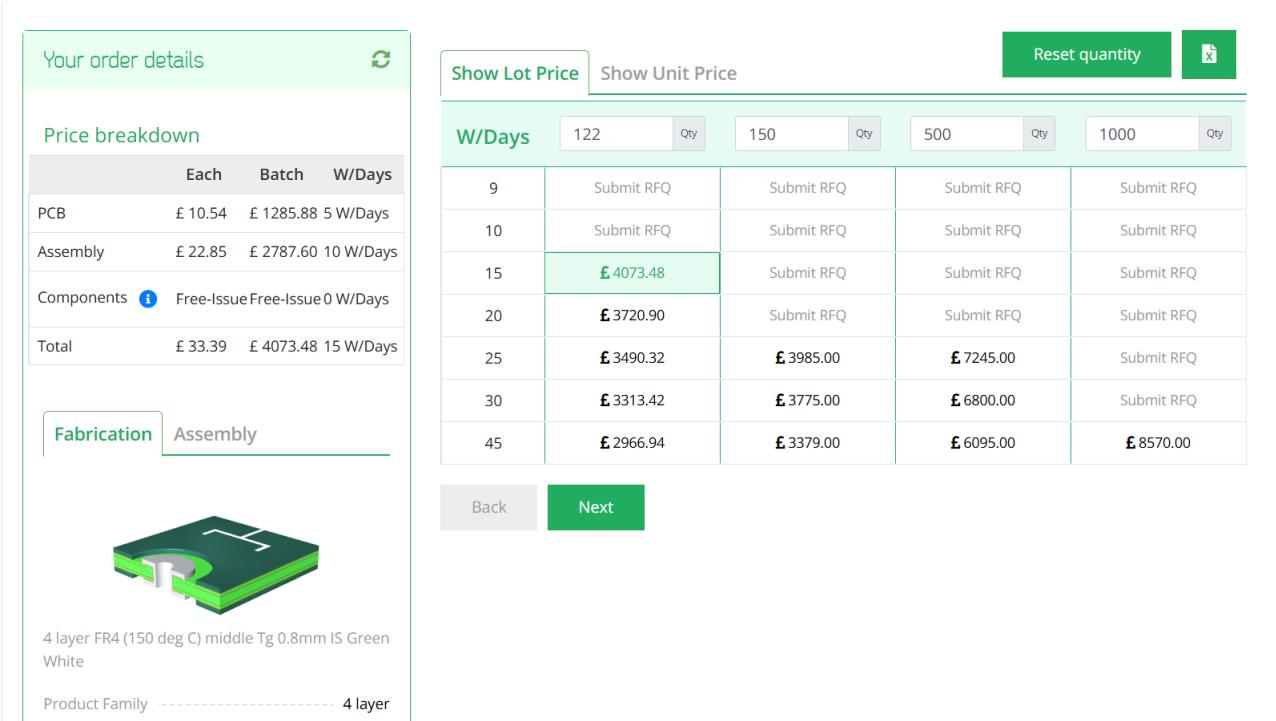


Figure 30: PCBTrain PCB production and assembly costs

438 **6.10 Changes Expected from v0.9 to v1.0**

439 **6.10.1 LED and Switching Circuit**

440 There will be minimal changes to the LED and switching circuit. Changes will be made to
441 the position of the switching devices, placing them slightly closer to each other to reduce
442 transmission line length. The LED will likely remain as the LC LED UT-67UV365P 365nm
443 0805 LED, but further LED tests will be performed. This takes a short amount of time, and
444 may lead to discovering better LEDs in the future which would be easy to swap in due to
445 standardised footprints.

446 **6.10.2 LVDS-to-TTL converter**

447 No changes are expected to this circuit.

448 **6.10.3 Power supplies**

449 Reverse voltage bias will be removed as no difference between normal and reverse bias was
450 observed photon output. The overcurrent protection and power enable circuit will be re-
451 worked.

452 **6.10.4 Connector**

453 No changes are expected to this.

454 **6.10.5 Fibre coupler**

455 A brand new fibre coupler will be designed due to the recent requirement changes regarding
456 the different fibre lengths.

457 **7 Server Rack and Cooling**

458 To house the electronics for the LI systems, two 42U server racks with 800 mm depth will
459 be used. The front of the server rack will be used for electrical connections and displays,
460 and the reverse/internal will be used only for fibre routing. The server racks will include
461 Uninterruptible Power Supplies (UPS) for safe power delivery and for power processing, to
462 avoid issues with potential instabilities in the main power supply. Each rack will include an
463 air conditioning unit to have a controlled temperature and remove humidity from the air,
464 as the relative humidity in the air is expected to be above 70%. Although specific tests on
465 running the LED electronics in humid conditions have not been carried out, it is known that
466 the optical switches for the laser calibration system requires lower humidity levels. In order
467 to simplify things and remove the potential of humidity issues with the LED electronics,
468 both server racks will be air conditioned. These systems are widely available and will be
469 chosen closer to installation.

470 **8 LED Monitoring**

471 To monitor the light output from the LEDs before attenuation by fibres and convolution
472 with water parameters, PMTs will be placed near to the LED sources. This is a similar
473 design to what is currently used in the Super-K UKLI system. Each LED connector will
474 feature a second fibre to take light to a series of PMTs, which are expected to be Hamamatsu
475 H10721-210. Due to the 8 mm diameter of the PMT window, up to 16 fibres can be attached,

476 meaning one PMT can monitor up to 16 LED boards at once. Each PMT will be powered
477 by a unique low cost power supply developed for the SK UKLI system. These will be housed
478 in a small 2–3 U server rack. The signals from the PMTs will then go to the dedicated HK
479 electronics channels that are set up for monitoring.

480 9 Control System for LEDs

481 The LEDs are driven by a differential LVDS signal originating from the FPGA. The FPGA
482 in use is the Genesys 2 [17] development board, which operates a pulsing VHDL module
483 clocked at 300 MHz. Pulses are generated on the rising edge of this clock, and toggling the
484 output (i.e., asserting and then deasserting the trigger) requires a minimum of two clock
485 cycles. Consequently, the shortest achievable pulse duration in this configuration is 3.3 ns.

486 One of the main limitations of this setup is the coarse time resolution: pulse durations
487 are effectively constrained to integer multiples of 3.3 ns. To achieve a broader and more
488 finely resolved spectrum of optical injection into the detector, improved temporal precision
489 is necessary. This is accomplished using the Xilinx **IODELAY** primitive, originally designed for
490 high-speed interface timing alignment. The **IODELAY** module permits fine-tuning of signal
491 timing to account for PCB trace mismatches, and in this application, it is repurposed to
492 introduce controlled delays between pulses.

493 To generate shorter pulses, two identical signals are created, one of which is delayed
494 using **IODELAY**. These signals are then combined using a logical AND operation, producing
495 a narrower pulse. Since the **IODELAY** module requires one clock cycle to process the input,
496 both signals—regardless of whether they are delayed—must pass through an **IODELAY** stage
497 to ensure temporal synchronisation.

498 Conversely, to produce longer pulses, the same methodology is applied, but the signals are
499 combined using a logical OR gate instead. This approach extends the pulse width beyond the
500 base clock resolution, enabling pulse durations ranging from approximately 1.5 ns to 4.5 ns
501 in 49 discrete steps. The lower bound is determined by the threshold of the LVDS-to-TTL
502 converter, which does not respond to pulses shorter than approximately 1.5 ns .

503 For channels using the longest optical fibres, this extended range is sufficient, given
504 the intrinsic dispersion in the fibre optics of around 5 ns. However, shorter fibres require
505 additional pulse shaping. To this end, an additional mechanism is implemented using a **for**
506 loop structure within the FPGA logic. This allows the pulse to persist for multiple clock
507 cycles, effectively producing longer pulses by repetition. However, due to FPGA architecture
508 constraints, each iteration of the loop consumes a clock cycle, necessitating careful timing
509 control. For instance, to produce a 6.6 ns pulse, the loop must be configured for two cycles,
510 accounting for the loop overhead.

511 Further refinement is under investigation through the daisy-chaining of multiple **IODELAY**
512 modules. This would enable sub-nanosecond granularity by introducing additional interme-
513 diate delay steps. While promising, this technique requires further validation and testing.

514 The pulse control data structure is currently under development. There are two types
515 of pulse description considered. In the first option, the software interface would require two
516 parameters per channel: a *coarse* step and a *fine* step, reflecting the approach used in the SK
517 system. The other option would be just a single variable and then simple logic turning that
518 variable into the *coarse* and *fine* step that the internal logic requires. Two hardware modules
519 are planned: one for generating the single shortest possible pulse (to minimise latency), and
520 another for multi-cycle pulses using programmable duration. A selection logic will assess the
521 input and route it to the appropriate module based on the desired pulse characteristics.

522 Each LED channel will be controlled independently, allowing for unique pulse configu-
523 rations across channels. The global trigger will be derived from the system clock, and each

524 channel will pulse in a predefined sequence while triggered from the global trigger. This
525 architecture also supports simultaneous pulsing of multiple channels. Should asynchronous
526 behaviour be required, additional per-channel delay logic can be implemented. Given the
527 five distinct fibre lengths used in the system, each channel group will also include a config-
528 urable delay offset to compensate for propagation time differences. These group delays will
529 be calibrated and fixed, with the option of fine-tuning individual channels post-deployment
530 if necessary.

531 The FPGA programming remains in active development. Inter-crate communication
532 protocols and synchronisation are currently under integration and testing.

533 10 Crate Electronics

534 10.1 Overview

535 The system specification calls for control of up to 122 LED channels, significantly exceeding
536 the channel counts used in current systems such as Super-Kamiokande or LUX-ZEPLIN,
537 which the previous generation of pulser boards are used for. To manage this complexity, the
538 design prioritises ease of use, maintainability, and straightforward deployment, particularly
539 given that the server racks will accommodate hundreds of optical fibres.

540 To achieve this, a system concept originally developed by ATLAS collaborators (specifically
541 by Ashley Greenal) has been adapted. The original design utilises a Genesys 2 FPGA
542 integrated into a half-width Verotec KM6-2 [18] Eurocard-compatible crate for testing purposes.
543 This concept has been extended to a full 19-inch rack width, enabling the integration
544 of up to 36 pulser boards within a single crate.

545 Each FPGA is capable of interfacing with up to 38 pulser boards, thereby maximising
546 the utilisation of available LVDS differential pairs, with an additional pair reserved for the
547 laser trigger signal. This configuration ensures full use of the Genesys 2's I/O capacity while
548 maintaining flexibility for future expansion.

549 The system architecture consists of three primary components: the Blade (Section 10.2),
550 Backplane (Section 10.3) and Eurocard (Section 10.4). This modular approach ensures
551 scalability and facilitates debugging, replacement, and upgrades. It also provides a robust
552 foundation for managing high channel counts while maintaining signal integrity and synchro-
553 nisation across the system.

554 10.2 Blade

555 The Blade is a simple, eight layer board, that has a SEAM-40-06.5-L-10-2-A-K-TR [19]
556 connector which is a direct fit for the Genesys 2's FMC connector. It features a PCIE 16X
557 connector at the edge for connectivity to the Backplane. The PCIE was selected by Ashley
558 Greenal as it is a well documented standard connector and there are a large amount of
559 connectors available that can be bought easily. While PCIE connectors are being used, the
560 PCIE standards for communication are not. This is a very dense PCB with all the differential
561 tracks on it, so buried vias and multiple layers will be used. See Figure 31 for a work in
562 progress version.

563 10.3 Backplane

564 The Backplane serves two primary functions: the distribution of differential signals from the
565 Blade to the Eurocards, and the reception and distribution of power throughout the crate
566 system. It accepts external power inputs of 12 V and ± 5 V, and includes a basic regulation
567 circuit to stabilise these supply voltages for downstream use.

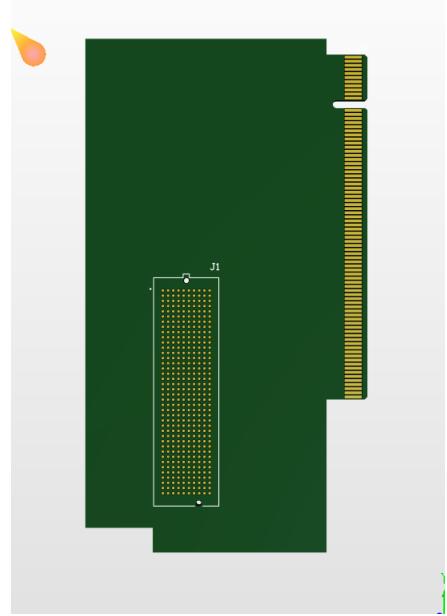


Figure 31: Blade Work in Progress

Given the mechanical constraints and routing complexity, the Backplane is implemented as a four-layer PCB with impedance-controlled traces to ensure signal integrity across all differential pairs. It features a single PCIe x16 connector to interface with the Blade, and three PCIe x8 connectors to interface with the Eurocards.

The Eurocards are positioned at slots 2, 8, and 64 within the crate. This arrangement creates two symmetrical chambers with 48 units spacing between cards, ensuring adequate space to accommodate the minimum long-term bend radius of the FP400URT optical fibres. This layout balances mechanical reliability with signal routing efficiency and supports long-term maintainability of the system. See Figure 32 for a work in progress version.

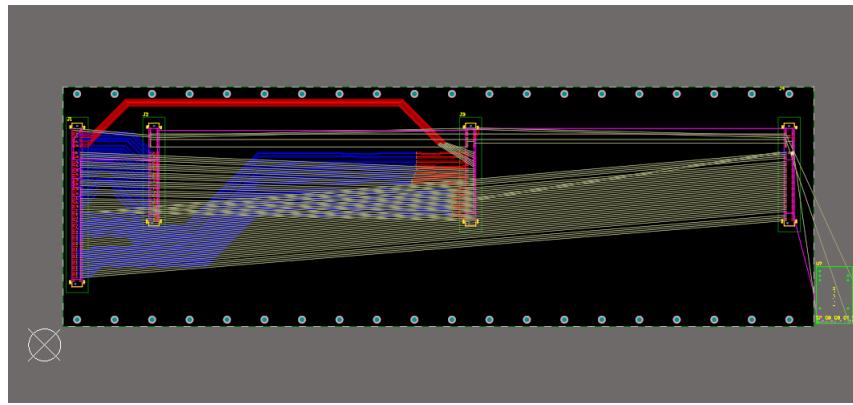


Figure 32: Backplane Work in Progress

10.4 Eurocard

The Eurocard format defines the physical and electrical standard for the crate system, hence the naming convention. Each Eurocard is equipped with a PCIe x8 connector for interfacing with the Backplane, and is designed to host up to 18 pulser boards—nine mounted on each face. Pulser boards connect via FS-1332120 Male[20] connectors, and each socket includes

582 two mounting holes for mechanical standoffs.

583 The board layout on each side consists of two staggered rows: five sockets in the back
584 row and four in the front. The two faces are laterally offset by approximately 10 mm to
585 prevent interference or fibre clashes when the system is fully populated and enclosed within
586 the crate chamber. This offset ensures smooth fibre routing and accommodates the bend
587 radius requirements of FP400URT fibres.

588 Power distribution within each Eurocard is handled by a THD 12-1212 [21]12 V DC-DC
589 regulator. This regulator provides local power isolation for the pulser boards and includes
590 a control pin connected to a PCA9698 [22] 40-pin GPIO expander. This allows for system-
591 level control, enabling or disabling all pulser boards on a card—an essential feature during
592 power-up, especially when the FPGA may inadvertently drive all differential outputs high
593 during reprogramming.

594 The GPIO expander is responsible for enabling the local 12 V regulator and for selectively
595 powering individual pulser boards. This facilitates fault isolation and power savings in
596 channels that are inactive or disconnected. Additional GPIO pins are assigned to monitor
597 output voltage levels via the overcurrent sensing circuitry.

598 To provide per-channel LED power control, an AD5673 [23] DAC is included. It out-
599 puts analogue control voltages to the onboard adjustable regulators on each pulser board,
600 allowing for independent LED drive voltage per channel. Both the GPIO and DAC devices
601 communicate with the system over the I²C protocol.

602 For laser synchronisation, the Eurocard includes a differential-to-NIM conversion stage.
603 This consists of an LVDS-to-TTL converter identical to that used on the pulser boards,
604 followed by a TTL-to-NIM converter. This ensures compatibility with legacy NIM-based
605 timing systems used in external laser triggering. See Figure 33 for a work in progress version.

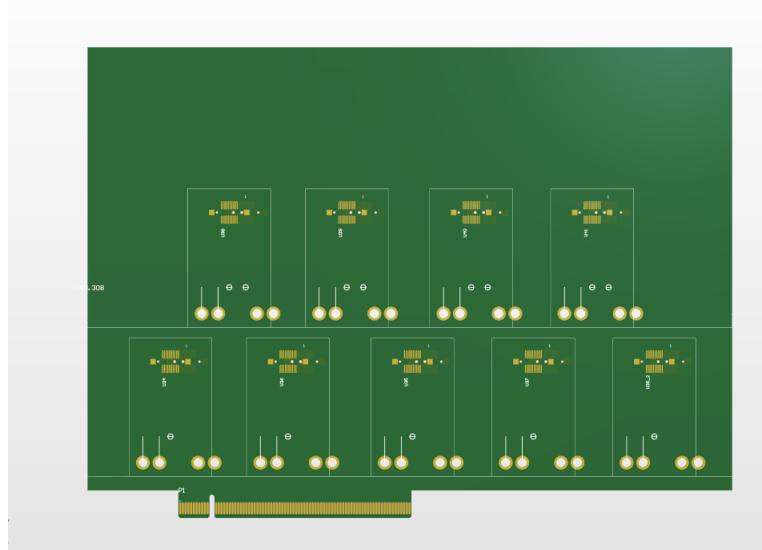


Figure 33: Eurocard Work in Progress

606 11 Conclusions

607 Write this

608 **References**

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