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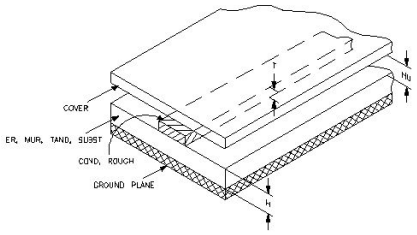
Characterizing the Substrate

In order to design a great filter in the microwave spectrum small details become increasingly important. A distributed element filter relies heavily on the characteristics of the substrate. Thankfully using ADS we can model these characteristics and change them easily. There are many options in ADS, but the basic simulation in ADS requires us to know the conductivity, height, thickness and relative permittivity.



Name	Description
H	Substrate thickness
Er	Relative dielectric constant
Mur	Relative permeability
Cond	Conductor conductivity
Hu	Cover height
T	Conductor thickness
TanD	Dielectric loss tangent
Rough	Conductor surface roughness; RMS value; refer to note 7

Figure 1 – ADS MSub Parameters[5]

Fortunately the sample we obtained from Rogers Corporation has a very detailed datasheet. [6]

Standard Thickness	Standard Panel Size	Standard Copper Cladding
RO4003C: 0.008" (0.203mm), 0.012 (0.305mm), 0.016"(0.406mm), 0.020" (0.508mm) 0.060" (1.524mm) RO4350B: *0.004" (0.101mm), 0.0066" (0.168mm)	12" X 18" (305 X457 mm) 24" X 18" (610 X 457 mm) 24" X 36" (610 X 915 mm) 48" X 36" (1.224 m X 915 mm) *0. 004" (0.101mm) material is not available in panel sizes larger than 24"x18" (610 X 457mm)	½ oz. (1.7µm) electrodeposited copper foil (.5ED/.5ED) 1 oz. (35µm) electrodeposited copper foil (1ED/1ED) 2 oz. (70µm) electrodeposited copper foil (2ED/2ED) **PIM Sensitive Applications:** ½ oz (17µm) LoPro Reverse Treated EDC (.5TC/.5TC) 1 oz (35µm) LoPro Reverse Treated EDC (1TC/1TC)

Figure 2 – Rogers R04003C Datasheet

Material	ρ (Ω·m) at 20 °C	σ (S/m) at 20 °C	Temperature coefficient[note 1] (K^{-1})	Reference
Silver	1.59×10^{-8}	6.30×10^{7}	0.0038	[17][18]
Copper	1.68×10^{-8}	5.96×10^{7}	0.00404	[19][20]

Medium	Susceptibility, volumetric, SI, χ_m	Permeability, μ (H/m)	Relative permeability, max., μ/μ_0	Magnetic field	Frequency, max.
Copper	-6.4×10^{-6} or -9.2×10^{-6}[16]	$1.256\,629 \times 10^{-6}$	0.999 994		

Figure 3- Properties of Copper [3][4]

Design, Build, and Test Calibration Structures

Many of the characteristics of the substrate can be obtained from the datasheet, but as engineers we need to know how these characteristic information is obtained. Using ADS we will attempt to make our own estimate of the relative permittivity of our substrate. Using a parallel distributed element structure

we will see some dramatic changes in the S21 at specific frequencies. Simulating the circuit and measuring the circuit with the VNA should give us an estimate of the actual effective permittivity.

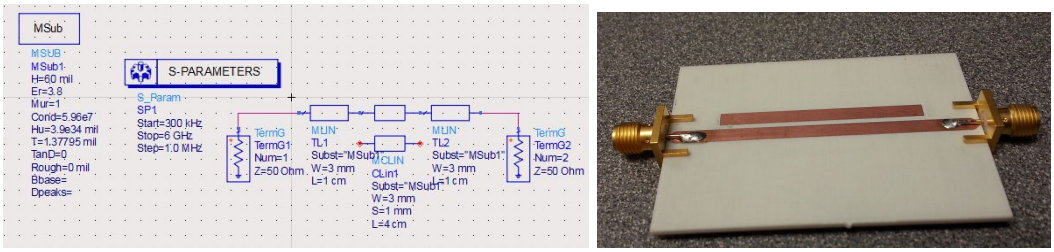


Figure 4- ADS Simulation and Actual Parallel Resonant Circuit

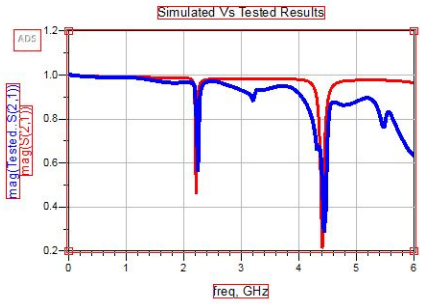


Figure 5- Measured and Simulated Results

TRL Calibration Board Design

All measurements will be done using a Vector Network Analyzer (VNA), which requires calibration prior to taking measurements. Proper calibration of the VNA requires the use of three references: *Through*, *reflect*, and *line* (TRL). The *through* connection is the two SMA terminals connected by a small transmission line, this is normalization reference. The *reflect* connection consists of two SMA connectors with a gap of $\lambda/4$, or at 1 GHz in a copper trace about 22.8 mm. The *line* connection consists of two SMA connectors connected by a $\lambda/4$ section of TL line.

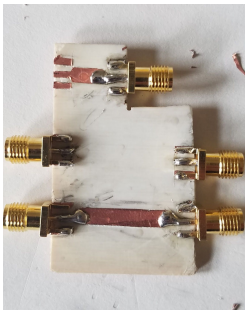


Figure 7- Constructed TRL Board (Mostly complete)

Clearly, since measurements are given in terms of λ, a TRL Board is only good for a given frequency, ior small range. Once the board is constructed, the calibration is performed by defining a Cal Kit in the VNA

software. This is done by defining the frequency range of measurement and assigning the through, reflect, and line measurements. For each connection all 4 S parameters are measured, and using these 12 measurements the VNA uses a set of equations to calculate 10 of the 12 error (it not being possible to calculate the forward and the reverse isolations terms with the available data). With these numbers saved as a Cal Kit, it is then possible to apply these settings when taking a measurement of, say, a filter design.

"Paper" Design

The only requirement for our filter is the graph below. Looking at the graph we can see that the insertion loss should be -4dB at the center frequency of 2.6 or 2.4 GHz. It is important to also notice that both filters have a roll-off of 40 dB for 100 MHz on either side. I would also venture to say that the filter has a perfectly flat passband for 100 MHz around the center frequency.

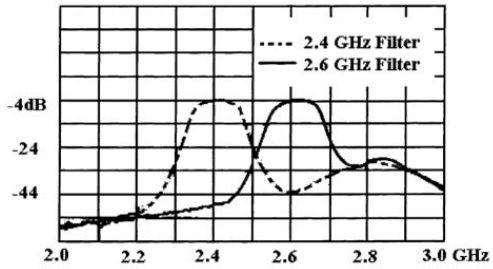


Figure 8- Filter Requirements

Distributed Element Filter

Designing the distributed element filter was greatly facilitated by ADS. I had seen pictures of similar filters [7] and knew I would need a parallel resonant element. I initially used a single element and 50 ohm strips to solder on the connections. I used ADS's tuning option to fit the length, width, and separation to our desired frequency range with a single element. This gave me a filter with a very large bandpass. The roll-off was not enough with a single element. I added more elements in series effectively adding more stages and increasing the roll-off.

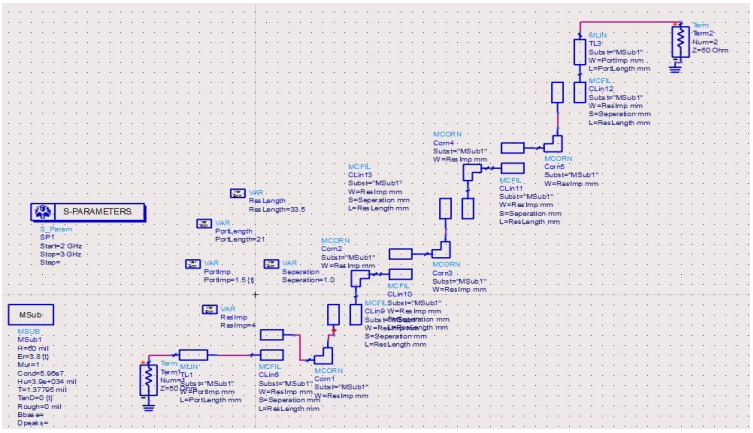


Figure 9- ADS Simulation of the Distributed Element Filter

My initial success was far too large to print on one sample of substrate. I used corner pieces in an effort to make my design more compact. As you can see from the figure below I tuned the whole circuit with a handful of variables. I knew it would be hard to realize, so I only incremented things in .5 millimeter increments. After hours of tuning I came up with my final design. A very simple design that could be cut by hand. The smallest measurement was 1.5 mm.

Figure 10- The Final Distributed Element Circuit

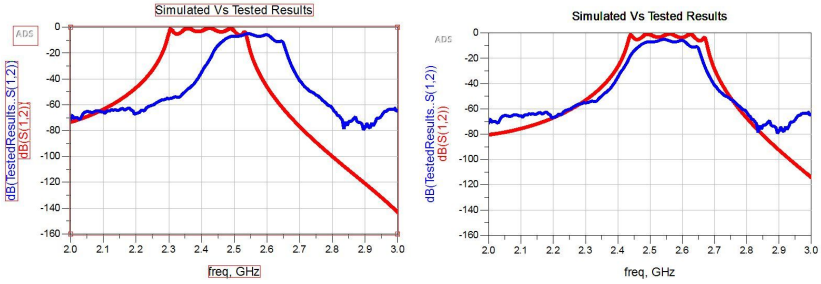


Figure 9- Comparison of Tested and Simulated Results and Adjusted Effective Permittivity

Results

Again using ADS i was able to discover the largest difference between simulation and reality. I used the tuning feature of ADS to adjust the Er of my substrate to 3.3 and the outputs were nearly identical. The insertion loss may be due to the input terminal strips a bit less than 50 ohms. I made them this way intentionally because it seemed to improve insertion loss in the simulation. Also a router issue made one input terminal strip just a tiny bit smaller than the other. The next prototype would be much closer to the expected result. An Er of 3.3 is close to the datasheet specs from Rogers as well.

SMD filter

When the filter was first designed, we followed the standard chebyshev design process. First we design the equivalent low pass filter, determining the cutoff frequency, attenuation and necessary components. Then we convert it into a bandpass filter with the equations listed below.

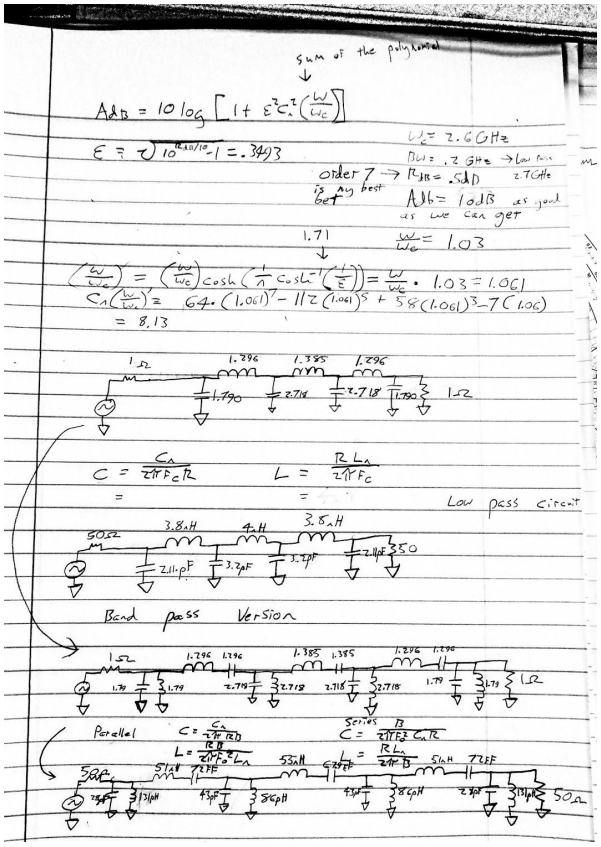


Figure 11- Paper Calculations for the SMD 2.6 GHz Filter

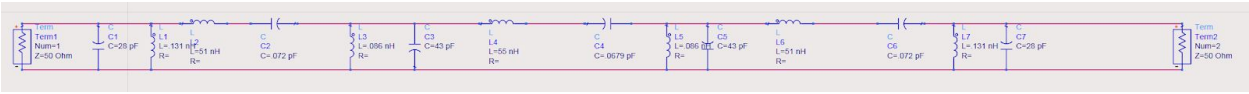


Figure 12- ADS Initial SMD Filter Simulation

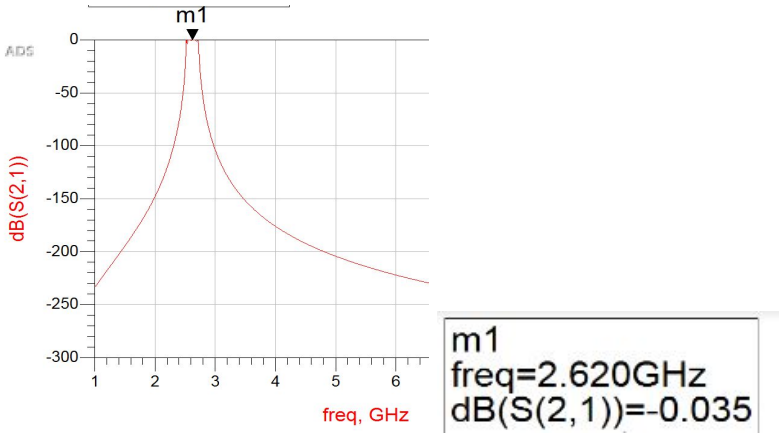


Figure 13- Results of Initial SMD Filter Simulation

But the problem is that these components don't actually exist. Nothing is perfect and circuits are no exception, we need more accurate simulations before we can build anything of this magnitude.

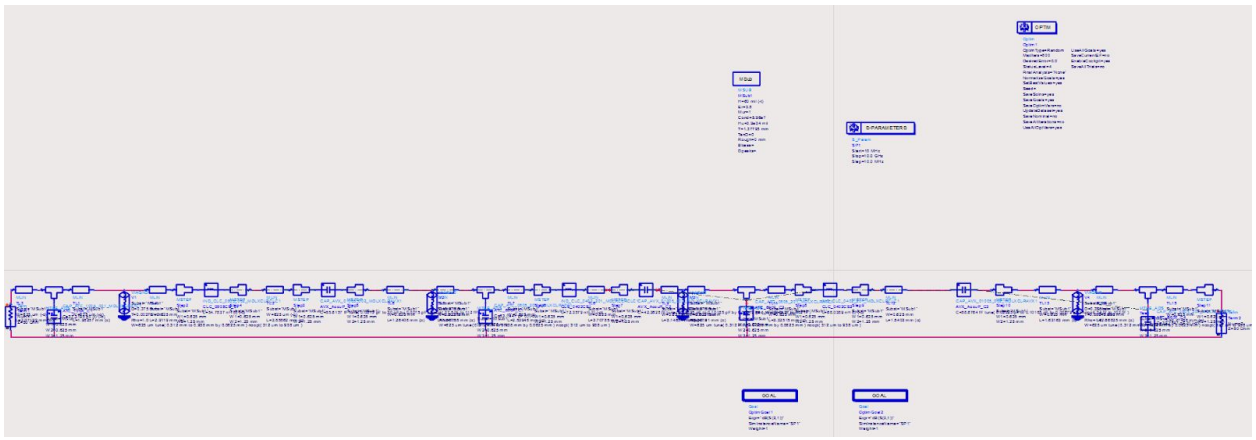


Figure 14- ADS SMD Filter Simulation with Added Microstrip Pads and Connections

Figure 15- ADS Results

EVERYTHING IS RUINED. Unfortunately so. Our band pass filter that worked so perfectly under perfect conditions broke at the sign of stress. Luckily, we have an option. We can remove unreliable components such as small inductors or capacitors to ground and replace them with vias and open circuit stubs, respectively. And run the optimization function, sometimes for hours. Until the response slowly and surely begins to look more and more like a filter

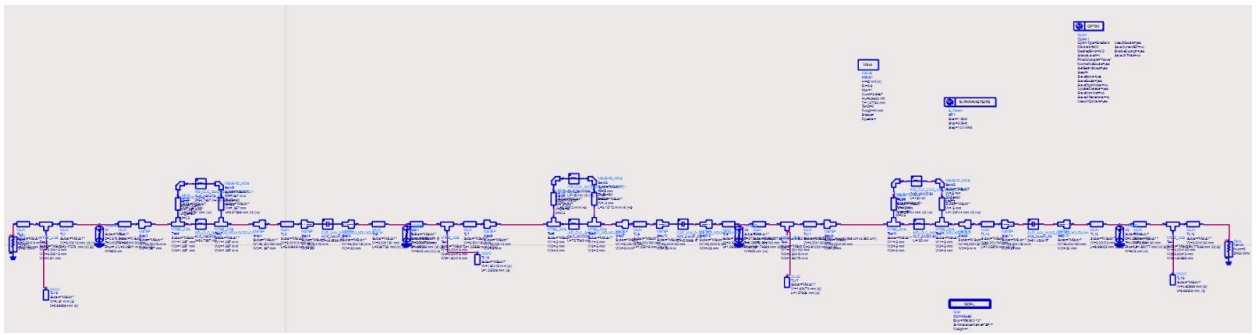


Figure 17- ADS Simulation of Distributed Element / SMD Hybrid

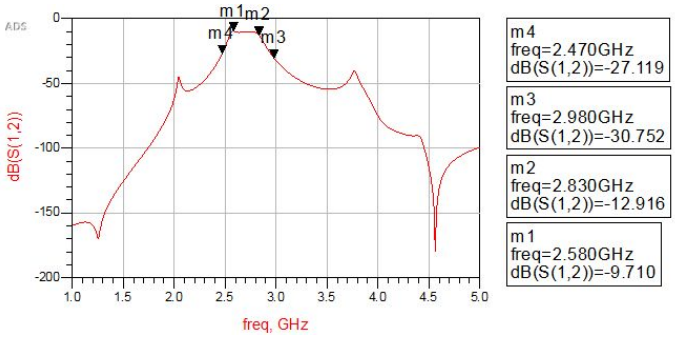


Figure 18- ADS Results of Distributed Element / SMD Hybrid

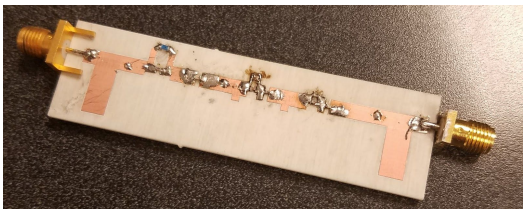


Figure 19- Realized SMD Filter

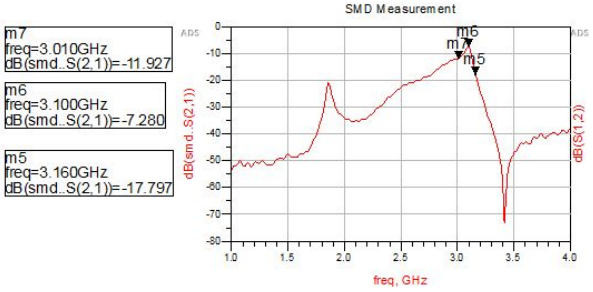


Figure 20- s(2,1) of the SMD Filter

Our output was not at all what we were hoping for. Due to the fact that the filter responds in the general frequency range, we have a large degree of hope for improvement. Possible failures include but definitely are not limited to

- SMD burn out
- Inexact substrate characterization
- Inexact conductivity of the copper and routing errors
- Solder improperly compensated for
- SMDS soldered on and not using a reflow oven

Further plans include compensating for SMD inductance by having more small open circuit stubs next to the component. This is because we can easily shave the stubs off to get the exact compensation for our SMD inductance. Other plans are using reflow ovens to exactly solder on with the least amount of solder.

References

[1]
C. Furse, R.J. Woodward, M.A. Jensen, “Laboratory Project in Wireless FSK Receiver Design,” IEEE Trans. Education, Vol. 47, no. 1, pp. 18-25, Feb. 2004.

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[3]
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[4]
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