ECE533 Project 1 and Project 2

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December 2018

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1 Introduction

The purpose of this project is to build a device that perdorms towards exact specifications. Things such as pad width, grounding, pin length and vias all come into play during this process. The specification required is a return loss of -15dB for S11, the reflection coefficient, up to 6Ghz. In addition the microstrip must be two inches in length. The device is initially designed in HFSS to reach specification, before results can be exported to build the device physically.

2 HFSS Simulation

The first step in creating the HFSS simulation is designing the 50 ohm microstrip. Hand calculations were used for the initial tuning, using the height of the microstrip, the height of the Roger 4003C PCB board, the dielectric constant, and our target impedance. We found a width of around 131.8 mils was ideal, but after speaking with Ha we understood further tuning would be needed when including the SMA connectors.

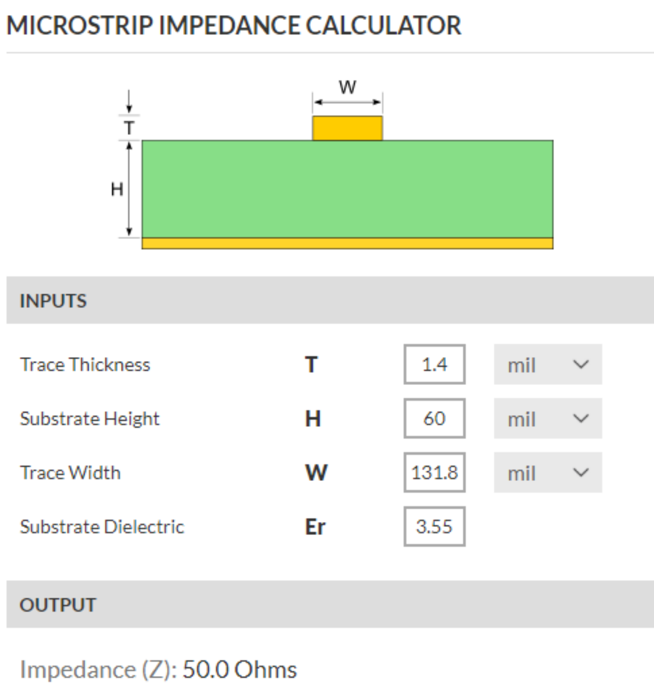

Figure 1: Calculated impedance

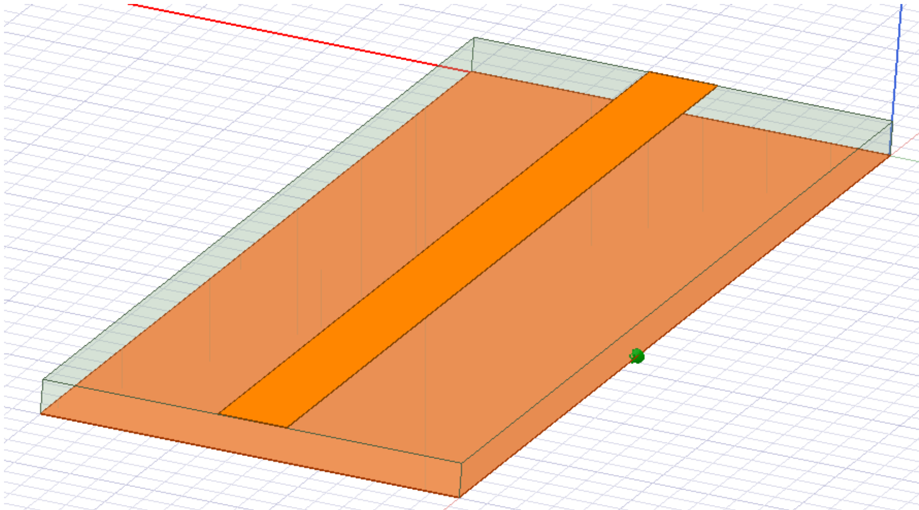

Figure 2: 50 Ohm Microstrip

With the microstrip created, our next step became implementing the SMA connectors into HFSS. By following the datasheet as it describes the SMA connector, we were able to create an accurate simulation of its electromagnetic properties. All final measurements at the various milestones in the build can be found further in the report.

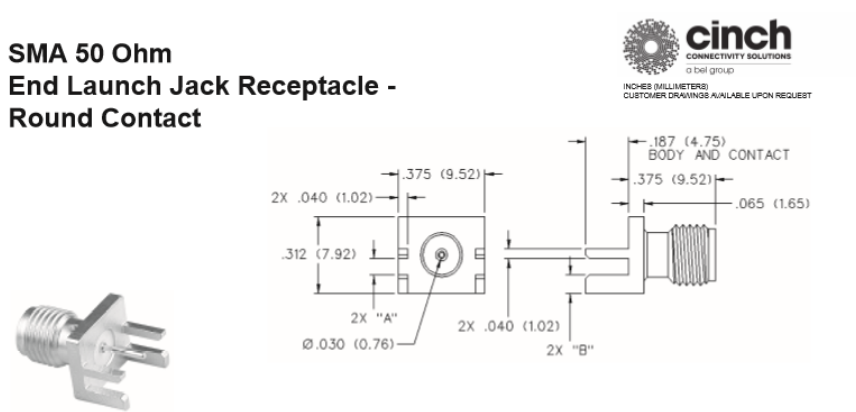

Figure 3: SMA connector specifications

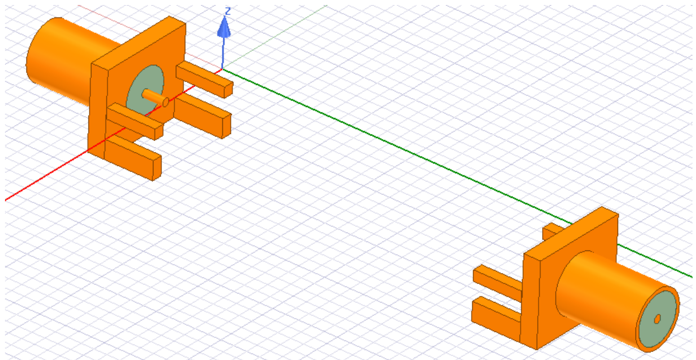

Figure 4: Our final SMA design in HFSS

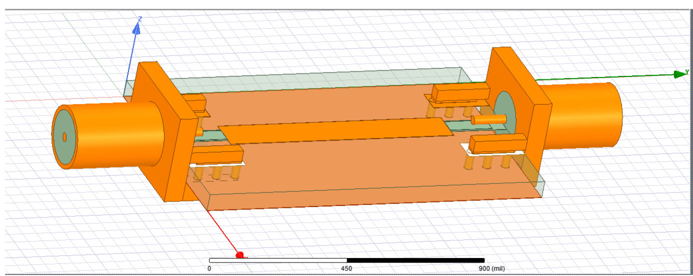

Figure 5: Product post optimization

The goal of the simulation was to vary a wide range of parameters, often coupled together, in such a way that the reflection coefficient (S11) decreases to -15dB. The initial simulations were complete failures, often due to the simulator taking hours to complete a single sweep. This was because the simulator was operating at an accuracy of .5% during an interpolating sweep. As well, the conductors were being modeled as copper, which causes the simulation to go through a large amount of needless calculations. By decreasing the accuracy to 5% and by simulating all metals as perfect electrical conductors (PEC), we were able to decrease the time consumed by a significant factor. We first started to optimize each parameter individually, with little success.

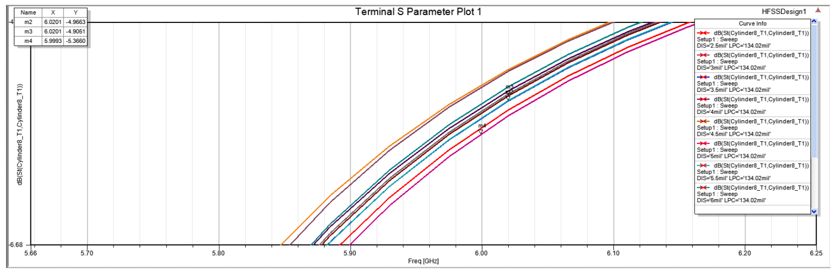

Figure 6: Optimization 1, landing pad distance. The lowest point is -5.3dB

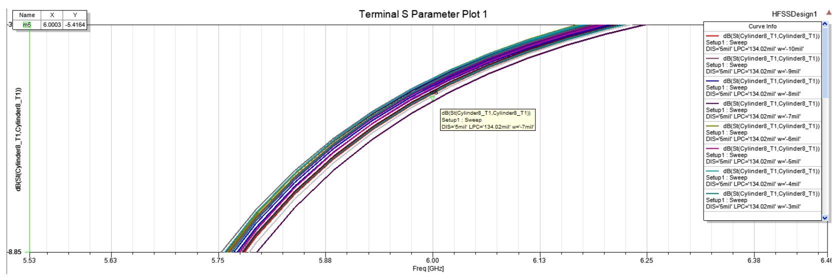

Figure 7: Optimization 1, landing pad width. The lowest point is -5.4dB

Our next step was to sweep through the simulation with two variables with the updated parameters, this actually gave us greatly improved results and helped solidify our design methodology.

- Build simulation
- Sweep parameters one by one from simulation
- Sweep parameters with newly updated values and with two variables

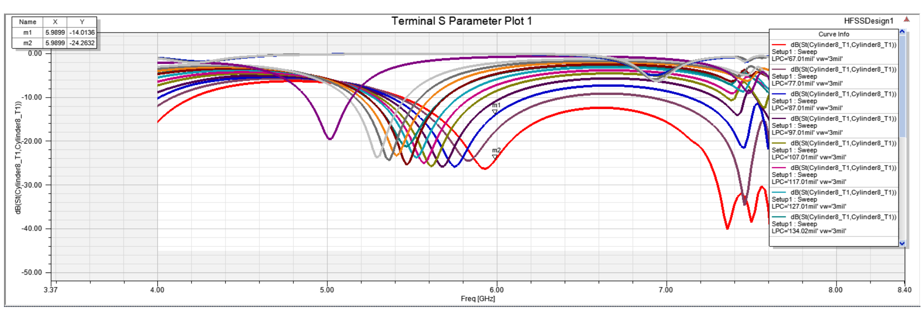

Figure 8: Two parameter simulation, at 6Ghz, the measurement is -24dB

While our measurements at 6Ghz are finally below -15 dB, it can be seen that points below 6Ghz are reaching above -15 dB. Our project deliverable state that "your final design should be better than -15 dB up to 6 GHz in return loss," meaning further optimization is needed. For our next sweep, landing pad width was changed. Results again improved, as the peak at 6Ghz improved to -14.76 dB.

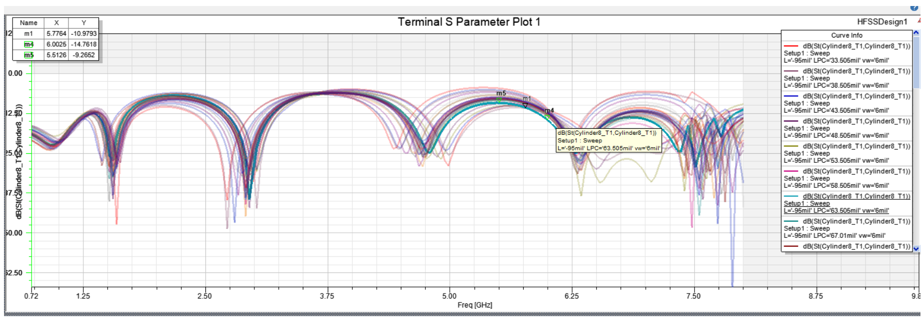

Figure 9: Three parameter simulation, at 6Ghz, the measurement is -14.76dB

To further optimize our results, the decision was made to split the landing pads for the pins into two distinct halves. That way, by adjusting both widths, a more optimized result can be found. For this sweep, landing pad 2 was changed. Again, results did improve, as the peak at 6Ghz slightly, changed to about -15.55 dB.

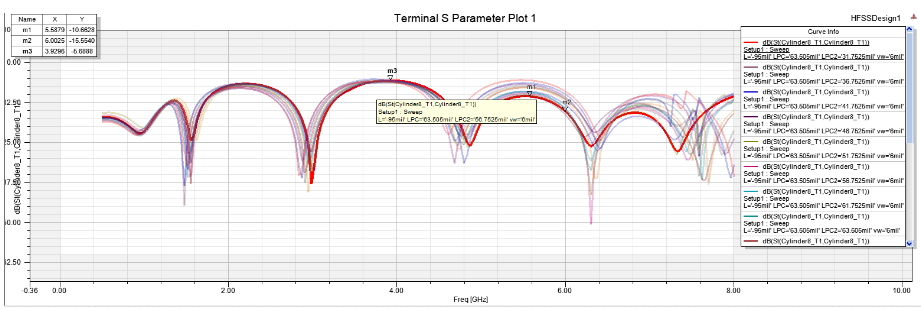

Figure 10: Three parameter simulation, at 6Ghz, the measurement is -15.55dB

Upon further examination, the best response is seen at 5.77Ghz.

- -6.9dB at 3.75Ghz, worst case response
- -14.42dB at 6Ghz
- -37dB at 5.77Ghz, best case response

Figure 11: List of notable frequency responses

Near the end of the project, an unlikely hero emerged where varying the width of the substrate itself actually yielded large changes in the frequency response. By doing this, we were able to bring down 3 of the 4 major resonances close to -15dB. A concerning factor about this response is the fact that the design is so sensitive to perturbation, meaning that any small change in the design due to defects can change the entire response of the system. This is not ideal.

2.1 Final S11 response

The return loss (S11) was brought down to -15dB for the majority of the frequencies between 0 to 6Ghz. However, there is a spot where the frequency response is above -15dB due to a resonance.

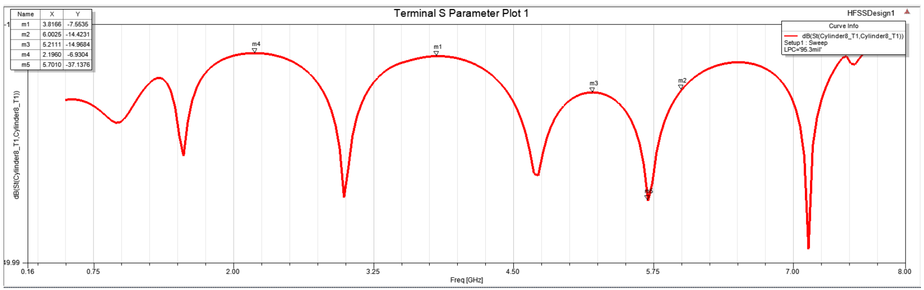

Figure 12: S11 final simulation with the connector

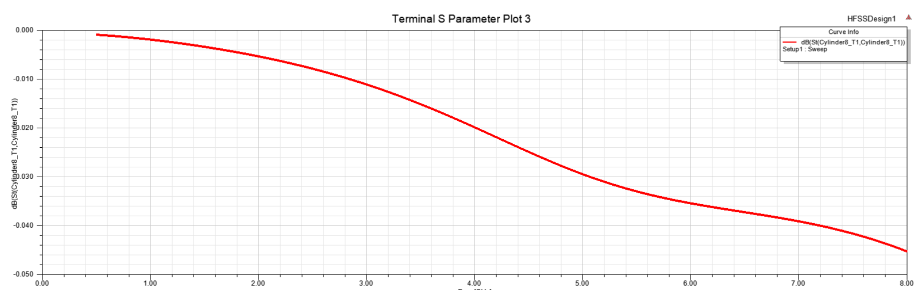

Figure 13: S11 of SMA connector

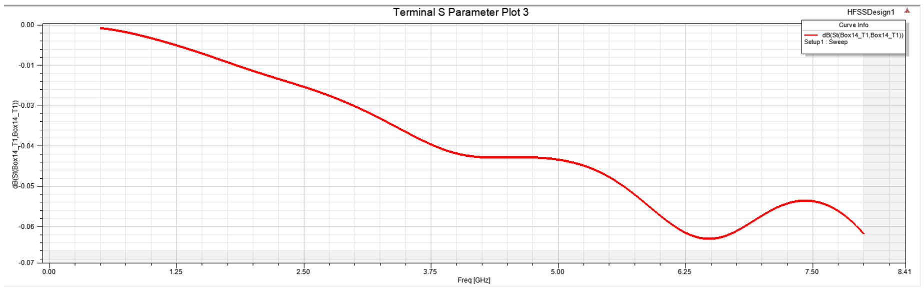

Figure 14: S11 final simulation without connector

2.2 Final S21 response

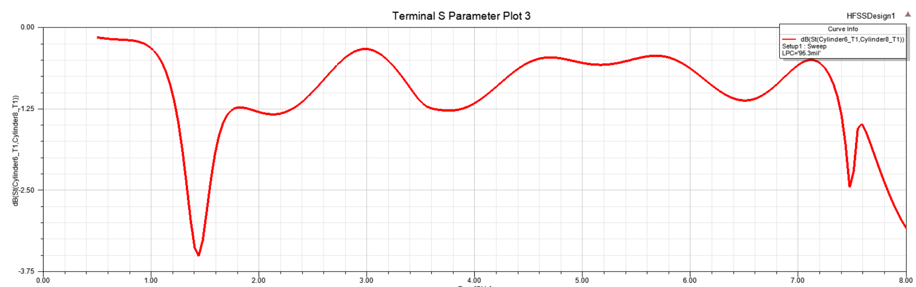

Figure 15: S21 final simulation with connector

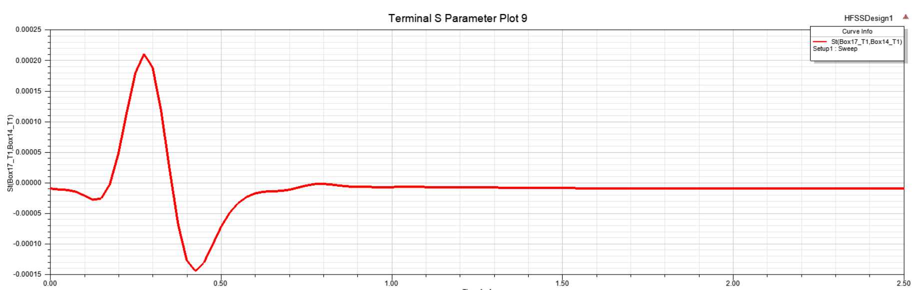

Figure 16: S21 final simulation without connector

2.3 TDR simulation

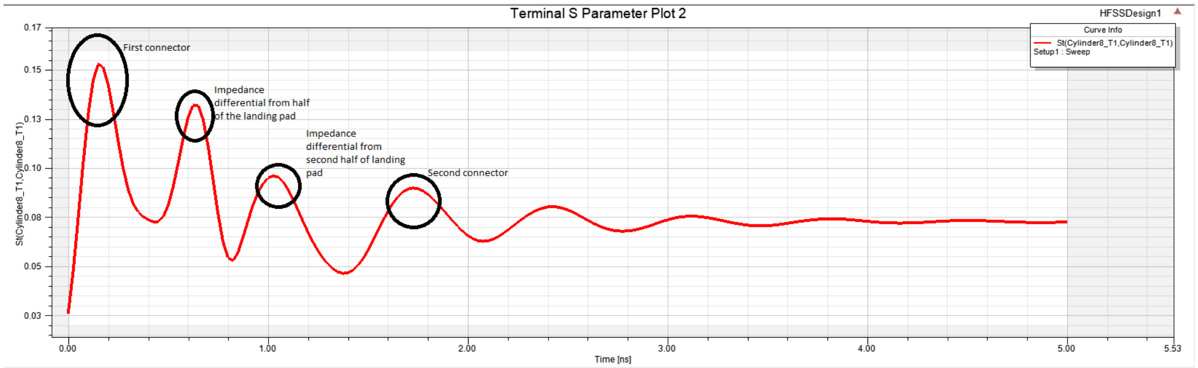

Figure 17: TDR simulation of the strip with a connector

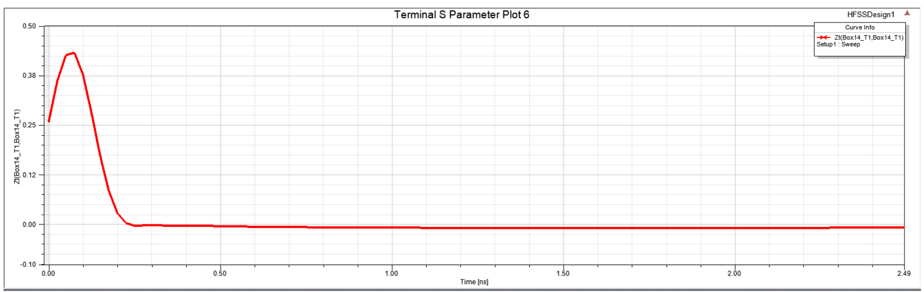

Figure 18: TDR simulation of the strip without a connector, notice the lack of impedance changes seen after the landing pad

2.4 Reflection on simulations

As seen in the S11 plot, the specs were not met. Our reasoning was because of the VIAs causing extra resonances as the frequency swept. Because the connector gave many paths to ground, especially as it passed through the pin. We think that if we increased the number of VIAs inside the pad, the number of actual resonances would decrease due to the decreased VIA inductance. This may help resist further resonances from raising the over all reflection.

3 Real life measurements

Using the export feature in HFSS, the DXF files were created for building the physical board. The three measurements respectively represented the trace/landing, the vias, and the board outline.

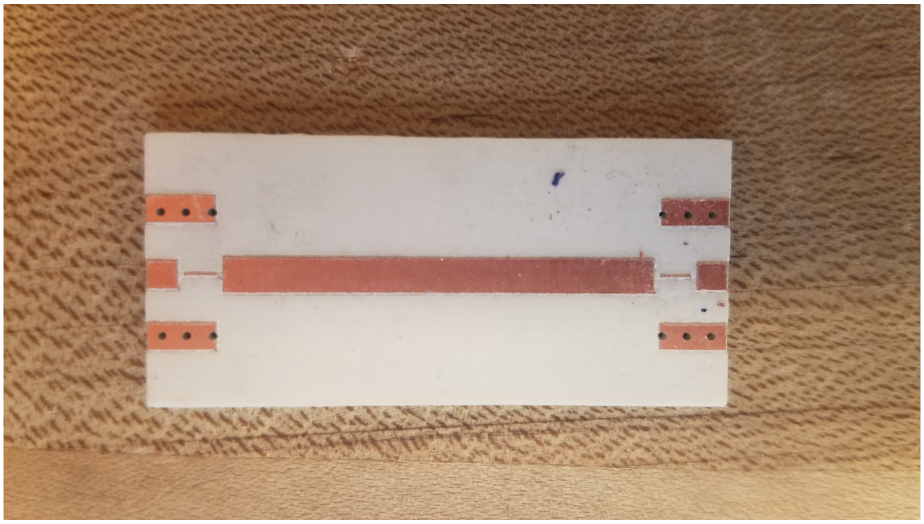

Figure 19: Landing pad without connector

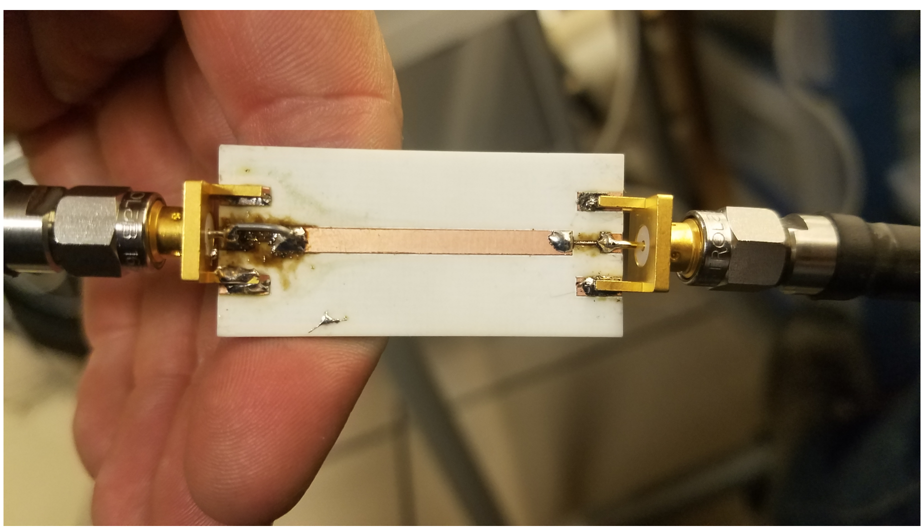

Figure 20: Landing pad with connector

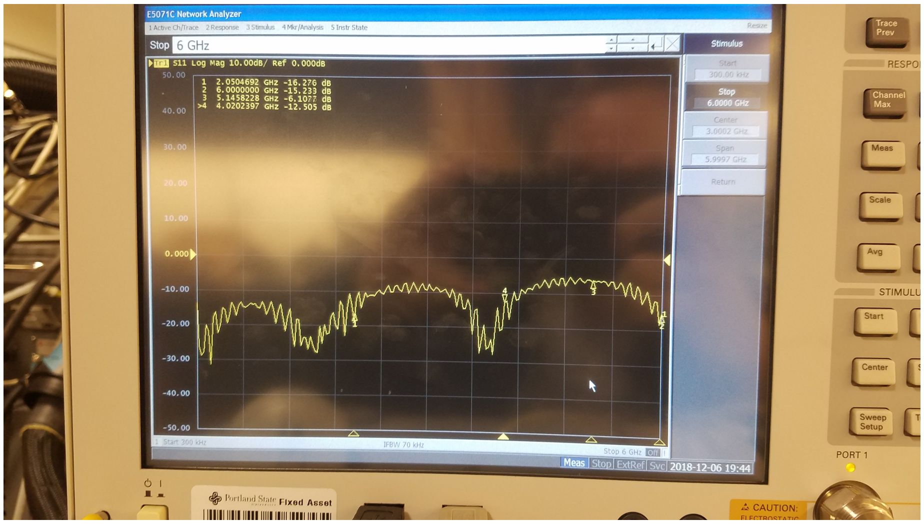

Figure 21: S11 real life measurements

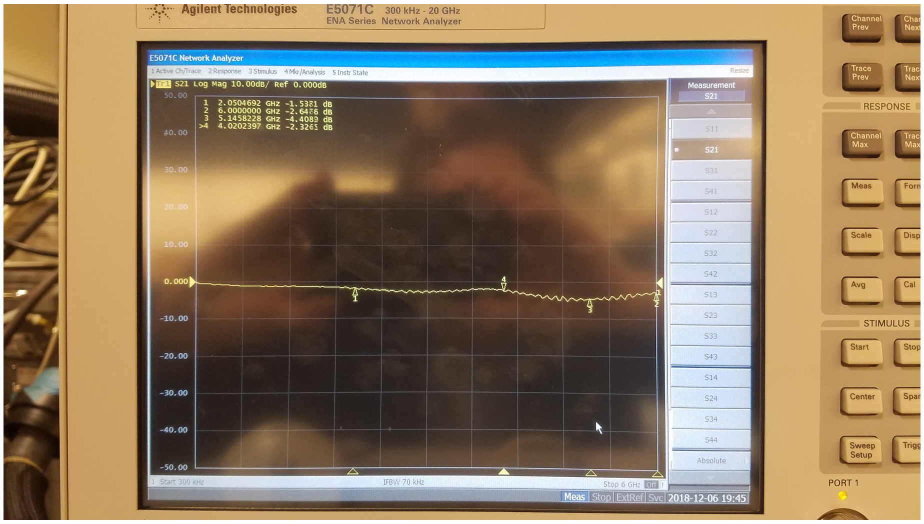

Figure 22: S21 real life measurements

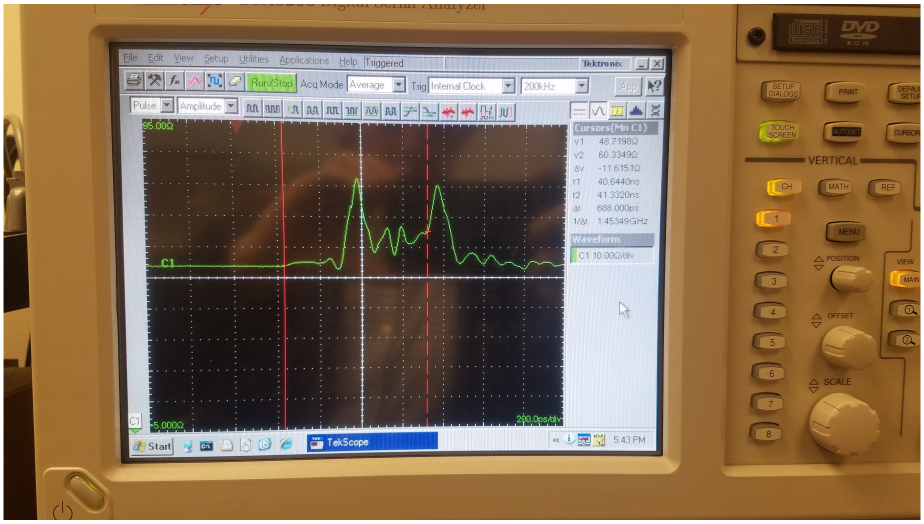

Figure 23: TDR measurements of the assembled strip

4 Analysis and Conclusion

Our simulation caused us a significant amount of errors initially due to extremely long simulation times for which we still have trouble explaining. We initially thought that this was due to bad connections and were able to clean up the simulation substantially by reconnecting the SMA connectors with solder.

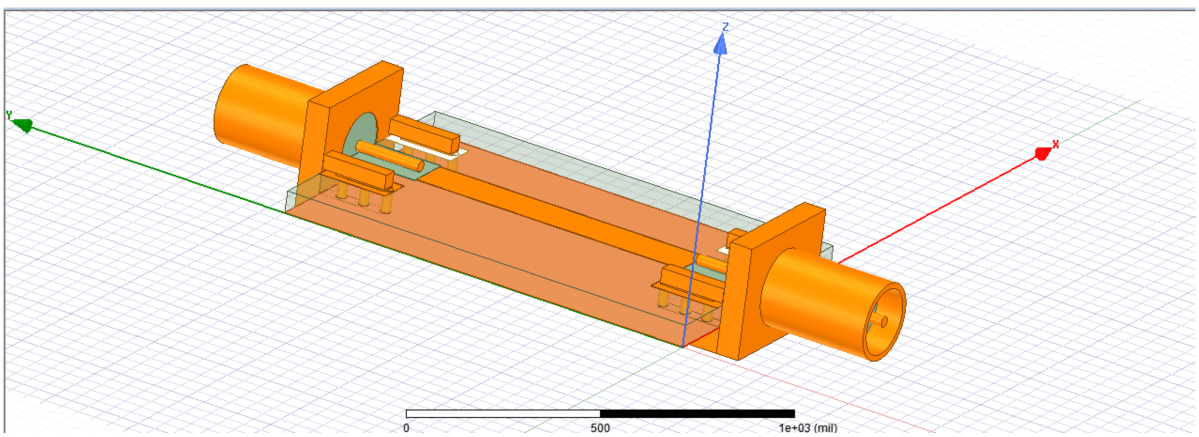

Figure 24: Original SMA landing pad design

4.1 Simulation

Although hard to see from the photo, this original design had the connectors carved into the trace. We did this because we didn't feel that the appropriate boundary conditions would be satisfied with a conductive cube connected between the pin and the trace. However, this was reconsidered and a solder pad was introduced.

Our simulation was further sped up by choosing the "fast" option in the frequency sweep menu, by performing a "fast" simulation we are able to change different possible variables to achieve the best possible results.

We tuned the design by varying different parameters such as the width of the landing pad for the pin, the distance between the via pads and the connector, the microstrip width, the width of the via pads themselves, the width of the board and combining all of them into various combinations in order to further optimize the design.

4.2 TDR

Our TDR simulation made little sense in terms of a complete circuit as the output peaks, which represent the SMA connectors, should match in reflection response on either end. We see this on our real life measurements, which indicate that the circuit is functioning correctly. However, our simulation had a single distinct peak and then no reflection following from the second port. Possible reasons for this include an improper wave port measurement, a short to ground before the connector and improper simulation set up.

For TDR measured in real life, we were able to see two distinct peaks at in between the connectors.

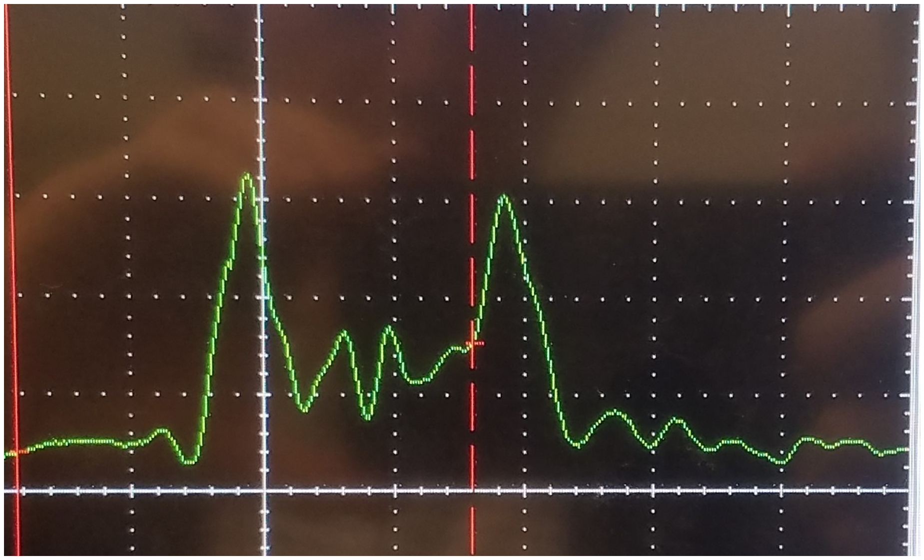

Figure 25: TDR measurement zoomed in

This is due to the impedance change seen in the landing pad. During these moments, the circuit behaves more like an inductor than like a capacitor, although the entire circuit is much more capacitive at that location. When the signal passes through the connector itself, even with trimmed pins, the connector behaves like an inductor.

4.3 Return Loss

Our simulated worst case scenario was at 3.75Ghz, with a maximum of -6.9dB however in the real life measurement this peak was shifted towards 5.14Ghz with a maximum of -6dB. Our best case scenario was at around 1.5Ghz with a response under 20dB. At 6Ghz, our design meets the spec requirements of -15.233dB. This indicates that the real life measurements were far better than our HFSS simulation, a common occurrence seen in this class, and that the simulation itself was accurate enough to predict the behavior of the connectors.
There are many different reasons why the entire design did not meet the spec. The primary reason would likely be due to the resonances seen in **both** the microstrip line simulation and real life measurements. These resonances likely are from the VIAs to ground creating an inductance to counter the capacitance of the entire line. This inductance can be further minimized by creating a wider landing pad and more VIAs (Totalling to 6 on either pad) stitched through the pad design.