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# ECE 171 Project 2

Winter 2017

## Problem Description

### Project function

The previous project described a 2 bit comparator that determined three different properties of the object.

- The first one determines if an object is equal to the second object.
- The second function determines if an object is greater than the second object.
- The third function determines if an object is less than the second object.

Importantly, it should be also known that the greater than and the less than functions are not mutually exclusive. If one is zero, it is not always the case that the other is one.

In this project, we need to be able to expand this comparator to any amounts of bits that the operator requires in an easy and clear operation.

### Requirements

- The project must be expandable for any number of bits.
- The test bench must verify all values for eight bits.

## Project Deliverables

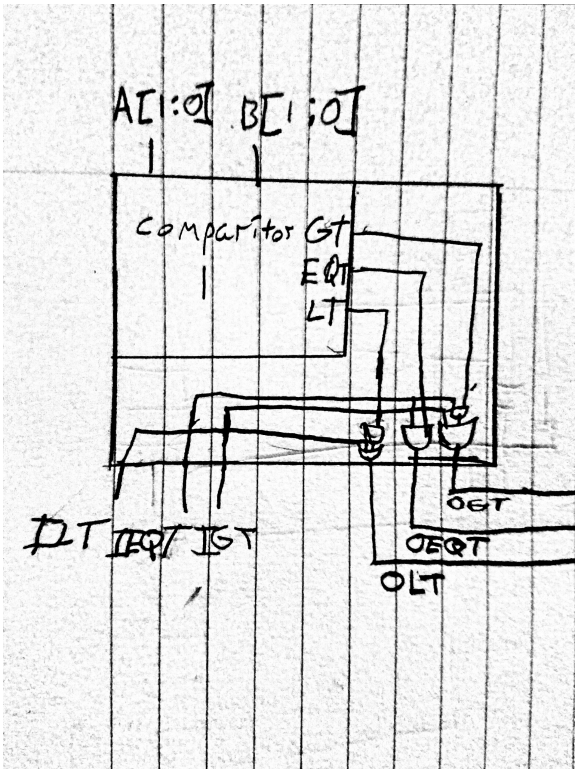
- Black box diagram of all functions
- VHL source code
- SOP equations for each function
- Timing diagram for the 2 bit design

## Project Approach

1. Design a black box diagram, determining both the inputs and outputs.
2. Build a truth table that shows the expected inputs and outputs for the desired function.
3. Interpret the truth table onto the already designed comparator 4. Code the minimized functions in VHL, in behavioral data flow
5. Verify the code with a test bench

# Project Design

## Black box and truth table diagrams




Black Box diagram for the first iteration.

| IGT | ILT | IEQ | LT | EQT | GT | OLT | OEQT | OGT |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | X | X | X | 1 | 0 | 0 |
| 1 | 0 | 0 | X | X | X | 0 | 0 | 1 |

Truth Table for expanded comparator

```
Working directory: "N:\Project 2\project2\"
Executable file:   C:\SynaptiCAD\bin\win32\simxloader32.exe
Program arguments:
 C:\SynaptiCAD\bin\win32\simxloader32.exe -s +loadpli1=syncadverilogx.dll +linedebug
SynaptiCAD VHDL/Verilog simulator rev. 45598.20072.
simgen: Note: Loaded recent snapshot `Compare8BitTest' from library `work'.
vpi_r: Note: PLI veriusertfs array loaded from library: `syncadverilogx.dll' using bootstrap: `register_syncad_tasks'
Init time: 8.1 s (CPU time: 8.1 s)
sim> start_corba_msg_pump
sim> run
SIM: *** Congratulations!   No errors detected

Simulation finished via $finish(1) at time 6553800 ns
Simulation time: 0.1 s (CPU time: 0.1 s)
sim>
```

Simulation output

# Source Code

## Project dataflow description

```
1
2  module Compare8Bit (A, B, IEQ, ILT, IGT, OEQ, OLT, OGT);
3  input [7:0] A, B;
4  input IEQ, ILT, IGT;
5  output OEQ, OLT, OGT;
6  wire  I1, I2, I3, I4, I5, I6,I7,I8,I9;
7
8  program A1 (A[7:6],B[7:6],IEQ,ILT,IGT,I1,I2,I3);
9  program A2 (A[5:4],B[5:4],I1,I2,I3,I4,I5,I6);
10 program A3 (A[3:2],B[3:2],I4,I5,I6,I7,I8,I9);
11 program A4 (A[1:0],B[1:0],I7,I8,I9,OEQ,OLT,OGT);
12
13 endmodule
14
15
16 ////////////////////////////////////////////////////////////////////////////////

17 //////////////As requested, the files are placed into a single program
18 module program (A,B, INEQ, INLT, INGT, OEQ, OLT, OGT);
19 input [1:0] A,B;
20 input INEQ, INLT, INGT;
21 output OEQ, OLT, OGT;
22 assign #6 OGT = INGT
```

```
23 |(INEQ&~INLT&((~B[0]&~B[1]&A[0])
24 |(~B[1]&A[1])
25 |(~B[0]&A[0]&A[1]))));
26 ////////////////////////////////////////////////////////////////////////////////

27 assign #6 OEQ = (~INGT)&(~INLT)&(INEQ)&((~B[0]&~B[1]&~A[0]&~A[1])
28 | (~B[1]&B[0]&~A[1]&A[0])
29 |(A[0]&A[1]&B[1]&B[0])
30 |(A[1]&~A[0]&B[1]&~B[0]));
31 ////////////////////////////////////////////////////////////////////////////////

32 assign #6 OLT = (~INGT)&(INLT)
33 |(INEQ&(~OGT & ~OEQ));
34
35 endmodule
```

## Verilog simulation for a single 2 bit comparator