
ECE323: Lab 3

Phase lock loop

PORLAND STATE UNIVERSITY
MASEEH COLLEGE OF ENGINEERING & COMPUTER SCIENCE
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

Authors:

STEPHEN JOHNSTON

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ECE 323 LAB: 3
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Abstract

The objective of our lab is to finalize our phase lock loop. In the previous labs, we built a voltage controlled oscillator as well as a low pass filter as well as tested and characterized the ring diode mixer. Now we assemble it all together to build the PLL.

Introduction

The phase lock loop is useful for a variety of applications due to its unique nature to hold onto a distinct frequency regardless of variations. This is primarily useful in modulation, FM radio, data transmission and reception. The PLL is comprised of an input frequency, a mixer, a voltage controlled oscillator and a low pass filter. The input frequency is first placed into a mixer, initially empty, and then the output is put into a VCO where the output is again mixed. The output of the mixer is

$$K_\phi \cdot \frac{1}{2}(\cos(w_1 + w_2) + \cos(w_1 - w_2))$$

Where w_1 and w_2 are the frequency of the VCO and the input frequency, respectively. This is then pushed through a low pass filter, so the signal $\cos(w_1 + w_2)$ is removed. This is then sent to the oscillator so that the output frequency is modulated to be proportional to the mixer input frequency. This proportionality causes the frequency of the oscillator to move above and below the RF input frequency. Once the frequency of the VCO (w_1) settles at exactly w_2 , the output of the mixer will be a DC signal and the VCO will stay exactly at that point. The benefit of the pll is that any deviation of the input frequency will cause the VCO to snap straight to the input frequency, as well the output of the phase detector is the demodulated frequency.

A PLL has distinct capture and hold ranges. The capture start is measured by the moment when the PLL locks on an *increasing frequency* and the hold end is when the PLL stops locking on during an *increasing frequency*. The capture end is

when the PLL locks on during a *decreasing frequency* and the hold start is when the PLL stops locking during a *decreasing frequency*.

Results

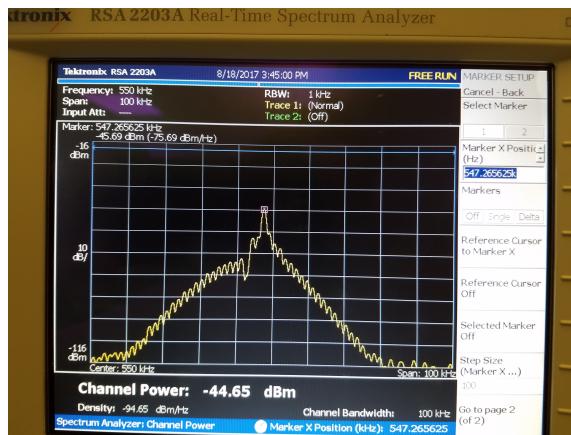


Figure 1: Pre-lock graph



Figure 2: Capture start

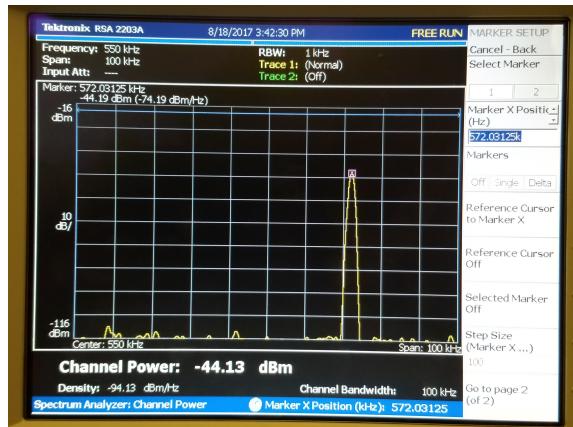


Figure 3: Capture end



Figure 4: Hold end

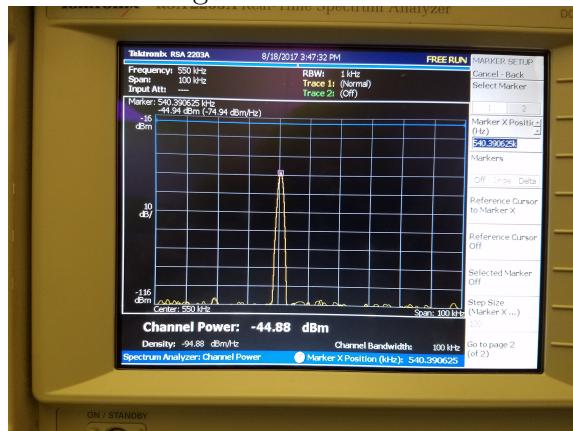


Figure 5: Hold start

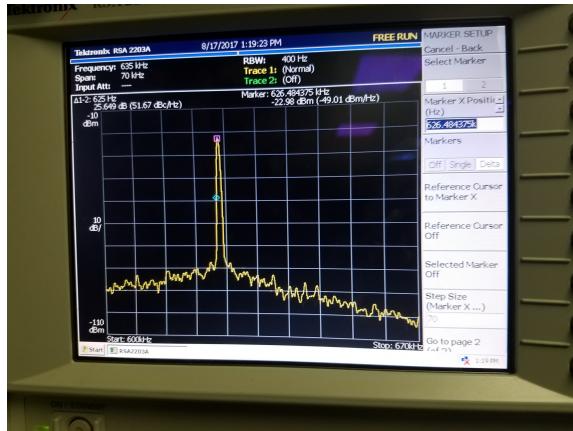


Figure 6: Lock using a second VCO as RF

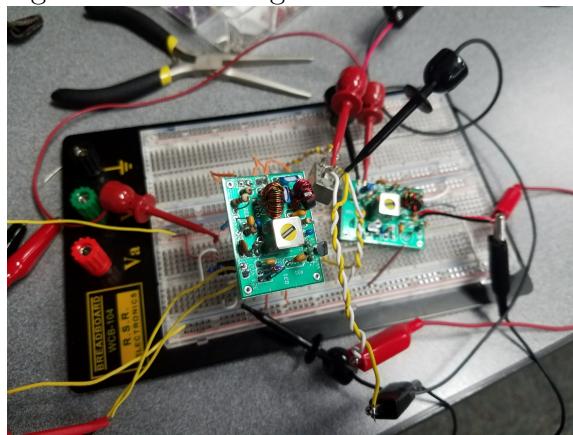


Figure 7: VCO and PLL assembled

	Upper and lower bounds of PLL		
	Low	High	Range
Lock	567kHz	572kHz	5kHz
Hold	540.39kHz	545.23kHz	4.84kHz
VCO + PLL			1kHz

Table 1: Upper and Lower bounds

Discussion

While not at a personally acceptable range, the Phase Locked loop performed adequately with respect to other classmates. Its lock and hold range was roughly 5kHz, which is not good enough for FM frequencies. The PLL did not perform at all while connected to an OP amp for a DC offset, for any different gain. When the PLL was connected to a second VCO as its reference frequency, the PLL was able to lock for about 1Khz