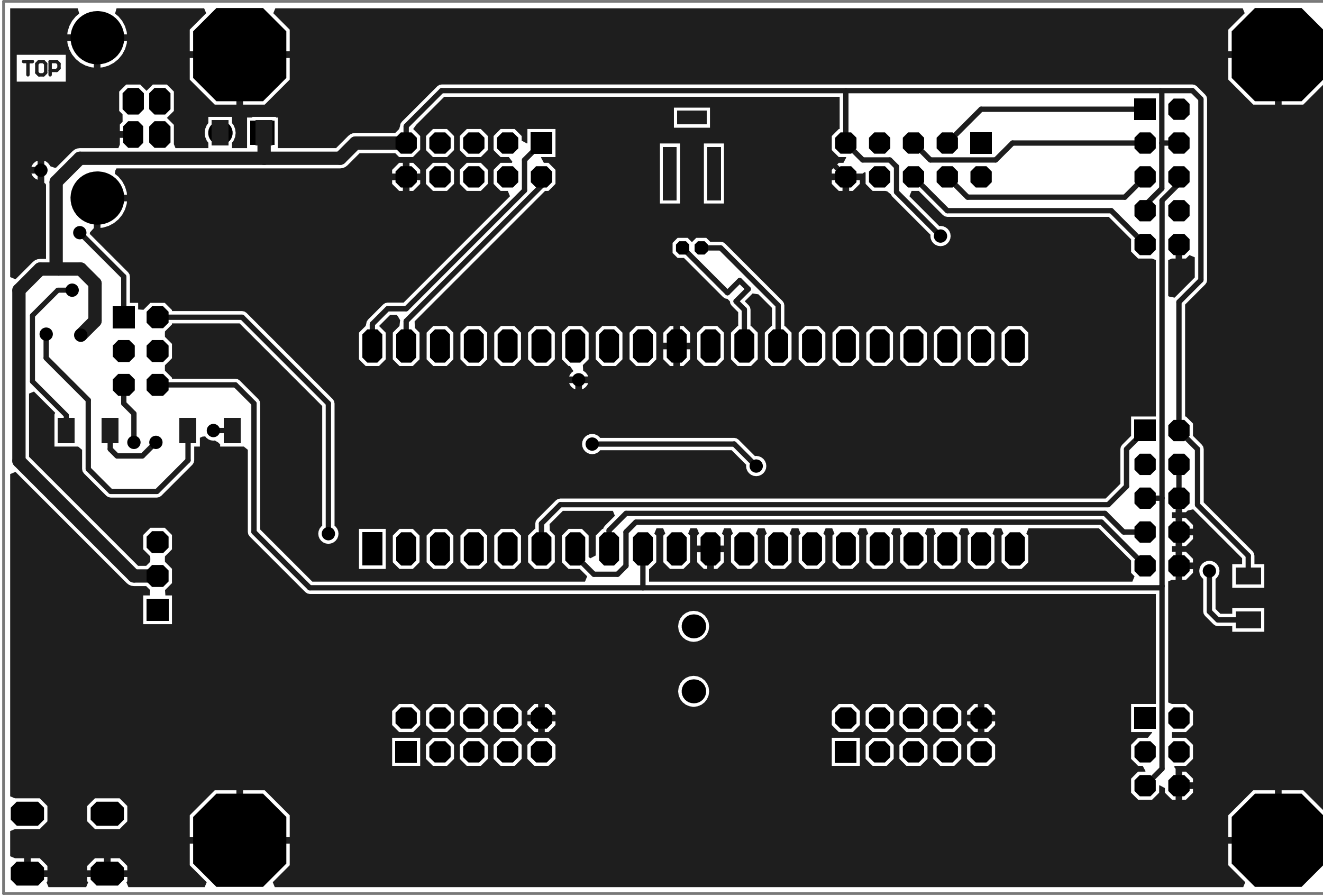
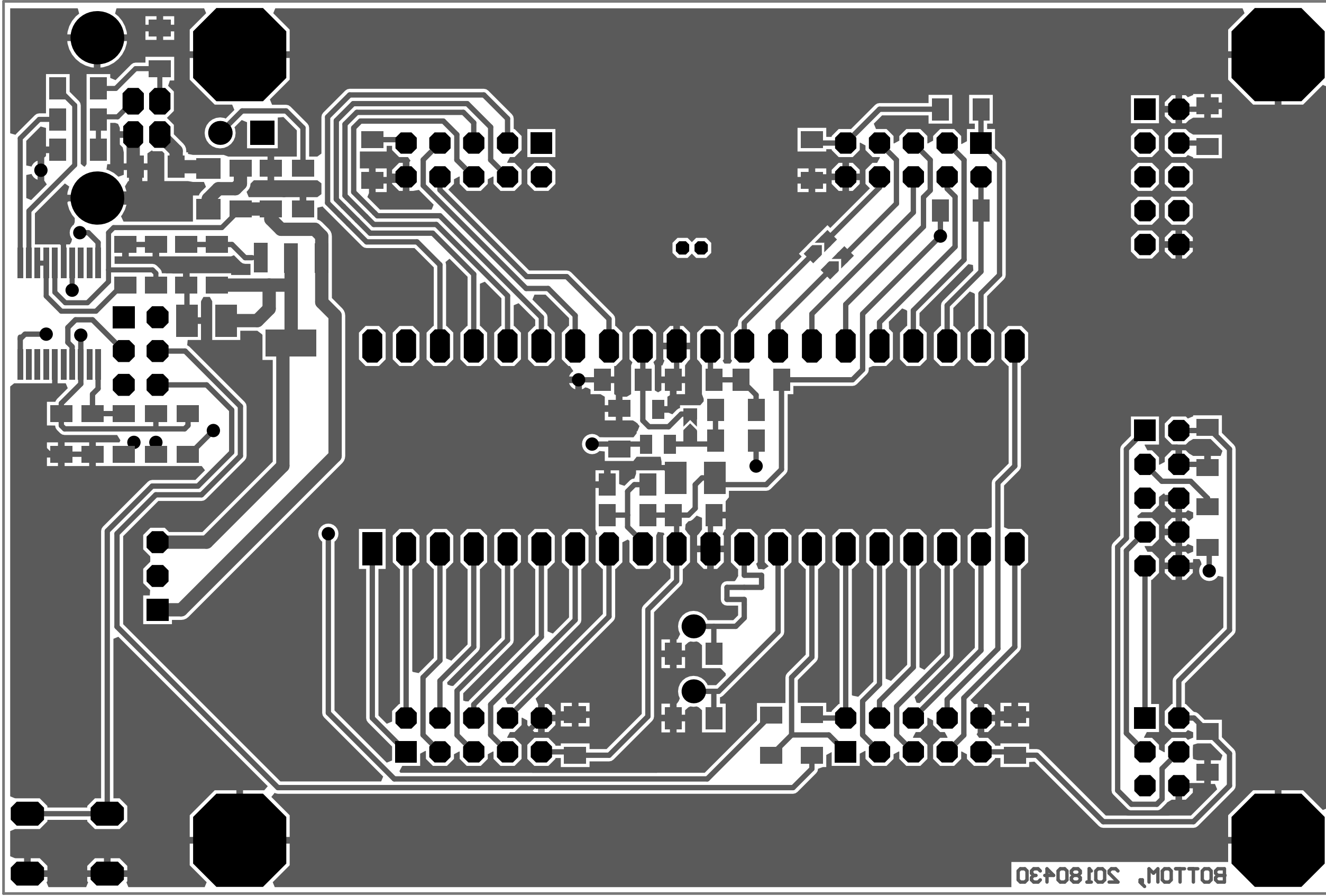




TOP






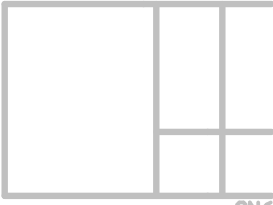
BOTTOM 50180430

  
10k




  
open source  
hardware

RESET

  
5V0

3V3

RxTx

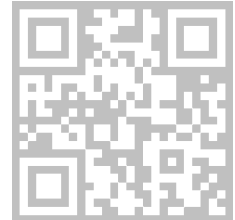


TxD  
RxD  
nDTR

RxD0  
TxD0  
nRST



POWER



<http://bit.ly/2wq4n0I>

PORT B

0: T0  
2: AIN0  
4: nSS  
6: MISO  
VCC

1: CLK0  
3: AIN1  
5: MOSI  
7: SCK  
GND

PORT B

PORT A

1: ADC1  
3: ADC3  
5: ADC5  
7: ADC7  
GND

0: ADC0  
2: ADC2  
4: ADC4  
6: ADC6  
VCC

PORT A



ATmega164PA / 324PA / 644PA

PORT D

0: RXD0  
2: RXD1  
4: OC1B  
6: OC2B  
VCC

1: TXD0  
3: TXD1  
5: OC1A  
7: OC2A  
GND

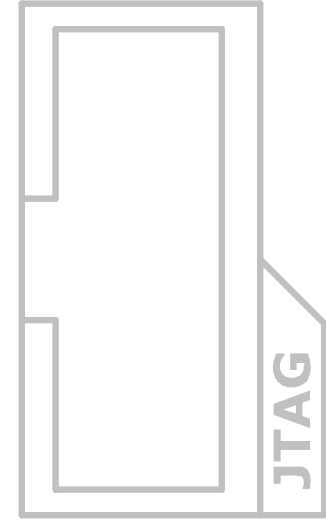
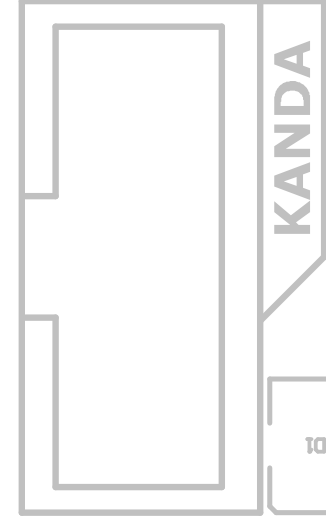
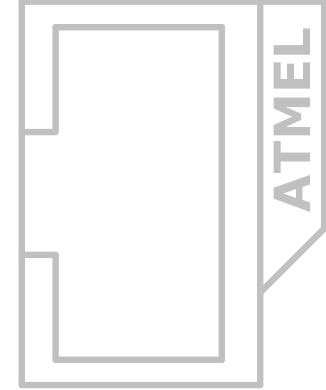
PORT D

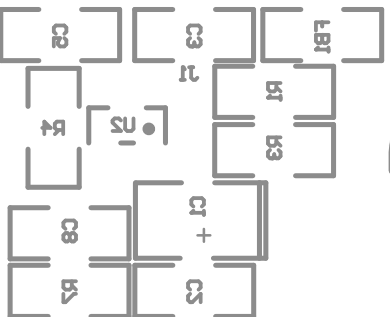
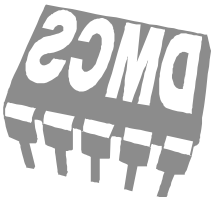
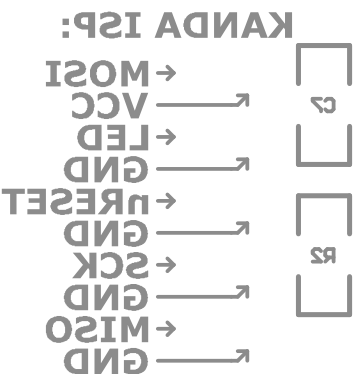
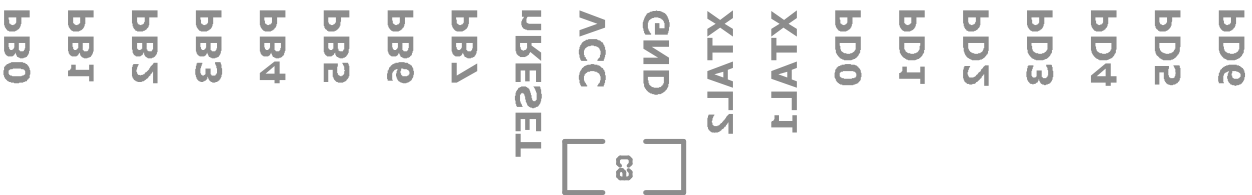
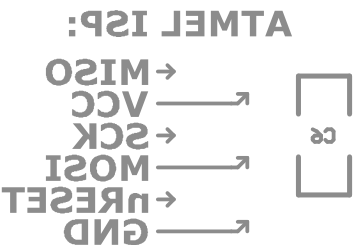
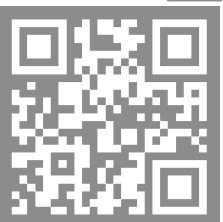
PORT C

1: SDA  
3: TMS  
5: TDI  
7: TOS2  
GND

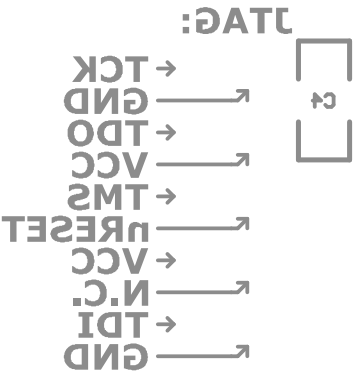
0: SCL  
2: TCK  
4: TDO  
6: TOS1  
VCC

PORT C





# POLITECHNIKA ŁÓDZKA



13 15

