Soham Kapur

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Areas of Interest: *RTL Coding | Digital Hardware Design | CPU Design | Verification | VLSI*

Education

8.78/10 **BTech in Electronics and Computer Engineering**, *Vellore Institute of Technology*, Chennai, Tamil Nadu *2021-25*

91% **Class XII (CISCE Board)**, *Hiranandani Foundation School*, Thane, Maharashtra *2019-21*

96% **Class X (CISCE Board)**, *Smt. Sulochanadevi Singhania School*, Thane, Maharashtra *2007-19*

Relevant Courses: FPGA Based System Design| VLSI Design | Embedded Systems | Compiler Design | Data Structures and Algorithms

Projects

Asynchronous Processor Design *Dec 2024 - Present*

Low Power Design

- Designing and testing an asynchronous pipelined processor using Verilog HDL.
- Implementing a fully clock-less, delay-insensitive, level-encoded pipeline with data bundles.

RISC-V Processor Design *Jul 2024 - Nov 2024*

CPU Design

- RTL design for a 4-stage Pipelined **RISC-V** Processor using Verilog HDL.
- Using **OpenLane2** for automated RTL to GDS2 flow of the processor.
- *Link:* RISC-V Processor

Shorthand Mnemonic Based Assembly Language *Mar 2024 - Apr 2024*

Compiler Design

- Created the syntax and structure of a shorthand notation Assembly Language, initially with **42 instructions**.
- Implemented a **Java simulation** of the instruction set, capable of performing basic operations.
- Link: Shorthand RISC

Solving the Subset Sum Problem by Timing the Greedy Algorithm *Aug 2023 - Sep 2023*

Analysis of Algorithms

- Analyzed and verified a fast algorithm to find an **exact solution** of the Subset Sum Problem.
- Implemented the algorithm resulting in **200% higher speed** than the conventional methods.
- Link: Subset Sum Problem - GBA

Circuit Switching using Dynamic Programming *May 2023 - Jul 2023*

Computer Networks

- Developed a simulation for Circuit Switching which performs static routing using a **Dynamic Programming** algorithm.
- Reduces number of **redundant paths** from the set of all possible paths in the Graph through custom parameters.
- Link: Circuit Switching

Experience

Summer Intern | *Centre for Nanoelectronics and VLSI Design*, VIT Chennai *June 2024 - July 2024*

- ASIC implementation of a single stage of a pipelined processor with RISC-V architecture.
- Designed and verified the Fetch stage of the processor in a team of 3.
- Tools Used: Verilog HDL, Xilinx Vivado, OpenLane2.

Leadership

Captain | *Team Aviators International*, VIT Chennai *Dec 2023 - Nov 2024*

- Led a **45 member** technical student team working on **UAVs** and Fixed Wing model planes.
- Raised over **Rs.2,00,000** in funding for the team through sponsorship.
- Completed **7 products** and participated in 4 competitions using the same.
- Technical Skills: **Ardupilot**, Pixhawk flight controller, UAV component selection.
- Achievements: **Runner Up** at GKN Aerospace Sustainable Aviation Challenge 2023

Skills and Competencies

Electronic Design Verilog HDL, Vivado, Quartus, Cadence Virtuoso, LTSpice

System Design Qsys, Simulink, TinkerCad

Programming Java, C, Matlab, R

Robotics ArduPilot, Mission Planner, Arduino

Soft Skills Fast Learner, Teamwork, Effective Communication, Research, Adaptability, Time Management