SINGLE PHASE DC-AC CONVERTER WITH FAULT TOLERANCE ABILITY FOR ISLANDED PV SYSTEMS

A Major Project Phase-1 Report

Submitted
in the partial fulfillment of the requirement for
the award of the degree of

BACHELOR OF TECHNOLOGY

In

"ELECTRICAL & ELECTRONICS ENGINEERING"

Submitted by

S. KRISHNA PRASAD (B16EE010)
P. SPANDANA (B16EE056)
R. VISHNU TEJA (B16EE012)
N.GOUTHAM (B17EE124L)

Under the Guidance of

SRI Dr. A. MADHUKAR RAO

Department of Electrical & Electronics Engineering

KAKATIYA INSTITUTE OF TECHNOLOGY& SCIENCE: WARANGAL

(Autonomous Institute under Kakatiya University, Warangal)

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

KAKATIYA INSTITUTE OF TECHNOLOGY& SCIENCE, WARANGAL: 506015

(Autonomous Institute under Kakatiya University, Warangal)

CERTIFICATE

This is to certify that this is the bonafide record of the Project work entitled "**SINGLE PHASE DC-AC CONVERTER WITH FAULT TOLERANCE ABILITY FOR ISLANDED PV SYSTEMS**" carried out by **S. KRISHNA PRASAD (B16EE010), P.SPANDANA (B16EE056), R.VISHNU TEJA (B16EE012), N.GOUTHAM (B17EE124L)** students of **IV year B.Tech. Electrical & Electronics Engineering** in partial fulfillment for the award of the degree of **Bachelor of Technology of Kakatiya University**.

Dr. A. MADHUKAR RAO
Asst. Prof. Dept of EEE

Prof. Dr. C. VENKATESH
HOD, EEE Dept.

ACKNOWLEDGEMENT

I wish to express sense of gratitude to my guide to **Dr. A. MADHUKAR RAO,** Asst. Professor, Electrical & Electronics Engineering Department, Kakatiya institute of Technology & Science, Warangal, who guided me at every moment during my entire thesis and giving valuable suggestions. His continuous encouragement at each of work and effort to push the work through are grateful acknowledged.

I specially thank **Dr. D. RAKESH CHANDRA**, Asst. Professor, Dept. of EEE for timely conduction of Major Project schedule.

I am indebted to **Dr. CHALLA VENKATESH,** Head of the Department, Electrical& Electronics Engineering. I also extend my gratitude to all the faculty members of the department without whose support at various stages this report will not be materialized.

Also, I offer my sincere admiration to **Prof. K. ASHOKA REDDY,** Principal, Kakatiya institute of Technology & Science, Warangal for his kind patronage and permission to utilize the resource of institute to carry out the work.

Last but not the least I wish to thanks my friends, seniors who helped me directly or indirectly in the successful completion of this work

S. KRISHNA PRASAD (B16EE010)
P. SPANDANA (B16EE056)
R. VISHNU TEJA (B16EE012)
N.GOUTHAM (B17EE124L)

ABSTRACT

A fault tolerant single phase seven level inverter is proposed in this project for islanded photovoltaic (PV) generation system. This topology has the capability of maintaining same output voltage magnitude in case of switch open circuit fault and/or source open or short circuit fault with slightly reduced number of voltage levels. This helps in supplying uninterruptable power to essential loads even under fault condition.

The topology also has the major advantage of energy balancing between two batteries using redundant switching states. This helps in reducing difference in state of charge (SOC) of batteries during partial shading or hotspots on PV panels. Power loss is calculated for the single phase seven level inverter and a comparison is drawn between conventional systems and this system. This system is simulated using MATLAB/SIMULINK and results are verified.

CONTENTS

LIST OF FIGURES

CHAPTER-1
INTRODUCTION

As there is a continuous increase in energy demand and depletion of conventional resources the demand for renewable energy sources like solar and wind energy systems are increasing. In recent years, attraction of human being is increasing towards the power generation based on renewable energy (RE) sources due to various advantageous features such as environmentally friendly, smaller in size etc., In this context, it is forced to explore more RE sources to meet the demand of power supply. From the last decade, penetration of the solar and wind energy systems in to energy sector is increasing day by day. This fulfills the energy requirement of remote locations. These remote and offshore locations are mostly islanded in nature and far away from technical expertise in case of troubleshooting. This motivates the research on development of fault tolerant converters. These fault tolerant converter under fault allows operation of the system with reduced power rating. This guarantees the continuous power supply to critical loads.

PV is increasingly vital RE energy source due to fast development of power generation technology and has advantages such as pollution free, low maintenance, no moving parts and grid decentralization. PV cell convert direct sunlight into electricity when semiconductor is illuminated by a photon, and the performance is measured in terms of its efficiency when converting sunlight into electricity. Photovoltaic solar panels absorb sunlight as a source of energy to generate direct current electricity. A photovoltaic (PV) module is a packaged, connected assembly of photovoltaic solar cells available in different voltages and wattages. Photovoltaic modules constitute the photovoltaic array of a photovoltaic system that generates and supplies solar electricity in commercial and residential applications. Photovoltaic modules use light energy (photons) from the Sun to generate electricity through the photovoltaic effect.

Conventional multilevel inverters have the advantage of improved power quality, harmonic profile, efficiency and lower filter size compared to two level inverters. But, the issues like increased device count to achieve higher number of voltage levels, capacitor voltage balancing, and reliability problems limits the use conventional multilevel inverters. Multilevel topologies presented only the device count and capacitor voltage balancing problems. But the reliability with respect to switch or source failure is not addressed in these topologies leading to overall system shutdown which in turn makes healthy part of the system being underutilized.

The switch failure issues are addressed in by using extra switches without compromising on number of voltage levels. The nine-switch topology presented has switch open and/or short circuit fault tolerant capability but, need of accessing both load neutral point and split dc link connection during fault operation is the disadvantage. The switch and/or source failures are addressed and it also have an advantage of energy balancing capability but, it has fault tolerant capability only for few switch failures. In this project a fault tolerant single phase seven level inverter is presented for remote and offshore PV applications.

The topology is having two asymmetrical separate PV strings rated accordingly of the total power rating as compared to single centralized PV inverter. Advantage of having two separate PV strings are reduced switch rating as the total dc link voltage is divided in to parts and has the energy sharing between two sources in case of partial shading or hotspots. The proposed topology has the fault tolerant capability for one of the switches and/or source open circuit fault and does not have neutral point voltage balancing and capacitor voltage balancing problems unlike conventional multilevel inverters. The fault tolerant is achieved by using extra bidirectional switch with least modification in switching combination.

CHAPTER-2
NEED FOR FAULT TOLERANT PV SYSTEMS

Increasing energy demand of the modern world and depletion of conventional energy sources are driving the power generation towards renewable energy sources. The early day challenges like Uncertainty and high initial installation cost were limiting the efficient utilization of all renewable energy sources. The tremendous growth in harvesting technology, recent developments in semiconductor fabrication technology has considerably reduced the initial cost and brought the renewable energy sources back to focus. This fulfills the energy requirement of remote locations. These remote and offshore locations are mostly islanded in nature and far away from technical expertise in case of troubleshooting. This motivates the research on development of fault tolerant converters. These fault tolerant converter under fault allows operation of the system with reduced power rating. This guarantees the continuous power supply to critical loads A photovoltaic system, also PV system or solar power system, is a power system designed to supply usable solar power by means of photovoltaics. It consists of an arrangement of several components, including solar panels to absorb and convert sunlight into electricity, a solar inverter to convert the output from direct to alternating current, as well as mounting, cabling, and other electrical accessories to set up a working system. It may also use a solar tracking system to improve the system's overall performance and include an integrated battery solution, as prices for storage devices are expected to decline.

2.1 PV (Photo Voltaic) System:

Photovoltaic solar panels absorb sunlight as a source of energy to generate direct current electricity. A photovoltaic (PV) module is a packaged, connected assembly of photovoltaic solar cells available in different voltages and wattages. Photovoltaic modules constitute the photovoltaic array of a photovoltaic system that generates and supplies solar electricity in commercial and residential applications.

Photovoltaic modules use light energy (photons) from the Sun to generate electricity through the photovoltaic effect. Most modules use wafer-based crystalline silicon cells or thin film cells. The structural (load carrying) member of a module can be either the top layer or the bottom layer. Cells must be protected from mechanical damage and moisture. Most modules are rigid, but semi-flexible ones based on thin-film cells are also available. The cells are connected electrically in series, one to another, to a desired voltage, and then in parallel to

increase amperage. The wattage of the module is the mathematical product of the voltage and the amperage of the module. A PV junction box is attached to the back of the solar panel and functions as its output interface. External connections for most photovoltaic modules use MC4 connectors to facilitate easy weatherproof connections to the rest of the system. A USB power interface can also be used.

Module electrical connections are made in series to achieve a desired output voltage or in parallel to provide a desired current capability (amperes) of the solar panel or the PV system. The conducting wires that take the current off the modules are sized according to the ampacity and may contain silver, copper or other non-magnetic conductive transition metals. Bypass diodes may be incorporated or used externally, in case of partial module shading, to maximize the output of module sections still illuminated.

Some special solar PV modules include concentrators in which light is focused by lenses or mirrors onto smaller cells. This enables the use of cells with a high cost per unit area (such as gallium arsenide) in a cost-effective way.

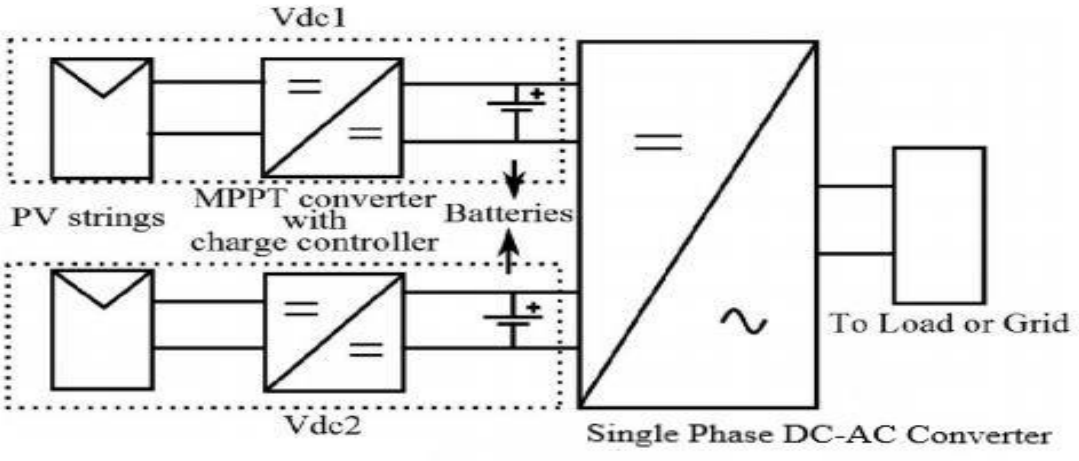


Fig (2.1): Block diagram of a Photo Voltaic (PV) System

2.2 Maximum Power Point Tracking (MPPT):

An MPPT, or maximum power point tracker is an electronic DC to DC converter that optimizes the match between the solar array (PV panels), and the battery bank or utility grid. To put it simply, they convert a higher voltage DC output from solar panels down to the lower voltage needed to charge batteries.

The block diagram and circuit diagram of a MPPT for a cell is shown below.

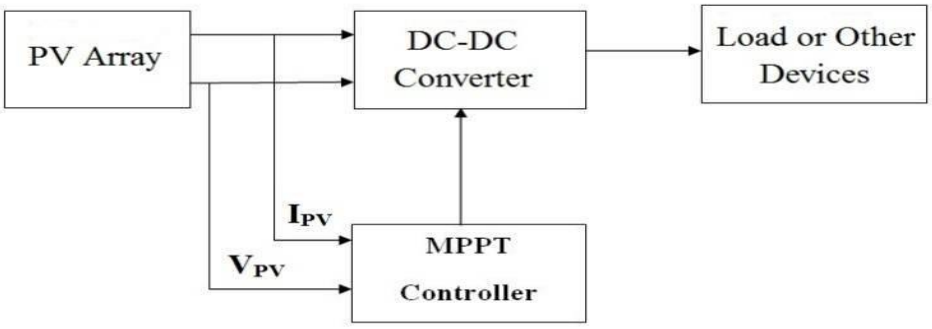


Fig (2.2): Block diagram of MPPT implementation

When a load is directly connected to the solar panel, the operating point of the panel will rarely be at peak power. The impedance seen by the panel determines the operating point of the solar panel. Thus, by varying the impedance seen by the panel, the operating point can be moved towards peak power point. Since panels are DC devices, DC-DC converters must be utilized to transform the impedance of one circuit (source) to the other circuit (load). Changing the duty ratio of the DC-DC converter results in an impedance change as seen by the panel. At a particular impedance (i.e. duty ratio) the operating point will be at the peak power transfer point. The I-V curve of the panel can vary considerably with variation in atmospheric conditions such as radiance and temperature. Therefore, it is not feasible to fix the duty ratio with such dynamically changing operating conditions.

MPPT implementations utilize algorithms that frequently sample panel voltages and currents, then adjust the duty ratio as needed. Microcontrollers are employed to implement the algorithms. Modern implementations often utilize larger computers for analytics and load forecasting.

CHAPTER- 03
INVERTERS

3.1 Introduction to Inverters:

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Inverters can be broadly classified into single level inverter and multilevel inverter. The converters have to be designed to obtain a quality output voltage or a current waveform with a minimum amount of ripple content. Numerous industrial applications have begun to require high power apparatus in recent years. For the control of electric power or power conditioning the conversion of electrical power from one form to another is necessary and the switching characteristics of the power devices permits these conversions.

Inverters are the devices that are used for conversion of DC to AC. In high power and high voltage applications the conventional two-level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of the power device ratings. The output voltage of an inverter can be fixed type or variable type at fixed or variable frequency. A variable output voltage can be obtained by varying the input dc voltage and maintaining the gain of the inverter constant. On the other hand, if the dc voltage is fixed variable output voltage can be obtained by varying the gain of the inverter. Inverter gain is defined as the ratio of ac output voltage to dc input voltage.

In the beginning multilevel converters were introduced to drive high voltages, like in High Voltage Direct Current (HVDC) applications to make the front-end connection between DC and AC lines. In this way the limits on the maximum voltage tolerable by the semiconductor switches were overtaken and the converters were able to drive directly the line voltage without a transformer. Nowadays it is possible to find multilevel applications even in low voltage field, like motor drive, because of the high quality of the AC output. In particular back-to-back multilevel systems can drive motors with very good performance concerning the line voltage and current distortions. Multilevel can even improve the converter losses.

3.2 Conventional Inverters:

In the conventional two-level inverters, the input DC is converted into the AC supply of desired frequency and voltage with the aid of semiconductor power switches. Depending on

the configuration, four or six switches are used. A group of switches provide the positive half cycle at the output which is called as positive group switches and the other group which supplies the negative half cycle is called negative group.

Limitations of conventional inverters:

1. The classical two-level inverter produces output with level either 0 or $+V_{dc}$ or $-V_{dc.}$
2. They cannot be used in high power and high voltage applications because of higher frequency and there will switching losses.
3. The output voltage waveform of ideal inverter should be sinusoidal but the waveform of conventional inverters is non-sinusoidal and contains certain harmonics.
4. Large capacitor will be connected across the DC voltage source which is costly and requires more space.

3.3 Multilevel Inverters:

Multilevel inverters have attracted much attention in high power electronics applications as the solution of needs for higher power ratings and the reduction of the output harmonic distortion, voltage stress (dv/dt) and EMI phenomenon. Multilevel began with the 3-level converter, then several multilevel converter topologies has been developed. Multi-level inverters provide more than 2 voltage levels. The basic principle of a multilevel inverter is to connect semiconductor switches in series so that the converter can operate with power ratings of several megavolt amperes and at medium voltage levels (1kv to 35kv) that exceed the individual switch voltage ratings. The output voltage waveform will be synthesized from several levels of capacitor voltage sources. As the number of levels increases, the obtained output waveform approaches the sinusoidal wave with less distortion, less switching frequency, higher efficiency etc…

The first multilevel topology introduced is the Cascades H-bridge design which implements a set of H-bridge separate dc source inverter serially connected to produce an n-voltage level. This was followed by diode clamped inverter which utilizes a bank of series capacitors paralleled with dc source to produce an n-additional voltage source, another multilevel topology subsequently introduced was flying capacitor design

in which the capacitors were floating rather than series connected. Moreover, there are different multilevel designs which involve parallel connection of inverter phases through inter-phase reactors.

3.3.1 Basic Principle of Operation:

Fig 1.1 shows the schematic of a pole in a multilevel inverter where Vo indicates an output phase voltage where any voltage level can be obtained depending on the selection of node voltage V1, V2, etc., hence this pole can be referred as single pole multiple throw switch. Series connected capacitor acts as the energy tank for the inverter, providing some nodes to which the multilevel inverter can be connected by connecting the switch to one node at a time, one can obtain the desired output.

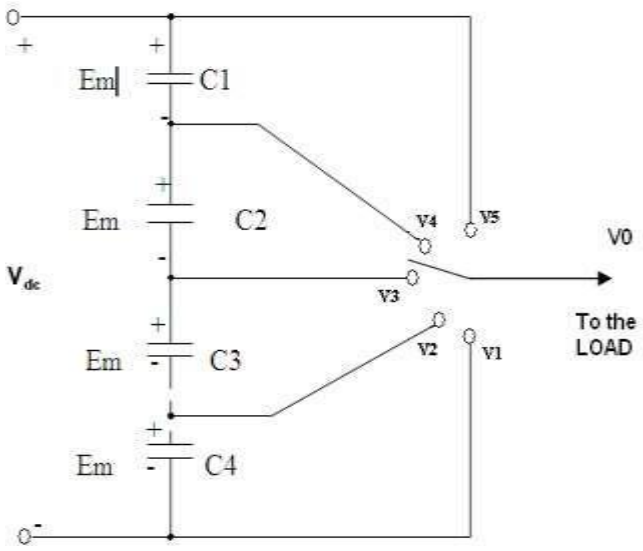


Fig (3.1): Schematic of Single Pole of Multilevel Inverter by a Switch.

For an m-level inverter needs (m-1) capacitors.

The most attractive features of multilevel inverters are as follows.

- They can generate output voltages with extremely low distortion and lower dv/dt.
- They draw input current with very low distortion.
- With a lower switching frequency, they can be operated.
- A multilevel inverter can eliminate the need for the step-up transformer and reduce the harmonics produced by the inverter.
- With additional voltage levels, the voltage waveform has more free-switching angles, which can be preselected for harmonics elimination.

The main disadvantage of multilevel inverter is that they require greater number of switches.

3.3.2Types of Multilevel Inverters

- Diode-clamped multilevel inverter
- Flying capacitor multilevel inverter
- Z-Source multilevel inverter
- Cascaded multilevel inverter with separate dc sources

(a) Diode Clamped Multilevel Inverter:

A diode-clamped multilevel inverter employs clamping diodes and cascaded dc capacitors to produce ac voltage waveforms with multiple levels. The inverter can be gradually configured as a three, four or five level topologies. Here five level topology is used.

Converter Configuration and Operation principle:

Fig 1.2 below shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes.

Switching States

To explain how the staircase voltage is generated, the neutral point is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across a and n.

1) For voltage level Van=$V_{dc}/2$, turn on all upper switches S1-S4.
2) For voltage level Van=$V_{dc}/4$, turn on three uppers witches S2 – S4 and one lower switch S1‘.
3) For voltage level Van=0, turn on two upper switchesS3and S4and two lower switchesS1‘ and S2‘
4) For voltage level Van= -$V_{dc}/4$, turn on one upper switch S4 and three lower switches

S1‘– S3‘.

5) For voltage level Van=-V_{dc}/2, turn on all lowerSwitchesS1‘–S4‘.

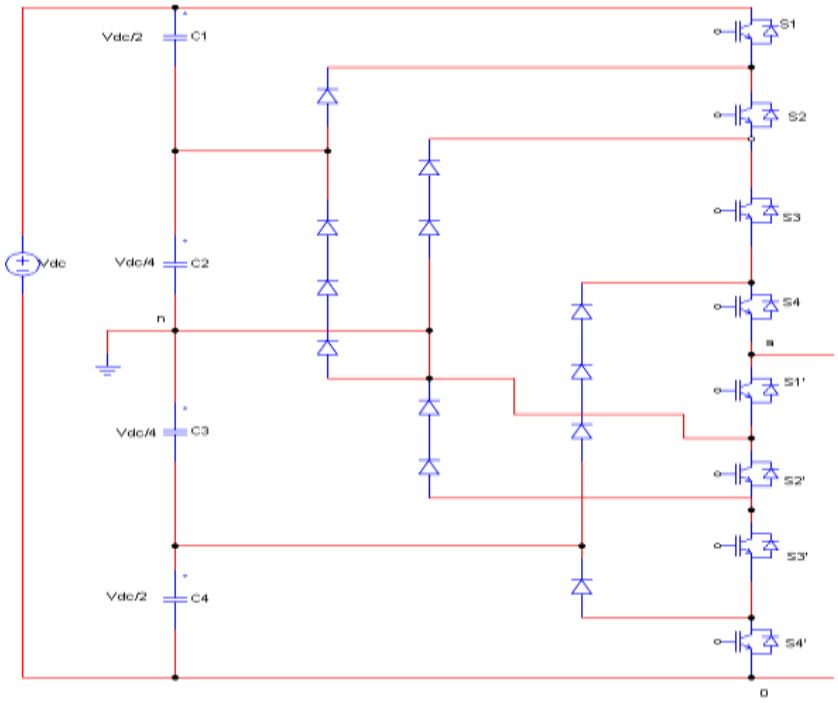


Fig (3.2): Five Level Diode Clamped Multi-Level Inverter Topology.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In the given circuit, the four complementary pairs are (S1, S1‘), (S2, S2‘),(S3, S3‘), and (S4, S4‘).

(b) Flying Capacitor Multilevel Inverter

The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs. gives the size of the voltage steps in the output waveform. Fig 1.3 shows single phase n- level configuration of capacitor clamped inverter. An *n*-level inverter will

require a total of (n-1)×(n-2)/2 clamping capacitors per phase leg in addition to (n-1) main dc bus capacitors**.** The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to V_{dc}/(n-1), for an n-level inverter. The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter.

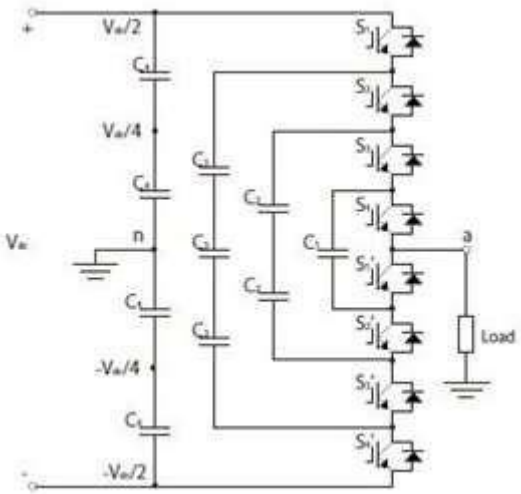


Fig (3.3): Flying Capacitor Multilevel Inverter

Advantages

- Large amount of storage capacitors can provide capabilities during power outages.
- Both real and reactive power flow can be controlled.

Disadvantages

- Excessive number of storage is required when the number of level increases.
- They are bulky
- The inverter control can be very complicated.

(c) Z-Sources Multilevel Inverter

A Z source network consists of a diode D on the DC side and a Z source of X shape consisting of two capacitors C1 and C2 and two inductors L1 and L2. The diode D presents forbidden reversed current flow. A three phase Z inverter will assume nine states

i.e. six active states where exchange of instantaneous power between load and DC circuit takes place and three null states when the load is shorted simultaneously by lower and upper groups of transistors and this state is defined as Shoot through.

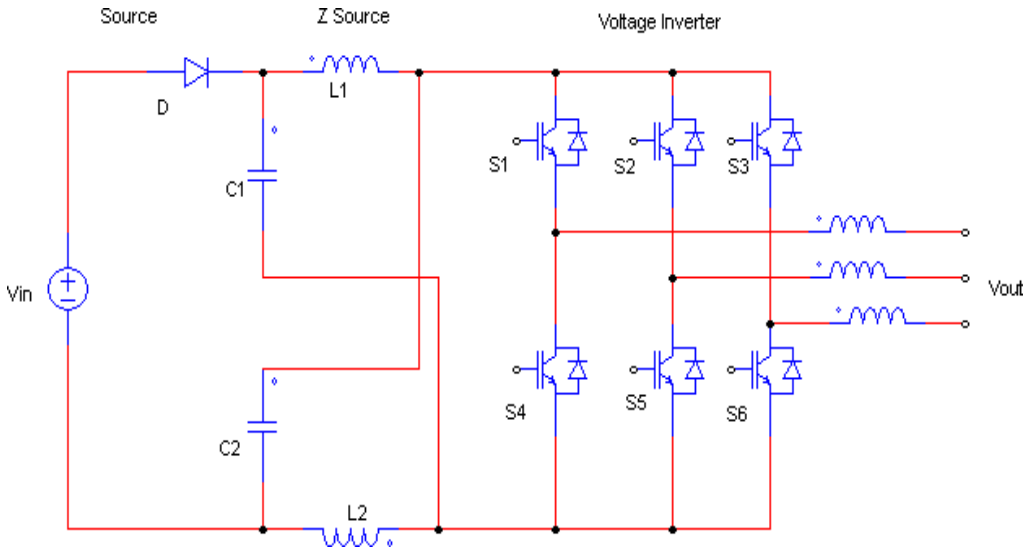


Fig (3.4): Basic Circuit Of Z-Source with A Voltage Inverter

The Shoot Through can be generated in seven ways

- Independently through every branch
- Simultaneously through two of the branches
- Simultaneously through all the three branches

The main and unique characteristic of Z inverter is the shoot through state which permits one raise output voltage above the input voltage Vin.

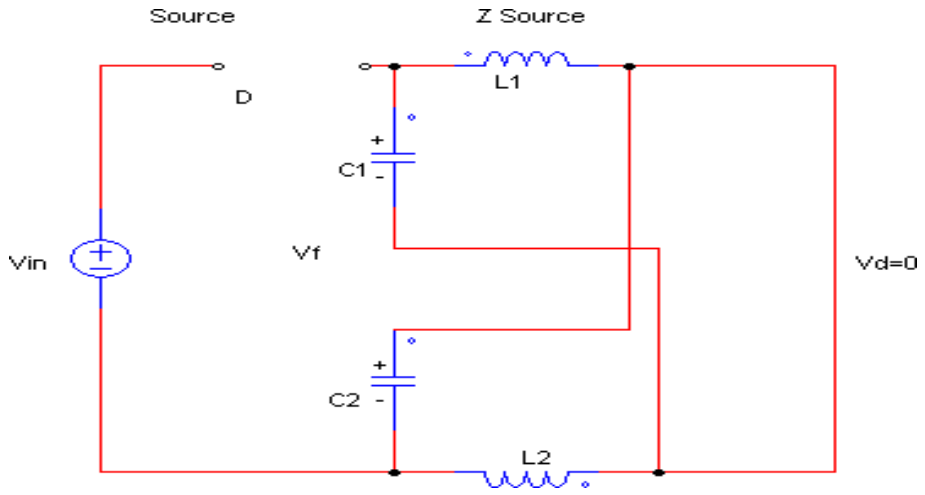


Fig (3.5): Shoot Through State Of Z-Source Network

The diode D will be polarized reversely and does not conduct the inverter bridge since output voltage V_d=0. The chokes L1 and L2 get energy which is stored in the capacitors C1 and C2.

$$V_c\text{-}V_l = 2V_c\text{-}V_{in} \quad (1.1)$$

The diode D conducts and voltage V_d increases stepwise from 0 to its maximum. Fig.1.6 shows the non shoot through state of the Z source network

$$V_l = V_{in} - V_c, \quad V_f = V_{in}, V_d \quad (1.2)$$

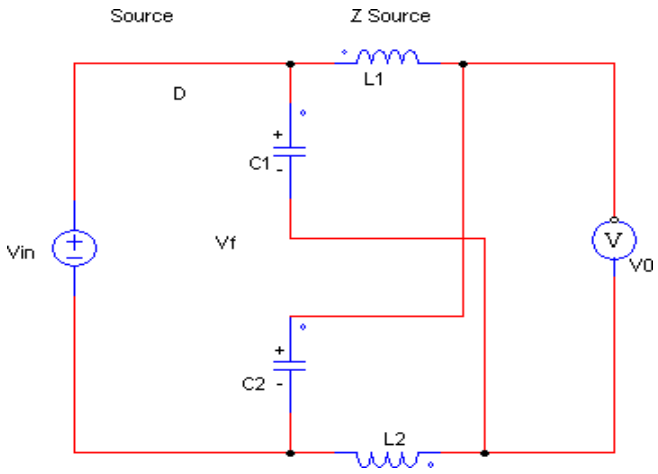


Fig (3.6): Non-Shoot Through State of Z Source Network

Advantages of the Z-converters are:

- Secures the function of increasing and decreasing of voltage in the one-step energy processing (lower costs and decreased losses).
- Resistant to short circuits on branches and to opening of the circuits that reduce EMI distortions.
- Relatively simple start-up (lowered current and voltage surges).

(d) Cascaded Multilevel Inverter

Each single DC sources is associated with a single H-bridge converter & AC terminal voltages of different level converters are connected in series & can generate three different voltage outputs,+V_{dc}, -V_{dc} and zero. This is explained with the help of fig 1.7.

The AC outputs voltage waveform is the sum of the individual converter outputs. Cascaded multilevel inverter is having an unique and attractive topology such as simplicity in structure, usage of less number of components etc. Their main advantage is that they can generate output voltages with extremely low distortion and lower voltage stresses (dv/dt). They can operate with a lower switching frequency. Cascaded Multilevel Inverter consist of series of H-bridge (Full Bridge) Inverter units. Each bridge will be fed from a separate DC source which may be obtained from batteries, fuel cells, or solar cells. The function of this multilevel inverter is to produce a desired voltage from several Separate Dc Sources (SDCSs).The ac terminal voltages of different level inverters are connected in series. This inverter does not require voltage-clamping diodes or voltage-balancing capacitors unlike in the diode-clamp or flying-capacitors inverter, hence inverter has more advantages. Each inverter level can generate three different voltage outputs $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4.To obtain $+V_{dc}$, switches S1 and S4 are turned on whereas $-V_{dc}$ can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series so that the generated voltage waveform will be the sum of all the inverter output voltages.

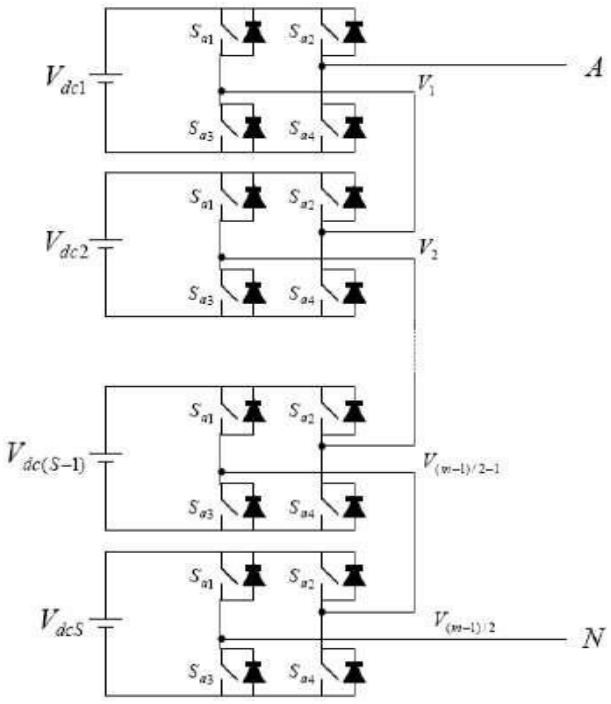


Fig (3.7): Equivalent Circuit of Cascaded Multilevel Inverter.

Applications of Cascaded H-Bridge Multilevel Inverter

- Motor drives
- Active filters
- Electric vehicle drives
- DC power source utilization

For our project we use cascaded-H inverter, because it has following advantages when compared to other multi-level inverters.

1. Better waveform quality of output voltage (more sinusoidal).
2. Reduced dV/dt, leading to reduction in EMI.
3. Lower voltage rating devices can be used.

Chapter-04
SEVEN LEVEL INVETRTER

4.1 Introduction:

Multi-level inverter is a modification of the conventional two-level inverter which will be capable of delivering desired number of AC voltage levels at the output with the help of multiple DC voltage inputs. With increased number of output voltage levels, we will get a smoother output waveform. Higher the number of voltage levels, smoother the output waveform. With smoother output, we get higher efficiency, less Total Harmonic Distortion (THD), lower switching loss and stress on electrical components. Thus, multi-level inverters require small filters which in turn reduce the cost of the inverters. Additionally, multi-level inverters are compact and lighter. Multi-level inverters are mostly used for high voltage and nigh power applications.

A seven-level inverter is a power electronic device which is capable of providing seven alternating voltage levels at the output using multiple DC voltage as input. The concept of seven-level inverter is kind of modification of conventional five level inverter. In seven level inverter we do not have to deal with the smaller number of levels instead in order to create a smoother output waveform, more than two voltage levels are combined together. Seven level inverters are very promising; they have nearly sinusoidal output voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverter.

4.2 Proposed Topology Description:

The initial inverters developed were only of two levels. The technology got advanced and multi-level inverters were developed which can produce a desired output of different voltage levels from many input DC voltage sources. As the number of levels increase, the output attains near sinusoidal wave shape reducing the harmonics. The more the number of levels, the lesser is the harmonic content. Hence MLIs are becoming popular in applications where high voltage and high power are used. The disadvantage of MLI is that it involves many switches which require corresponding gate drive circuitry. This in turn increases the expenditure. Therefore, the reduction in number of switches is essential. In this proposed topology we reduced the number of switches required for developing a seven-level inverter. A

conventional 7-level cascaded MLI requires 12 switches and the number of switches can be reduced. Here, in our proposed inverter topology, we developed a seven-level inverter with six switches only. S1, S2, S3, S4 are unidirectional whereas S5 and S6 are bi directional switches.

A fault tolerant single phase seven level inverter is proposed in this project for islanded photovoltaic (PV) generation system. This inverter is proposed for offshore PV applications. The topology has the capability of maintaining same output voltage magnitude in case of switch open circuit fault and/or source open or short circuit fault with slightly reduced number of voltage levels. This helps in supplying uninterruptable power to essential loads even under fault condition. The topology also has the major advantage of energy balancing between two batteries using redundant switching states. This helps in reducing difference in state of charge of batteries during partial shading or hotspots on PV panels. Here the inverter is fed with two separate PV strings of equal power ratings with associated maximum power point tracking (MPPT) converter for each string.

The proposed seven level inverter topology here is a slight modification of seven level inverter and is fault tolerant. It comprises of single-phase conventional H-bridge inverter, two asymmetrical DC voltage sources, two bidirectional switches and load. The modified H-bridge topology is significantly advantageous over other topologies i.e. less power switch, power diodes, and less capacitors for inverters of the same number of levels. The inverter we use here is of cascaded H- bridge type. We use this type of inverter because these inverters require. less number of switches in each switching level. The additional advantage of using this type of inverter is reduced Total Harmonic Distortion (THD). The only disadvantage using cascaded H-bridge inverter is it needs isolated DC voltage sources.

4.3 Block Diagram of Proposed Seven Level Inverter:

A single-phase DC-AC converter with fault tolerance ability for islanded PV systems is shown above. This seven-level inverter is a modification of five level inverter with the same number of switches but the DC sources are made to be asymmetrical whereas this system acts as a five-level inverter if we keep symmetrical DC sources.

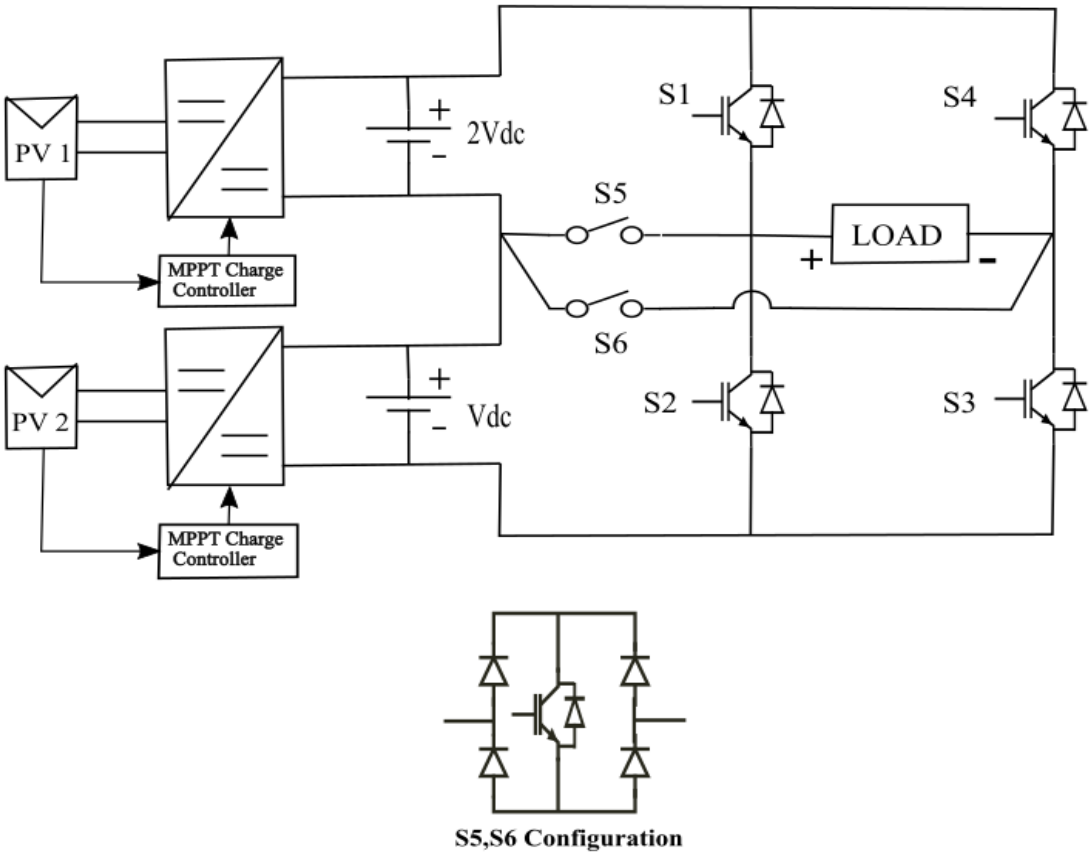


Fig (4.1). Circuit diagram of Seven Level Inverter

There are two separate PV sources each connected to a MPPT charge controller and a DC-DC boost converter as shown in fig above. The output of the two boost converters are fed to a DC voltage sources and these acts as power sources for the seven-level inverter. The system has four unidirectional switches S1, S2, S3 and S4 connect in cascaded H bridge style to have less total harmonic distortion. The switches S5 and S6 are bidirectional switches and their configuration is also described in the above figure.

4.4 Simulation Parameters

Supply parameters:

$V_{dc1} = 100\ KV$

$V_{dc2} = 200\ KV$

$V_{rms} = 215\ V$

Frequency = 50 Hz

Switching frequency = 2 Khz

Load parameters:

Resistance = 100 Ω

Inductance = 30 mH

4.5 Operation of Seven Level Inverter:

The given single phase seven-level inverter is capable of producing seven levels (Vdc, 2Vdc, Vdc, 0, −Vdc, −2Vdc, −Vdc) in output from the two DC sources (Vdc and 2Vdc) in the input. As the DC sources here are placed in an asymmetrical way, it is easy to produce seven levels. If we modified the arrangement to symmetrical way, the inverter acts as five level inverter only. All the switches in the circuit are triggered in a manner that they provide seven levels by using Phase Disposition Pulse Width Modulation Technique. The output wave of seven level inverter is shown below.

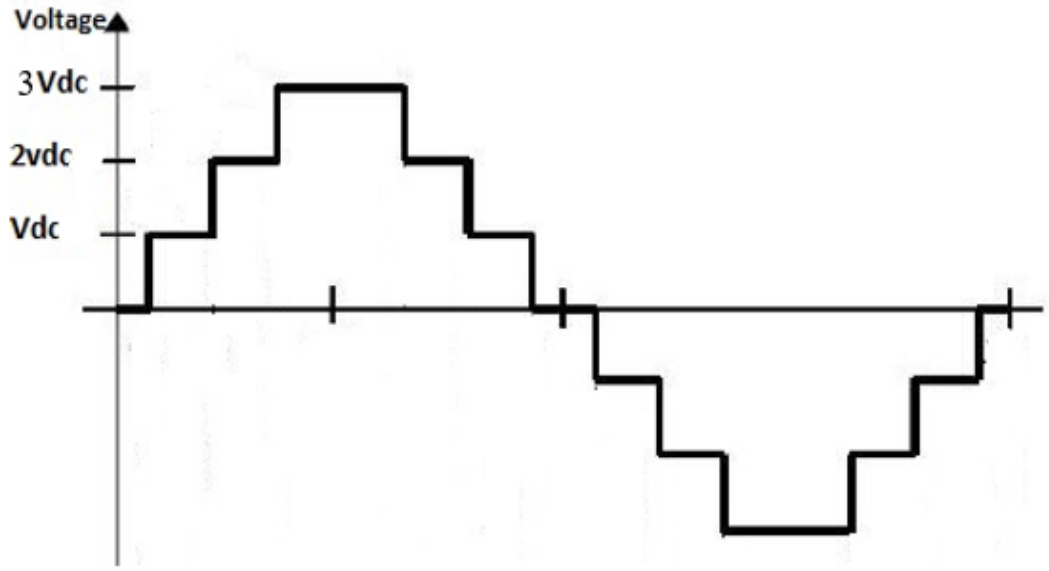


Fig (4.2): Output wave form of a Seven level inverter

Mode I operation: Maximum positive output (3Vdc):

S1 is ON connecting the load positive terminal to 2Vdc, and S3 is ON connecting the load negative terminal to Vdc. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc. Fig. 4(a) shows the current paths that are active at this stage.

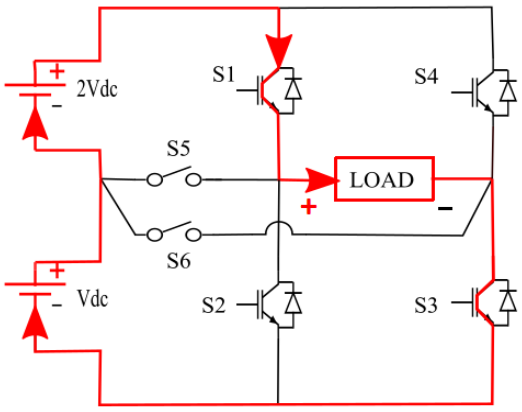


Fig (4.3): Path for Positive output (3Vdc)

Mode II operation: Positive output (2Vdc):

S1 is ON connecting the load positive terminal to 2Vdc and S6 is ON connecting the load negative terminal to Vdc. All other controlled switches are OFF. Fig. 4(a) shows the current paths that are active at this stage.

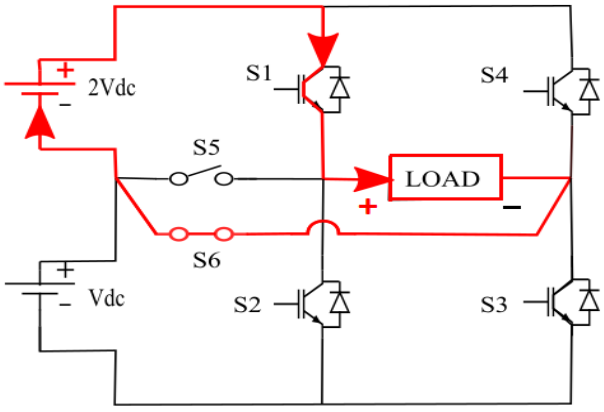


Fig (4.4): Path for Positive output (2Vdc)

Mode III operation: Positive output (Vdc):

S5 is ON connecting the load positive terminal to Vdc and S3 is ON connecting the load negative terminal to Vdc. All other controlled switches are OFF. Fig. 4(a) shows the current paths that are active at this stage.

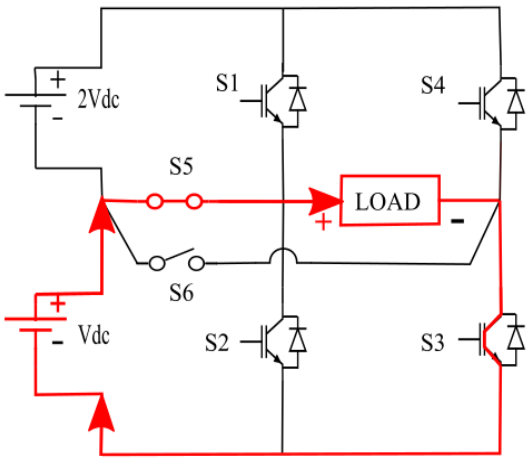


Fig (4.5): Path for Positive output (Vdc)

Mode IV operation: Zero output:

S5 is ON connecting the load positive terminal to neutral and S6 is ON connecting the load negative terminal to neutral. All other controlled switches are OFF. Fig. 4(a) shows the current paths that are active at this stage.

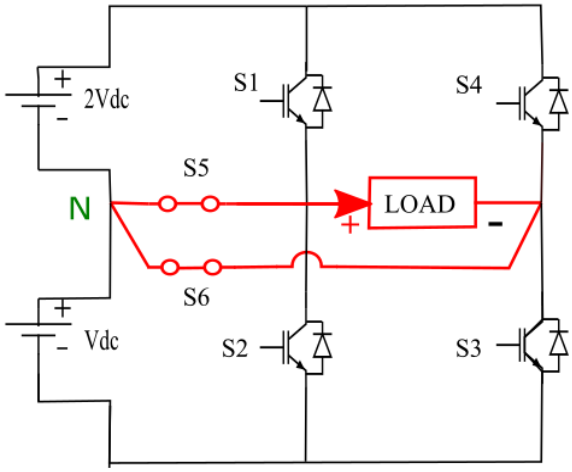


Fig (4.6): Path for Zero output (0Vdc)

Mode V operation: Negative output (-Vdc):

S6 is ON connecting the load negative terminal to Vdc and S2 is ON connecting the load positive terminal to Vdc. All other controlled switches are OFF. Fig. 4(a) shows the current paths that are active at this stage.

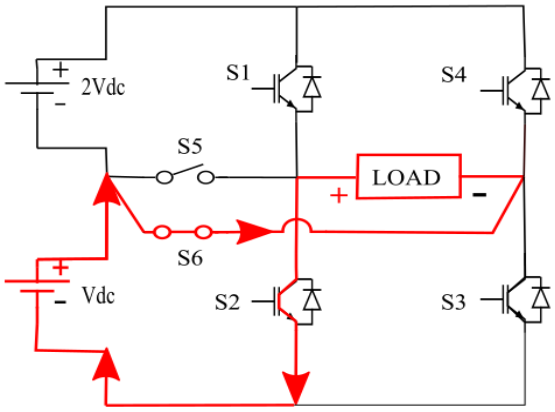


Fig (4.7): Path for Negative output (-Vdc)

Mode VI operation: Negative output (-2Vdc):

S4 is ON connecting the load negative terminal to 2Vdc and S5 is ON connecting the load positive terminal to 2Vdc. All other controlled switches are OFF. Fig. 4(a) shows the current paths that are active at this stage.

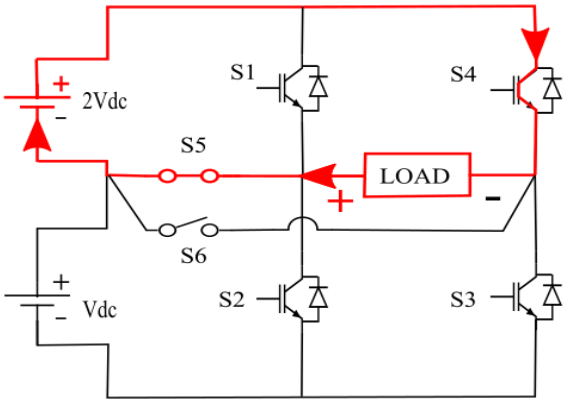


Fig (4.8): Path for Negative output (-2Vdc)

Mode VII operation: Negative output (-3Vdc):

S4 is ON connecting the load negative terminal to 2Vdc and S2 is ON connecting the load positive terminal to Vdc. All other controlled switches are OFF. Fig. 4(a) shows the current paths that are active at this stage. The paths for all the seven levels of output are shown below.

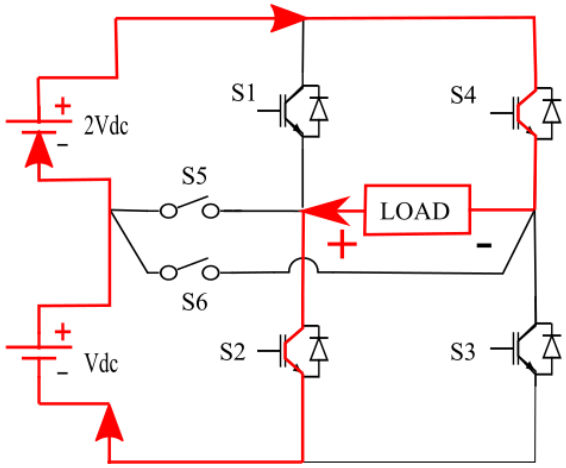


Fig (4.9): Path for Negative output (-3Vdc)

Chapter-05
CONTROL PWM TECHNIQUES

Pulse width modulation techniques are used to design the width of pulse sequences so that a fundamental component voltage with specified magnitude and phase emerges, and harmonics are shifted towards higher frequency bands.

A PWM waveform consists of a series of positive and negative pulses of constant amplitude but with variable switching instances. The typical goal is to generate a train of pulses such that the fundamental component of the resulting waveform has a specified frequency and amplitude. The converter switches are turned on and off several times during each half cycle and the output voltage is controlled by varying the width of the pulses.

Pulse width Modulation (PWM) techniques for two level inverters have been studied extensively during the past decades. Many different PWM methods have been developed to achieve the following aims;

- Wide linear modulation range
- Reduced switching loss
- Total harmonic distortion in the spectrum of switching waveform are less
- Less memory spaces
- Less computation time on implementing in digital processors for proposed work.

A number of modulation strategies are used in multilevel power conversion applications. They can generally be classified into modulating signals and carrier redistribution signal.

Pulse width Modulation, or PWM, is a technique obtaining analog results with digital means. Digital control is used to create a square wave, a signal switched between on and off.

Purpose of PWM:

1. Control ac-side fundamental voltage (Dc bus voltage being fixed and possibly unregulated).
2. Mitigation of harmonic voltages and their harmful effects.

5.1 Types of Modulating signals

These are classified as

- Sinusoidal PWM (SPWM)
- Third Harmonic injection PWM (THPWM)
- Modified Space Vector PWM (MSVPWM)

5.1.1 Sinusoidal PWM

This is the most widely accepted PWM technique, where a triangular wave is compared with a sinusoidal reference known as modulating signal, as shown below.

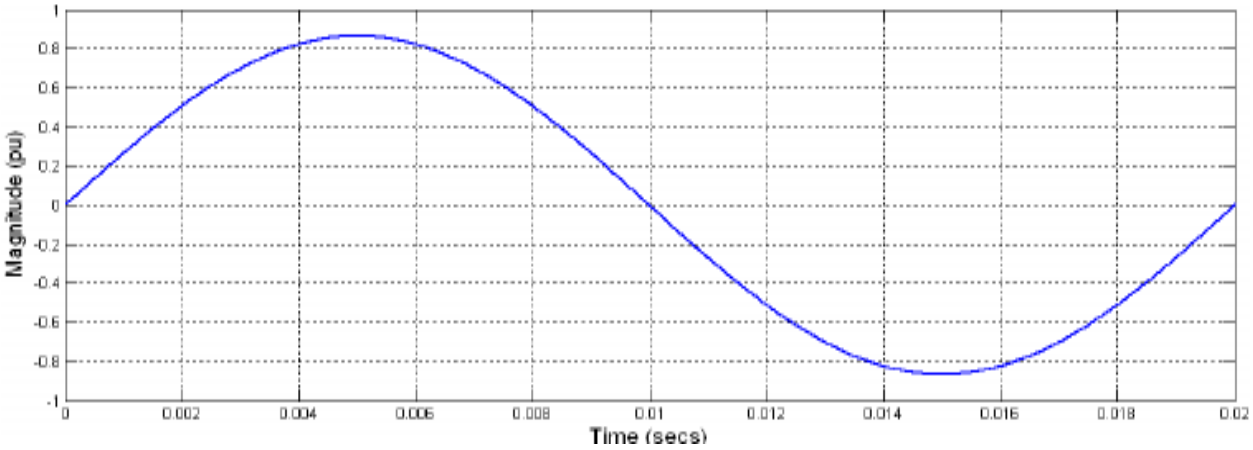


Fig (5.1): Sinusoidal modulating signal control technique

5.1.2 Third Harmonic injection PWM

A method to improve the gain of the pulse width modulator, in a multilevel inverter is to inject a third harmonic. This technique is derived from conventional sinusoidal PWM with the addition of a 17% third harmonic component to the sine reference waveform as shown below

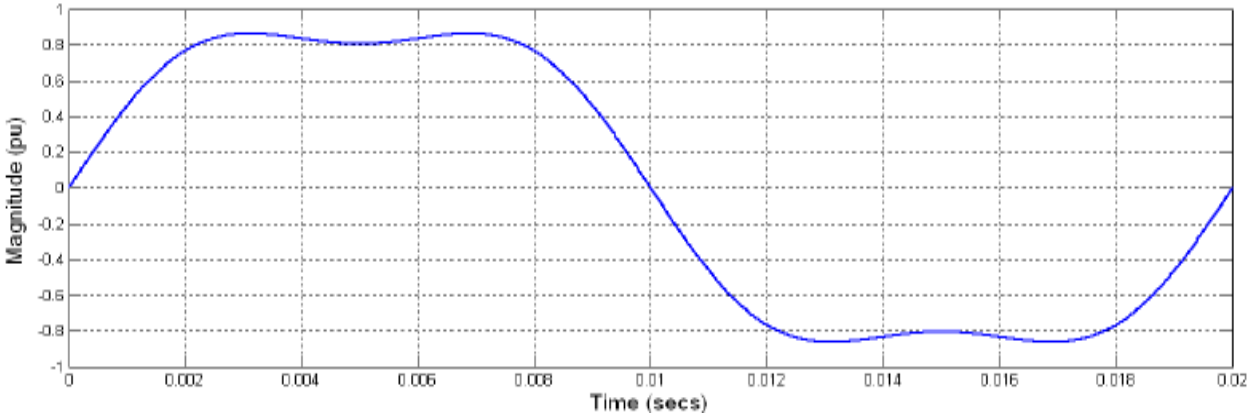


Fig (5.2): Third Harmonic injection modulating signal control technique.

5.1.3 Modified space vector PWM

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other. To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, Voffset1, is added to the reference phase voltage, where the magnitude of Voffset1 is given by

$$\text{V offset} = \frac{-(\text{Vmax} + \text{Vmin})}{2}$$

Vmax = maximum magnitude of the three sampled reference phase voltages

Vmin = minimum magnitude of the three sampled reference phase voltages, in a sampling interval.

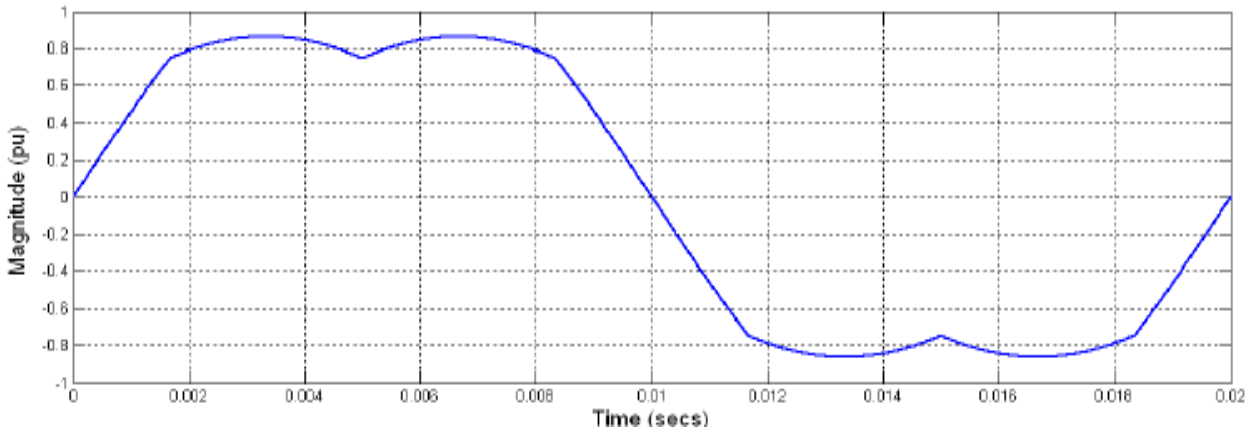


Fig (5.3): Modified space vector modulating signal control technique.

Carrier-Based Modulation technique

Implementation of carrier-based PWM technique exists in two methods. The direct digital technique has a pre-calculated inverter state, time length of each carrier, and modulation cycle employing space vector theory. The indirect technique works with carrier triangle intersection technique. Reference modulation wave with a low frequency is compared with high-frequency triangular carrier wave and the intersection results in pulse switching sequence.

In the operation of MLIs, carrier triangular intersection technique is easy to implement with modulation wave comparison strategy. Bipolar sinusoidal wave, unipolar sinusoidal

wave, and saw tooth wave are preferable for the modulation wave.

Single triangular carrier wave is suitable for two-level and three-level traditional MLIs. In case of five levels and more than five levels, multi-carrier triangular waves are used for the generation of levels. Based on position of multi-carrier waves, phase shift and level shift PWM techniques are proposed

5.2 Multicarrier PWM techniques

Multicarrier PWM techniques entail the natural sampling modulating or reference waveform typically being sinusoidal same as that of output frequency of the inversion system, through several carrier signals typically being triangular waveforms of higher frequencies of several kilo Hertz

5.2.1 Phase Disposition PWM technique:

The Phase disposition PWM technique is to use the several carriers with single modulating waveform. In this all the (n-1) carrier for n level inverter are in phase and the carriers are disposed so that the bands they occupy are contiguous. The modulation wave is centred in the middle of the carrier set. The PWM pulses are generated when the magnitude of the reference signal is greater than the triangular signals.

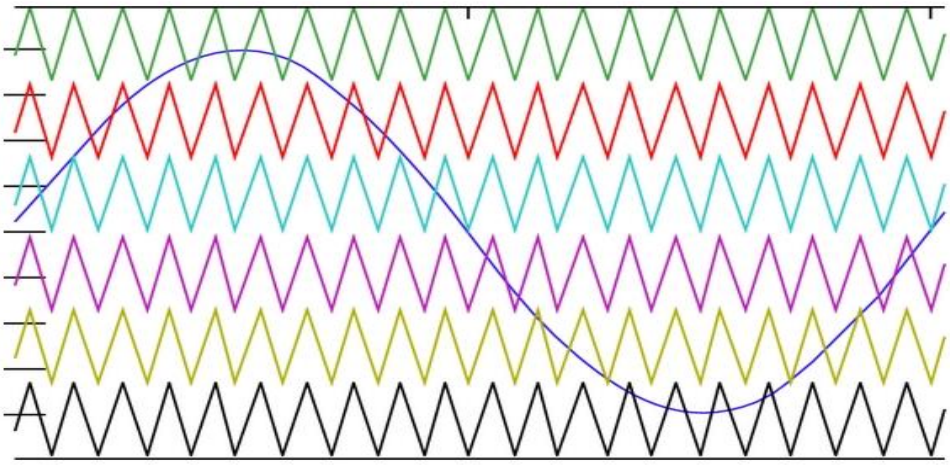


Fig (5.4): Wave form of Phase Disposition

5.2.2 Phase Opposition Disposition (POD)

The carrier waveforms are all in phase above and below the zero-reference value however, there is 180 degree phase shift between the ones above and below zero respectively, for various modulating signals. The significant harmonics, once again, are located around the

carrier frequency (fc) for both the phase and line voltage waveforms.

Unipolar sinusoidal PWM method is not possible for POD PWM technique due to no below zero reference value in unipolar modulation wave.

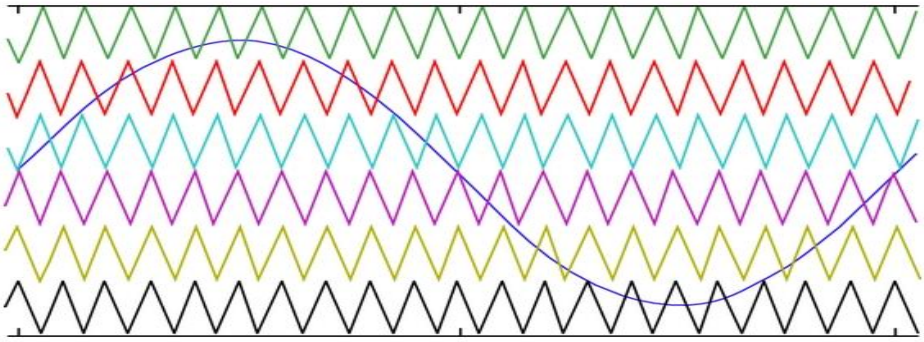


Fig (5.5): Wave form of Phase Opposition Disposition

5.2.3 Alternative Phase Opposition Disposition (APOD)

This technique requires each of the (n-1) carrier waveforms, for an n-level phase waveform, to be phase displaced from each other by 180 degrees alternately for various modulating signals. The most significant harmonics are centred as sidebands around the carrier frequency fc and therefore no harmonics occur at fc.

All carrier waves are compared with the low-frequency modulation bipolar sinusoidal wave or unipolar sinusoidal wave with preferred amplitude and frequency measured based on the level of Multi-level Inverter.

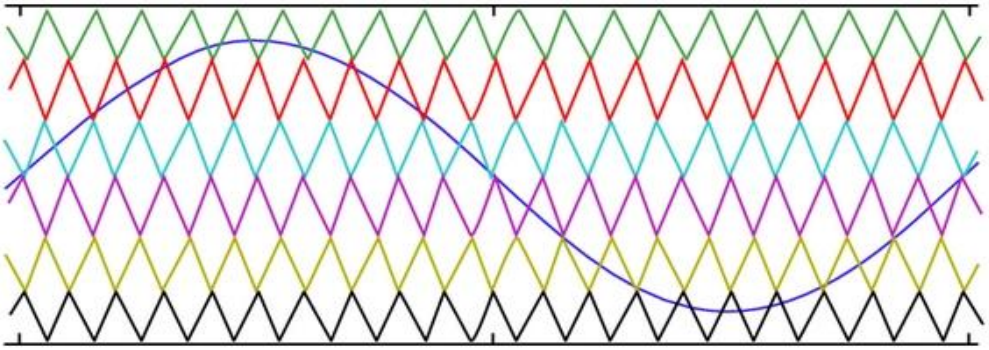


Fig (5.6): Wave form of Alternative Phase Opposition Disposition.

5.3 Advantages of PULSE WIDTH MODULATION TECHNIQUES

1. Using Pulse Width Modulation techniques lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are also minimized. Both the output voltage and frequency control is possible in a single power stage of the inverter without any additional components.
2. The presence of constant DC supply permits the parallel operation of several independent Pulse Width Modulation inverters on the same rectifier power supply.
3. Pulse Width Modulation inverter has a transient response which is much better than that of quasi-square wave rectifier.
4. The commutative ability of Pulse Width Modulation inverters remain substantially constant compared to variable dc link inverter, irrespective of the voltage and frequency settings
5. The power factor of the system is good, as a diode rectifier can be employed on the link side.

For a Seven Level Inverter, the total harmonic distortion (THD) is very less for Phase Disposition (PD) PWM technique than Phase Opposition (PO) and Alternate Phase Opposition-Disposition (APOD). The THD value for these PWM techniques is 18.05% for Phase Disposition, 22.48% for Phase Opposition and 25.20% for Alternate Phase Opposition-Disposition. Due to this advantage, here in this topology, Phase Disposition PWM technique is used for the seven-level inverter used in this project.

CHAPTER- 06

MATHAMETICAL MODELLING

Mathematical modelling of circuit has total control over the simulation process that gives a smaller execution time. On the other hand it takes long time for the initial setup as the user has to develop all possible composition of differential and algebraic equations that results in troubleshooting and debugging of codes developed with the mathematical models but for circuit modelling setup time is small in the beginning and the changes can be made easily[4] .On the other side, it has little control on the simulation process that results in long simulation time.

In comparison of all models, mathematical circuitry technique has a total control over the model and there is no limitation about the model and on the other hand it is difficult to implement the hardware, in addition to this it is difficult to model non-ideal model but most important thing is it is restricted to time domain analysis only. When it comes to transfer function technique it is not difficult to simulate and implement and very important thing is that here both time domain and frequency domain analysis can be made so here because of frequency domain modelling system can be studied with respect to its stability analysis and hence the performance of the system can be estimated so that is the advantage of this modelling technique. On the other hand, it is applicable only for single input and single output model and also it is difficult for nonideal model and it requires supplementary tool box for text programming. When it comes to state-space modelling it is exactly same as transfer function modelling with respect to pros and cons, however state space modelling allows to model the system with multiple input and multiple output.

When it comes to literature survey, there are many types of modelling followed by simulation literatures which are there for boost converter but it is only for non-ideal so it will not be good for education. As of now no literature gives complete modelling followed by simulation and their computational implementation techniques for boost converters but here all four modelling techniques followed by their simulation along with their computational implementation are done for boost converter and results are clearly shows that they are perfectly overlapping each other. There are many simulation tools like PSim, MATLAB, PSpice, PSCAD and so on are available in the market for power converter modelling and simulation.

It is a major method of modelling and simulation of systems which oversee the laws of physics. Different forms of assumption may be considered in mathematical modelling process based on the particular scenario. State space modelling technique is used for optimal control problems whereas transfer function technique is used for transient response or frequency response analysis of SISO transfer function modelling technique is preferred than any other modelling technique. As soon as mathematical model is derived for the given system various computational methods can be used synthesis and analysis.

6.1 Mathematical Modelling of PV cell.

Solar cells consist of a p-n junction fabricated in a thin wafer or layer of a semiconductor material. In the dark, the I-V output characteristic of a solar cell has an exponential characteristic like that of a diode. When photons from the solar energy hits the solar cell, with energy greater than band gap energy of the semiconductor, electrons are knocked loose from the atoms in the material, creating electron-hole pairs. These carriers are swept apart under the influence of the internal electric fields of the p-n junction and create a current proportional to the incident radiation. When the cell is short circuited, this current flows in the external circuit and when open circuited, this current is shunted internally by the intrinsic p-n junction diode. The characteristics of this diode therefore set the open circuit voltage characteristics of the cell. The photovoltaic modules are made up of silicon cells. The silicon solar cells give output voltage of around 0.7V under open circuit condition. The current rating of the modules depends on the area of the individual cells. Higher the cell area, high is the current output of the cell.

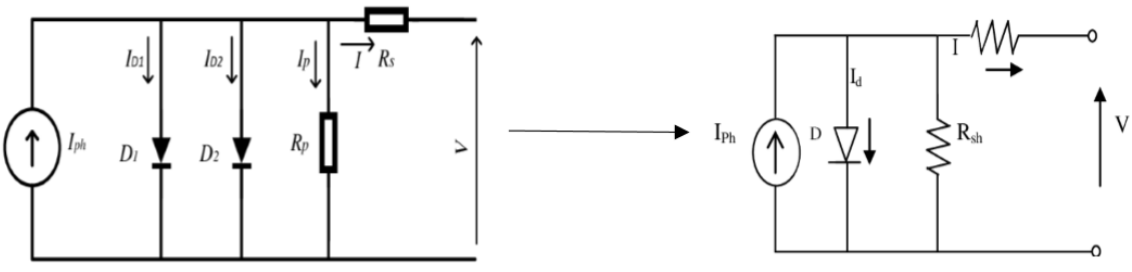


Fig (6.1): Double diode model

Fig (6.2): Single diode model

$$I = I_{ph} - I_{s1}\left[e^{\frac{q(V+IRse)}{kT}} - 1\right] - I_{s2}\left[e^{\frac{q(V+IRse)}{AkT}} - 1\right] - \frac{(V+IRse)}{Rsh}$$

$$I = I_{ph} - I_s\left[e^{\frac{q(V+IRse)}{AkT}} - 1\right] - \frac{(V+IR_{se})}{R_{sh}}$$

$$Iph = Isc * \frac{Irr}{1000} * [1 + (Tcell - Tref) * K)]$$

Where

Iph is the photo diode current generated by solar cell mainly depending upon irradiance and temperature.

Is1 is the saturation current of diode D1 due to diffusion mechanism.

Is2 is the saturation current due to recombination in space charge layer.

Rsh is the shunt resistance representing shunt current leakage to the ground;

Rse is the series resistance representing contact resistances etc.,

k is Boltzmann's constant, 1.38x10-23 J/K.

q is the electron charge, 1.6 x 10-19 C.

Tc is the Cell working temperature.

V is the terminal voltage of solar cell.

However, the above model can be further simplified by omitting the current Is2. The reverse saturation current of diode D2 due to recombination of charge carrier in space charge layer is neglected as the amount of recombination is less and negligible. This assumption is very much acceptable especially under standard test conditions and induces errors only at very low values of irradiation such as 100W/m2.

6.2 Mathematical modelling of Boost Converter:

Here mathematical model is obtained for the boost converter circuit based on theory of its working principle. Ideal model of non-isolated DC-DC Boost converter is considered for simplifying the complexity of modelling. Fig. shows the basic boost converter and it is used in this entire project for all four modelling techniques. The boost converter is made with two energy storage elements, one n-channel MOSFET and one diode. During switching process MOSFET and diode work compliment to one another i.e. When MOSFET is ON diode is OFF and when diode is ON, MOSFET is OFF at a given interval of time.

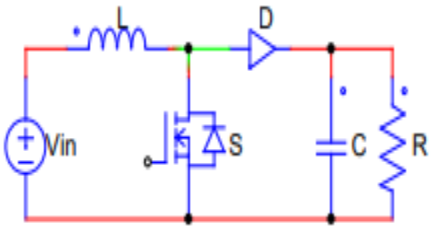


Fig (6.3): Boost Converter

The mathematical modeling begins with storage elements capacitor and inductor in the boost converter as shown in Fig.1. inductor voltage and capacitor current are given in below equations respectively.

$$v_L = L\frac{di_L}{dt}$$

$$i_c = c\frac{dv_c}{dt}$$

The boost conversion begins when the switching process starts, which results in two forms of circuits as shown in Figures

While inductor VL for switching condition of ON and OFF are shown in (3) and (4) respectively.

$$v_L = (v_{in} - v_{out}) * \overline{PWM}$$

$$v_L = v_{in} * PWM$$

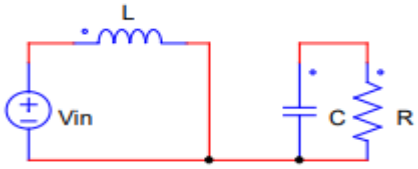


Fig (6.4): Boost converter in ON state during operation

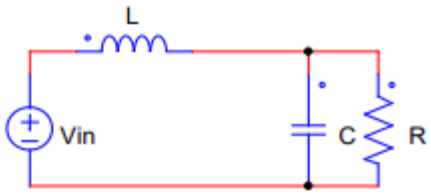


Fig (6.5): Boost converter in OFF state during operation

The current flowing through can be determined by integrating

$$i_L = \frac{1}{L}\int v_L dt$$

After obtaining, the current through the capacitor can be determined, where is the current through load resistor.

$$i_C = i_L - i_R$$

After obtaining i_c, the capacitor voltage can be calculated , which indicates the load voltage of the boost converter in case of ideal model.

$$v_C = \frac{1}{C}\int i_C dt$$

Transfer Function Modelling

Boost converter is modelled in S-domain using transfer function modeling technique. By referring boost converter when switch is OFF the total impedance can be given by the following equation.

$$Z_{total} = Z_1(S) + Z_2(S)$$

Z1(S) is given by

$$\frac{Vin(S)}{I(S)} = Z_1(S) = \left(R\frac{1}{Cs}\right) + Ls$$

$$\frac{Vin(S)}{I(S)} = \frac{RCLs^2 + Ls + R}{RCs + 1}$$

Inductor current is given by

$$I(S) = \frac{RCs + 1}{RCLs^2 + Ls + R}\, Vin(S) - - - - - (a)$$

Z2(S) is given by

$$\frac{Vout}{I(S)} = Z_1(S) = \frac{R}{RCs + 1}$$

Therefore, transfer function is given by

$$\frac{Vout}{Vin} = \frac{R}{RCLs^2 + Ls + R} - - - - - - - - (b)$$

Equation a and b are implemented in functional block of the transfer function as shown in fig below

Transfer function modelling technique for boost converter allows to analyse the stability of the boost converter thoroughly with system responses such as step, bode plot, pole and zero responses which are obtained from MATLAB Functions such as step(),bode() and pzmap() respectively.

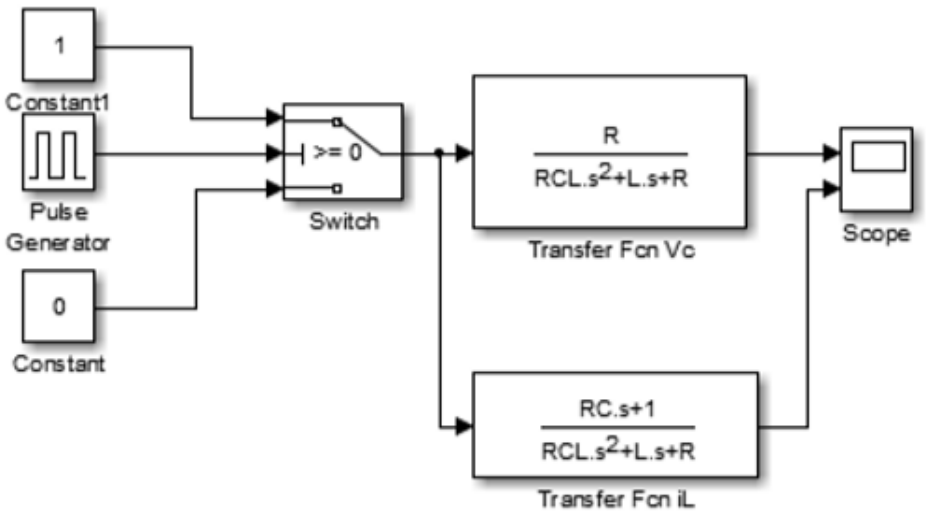


Fig (6.6): Transfer function model in functional block implementation

CHAPTER-07

POWER LOSS CALCULATIONS

Power losses in all of the switching devices can be divided in three groups

1. Conduction losses

2. Switching losses

3. Blocking(leakage) losses that is normally being neglected

Here in this project we use IGBT as switch. The IGBT power losses like the other switching devices can be divided in three groups, but leakages power losses are neglected.

7.1 IGBT power losses calculations

Conduction losses

Conduction losses occur in the switches and in the anti-parallel diodes. Conductions losses for the switches and the conduction losses for the anti-parallel diodes can be calculated by the following two equations.

$$P_{ci} = u_{CEO}.I_{Iav} + r_c.I^2{}_{Irms}$$

$$P_{cd} = u_{DO}.I_{Dav} + r_D.I^2{}_{Drms}$$

Where

Uce0 : on state zero current collector emitter voltage

Icav : average switch current

rc : collector emitter on-state resistance

Icrms : RMS switch current

uD0 : diode approximation with a series conduction of DC voltage sources

IDav : average diode current

rD : diode on-state resistance

IDrms: RMS diode current

uce0 and rc can be obtained from the diagram collector-emitter voltage versus collector current in the datasheet.

uD0 and rD can be obtained from the diagram forward voltage versus forward current in the datasheet.

Switching losses:

Switching losses are created in the switches and in the anti-parallel diodes. Switching losses for the switch can be calculated by

$$P_{swI} = \left(E_{onI} + E_{offI}\right).f_{sw}$$

$$P_{swD} = \left(E_{onD} + E_{offD}\right).f_{sw}$$

where

EonI : turn on energy losses in IGBT

EoffI : turn off energy losses in IGBT

EonD : turn on energy losses in diode

EoffD : turn off energy losses in diode that normally is being neglected

fsw : switching frequency

EonI, EoffI, EonD can be obtained from the datasheet of each IGBT.

In case, if we use MOSFETs instead of IGBTs, the power loss calculations goes like this.

7.2 MOSFET power losses calculations

The Mosfet power losses can as for the other switching devices can be divided in three groups when leakage power losses are neglected.

Conduction losses

Like in the IGBT, conductions losses are in the switches and in the anti-parallel diodes. Conduction losses for the switch and conduction losses for anti-parallel diode can be calculated by the following two equations.

$$P_{cM}=R_{DSon}.I^2{}_{Mrms}$$

$$P_{cd}= u_{DO}.I_{Dav} + r_D.I^2{}_{Drms}$$

where

RDSon: drain-source on-state resistance

IMrms: RMS value of the MOSFET on-state current

uD0: diode approximation with a series conduction of DC voltage sources

IDav: average diode current

RD: diode on-state resistance

IDrms: RMS diode current

RDSon should be obtained from the datasheet. uD0 and RD should be obtained from the diagram “Forward character of reverse diode” in the datasheet.

Switching losses

Switching losses include switch-on transient and switch-off transient. Energy losses for on transient and energy losses for off transient and Total switching losses can be calculated by the following equations.

$$P_{swM} = \left(E_{onM} + E_{offM}\right).f_{sw}$$

$$E_{onM} = V_{DD} \,.I_{Don}.\frac{t_{ri} + t_{fv}}{2} + Q_{rr}.V_{DD}$$

$$E_{onM} = V_{DD} \,.I_{Doff}.\frac{t_{ri} + t_{fi}}{2}$$

$$t_{rv} = \frac{t_{rv1} + t_{rv2}}{2}$$

$$t_{rv1} = \left(V_{DD} - R_{Dson} \,.I_{Don}\right).R_G \frac{C_{GD1}}{V_{(plateau)}}$$

$$t_{rv2} = \left(V_{DD} - R_{Dson} \,.I_{Don}\right).R_G \frac{C_{GD2}}{V_{(plateau)}}$$

where

VDD: Voltage across the MOSFET

IDon,IDoff : The current passing through MOSFET during on-time or off-time

Tri: Current rise time

Tfi: Current fall time

Trv: Voltage rise time

Tfv: Voltage fall time

CGD: Gate-Drain capacitor

V (plateau): Gate plateau voltage

RG: Gate resistance that is depends on the drive circuit of the MOSFET

If VDS is between 0, VDD/2 the gate-drain capacitance will be $C_{GD}(R_{Dson}.I_{on}) = C_{GD1}$. If VDS is between VDD/2, VDD the gate-drain capacitance will be CGD (VDD) = CGD2.

VDD, IDon, IDoff should be measured. tri, tfi, CGD, RG, V(plateau) values should be found in the MOSFET datasheet.

CHAPTER-8

SIMULATION IN MATLAB/ SIMULINK

8.1 Simulation Circuit diagram:

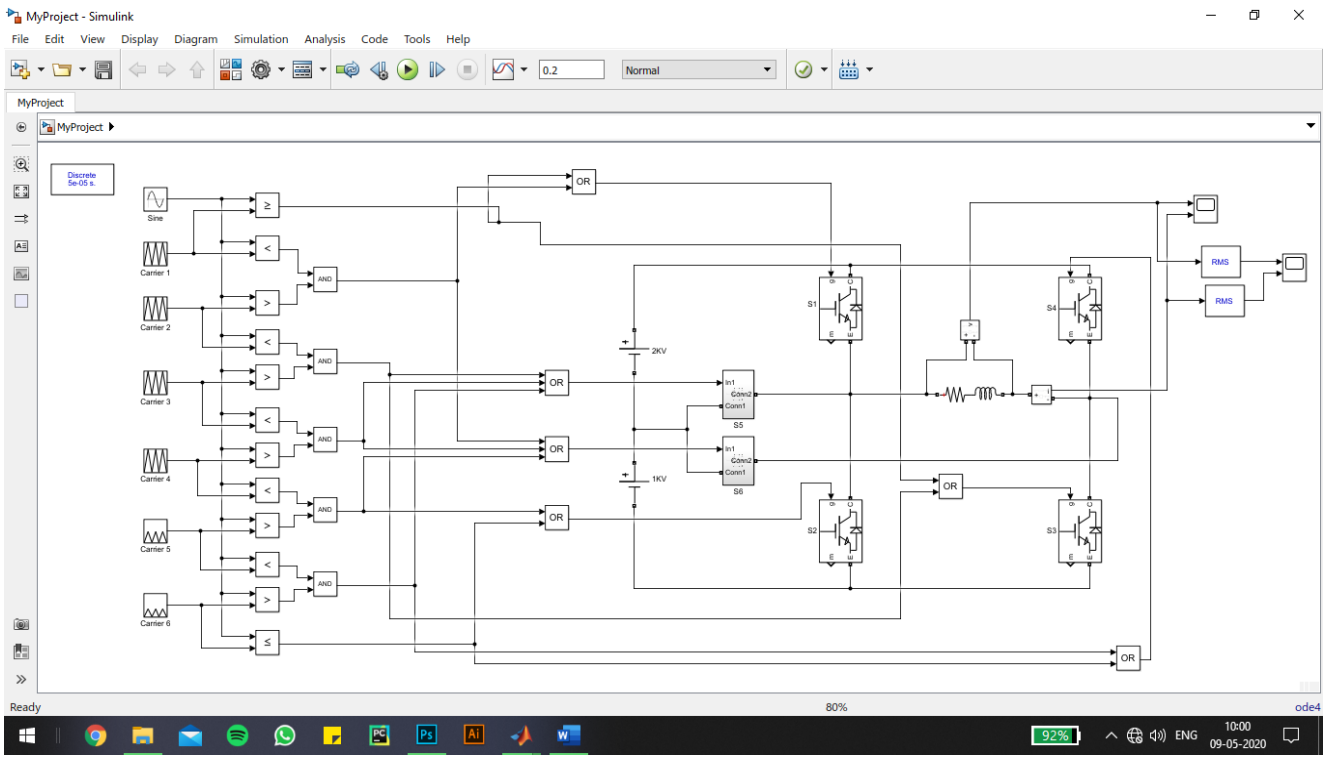


Fig (8.1) Simulation Circuit diagram of proposed Seven level inverter in MATLAB

The circuit diagram of the proposed seven level inverter is designed as per the block diagram of the model. Here in this simulation, as per PWM technique, for any inverter to generate n levels of output, it needs n-1 number of carrier waves. You can observe the 6 carrier waves and a sinusoidal modulating signal are used in the simulation. Let us consider the sine wave to be 'm' and 6 carrier waves to be Cr1 to Cr6. So, to generate seven levels the conditions will be:

For 3Vdc: m >= Cr1

2 Vdc: Cr2<m<Cr1

1Vdc: Cr3<m<Cr4

0Vdc: Cr4<m<Cr5

-1 Vdc: Cr5<m<Cr4

-2Vdc: Cr6<m<Cr5

-3Vdc: m<= Cr6

Simulation Parameters:

Supply parameters:

$V_{dc1} = 100\ KV$

$V_{dc2} = 200\ KV$

$V_{rms} = 215\ V$

Frequency = 50 Hz

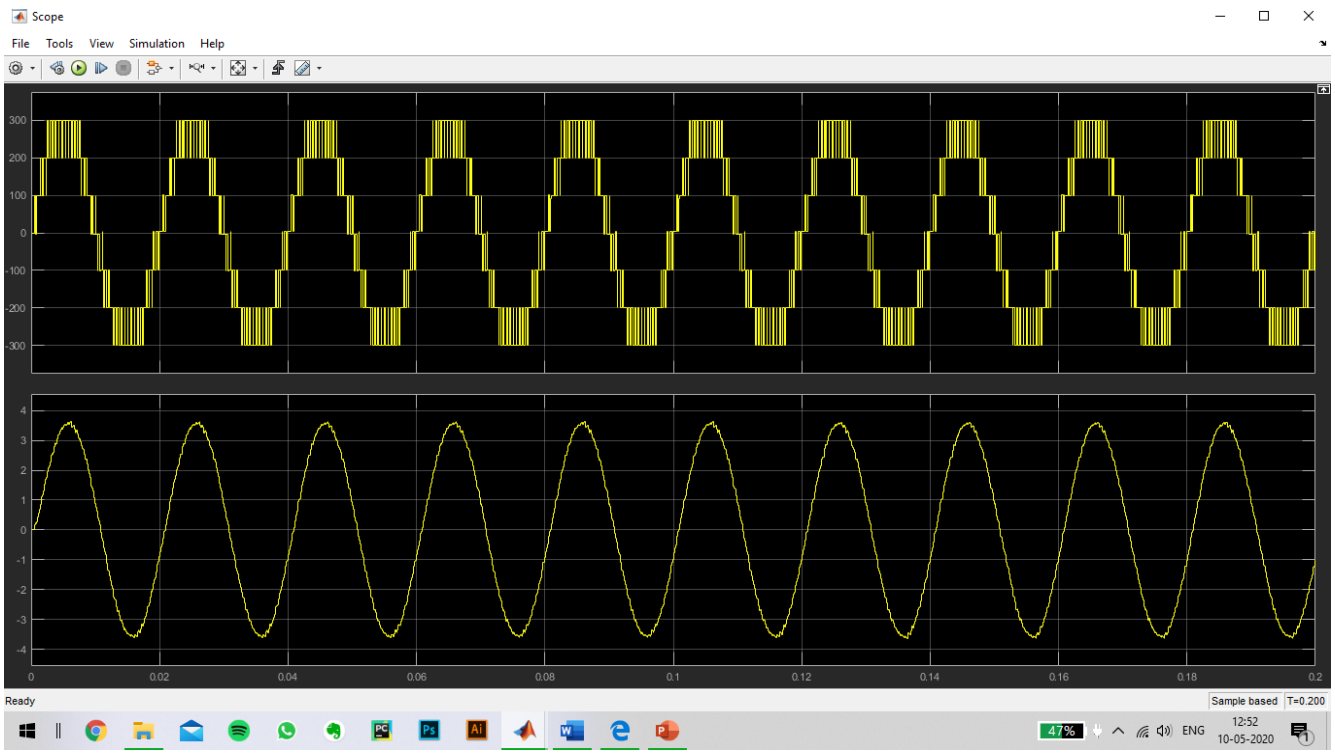
Switching frequency = 2 Khz

Load parameters:

Resistance = 100 Ω

Inductance = 30 mH

8.2 Output of the Simulated Proposed Seven Level Inverter



Fig(8.2): Output of the proposed Seven Level Inverter

8.3 Switching Combinations for Seven Level Inverter Operation

Voltage levels	S1	S2	S3	S4	S5	S6
Higher Voltage_Level (+3 V_{dc})	1	0	1	0	0	0
Second Higher Voltage Level (+2 V_{dc})	1	0	0	0	0	1
Third Higher Voltage Level (+1 V_{dc})	0	0	1	0	1	0
Zero Voltage Level (0 V_{dc})	0	0	0	0	1	1
Third Lowest Voltage Level (-1 V_{dc})	0	1	0	0	0	1
Second Lowest Voltage Level (-2 V_{dc})	0	0	0	1	1	0
Lowest Voltage Level (-3 V_{dc})	0	1	0	1	0	0

8.4 Fast Fourier Transform (FFT) Analysis of Output Voltage and Output Current:

A fast Fourier transform (FFT) is an algorithm that computes the discrete Fourier transform (DFT) of a sequence, or its inverse (IDFT). Fourier analysis converts a signal from its original domain (often time or space) to a representation in the frequency domain and vice versa. The DFT is obtained by decomposing a sequence of values into components of different frequencies. This operation is useful in many fields, but computing it directly from the definition is often too slow to be practical. An FFT rapidly computes such transformations by factorizing the DFT matrix into a product of sparse (mostly zero) factors. As a result, it manages to reduce the complexity of computing the DFT from , which arises if one simply applies the definition of DFT, to , where is the data size. The difference in speed can be enormous, especially for long data sets where *N* may be in the thousands or millions. In the

presence of round-off error, many FFT algorithms are much more accurate than evaluating the DFT definition directly or indirectly. There are many different FFT algorithms based on a wide range of published theories, from simple complex-number arithmetic to group theory and number theory

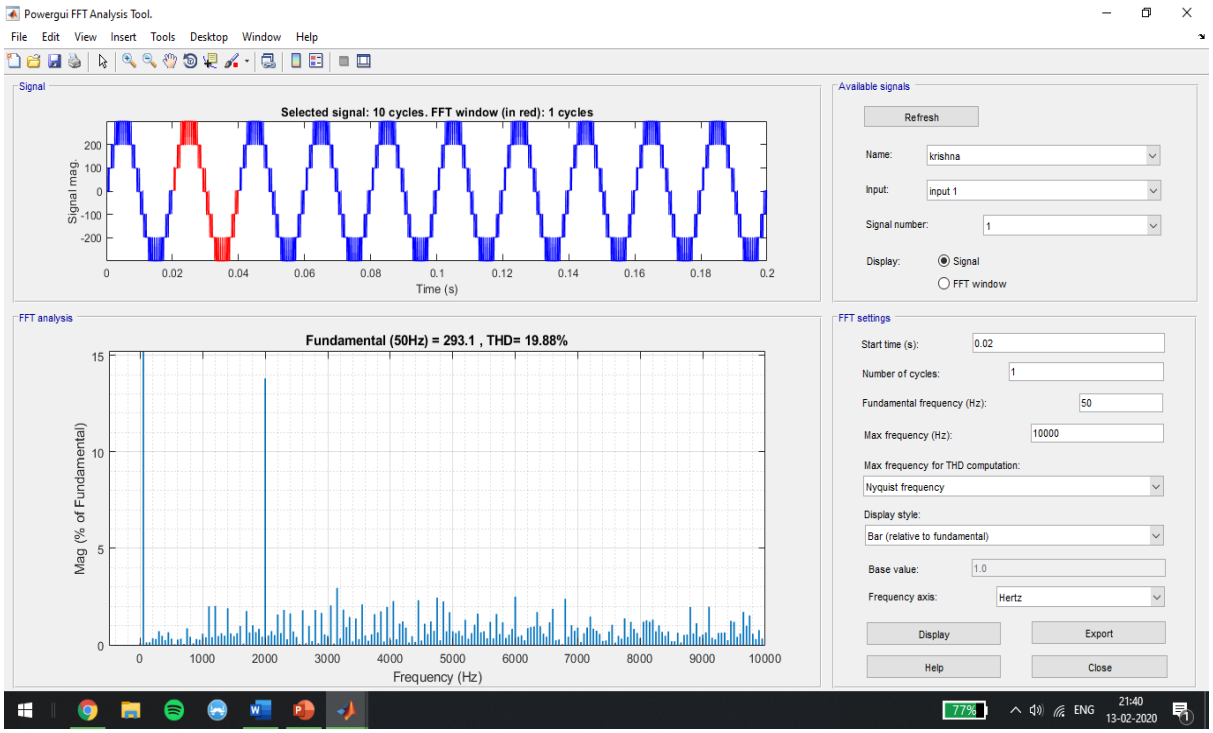


Fig (8.3): FFT analysis of Output Voltage

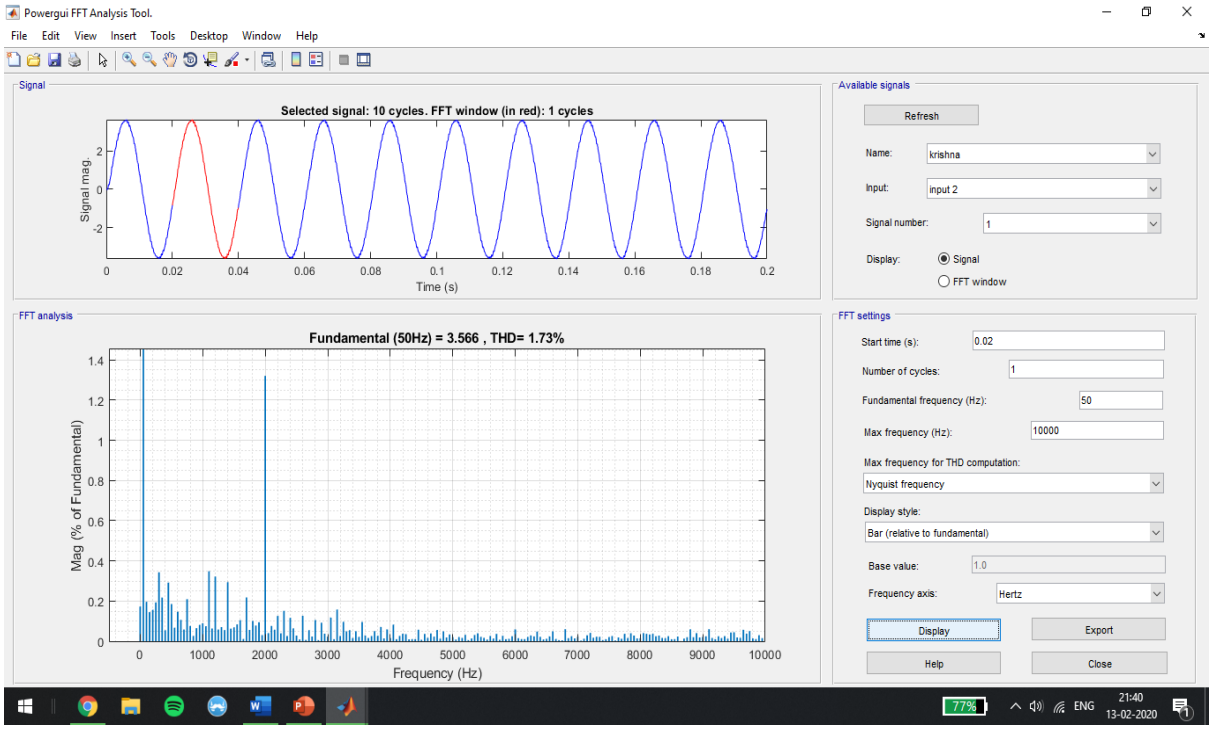


Fig (8.4): FFT analysis of Output Current**.**

8.5 Simulation Circuit under fault condition at a switch.

In order to conduct fault analysis, there was a fault made at switch S1 intentionally such that after 0.1s, the switch S1 is open circuited and fault occurs. At this time, the proposed seven level inverter acts as three level inverter and produces output with lower voltage levels.

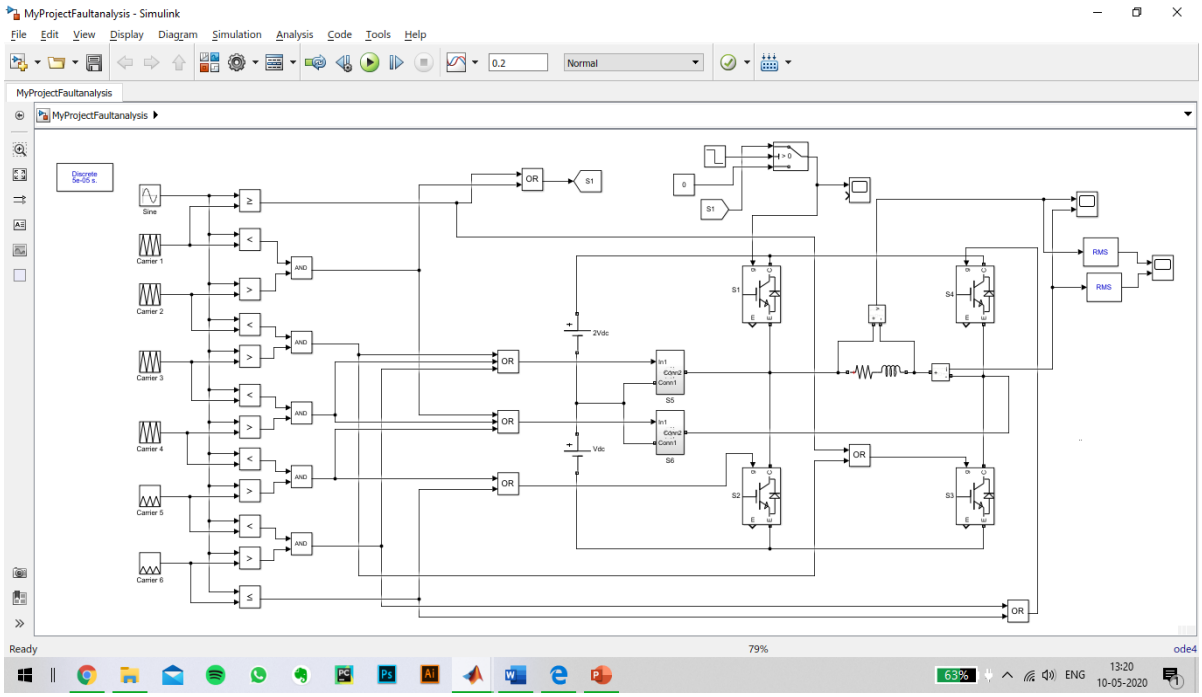
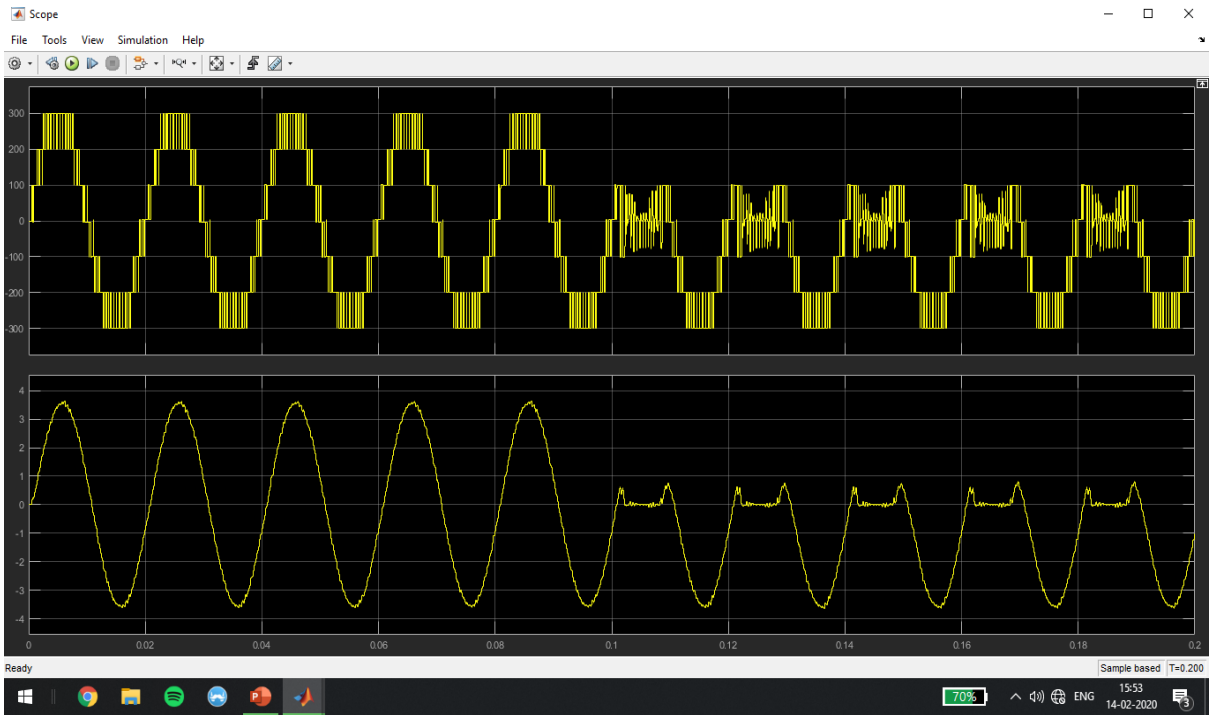


Fig (8.5): Circuit diagram under fault condition at switch S1



Fig(8.6): Output of the Inverter under fault condition.

CHAPTER-9

REFERENCES

1) Jih-Sheng Lai, Fang Zheng Peng, "Multilevel converters-a new breed of power converters," IEEE Transactions on Industry Applications, vol.32, no.3, pp.509-517, May/Jun 1996.

2) Alian Chen, Lei Hu, Lifeng Chen, Yan Deng, Xiangning He, "A multilevel converter topology with fault-tolerant ability," IEEE Transactions on Power Electronics, vol.20, no.2, pp.405-415, March 2005.

3) A.,M.R., Sivakumar, K., "A Fault Tolerant Single Phase Five-level Inverter for Grid Independent PV systems," IEEE Transactions on Industrial Electronics, vol.PP, no.99, pp.1,1 doi: 0.1109/TIE.2015.2455523.

4) Filho, F., Yue Cao, Tolbert, L.M., "11-Level cascaded H-bridge grid-tied inverter interface with solar panels," Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp.968-972, 2125 Feb. 2010.

5) Rodriguez, J., Jih-Sheng Lai, Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Transactions on Industrial Electronics, vol.49, no.4, pp.724-738, Aug 2002.

6) Jia-Min Shen, Hurng-Liahng Jou, Jinn-Chang Wu, Kuen-Der Wu, "FiveLevel Inverter for Renewable Power Generation System," IEEE Transactions on Energy Conversion, vol.28, no.2, pp.257,266, June 2013.

7) de Brito, M.A.G., Galotto, L., Sampaio, L.P., de Azevedo e Melo, G., and Canesin, C.A., "Evaluation of the Main MPPT Techniques for Photovoltaic Applications," IEEE Transactions on Industrial Electronics, vol.60, no.3, pp.1156-1167, March 2013.

8) P. Palanivel and S.S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," IET Power Electron., vol.4, no.8, pp.951-958, sept.2011.