CSE 4207 CT 4 Assignment Instructions

Last Date of Submission: 11 June 11:59 PM
Assignment Doc: Link
Assignment Template Doc: Link

Assignment is compulsory.
You must follow the same coding style and naming conventions used in code repo and video tutorials.
It is highly recommended to complete the entire assignment for those who are interested in the VLSI industry.

Marks Distribution (For details, check Assignment Template Doc: Link):

Category	Task	Marks
A	Combinational (ALU Op) Circuit using Verilog	14
B	Combinational (ALU Op) Circuit using Verilog + Synthesis	17
C	Combinational (ALU Op) + FSM Circuit using Verilog + Synthesis	20

A. **Combinational (ALU Op) Circuit using Verilog (14 Marks):** You have to write ALU modules (See Assignment Doc) in Verilog HDL with test bench.
   a. **Code Repo:** ALU.v, ALU_ADD_SUB_Nbit.v, ALU_SHL_Nbit.v, ALU_tb.v
   b. **Slides:** HDL 1 - Combinational Circuit (Link), HDL 2 - Sequential Circuit (Link), ALU 6 - Final 4-bit ALU Design (Link)

B. **Combinational (ALU Op) Circuit using Verilog + Synthesis (16 Marks):** You have to synthesize the design with Openlane tool and you have to show info described in the assignment template.
   a. **Environment Setup:** Use dual boot ubuntu (Highly recommended) /windows subsystem for linux (Not recommended/Not all features may work) to install OpenLane tools. Video: Link
   b. **Tutorials:** Video 1: Link, Video 2: Link, Video 3: Link, Repo: Link
   c. **Instructions:**
      - **Config.json:** 1. "DESIGN_NAME": "not_gate" where "not_gate" is the name of the top module of your design, 2. "VERILOG_FILES": ["dir::not.v"] here put names of all of your .v except test bench files like ["dir::not.v", "dir::not2.v"], "CLOCK_PORT": "clk" where clk is name of clock port, these two parameters need to be changed in case of error "DIE_AREA": "0 0 50 50" and "PLACE_DENSITY": 0.65. Use chatgpt to diagnose error messages.
      - **RTL Synthesis info:** All synthesis information can be found in the synthesis folders (both before and after synthesis) inside the runs directory. Check all the files (also those with .rpt extension) within

these folders to get RTL synthesis info. To view the synthesized design, locate the .dot file (typically named top_module_name.dot) and first go to that directory and use the following command: xdot top_module_name.dot here top_module_name is the name of your top module.

- **RTL Floor plan + RTL Power Analysis + GDS + Heatmap:** Follow Video Tutorials.

C. **Combinational (ALU Op) + FSM Circuit using Verilog + Synthesis (20 Marks):** You have to design a top-level circuit where an FSM (Finite State Machine) acts as the controller and sends data inputs to an ALU, which functions as the datapath. The FSM will have five states: `START` (initial state), `FINISH` (final state), `ONE`, `TWO`, and `THREE`. The states `ONE`, `TWO`, and `THREE` will send three different inputs (`a`, `b`, and `op`) to the datapath. The top-level circuit will produce two outputs received from the controller: the result from the ALU and a flag indicating whether the result is greater than 0. Make sure to include at least one test case where the flag value is 0.

   a. **Google Drive Link (Full Folder):** Link

   b. **Video Tutorials:** Video 1: Link, Video 2: Link

   c. **Repo:** Important Repo: Link, All Repo: Link

Upload Instructions:

1. **Google Classroom:**

   a. **VIDEO: Make sure to upload a video (You can use Zoom to create video) in Google Classroom** and make sure to include following:

Check List 1: Have you explained the design using testbenches to prove that your circuit is working correctly and giving correct results?	YES/NO
Check List 2: Have you shown full synthesis results showing all the required info including RTL Synthesis, RTL Floorplan, RTL Power Analysis, GDS and Heatmap (for details, see assignment template doc)?	YES/NO

   Rename the video using format: 19CT4Assignment_video_1903060.

   b. **DOC:** Submit only assignment doc in **PDF** using following format: **19CT4Assignment_doc_1903060.**

2. **Warning:**

   a. **Do not submit the `.exe` file. Google Drive may block the file and the zipped folder cannot be downloaded/examined by the examiner.**

b. **Do not zip files using winrar (.rar) or 7zip (.7z). Zip files using only the default windows zip file (.zip) feature (Instructions: Right Click on Folder -> Send to -> Compressed (zipped) folder).**

Academic Honesty Policy:

1. Do not cheat and be honest.
2. Do not share your answers.
3. *If it is found that someone cheated by copying someone's program file/snapshot, then the original author of the files (If identified) will get severe punishments.*
4. *Someone found guilty of cheating will have his/her CT Marks become 0.*
5. *If someone is aware of someone's/organized group's cheating, he/she is welcomed to send (anonymous) mail to the teacher. Teacher will keep the sender's identity secret and reward that sender heavily with extra CT marks.*