National University of Computer & Emerging Sciences, Karachi
Department of Computer Science
SPRING 2022

Course Code: EE-1005	**Course Name:** Digital Logic Design
Course Teacher: Aashir Mahboob	**Assignment No:** 03

Instructions for Submission:

1. *Use A4 size paper for solution of each Question.*
2. *You are required to Submit Assignment in hardcopy and also upload scanned copy on Google classroom.*
3. *The deadline for submission is 26th* ***May,2022.***
4. ***Copying is not allowed at all.*** *Any similarities among the submitted files of any student will result in* ***zero marks****.*

CLO #02 &03 (Total Marks -10)

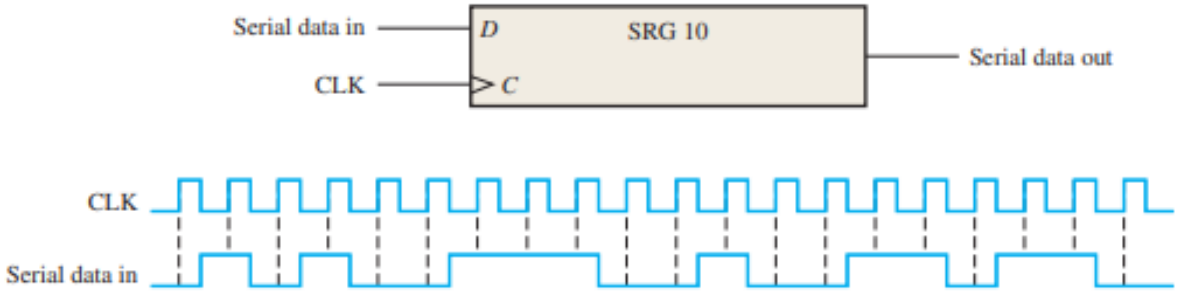
1. Design a counter to produce the following binary sequence. Use J-K flip-flops.

$$1, 4, 3, 5, 7, 6, 2, 1, \ldots$$

2. Design a counter to produce the following binary sequence. Use J-K flip-flops.

$$0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, \ldots$$

3. For the serial in/serial out shift register, determine the data-output waveform for the data-input and clock waveforms in Figure below. Assume that the register is initially cleared.



4. For the 8-bit bidirectional register in Figure below, determine the state of the register after each clock pulse for the RIGHT/LEFT control waveform given. A HIGH on this input enables a shift to the right, and a LOW enables a shift to the left. Assume that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the LSB. There is a LOW on the data-input line.