Homewrok 04 EE227 **Instructor: Behraj Khan**

Instructions:

- You are required to solve the homework on A4 Paper only.
- All the answers must be solved according to the sequence given in order.
- Submission deadline will be strictly followed.
- Your homework will be graded as zero in case of failing instructions.
- Submission deadline is Thursday (14:59:59, 11th June 2020).

Max Marks: 85 points

Question 1: (Combinational Logic Analysis) [20 Points]

(a) Implement the following Boolean function F using the two-level forms: **AND-NOR** and **OR-NAND**
F (A, B, C, D) = Σ(0,1,3,6,9,12) ; d (A, B, C, D) = Σ (2, 4, 5,11,13) [4]

(b) Design a combinational circuit with four inputs and one output. (i) The output is 1 when the binary value of the inputs is less than 8. The output is 0 otherwise. (ii) The output is 1 when the binary value of the inputs is an even number. [5]

(c) Apply DeMorgan's theorems to each expression: Also draw the circuit diagram [4]
(i) [A(B+C')'D]' **(ii)** [(M+N'){(M'+N)(M+N)}']'

(d) Convert the following Boolean expression into standard SOP form: BC'D + DE(B'C + DE) [2]

(e) Convert the following Boolean expression into standard POS form: (A+B+C')(B+D')(A'+B'+C+D) [2]

(f) Modify the circuit figure 1 for active HIGH. Writ down the statement for the input and output conditions. [3]

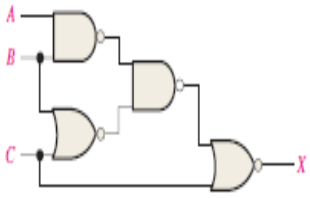
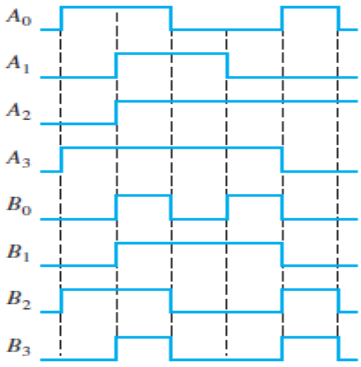


Fig-1



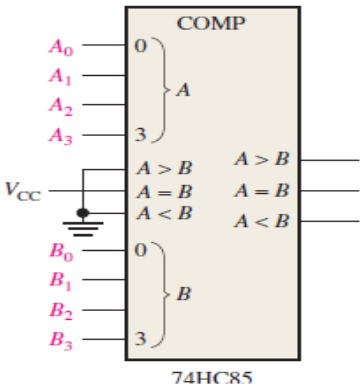


Fig-2

Question 2: (Functions of Combinational Logic) [18 Points]

(a) For the 4-bit comparator in Figure-2, plot each output waveform for the inputs shown. The outputs are active-HIGH. [3]

(b) Design a full-subtractor circuit incrementer. (A circuit that adds one to a four-bit binary number.) [4]

(c) Implement a full adder with (i) Two 4X1 multiplexers (ii) 3-8 line Decoder. [6]

(d) Implement the logic function in table by using a (74S151) 8 input data selector/multiplexer.
X(A3,A2, A1, A0) = ∑(0,1,3,5,6,10,11) [5]

Question 3: (Latches and Flip Flop) [8 Points]

(a) The following serial data are applied to the flip-flop through the OR gates as indicated in Figure. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first. [4]

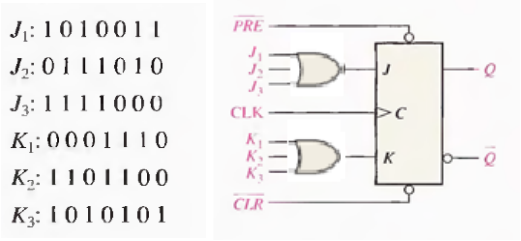


Fig-2

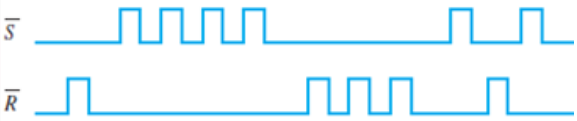


Fig-3

(b) Develop the Q output waves for the active low SR flip-flop with input wave forms shown in figure-3. [2]

(c) The Q output of an edge-triggered D flip flop is shown in fig-4. Determine the input waveform on the D input that is required to produce this output if the flip flop is a positive edge-triggered type. [2]

Question 4: (Counter) [23 Points]

(a) Show how to connect a 74HC93 4-bit asynchronous counter for each of the following moduli :(i) 13 (ii) 08 [4]

(b) For the circuit in Figure-5 develop a timing diagram for eight clock pulses, showing the QA and QB outputs in relation to the clock. [4]

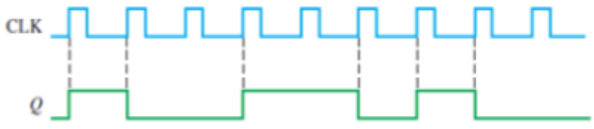


Fig-4

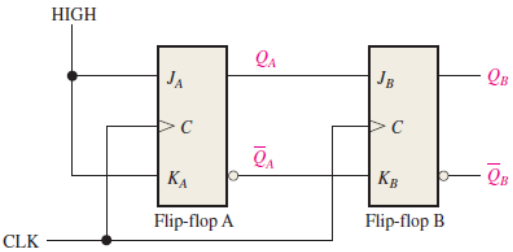


Fig-5

(c) Develop the Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in fig-6 A binary 0 is on the data inputs. Start with a count of 0000. [4]

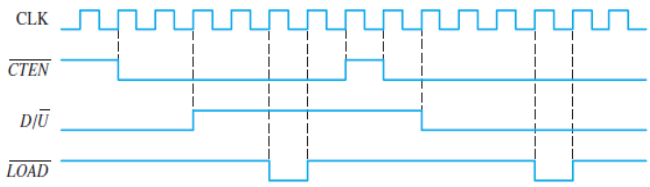


Fig -6

(d) Determine the sequence of the counter in fig-7. Begin with the counter cleared. [3]

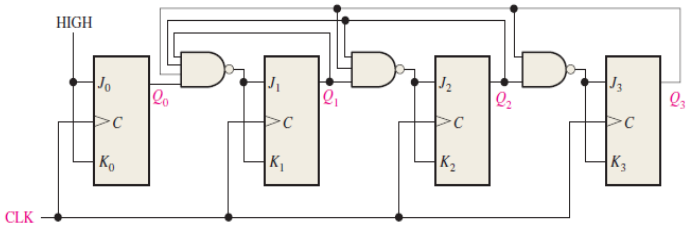


Fig -7

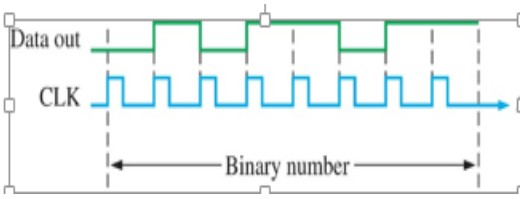


Fig-8

(e) Design a counter to produce the following binary sequence. (Use J-K flip-flops) 0, 9, 1, 8, 2, 7, 3, 6, 4, 5 [8]

Question 5: (Shift Register) [16 Points]

(a) If a 5-bit ring counter has an initial state 11001, determine the waveform for each *Q* output. [4]

(b) Design a modulus-8 Johnson counter using J K flip flop. Write the sequence in tabular form. [4]

(c) The sequence 10101 is applied to the input of a 5-bit serial shift register that is initially cleared. What are the states of the shift register from 1 to 10 clock pulses? [4]

(d) A leading-edge clocked serial in/parallel out shift register has a data-output waveform as shown in fig- 8. What binary number is stored in the 8-bit register if the first data bit out (leftmost) is the LSB? [4]