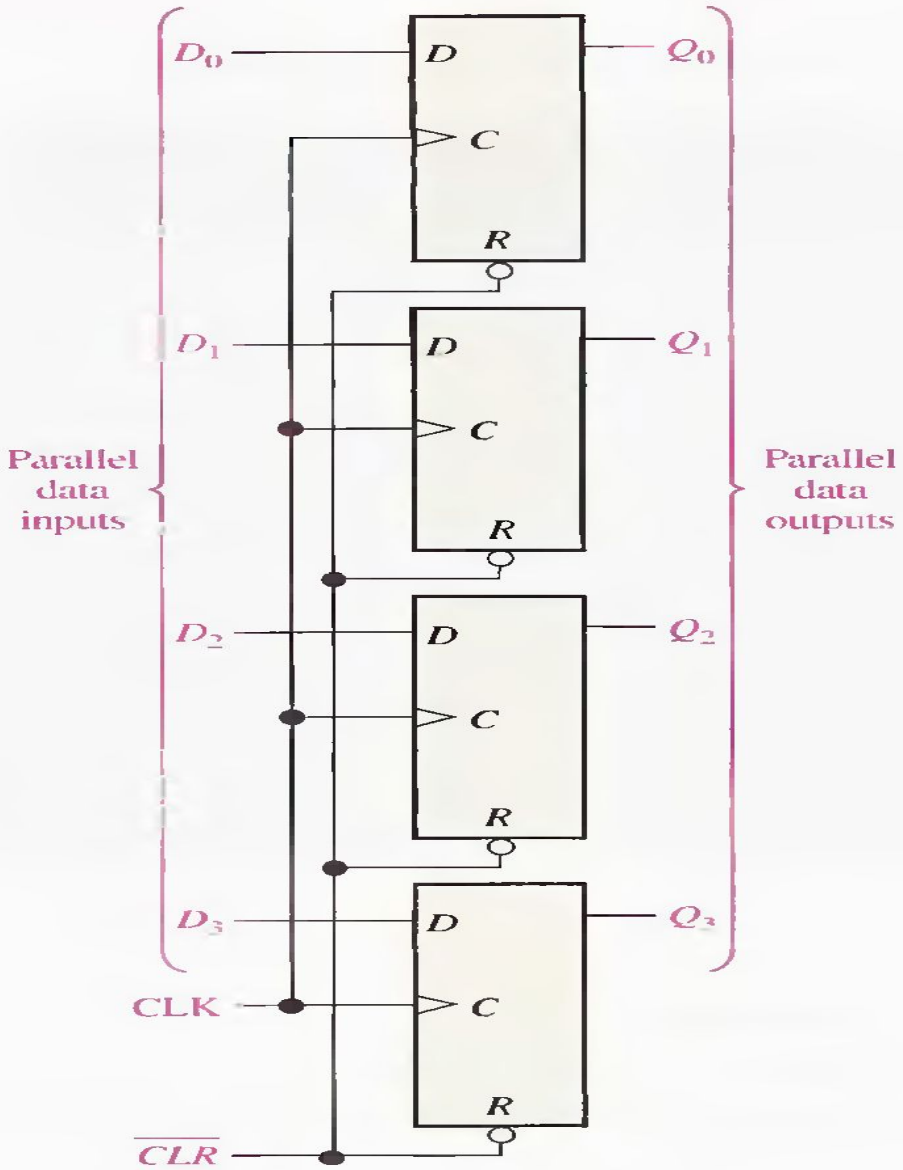
Digital Logic Design EE(1005)

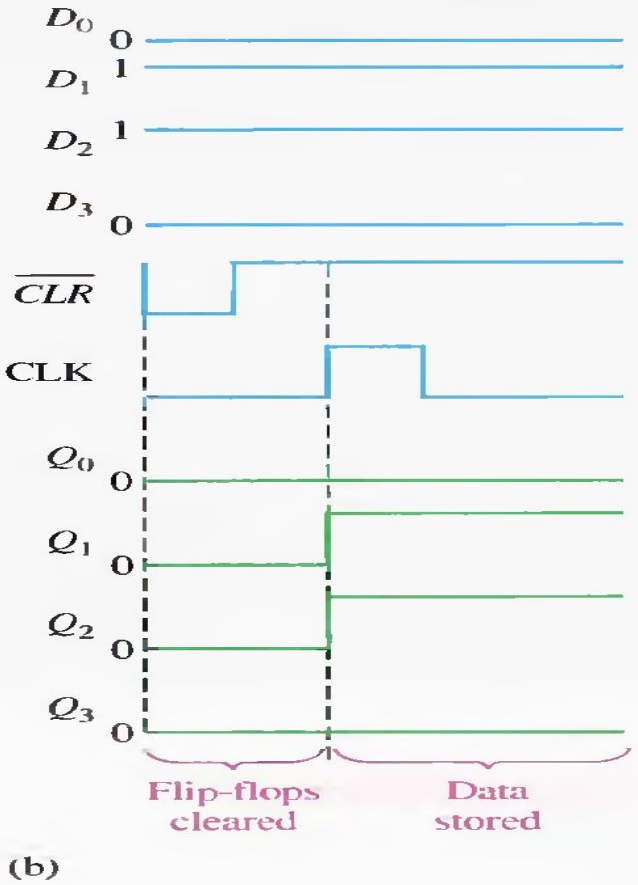
Lecture- 30

Chapter No:7
Latches and Flip Flop

FLIP-FLOP APPLICATIONS

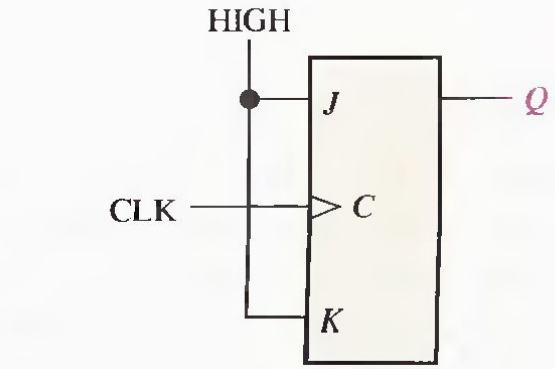
Parallel Data Storage

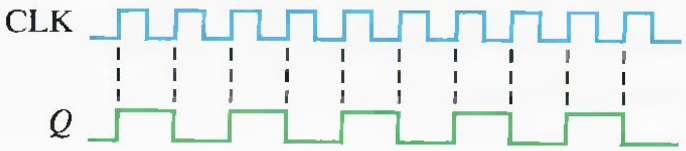




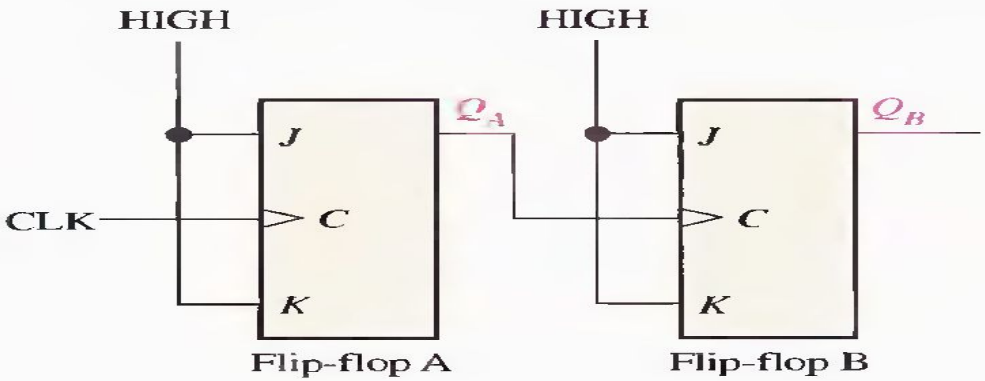
Frequency Division

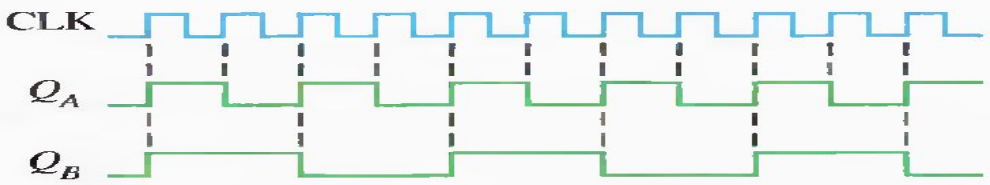
The J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.



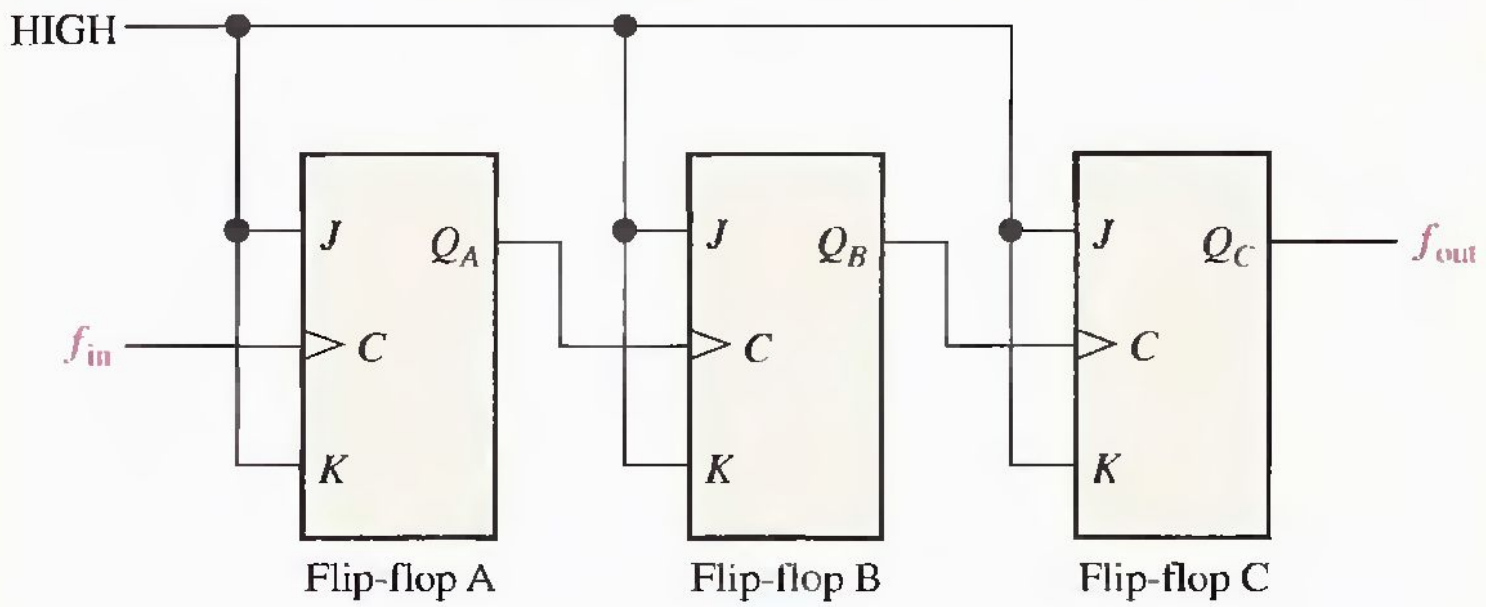


Example of two J-K flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK.

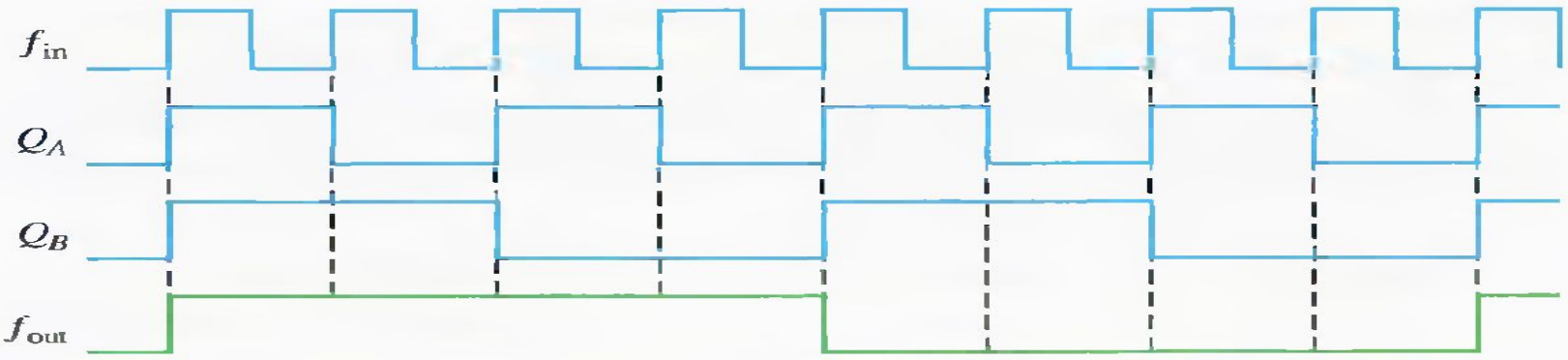




Develop the f_{out} waveform for the circuit in Figure when an 8 kHz square wave input is applied to the clock input of flip-flop A.

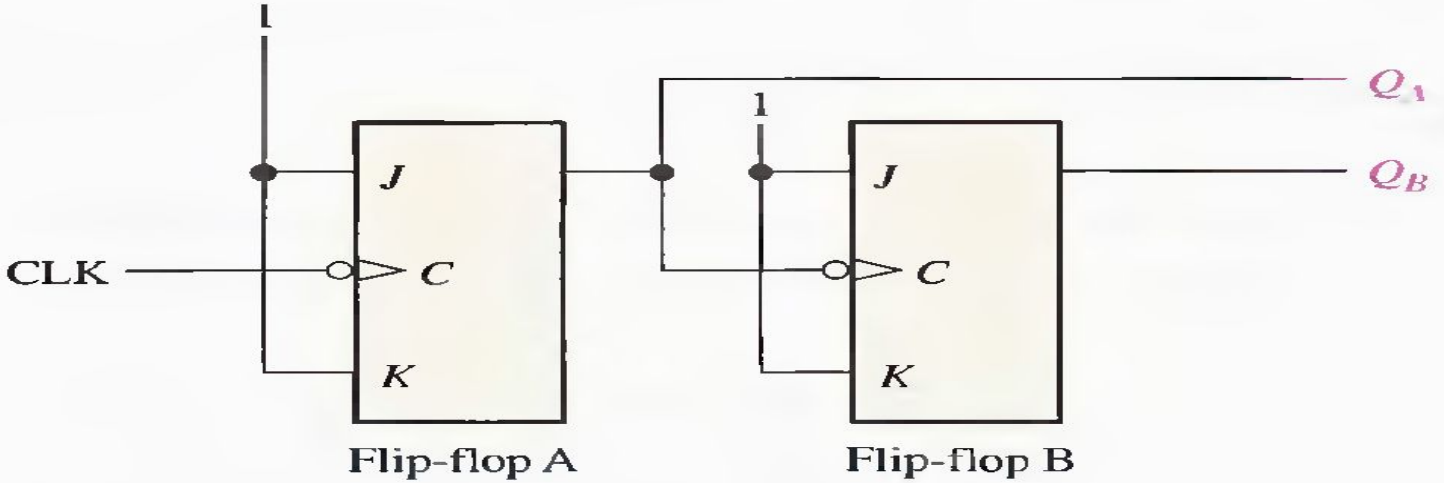


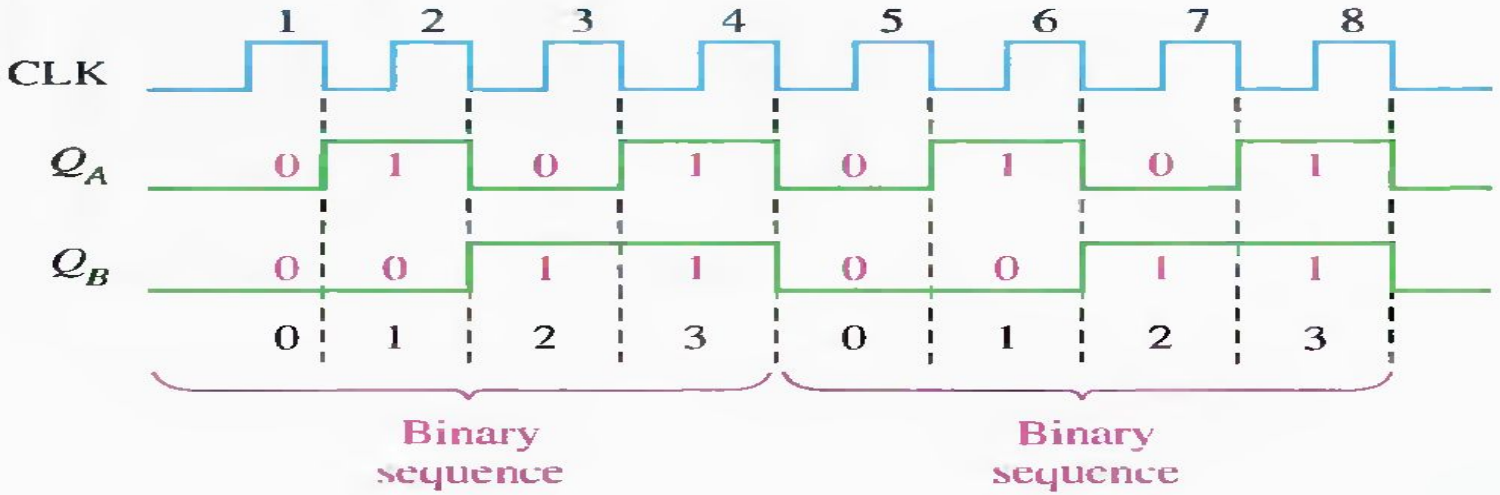
The three flip-flops are connected to divide the input frequency by eight ($2^3 = 8$)



Counting

Flip-flops used to generate a binary count sequence. Two repetitions (00, 01, 10, 11) are shown.





Determine the output waveforms in relation to the clock for Q_A, Q_B, and Q_C.