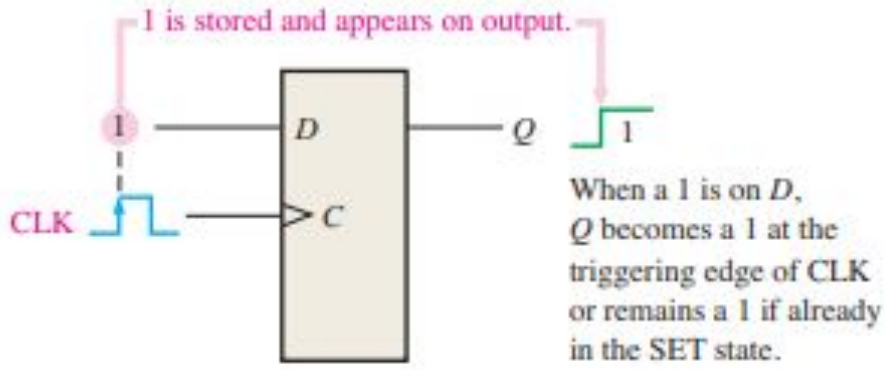
Chapter No:8
Shift Registers

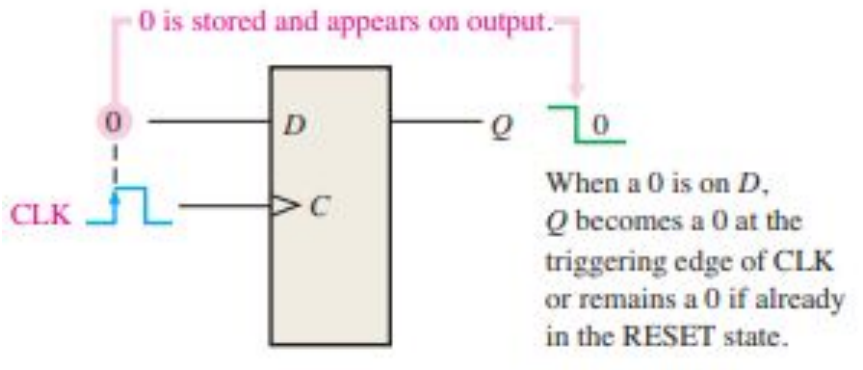
TOPICS

1. Basic Shift Register Operations.
2. Serial In/Serial Out Shift Registers.
3. Serial In/Parallel Out Shift Registers.
4. Parallel In/Parallel Out Shift Registers.
5. Bidirectional Shift Registers.

A register is a digital circuit with two basic functions: data storage and data movement. The storage capability of a register makes it an important type of memory device.

Figure 8-1 illustrates the concept of storing a 1 or a 0 in a D flip-flop. A 1 is applied to the data input as shown, and a clock pulse is applied that stores the 1 by setting the flip-flop. When the 1 on the input is removed, the flip-flop remains in the SET state, thereby storing the 1. A similar procedure applies to the storage of a 0 by resetting the flip-flop, as also illustrated in Figure 8-1





Shift Register

Shift registers consist of arrangements of flip-flops and are important in applications involving the storage and transfer of data in a digital system. A register has no specified sequence of states, except in certain very specialized applications. A register, in general, is used solely for storing and shifting data (1s and 0s) entered into it from an external source and typically possesses no characteristic internal sequence of states

Storage capacity of a register

The storage capacity of a register is the total number of bits (1s and 0s) of digital data it can retain. Each stage (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity.

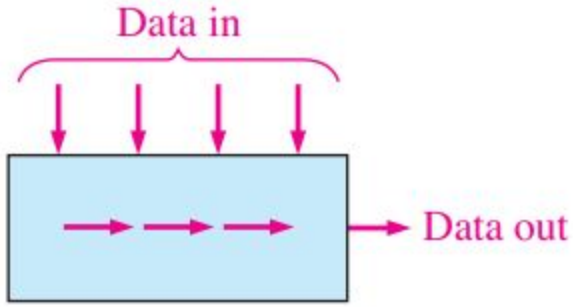
Types of data movement in shift registers.

The shift capability of a register permits the movement of data from stage to stage within the register or into or out of the register upon application of clock pulses.

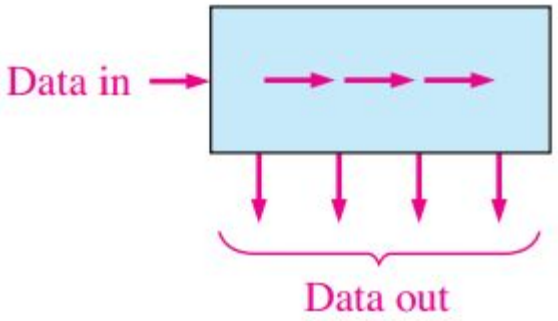
(a) Serial in/shift right/serial out

(b) Serial in/shift left/serial out

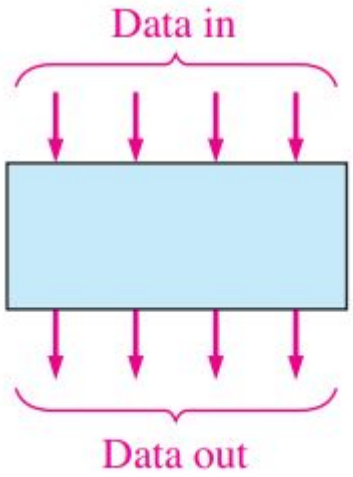
Types of data movement in shift registers.



(c) Parallel in/serial out



(d) Serial in/parallel out



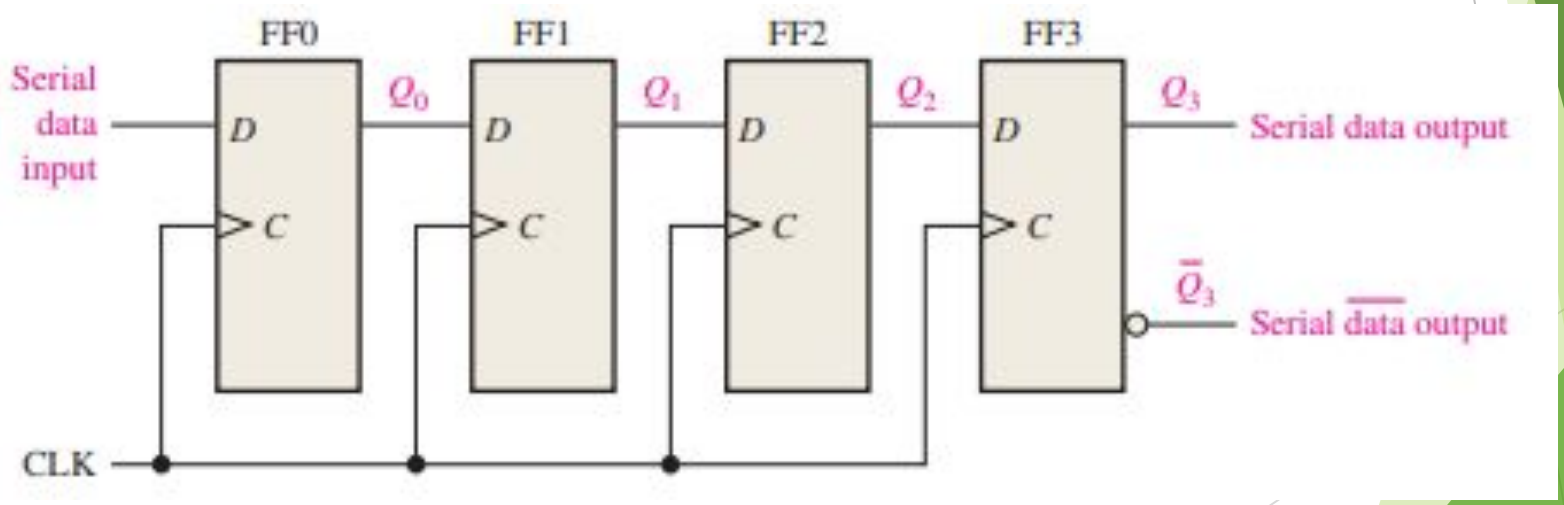
(e) Parallel in/parallel out

(f) Rotate right

(g) Rotate left

Serial In/Serial Out Shift Registers

The serial in/serial out shift register accepts data serially—that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. Let's first look at the serial entry of data into a typical shift register. Figure 8–3 shows a 4-bit device implemented with D flip-flops. With four stages, this register can store up to four bits of data



DATA = The four bits 1010 into the register
The register is initially clear.

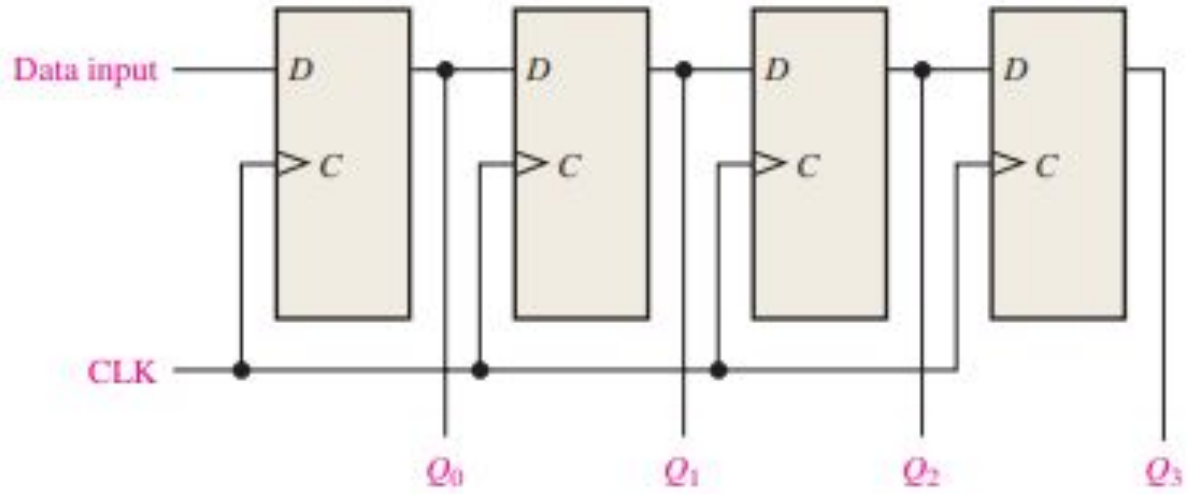
CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

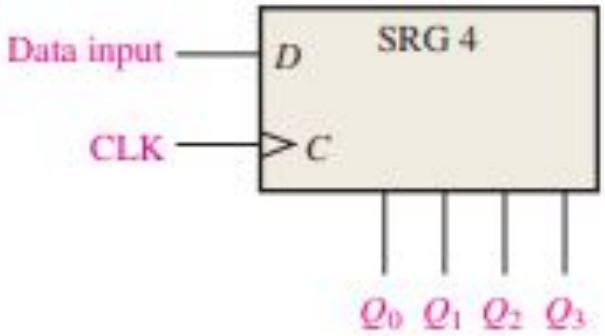
This completes the serial entry of the four bits into the shift register, where they can be stored for any length of time as long as the flip-flops have dc power.

Serial In/Parallel Out Shift Registers

Data bits are entered serially (least-significant bit first) into a serial in/parallel out shift register in the same manner as in serial in/serial out registers. The difference is the way in which the data bits are taken out of the register; in the parallel output register, the output of each stage is available. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output.

Serial In/Parallel Out Shift Registers

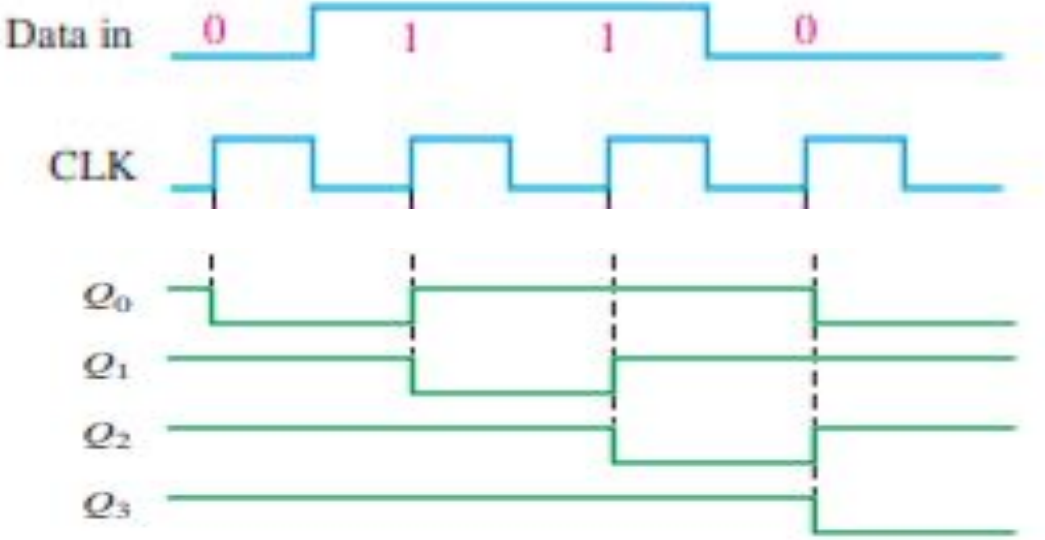


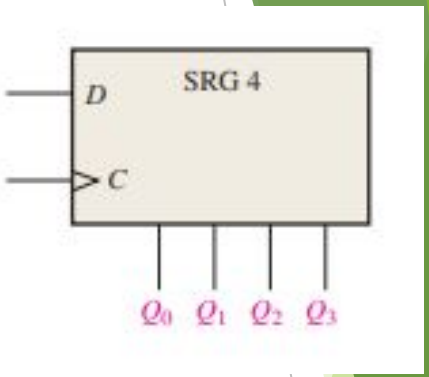


Once the data are stored, each bit appears on its respective output line

EXAMPLE

Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms below. The register initially contains all 1s.





EXERCISE

Show the states (Draw waveforms) of the 4-bit register (SRG 4) for the data input 1010. The register initially contains all 0s.

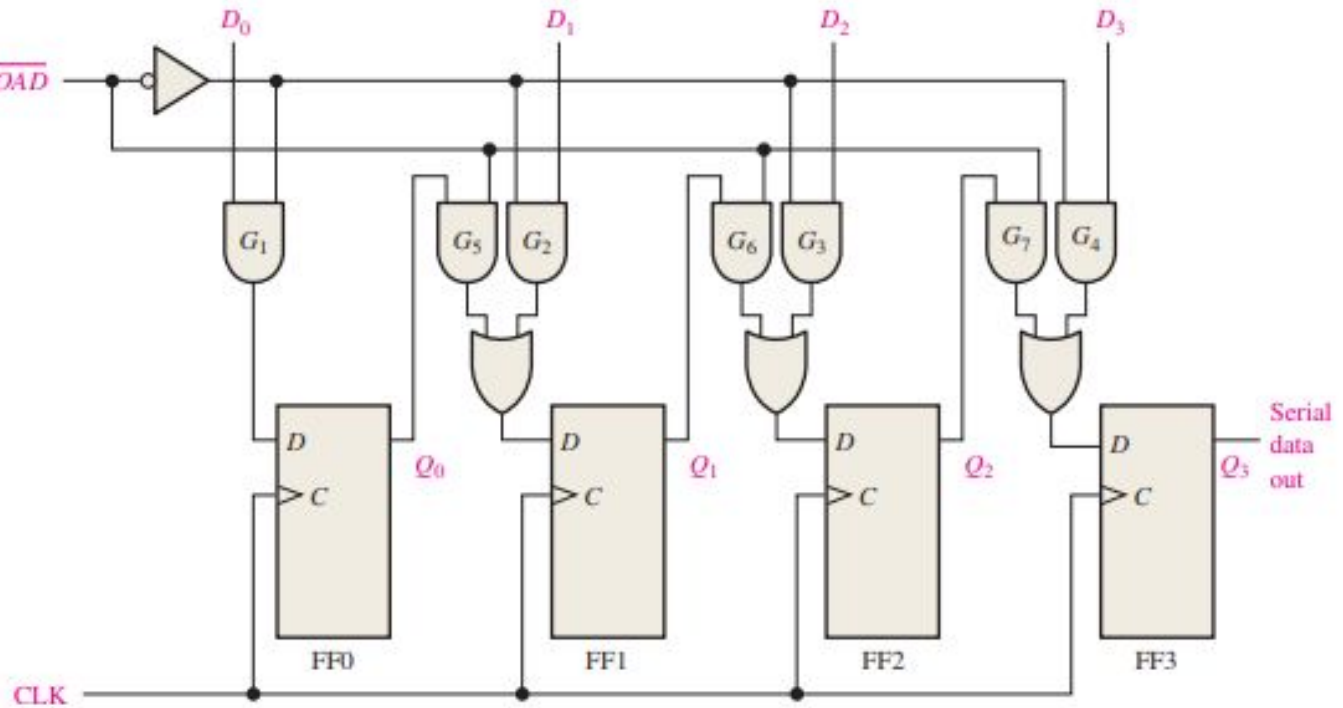
EXERCISE

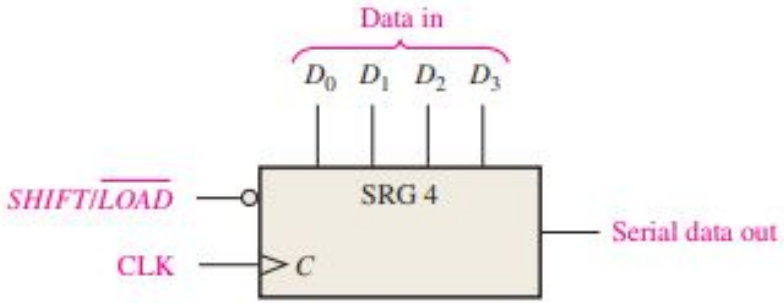
The sequence 1011 is applied to the input of a 4-bit serial shift register that is initially cleared. What is the state of the shift register after three clock pulses?

Parallel In/Serial Out Shift Registers

For a register with parallel data inputs, the bits are entered simultaneously into their respective stages on parallel lines rather than on a bit-by-bit basis on one line as with serial data inputs. The serial output is the same as in serial in/serial out shift registers, once the data are completely stored in the register.

Parallel In/Serial Out Shift Registers





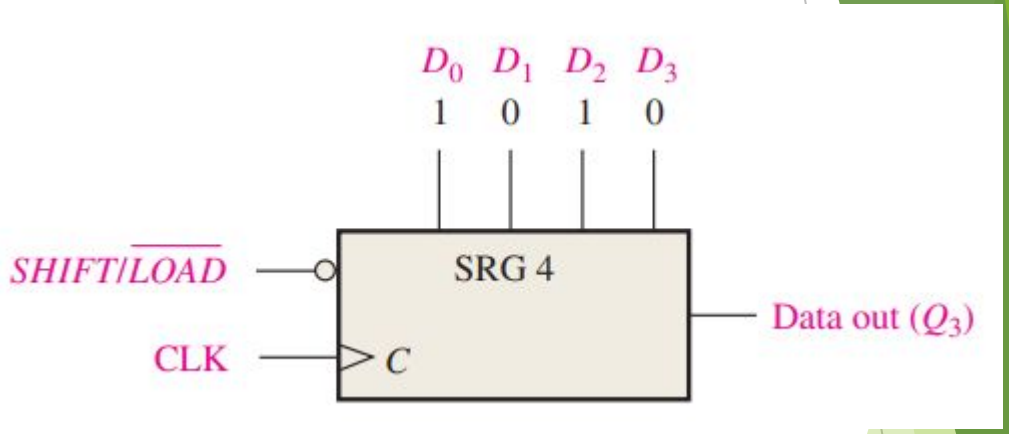
Parallel In/Serial Out Shift Registers

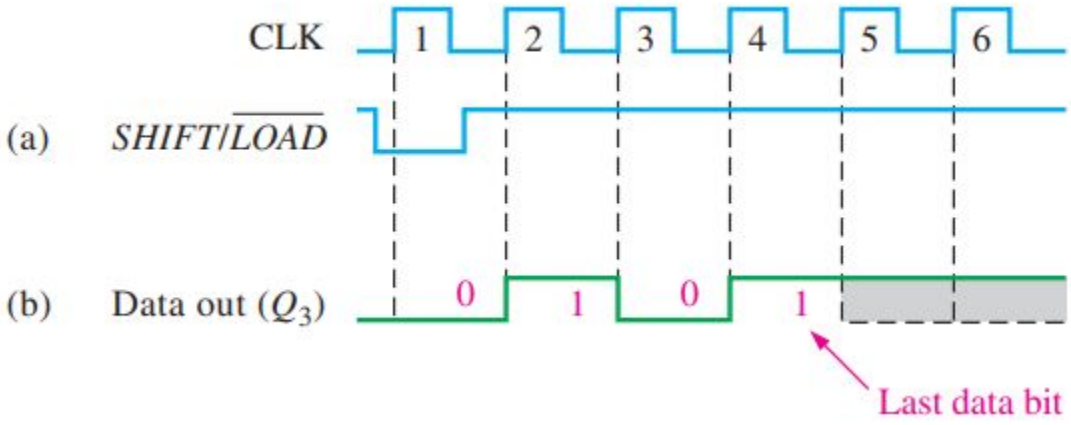
There are four data-input lines, D0, D1, D2, and D3, and a SHIFT/LOAD input, which allows four bits of data to load in parallel into the register. When SHIFT/LOAD is LOW, gates G1 through G4 are enabled, allowing each data bit to be applied to the D input of its respective flip-flop. When a clock pulse is applied, the flip-flops with D = 1 will set and those with D = 0 will reset, thereby storing all four bits simultaneously.

When SHIFT/LOAD is HIGH, gates G1 through G4 are disabled and gates G5 through G7 are enabled, allowing the data bits to shift right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which AND gates are enabled by the level on the SHIFT/LOAD input. Notice that FF0 has a single AND to disable the parallel input, D0. It does not require an AND/OR arrangement because there is no serial data in.

EXAMPLE

Show the data-output waveform for a 4-bit register with the parallel input data and the clock and SHIFT/LOAD waveforms given in Figure 8–11(a). Refer to Figure 8–10(a) for the logic diagram



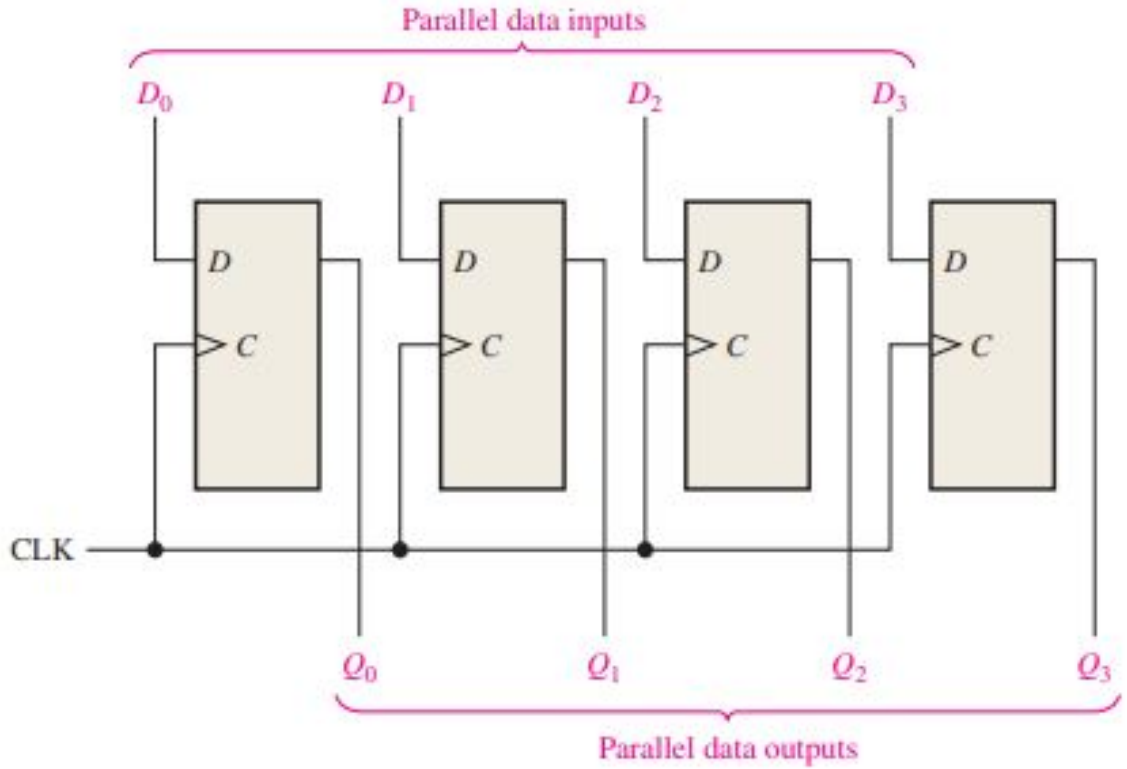


Related Problem

Show the data-output waveform for the clock and SHIFT/LOAD inputs shown in Figure 8–11(a) if the parallel data are = 0101.

Parallel In/Parallel Out Shift Registers

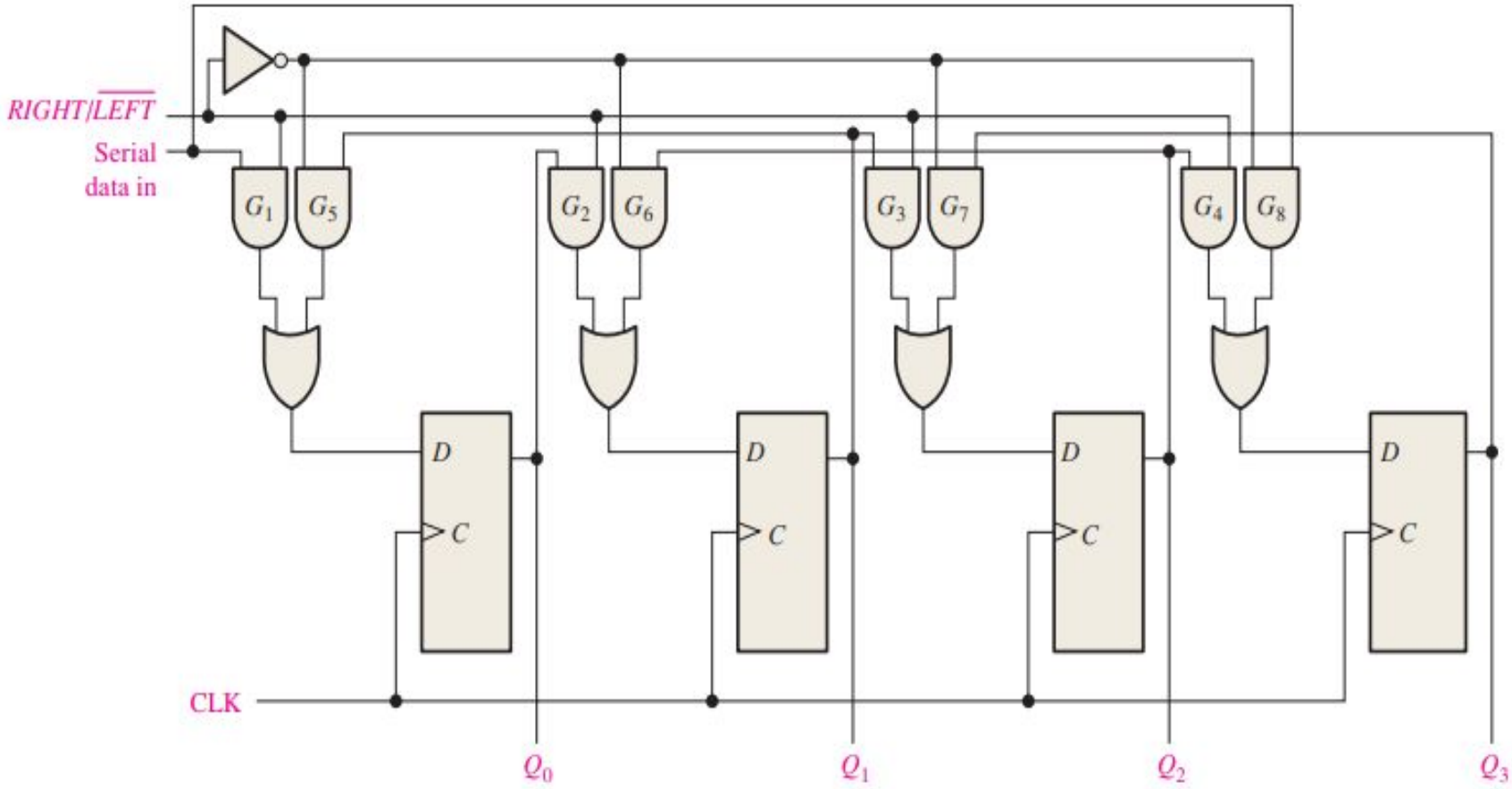
Parallel entry and parallel output of data have been discussed. The parallel in/parallel out register employs both methods. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs. Figure 8–14 shows a parallel in/parallel out shift register.



Bidirectional Shift Registers

A bidirectional shift register is one in which the data can be shifted either left or right. It can be implemented by using gating logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left, depending on the level of a control line.

Bidirectional Shift Registers

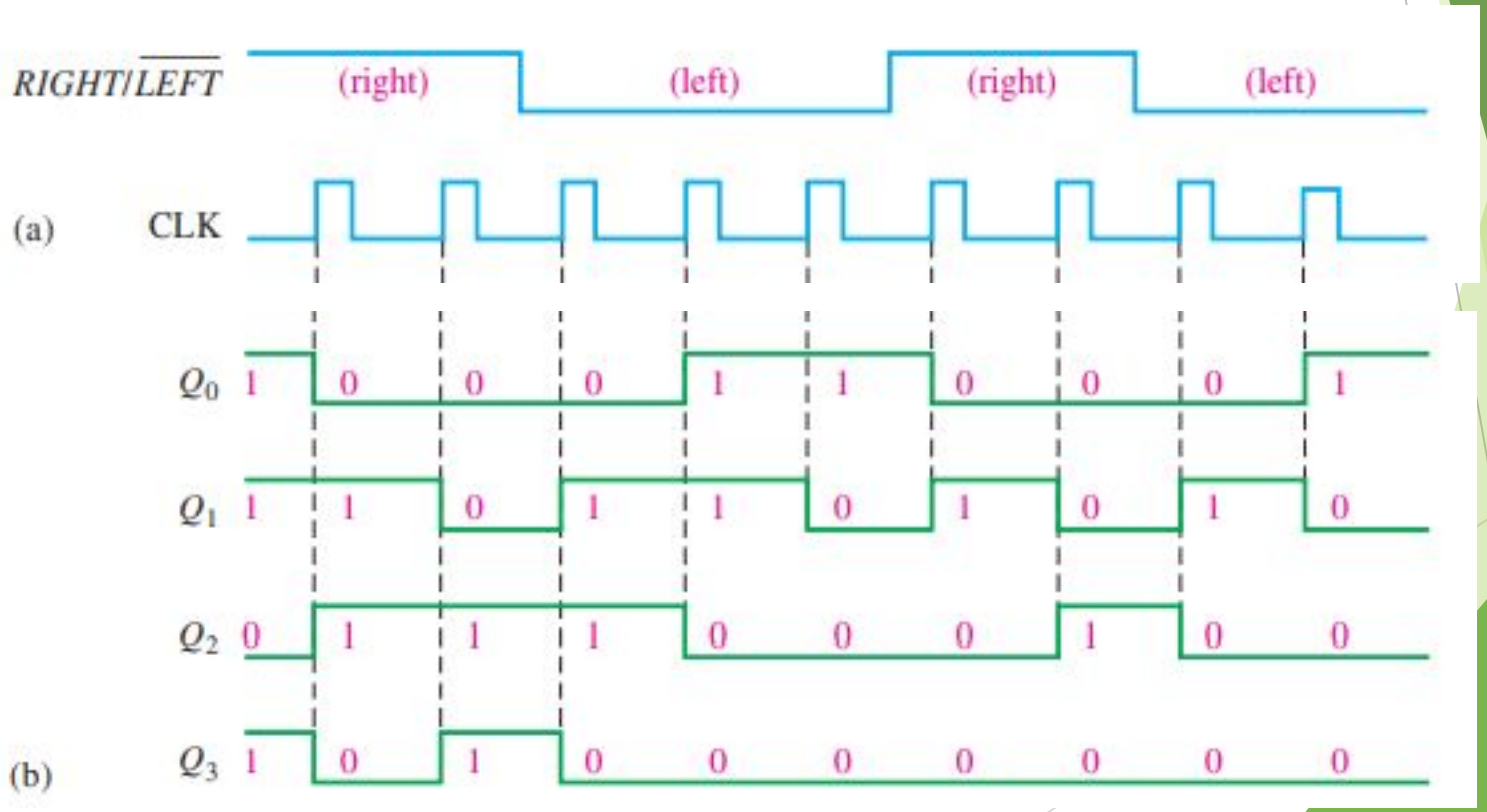


Bidirectional Shift Registers

- A HIGH on the RIGHT/**LEFT** control input allows data bits inside the register to be shifted to the right.
- A LOW enables data bits inside the register to be shifted to the left.
- When the RIGHT/**LEFT** control input is HIGH, gates G1 through G4 are enabled, and the state of the Q output of each flip-flop is passed through to the D input of the following flip-flop. When a clock pulse occurs, the data bits are shifted one place to the right.
- When the RIGHT/**LEFT** control input is LOW, gates G5 through G8 are enabled, and the Q output of each flip-flop is passed through to the D input of the preceding flip-flop. When a clock pulse occurs, the data bits are then shifted one place to the left.

EXAMPLE

Determine the state of the shift register after each clock pulse for the given RIGHT/**LEFT** control input waveform in Figure below. Assume that Q0 = 1, Q1 = 1, Q2 = 0, and Q3 = 1 and that *the serial data-input line is LOW.*



EXERCISE

Invert the RIGHT/LEFT waveform, and determine the state of the shift register in previous example after each clock pulse.