Digital Logic Design EE(1005)

Lecture- 25

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Chapter No:7
Latches and Flip Flop

*Flip-Flops_*

. The fundamentals of sequential logic , Bistable, Monostable, and Astable logic devices called multivibrators . A multivibrator circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output.

Astable - A *free-running multivibrator* that has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.

Monostable - A *one-shot multivibrator* that has only **ONE** stable state and is triggered externally with it returning back to its first stable state.

Bistable - A *flip-flop* that has **TWO** stable states that produces a single pulse either positive or negative in value.

Two categories of bistable devices are the latch and the flip-flop. The flip-flop is a basic building block for counters, registers, and other sequential control logic and is used in certain types of memories

LATCHES

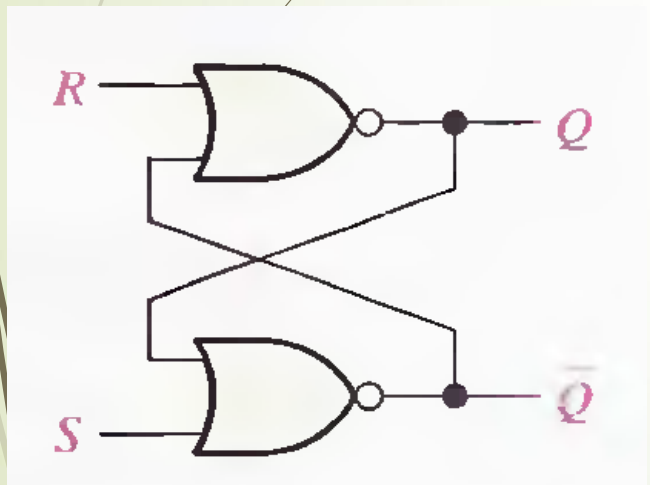
The **latch** is a type of temporary storage device that has two stable states (bistable) and is normally placed in a category separate from that of flip-flops. Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs. The main difference between latches and flip-flops is in the method used for changing their state.

FLIP-FLOPS

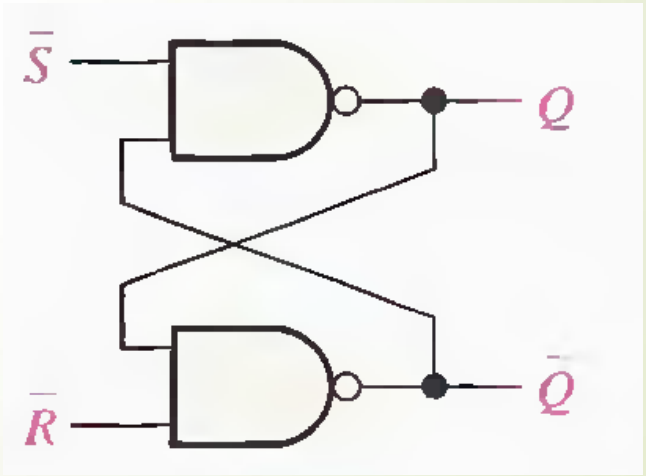
Flip-flops are synchronous bistable devices, also known as *bistable multivibrators*. In this case, the term *synchronous* means that the output changes state only at a specified point on the triggering input called the **clock** (CLK), which is designated as a control input, *C;* that is, changes in the output occur in synchronization with the clock.

The S-R (SET-RESET) Latch

A latch is a type of bistable logic device or multivibrator. An active-HIGH input S-R (SET- RESET) latch is formed with two cross-coupled NOR gates, an active-LOW input S-R latch is formed with two cross-coupled NAND gates, .That the output of each gate is connected to an input of the opposite gate .This produces the regenerative feedback that is characteristic of all latches and flip-flops.

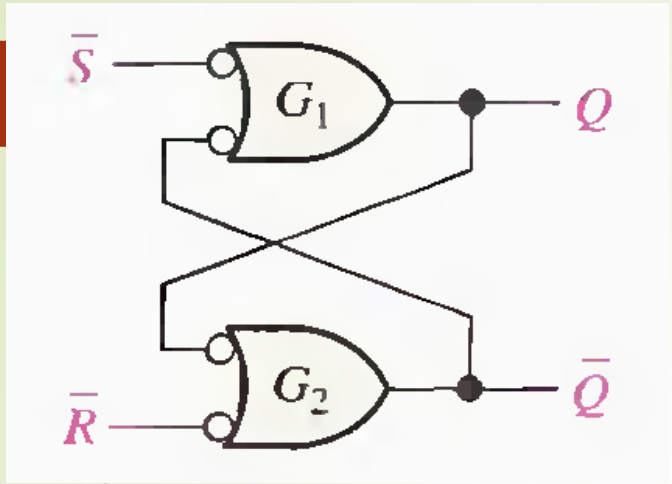


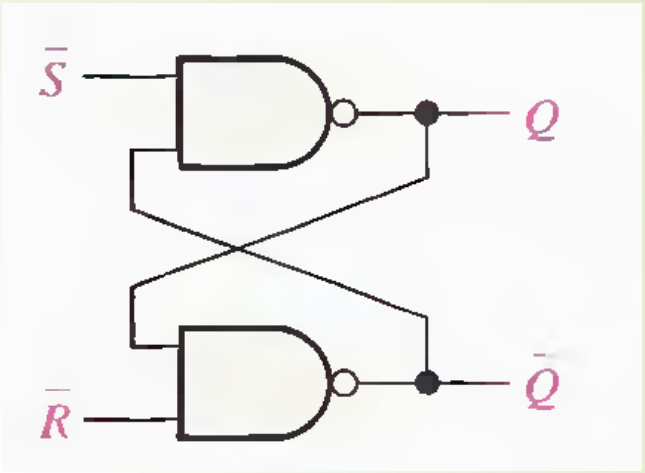
Active-HIGH input S-R latch



Active-LOW input $\bar{S}$-$\bar{R}$ latch

Negative-OR equivalent of the NAND gate S-R latch





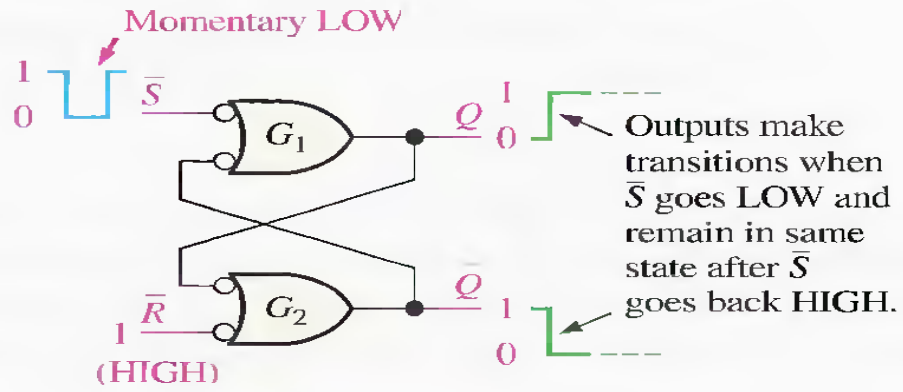
When Q is HIGH, $\overline{Q}$ is LOW, and when Q is LOW, $\overline{Q}$ is HIGH.

Let's start by assuming that both inputs and the Q output are HIGH. Since the Q output is connected back to an input of gate G2, and the R' input is HIGH, the output of G 2 must be LOW. This LOW output is coupled back to an input of gate G1 to ensuring that its output is HIGH. When the Q output is HIGH, the latch is in the SET state. It will remain in this state in-definitely until LOW is temporarily applied to the R' input.

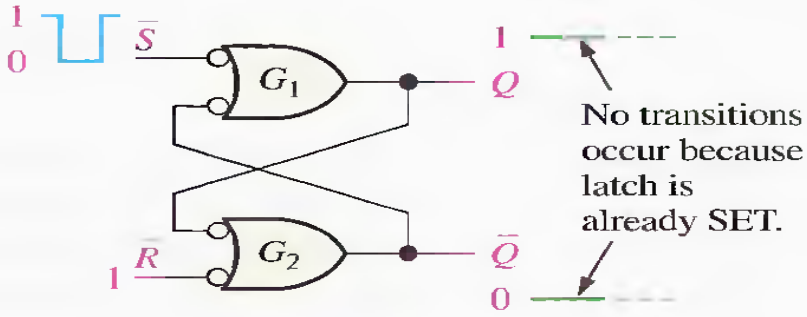
With a LOW on the R' input and a HIGH on S', the output of gate G 2 is forced HIGH. This HIGH on the Q' output is coupled back to an input of G 1 , and since the S' input is HIGH, the output of G 1 goes LOW. This LOW on the Q output is then coupled back to an input of G 2 , ensuring that the Q' output remains HIGH even when the LOW on the R' input is removed. When the Q output is LOW, the latch is in the RESET state. Now the latch remains indefinitely in the RESET state until a LOW is applied to the S' input.

A latch can reside in either of its two states, SET or RESET.

SET means that the Q output is HIGH.

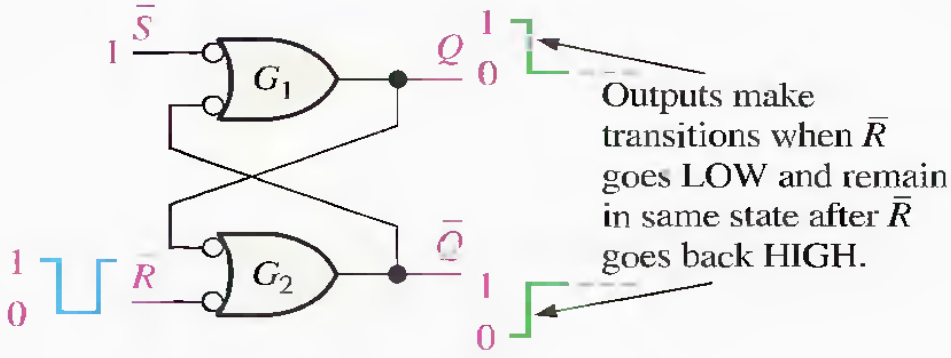


Latch starts out RESET ($Q = 0$).

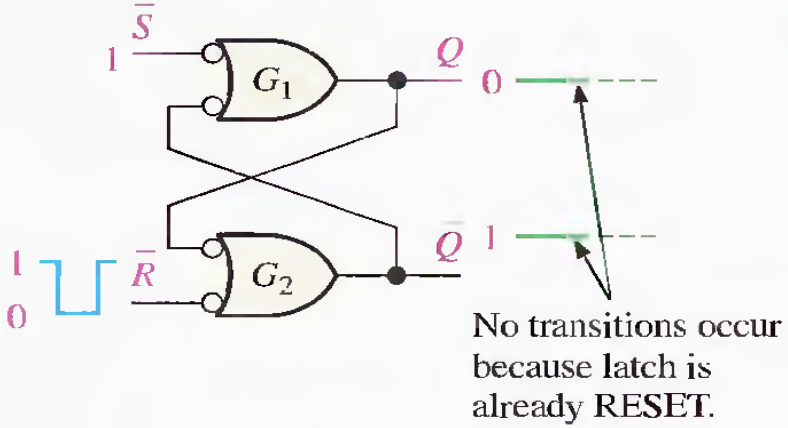


Latch starts out SET ($Q = 1$).

RESET means that the Q output is LOW.

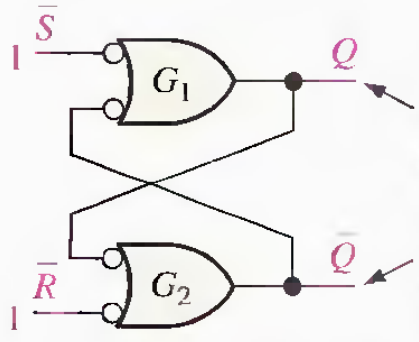


Latch starts out SET ($Q = 1$).



Latch starts out RESET ($Q = 0$).

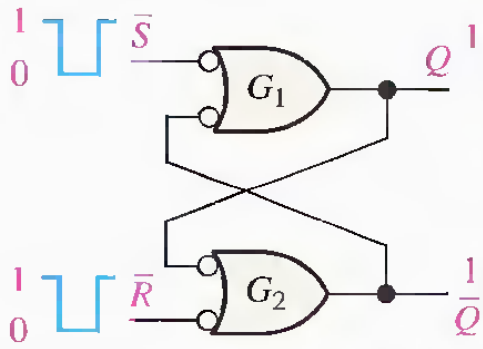
No-change condition



Outputs do not change state. Latch remains SET if previously SET and remains RESET if previously RESET.

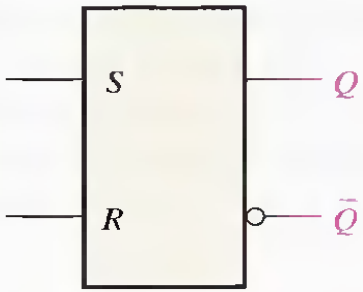
HIGHS on both inputs

Invalid condition

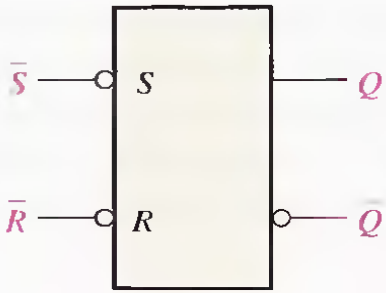


Output states are uncertain when input LOWs go back HIGH.

Simultaneous LOWs on both inputs

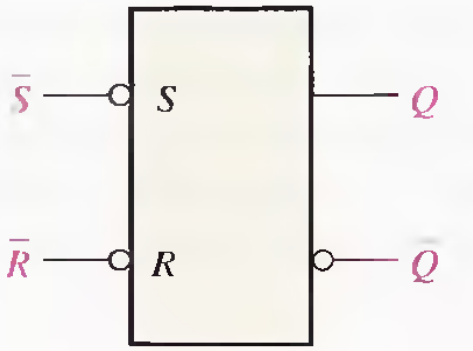


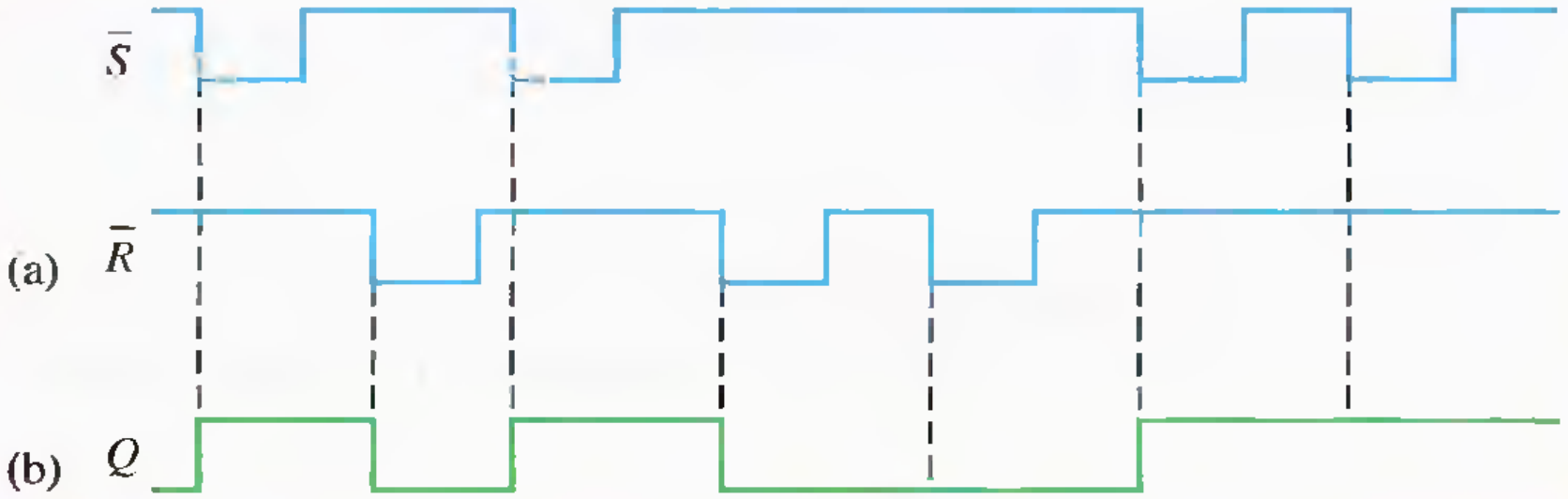
(a) Active-HIGH input S-R latch



INPUTS		OUTPUTS		COMMENTS
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

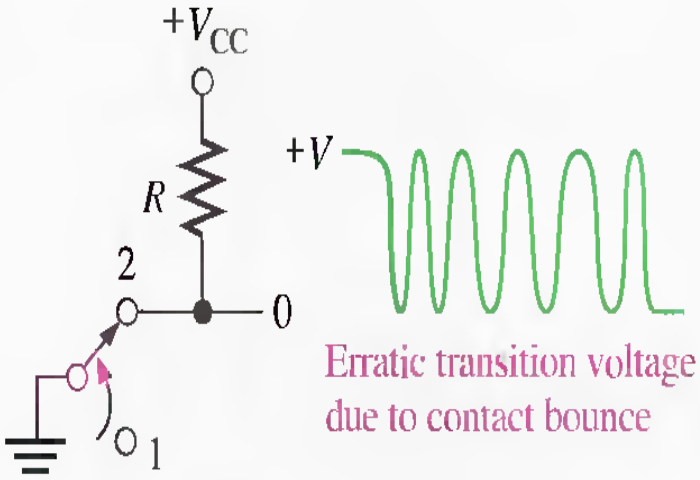
If the $\overline{S}$ and $\overline{R}$ waveforms in Figure are applied to the inputs of the latch in Figure determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.



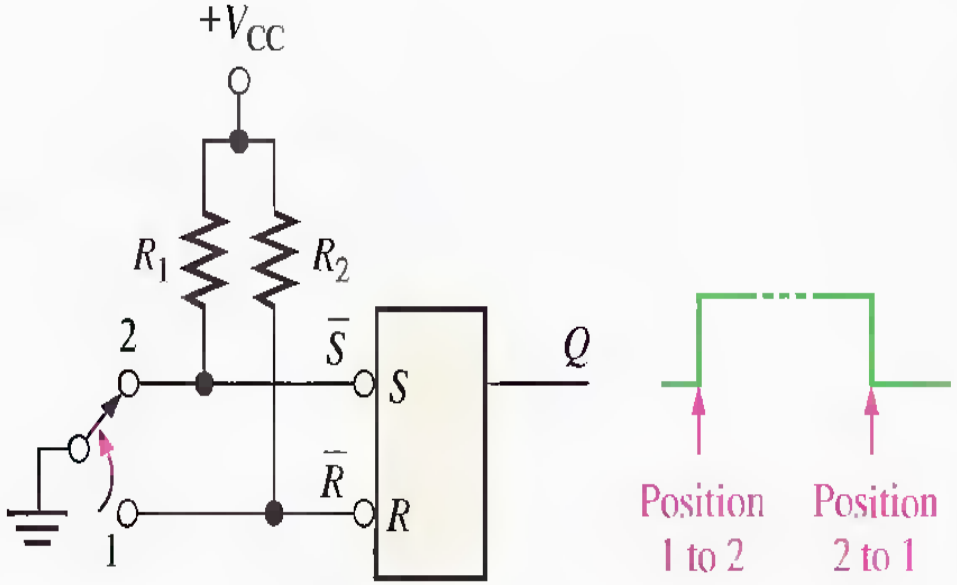


An Application

The Latch as a Contact-Bounce Eliminator



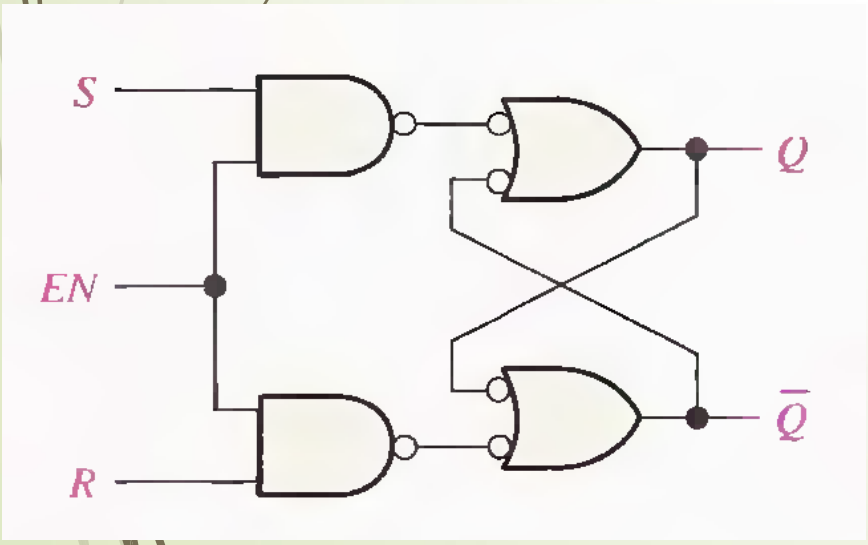
(a) Switch contact bounce

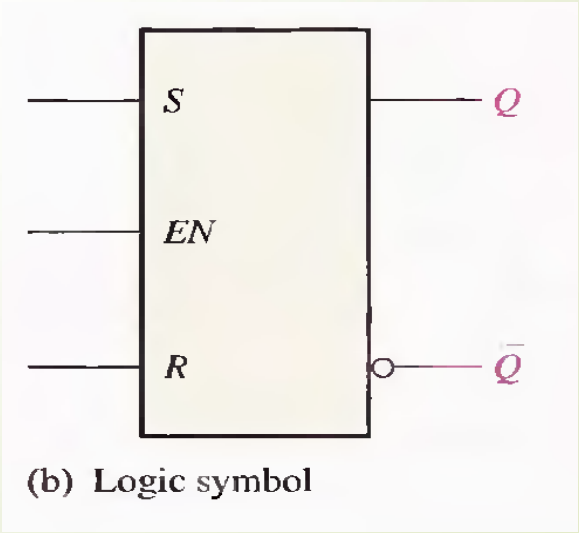


(b) Contact-bounce eliminator circuit

The Gated S-R Latch

A gated latch requires an enable input. EN (G is also used to designate an enable input). The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs. In this circuit, the invalid state occurs when both Sand R are simultaneously HIGH.

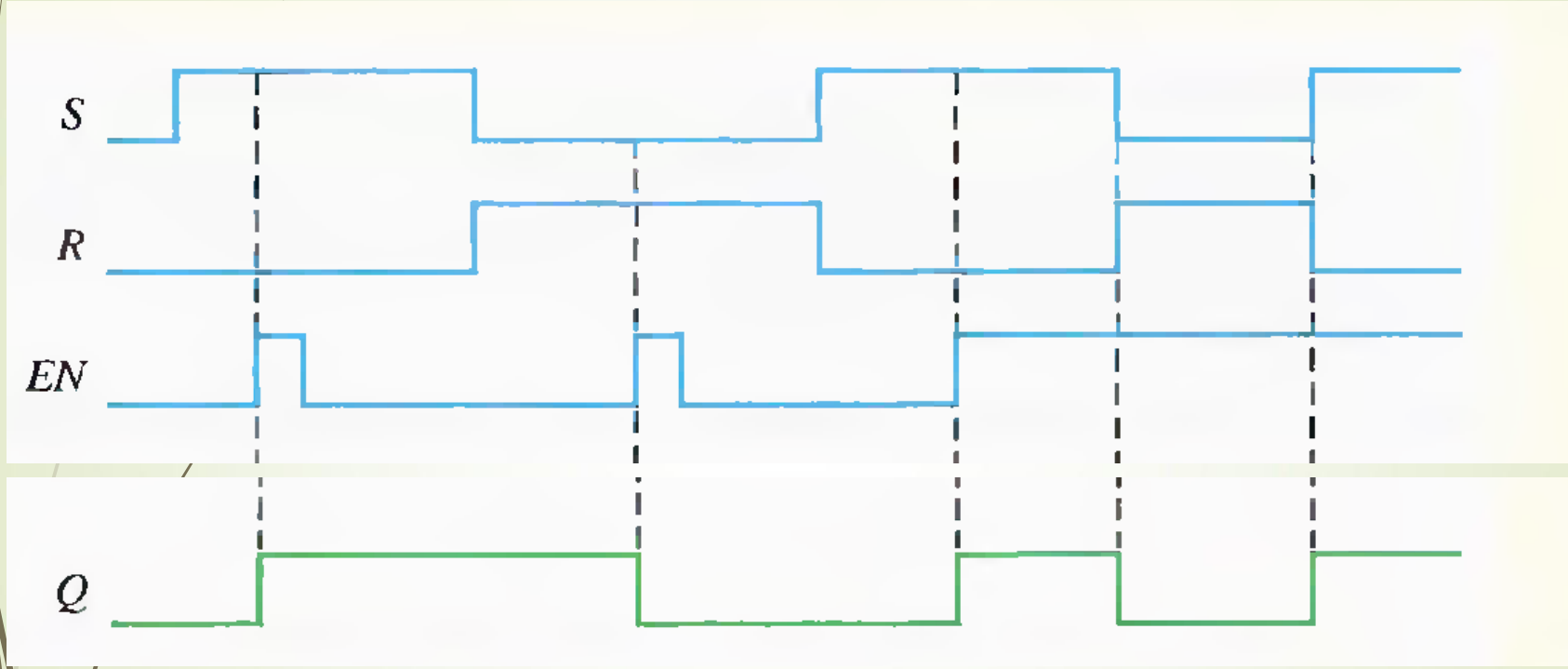




(b) Logic symbol

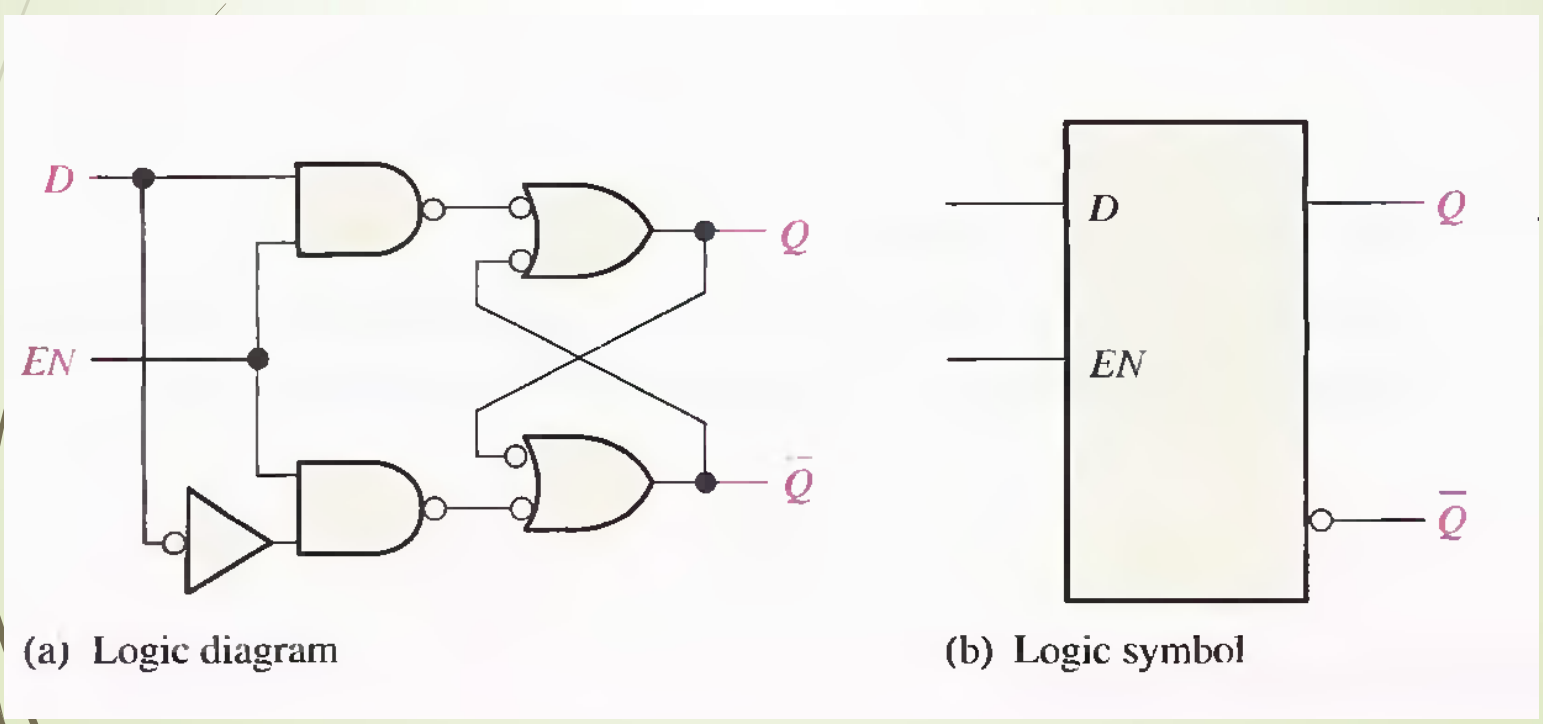
a gated S-R latch that is initially RESET.

Determine the Q output waveform



The Gated D Latch

Gated D latch is differs from the S-R latch because it has only one input in addition to EN. This input is called the D (data) input. When the D input is HIGH and the EN input is HIGH, the latch will set. When the D input is LOW and EN is HIGH, the latch will reset. Stated another way, the output Q follows the input D when EN is HIGH.



(a) Logic diagram (b) Logic symbol

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.