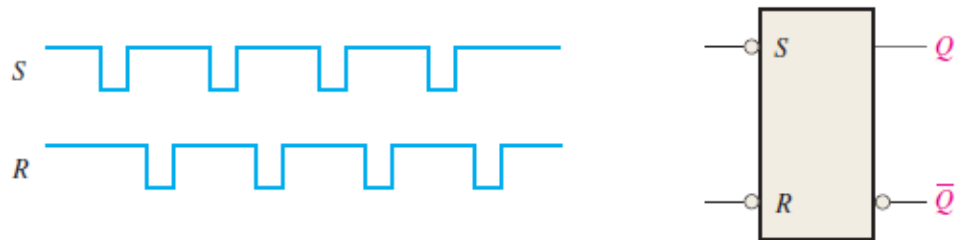


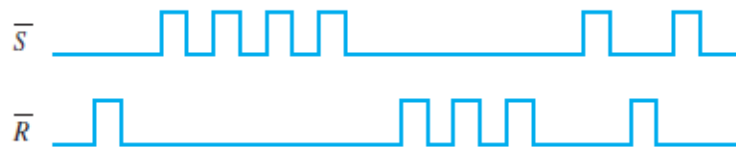
## Assignment-4

1. If the waveforms in Figure 7-70 are applied to an active-HIGH S-R latch, draw the resulting  $Q$  output waveform in relation to the inputs. Assume that  $Q$  starts LOW.



**FIGURE 7-70**

2. Solve Problem 1 for the input waveforms in Figure 7-71 applied to an active-LOW  $\bar{S}$  -  $\bar{R}$  latch.



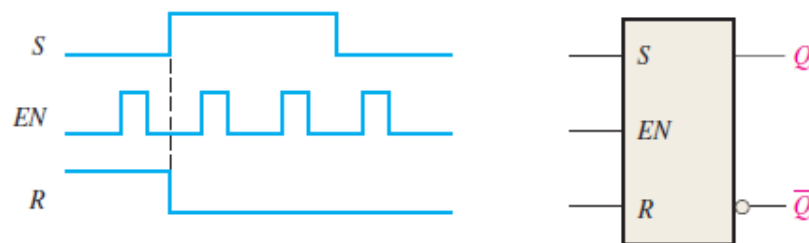
**FIGURE 7-71**

3. Solve Problem 1 for the input waveform in Figure 7-72.



**FIGURE 7-72**

4. For a gated S-R latch, determine the  $Q$  and  $\bar{Q}$  outputs for the inputs in Figure 7-73. Show them in proper relation to the enable input. Assume that  $Q$  starts LOW.



**FIGURE 7-73**

5. Determine the output of a gated D latch for the inputs in Figure 7-74.



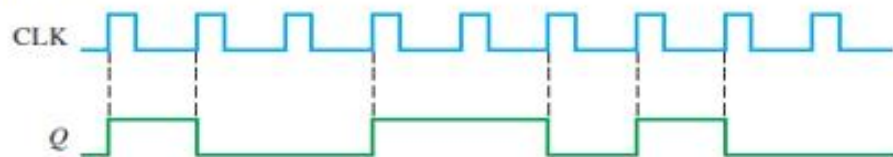
**FIGURE 7-74**

6. Determine the output of a gated D latch for the inputs in Figure 7-75.



**FIGURE 7-75**

9. The  $Q$  output of an edge-triggered D flip-flop is shown in relation to the clock signal in Figure 7-78. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.



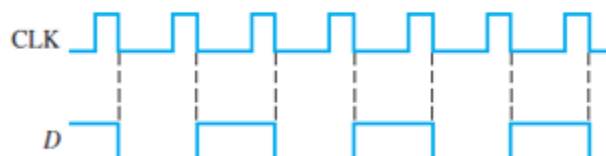
**FIGURE 7-78**

10. Draw the  $Q$  output relative to the clock for a D flip-flop with the inputs as shown in Figure 7-79. Assume positive edge-triggering and  $Q$  initially LOW.



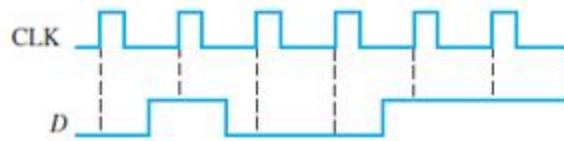
**FIGURE 7-79**

11. Solve Problem 10 for the inputs in Figure 7-80.



**FIGURE 7-80**

12. For a positive edge-triggered D flip-flop with the input as shown in Figure 7–81, determine the  $Q$  output relative to the clock. Assume that  $Q$  starts LOW.



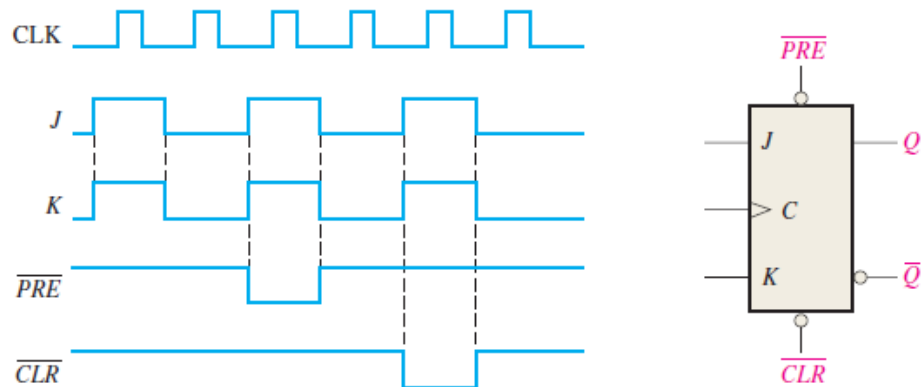
**FIGURE 7–81**

13. Solve Problem 12 for the input in Figure 7–82.



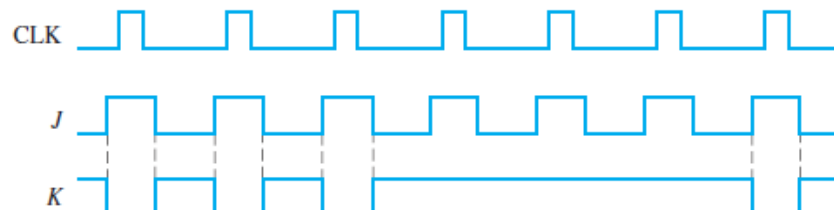
**FIGURE 7–82**

14. Determine the  $Q$  waveform relative to the clock if the signals shown in Figure 7–83 are applied to the inputs of the J-K flip-flop. Assume that  $Q$  is initially LOW.



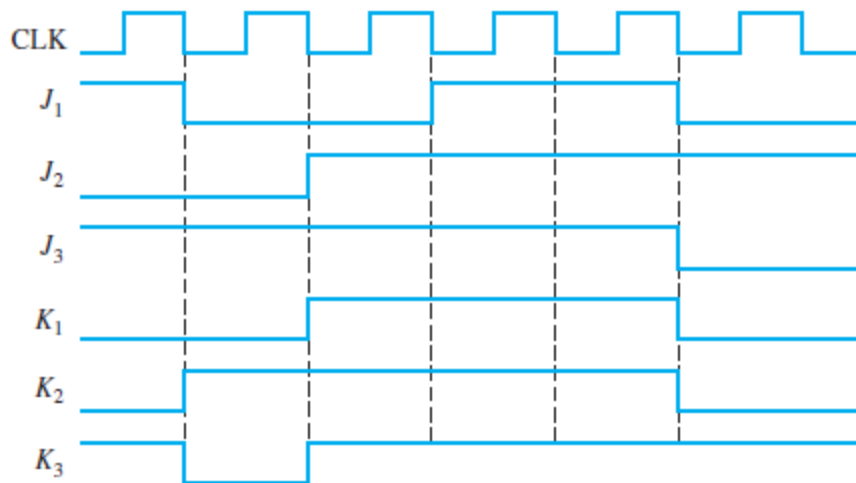
**FIGURE 7–83**

15. For a negative edge-triggered J-K flip-flop with the inputs in Figure 7–84, develop the  $Q$  output waveform relative to the clock. Assume that  $Q$  is initially LOW.



**FIGURE 7–84**

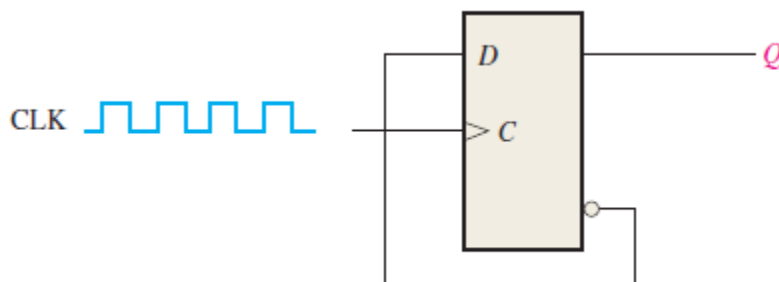
16. For the circuit in Figure -1, complete the timing diagram in Figure 2 by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.



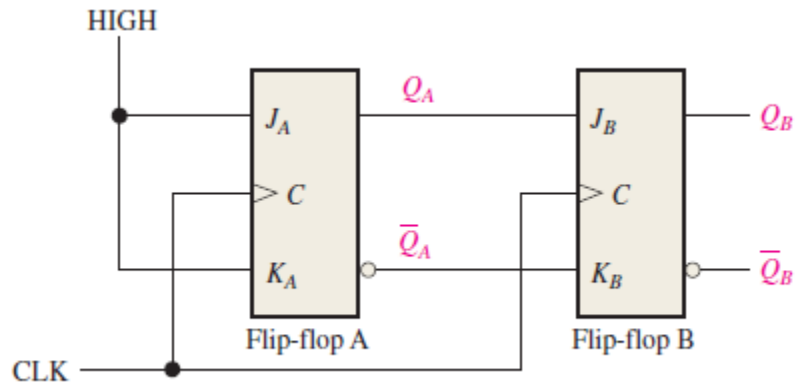
17. Show how to connect a 4-bit asynchronous counter for each of the following moduli. Also for 30kHz clock determine the frequency at the output of each counter.

(a) 9    (b) 11    (c) 13    (d) 14    (e) 15

18. A D flip-flop is connected as shown in Figure 7-90. Determine the Q output in relation to the clock. What specific function does this device perform?



19. For the circuit in Figure, develop a timing diagram for eight clock pulses, showing the QA and QB outputs in relation to the clock.



22. Design a counter to produce the following binary sequence. Use J-K flip-flops.  
1, 4, 3, 5, 7, 6, 2, 1, ....
23. Design a counter to produce the following binary sequence. Use J-K flip-flops.  
0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, ...
24. Design a binary counter with the sequence shown in the state diagram of Figure.  
(using D flip flop)

