

Course Code: EE1005	Course Name: Digital Logic Design (DLD)
Instructor Name / Names: Mr. Aamir , Mr Aashir , Mr. Behraj , Mr. Hamza, Ms. Rabia Tabassum, Ms. Rukhsar , Ms. Sumaiyah , Mr. Zakir	
Student Roll No:	Section No:

Instructions:

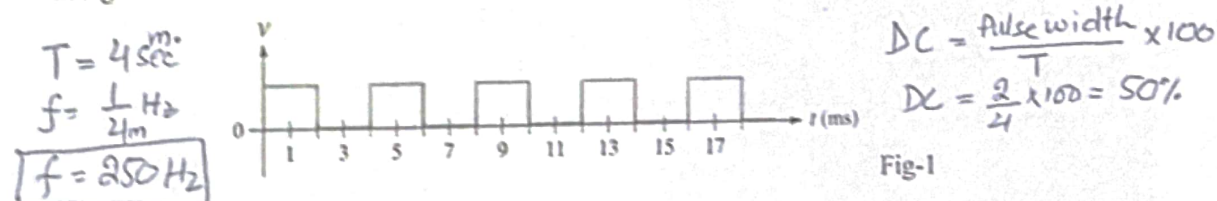
- Return the question paper.
- Read each question completely before answering it. There are 3 questions and 2 pages.
- In case of any ambiguity, you may make assumption. But your assumption should not contradict any statement in the question paper.
- All the answers must be solved according to the sequence given in the question paper.
- This paper is subjective.

Time: 60 minutes.

Max Marks: 45 points

Question 1: (Digital System) [18]

- a) For the digital waveform shown in Fig.-1, determine the duty cycle and frequency of the waveform in Fig.-1 [2]



- b) Express the decimal number (-98) in binary as an 8-bit sign-magnitude number, the 1's complement form, and 2's complement form. [6]

8 bit-sign-mag. +98 01100010 & -98 11100010
 1's Complement 10011101
 2's Complement 10011110

- c) Perform the following 8-bit sign numbers operation: [2]
 $10001100 + 00111001$

$$\begin{array}{r}
 10001100 \\
 00111001 \\
 \hline
 11000101
 \end{array}$$

- d) Convert the following number in BCD [2]
 (i) 10110101_2 (ii) 567_{10}

(i) 10110101_2
 $= 181_{10}$

BCD = 0001 1000 0001

(ii) 567_{10}

0101 0110 0111 = BCD

- e) Convert the following grey code in binary number (i) 1011 (ii) 1100

[2]

(i) 1011 → Binary 1101 (ii) 1100 → Binary 1000

- f) Solve the following operations in binary form:

[4]

- (i) $1101_2 \times 1010_2$ (ii) $1011_2 \div 11_2$

$$\begin{array}{r} 1101 \\ 1010 \\ \hline 0000 \\ 1101x \\ 0000xx \\ 1101xxx \\ \hline 10000010 \end{array}$$

(ii) 10000010

$$\begin{array}{r} 11 \\ 11 \overline{) 1011} \\ \underline{1001} \\ 10 \end{array}$$

(ii) 11 with remainder 10

Question 2: (Logic Gates and Its Applications) [7]

- a) Your instructor teaches CS1005 to the students where some of them are registered and some of them are not, he asked you to design a logic diagram which will be used for checking if the student is allowed to sit in exam or not based on following scenario:

If the student is registered and his/her attendance is 80% then the student is allowed to sit in exam otherwise not.

The attendance of the student below 80% is represented by LOW signal and above 80% by HIGH signal.

Before drawing the logic diagram, you must write down the truth table and logic expression from the table as well. Your logic circuit will be connected to a RED light which will remain off if the student is allowed to sit in exam otherwise ON.

[4]

Registration	Attendance	Allowed
0	0	1
0	1	1
1	0	1
1	1	0

$$X = \overline{A}B$$



- b) Determine the output waveform in Fig-2 and draw the timing diagram with respect to given number (1 to 16) in answer sheet.

[3]

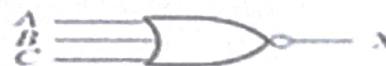
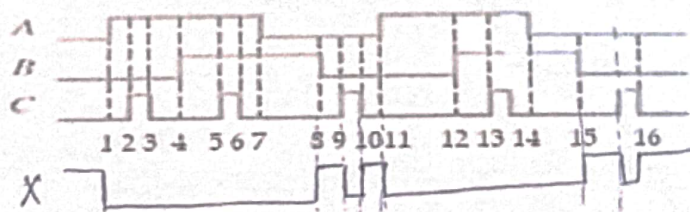


Fig-2

Question 3: (Boolean Algebra) [20]

- a) Apply DeMorgan's theorems to the expression and simplify it.

[4]

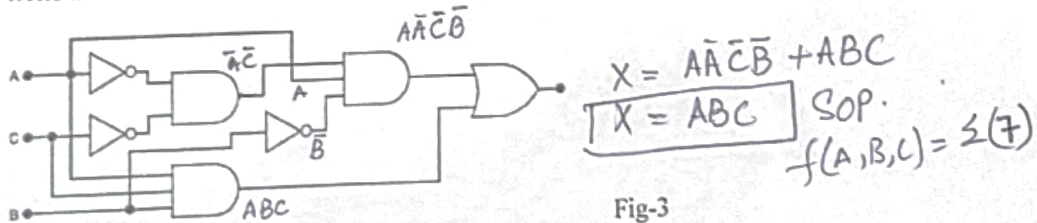
$$\begin{aligned} & \overline{\overline{A+B\bar{C}} + \overline{(A+C)D} + \overline{AB}} \\ & \overline{A+B\bar{C}} + \overline{(A+C)D} + \overline{AB} \\ & \left[\overline{(A+B\bar{C})} \cdot \overline{(A+C)D} \right] AB \\ & \left[(A+B\bar{C}) \cdot \overline{(A+C)D} \right] AB \\ & \left[(A+B\bar{C})(A+C+D) \right] AB \\ & \left[AA+AC+A\bar{D}+AB\bar{C} + B\bar{C}C + B\bar{C}\bar{D} \right] AB \\ & \left[A+AC+A\bar{D}+AB\bar{C} + B\bar{C}\bar{D} \right] AB \\ & = \left[A[1+C+\bar{D}] + AB\bar{C} + B\bar{C}\bar{D} \right] AB \\ & \left[A+AB\bar{C} + B\bar{C}\bar{D} \right] AB \\ & \left[A[1+B\bar{C}] + B\bar{C}\bar{D} \right] AB \\ & \left[A+B\bar{C}\bar{D} \right] AB \\ & AAB + AB\bar{B}\bar{C}\bar{D} \\ & AB + ABC\bar{D} \\ & AB[1+C\bar{D}] = AB \end{aligned}$$

[6]

- b) Simplify it using Boolean algebra. Also develop the truth table.

$$\begin{aligned} & \bar{A}C(\bar{A}BD) + \bar{A}B(\bar{C}+D) + \bar{A}\bar{B}C \\ & \bar{A}C[A+\bar{B}+\bar{D}] + \bar{A}B(\bar{C} \cdot \bar{D}) + \bar{A}\bar{B}C \\ & \bar{A}AC + \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C \\ & \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C \\ & \bar{B}C(\bar{A}+A) + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} \\ & \bar{B}C + \bar{A}D(C+B\bar{C}) \\ & \bar{B}C + \bar{A}\bar{D}(C+B) \\ & \bar{B}C + \bar{A}C\bar{D} + \bar{A}\bar{D}B \end{aligned}$$

- c) Write the standard SOP and POS forms of the logic expression for the following circuits (Fig-3). [4]



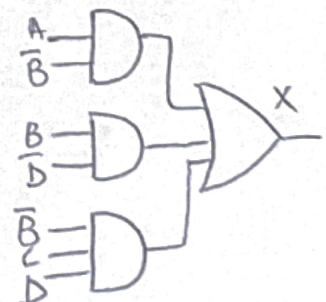
$$\begin{aligned} & \text{POS} \Rightarrow f(A,B,C) = \prod(0,1,2,3,4,5,6) \\ & (A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})(\bar{A}+B+C)(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+C) = \text{POS} \end{aligned}$$

- d) Use a Karnaugh map to simplify (in SOP form) the given Boolean functions. Implement the simplified form into circuit. [6]

$$F(A,B,C,D) = \prod(0,1,2,5,7,13,15)$$

AB \ CD	00	01	11	10
00	0	0	1	0
01	1	0	0	1
11	1	0	0	1
10	1	1	1	1

$$X = A\bar{B} + B\bar{D} + \bar{B}CD$$



BEST OF LUCK!