DIGITAL LOGIC DESIGN EE(1005)

LECTURE-18

Chapter No:5
Combinational Logic Analysis

CHAPTER OUTLINE

- Basic Combinational Logic Circuits
- Implementing Combinational Logic
- The Universal Property of NAND and NOR Gates
- Combinational Logic Using NAND and NOR Gates
- Pulse Waveform Operation

EXAMPLE

When simplifying the expression for the output of a combinational logic circuit, you may encounter the XOR or XNOR operations as you are factoring. This will often lead to the use of XOR or XNOR gates in the implementation of the final circuit. To illustrate, simplify the circuit of Figure 4-24(a).

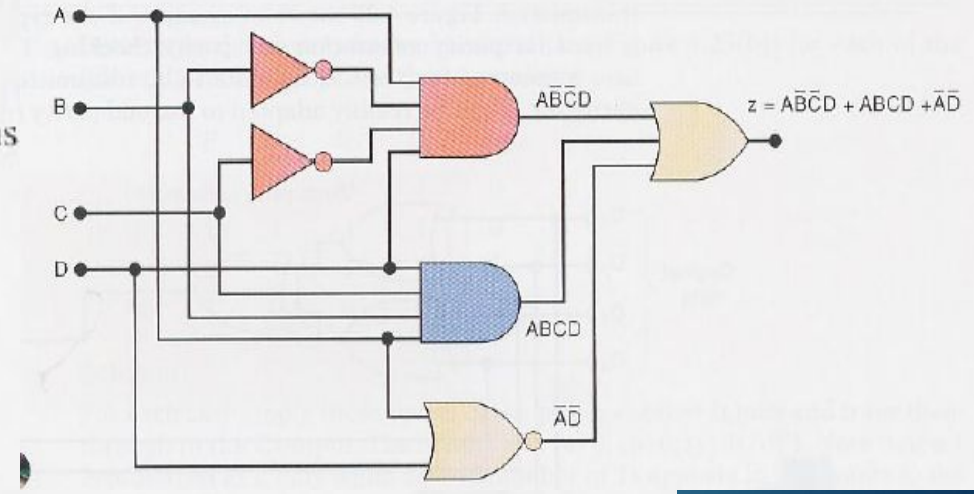
Solution

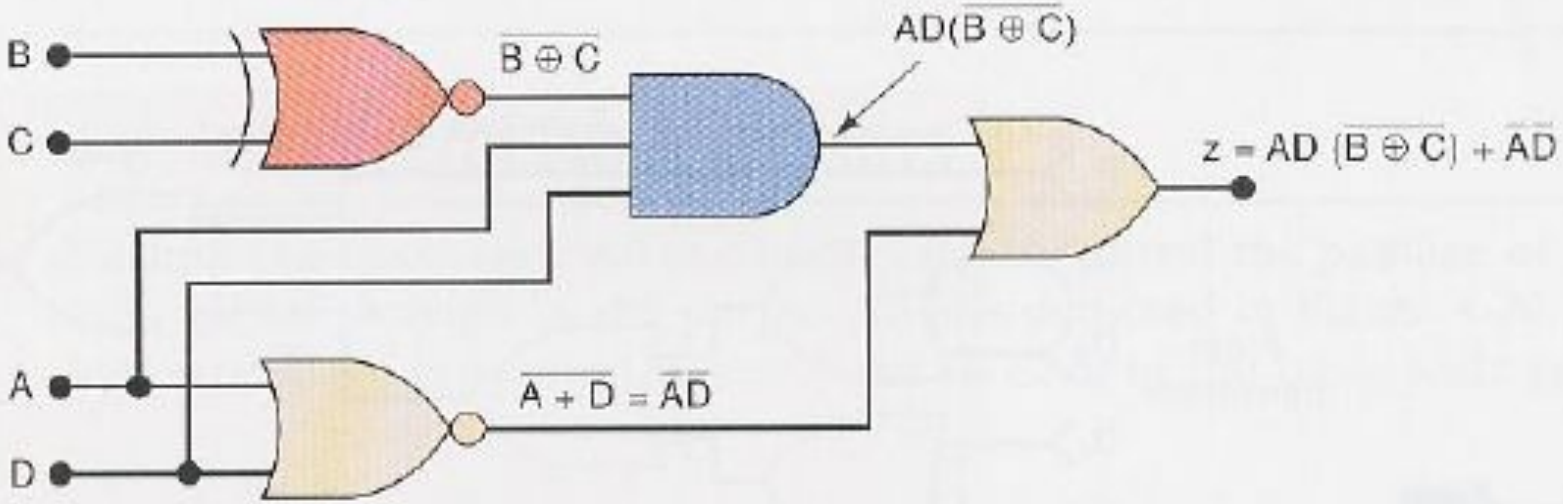
The unsimplified expression for the circuit is obtained as

$$z = ABCD + A\overline{B}\,\overline{C}D + \overline{A}\,\overline{D}$$

We can factor AD from the first two terms:

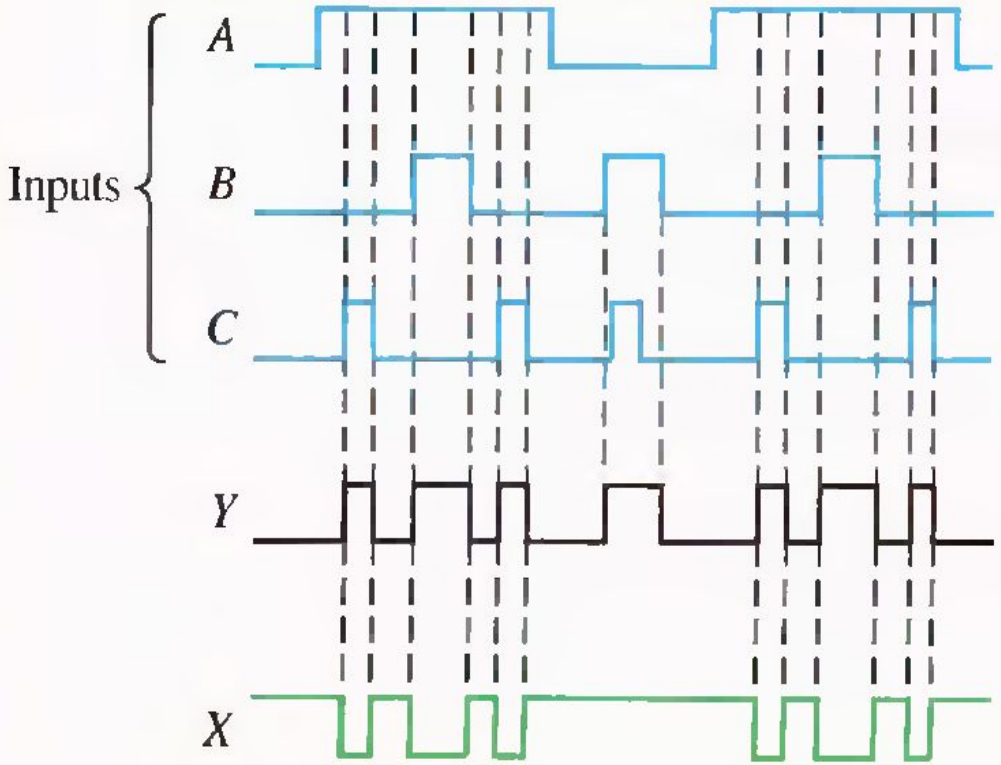
$$z = AD(BC + \overline{B}\,\overline{C}) + \overline{A}\,\overline{D}$$

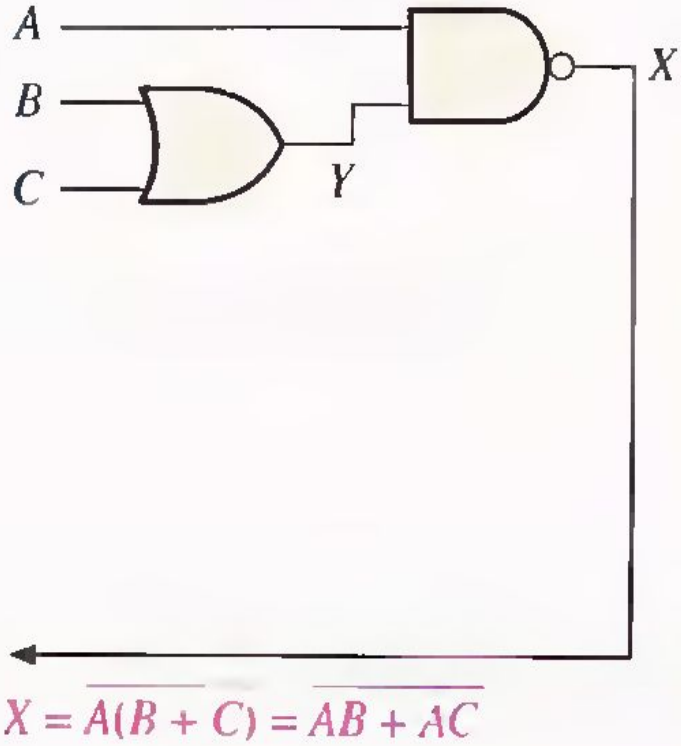




LOGIC CIRCUIT OPERATION WITH PULSE WAVEFORM INPUTS

Determine the final output waveform X for the circuit in Figure

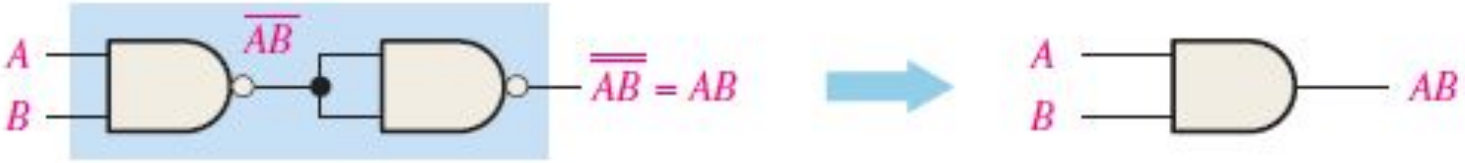




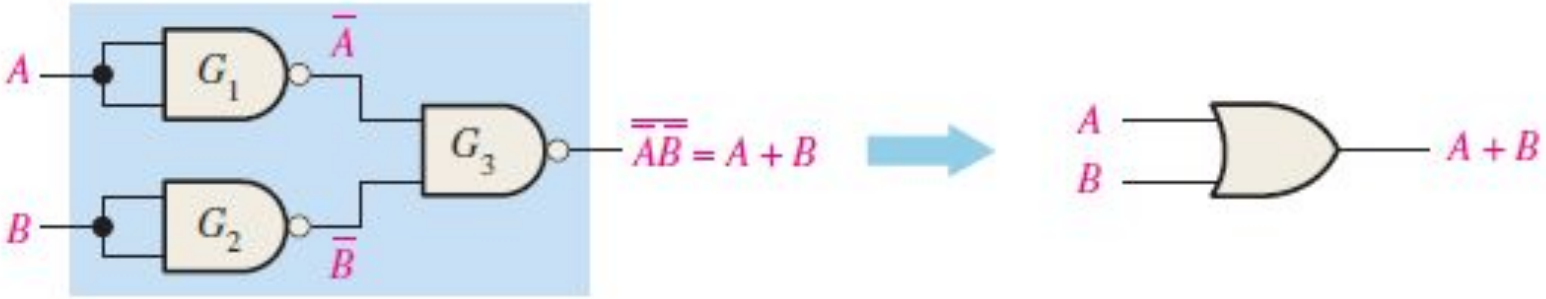
$$X = \overline{A(B + C)} = \overline{AB + AC}$$

The NAND Gate as a Universal Logic Element

(a) One NAND gate used as an inverter

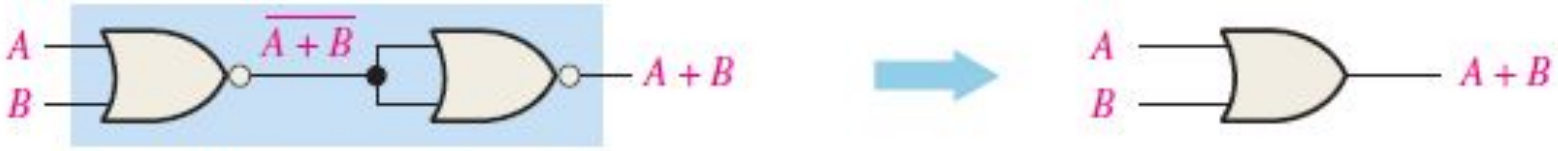


(b) Two NAND gates used as an AND gate

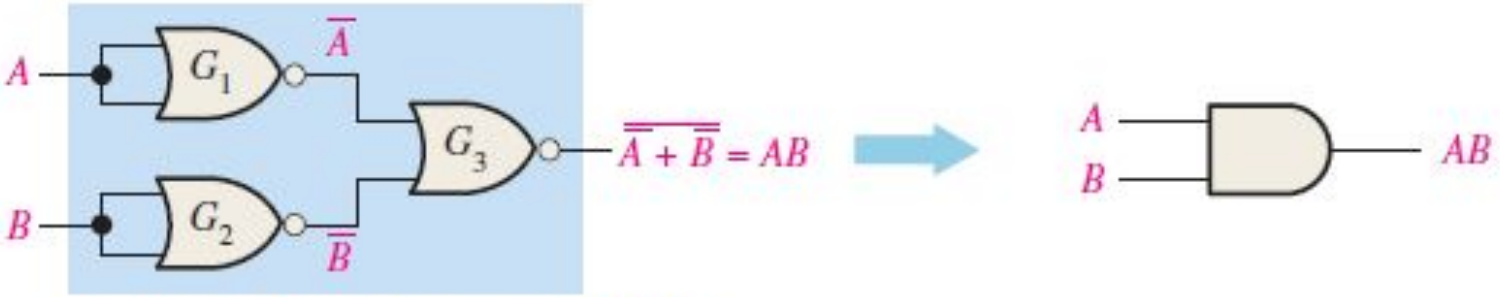


The NOR Gate as a Universal Logic Element

(a) One NOR gate used as an inverter



(b) Two NOR gates used as an OR gate



(c) Three NOR gates used as an AND gate

COMBINATIONAL LOGIC USING NAND AND NOR GATES

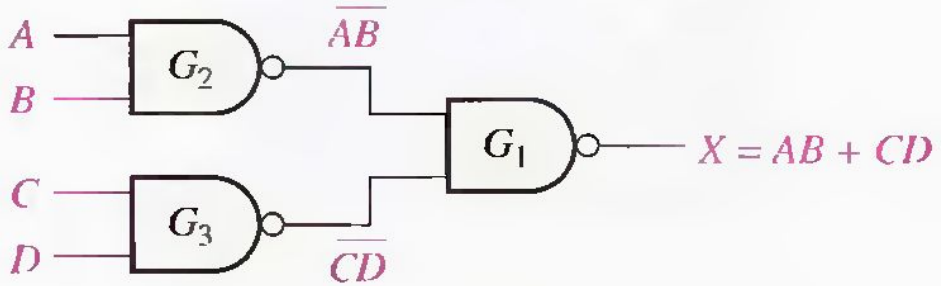
NAND Logic

$$\overline{AB} = \overline{A} + \overline{B}$$

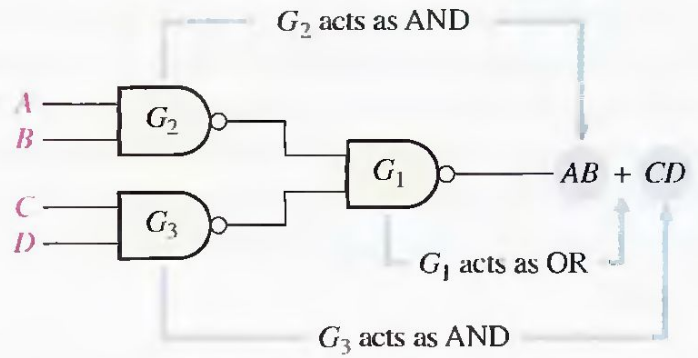
NAND — negative-OR

NAND logic for $X = AB + CD$.

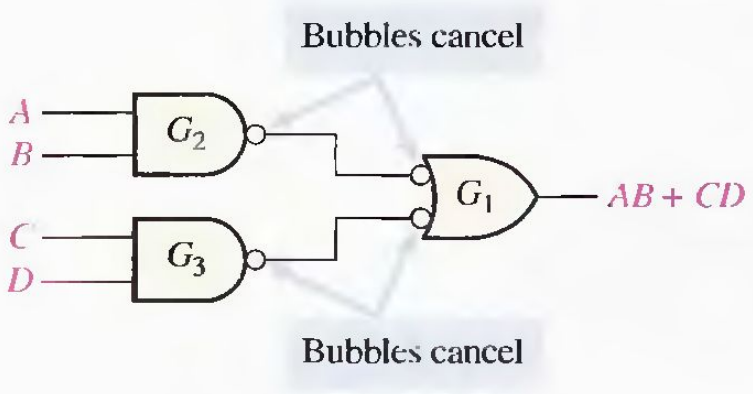
$$\begin{aligned} X &= \overline{(\overline{AB})(\overline{CD})} \\ &= \overline{(\overline{A} + \overline{B})(\overline{C} + \overline{D})} \\ &= (\overline{\overline{A} + \overline{B}}) + (\overline{\overline{C} + \overline{D}}) \\ &= \overline{\overline{A}}\,\overline{\overline{B}} + \overline{\overline{C}}\,\overline{\overline{D}} \\ &= AB + CD \end{aligned}$$



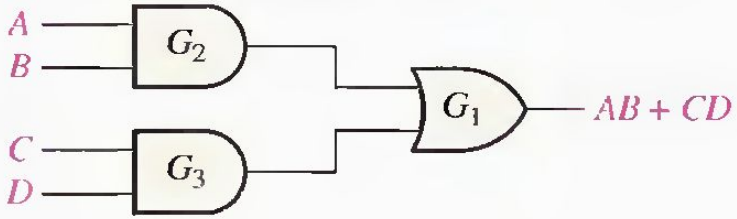
NAND Logic Diagrams Using Dual Symbols



(a) Original NAND logic diagram showing effective gate operation relative to the output expression

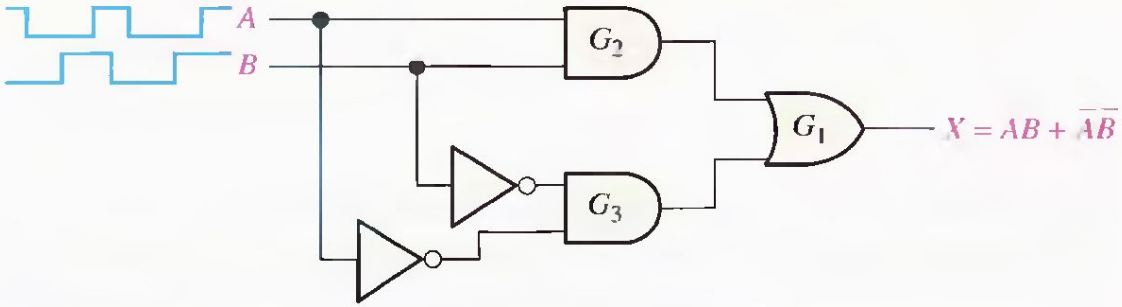


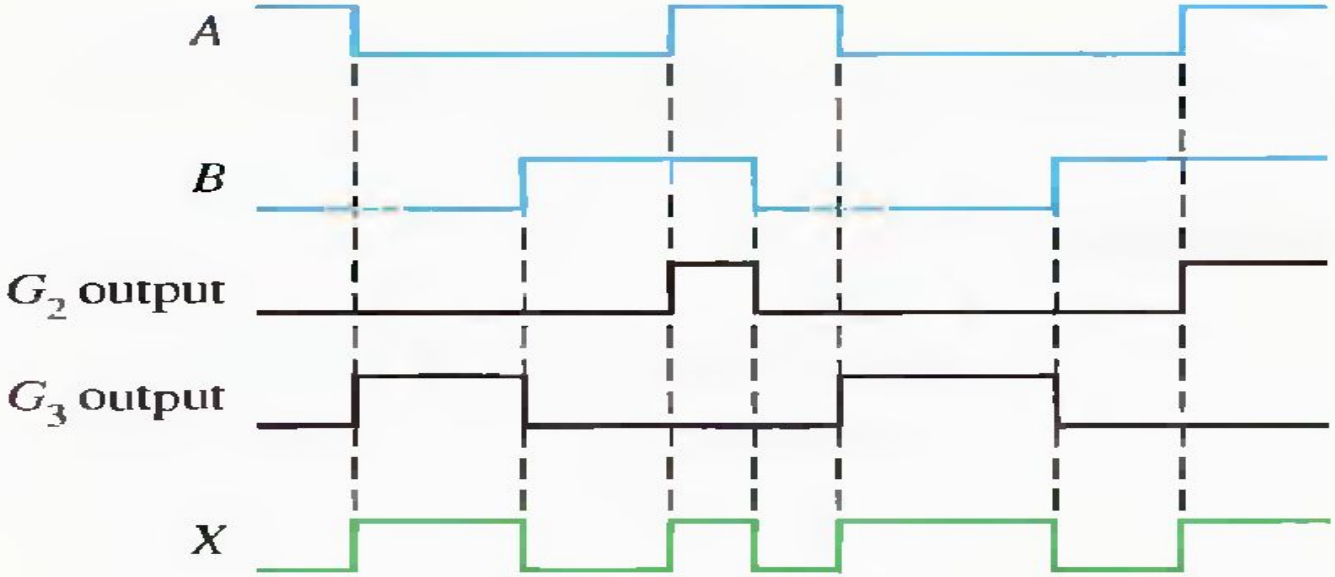
(b) Equivalent NAND/Negative-OR logic diagram



(c) AND-OR equivalent

Draw the timing diagram for the circuit in Figure 5–30 showing the outputs of G_1, G_2, and G_3 with the input waveforms, A, and B, as indicated.





Determine the output waveform X for the logic circuit in Figure. By first finding the intermediate waveform at each of points Y1, Y 2, Y 3 , and Y4.