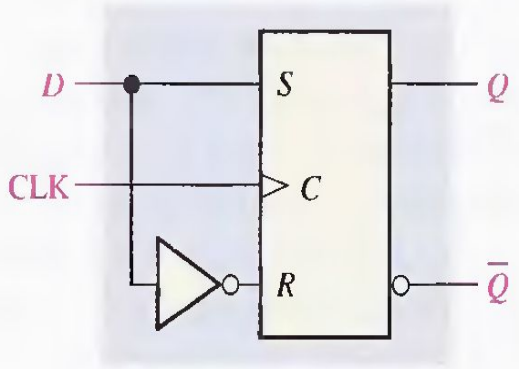
Digital Logic Design EE(1005)

Chapter No:7
Latches and Flip Flop

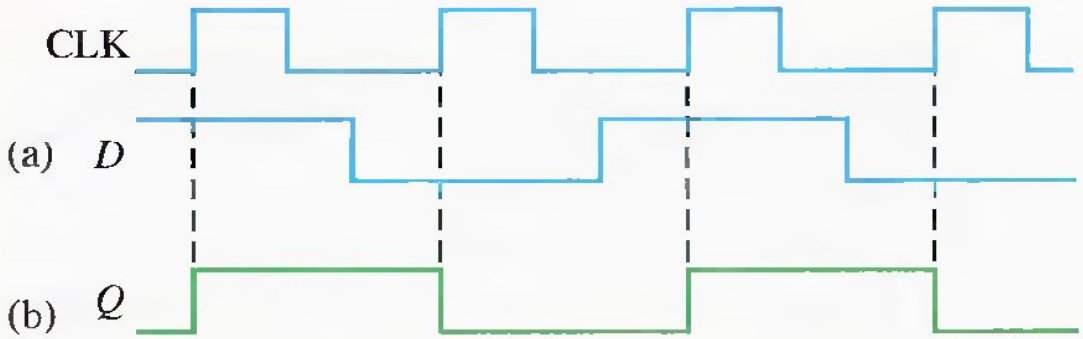
The Edge-Triggered D Flip-Flop

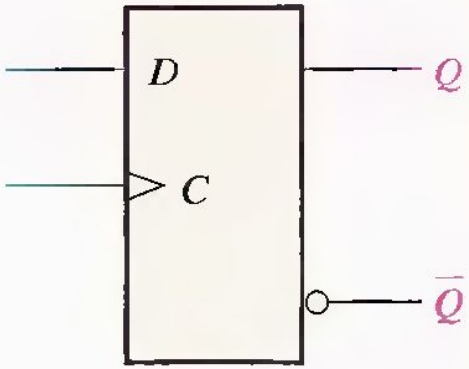
The **D flip-flop** is useful when a single data bit (1 or 0) is to be stored.



INPUTS		OUTPUTS		
D	CLK	Q	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH





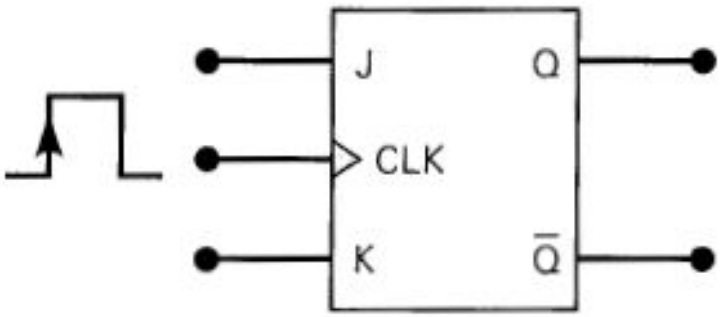
The Edge-Triggered J-K Flip-Flop

The J and K inputs control the state of the FF in the same ways as the S and C input do for the clocked S-C Flip Flop except one major difference:

The J=K=1 condition does not result in an ambiguous output.

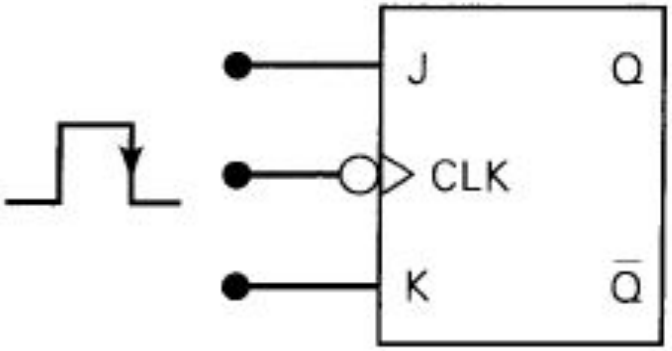
For this condition J=K=1, the FF will always go to its opposite state upon the positive transition of the clock signal. This is called the

Toggle Mode of operation.



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

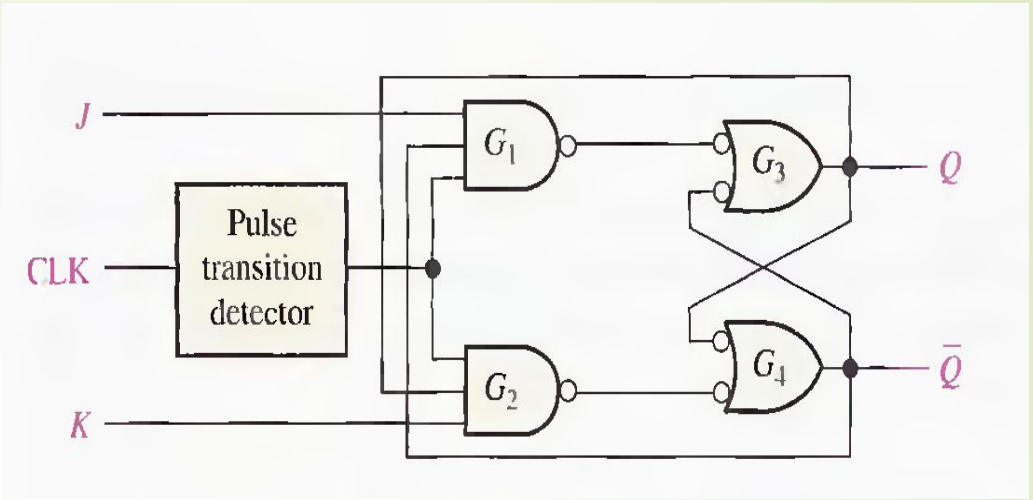
J-K flip-flop that triggers only on negative-going transitions.



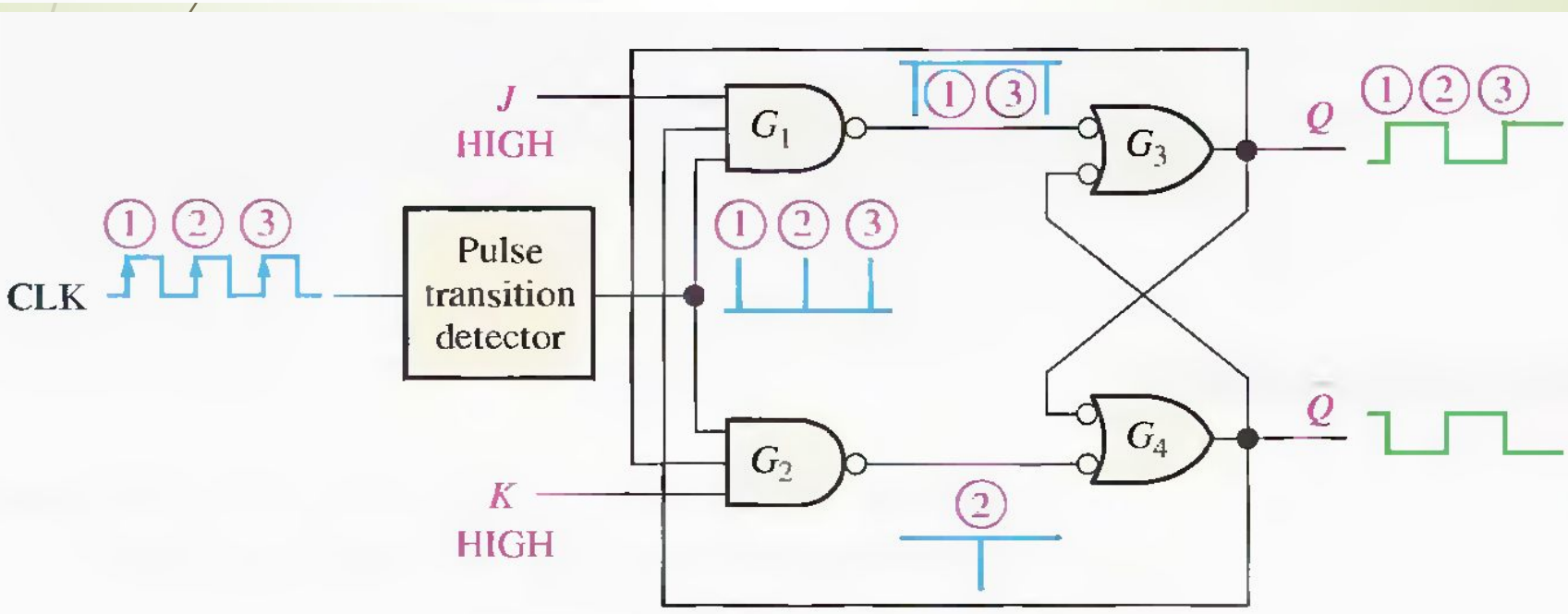
J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q}_0$ (toggles)

The Edge-Triggered J-K Flip-Flop

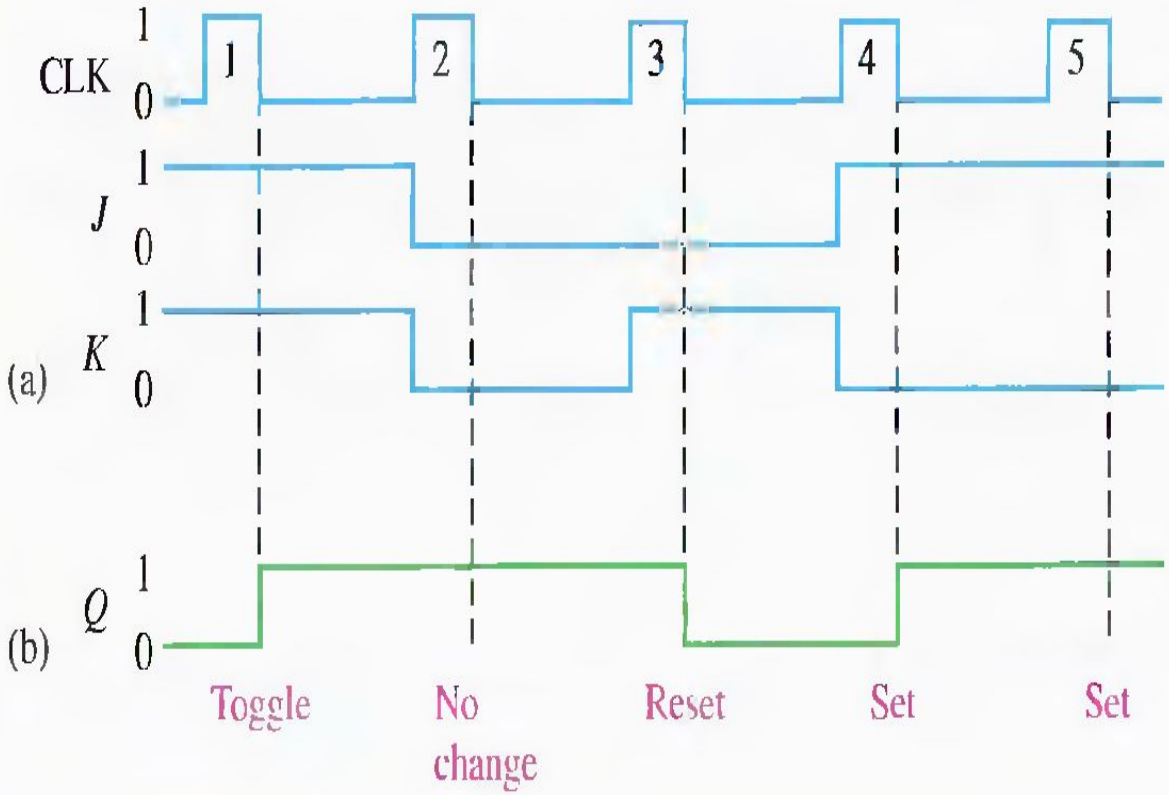
A simplified logic diagram for a positive edge-triggered J-K flip-flop.

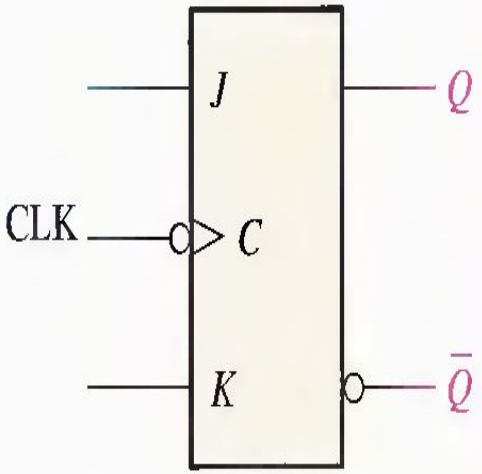


Transitions illustrating the toggle operation when $J = 1$ and $K = 1$.

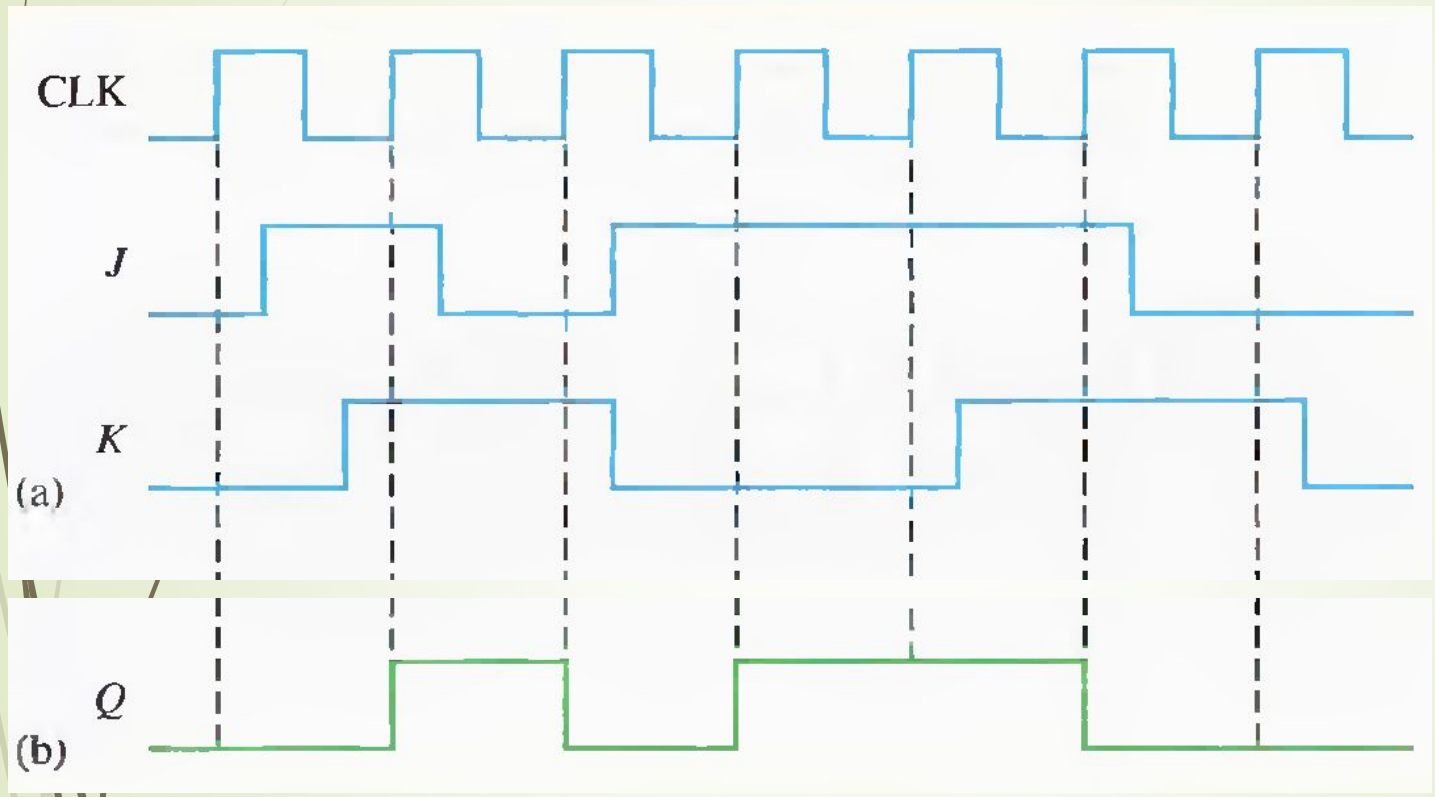


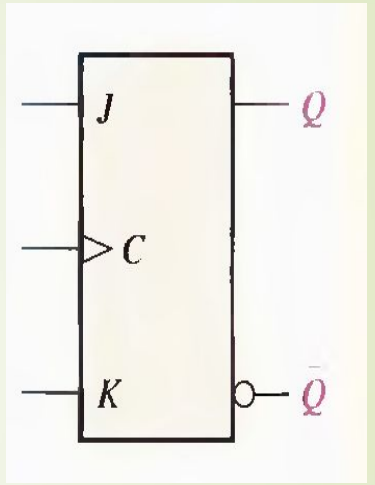
The waveforms in Figure are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.



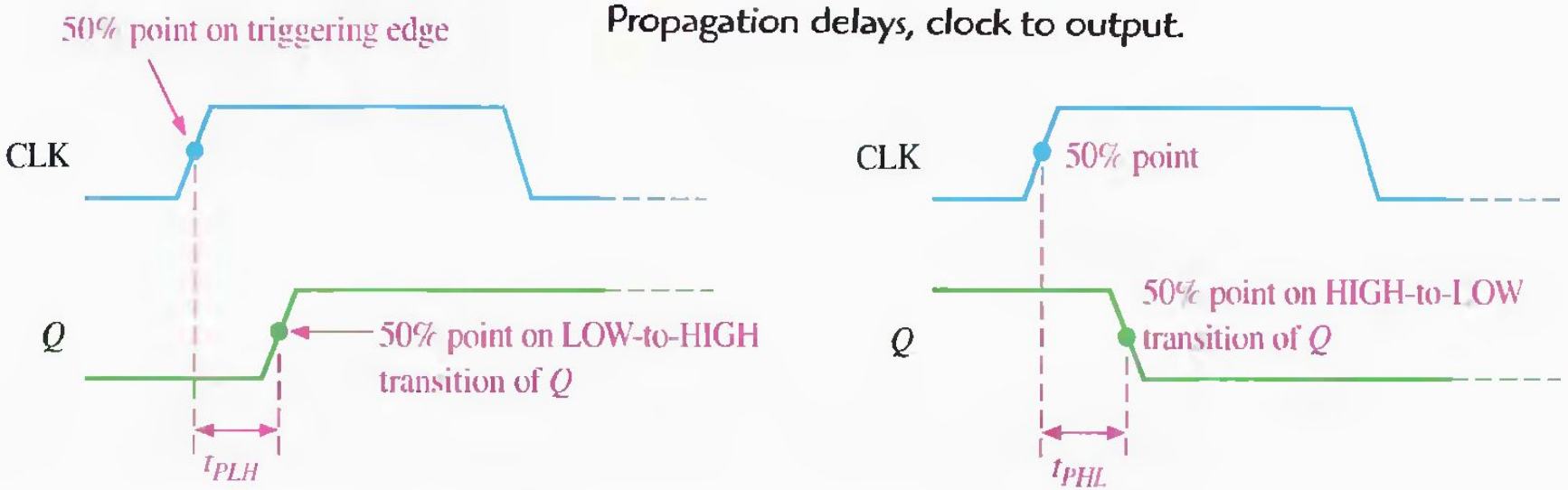


The waveforms in Figure are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.



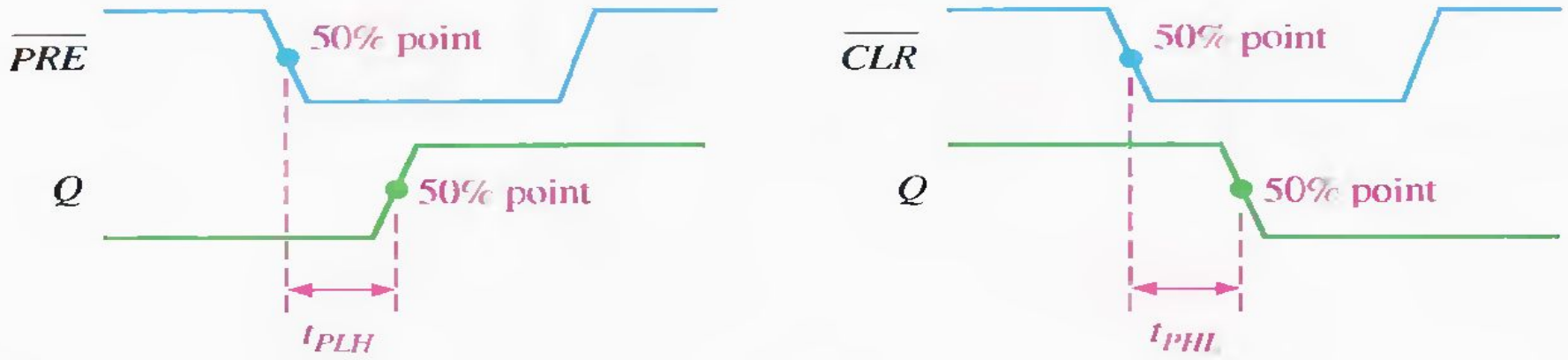


Propagation Delay Times



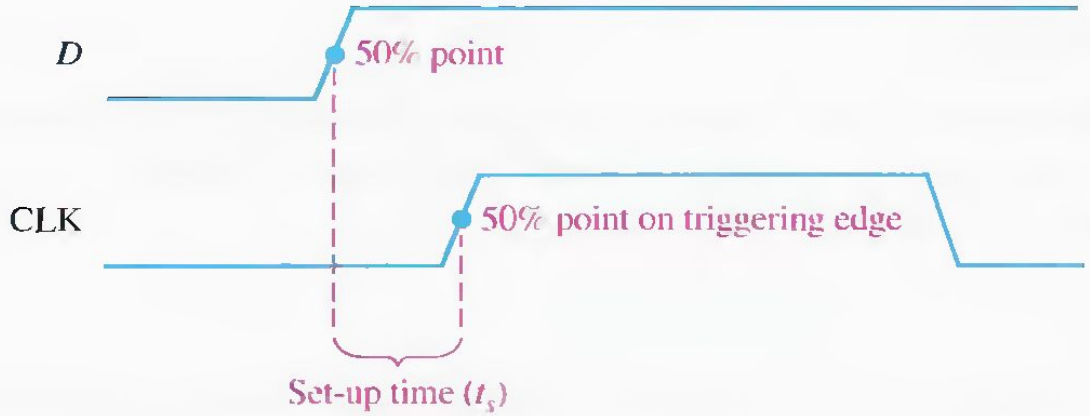
Propagation delays, clock to output.

Propagation delays, preset input to output and clear input to output.



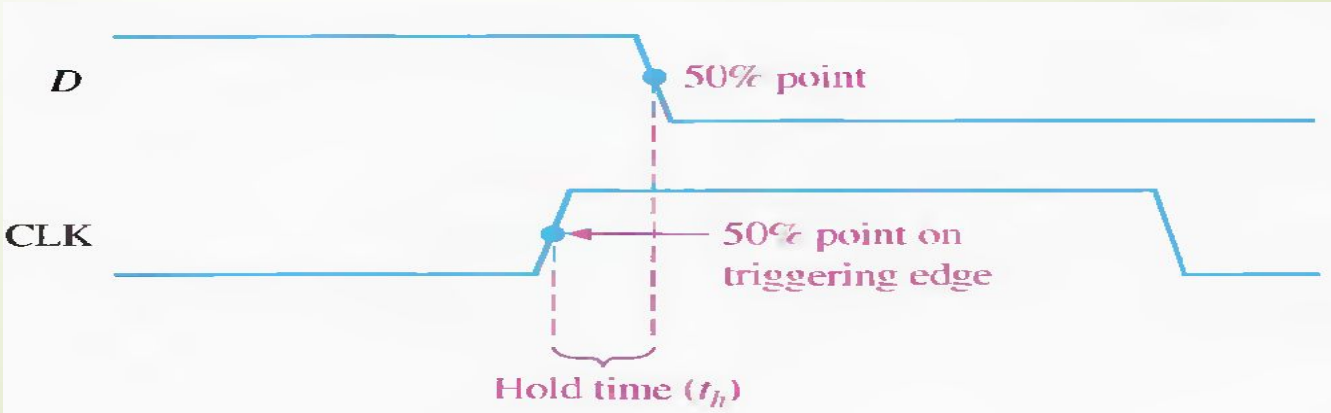
Set-up Time

The set-up time (ts) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or Sand R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Hold Time

The hold time (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Maximum Clock Frequency

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5\text{ V} \times 5\text{ mA} = 25\text{ mW}$$