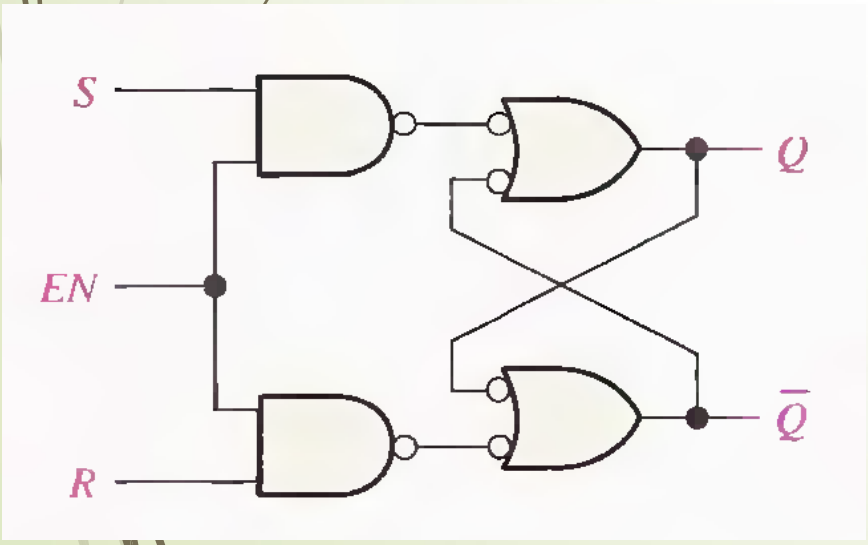
Digital Logic Design EE(1005)

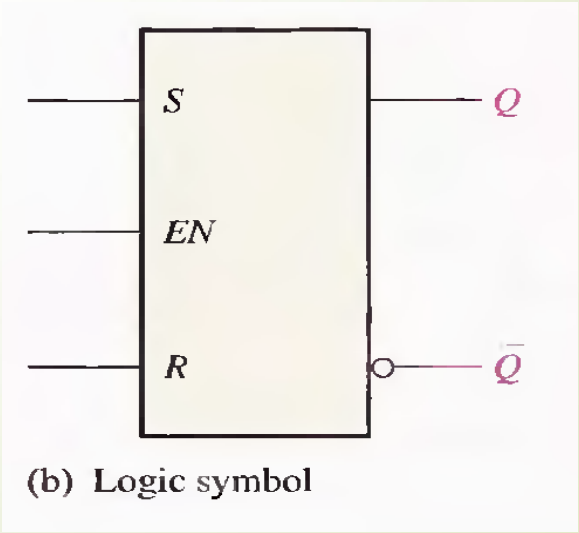
Lecture- 25

Chapter No:7
Latches and Flip Flop

The Gated S-R Latch

A gated latch requires an enable input. EN (G is also used to designate an enable input). The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs. In this circuit, the invalid state occurs when both Sand R are simultaneously HIGH.

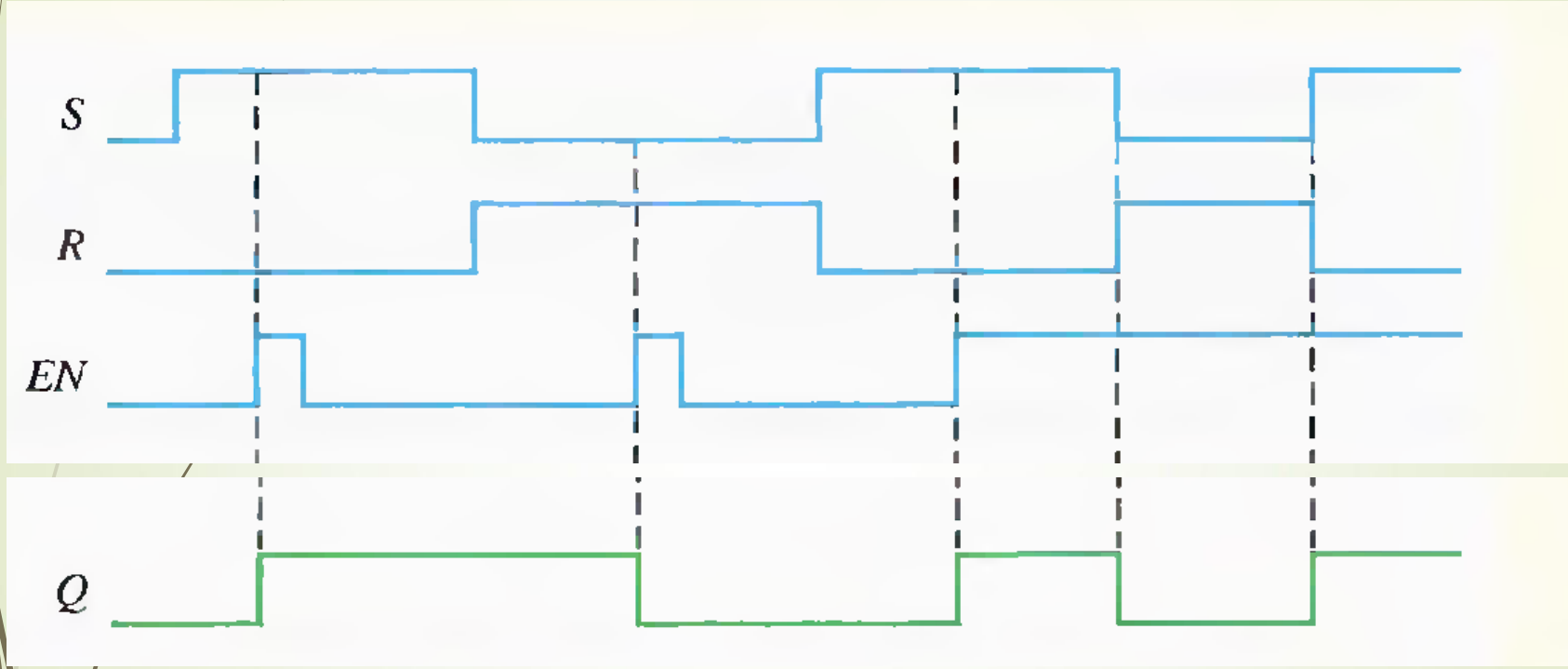




(b) Logic symbol

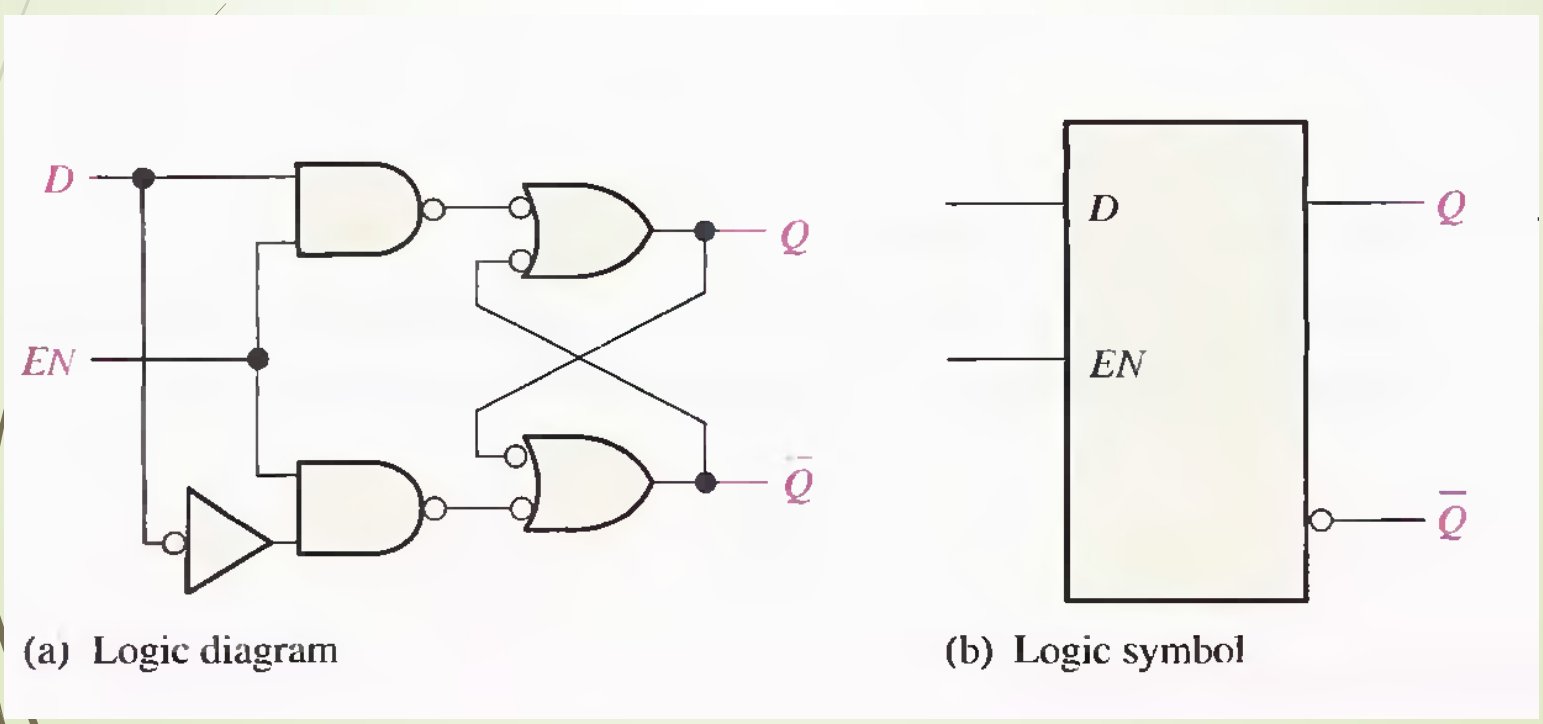
a gated S-R latch that is initially RESET.

Determine the Q output waveform



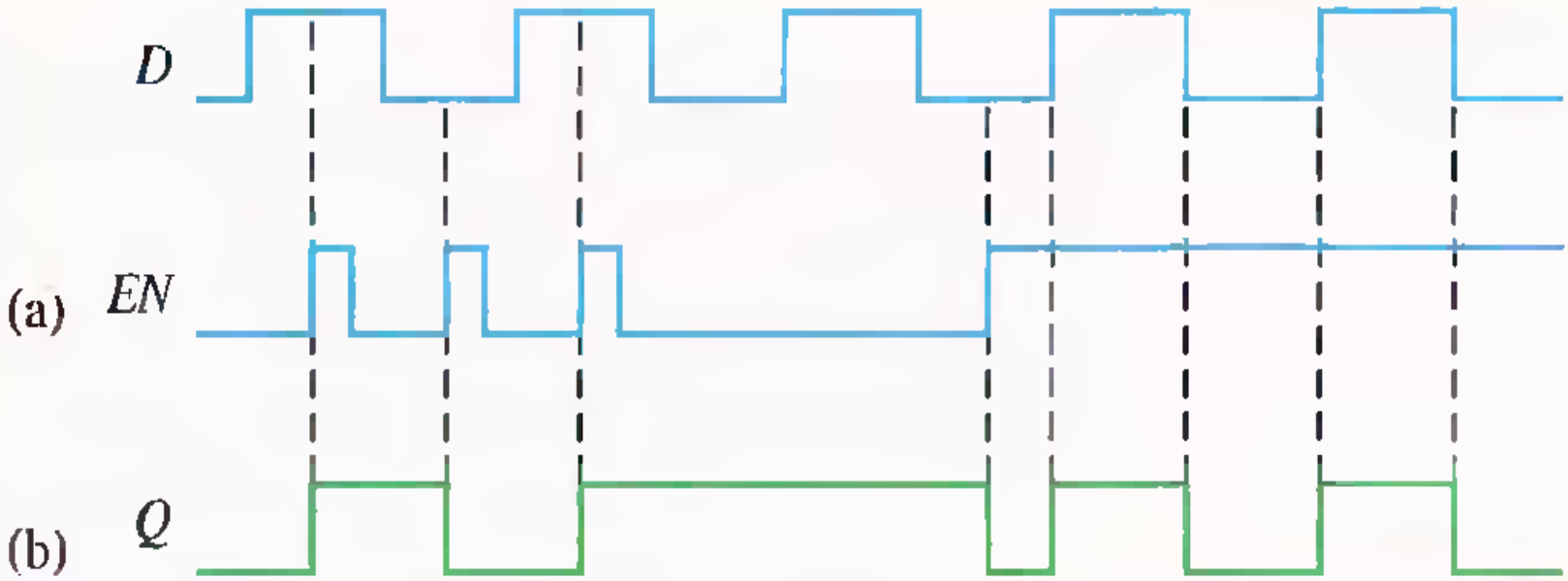
The Gated D Latch

Gated D latch is differs from the S-R latch because it has only one input in addition to EN. This input is called the D (data) input. When the D input is HIGH and the EN input is HIGH, the latch will set. When the D input is LOW and EN is HIGH, the latch will reset. Stated another way, the output Q follows the input D when EN is HIGH.



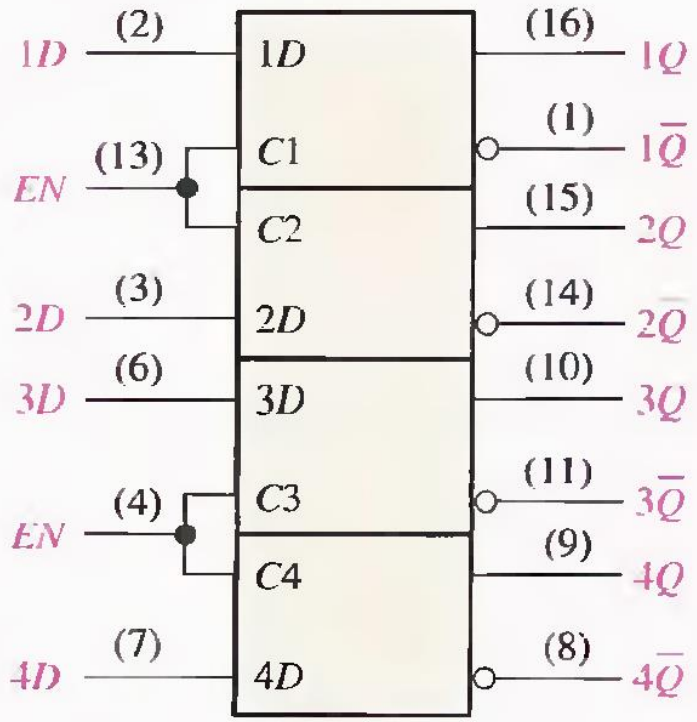
(a) Logic diagram (b) Logic symbol

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



THE 74LS75 D LATCH

The 74LS75 quad gated D latches.



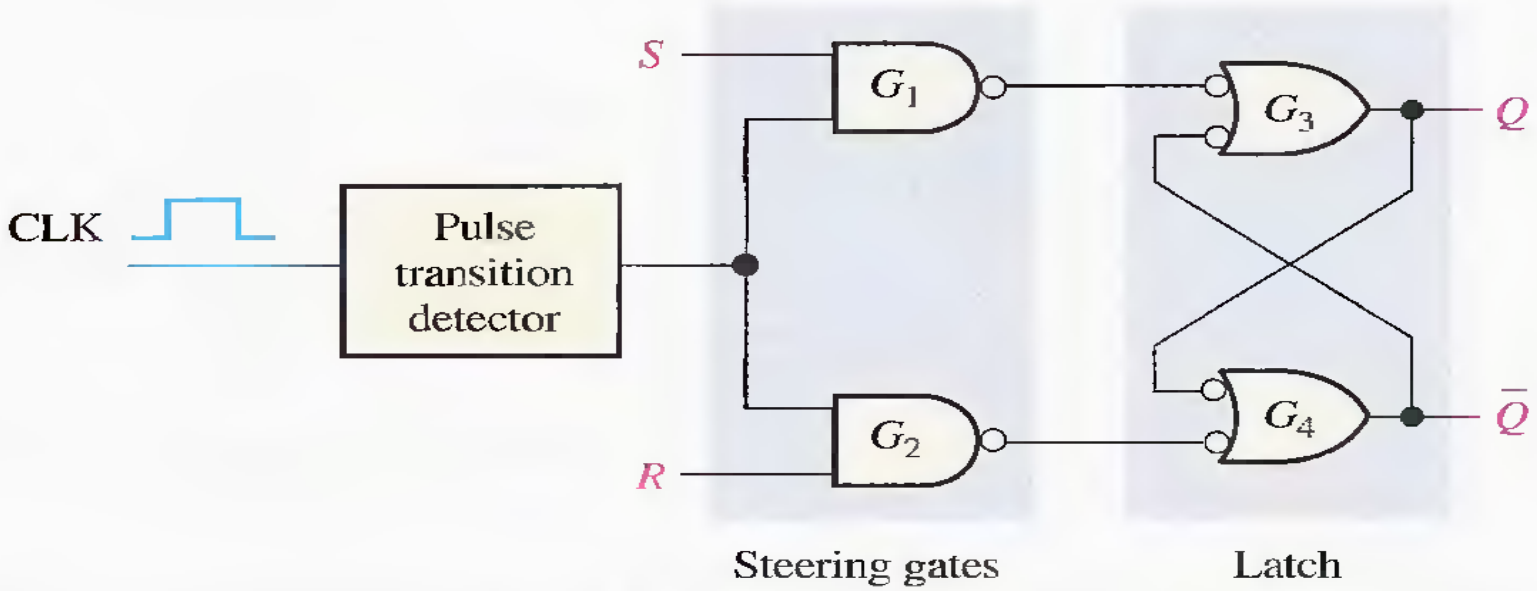
(a) Logic symbol

Inputs		Outputs		
D	EN	Q	$\overline{Q}$	Comments
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

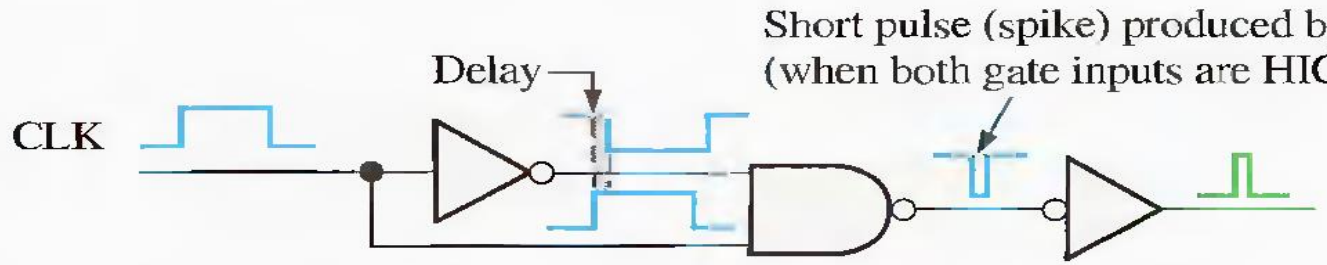
Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

A Method of Edge-Triggering

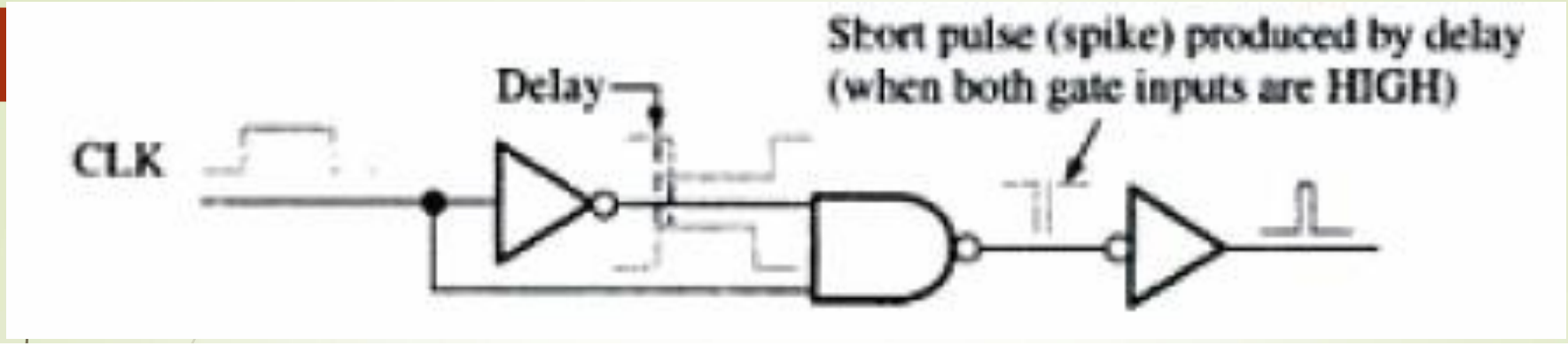


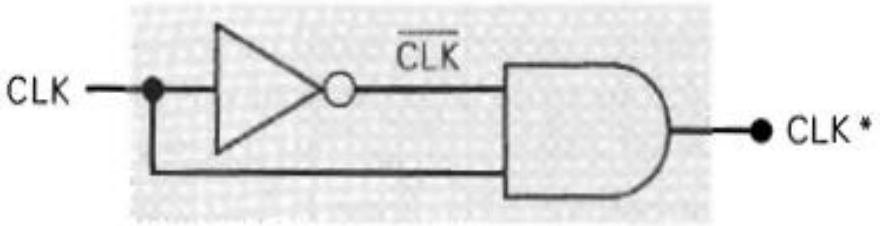
(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

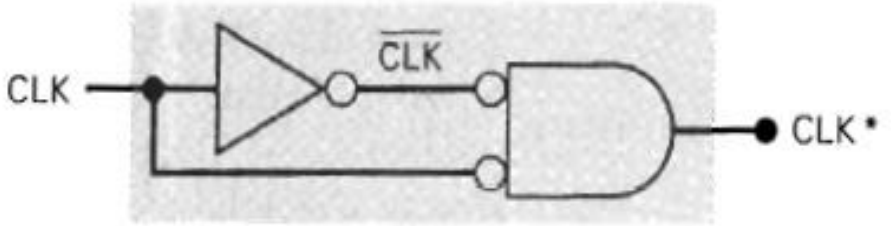


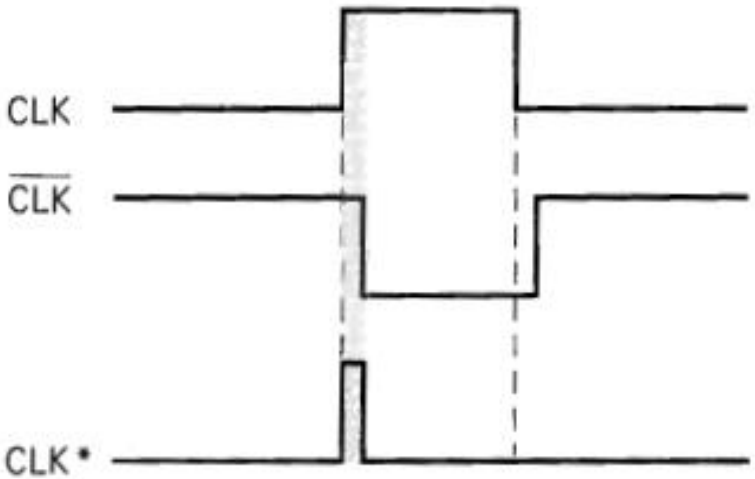
(b) A type of pulse transition detector

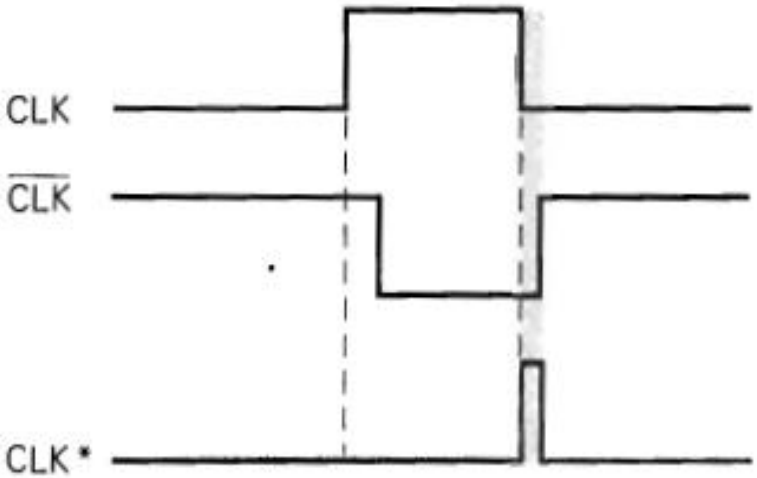
A type of Pulse Transition detector



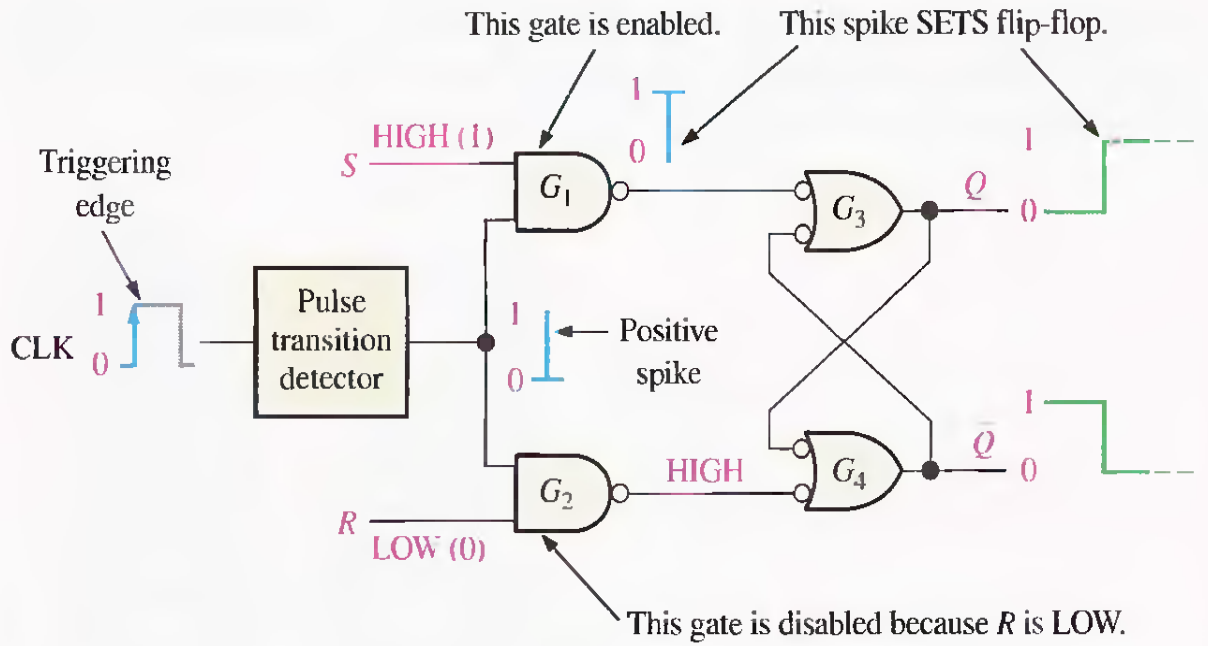








Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.



Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.