DIGITAL LOGIC DESIGN EE(1005)

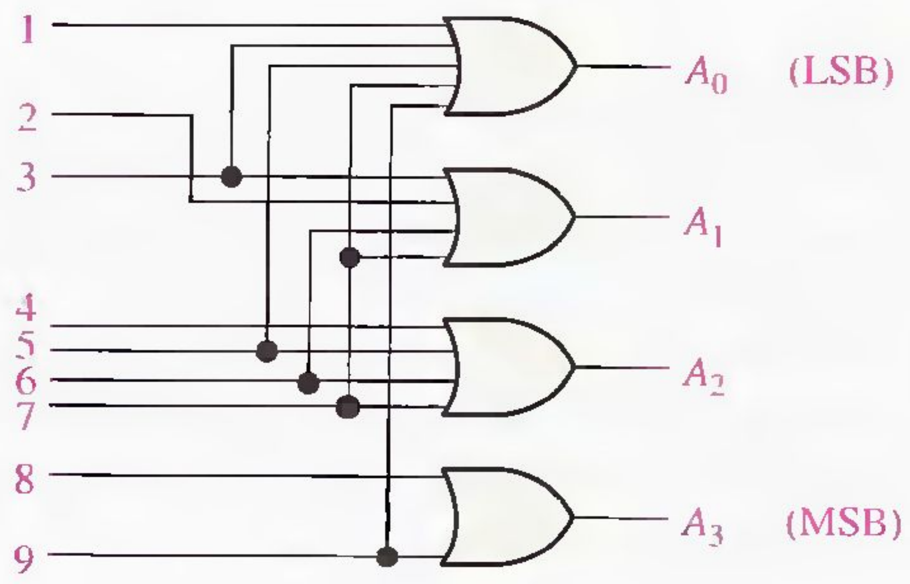
LECTURE-22

Chapter No:6 Function of combinational logic

TOPICS

1. Half and Full Adders
2. Parallel Binary Adders
3. Comparators
4. Decoders
5. Encoders
6. Code Converters
7. Multiplexers (Data Selectors)
8. Demultiplexers

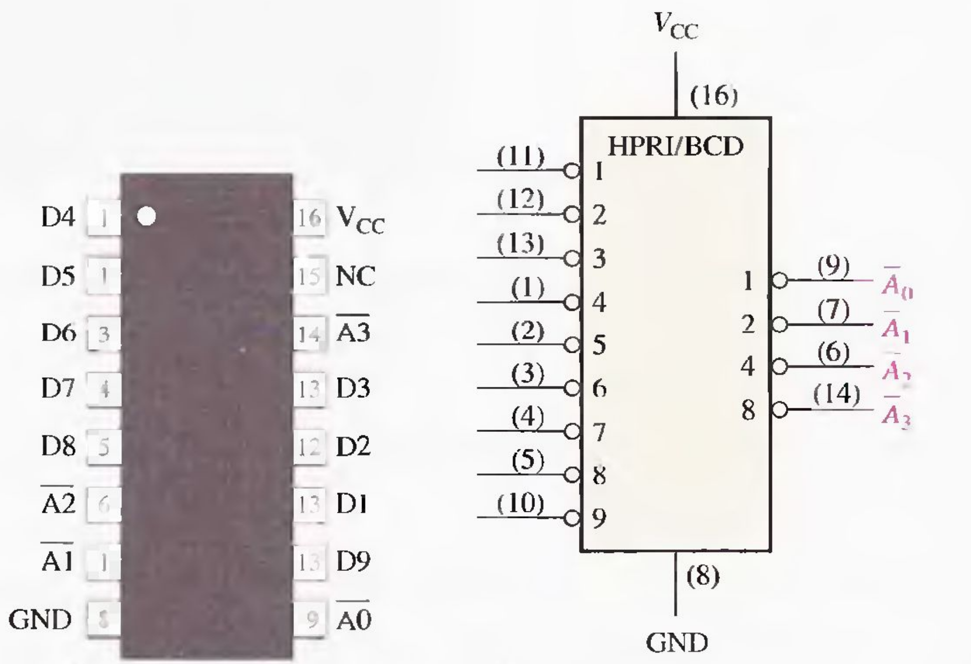
ENCODERS



Basic logic diagram of a decimal-to-BCD encoder. A 0-digit input is not needed because the BCD outputs are all LOW when there are no HIGH inputs.

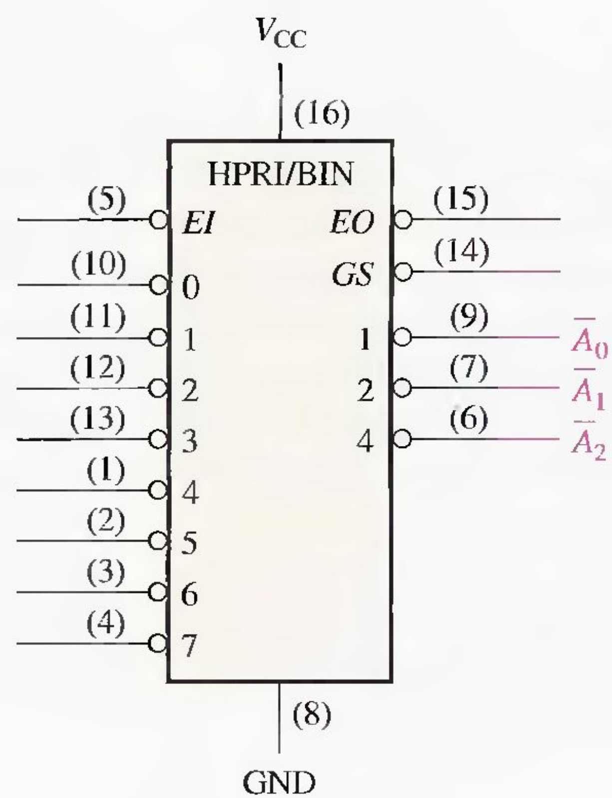
The Decimal-to-BCD Priority Encoder This type of encoder performs the same basic encoding function as previously discussed. A **priority encoder** also offers additional flexibility in that it can be used in applications that require priority detection. The priority function means that the encoder will produce a BCD output corresponding to the *highest-order decimal digit* input that is active and will ignore any other lower-order active inputs. For instance, if the 6 and the 3 inputs are both active, the BCD output is 0110 (which represents decimal 6).

THE 74HC147 DECIMAL-TO-BCD ENCODER

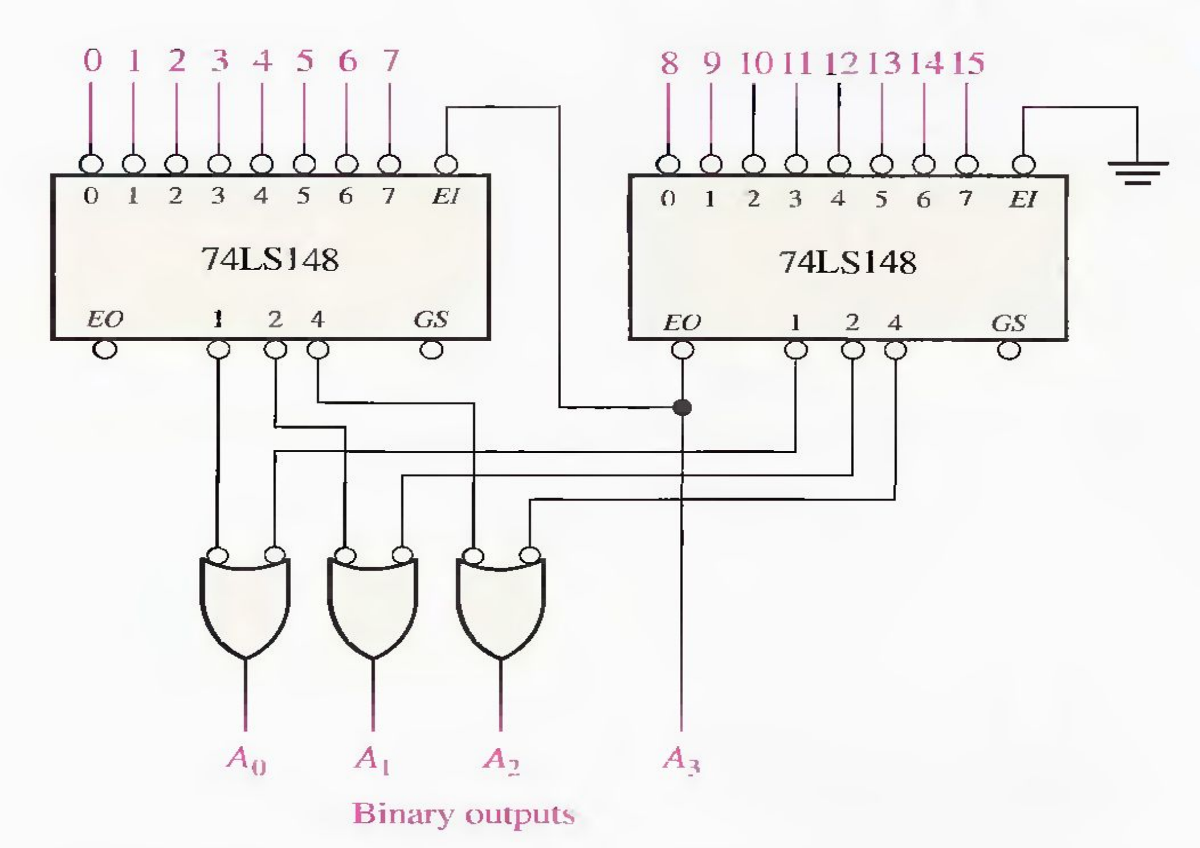


(a) Pin diagram (b) Logic diagram

Logic symbol for the 74LS148 8-line-to-3-line encoder.



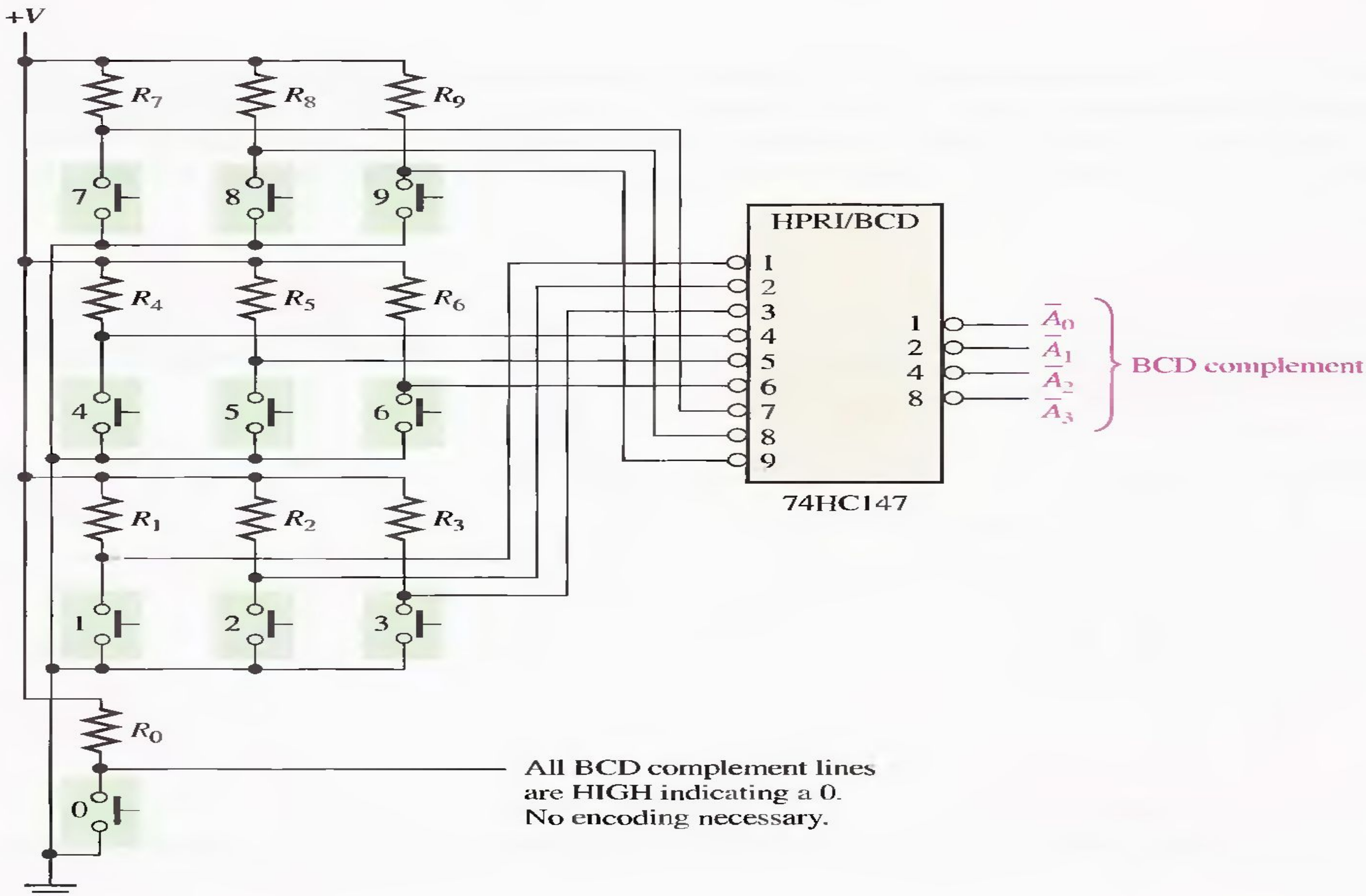
The 74LS148 can be expanded to a 16-1ine-to-4-line encoder by connecting the EO of the higher-order encoder to the EI of the lower-order encoder and negative-ORing the corresponding binary outputs as shown in Figure . The EO is used as the fourth and MSB. This particular configuration produces active-HIGH outputs for the 4-bit binary number.



A 16-line-to-4 line encoder using 74LS148s and external logic.

An Application

A classic application example is a keyboard encoder.

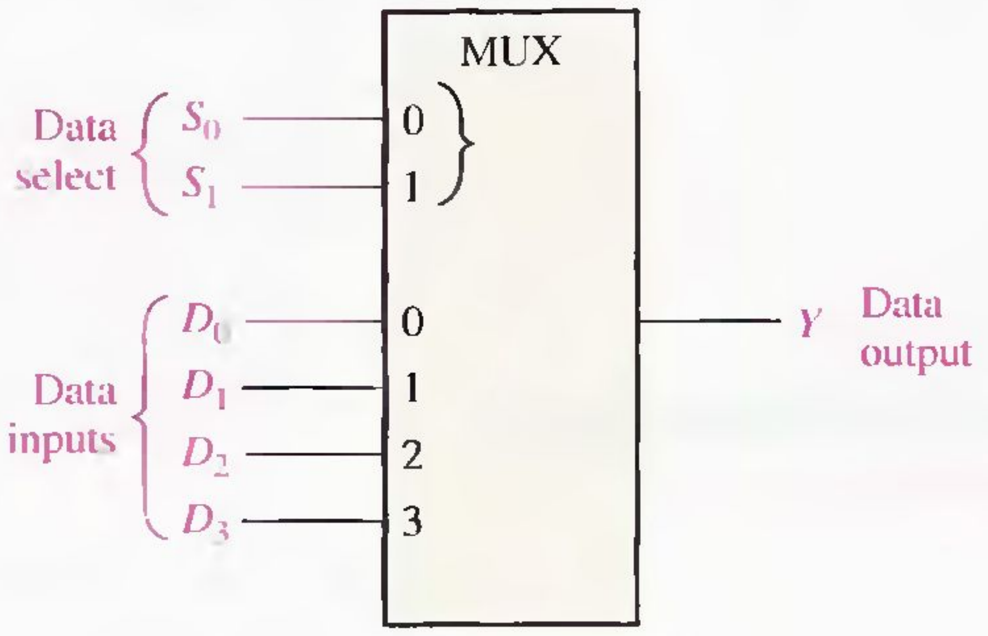


MULTIPLEXERS (DATA SELECTORS)

A **multiplexer (MUX)** is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on any one of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

Logic symbol for a 1-of-4 data selector/multiplexer.

DATA-SELECT INPUTS S_1	S_0	INPUT SELECTED
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



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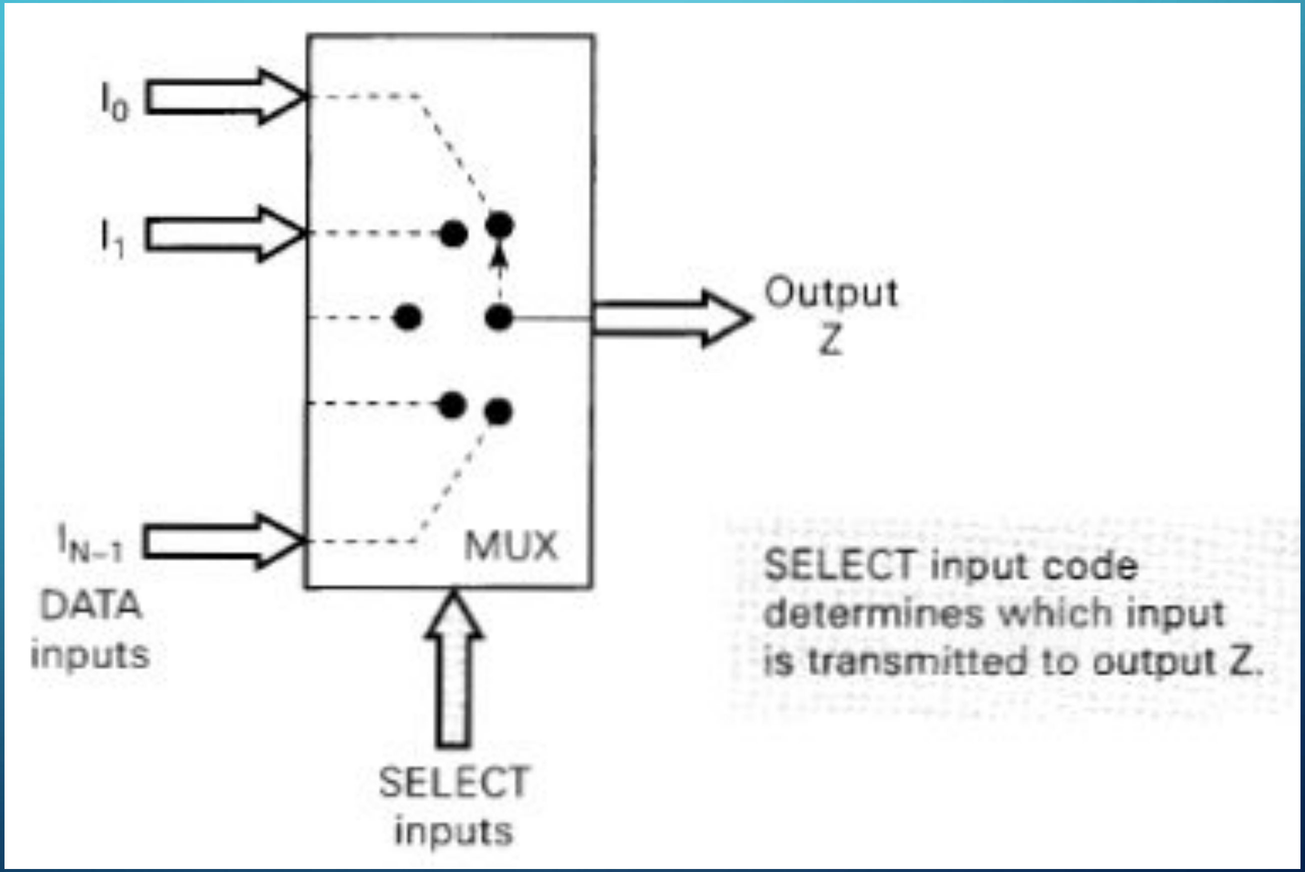
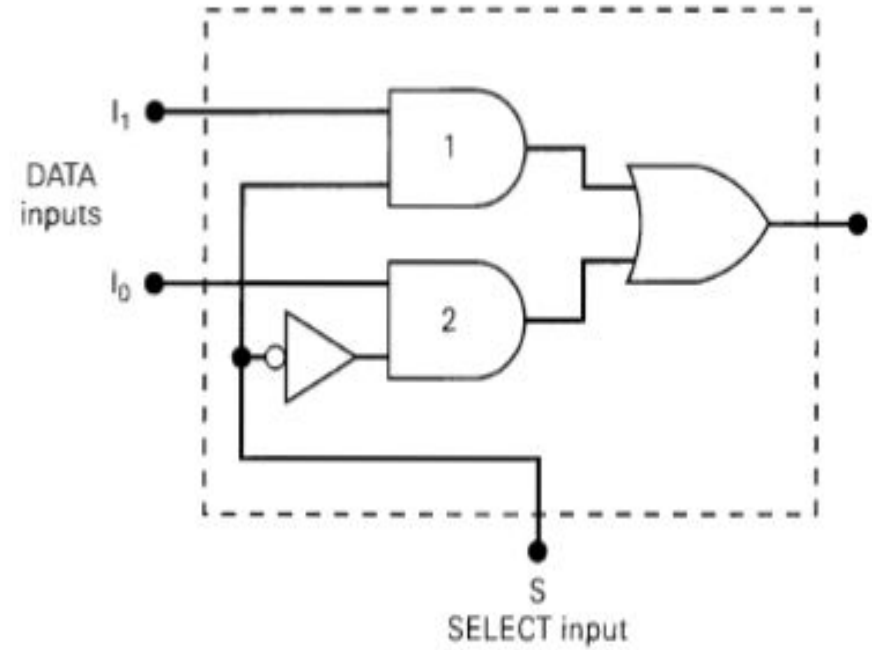


Basic Two-Input Multiplexer

$$Z = I_0\bar{S} + I_1 S$$



S	Output
0	$Z = I_0$
1	$Z = I_1$

With $S = 0$, this expression becomes

$$\begin{aligned} Z &= I_0 \cdot 1 + I_1 \cdot 0 \\ &= I_0 \end{aligned} \quad \text{\{gate 2 enabled\}}$$

With $S = 1$, the expression becomes

$$Z = I_0 \cdot 0 + I_1 \cdot 1 = I_1 \quad \text{\{gate 1 enabled\}}$$

Logic symbol for a 1-of-4 data selector/multiplexer.

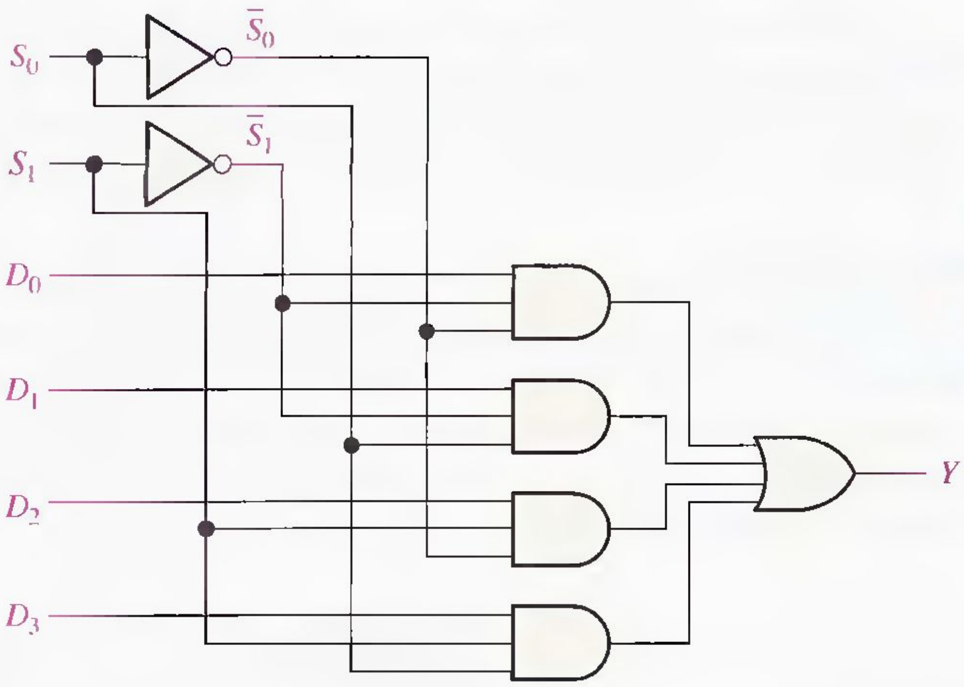
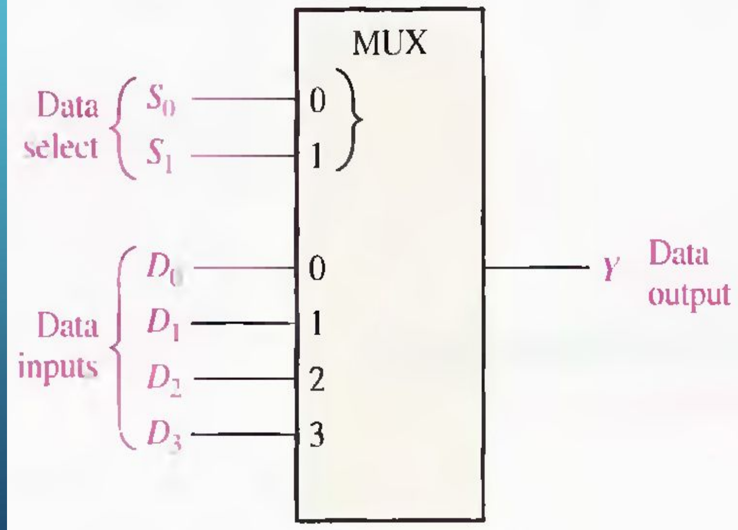


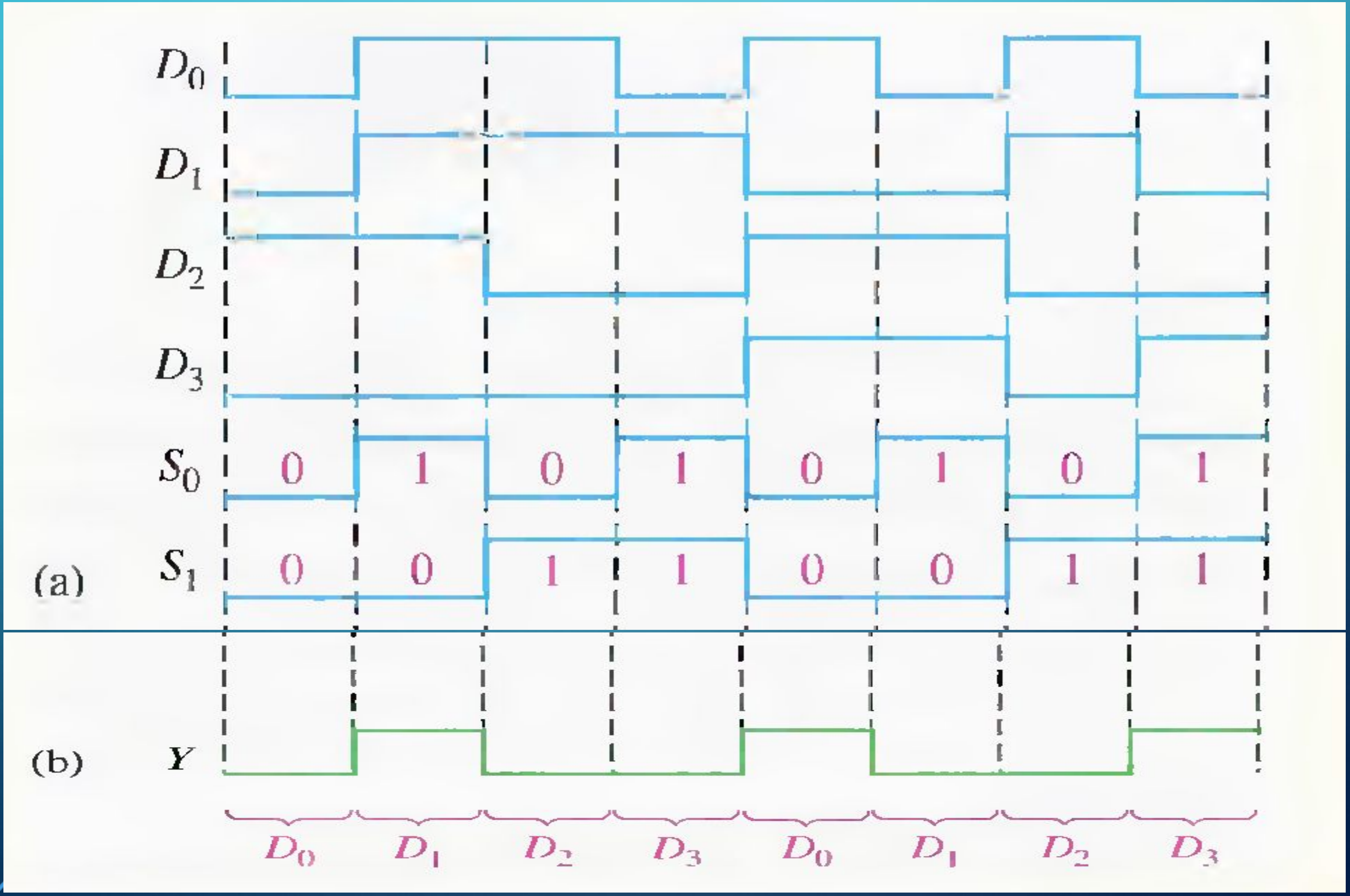
Figure -2

DATA-SELECT INPUTS S_1	S_0	INPUT SELECTED
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



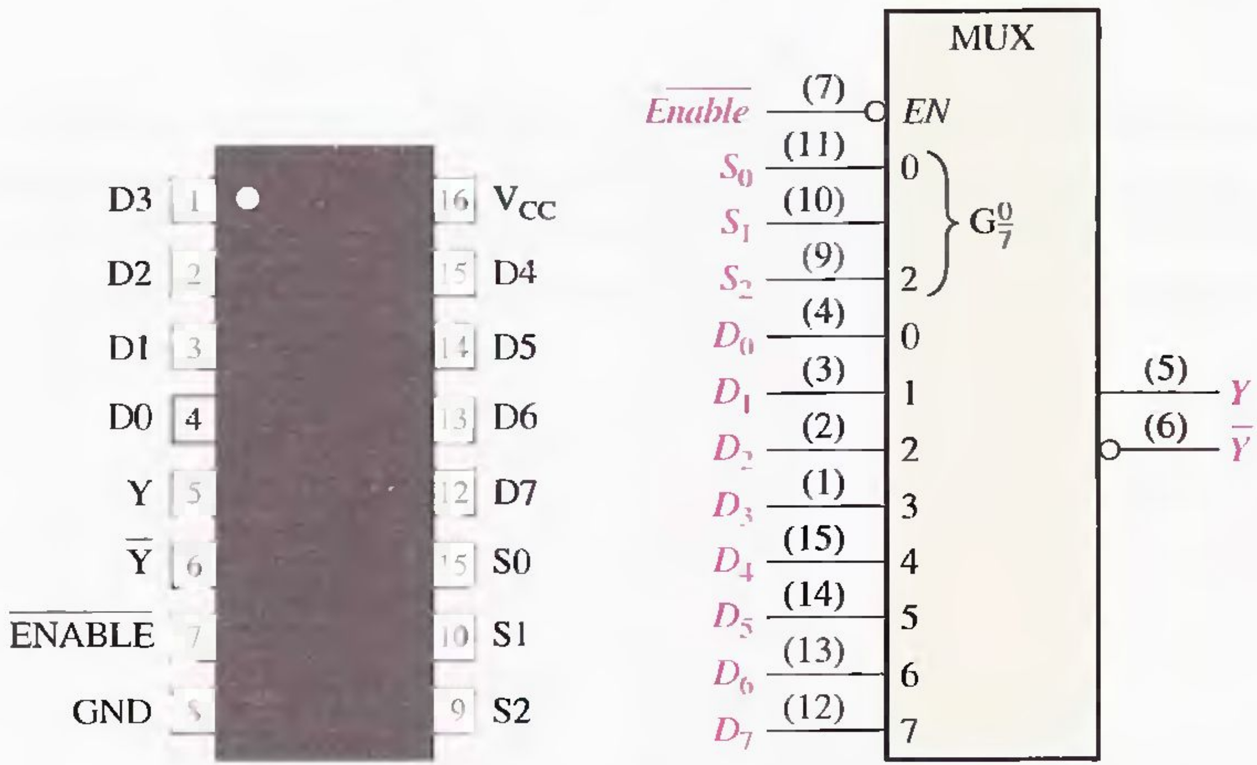
$$Y = D_0\bar{S}_1\bar{S}_0 + D_1\bar{S}_1S_0 + D_2S_1\bar{S}_0 + D_3S_1S_0$$

Example:
The data-input and data-select waveforms in Figure are applied to the multiplexer in Figure -2 . Determine the output waveform in relation to the inputs.



THE 74LS151 8-INPUT DATA SELECTOR/MULTIPLEXER

The 74LS151 has eight data inputs (D_0–D_7) and, therefore, three data-select or address input lines (S_0–S_2). Three bits are required to select any one of the eight data inputs ($2^3 = 8$). A LOW on the $\overline{Enable}$ input allows the selected input data to pass through to the output.

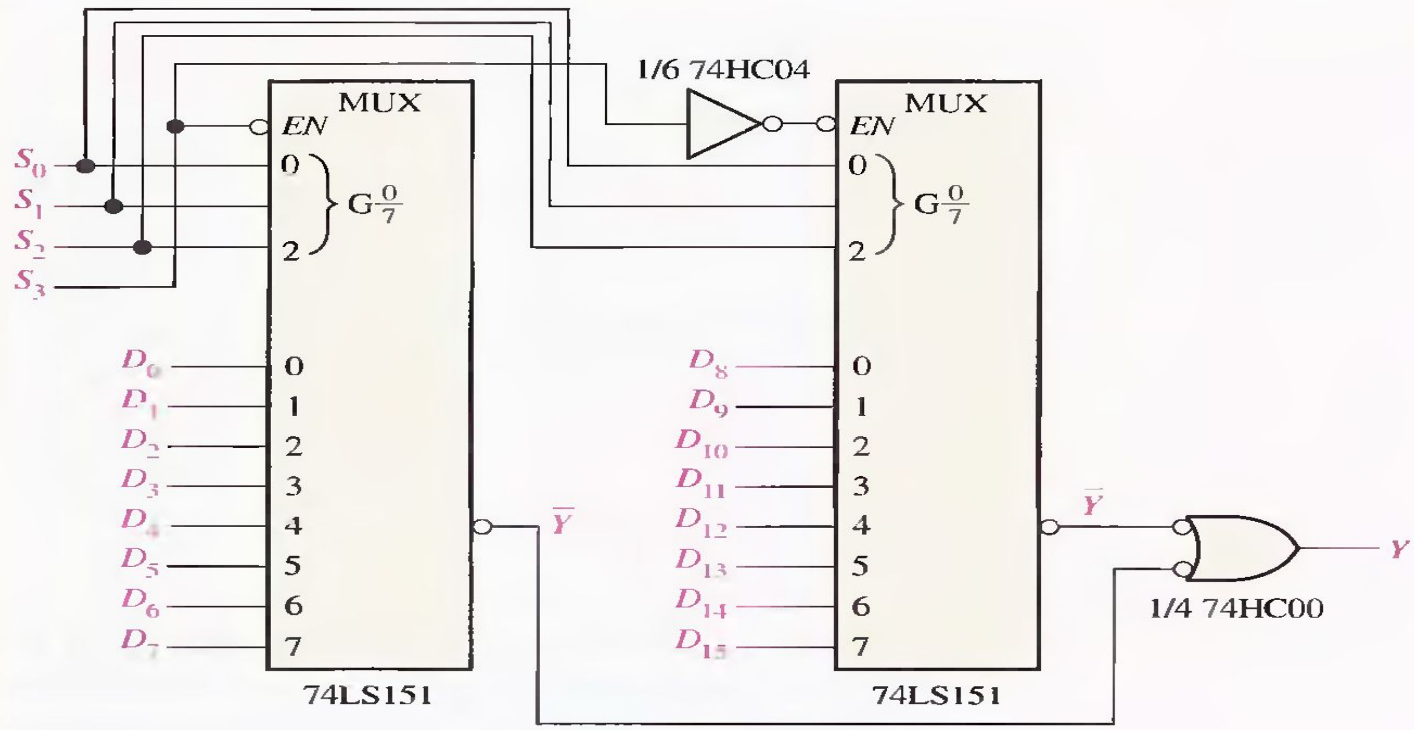


(a) Pin diagram

(b) Logic symbol

Use 74LS151s and any other logic necessary to multiplex 16 data lines onto a single data-output line.

An implementation of this system is shown in Figure 6–51. Four bits are required to select one of 16 data inputs ($2^4 = 16$). In this application the *Enable* input is used as the most significant data-select bit. When the MSB in the data-select code is LOW, the left 74LS151 is enabled, and one of the data inputs (D_0 through D_7) is selected by the other three data-select bits. When the data-select MSB is HIGH, the right 74LS151 is enabled, and one of the data inputs (D_8 through D_{15}) is selected. The selected input data are then passed through to the negative-OR gate and onto the single output line.



Determine the codes on the select inputs required to select each of the following data inputs: D_0, D_4, D_8, and D_{13}.