STM32F100C8xx STM32F100x4 STM32F100x6 STM32F100x8 STM32F100xB
(48p)
16 to 128 Kbytes of Flash memory
4 to 8 Kbytes of SRAM

SMR76.github.io

LQFP48

Left side (pins 1–12):
- 1 VBAT
- 2 PC13 TAMPER-RTC
- 3 PC14 OSC32_IN
- 4 PC15 OSC32_OUT
- 5 OSC_IN | PD0
- 6 OSC_OUT | PD1
- 7 NRST
- 8 VSSA
- 9 VDDA
- 10 PA0 WKUP / USART2_CTS/ADC1_IN0 /TIM2_CH1_ETR
- 11 PA1 USART2_RTS(12)/ADC1_IN1 / TIM2_CH2
- 12 PA2 USART2_TX/ADC1_IN2 /TIM1_BKIN /TIM16_CH1/ TIM2_CH3/TIM15_CH1

Top side (pins 48–37):
- 48 VDD_3
- 47 VSS_3
- 46 PB9 TIM4_CH4 /TIM17_CH1 | I2C1_SDA
- 45 PB8 TIM4_CH3 /TIM16_CH1 / CEC | I2C1_SCL
- 44 BOOT0 | JTDO
- 43 PB7 I2C1_SDA/TIM17_CH1N | TIM4_CH2/ USART1_RX
- 42 PB6 I2C1_SCL/TIM4_CH1 | TIM16_CH1N | USART1_TX
- 41 PB5 I2C1_SMBA / TIM16_BKIN | TIM3_CH2 /SPI1_MOSI
- 40 PB4 NJTRST TIM3_CH1/SPI1_MISO
- 39 PB3 BOOT0 TIM2_CH2 /PB3/TRACESWO/SPI1_SCK
- 38 PA15 JTDI TIM2_CH1_ETR/ PA15/SPI1_NSS
- 37 PA14 JTCK/SWCLK

Right side (pins 36–25):
- 36 VDD_2
- 35 VSS_2
- 34 PA13 JTMS-SWDIO
- 33 PA12 USART1_RTS / TIM1_ETR
- 32 PA11 USART1_CTS / TIM1_CH4
- 31 PA10 USART1_RX /TIM1_CH3 / TIM17_BKIN
- 30 PA9 USART1_TX / TIM1_CH2 / TIM15_BKIN
- 29 PA8 USART1_CK / MCO /TIM1_CH1
- 28 PB15 SPI2_MOSI /TIM1_CH3N /TIM15_CH1N
- 27 PB14 SPI2_MISO/TIM1_CH2N /USART3_RTS
- 26 PB13 SPI2_SCK/TIM1_CH1N | USART3_CTS
- 25 PB12 SPI2_NSS/I2C2_SMBA/TIM1_BKIN/USART3_CK

Bottom side (pins 13–24):
- 13 PA3 USART2_RX/ADC1_IN3 / TIM2_CH4/ TIM15_CH2
- 14 PA4 SPI1_NSS/ADC1_IN4/USART2_CK /DAC1_OUT
- 15 PA5 SPI1_SCK/ADC1_IN5 /DAC2_OUT
- 16 PA6 SPI1_MISO/ADC1_IN6 TIM3_CH1 TIM1_BKIN/TIM16_CH1
- 17 PA7 SPI1_MOSI / ADC1_IN7 / TIM3_CH2 TIM1_CH1N/ TIM17_CH1
- 18 PB0 ADC1_IN8/TIM3_CH3 TIM1_CH2N
- 19 PB1 ADC1_IN9/TIM3_CH4 TIM1_CH3N
- 20 PB2 BOOT1
- 21 PB10 I2C2_SCL / USART3_TX TIM2_CH3 /HDMI_CEC
- 22 PB11 I2C2_SDA / USART3_RX TIM2_CH4
- 23 VSS_1
- 24 VDD_1