DC-DC Resonant Converter

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Abstract: -

Power supplies are electrical circuits which converts a voltage at one level into a voltage at another level. It mainly comprises of a transformer, rectifier, filter, and regulator circuits. Every electronic application needs a supply foremost; or else there is simply no question of its functioning. Thus, power supplies and their evolving designs are always a necessity, and there is constant research into making it more efficient.

DC-DC Power converters are one kind of electrical power converters. It must have a low output impedance and stable voltage source. This project focuses on the Buck (step-down) converter topology.

This project was undertaken to study about resonant converters and the practical considerations in their fabrication, consequently making use of numerous software which are popularly used in the industry today.

Further research in this project could focus upon trying to establish multi-resonance in converters using inductors and capacitors. Also, a different design of the output filter inductor could be attempted.

Outline of Project :-

- Power circuit design as per specifications
- Magnetics – output filter inductor of power circuit
- Gate driver circuit design
- Controller design – closed loop voltage control
- PCB design

Problem Statement:-

Design and fabricate a closed loop 12 V to 5 V resonant buck converter with switching frequency 200 kHz in both zero-current switching and zero-voltage switching topologies.

1) Power Circuit:-

A buck converter is a DC-DC power converter which steps down voltage. It provides much higher power efficiency as compared to linear regulators, which dissipate power as heat but do not step up output current.

MOSFET used – **IRF640N** (Infineon Technologies N-channel MOSFET)

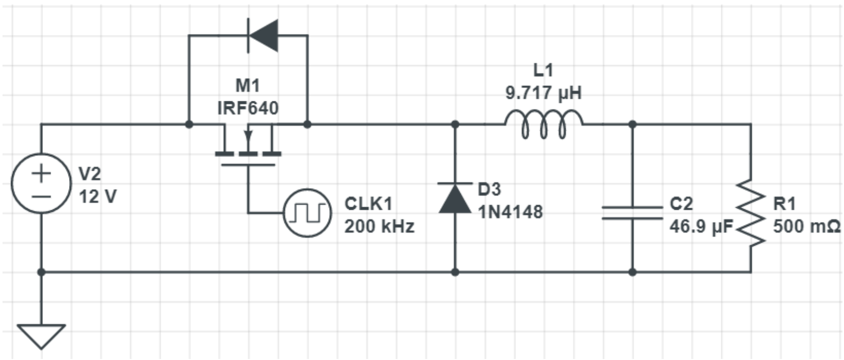


Figure 1:Buck converter power circuit

L1 and C2 form the output low pass filter which blocks the ac components of the switching frequency from reaching the output. Here the switching devices are a combination of a n-channel MOSFET and a diode, which makes a buck chopper specifically.

The following equations can be derived by using Volt-second balance and charge balance:-

- $V_o = V_g*D$
- $P_o = V_o*I_o$
- $\Delta I_l = \frac{(1-D)V_g(D)}{f*L}$
- $\Delta V_c = \frac{D(1-D)V_g}{8f^2LC}$
- $I_{in} = \frac{P_{in}}{V_g}$
- $I_{d,\,avg} = (1-D)*I_o$, Average diode current
- $I_{sw,rms} = \sqrt{D}*I_o$, RMS switch current
- PIV = V_{in}, (Peak Inverse Voltage of diode)

(Allowable capacitor voltage ripple is 1% of V_o)

(Inductor ripple current = 15% of I_o)

V_o= Output voltage
D = Duty cycle
V_g = Input voltage
I_o = Output current
ΔI_l = Inductor ripple current
ΔV_c = Capacitor voltage ripple
f_s = Switching frequency
I_{sw} = Switch current
P_{in}, P_o = Input, Output Power
$I_{sw,rms}$ = RMS Switch current

<u>Calculated Values: -</u>

D = 0.416 P_o = 50 W ΔI_l = 1.5 A ΔVc = 0.12 V I_{in} = 4.16 A

C = 562.6 uF L = 9.717 uH $I_{d,avg}$ = 5.84 A

<u>Simulation Results:-</u>

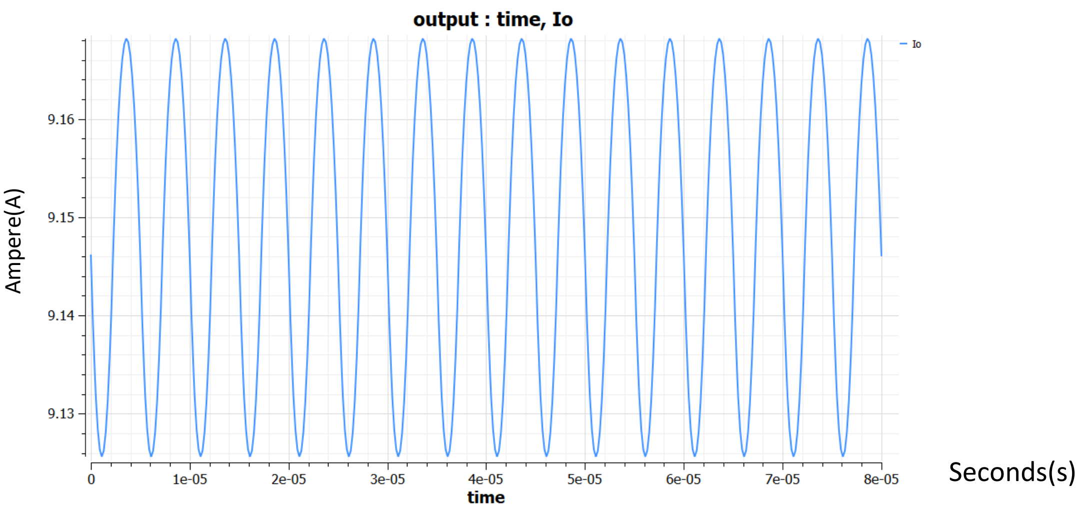


Figure 2:Output current vs time

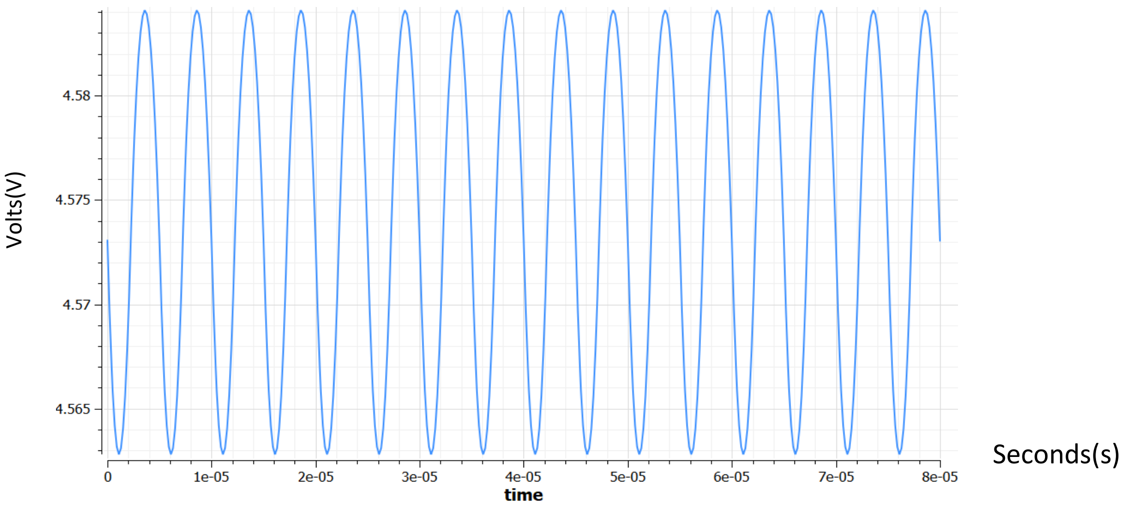


Figure 3:Output Voltage vs time

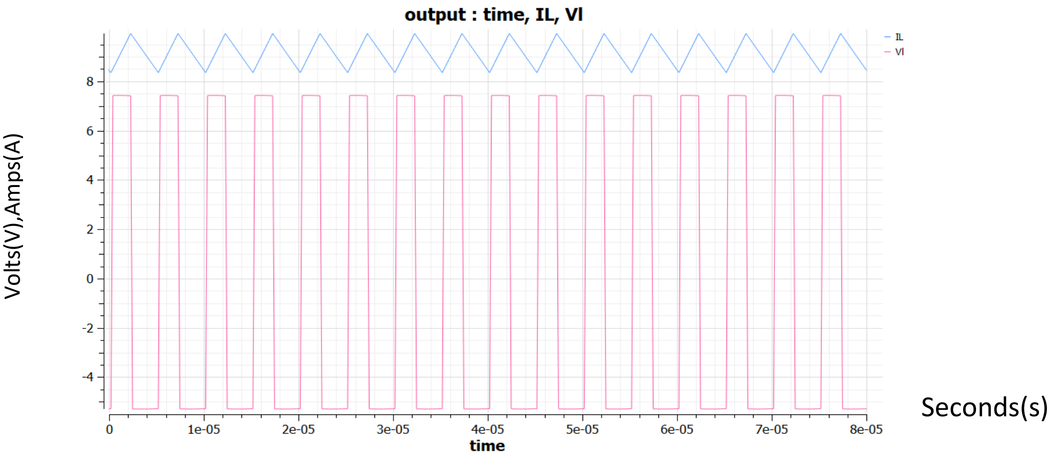


Figure 4:Inductor current, Inductor voltage vs time

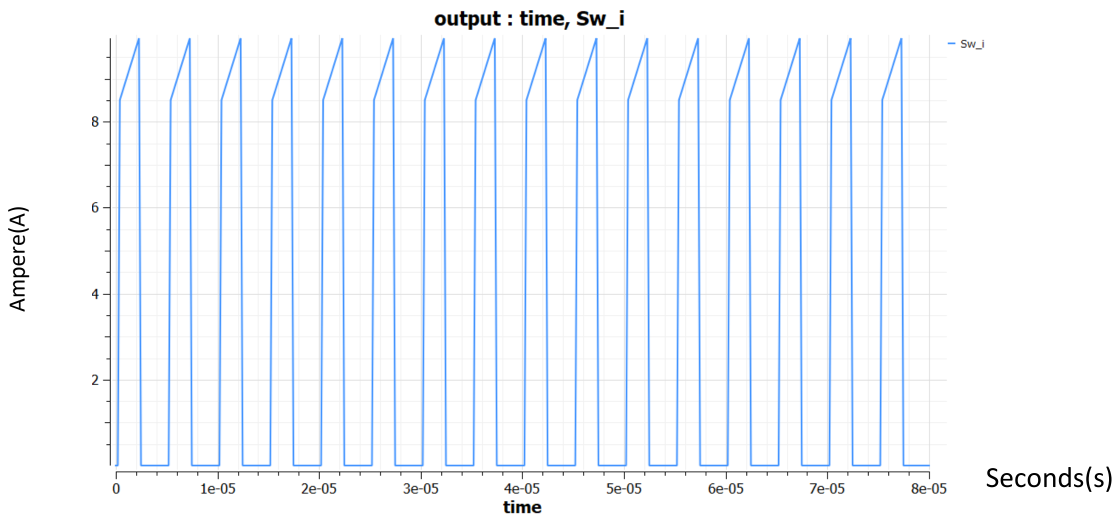


Figure 5:Switch current vs time

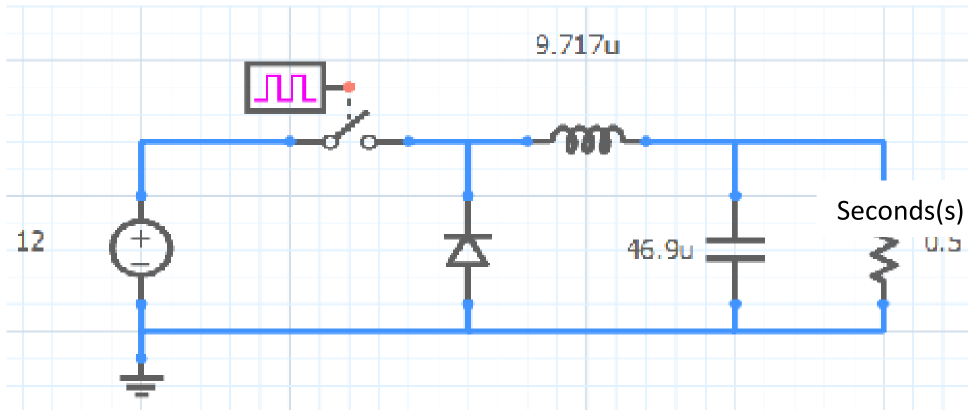


Figure 6:SEQUEL simulation circuit

Magnetics – Output filter inductor design

From the Power circuit equations, we get L = 9.717 uH (12 A). The inductor is designed following [1].

Terms used in the following equations:-

1. Core Reluctance - $\mathcal{R}$ (H^{-1})
2. Current Density – J (A/mm^2)
3. Wire size – a_w (m^2)
4. Effective length of core – l_e (mm)
5. Effective airgap length – l_g (mm)
6. Permeability of free space - μ_o (N/A^2)
7. Relative permeability - μ_r
8. Winding factor – k_w
9. Peak flux density – B_m (T)
10. Core Area – A_c (mm^2)
11. Window Area – A_w (mm^2)
12. Number of turns – N
13. Inductor rms current , peak current – I_{rms} (A), I_p (A)

Core Geometry – **EE core**

- Core Reluctance $(\mathcal{R}) = \frac{l_e}{\mu_o \mu_r A_C}$
- Total Reluctance $(\mathcal{R}_{TOT}) = \frac{l_e}{\mu_o \mu_r A_C} + \frac{l_g}{\mu_0 A_C}$
- Wire size $a_w = \frac{I_{rms}}{J}$ m^2
- $LI = NA_cB_m = N\varphi_p$
- $k_wA_w = Na_w = NI_{rms}/J$
- $k_w = 0.3\text{-}0.5$, $B_m = 0.2$ T, $J = 3$ A/mm^2.
- Required Air gap length = $l_g = \frac{\mu_o N I_p}{B_m}$
- Input L, I_p, I_{rms}, Wire Tables, Core Tables, J, B_m, k_w, f_{sw} (for choosing core material)

Effective core parameters

SYMBOL	PARAMETER	VALUE	UNIT
$\Sigma(I/A)$	core factor (C1)	0.850	mm^{-1}
V_e	effective volume	5590	mm^3
l_e	effective length	69.3	mm
A_e	effective area	80.7	mm^2
A_{min}	minimum area	80.7	mm^2
m	mass of core half	≈ 14	g

Figure 7:Core Parameters [6]

Assumptions:-

1. *No Fringing :* $l_g << \sqrt{A_c}$
2. *Core Reluctance <<Air gap reluctance,* $\frac{l}{\mu_r} = l_g$

Inputs:-

	Inputs			
S.No	Parameters	Symbol	Value	Unit
1	Inductance	L	10	uH
2	Flux Density	B	0.2	T
3	Peak current	I_p	15	A
4	RMS Current	Irms	10.1	A
5	Current Density	J	3	A/mm^2
6	Window Factor	Kw	0.2	

$\mu_0 = 12.57 * 10^{-7}$ Constant

Calculations:-

	Calculations				
	Calculated	Value	Unit		
	Ac * Aw	12625	mm^4		
	aw	3.37	mm^2		
From Core Table	Ac	80.7	mm^2		
	Aw	158.76	mm^2		
	MLT	67	mm		
From Wire Table	aw	3.243	mm^2	SWG	14
	Resistance/km	5.317	Ω/km		
	New Ac*Aw	12811.93	mm^4		

Outputs:-

	Outputs			
S.No	Parameters	Symbol	Value	Unit
1	No.of Turns	N	10	
2	Wire Size	a_w	3.243	mm^2
3	Air Gap (Core)	lg	0.94275	mm
4	Wire Length	L	670	mm
5	Resistance	R	0.0035624	Ω
6	NewCurrent Density	J'	3.1144002	A/mm^2
7	New Window Factor	Kw'	0.204	

<u>Losses in inductor and choosing core material:-</u>

To compute the losses in the Inductor we see that there are two kinds of losses, namely:-

1) Copper Loss, $P_{Cu} = I_{rms}^2 * R_{wire}$
2) Core Loss, P_{core}

R_{wire} is the resistance of wire used in winding the inductor.

$R_{wire} = 5.317\ \Omega/km$ (SWG 14)

As per chosen wires, $P_{Cu} = 0.356$ W.

Calculating AC flux density, we get 10mT, corresponding core loss is negligible.

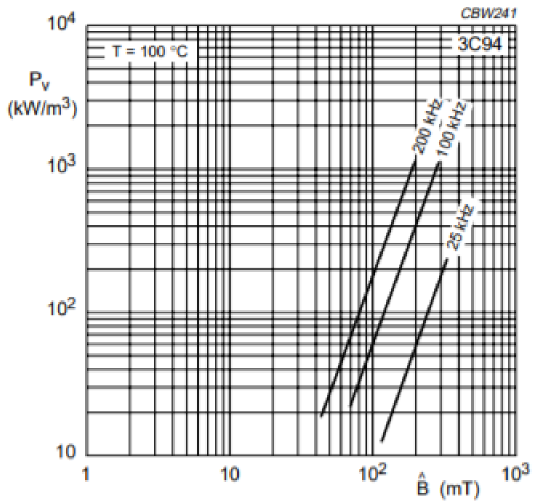


Figure 8:Core Loss[6]

Despite having very low value of AC flux density in the core, an iron core cannot be used here due to high switching frequency of 200 kHz, which would lead to large hysteresis losses.

Core Type – E34/14/9 [7]

Core Material Selected – 3C94 [7]

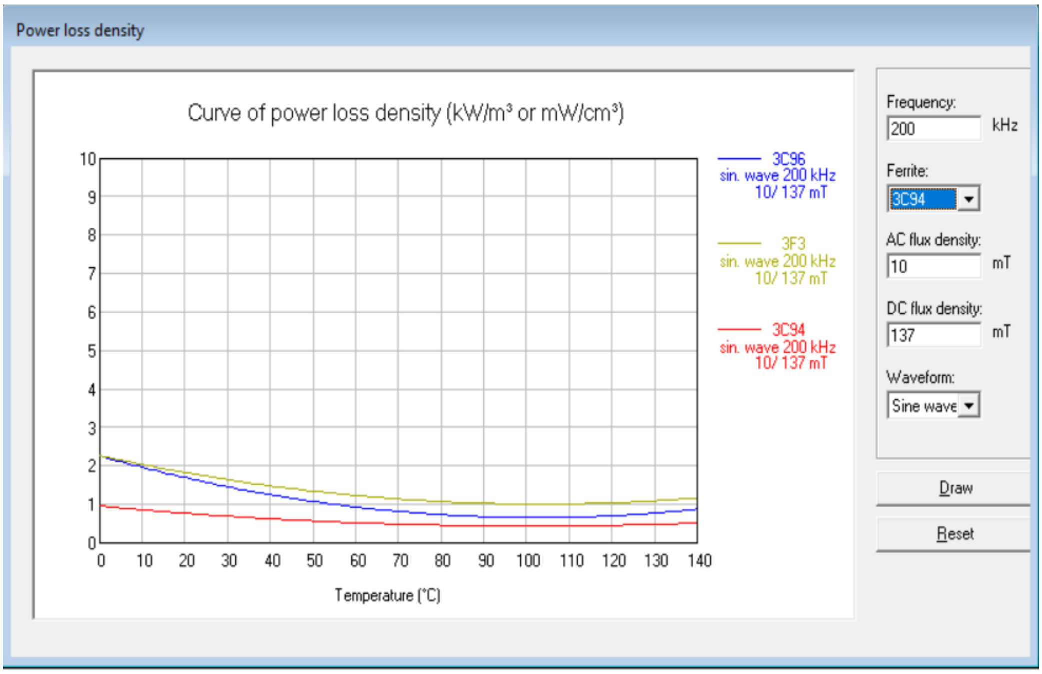


Figure 9: Comparison of Core Material Losses using Ferroxcube SFDT software (B_m = 10mT, f_{sw} = 200kHz) – [8]

Losses and efficiency:-

- Conduction Loss in MOSFET = $I_{sw(rms)}^2 R_{dson}$
- Conduction Loss in Diode = $I_o*V_F*(1-D)$, V_F = forward bias voltage
- Switching loss = $0.5*V_g*I_o*(t_r+t_f)*f_{sw}$, t_r,t_f – rise and fall times
- Inductor Loss = $P_{Cu} + P_{core}$
- Operation loss by IC = $V_g * I_{cc}$ (I_{cc}=1mA, current drawn by IC- SG3524)
- Power Loss in output Capacitor = $I_c^2 * ESR$, (I_c – Capacitor RMS current)

∴ the computed losses are as follows:-

- ❑ The diode loss = 6.45 W (**Dominant**)
- ❑ MOSFET conduction loss = 5.6 W
- ❑ Switching Loss = 0.504 W
- ❑ Inductor Loss = 0.356 W
- ❑ IC operation Loss = 0.012 W
- ❑ Capacitor Loss = 0.01 W

$$\text{Efficiency} = \frac{Output\ Power}{Input\ Power}$$

- Output Power = 50 W
- Input Power = 61 W

$$\boxed{\text{Efficiency} = 81.92\%}$$

Improving the efficiency: -

- Efficiency can be improved by using different MOSFET with lower R_{dson} (i.e < 0.15 Ω)
- Diode loss can be substantially reduced by opting for synchronous buck converter

1.1Closed Loop Control:-

The main objective here is to have a steady DC output of 5V. In order to do this, we use the voltage mode control of the output, so that the duty ratio is adjusted so as to maintain constant output voltage. Frequency domain parameters are used to analyze and design the feedback circuit.

1.1.a Small Signal Analysis :-

We derive the transfer function of the non-ideal buck converter, considering $R_{ds\text{-}on}$ MOSFET on-state resistance, ESR of Capacitor-r_c, ESR of inductor r_l.

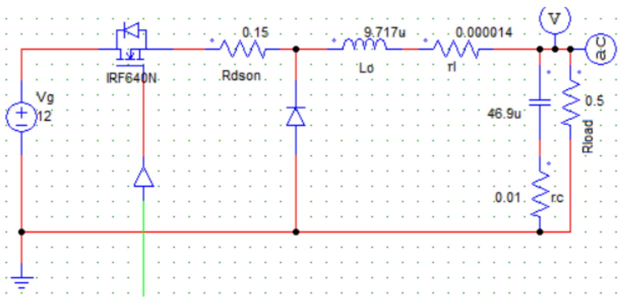


Figure 10:Nonideal buck converter power circuit

r_l = Length of wire * R_{wire} = Number of Turns (N) * Mean Length per turn (MLT) * R_{wire}

r_l = 14 uΩ

IRF640N on-state resistance R_{dson} = 0.15 Ω

r_c = 10 mΩ

Load resistance R >> $r_c + r_l + R_{ds\text{-}on}$

Expression for Duty ratio $\boxed{D_p = \frac{Vo(R+r_l)}{Vo*R_{dson}+R*V_g}}$ ------- Eqn.1

Final Transfer function $\boxed{G_{vd}(s) = \frac{R\left(V_g+Il(-R_{dson})\right)*(1+sC*rc)}{\Delta(s)}}$ where Δ(s) is

$$\Delta(s) = s^2LCR + s[L+RC\{r_c + r_l+D_p(R_{dson})\}+r_cC\{D_p(R_{dson})+r_l\}]+R+D_p(R_{dson}+2*r_l)]$$

--------Eqn.2

Thus, we see that the transfer function is a second-order system with complex pole pair.

Here, $\omega_o = \sqrt[2]{\frac{R+D_p(R_{dson}+2*r_l)}{LCR}})$

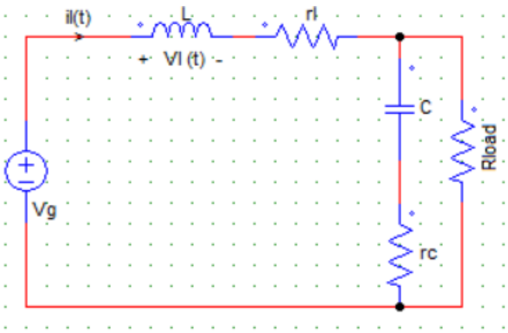


Figure 11:Switch ON state

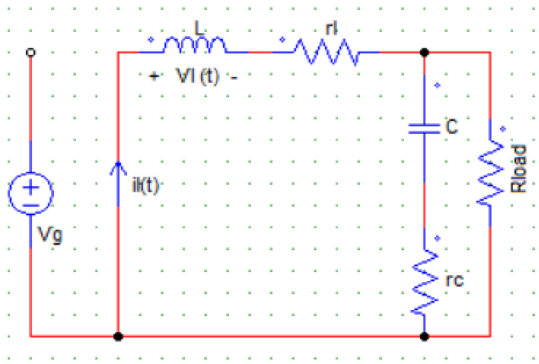


Figure 12:Switch OFF state

Controller design: -

Parameters: Steady state error (<1%), permissible transient overshoot (<5%), settling time.

Following Section 6.2.2 – [1],

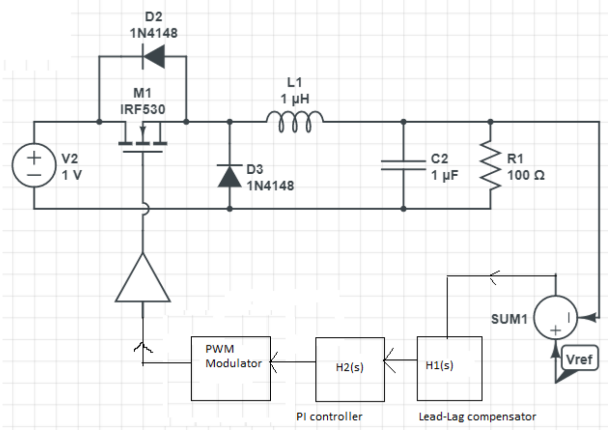


Figure 13:Controller Block diagram

We design the compensator with two blocks cascaded. $H_1(s)$ achieves desired bandwidth and phase margin, $H_2(s)$ reduces the steady state error.

Thus $H_1(s)$ is a lead-lag compensator – $\boxed{H_1(s) = K_1\frac{1+\frac{s}{w_{z1}}}{1+\frac{s}{\omega_{p1}}}}$

$H_2(s)$ is designed so that it does not affect the phase margin and gain margin already designed.

$H_2(s)$ is a PI controller - $\boxed{H_2(s) = \frac{1+\frac{s}{\omega_{z2}}}{\frac{s}{\omega_{z2}}}}$

Overall compensator transfer function is

$$\boxed{H(s) = K_1\frac{1+\frac{s}{w_{z1}}}{1+\frac{s}{\omega_{p1}}}\frac{1+\frac{s}{\omega_{z2}}}{\frac{s}{\omega_{z2}}}}$$

For acceptable transient overshoot, the phase margin must be greater than 45°. Due to the complex pole pair of Gvd(s), $\omega_{z1}=\omega_0$, $\omega_{p1} = 10*\omega_{z1}$. K_1 is adjusted to get required phase margin at the desired crossover freqeuncy. **K_1 = 0.25.**

$$\therefore H1(s)H2(s) = K_1 * \frac{1+\frac{s}{49378}}{1+\frac{s}{493780}} * \frac{1+\frac{s}{5000}}{\frac{s}{5000}} = \frac{5.063*10^{-6}s+0.25}{2.025*10^{-6}s+1} * \frac{0.0002s+1}{0.0002s}$$

Symbols used above: -

1. ω_{z1}, ω_{p1} = Zero, pole of $H_1(s)$ transfer function (Lead -lag compensator)
2. ω_{z2} = Zero of PI Controller $H_2(s)$
3. K_1 = Constant

Results: -

- Final phase margin φ_m = 79.81°
- Gain margin = infinite

- Gain crossover frequency $\omega_c = 2.06*10^4$ rad/s or $f_c = 3278.59$ Hz

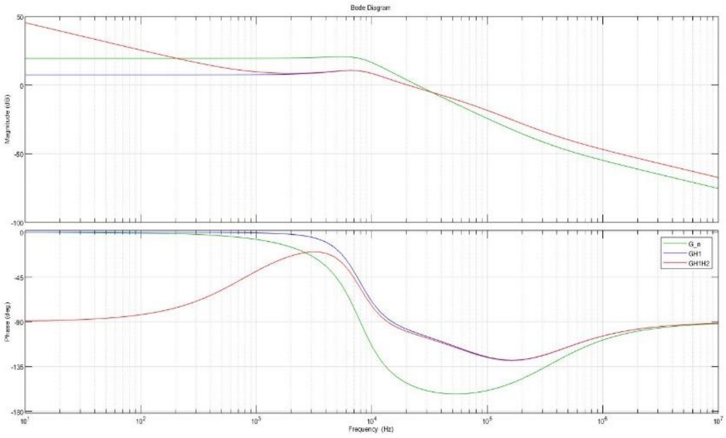
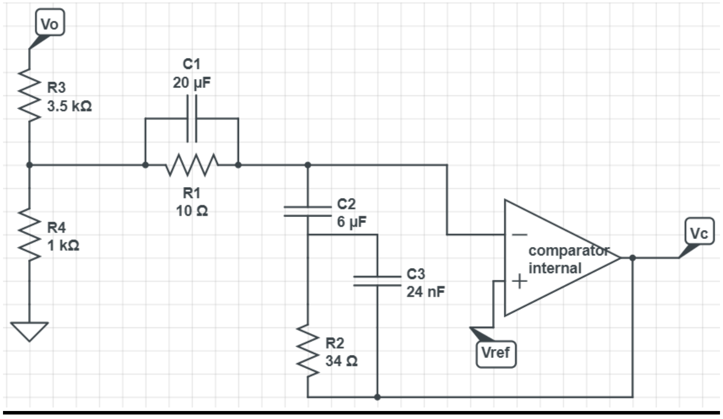


Figure 14: Bode Plot of closed loop buck converter

Circuit components:-



Component	Value
R1	10 Ω
R2	33.3 Ω
R3	3.5 kΩ
R4	1 kΩ
C1	20 uF
C2	6 uF
C3	24 nF

Figure 15: Closed loop control circuit

$Z_2 = (R_2 + \frac{1}{sC_2}) \parallel (\frac{1}{sC_3}) = \frac{1+sR_2C_2}{s(C_2+C_3)(\frac{1+sR_2C_2C_3}{C_3+C2})}$, $Z_1 = R_1 \parallel \frac{1}{sC_1} = \frac{R_1}{1+sR_1C_1}$ ------- Eqn.3

$\omega_{z2} = 1/R_2C_2 = 5000$, $R_2C_2 = 0.0002$ ------- Eqn.4

$\omega_{z1} = 1/R_1C_1 = 49378$, $R_1C_1 = 2.025 * 10^{-5}$ ------- Eqn.5

$V_c = V_{ref}\,(1+\frac{Z_2}{Z_1}) - V_x\,(\frac{Z_2}{Z_1}) = 1.1112$ V , ($V_x = V_{ref} = 3$ V) ------- Eqn.6

$K = \frac{R_4}{3(R_3+R_4)} * \frac{R_2C_2}{R_1(C_2+C_3)}$ ------- Eqn.7

$\omega_{p1} = \frac{C_2+C_3}{R_2*C_2*C_3}$ ------- Eqn.8

Using these above equations, the component values are determined.

Resonant Converter:-

ZCS Converter:-

The closed loop buck converter can now be converted into a resonant converter, first one being Zero-Current Switching type. Gate pulse is high until switch current $i_s(t)$ reverses polarity, at which point, the MOSFET (M) body diode will conduct. Now gate pulse is removed. M will turn off at $i_s(t)$ zero-crossing from negative to positive.

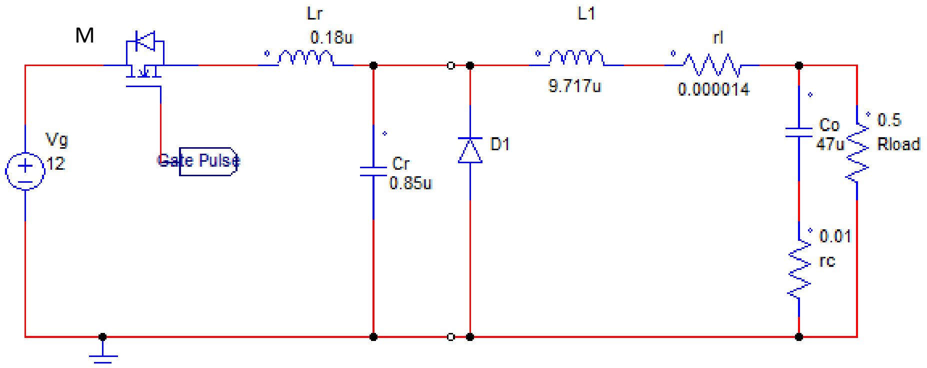


Figure 16: ZCS Buck converter power circuit

Calculations:-

Input: $V_g = 12$ V, $V_o = 5$ V, $I_0 = 10$A, $f_{sw} = 200$ kHz

L_r, C_r are the resonant inductance and capacitance respectively.

Q – Quality factor

$\therefore$ Let $M_f = V_0/V_g = 0.416$

$Q = \omega_o R C_r = R/Z_0$, where $Z_0 = \sqrt{\frac{L_r}{C_r}}$

$M_f = G_f(\sigma)\frac{f_{sw}}{f_o}$ where $G_f(\sigma)$ is practically constant $= 1$.

So conversion factor of the converter can be taken as $M_f = \frac{f_{sw}}{f_o}$.

$$\therefore f_0 = 480.769 \text{ kHz } = 481 \text{ kHz}$$

$\omega_0 = 2\pi f_0 = \sqrt[2]{\frac{L_r}{C_r}} = 3022.21 * 10^3 \text{rad/s}$ $\quad$ $L_r = \frac{Z_O}{\omega_O}$, $C_r = \frac{1}{Z_0\omega_0}$

Let $\sigma = \frac{Io}{Vg} * \sqrt{\frac{L_r}{C_r}}$, a dimensionless parameter. ------- Eqn.9

For successful ZCS switching, source current must have a zero-crossing.

$\therefore i_s(t) = I_o + V_g * \sqrt{\frac{C_r}{L_r}} * \sin(\omega_o t) = 0$

or, $i_s(t) = I_o(1 + \frac{1}{\sigma}\sin(\omega_o t) = 0$ ------- (Using Eqn.9)

$$\therefore I_o \leq V_g * \sqrt{\frac{C_r}{L_r}} \text{ or } \sigma \leq 1$$

Choosing L_r = 0.18 uH (31 A), C_r = 0.9 uF (10 V), we get σ = 0.3762.

Verification by PSIM simulation:-

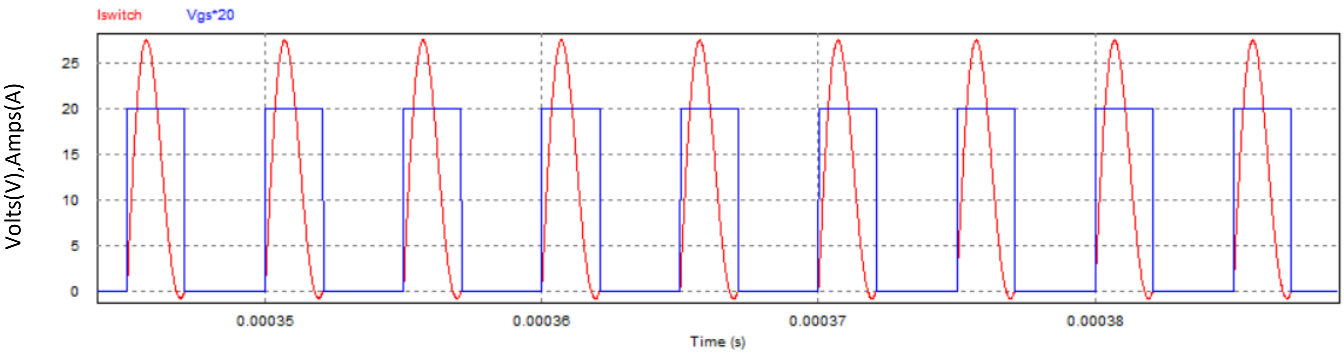


Figure 17: ZCS Switching action (I_{sw}, V_{gs} vs time)

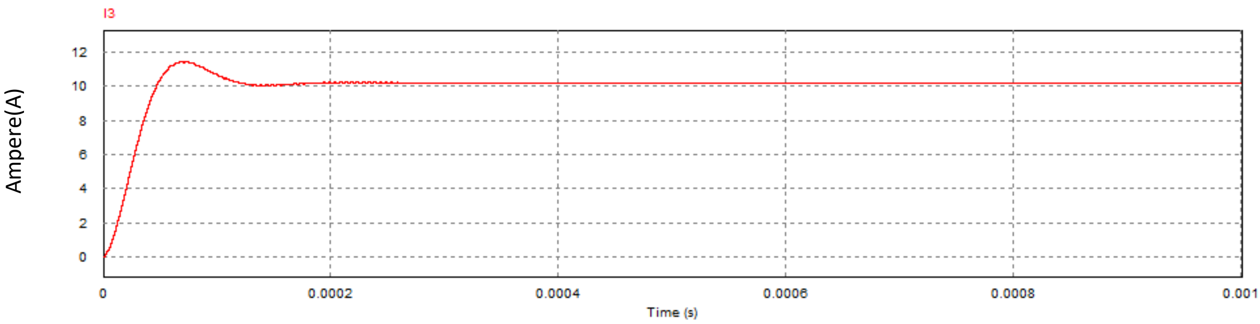


Figure 18: Output current 10A

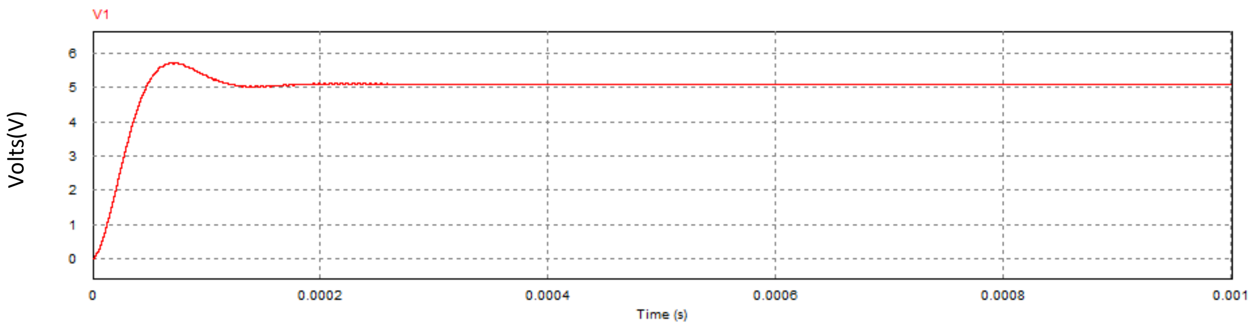


Figure 19: Output Voltage 5V

ZVS (Zero-Voltage Switching): -

The dual of the ZCS type is the ZVS action. Resonance determines the off-time here.

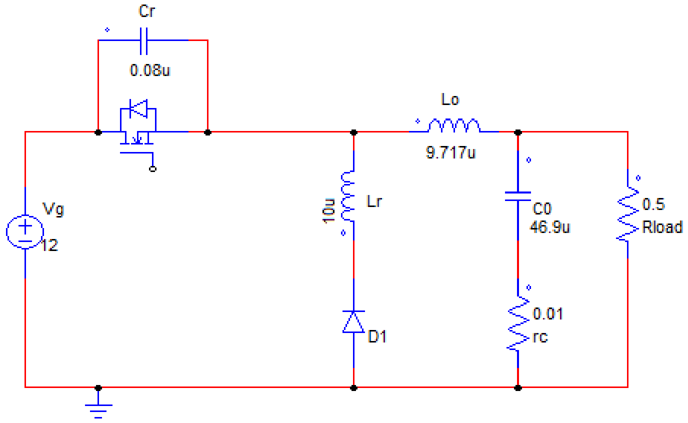


Figure 20: ZVS Buck Converter Power circuit

$V_g - v_t(t) - L_r\frac{di_s}{dt} = 0$ ---- Eqn.10

$v_c(t) = C_r\frac{dv_t}{dt} = i_s + I_o$ ---- Eqn.11

Solving, we get $v_c(t) = V_g + I_o Z_o \sin(\omega_o t)$ ---- Eqn.12

Let $\sigma = \frac{Io}{Vg} * \sqrt{\frac{L_r}{C_r}}$, a dimensionless parameter.

Rewriting Eqn.12, $v_c(t) = V_g\,(1 + \sigma * \sin(\omega_o t))$ ---- Eqn.13

Thus from Eqn.13, it can be seen that for ZVS action, $\sigma \geq 1$.

Choosing L_r = 10 uH (4 A), C_r = 0.08 uF (40 V), we get σ = 9.3169.

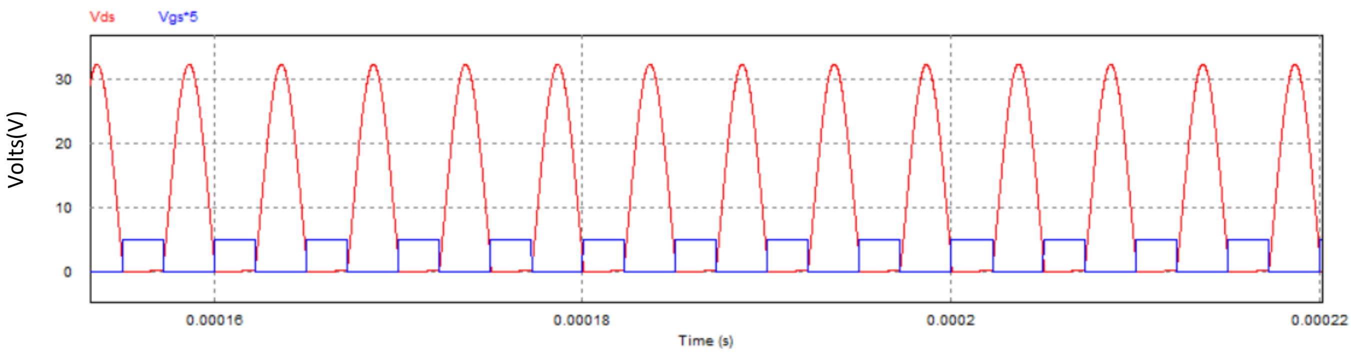


*Figure 21: V_{ds}, V_{gs}*5 vs time, ZVS switching action*

Gate driver - UCC5304DWVR – Texas Instruments

The UCC5304 device is an isolated single-channel gate driver with 4 A peak source and 6 A peak sink current. It has been used here to drive the MOSFET – IRF640N. Using this IC from Texas Instruments obviated providing isolation between the gate driver circuit and power circuit separately with the use of pulse-transformer or optical isolation. Since the input of UCC5304 is isolated from the output drivers, the input signal amplitude can be larger than VDD (within recommended limit).

- Pin 1 is supplied from SG3524 through an inverter.
- Pin 8, VDD, is given +18 V isolated supply.
- Pin 5,6 grounded.
- Pins 2,3 given a +5 V supply using L7805 regulator.

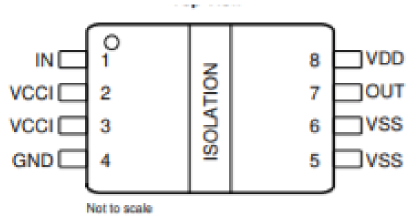


Figure 22: Pin configuration [9]

- Pin 7, OUT pin is fed to the gate terminal of IRF640N through 22 Ω resistors.

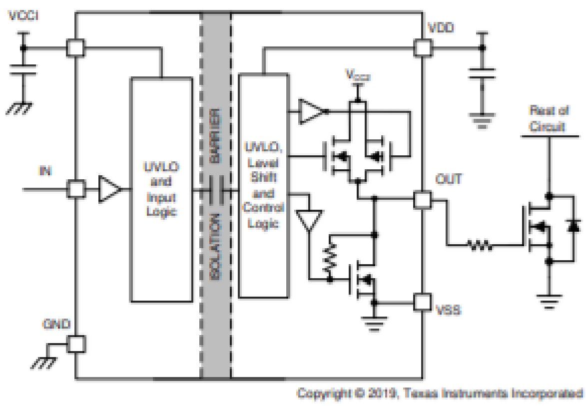
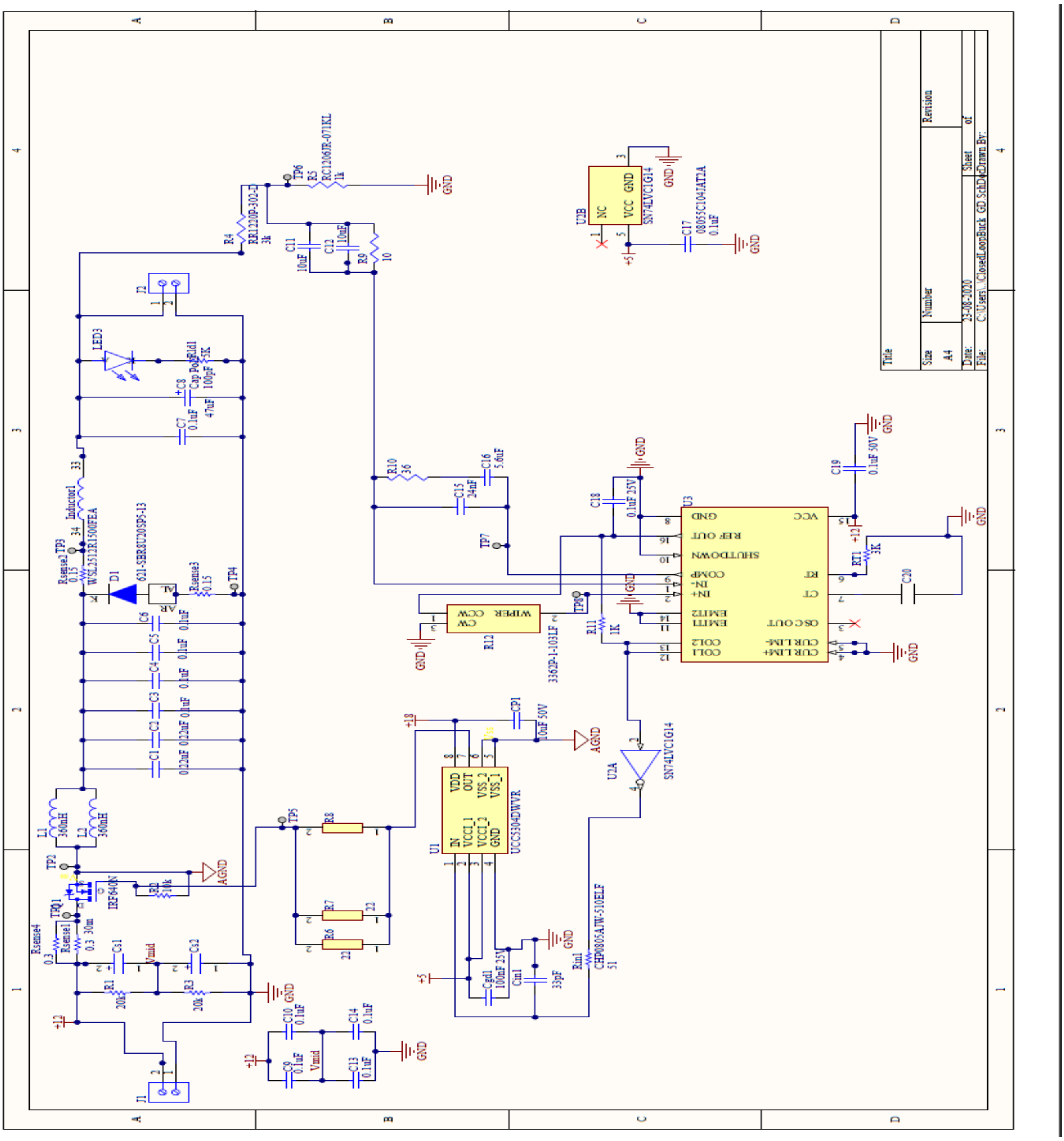


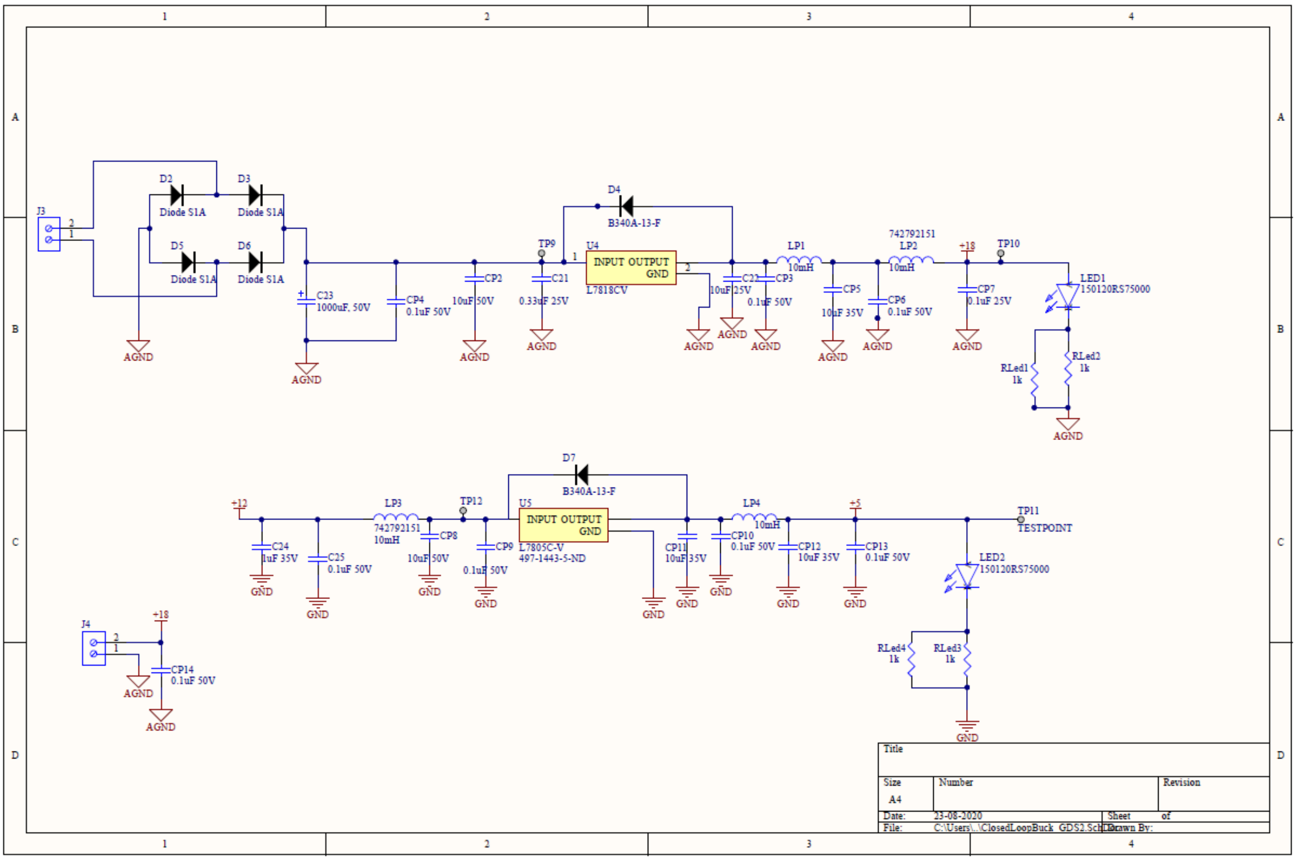
Figure 23: Typical application [9]

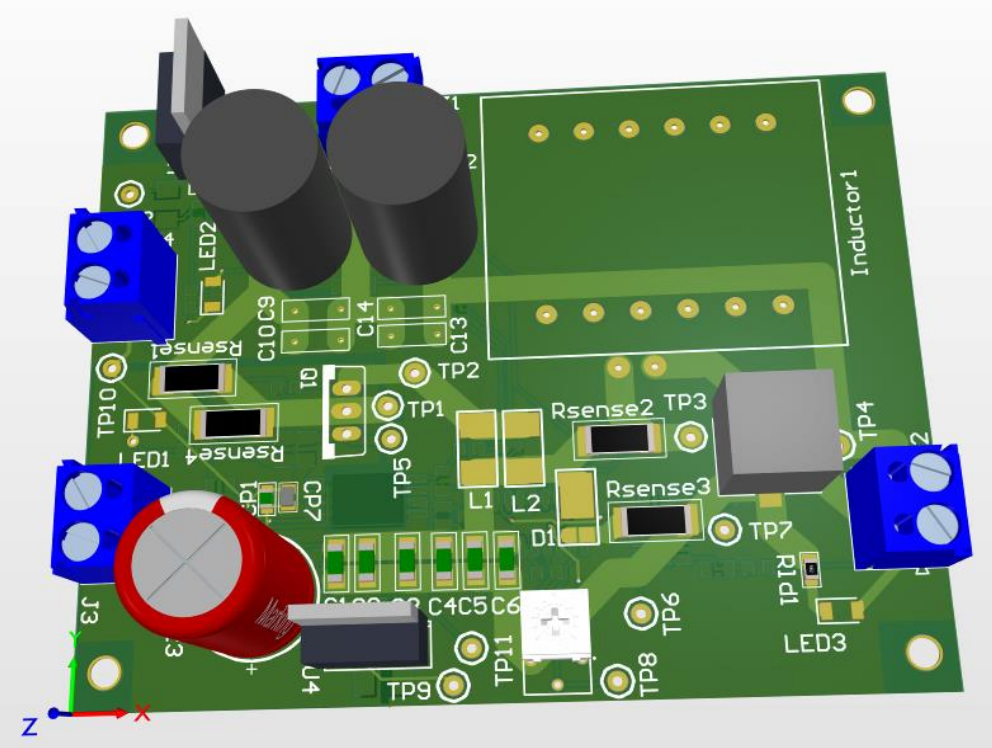
- 50 V, 10 uF MLCC and 50 V, 220 nF MLCC are chosen for C_{VDD} (refer. Figure 23).
- Bypass capacitor connected to pins 2,3 is a 25 V, 100 nF MLCC.
- R_{IN} = 51 Ω, C_{IN} = 33 pF are chosen following recommendations in datasheet. [9]

Altium Schematic:-



Schematic page 2




Inductor1
LED2
Rsense1
C10
C9
C14
C13
TP2
TP10
TP1
Rsense2
TP3
TP4
LED1
Rsense4
TP5
CP7
L1
L2
Rsense3
D1
TP7
J3
C4
C5
C6
TP6
LED3
TP11
TP8
TP9
U4

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[6] Datasheet –

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