Short-Circuit Fault Diagnosis for Three-Phase Inverters based on Voltage Space Patterns

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***Abstract*—This paper introduces a fault detection and isolation (FDI) method for faulty semiconductor switches in a three-phase pulsewidth modulated (PWM) voltage source inverter (VSI). Short-circuit switch faults are the leading cause of failure in power converters. It is extremely vital to detect them in the early stages to prevent unwanted shutdown and catastrophic failures in motor drives and power generation systems. Against the common FDI methods for power electronic inverters that use the phase currents and the PWM Gate control signals, the proposed method uses only the inverter output voltages. This method analyses the PWM switching signals in a time-free domain called voltage space. For a healthy inverter, the projection of the state transitions in the voltage space result in a cubic pattern. Each short-circuit switch fault changes the voltage space pattern (VSP) uniquely that allows isolating the faulty switch. The fault detection time is within only one PWM carrier period that is significantly faster than current-based conventional methods. The FDI result is independent to the load, PWM switching frequency, and feedback loop. This method can address the reliability problem of multilevel inverters in renewable electrical generation systems and can dramatically reduce the number of required sensors.**

***Index Terms*—fault detection and isolation, fault diagnosis, inverter, motor drive, pattern analysis, pulsewidth modulation (PWM), short-circuit fault, state transition, voltage space.**

I. Introduction

RELIABILITY of power electronic inverters is crucial to any advanced electrical system.

Inverters generate ac voltage from a dc power supply, e.g., battery, solar cell, or fuel cell. They are considered as an important part of every electrical energy generation system from small scale appliances to electrical vehicles, aircraft, and high voltage power plants. Inverters are also widely used in motor drive applications to adjust the speed of the motors in industrial rotary machines.

In a VSI, semiconductor switches such as insulated gate bipolar transistors (IGBTs) and metal oxide field effect transistors (MOSFETs) control the frequency and shape of the desired ac voltage. The number of switches depends on the circuit topology. For a two-level three-phase VSI, six IGBTs are used and the number of switches increases in multilevel inverters. These switches can become faulty due to ageing, overloading, or unpredicted operational conditions. Almost 70% [1] of faults in variable-speed drives are related to power switches.

Short-circuit faults, also called as transistor latch-ups, are one of the most common failures in semiconductor switches [2], [3]. When a short-circuit fault occurs, the switch become closed and remains in the on state regardless to the gate control voltage. The first problem occurring after a short-circuit fault is a very high current flowing in the two switches of one phase leg and the dc source, as soon as the other switch of the leg is turned on [4]. These faults can cause severe damages to the battery or the load connected to the inverter.

There exists several FDI methods for detecting switch faults in motor drives and VSIs. These FDI methods necessitate monitoring either phase currents, e.g., [4], [5], [6], [7], phase voltages, e.g., [4], [6], [8], [9], [10], switch gate voltage, e.g., [5], [11], motor torque, e.g., [6], or a combination of these signals. Although placing more detectors can make the FDI algorithm simpler, it adds extra cost and weight to the system. Moreover, it can involve new reliability problems related to the sensors and detector health issues.

Most of the existing FDI methods analyse sinusoidal output of the inverter. Usually, a few cycles of the inverter sinusoidal output are required for the fault detection purpose. It makes the fault detection time in the order of one period of the main sinusoidal waveform (20 ms), e.g., in [7] and [9]. Modern IGBTs (or MOSFETs) can tolerate current values between $2-10$ times the nominal current [4]. However, the switch may be destroyed due to the temperature rise induced by the extremely high instantaneous power dissipated in the switch [4]. Therefore, it is ideal to detect a short-circuit fault within one switching period to prevent short-circuit failures caused by two closed serial switches in one phase leg.

To achieve such a fast result, the FDI algorithm should be based on analysing inverter switching signals instead of the sinusoidal signal. Using switching signals for detecting switch faults is reported in [1] and [12]. However, none of them is applied for short-circuit faults. Moreover, these papers compare the output signals with the gate control signals that require access to the control module.

A model based FDI method for single phase VSIs is proposed in [10]. The monitored output is compared to the model output and the residuals are mapped to the faults through a lookup table. Since this method is highly dependent to the circuit model, tolerances of the components and modeling errors can effect the FDI result and lead to false alarms.

Frequency analysis is a common technique for analysing periodic signals. It is assumed that each fault will lead to a specific sideband frequency [13] or will change the magnitude of some specific harmonics [14], [15]. Therefore, by mapping the frequencies changes to the faults, the diagnosis step is completed. Frequency analysis is widely used to diagnose motor faults by monitoring current signals [16]. Unfortunately, Fast Fourier Transform (FFT) is not suitable for analysing inverter PWM switching waveform. PWM waveform is a nonlinear time dependent signal with a wide frequency band. It is a chain

of pulses with different widths. In practice, the widths of the pulses are affected by the PWM control block, feedback loop, load changes, and operation conditions. Therefore, voltage signal is not a periodic signal in general, and the existing signal analysis methods, e.g. Fourier transform, that is based on the assumption of periodicity of the signal, are not appropriate to analyse it.

This paper proposes an online FDI method based on inverter output PWM voltage signals. In the proposed method, the voltages of each phase are monitored and represented as a point in a three-dimensional voltage space. Then, the patterns are analysed in this time-independent space. It is shown that for an inverter in normal operation, a cubic pattern will be achieved in the voltage space which is independent of load types and output current frequency. Switch faults can change the VSP uniquely. The proposed method is validated on a three-phase VSI, and all short-circuit switch faults are detected and isolate successfully. The number of necessary detectors is reduced to three voltage detectors that can reduce the FDI implementation cost. The fault detection time is successfully limited to only one carrier period.

Section II presents a literature review on FDI for power electronic inverters. Section III describes the three-phase VSI and the PWM control strategy. Section IV introduces voltage space patterns and short-circuit fault banned zones. The VSP-based FDI procedure is described in Section V. The implementation issues and the properties of the VSP-based FDI method are discussed in Section V-E, and the simulation results are shown in Section VI. Section VII concludes the paper.

II. Literature Review

Electrolyte capacitors and semiconductor switches are reported to have the most failure rates in the electronic converters [17], [18], [19], [20]. About 38% of the faults in adjustable-speed drives in the industry are because of failures in power converters [19]. Open-circuit faults generally do not cause shutdown in the VSIs [21]. On the other hand, short-circuit faults can cause an explosion [4] and an expensive down time [8] and must be stopped within a few microseconds [4] by means of a fast FDI method.

In dealing with three-phase power electronic circuits, all three phases may contain information about the faulty component. In order to reduce the feature domain size, and achieve time-independent features, space vector analysis is used. Coordinate transformations [4], [8], [12], [22], [23], [24] such as Park's vector and Concordia has been widely used to convert the 3D current space into 2D space. Pattern recognition methods have been applied to extract fault features from the transformed 2D patterns. Table I compares feature extraction techniques for power electronic inverters. Complexity, speed, and implementation effort of each technique is considered in this comparison. A technique with low computational complexity, high speed and low implementation effort is preferred.

Fault detection and isolation techniques aim to map the features to the faults. Regardless to the feature extraction technique, different methods can be used for fault detection and isolation. The fault detection and isolation techniques which have been applied for VSIs in the literature include limit checking [4], [22], rule-based reasoning [5], Neural Networks [25], Bayesian Networks, and qualitative hybrid Bond Graph (QHBG). Table II compares FDI methods for power electronic inverters. Complexity of the FDI algorithm, accuracy of the result, Robustness to the noise, Robustness to the component's tolerance, and speed of the method are the critical aspects of a FDI algorithm which should be considered.

Feature extraction method	Complexity	Speed	Implementation effort
Parameter estimation	High	Fast	Moderate
Time domain analysis	Low	Fast	Low
Frequency analysis	High	Slow	High
Short Fourier transform	High	Slow	High
Wavelet analysis	High	Slow	High
Space vector analysis	Low	Moderate	Low
Coordinate Transformation	Moderate	Moderate	Low

TABLE I: Comparison of feature extraction techniques.

FDI Method	Algorithm complexity	Accuracy	Robustness	Speed
Limit Checking	Simple	Good	Poor	Good
Rule Based	Moderate	Good	Poor	Moderate
Neural Networks	Complex	Moderate	Good	Low
Bayesian Networks	Complex	Moderate	Good	Low
QHBG	Moderate	Poor	Good	Moderate

TABLE II: Comparison of FDI methods.

The speed of a FDI system is particularly important for fault tolerant control purpose. The faults in electronic devises can propagate very fast and can change to the catastrophic failure within a few microseconds. Table III compares fault detection time of different approaches which have been used in the literature for isolating faulty switches in VSIs. Most of these methods analyse the current signal. Therefore, the diagnosis time is in the order of one period of the current signal. For a 50 Hz inverter this time is around 20 ms. The fastest diagnostic speed is reported in [12] which can diagnose the open-circuit switch fault within $85\mu s$. They monitor the

FDI time	Fault Type	Fault Feature	Requirements	Feature Extraction Method	Fault Diagnosis Method	Comments
> 3s [26]	Open circuit fault	Offset polarity of dc current	-Phase current	dc filtering and limit checking	Expert system (Look-up-table)	-Needs threshold setting. -Detection time depend on low pass filter used in dc current extraction. -Assumes the phase voltages are balanced with the sinusoidal pwm modulation before and after the fault. -Assumes magnetic linearity and infinite rotor inertia.
< 20ms [6]	Open circuit and short circuit faults	Max, Min, Median, Mean, Standard deviation,and dc component of the power spectrum of V, I, and T	-Phase current, -Phase voltage, -Motor torque	Neural networks	Limit checking and rule-based reasoning	-Training -Threshold setting
< 20ms [23]	Open circuit faults	Centroid of the current pattern in $\alpha\ \beta$ plane	Phase current	Concordia Transform	Limit checking and case-based reasoning	-Cannot isolate short-circuit faults -Load dependent -Frequency dependent
≈ 20ms [9]	short circuit faults	RMS value of all phase filtered Voltages	Three phase Voltage	Filtering and RMS calculating	Limit checking and minimisation	-Only can isolate the faulty cell not the faulty switch -Threshold setting
< 20ms [7]	short circuit faults	2^{nd} and e^{rd} harmonic oscillations of phase currents	Three phase current	Filtering ringing frequency	Look-up table	-Fault isolation is dependent to the circuit parameters and need further works -When the number of switches increase, the fault diagnosis become complicated. -The switch faults may not be isolable.
≈ 20ms	Open circuit and short circuit faults	Polarity of phase voltage and entropy of phase Voltage and current	Three phase current, and voltage	Entropy calculation	Neural networks	-Training -Dependent to fault occurrence time -Computational Complexity -Load dependent
≈ 2.2ms [24]	Open circuit faults	Average absolute values of the three normalised phase currents	Three phase current	Coordinate transformation	Look-up table	-Threshold setting -Load dependent
≈ 85μs [12]	Open circuit faults	Average absolute values of the three normalized phase currents	Three phase voltages -Switch control Signals	Coordinate transformation	Parameter estimation	-Requires access to the -Gate control signals -Not scalable to circuit with high number of switches

TABLE III: Comparison of FDI time of different approaches for three-phase VSIs.

Ref.	Fault Type	Fault Feature	Requirements	Feature Extraction Method	Fault Diagnosis Method	Comments
[5]	Open circuit and short circuit faults	Slope of the phase currents, and the input and output voltage value of the gate drive of each switch	-Phase current, -Input/output voltages of Gate drive of each switch -Circuit model	Limit checking	Case-based reasoning	-Not proper for circuits with high number of switches -Threshold setting -Details of the circuit element -Many sensors
[27]	Open circuit faults	RMS value of the wavelet packet decomposition coefficients -2^{nd} harmonic of dc side current	Phase current	Wavelet packet decomposition	Look-up table	-High computational cost -Frequency dependent -Load dependent -Assumption of current balance after fault.
[4]	short circuit faults	Phase of the harmonic at the switching frequency	Three phase current, and voltage	Coordinate Transformation	Limit-checking	-Threshold setting -Dependent to switching frequency -Load dependent
[22]	Open circuit faults	Phase and amplitude of the Concordia current vector	Three phase current	Coordinate Transformation PCA	Limit-checking Look-up table	-Threshold setting -Load dependent
[8]	Short circuit faults	Sector of space vector frequency	Three phase voltage	Coordinate transformation	Look-up table	-Threshold setting -Cannot isolate the faulty switch

TABLE IV: Comparison of FDI approaches for three-phase VSIs.

switching voltage which has a higher frequency. Thus, the diagnosis speed is much more higher than the methods based on the current waveform. However, they need to monitor three normalised phase currents voltages as well as switch control signals.

Thus, access to the gate control signals is needed in this diagnostic method. Moreover, the number of sensors increase rapidly for more complex inverters.

Table IV summarises the combination of feature extraction and FDI methods which have been used in the literature for diagnosis switch faults in three-phase VSIs. The methods are mainly appropriate to isolate either open-circuit faults [22], [27], [28] or short-circuit faults [4], [8]. The methods which are based on analysing current signal, e.g. [4] ,[22], [27], and [29], are load dependent. Thus, changing the load can increase the false alarm rate of the diagnostic system.

In many situations, the load is not constant and can be changed by user or by environment conditions during the operation. Thus, the current waveform will be changed regarding to the load type and value. Therefore, the fault detection algorithm which are based on the analysis of the sinusoidal current waveform may lead to false alarm when the load changes. Moreover, the fault detection time depends on the time constant of the load [30]. Although the sinusoidal signal is easier than the PWM switching signal to be analysed, it has some disadvantages for FDI purpose. Filtering the switching signal can eliminate some useful information about switch faults. It can also make some delays. Moreover, the faults can be mistaken by fluctuations of the load or filter parameters. Therefore, for diagnosis switch faults, it is recommended to monitor and analyse switching signals instead of the sinusoidal signals.

Limit checking and case based reasoning is still the most common diagnosis method which needs threshold setting and cannot be extended to unknown faults in more complex systems.

III. Three-Phase Voltage Source Inverter

Figure 1 illustrates a VSI circuit with six identical switches, Q_i for $i = 1$ to 6. Gate control signals g_i, control on–off state of Q_i; for $g_i = 1$, Q_i is in the on state and the switch conducts. On the other hand, when $g_i = 0$, Q_i is in the off state, and it does not conduct. Gate signals of two switches of one phase leg are complementary; for example, if $g_1 = 1$ then $g_2 = 0$ and Q_1 is closed, resulting in $v_A = +E_N$; conversely, if $g_1 = 0$ then $g_2 = 1$ and Q_2 is closed, resulting in $v_A = -E_N$, where E_N is a constant value proportional to the voltage of the dc source. Hence, the output voltage of each phase alternates regularly between two levels of voltage that forms a square wave. A control block determines the pulsewidth of the waveform. Sinusoidal pulsewidth modulation (SPWM) is a common technique to control the gate signals such that a sinusoidal output is obtained after filtering the square waveform.

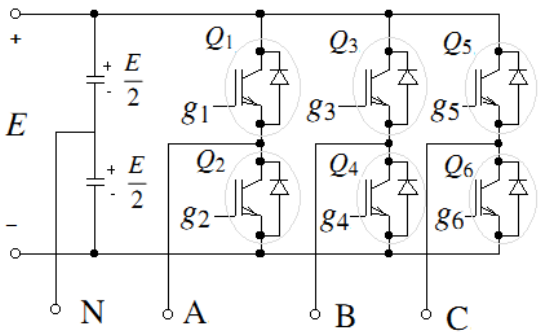


Fig. 1: A Three-phase inverter.

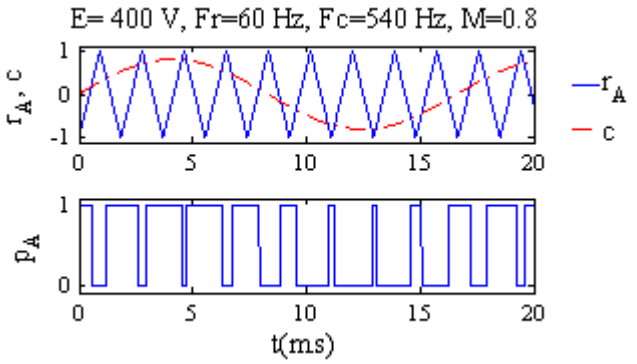


Fig. 2: Generating SPWM Signal.

A. Sinusoidal Pulse Width Modulation (SPWM)

SPWM is one of the most common modulation methods introduced by Schoänung in 1964 [31]. The control block generates SPWM pulses $p_\varphi(t)$, by comparing a triangular carrier waveform $c(t)$, to a reference modulating signal, $r_\varphi(t)$.

$$p_\varphi(t) := \begin{cases} 1, & r_\varphi(t) \geq c(t) \\ 0, & r_\varphi(t) < c(t) \end{cases} \tag{1}$$

$$r_\varphi(t) := A_r sin(2\pi F_r t + \phi_\varphi), \qquad \text{for } \varphi = A, B, C \tag{2}$$

A_r, and F_r are the amplitude and frequency of the reference signal. The displacement angle between reference and carrier signals $\phi = 0, -\frac{2\pi}{3}, \frac{2\pi}{3}$ for $\varphi = \mathrm{A}, \mathrm{B}, \mathrm{C}$ respectively. The carrier signal, with amplitude A_c and frequency F_c, is defined

$$c(t) := \begin{cases} 4A_c(F_c t - k - \frac{1}{4}), & \text{if } kT_c \leq t < (k+\frac{1}{2})T_c \\ -4A_c(F_c t - k - \frac{3}{4}), & \text{if } (k+\frac{1}{2})T_c \leq t < (k+1)T_c \end{cases}$$

$$\text{where } k = \lfloor \frac{t}{T_c} \rfloor. \tag{3}$$

T_c and T_r are the periods of $c(t)$ and $r_\varphi(t)$ respectively. N is the frequency–modulation ratio which is chosen as a multiple integer of 3 to ensure elimination of the dominant harmonics and perfect symmetry in the three phase outputs [32], [33].

$$N := \frac{F_c}{F_r} = \frac{T_r}{T_c} = 3m_1, \qquad m_1 \in \mathbb{N}^+$$

The amplitude–modulation ratio or the modulation index M is less than one for the power electronic applications when the over–modulation is avoided.

$$M := \frac{A_r}{A_c} \qquad 0 < M < 1 \tag{4}$$

Figure 2 illustrates the concept of SPWM modulation. In this figure, $M = 0.8$ and $F_r = 60$Hz are chosen as the typical power inverter application. Typically F_c in the 1 to 20 kHz range are applied [9]; however, in this figure, F_c is reduced to 540 Hz for better illustration purpose. Figure 3 depicts the six gate control signals generated from the SPWM signal of Fig. 2 where

$$\begin{aligned} g_1(t) &:= p_\mathrm{A}(t) & g_2(t) &:= 1 - g_1(t) \\ g_3(t) &:= p_\mathrm{B}(t) & g_4(t) &:= 1 - g_3(t) \\ g_5(t) &:= p_\mathrm{C}(t) & g_6(t) &:= 1 - g_5(t) \end{aligned} \tag{5}$$

The resulting phase voltages $\mathrm{v_A}$, $\mathrm{v_B}$, and $\mathrm{v_C}$ are shown in Fig. 4 for a healthy inverter.

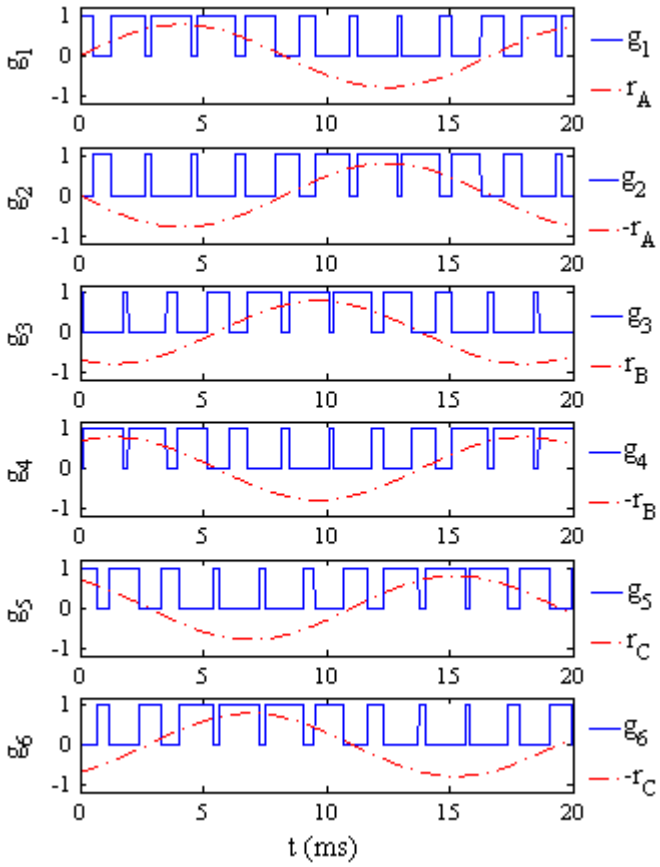


Fig. 3: Gate control signals.

B. Inverter Modeling

This section describes a structural model for the three-phase VSI. Assume R_u is the internal resistance of an upper switch of a phase leg, e.g., Q_1 for $\varphi = \mathrm{A}$, and R_l is the internal resistance of the lower switch of that phase leg, i.e. Q_2 in this example. From the circuit equations,

$$\mathrm{v}_\varphi = \frac{E}{2} \cdot \frac{R_l - R_u}{R_l + R_u} = \frac{E}{2} \cdot \frac{1 - \frac{R_u}{R_l}}{1 + \frac{R_u}{R_l}} \tag{6}$$

Let R_{on}, and R_{off} be the internal resistance of a healthy switch in the on and off states.

$$\rho_0 := \frac{R_{\text{on}}}{R_{\text{off}}}. \tag{7}$$

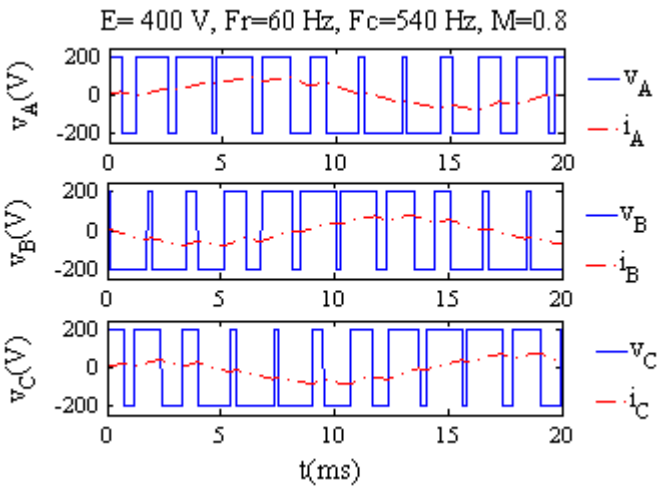


Fig. 4: Current and voltage waveforms in the no-fault situation.

Thus, the internal resistance of a switch R_i is equal to R_{on}, when $g_i = 1$; conversely, $R_i = R_{\text{off}}$ when $g_i = 0$.

$$\frac{R_u}{R_l} = \begin{cases} \rho_0, & \text{if } g_u = 1 \text{ and } g_l = 0 \\ \dfrac{1}{\rho_0}, & \text{if } g_u = 0 \text{ and } g_l = 1 \end{cases} \tag{8}$$

Replacing $\frac{R_u}{R_l}$ from (8) in (6)

$$\mathrm{v}_\varphi = \begin{cases} \frac{E}{2}\epsilon_0, & g_u = 1 \text{ and } g_l = 0 \\ -\frac{E}{2}\epsilon_0, & g_u = 0 \text{ and } g_l = 1 \end{cases} \tag{9}$$

where

$$\epsilon_0 := \frac{1-\rho_0}{1+\rho_0} \tag{10}$$

For a healthy switch, $R_{\text{on}} << R_{\text{off}}$; thus, $\rho_0 \approx 0$, and $\epsilon_0 \approx 1$. Let $E_N = \frac{E}{2}\epsilon_0$ be the absolute value of the phase voltage for the inverter in the no-fault condition. Thus,

$$\mathbf{v}(t) := \mathbf{e} \cdot \mathbf{D}(t) \tag{11}$$

where $\mathbf{v}(t) = [\mathrm{v_C}(t), \mathrm{v_B}(t), \mathrm{v_A}(t)]$, $\mathbf{e} = [E_N, -E_N]$, and

$$\mathbf{D}(t) := \begin{bmatrix} d_1(t) & d_3(t) & d_5(t) \\ d_2(t) & d_4(t) & d_6(t) \end{bmatrix} \tag{12}$$

is a binary matrix representing the dynamic model of the inverter

$$d_i(t) := \begin{cases} 1 & \text{if } Q_i \text{ is on at time t,} \\ 0 & \text{if } Q_i \text{ is off at time t.} \end{cases} \tag{13}$$

Eight switching states are possible based on different combinations of the gate control signals.

$$\forall t \qquad \mathbf{D}(t) \in \mathbb{D}, \tag{14}$$

where $\mathbb{D}$ is the set of all eight normal switch combinations $\mathbb{D} = \{\mathbf{D}_s : \forall s \in \mathbb{S}\}$, and $\mathbb{S}$ is the set of eight states $\mathbb{S} = \{0, 1, \ldots, 7\}$. Table V shows $\mathbf{D}_s$ for all eight possible switching states.

s	$\mathbf{D}_s$	$\mathbf{v}_s$
0	$\begin{bmatrix} 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}$	$[-E_N \quad -E_N \quad -E_N]$
1	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$[-E_N \quad -E_N \quad E_N]$
2	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}$	$[-E_N \quad E_N \quad -E_N]$
3	$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}$	$[-E_N \quad E_N \quad E_N]$
4	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}$	$[E_N \quad -E_N \quad -E_N]$
5	$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$	$[E_N \quad -E_N \quad E_N]$
6	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$	$[E_N \quad E_N \quad -E_N]$
7	$\begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix}$	$[E_N \quad E_N \quad E_N]$

TABLE V: Switching states and output phase voltages.

The switching state of the inverter at a given time t is

$$s(t) := \mathbf{u} \cdot \mathbf{b} \tag{15}$$

where $\mathbf{b} := [4\ 2\ 1]^T$ and $\mathbf{u} := [1\ 0] \cdot \mathbf{D}(t)$. In the other word, s is the decimal value of the first row of $\mathbf{D}$. By this definition, (15) assigns a unique number for each switching state of the inverter.

Proposition 1. *For every $\iota, \kappa \in \mathbb{S}$ and $\iota \neq \kappa$, $\mathbf{D}_\iota \neq \mathbf{D}_\kappa$.*

Proof: From (13) and (5),

$$\mathbf{D}(t) = \begin{bmatrix} p_{\mathrm{C}}(t) & p_{\mathrm{B}}(t) & p_{\mathrm{A}}(t) \\ 1-p_{\mathrm{C}}(t) & 1-p_{\mathrm{B}}(t) & 1-p_{\mathrm{A}}(t) \end{bmatrix} \tag{16}$$

and

$$\mathbf{u}(t) = [1\ 0] \cdot \mathbf{D} = [p_{\mathrm{C}}(t), p_{\mathrm{B}}(t), p_{\mathrm{A}}(t)].$$

Equation 15 gives the binary to decimal conversion of $\mathbf{u}$. Thus, there exists a one-to-one correspondence between s and $\mathbf{u}$. On the other hand, from (16) $\mathbf{u}$ uniquely defines $\mathbf{D}$ for a healthy inverter. Therefore, the switch combination of the inverter $\mathbf{D}$ can be represented uniquely by s for each switching state. Given the switching state s the switch combination $\mathbf{D}$ can be determined from (16) with $p_{\mathrm{A}}(t)$, $p_{\mathrm{B}}(t)$, and $p_{\mathrm{C}}(t)$ being the first, second, and third digits of a binary number equal to s(t), i.e., $p_{\mathrm{A}}(t) = s(t) \mod 2$, $p_{\mathrm{B}}(t) = \lfloor \frac{s(t) \mod 4}{2} \rfloor$, and $p_{\mathrm{C}}(t) = \lfloor \frac{s(t)}{4} \rfloor$. ■

IV. State transition patterns in voltage space

Assume a voltage space consisting of $\mathrm{v_A}(t)$, $\mathrm{v_B}(t)$, and $\mathrm{v_C}(t)$ as its axes and a cube centred at the origin with the side length of $2E_N$ (Fig. 5). The switching states from Table V can be mapped to the vertices of this cube in the voltage space.

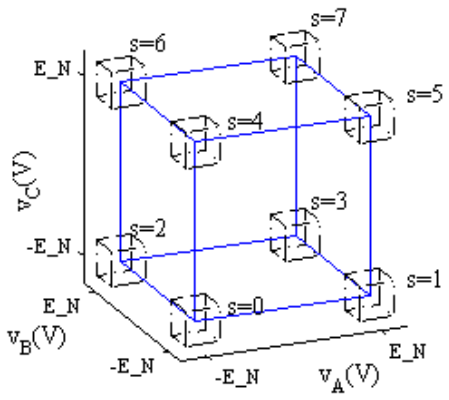


Fig. 5: Voltage space and the eight normal switching states.

A. State Transition patterns

In this section, the state transition patterns in the voltage space are introduced. Assume the phase voltages are monitored for $t \le t_0$ and the switching states are extracted. Equation (17) defines a sequence of nonequivalent adjacent switching states X observed for $t \le t_0$

$$X(t_0) = \langle s(t_0), s(t_1), s(t_2), \dots, s(t_n), \dots \rangle, \qquad \text{for } n \in \mathbb{N} \tag{17}$$

where $t_0 > t_1 > t_2 > \cdots > t_n > \dots$ and t_n is every time instance at which the value of the switching state changes, i.e,

$$s(t_n) \neq s(t_n^-).$$

where t^- is a time instance very near to t but less than it.

Whenever two adjacent switching states are non-equal, a transition occurs. A transition is shown by a line in the voltage space. In the following propositions, it is proven that the transitions occur at the edges of the cube (rather than its diagonals); Proposition (2) shows that the switching state s changes whenever one of the PWM signals of a phase leg varies, and Proposition 3 proves that the phase changes occur at different time instances within one carrier period (T_c).

Proposition 2. *Assume the value of p_A, p_B, and p_C changes at $t = \alpha$, $t = \beta$, and $t = \gamma$ respectively.*

$$p_\varphi(t_n) \neq p_\varphi(t_n^-) \Leftrightarrow s(t_n) \neq s(t_n^-).$$

Proof: Let denote

$$t_n = \begin{cases} \alpha_n & \text{if } p_{\mathrm{A}}(t_n) \neq p_{\mathrm{A}}(t_n^-), \\ \beta_n & \text{if } p_{\mathrm{B}}(t_n) \neq p_{\mathrm{B}}(t_n^-), \\ \gamma_n & \text{if } p_{\mathrm{C}}(t_n) \neq p_{\mathrm{C}}(t_n^-). \end{cases}$$

If $p_{\mathrm{A}}(\alpha_n) \neq p_{\mathrm{A}}(\alpha_n^-)$, then $p_{\mathrm{A}}(\alpha_n) = 1 - p_{\mathrm{A}}(\alpha_n^-)$ for $p_\varphi(t) \in \{0, 1\}$. From (16)

$$\mathbf{D}(\alpha_n) = \begin{bmatrix} p_{\mathrm{C}}(\alpha_n) & p_{\mathrm{B}}(\alpha_n) & p_{\mathrm{A}}(\alpha_n) \\ 1 - p_{\mathrm{C}}(\alpha_n) & 1 - p_{\mathrm{B}}(\alpha_n) & 1 - p_{\mathrm{A}}(\alpha_n) \end{bmatrix} = \begin{bmatrix} p_{\mathrm{C}}(\alpha_n^-) & p_{\mathrm{B}}(\alpha_n^-) & 1 - p_{\mathrm{A}}(\alpha_n^-) \\ 1 - p_{\mathrm{C}}(\alpha_n^-) & 1 - p_{\mathrm{B}}(\alpha_n^-) & p_{\mathrm{A}}(\alpha_n^-) \end{bmatrix} \tag{18}$$

Applying $\mathbf{D}(\alpha_n)$ in (15),

$$s(\alpha_n) = 4p_{\mathrm{C}}(\alpha_n^-) + 2p_{\mathrm{B}}(\alpha_n^-) + 1 - p_{\mathrm{A}}(\alpha_n^-)$$

On the other hand,

$$s(\alpha_n^-) = 4p_{\mathrm{C}}(\alpha_n^-) + 2p_{\mathrm{B}}(\alpha_n^-) + p_{\mathrm{A}}(\alpha_n^-)$$

Thus,

$$s(\alpha_n) - s(\alpha_n^-) = 1 - 2p_{\mathrm{A}}(\alpha_n^-)$$

, and since $p_{\mathrm{A}}(\alpha_n^-) \in \{0, 1\}$,

$$s(\alpha_n) - s(\alpha_n^-) \neq 0 \Rightarrow s(\alpha_n) \neq s(\alpha_n^-).$$

Similarly, it can be proven that

$$\text{if } p_{\mathrm{A}}(\beta_n) \neq p_{\mathrm{A}}(\beta_n^-) \Leftrightarrow s(\beta_n) \neq s(\beta_n^-)$$

and

$$\text{if } p_{\mathrm{A}}(\gamma_n) \neq p_{\mathrm{A}}(\gamma_n^-) \Leftrightarrow s(\gamma_n) \neq s(\gamma_n^-).$$

The result shows a change in the switching state $s(t)$ happens whenever one of the $p_{\mathrm{A}}(t)$, $p_{\mathrm{B}}(t)$, or $p_{\mathrm{C}}(t)$ changes. ■

Proposition 3. *Assume that $W(t_0)$ is a subsequence of $X(t_0)$ as described in (17) with the length of w such that $t_0 - t_w < T_c$.*

For $w = 6$, $t_0 - t_w < T_c$ and the changes of the PWM signals (p_A, p_B, p_C) occur at different time instances α_{n_1}, β_{n_2}, and γ_{n_3}, where $n_1 \neq n_2 \neq n_3$, and $\min\{n_1, n_2, n_3\} \geq 0$, and $\max\{n_1, n_2, n_3\} \leq w$, i.e.,

$$p_A(\alpha_{n_1}) \neq p_A(\alpha_{n_1}^-), p_B(\alpha_{n_1}) = p_B(\alpha_{n_1}^-), p_C(\alpha_{n_1}) = p_C(\alpha_{n_1}^-),$$

and

$$p_A(\beta_{n_2}) = p_A(\beta_{n_2}^-), p_B(\beta_{n_2}) \neq p_B(\beta_{n_2}^-), p_C(\beta_{n_2}) = p_C(\beta_{n_2}^-),$$

and

$$p_A(\gamma_{n_3}) = p_A(\gamma_{n_3}^-), p_B(\gamma_{n_3}) = p_B(\gamma_{n_3}^-), p_C(\gamma_{n_3}) \neq p_C(\gamma_{n_3}^-).$$

Proof: Let define $\tau(q) := \{t | \frac{q}{2} T_c \le t < \frac{q+1}{2} T_c\}$ for $q \in \mathbb{Z}$. If the theorem is true, there exist α_{n_1}, β_{n_2}, and γ_{n_3} in $\tau(q)$, such that $\alpha_{n_1} \neq \beta_{n_2}$, $\alpha_{n_1} \neq \gamma_{n_3}$, and $\beta_{n_2} \neq \gamma_{n_3}$. From Proposition 2 if $s(t_n) \neq s(t_n^-)$, then $p_\varphi(t_n) \neq p_\varphi(t_n^-)$ and from (1)

$$r_\varphi(t_n) = c(t_n). \tag{19}$$

Let $q = \lfloor \frac{2t}{T_c} \rfloor$; thus, from (3),

$$c(t) = \begin{cases} 4A_c(F_c t - k - \frac{1}{4}), & \text{for } q = 2k \\ -4A_c(F_c t - k - \frac{3}{4}), & \text{for } q = 2k+1 \end{cases} \tag{20}$$

Let assume $q = 2k$. Applying (8), and (20) in (19)

$$A_r sin(2\pi F_r t_n + \phi) - 4A_c(F_c t_n - k - \frac{1}{4}) = 0 \tag{21}$$

$$M sin(2\pi F_r t_n + \phi) = 4(F_c t_n - k - \frac{1}{4}) \tag{22}$$

Let

$$\chi_\varphi := sin(2\pi F_r t_n + \phi). \tag{23}$$

Applying χ_φ in (22),

$$M\chi_\varphi = 4(F_c t_n - k - \frac{1}{4}) \tag{24}$$

hence,

$$t_n = T_c(\frac{1}{4} + k + \frac{M\chi_\varphi}{4}). \tag{25}$$

From (23),

$$-1 \le \chi_\varphi \le 1 \tag{26}$$

and consequently,

$$kT_c < t_n < (\frac{1}{2}+k)T_c;$$

thus,

$$2k < \frac{2t_n}{T_c} < 2k+1$$

and $q = \lfloor \frac{2t_n}{T_c} \rfloor = 2k$. The result proves the existence of $\alpha_{n_1}, \beta_{n_1}, \gamma_{n_1}$ for even $q = \lfloor \frac{2t_n}{T_c} \rfloor$. Similar proof can be used for the odd $q = 2k+1$. So, for every $t_0 \geq \tau(q')$ there exists an integer $q = q' - 1$ where $q' = \lfloor \frac{2t_0}{T_c} \rfloor - 1$ such that $\{\alpha_{n_1}, \beta_{n_2}, \gamma_{n_3}\} \in \tau(q)$. Now, it is shown $\alpha_{n_1} \neq \beta_{n_2} \neq \gamma_{n_3}$.
From (25),

$$\alpha_{n_1} = T_c(\frac{1}{4}+k+\frac{M\chi_A}{4}) \quad (27)$$

$$\beta_{n_2} = T_c(\frac{1}{4}+k+\frac{M\chi_b}{4}) \quad (28)$$

$$\gamma_{n_3} = T_c(\frac{1}{4}+k+\frac{M\chi_c}{4}) \quad (29)$$

If α_{n_1} were equal to β_{n_2}, from (27) and (28) $\chi_A = \chi_b$. Replacing χ_φ from (23) yields

$$sin(2\pi F_r \alpha_{n_1}) = sin(2\pi F_r \alpha_{n_1} - \frac{2\pi}{3}) \quad (30)$$

Solving the above equation gives

$$\alpha_{n_1} = \frac{6m_2+5}{12F_r}, \qquad m_2 \in \mathbb{Z}. \quad (31)$$

Now it is shown that α_{n_1} is not an acceptable solution. From (27),

$$M = \frac{4F_c\alpha_{n_1} - 4k - 1}{sin(2\pi F_r \alpha_{n_1})} \quad (32)$$

by replacing α_{n_1} from (31),

$$M = \frac{\frac{F_c}{3F_r}(6m_2+5) - 4k - 1}{sin(\frac{5\pi}{6} + m_2\pi)}. \quad (33)$$

From (4), $\frac{F_c}{3F_r} = m_1$; thus,

$$M = \frac{6m_2m_1 + 5m_1 - 4k - 1}{(-1)^{m_2} sin(\frac{5\pi}{6})} = (-1)^{m_2}(12m_2m_1 + 10m_1 - 8k - 2) \quad (34)$$

Equation (34) forces M to be an integer value which contradicts the assumption, so it is forced to conclude that $\alpha_{n_1} \neq \beta_{n_2}$. Similarly, $\alpha_{n_1} = \gamma_{n_3}$ results in

$$\alpha_{n_1} = \frac{6m_3+1}{12F_r}, m_3 \in \mathbb{Z}. \quad (35)$$

Applying α_{n_1} in (32)

$$M = \frac{\frac{N}{3}(6m_3+1) - 4k - 1}{sin(\frac{\pi}{6}m_3\pi)} = \frac{6m_1m_3 + m_1 - 4k - 1}{(-1)^{m_3} sin(\frac{\pi}{6})} = (-1)^{m_3}(12m_1m_3 + 2m_1 - 8k - 2) \quad (36)$$

$$\Rightarrow M \in \mathbb{Z}$$

Also, $\beta_{n_2} = \gamma_{n_3}$ results in

$$\beta_{n_2} = \frac{2m_4+1}{4F_r}, \qquad m_4 \in \mathbb{Z}. \quad (37)$$

From (28),

$$M = \frac{4F_c\beta_{n_2} - 4k - 1}{sin(2\pi F_r \alpha_{n_1} - \frac{2\pi}{3})} \quad (38)$$

Applying β_{n_2} from (37) in (38),

$$M = \frac{\frac{F_c}{F_r}(2m_2+1) - 4k - 1}{sin(-\frac{\pi}{6} + m_4\pi)} = \frac{6m_4m_1 + 3m_1 - 4k - 1}{(-1)^{m_4} sin(-\frac{\pi}{6})} = (-1)^{1+m_4}(12m_4m_1 + 6m_1 - 8k - 2) \quad (39)$$

$$\Rightarrow M \in \mathbb{Z}$$

The results show M is an integer which is inconsistent with the assumption $0 < M < 1$. Therefore, it is concluded that $\alpha_{n_1} \neq \beta_{n_2}$, $\alpha_{n_1} \neq \gamma_{n_3}$, and $\beta_{n_2} \neq \gamma_{n_3}$ exist in $\tau(q)$.
Therefore, $W(t_0)$ for $t_0 \in \tau(q+1)$ and $t_w \in \tau(q-1)$ includes $\tau(q)$. It means within $t_0 - t_w < T_c$ all $\alpha_{n_1}, \beta_{n_2}, \gamma_{n_3} \in \tau(q)$ can be observed. Since only three states changes within $\tau(q)$

$$\lfloor \frac{n_1}{3} \rfloor = \lfloor \frac{n_2}{3} \rfloor = \lfloor \frac{n_3}{3} \rfloor = q \quad (40)$$

and the minimum w that certainly includes $\tau(q)$ is equal to 6. ■

Proposition 4. *If v_A is monitored for a time span such as $W(t_0)$ where α^- and α belong to $W(t_0)$, then both levels of voltage, $\pm E_N$, will be observed.*

$$\{v_A(\alpha^-), v_A(\alpha)\} = \{-E_N, E_N\},$$

$$\{v_B(\beta), v_B(\beta^-)\} = \{E_N, -E_N\},$$

and

$$\{v_C(\gamma), v_C(\gamma^-)\} = \{E_N, -E_N\}.$$

Proof: Let $\varphi = \mathrm{A}$, applying $\mathbf{D}(\alpha_n)$ from (18) in (11)

$$\mathbf{v}(\alpha_n) = \mathbf{e} \cdot \mathbf{D}(\alpha_n) = [E_N, -E_N] \begin{bmatrix} p_C(\alpha_n^-) & p_B(\alpha_n^-) & 1-p_A(\alpha_n^-) \\ 1-p_C(\alpha_n^-) & 1-p_B(\alpha_n^-) & p_A(\alpha_n^-) \end{bmatrix} = [\mathrm{v_C}(\alpha_n^-), \mathrm{v_B}(\alpha_n^-), -\mathrm{v_A}(\alpha_n^-)]. \quad (41)$$

From (11)

$$\mathbf{v}(\alpha_n^-) = [\mathrm{v_C}(\alpha_n^-), \mathrm{v_B}(\alpha_n^-), \mathrm{v_A}(\alpha_n^-)]$$

Squaring both sides yields $\mathrm{v_A}(\alpha_n) = -\mathrm{v_A}(\alpha_n^-)$. Thus,

$$\mathrm{v_A}(\alpha_n) = \begin{cases} E_N, & \text{if } \mathrm{v_A}(\alpha_n^-) = -E \\ -E_N, & \text{if } \mathrm{v_A}(\alpha_n^-) = E \end{cases}$$

The similar proof can be done for $\varphi = \mathrm{B}$, and $\varphi = \mathrm{C}$. Thus, $\{\mathrm{v_A}(\alpha), \mathrm{v_A}(\alpha^-)\} = \{E_N, -E_N\}$, also $\{\mathrm{v_B}(\beta), \mathrm{v_B}(\beta^-)\} = \{E_N, -E_N\}$, and $\{\mathrm{v_C}(\gamma), \mathrm{v_C}(\gamma^-)\} = \{E_N, -E_N\}$. ■

As a result of Proposition 4, if just one of the voltage levels is observed in a window of time containing α, β, or γ, then a fault in detected in phase A, B, or C. In this situation, some switching states cannot be observed that can be indicated by a fault banned zone in the voltage space pattern.

B. Fault Banned Zones

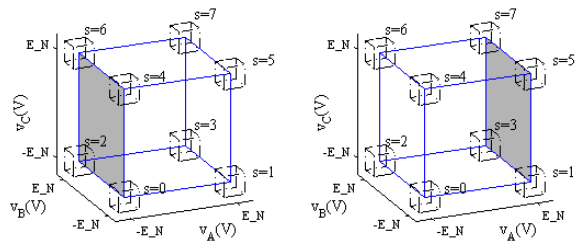
Consider a short-circuit fault in a switch of phase leg $\tilde{\varphi}$. $\tilde{R}_{\text{off}}$ and $\tilde{R}_{\text{on}}$ denote the internal resistances of the faulty switch in the off and on states respectively. In the faulty situation, $\tilde{R}_{\text{off}} \approx \tilde{R}_{\text{on}} \approx 0$. If the upper switch of the phase leg is faulty, $\mathrm{v}_{\tilde{\varphi}} = \mathrm{v}^u$, where

$$\mathrm{v}^u = \begin{cases} \frac{E}{2} \cdot \epsilon_1 & \text{for } g_u = 1, g_l = 0 \\ \frac{E}{2} \cdot \epsilon_2 & \text{for } g_u = 0, g_l = 1 \end{cases},$$

$\epsilon_1 \approx 1$, and $\epsilon_2 \approx 0$; thus, $\mathrm{v}^u \neq -E_N$. In this situation, the voltage space pattern does not appear in the $\mathrm{v}_{\tilde{\varphi}} = -E_N$ plane of the voltage space. This plane is associated with four switching states that indicate a face of the cubic pattern in the voltage space. The voltage space pattern cannot enter this zone in the presence of the fault; thus, this area is named a fault banned zone. Six faces of the cubic pattern allow isolating six different faulty switches. On the other hand, $\mathrm{v} = \mathrm{v}^l$ if the lower switch of phase $\tilde{\varphi}$ is faulty, where

$$\mathrm{v}^l = \begin{cases} -\frac{E}{2} \cdot \epsilon_2 & \text{for } g_u = 1, g_l = 0 \\ -\frac{E}{2} \cdot \epsilon_1 & \text{for } g_u = 0, g_l = 1 \end{cases}$$

Thus, $\mathrm{v}^l \neq +E_N$, and the fault baned zones is in the $\mathrm{v}_{\tilde{\varphi}} = +E_N$ plane in the voltage space; thus, the fault banned zones of upper and lower switches of a phase leg are in the opposite faces of the cubic pattern. For example, Fig. 6 illustrates the fault banned zones for Q_1 and Q_2 where $\tilde{\varphi} = A$. The fault



(a) Fault banned zone for Q_1 (b) Fault banned zone for Q_2

Fig. 6: Fault banned zones for a faulty switch in phase A.

banned zone of Q_j can be represented by F_j, a set of four switching states that are not achievable in the presence of a fault in Q_j. In (15), the switching states were determined based on the state of the upper switches of the inverter, $\mathbf{u}$. Conversely, equation (43) calculates $\widetilde{s}$, the switching state based on the on–off states of the lower switches $\mathbf{l}$, where

$$\mathbf{l} := [0\ 1] \cdot \mathbf{D}(t)$$

From (16),

$$\mathbf{l} = [1 - p_{\mathrm{C}}(\alpha_n)\ \ 1 - p_{\mathrm{B}}(\alpha_n)\ \ 1 - p_{\mathrm{A}}(\alpha_n)]$$

and

$$\mathbf{u} + \mathbf{l} = [1\ 1\ 1];$$

thus,

$$\mathbf{u} = [1\ 1\ 1] - \mathbf{l}, \tag{42}$$

by applying $\mathbf{u}$ in (15)

$$\widetilde{s}(t) := ([1\ 1\ 1] - \mathbf{l}) \cdot \mathbf{b}. \tag{43}$$

In the no-fault situation, $\widetilde{s}(t) = s(t)$. However, in the presence of a faulty switch $\widetilde{s}(t)$ can be different from $s(t)$. This difference is used to define fault banned zones, F_j.

$$F_j := Y_j^u \cup Y_j^l - Y_j^u \cap Y_j^l \tag{44}$$

In (44), Y_j^u and Y_j^l are two sets of all possible $s(t)$ and $\widetilde{s}(t)$ that can be obtained in the presence of a short-circuit fault in Q_j

$$Y_j^u = \{s(t) | d_j(t) = 1, \forall g_i(t) \in \{0, 1\}\}$$

and

$$Y_j^l = \{\widetilde{s}(t) | d_j(t) = 1, \forall g_i(t) \in \{0, 1\}\}.$$

V. Procedure of Fault Detection and Isolation

In this section, a fault diagnosis algorithm is proposed for unknown switching frequency; where access to the control signals is not possible or the switching frequency changes by the feedback loop. Suppose that the system is healthy at time t_0 and a fault will occur at $t_f > t_0$. The objective is to detect and isolate the faulty switch at time $t_e > t_f$ given the switching states. The process contains four stages; extracting switching states, initialization, fault detection, and fault isolation.

A. Extracting Switching States

Fault diagnosis process commence by monitoring three phase voltages and extracting the corresponding switching states. Let

$$\mathbf{v}(t) = [\mathrm{v}_{\mathrm{C}}(t),\ \mathrm{v}_{\mathrm{B}}(t),\ \mathrm{v}_{\mathrm{A}}(t)] \tag{45}$$

be the vector of observed voltages from the detectors. A threshold span ϵ_m in the neighbourhood of each normal voltage level E_N is defined, and the monitored voltage vector in this neighbourhood is mapped to a known $\mathbf{v}_s$. The neighbourhood of $\mathbf{v}_s$ is defined as

$$\mathbf{h}_s = \mathbf{v}_s \cdot \mathrm{diag}(\epsilon_{\mathrm{C}}, \epsilon_{\mathrm{B}}, \epsilon_{\mathrm{A}})$$

where ϵ_φ for $\varphi = \mathrm{A}, \mathrm{B}, \mathrm{C}$ is the distance between $\mathbf{v}_s$ and $\mathbf{h}_s$ in each direction of the voltage space. Equation (46) defines a set of all voltages in the neighbourhood of $\mathbf{v}_s$ within a distance of ϵ_m in each direction of the voltage space.

$$\mathbf{H}_s =: \{\mathbf{h}_s | \forall 1 - \epsilon_m \leq \epsilon_\varphi < 1 + \epsilon_m\} \tag{46}$$

ϵ_m is selected such that both levels of voltage in the faulty situation, v^u and v^l, are isolable, e.g., $\epsilon_m = 0.25$.

From Proposition 1 and definition (11) there exists a one-to-one correspondence between $\mathbf{v}_s$ and s. Thus, any observed voltage vector $\mathbf{v}(t)$ can be mapped to a known state $\kappa \in \mathbb{S}$, where $\mathbb{S}$ is as defined in (14).

$$s(t) := \begin{cases} \kappa, & \text{if } \mathbf{v}(t) \in \mathbf{H}_\kappa \\ s(t^-) & \text{otherwise.} \end{cases} \tag{47}$$

B. Initialization

Let $W(t_0) = \langle s(t_0), s(t_1), s(t_2), \ldots, s(t_5)\rangle = \langle w_1, w_2, \ldots, w_6\rangle$ be a subsequence of non-equal adjacent switching states. The sequence $W(t_0)$ contains α_{n_1}, β_{n_2} and γ_{n_2} in a random order, therefore, $W(t_0)$ is shown as a sequence of sets

$$W(t_0) = \langle S'_{q_0+1}, S_{q_0}, S'_{q_0-1}\rangle,$$

where $S_q = \{s(\alpha_{n_1}), s(\beta_{n_2}), s(\gamma_{n_3})\}$, $q = \lfloor \frac{n_1}{3} \rfloor = \lfloor \frac{n_2}{3} \rfloor = \lfloor \frac{n_3}{3} \rfloor$, $S'_q \subset S_q$, $|S'_{q_0+1}| = \psi$, and $t_\psi = max\{\alpha_{n_1}, \beta_{n_2}, \gamma_{n_3}\}$. To find ψ, three consequent states that contain changes of all three phases, i.e., S_q should be found. Let $\oplus$ be the XOR operator which is applied to the binary value of s(t). From the state definition,

$$p_A(\alpha_{n_1}) \neq p_A(\alpha^-_{n_1}) \Rightarrow s(\alpha_{n_1}) \oplus s(\alpha^-_{n_1}) = 1,$$
$$p_B(\beta_{n_2}) \neq p_B(\beta^-_{n_2}) \Rightarrow s(\beta_{n_2}) \oplus s(\beta^-_{n_2}) = 2,$$
$$p_C(\gamma_{n_3}) \neq p_C(\gamma^-_{n_3}) \Rightarrow s(\gamma_{n_3}) \oplus s(\gamma^-_{n_3}) = 4.$$

Therefore, there exists a subsequence of $W(t_0)$ such that

$$\{w_\psi \oplus w_{\psi+1}, w_{\psi+1} \oplus w_{\psi+2}, w_{\psi+2} \oplus w_{\psi+3}\} = \{1,2,4\},$$

where $1 \leq \psi \leq 3$. The initialization stage will be accomplished by finding ψ.

C. Fault Detection

After the initialization stage, the system is being monitored for more new states. Let $\lambda = \psi + 3\theta$ and

$$U(t_{\lambda-\eta}) = \langle x_{\lambda-\eta}, \ldots, x_{\lambda-1}, x_\lambda\rangle, \qquad 1 \leq \eta \leq 3.$$

Whenever a new state is detected, the fault detection test is carried on. Let $\hat{U}(\eta) = x_{\lambda-\eta} \oplus x_{\lambda-\eta+1}$. A fault is detected if $\hat{U}(\eta) \notin \{1,2,4\}$, or $\hat{U}(\eta) = \hat{U}(\eta-1)$. If a fault is detected, the fault occurrence time is $t_{\lambda-\theta} < t_f < t_{\lambda-\eta}$ which is less that one carrier period. However, if

$$\{x_{\lambda-3} \oplus x_{\lambda-2}, x_{\lambda-2} \oplus x_{\lambda-1}, x_{\lambda-1} \oplus x_\lambda\} = \{1,2,4\}$$

No fault is detected. Thus, θ is increased by one, and the fault detection test will be continued by restarting η. If a fault is detected, the fault isolation stage will be run.

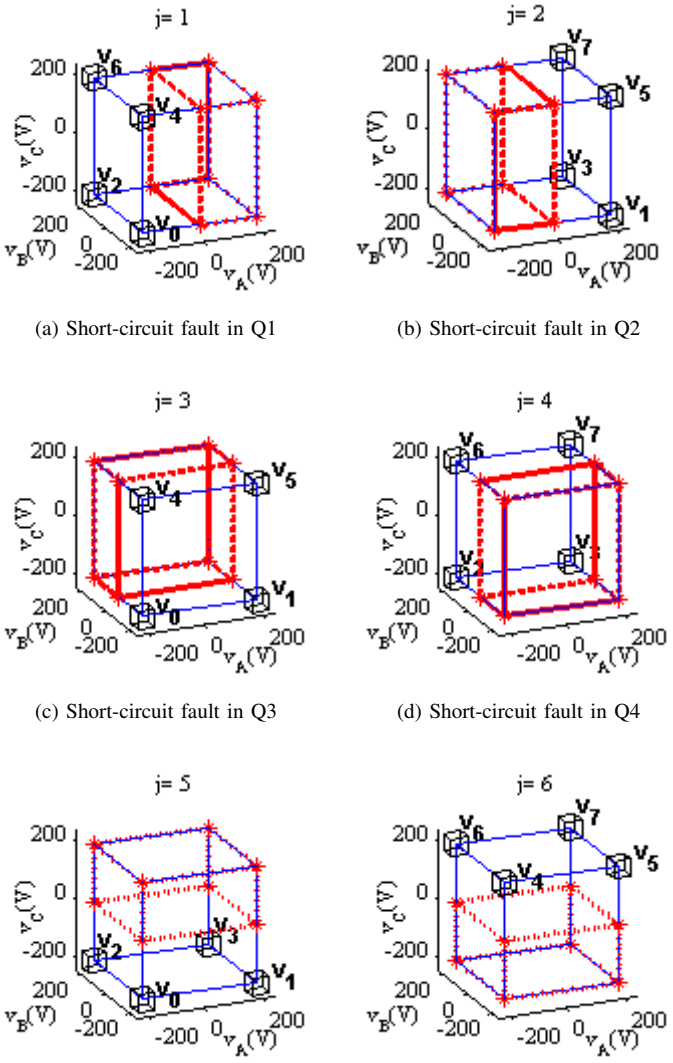
D. Fault Isolation

Based on what was described in Section V-C, if the phase voltages are monitored for a period of T_c, the value of all phase voltages will definitely change from one level to another one. Therefore, the voltage space pattern will not remain inside one face of the cubic pattern for $t_w = t_0 - T_c$. Thus, if non of the monitored states were a subset of F_j, as defined in Section IV-B, Q_j is diagnosed as the faulty switch. All fault banned zones are calculated in Table VI for a short-circuit fault in Q_j where $j = 1$ to 6.

short-circuit fault location (Q_j)	Fault banned zone (F_j)
Q_1	{0,2,4,6}
Q_2	{1,3,5,7}
Q_3	{0,1,4,5}
Q_4	{2,3,6,7}
Q_5	{0,1,2,3}
Q_6	{4,5,6,7}

TABLE VI: Fault banned zones.

For the isolation purpose, the intersection of $W(t_e) = \langle x_{\lambda-2}, x_{\lambda-1}, \ldots, x_{\lambda+3}\rangle$ and each fault banned zone is calculated. If $W(t_e) \cap F_j = \emptyset$ then Q_j is isolated as the faulty switch. Fig. 7 illustrates the fault isolation in the voltage space for all six switches. After the fault occurs, the pattern cannot enter the fault banned zone of the faulty switch.



(a) Short-circuit fault in Q1

(b) Short-circuit fault in Q2

(c) Short-circuit fault in Q3

(d) Short-circuit fault in Q4

(e) Short-circuit fault in Q5

(f) Short-circuit fault in Q6

Fig. 7: Fault isolation in the voltage space.

E. Discussion

In this section, the property of the VSP-based FID method is discussed.

1) Fault diagnosis time: VSP based FDI is an online method that can detect and isolate the faulty switch in less than one period of the carrier signal. For example, with $T_c = 20$KHz fault isolation time is less than 50μs. This is the fastest FDI method available for inverters.

2) Number of sensors: Only three voltage detectors are needed for the FDI purpose. It might be possible to used the built voltage detectors of the in switch driver IC and implement

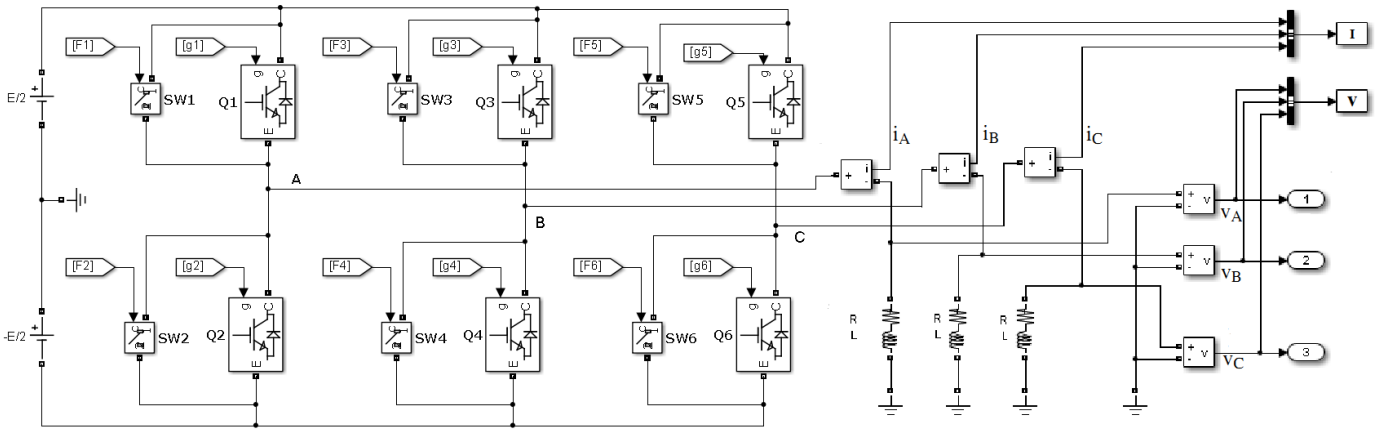


Fig. 8: Simulink model of the VSI.

the FDI software inside the driver IC without adding extra voltage detectors.

3) Robustness to load changes: If the value or type of the load changes only the current waveform changes; however, the voltage switching waveform will not be affected. Therefore, the proposed FDI method is robust to the load changes.

4) Fault occurrence time: The faults are probable to occur in any time, and the corresponding current waveform will be different even for the same switch. However, in the proposed VSP-based FDI method, the fault banned zones are independent to the fault occurrence time, hence the FDI result will not be effected by changing the fault occurrence time.

5) Robustness to the modeling errors: VSP does not require accurate model of the circuit's components. The voltage neighbor sets will cancel out the effect of modeling error or ambient disturbances. Thus, patterns will remain constant even if there were some errors in the mathematical model or in the presence of noise. Because the voltage levels are normally far away from each other (e.g. 200V and -200V), the model errors or component's tolerances will not affect the FDI result. However, in the other model based method like [10], any small differences between the mathematical model of the system and the actual system could lead to false alarm.

6) Switching frequency: The VSPs and the fault banned zones are independent to the switching frequency. Therefore, the changes of carrier frequency will not effect the FDI result. Interestingly, a higher switching frequency will lead to a shorter fault detection time and increases the fault detection speed.

VI. Simulation

To evaluate the performance of the VSP-based FDI method, a three-phase two-level VSI with six IGBT switches is modelled using Matlab SimPowerSystems as shown in Fig. 8. In this model, all six IGBTs are similar, and the internal resistance of each switch is $R_{\text{on}} = 1\text{m}\Omega$, and $R_{\text{off}} = 100$ KΩ in on and off states respectively. Figure. 9 shows the SPWM block that controls the on–off state of the IGBTs. In order to simulate the short-circuit faults, a circuit breaker with internal resistance $R_f = 1\text{m}\Omega$ is added in parallel to each IGBT. In the normal situation, F1 to F6 of Fig. 8 are low; thus, SW1 to SW6

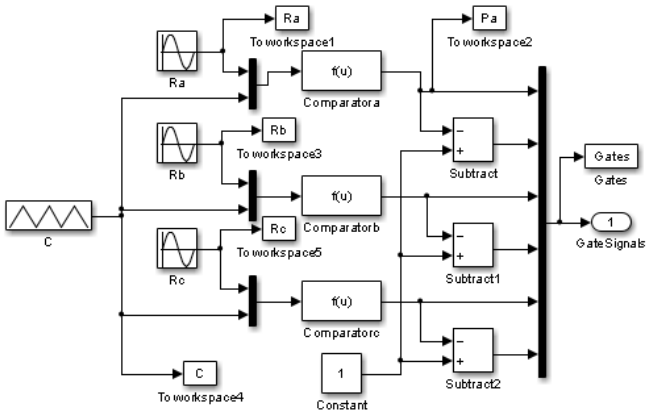


Fig. 9: Simulink model of the PWM control block.

are open. The fault simulator block inserts a short-circuit fault in Q_j by closing the parallel switch at $t = t_f$. For example, if F1=1 then SW1 is closed which simulates a short-circuit fault in Q_1. This model covers short-circuit faults caused either by gate-misfiring, or damaging of internal diode, or drain-source junction. Only single faults are considered in the simulations. Fig. 10 depicts the FDI model in Matlab Simulink. The output

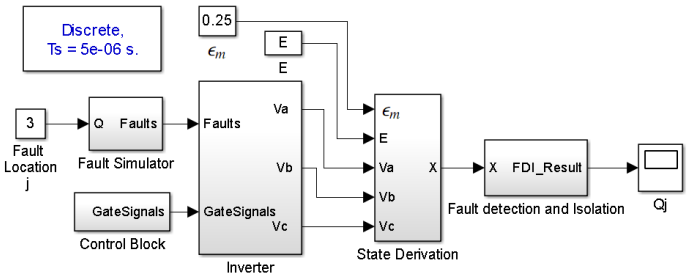


Fig. 10: Simulink model of the FDI procedure.

of the inverter is connected to a three-phase grounded Y-connected serial RL load. The load is selected such that its time constant $\frac{L}{R}$ is equal to $\frac{1}{3Fr}$. In this model, $R = 1\Omega$ and $L = 5.6$mH for all three phases, and $E = 400$. Three voltage detectors monitor the phase voltages. The sampling period

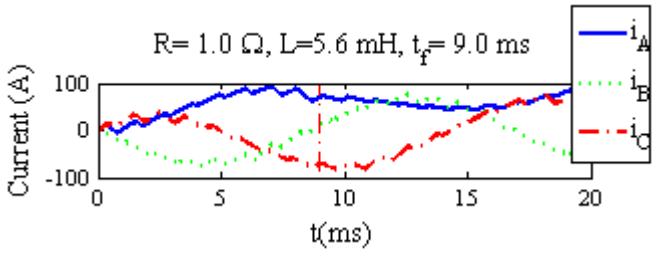
T_s is less than $\frac{P_m}{2}$ so that all changes in the voltage signals are detectable, where P_m is the minimum pulse width of the voltage signal. The minimum pulse width occurs at the peak of the reference signal; thus, $\frac{P_m}{T_c} = \frac{1-M}{2}$, hence $P_m = \frac{1-M}{2} T_c$.

Figure 11 illustrates the simulation results for $j = 1$ as an example of a fault in an upper switch. In this model, $F_r = 60$Hz, $F_c = 900$Hz, $M = 0.8$, and the fault occurs at $t_f = 9ms$. In Fig. 11a, i_A, i_B, and i_C represents the current signals of phases A, B, and C respectively. The current signal is illustrated in order to show the effect of the switch fault in the load. However, the current is not used for the FDI purpose. Figure 11b depicts the phase voltages obtained from three voltage detectors. Figures 11c and 11d show the switching states in the time domain and in the voltage domain respectively. As shown in Fig. 11d, after the fault occurs the pattern does not appear on a face of the cube determined by $\mathbf{v}_0, \mathbf{v}_2, \mathbf{v}_4$, and $\mathbf{v}_6$. Comparing to the fault banned zones of Table VI, Q_1 is isolated as the faulty switch. Fig. 11e provides the FDI result. In this figure, $j = 0$ represents the no-fault situation and $j = 1$ indicates the existence of a fault in Q_1. In this example, the fault is detected in $t_d = 392.5\mu s$ which is equal to 35% of T_c. The result validates that the fault is detected in less than one carrier period.

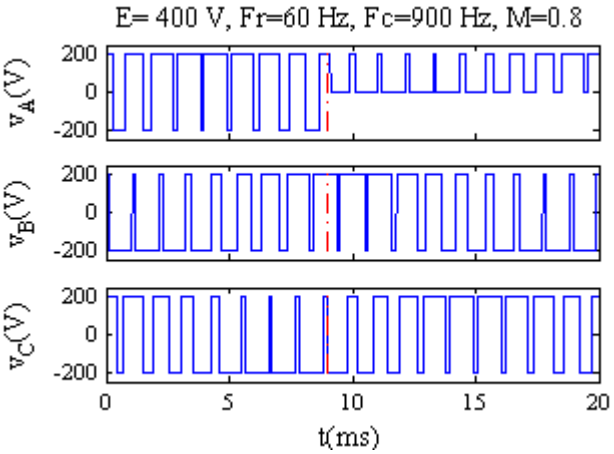
On the other hand, Fig. 12 illustrates the simulation results for $j = 6$ as an example of a fault in a lower switch. In this model, $t_f = 8.5ms$, and the other conditions are similar to the previous example. As shown in Fig. 12c, after the fault occurs, the pattern does not belong to the face indicated by $\mathbf{v}_4, \mathbf{v}_5, \mathbf{v}_6$, and $\mathbf{v}_7$. Comparing to the fault banned zones of Table VI, Q_6 is isolated as the faulty switch. It can be seen from Fig. 12d that j jumps from 0 to 6 in $t_d = 142.5\mu s$ after the fault occurs. In this example, the fault detection time is equal to 13% of T_c that is less than one carrier period as predicted in the theory.

The maximum fault detection time is proportional to the carrier period. Therefore, for higher carrier frequencies, the fault detection time is lower. In the theory, an infinite sampling frequency was assumed. However, in the simulations, the sampling period is limited. Therefore, in some instances where $\alpha - \beta < T_s$ (or $\beta - \gamma < T_s$, or $\alpha - \gamma < T_s$), the difference between α and β (or β and γ, or α and γ) is not detectable, and two phase voltages can change at the same time which results in a diagonal pattern in the voltage space as can be seen in Fig. 13d. This transitions can cause false alarms. In order to prevent this false alarms, the FDI procedure is limited to the fault isolation task. The isolation task is continually running, and if $j \neq 0$ a fault is detected. Although this modification can increase the maximum fault detection time, no false alarm will be detected.

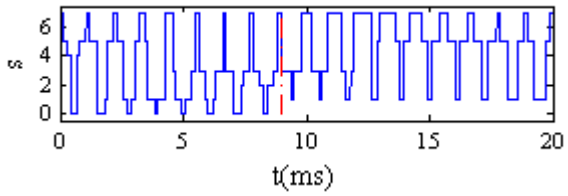
For example, Fig. 13 illustrates the simulation results for a short-circuit fault in Q_5 while $F_c = 19.98KHz$. The FDI result is shown in Fig. 13e. The fault detection time is $t_d = 92.5\mu s$ in this example. Figure. 14 illustrates the simulation results for a short-circuit fault in Q_4 while $F_c = 19.98KHz$. The FDI result is shown in Fig. 14e. The fault detection time is $t_d = 70\mu s$ in this example. Figure. 15 illustrates the simulation results for a short-circuit fault in Q_3 while $F_c = 19.98KHz$. As shown in Fig. 15d, the fault detection time is $t_d = 70\mu s$ in this example. Figure. 16 illustrates the simulation results for a short-circuit fault in Q_2 while $F_c = 19.98KHz$.



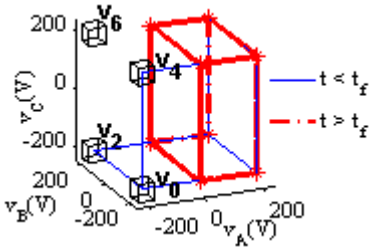
(a) Phase current signals.



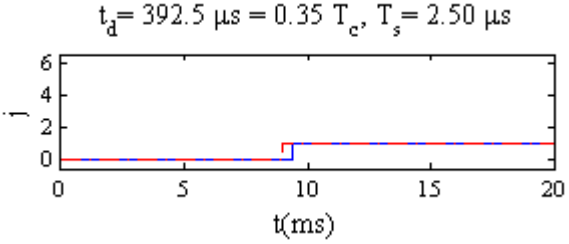
(b) Phase voltage signals.



(c) Switching states.

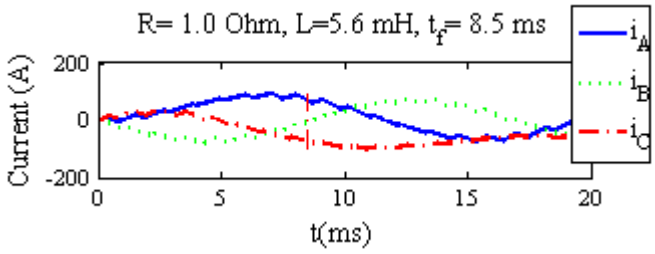


(d) Switching state pattern in the voltage space

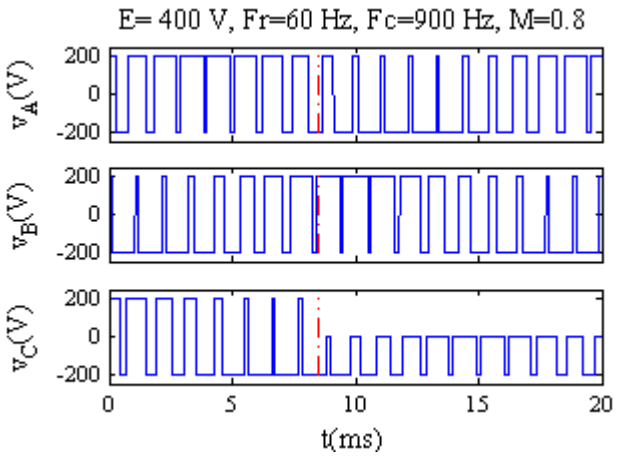


(e) FDI result.

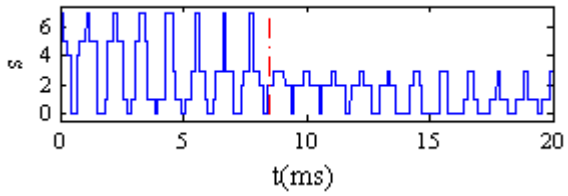
Fig. 11: Short-circuit fault in Q_1.

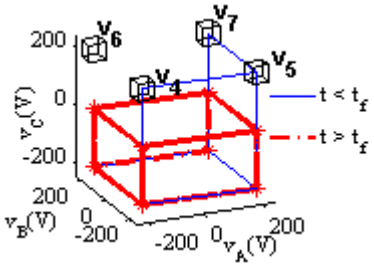


(a) Phase current signals.

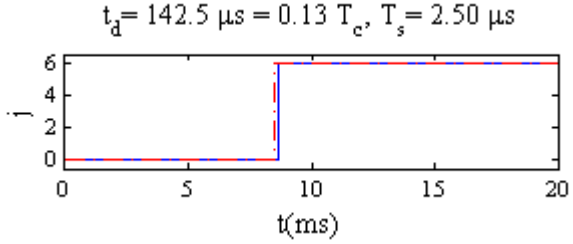


(b) Phase voltage signals.



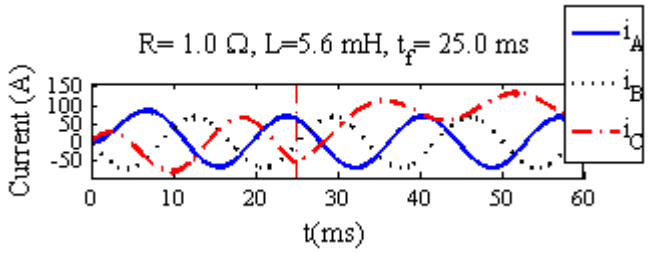


(c) Switching state pattern in the voltage space

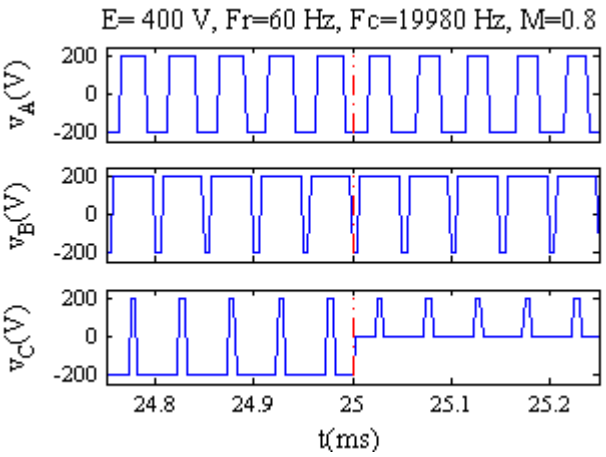


(d) FDI result.

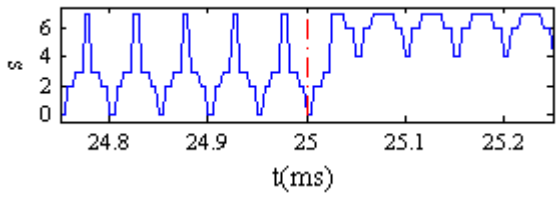
Fig. 12: Short-circuit fault in Q_6.



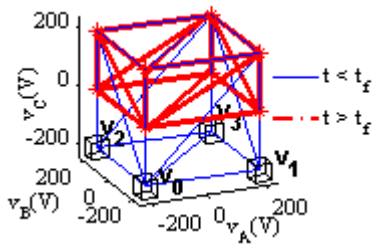
(a) Phase current signals.



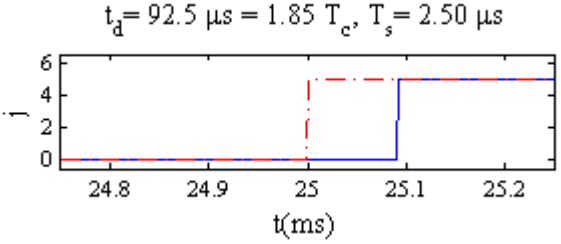
(b) Phase voltage signals.



(c) Switching states.

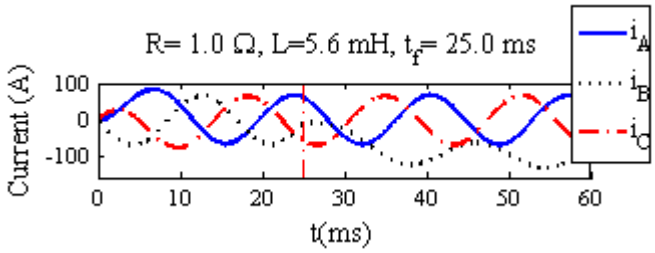


(d) Switching state pattern in the voltage space

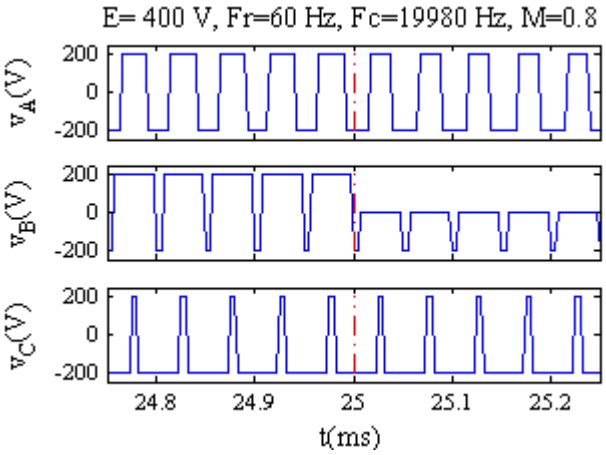


(e) FDI result.

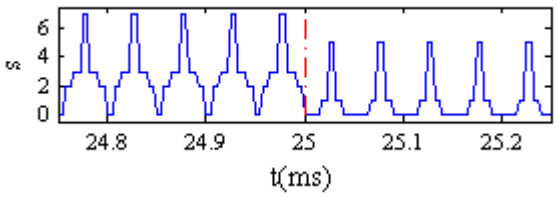
Fig. 13: Short-circuit fault in Q_5.



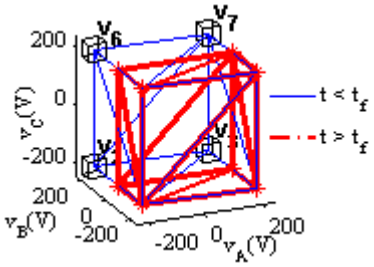
(a) Phase current signals.



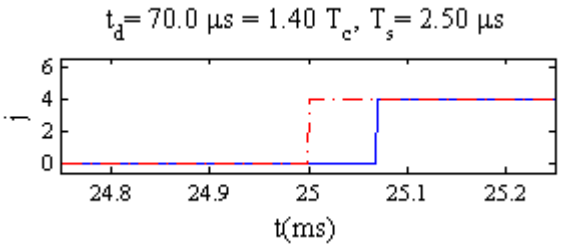
(b) Phase voltage signals.



(c) Switching states.

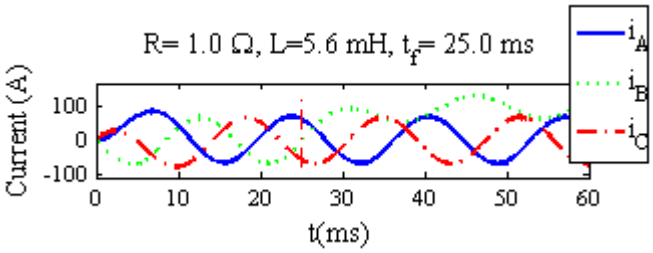


(d) Switching state pattern in the voltage space

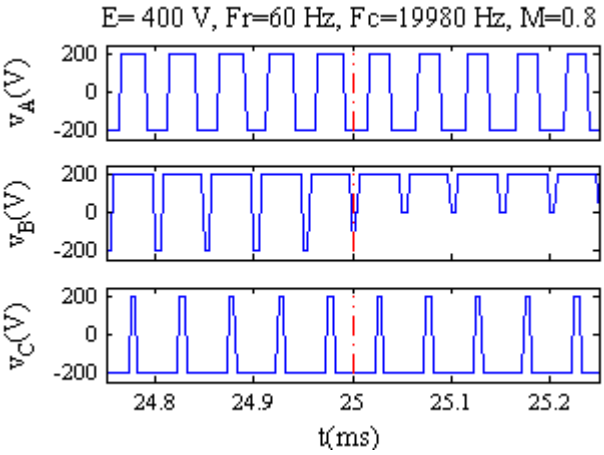


(e) FDI result.

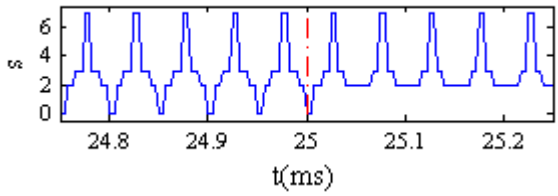
Fig. 14: Short-circuit fault in Q_4.

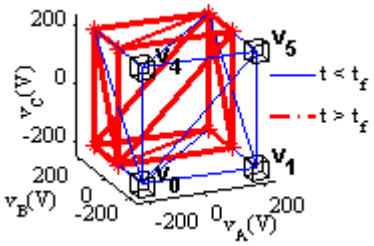


(a) Phase current signals.

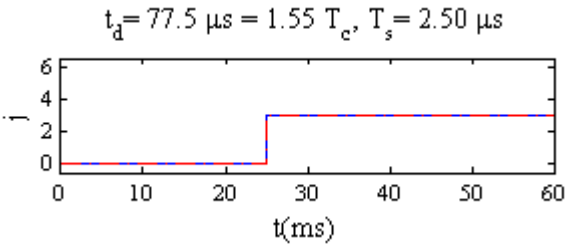


(b) Phase voltage signals.



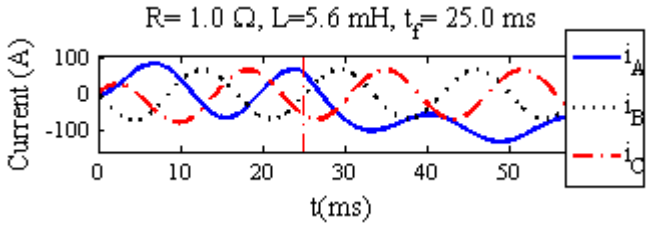


(c) Switching state pattern in the voltage space

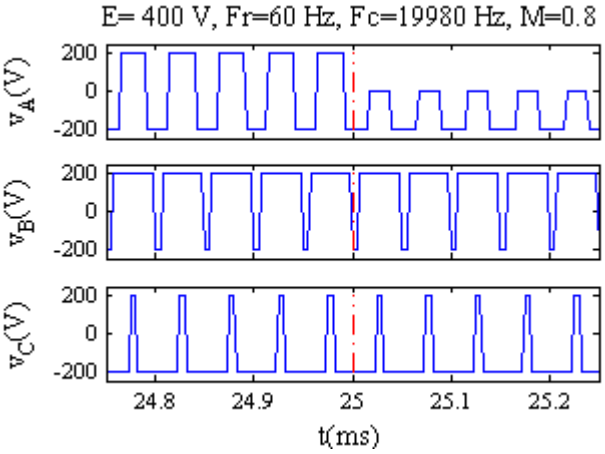


(d) FDI result.

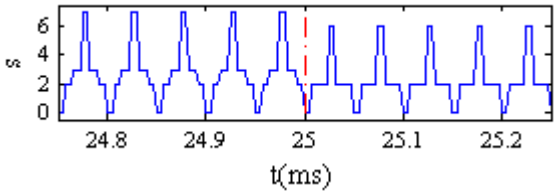
Fig. 15: Short-circuit fault in Q_3.



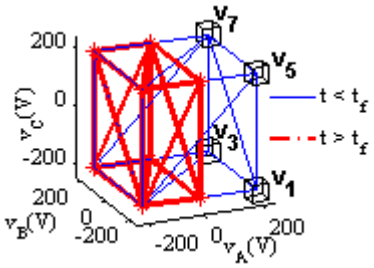
(a) Phase current signals.



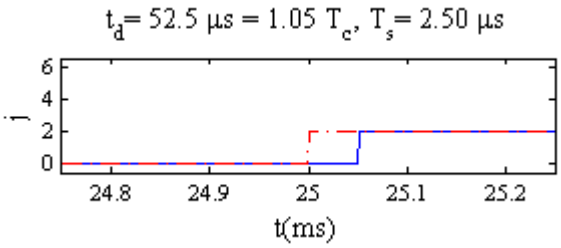
(b) Phase voltage signals.



(c) Switching states.



(d) Switching state pattern in the voltage space



(e) FDI result.

Fig. 16: Short-circuit fault in Q_2.

As shown in Fig. 16e, the fault detection time is reduced to $t_d = 52.2\mu s$.

VII. Conclusion

This paper has developed a fault diagnosis method for isolating IGBT short-circuit faults in VSIs. The ability to locate faulty transistor in a two-level three-phase inverter has been demonstrated. Fault banned zones has been introduced and extracted from the structural model of the inverter. Because the fault banned zones are independent to the load changes and PWM frequency, the method can be used in the closed loop applications. It has been proven that in theory, the VSP-based FDI method isolates the faulty switch within only one PWM carrier period. Implementation of fault tolerant control algorithms is possible using the high speed property of the proposed method.

The application of VSP for detecting other types of fault such as open-circuit faults, incipient faults, ageing, and degradation of transistors will be reported in the future. Some improvements can be done to make VSP FDI method suitable for multiphase multilevel inverters with a high number of switches in solar energy and aerospace applications. The voltage space patterns facilitate the isolation task.

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