MINI PROJECT

Design and Stimulation of Low Power Single-Phase Clocked D-Flip-Flop Using Cadence 180nm

SOBIKA S K

PG Scholar

Kongu Engineering College

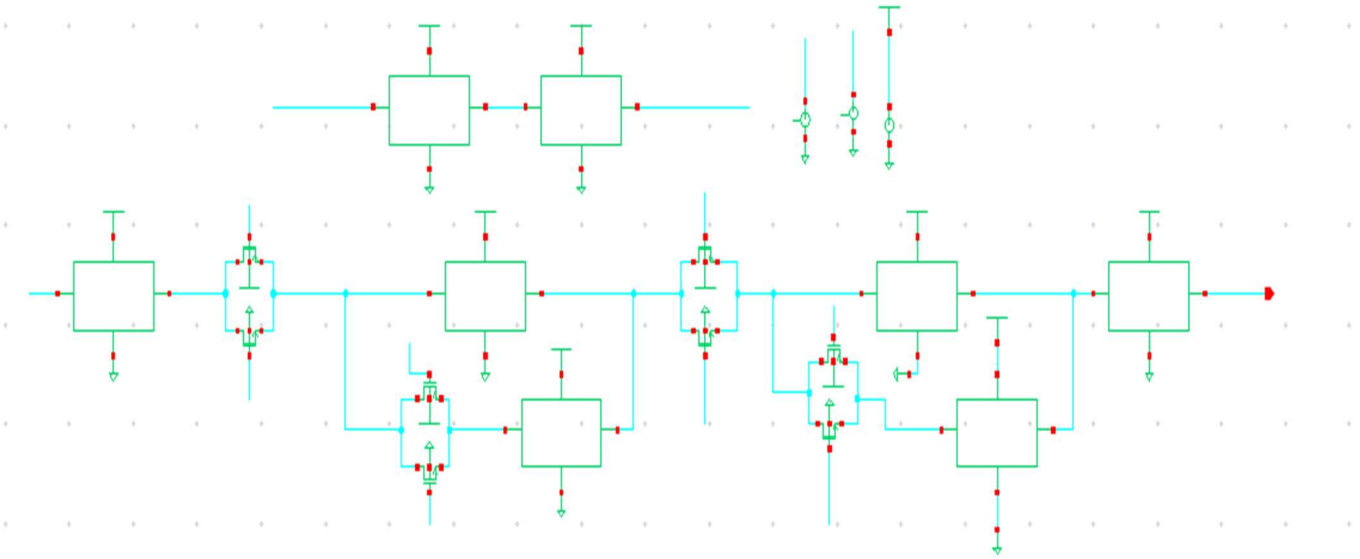
Perundurai

ABSTRACT:

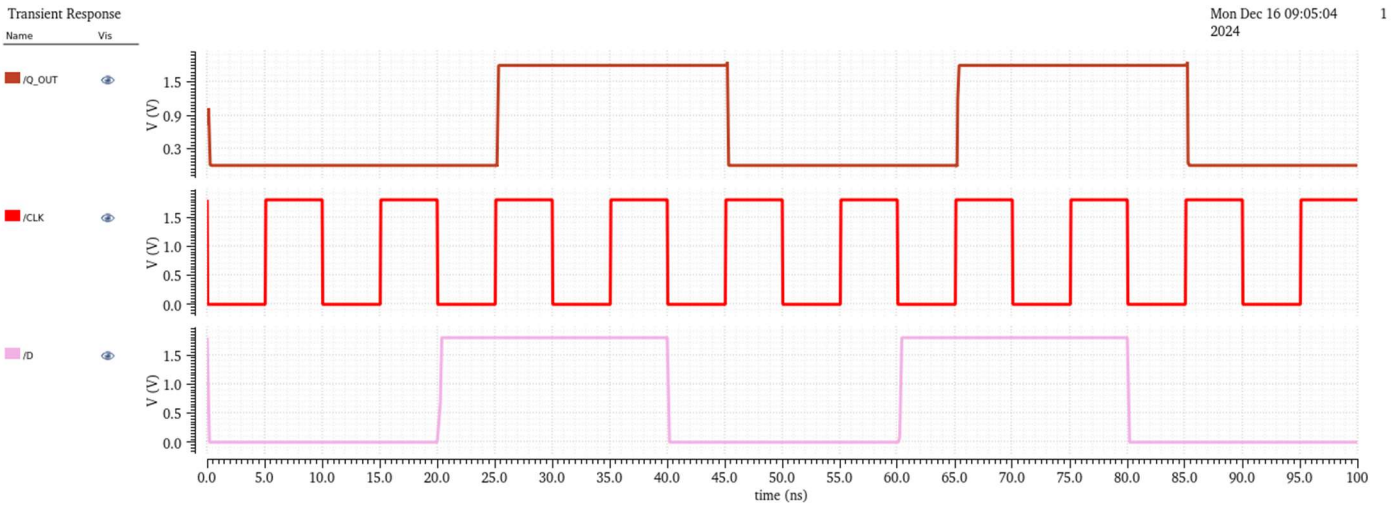
Optimizing the power consumption of flip-flops (FFs), as fundamental components of digital systems, can significantly enhance overall system efficiency. This article presents an energy-efficient retentive true-single-phase-clocked (TSPC) FF. By employing an input-aware precharge scheme, the proposed TSPC FF selectively precharges only when required, minimizing unnecessary power usage. Additionally, floating node analysis and transistor-level optimization are implemented to achieve high energy efficiency without substantial area overhead. Simulations and measurements based on advanced CMOS technology validate the design, demonstrating significant reductions in power consumption compared to conventional transmission-gate flip-flops (TGFF), particularly at low data activity levels. Furthermore, the proposed FF achieves reduced CK-to-Q delay compared to TGFF, highlighting its superior performance in energy efficiency and speed.

Index Terms— Flip-flop (FF), low voltage operation, low-power, cadence 180nm, true-single-phase-clocked (TSPC).

CIRCUIT DIAGRAM :



OUTPUT WAVEFORM :



CONCLUTION :

In this article, an energy-efficient retentive TSPC FF is proposed. By removing redundant precharge and discharge operations with the input-aware precharge scheme, the power of the proposed FF is greatly reduced. Furthermore, floating node analysis is applied to the proposed structure to avoid the generation of short-circuit paths. Then, transistor level optimizations are applied to the circuit to further reduce the area and power consumption. Postlayout simulation results show that the proposed FF saves more than 80% power consumption compared with TGFF under 10% data activity.Measurement results of ten test chips also demonstrate that the proposed FF has a significant energy efficiency improvement compared with TGFF. The CK-to-Q delay of the proposed FF is 26.18% lower than that of TGFF. The area of the proposed FF is just 4.8% larger than that of TGFF, indicating little area overhead to achieve such benefits.

.

REFERENCE :

1. *L. Atzori, A. Iera, and G. Morabito, "The Internet of Things: A survey," Computer Networks, vol. 54, no. 15, pp. 2787–2805, Oct. 2010.*
2. *T. Tekeste, H. Saleh, B. Mohammad, A. Khandoker, and M. Ismail, "A nano-watt ECG feature extraction engine in 65-nm technology," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 8, pp. 1099–1103, Aug. 2018.*
3. *T. Tekeste, H. Saleh, B. Mohammad, and M. Ismail, "Ultra-low power QRS detection and ECG compression architecture for IoT healthcare devices," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 2, pp. 669–679, Feb. 2019.*
4. *A. Pullini, D. Rossi, I. Loi, G. Tagliavini, and L. Benini, "Mr. Wolf: An energy-precision scalable parallel ultra-low-power SoC for IoT edge processing," IEEE Journal of Solid-State Circuits, vol. 54, no. 7, pp. 1970–1981, Jul. 2019.*
5. *J. P. Cerqueira, T. J. Repetti, Y. Pu, S. Priyadarshi, M. A. Kim, and M. Seok, "Catena: A near-threshold, sub-0.4-mW, 16-core programmable spatial array accelerator for ultralow-power mobile and embedded Internet of Things," IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2270–2284, Aug. 2020.*
6. *J. L. Shin et al., "The next generation 64b SPARC core in a T4 SoC processor," IEEE Journal of Solid-State Circuits, vol. 48, no. 1, pp. 82–90, Jan. 2013.*
7. *L. Moreau, R. Dekimpe, and D. Bol, "A 0.4 V 0.5 fJ/cycle TSPC flip-flop in 65 nm LP CMOS with retention mode controlled by clock-gating cells," in Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), May 2019, pp. 1–4.*
8. *A. Andrei, P. Eles, O. Jovanovic, M. Schmitz, J. Ogniewski, and Z. Peng, "Quasi-static voltage scaling for energy minimization with time constraints," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 1, pp. 10–23, Jan. 2011.*
9. *X. Zhang et al., "32-bit×32-bit multiprecision Razor-based dynamic voltage scaling*

multiplier with operands scheduler," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 4, pp. 759–770, Apr. 2014.

10. *W.-J. Tsou et al., "Digital low-dropout regulator with anti-PVT-variation technique for dynamic voltage scaling and adaptive voltage scaling multicore processor," in IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, Feb. 2017, pp. 338–339.*
11. *S. Jain, L. Lin, and M. Alioto, "Dynamically adaptable pipeline for energy-efficient microarchitectures under wide voltage scaling," IEEE Journal of Solid-State Circuits, vol. 53, no. 2, pp. 632–641, Feb. 2018.*
12. *J. Lee et al., "A self-tuning IoT processor using leakage-ratio measurement for energy-optimal operation," IEEE Journal of Solid-State Circuits, vol. 55, no. 1, pp. 87–97, Jan. 2020.*