|  |  |
| --- | --- |
| Name: Sohaib Liaquat | EE-272L Digital Systems Design |
| Reg. No.: 2023-EE-061 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Manual 3**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization (CLO1) | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation (CLO2) | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA (CLO2) | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

**Tasks:**

(a) Truth table of circuit:

Table 1. Expanded truth table of the circuit

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Input | Input | Input | NOT | OR 1,2 | NAND | XOR 1 (Output) | XOR 2 | AND (Output) |
|  |  |  |  |  |  |  | ( |  |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |

Table 2. Truth table of the circuit

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

(b) Maximum combinational delay in Synthesis:

Path 1 from ‘a’ to ‘y’ has the maximum delay i.e. **6.850 ns**.

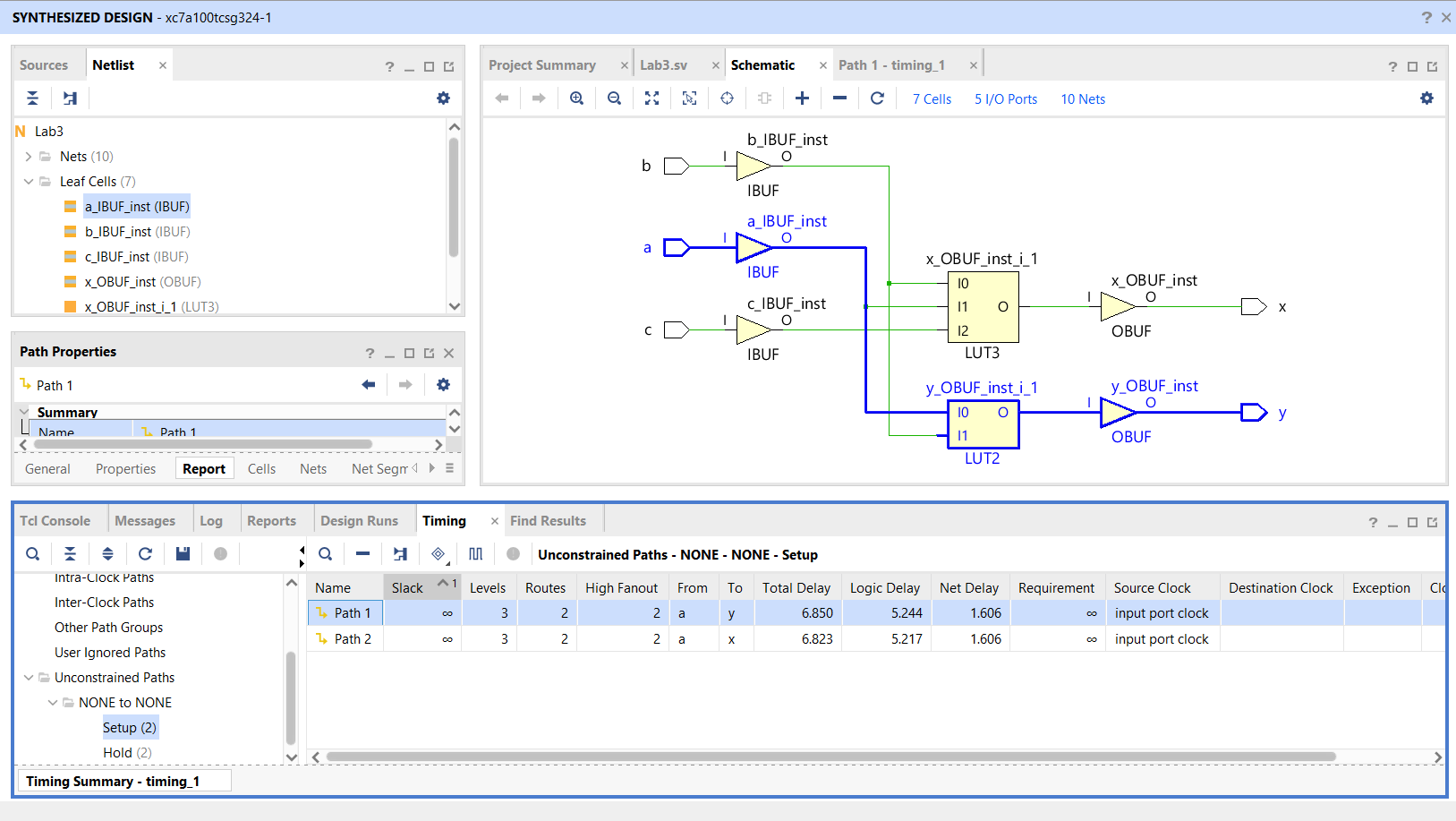
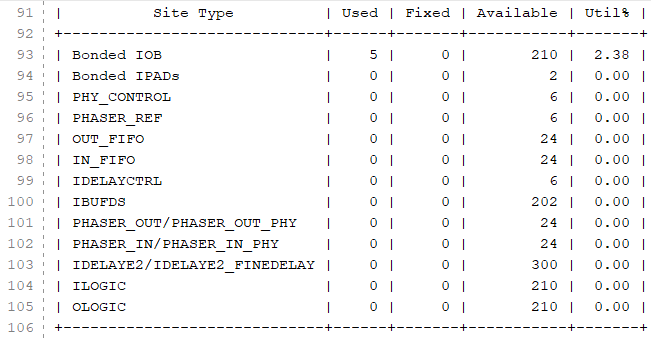
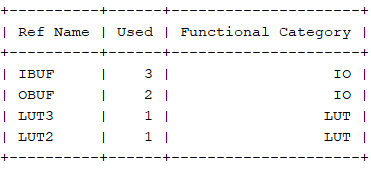
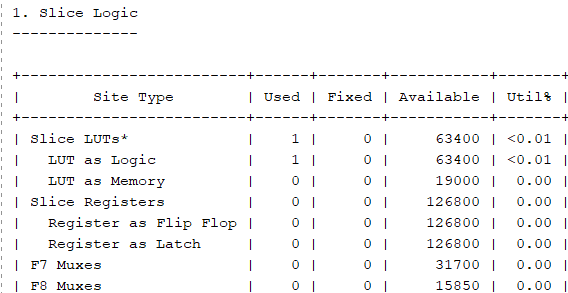
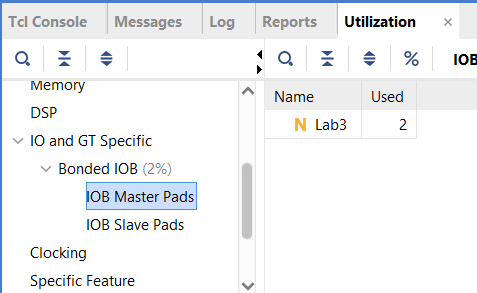


Fig 1. Maximum combinational delay in synthesis

(c) Resource Utilization:





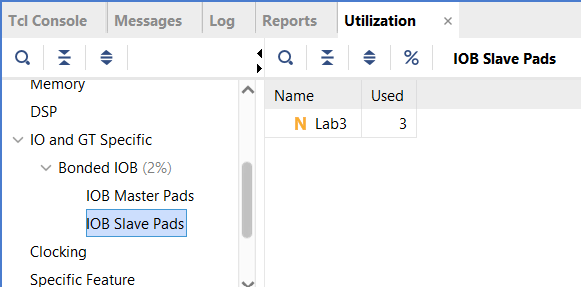


Fig 2. Resource utilization. Look up tables, input, and output ports

**APPENDIX**

* System Verilog Code:

module Lab3(

    input  logic a,

    input  logic b,

    input  logic c,

    output logic x,

    output logic y

    );

    //-----Local Signals-----//

    logic not\_out;

    logic or\_1\_out;

    logic nand\_out;

    logic or\_2\_out;

    logic xor\_out;

    //-----Circuit Description-----//

    assign not\_out = ~c;

    assign or\_1\_out = a | b;

    assign nand\_out = ~(a & b);

    assign or\_2\_out = a | b;

    assign xor\_out = nand\_out ^ or\_2\_out;

    //-----Output Signals-----//

    assign x = not\_out ^ or\_1\_out;

    assign y = or\_1\_out & xor\_out;

endmodule

* Constraint file Code:

# Outputs (LEDs)

set\_property -dict { PACKAGE\_PIN V12 IOSTANDARD LVCMOS33 } [get\_ports { y }]; #IO\_L20N\_T3\_A07\_D23\_14 Sch=led[14]

set\_property -dict { PACKAGE\_PIN V11 IOSTANDARD LVCMOS33 } [get\_ports { x }]; #IO\_L21N\_T3\_DQS\_A06\_D22\_14 Sch=led[15]

# Inputs (Switches)

set\_property -dict { PACKAGE\_PIN V10 IOSTANDARD LVCMOS33 } [get\_ports { a }]; #IO\_L21P\_T3\_DQS\_14 Sch=sw[15]

set\_property -dict { PACKAGE\_PIN U11 IOSTANDARD LVCMOS33 } [get\_ports { b }]; #IO\_L19N\_T3\_A09\_D25\_VREF\_14 Sch=sw[14]

set\_property -dict { PACKAGE\_PIN U12 IOSTANDARD LVCMOS33 } [get\_ports { c }]; #IO\_L20P\_T3\_A08\_D24\_14 Sch=sw[13]

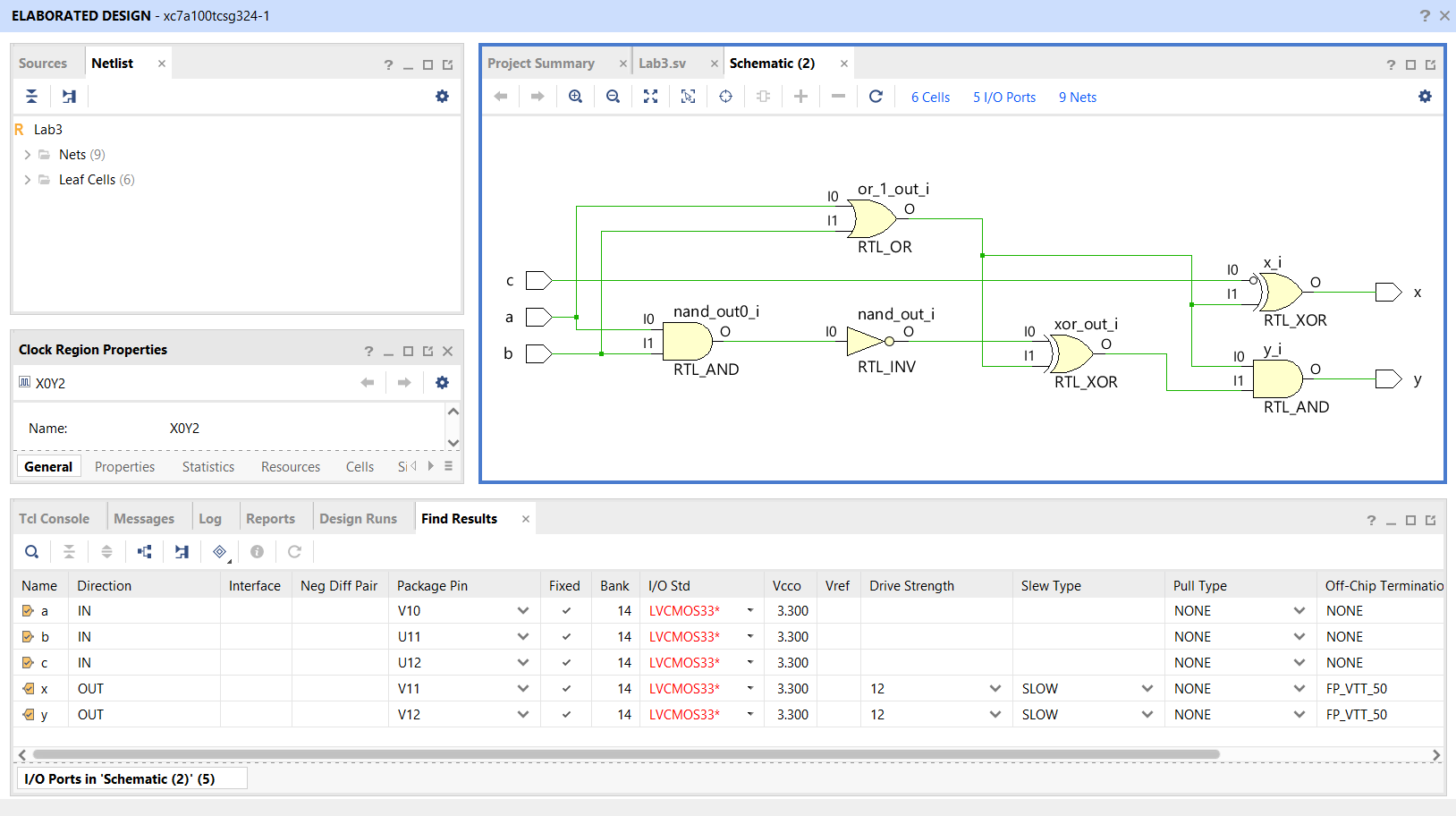
* RTL schematic:

Fig 3. RTL Schematic for the given circuit.