



NAND Flash Memory

MT29F128G08CB[C/E]AB, MT29F256G08CE[C/E]AB

MT29F512G08C[K/M][C/E]AB, MT29F1T08CU[C/E]AB

Features

- Open NAND Flash Interface (ONFI) 3.0-compliant¹
- JEDEC NAND Flash Interface Interoperability (JESD230) compliant
- Multiple-level cell (MLC) technology
- Organization
 - Page size x8: 17,600 bytes (16,384 + 1216 bytes)
 - Block size: 512 pages (8192K + 608K bytes)
 - Plane size: 2 planes x 1024 blocks per plane
 - Device size: 128Gb: 2048 blocks;
256Gb: 4096 blocks;
512Gb: 8192 blocks;
1Tb: 16,384 blocks
- NV-DDR2 I/O performance
 - Up to NV-DDR2 timing mode 6²
 - Clock rate: 6ns (NV-DDR2)
 - Read/write throughput per pin: 333 MT/s
- NV-DDR I/O performance
 - Up to NV-DDR timing mode 5³
 - Clock rate: 10ns (NV-DDR)
 - Read/write throughput per pin: 200 MT/s
- Asynchronous I/O performance
 - Up to asynchronous timing mode 5
 - t_{RC}/t_{WC} : 20ns (MIN)
 - Read/write throughput per pin: 50 MT/s
- Array performance
 - Read page: 115 μ s (MAX)
 - Program page: 1600 μ s (TYP)
 - Erase block: 3ms (TYP)
- Operating Voltage Range
 - V_{CC} : 2.7–3.6V
 - V_{CCQ} : 1.7–1.95V, 2.7V–3.6V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set
 - Program cache
 - Read cache sequential
 - Read cache random
 - One-time programmable (OTP) mode
 - Multi-plane commands
 - Multi-LUN operations
 - Read Unique ID
 - Copyback

- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management (page 153).
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
 - Operation completion
 - Pass/fail condition
 - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the NV-DDR/NV-DDR2 interface
- Copyback operations supported within the plane from which data is read
- Quality and reliability
 - Data retention: JESD47 compliant; see qualification report
 - Endurance: 3000 PROGRAM/ERASE cycles
- Operating temperature:
 - Commercial: 0°C to +70°C
 - Industrial (IT): –40°C to +85°C
- Package
 - 152-ball BGA

- Notes:
1. The ONFI 3.0 specification is available at www.onfi.org.
 2. 1.8V V_{CCQ} up to NV-DDR2 timing mode 6 for 333MT/s. 3.3V V_{CCQ} up to NV-DDR2 timing mode 3 for 166MT/s.
 3. 1.8V V_{CCQ} up to NV-DDR timing mode 5 for 200MT/s. 3.3V V_{CCQ} up to NV-DDR timing mode 4 for 166MT/s.

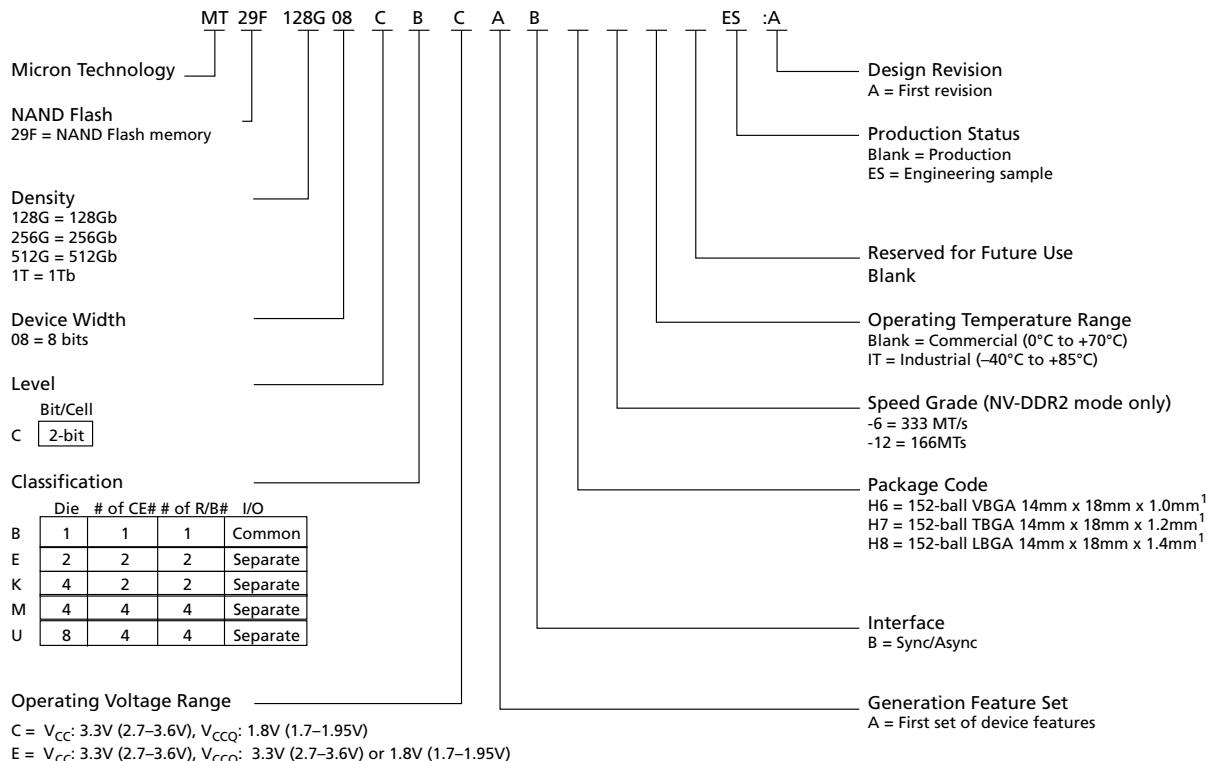
Release: 3/26/13



Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Numbering



Release: 3/26/13

Note: 1. Pb-free package.



Contents

General Description	12
Asynchronous, NV-DDR, and NV-DDR2 Signal Descriptions	12
Signal Assignments	14
Package Dimensions	15
Architecture	18
Device and Array Organization	19
Bus Operation – Asynchronous Interface	24
Asynchronous Enable/Standby	24
Asynchronous Bus Idle	24
Asynchronous Pausing Data Input/Output	25
Asynchronous Commands	25
Asynchronous Addresses	26
Asynchronous Data Input	27
Asynchronous Data Output	28
Write Protect	29
Ready/Busy#	29
Bus Operation – NV-DDR Interface	34
NV-DDR Enable/Standby	35
NV-DDR Bus Idle/Driving	35
NV-DDR Pausing Data Input/Output	36
NV-DDR Commands	36
NV-DDR Addresses	37
NV-DDR DDR Data Input	38
NV-DDR Data Output	39
Write Protect	41
Ready/Busy#	41
Bus Operation – NV-DDR2 Interface	42
Differential Signaling	43
Warmup Cycles	43
On-die Termination (ODT)	44
Self-termination On-die Termination (ODT)	45
Matrix Termination	46
Matrix Termination Examples	49
NV-DDR2 Standby	54
NV-DDR2 Idle	55
NV-DDR2 Pausing Data Input/Output	55
NV-DDR2 Commands	55
NV-DDR2 Addresses	56
NV-DDR2 Data Input	57
NV-DDR2 Data Output	58
Write Protect	59
Ready/Busy#	59
Device Initialization	60
V _{PP} Initialization	62
Activating Interfaces	63
Activating the Asynchronous Interface	63
Activating the NV-DDR Interface	63
Activating the NV-DDR2 Interface	63
CE# Pin Reduction and Volume Addressing	65
Initialization Sequence	67

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Features

Volume Appointment Without CE# Pin Reduction	68
Appointing Volume Addresses	69
Selecting a Volume	69
Multiple Volume Operation Restrictions	69
Volume Reversion	70
Command Definitions	72
Reset Operations	75
RESET (FFh)	75
SYNCHRONOUS RESET (FCh)	76
RESET LUN (FAh)	77
Identification Operations	78
READ ID (90h)	78
READ ID Parameter Tables	79
READ PARAMETER PAGE (ECh)	80
Parameter Page Data Structure Tables	82
READ UNIQUE ID (EDh)	100
Configuration Operations	101
SET FEATURES (EFh)	101
GET FEATURES (EEh)	102
VOLUME SELECT (E1h)	109
ODT CONFIGURE (E2h)	111
Status Operations	114
READ STATUS (70h)	115
READ STATUS ENHANCED (78h)	116
Column Address Operations	117
CHANGE READ COLUMN (05h-E0h)	117
CHANGE READ COLUMN ENHANCED (06h-E0h)	118
CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation	119
CHANGE WRITE COLUMN (85h)	120
CHANGE ROW ADDRESS (85h)	121
Read Operations	123
READ MODE (00h)	125
READ PAGE (00h-30h)	126
READ PAGE CACHE SEQUENTIAL (31h)	127
READ PAGE CACHE RANDOM (00h-31h)	128
READ PAGE CACHE LAST (3Fh)	130
READ PAGE MULTI-PLANE (00h-32h)	131
Read Retry Operations	133
Program Operations	135
PROGRAM PAGE (80h-10h)	135
PROGRAM PAGE CACHE (80h-15h)	137
PROGRAM PAGE MULTI-PLANE (80h-11h)	139
Erase Operations	141
ERASE BLOCK (60h-D0h)	141
ERASE BLOCK MULTI-PLANE (60h-D1h)	142
ERASE BLOCK MULTI-PLANE (60h-60h-D0h)	142
Copyback Operations	143
COPYBACK READ (00h-35h)	144
COPYBACK PROGRAM (85h-10h)	145
COPYBACK READ MULTI-PLANE (00h-32h)	145
COPYBACK PROGRAM MULTI-PLANE (85h-11h)	146
One-Time Programmable (OTP) Operations	147

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Features

PROGRAM OTP PAGE (80h-10h)	148
PROTECT OTP AREA (80h-10h)	149
READ OTP PAGE (00h-30h)	150
Multi-Plane Operations	151
Multi-Plane Addressing	151
Interleaved Die (Multi-LUN) Operations	152
Error Management	153
Shared Pages	154
Output Drive Impedance	158
AC Overshoot/Undershoot Specifications	161
Input Slew Rate	163
Output Slew Rate	170
Power Cycle Requirements	172
Electrical Specifications	173
Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)	175
Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)	175
Electrical Specifications – DC Characteristics and Operating Conditions (V _{CCQ})	176
Single-Ended Requirements for Differential signals	178
Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)	180
Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)	182
Electrical Specifications – Array Characteristics	195
Asynchronous Interface Timing Diagrams	196
NV-DDR Interface Timing Diagrams	207
NV-DDR2 Interface Timing Diagrams	229
Revision History	252
Rev. G – 3/13	252
Rev. F – 2/13	252
Rev. E – 8/12	252
Rev. D – 2/12	253
Rev. C – 12/11	253
Rev. B – 8/11	254
Rev. A – 7/11	254

Release: 3/26/13



List of Tables

Table 1: Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions	12
Table 2: Array Addressing for Logical Unit (LUN)	23
Table 3: Asynchronous Interface Mode Selection	24
Table 4: NV-DDR Interface Mode Selection	34
Table 5: NV-DDR2 Interface Mode Selection	42
Table 6: On-die Termination DC Electrical Characteristics	45
Table 7: LUN state for Matrix Termination	47
Table 8: Volume appointment for Matrix Termination example	49
Table 9: Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example	50
Table 10: Parallel Non-Target ODT settings configuration example	53
Table 11: Command Set	72
Table 12: Read ID Parameters for Address 00h	79
Table 13: Read ID Parameters for Address 20h	79
Table 14: Read ID Parameters for Address 40h	79
Table 15: ONFI Parameter Page Data Structure	82
Table 16: JEDEC Parameter Page Defintion	92
Table 17: Feature Address Definitions	101
Table 18: Feature Address 01h: Timing mode	103
Table 19: Feature Address 02h: NV-DDR2 configuration	104
Table 20: Feature Address 30h: V _{PP}	105
Table 21: Feature Address 58h: Volume configuration	106
Table 22: Feature Addresses 10h and 80h: Programmable Output Drive Strength	106
Table 23: Feature Address 81h: Programmable R/B# Pull-Down Strength	107
Table 24: Feature Addresses 89h: Read Retry	107
Table 25: Feature Address 90h: Array Operation Mode	108
Table 26: Volume Address	110
Table 27: ODT Configuration Matrix	111
Table 28: Status Register Definition	114
Table 29: OTP Area Details	148
Table 30: Error Management Details	153
Table 31: Shared Pages	154
Table 32: Output Drive Strength Conditions (V _{CCQ} = 1.7–1.95V)	158
Table 33: Output Drive Strength Impedance Values (V _{CCQ} = 1.7–1.95V)	158
Table 34: Output Drive Strength Conditions (V _{CCQ} = 2.7–3.6V)	159
Table 35: Output Drive Strength Impedance Values (V _{CCQ} = 2.7–3.6V)	159
Table 36: Pull-Up and Pull-Down Output Impedance Mismatch for Asynchronous and NV-DDR	160
Table 37: Pull-Up and Pull-Down Output Impedance Mismatch for NV-DDR2	160
Table 38: Aynchronous Overshoot/Undershoot Parameters	161
Table 39: NV-DDR Overshoot/Undershoot Parameters	161
Table 40: NV-DDR2 Overshoot/Undershoot Parameters	161
Table 41: Test Conditions for Input Slew Rate	163
Table 42: NV-DDR Maximum and Minimum Input Slew Rate	163
Table 43: Input Slew Rate derating for NV-DDR (V _{CCQ} = 1.7–1.95V)	163
Table 44: Input Slew Rate derating for NV-DDR/NV-DDR2 (V _{CCQ} = 2.7–3.6V)	164
Table 45: NV-DDR2 Maximum and Minimum Input Slew Rate	164
Table 46: Input Slew Rate derating for NV-DDR2 single-ended (V _{CCQ} = 1.7–1.95V)	165
Table 47: Input Slew Rate derating for NV-DDR2 differential (V _{CCQ} = 1.7–1.95V)	165
Table 48: Test Conditions for Output Slew Rate	170
Table 49: Output Slew Rate for Asynchronous and NV-DDR (V _{CCQ} = 2.7–3.6V)	170
Table 50: Output Slew Rate for Single-Ended NV-DDR or NV-DDR2 (V _{CCQ} = 1.7–1.95V)	170

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Features

Table 51: Output Slew Rate for Differential NV-DDR2 ($V_{CCQ} = 1.7\text{-}1.95$)	171
Table 52: Output Slew Rate Matching Ratio for NV-DDR2	171
Table 53: Power Cycle Requirements	172
Table 54: Absolute Maximum Ratings by Device	173
Table 55: Recommended Operating Conditions	173
Table 56: Valid Blocks per LUN	173
Table 57: Capacitance: 152-Ball BGA Package	174
Table 58: Test Conditions	174
Table 59: DC Characteristics and Operating Conditions (Asynchronous Interface)	175
Table 60: DC Characteristics and Operating Conditions (NV-DDR and NV-DDR2 Interface)	175
Table 61: Asynchronous/NV-DDR DC Characteristics and Operating Conditions (3.3VV _{CCQ})	176
Table 62: Asynchronous/NV-DDR DC Characteristics and Operating Conditions (1.8VV _{CCQ})	176
Table 63: NV-DDR2 DC Characteristics and Operating Conditions for Single-Ended signals (1.8VV _{CCQ})	177
Table 64: NV-DDR2 DC Characteristics and Operating Conditions for Differential signals(1.8VV _{CCQ})	178
Table 65: Single-Ended Levels for RE _t , RE _c , DQS _t , DQS _c (1.8VV _{CCQ})	179
Table 66: Differential AC Input/Ouput Parameters	179
Table 67: AC Characteristics: Asynchronous Command, Address, and Data	180
Table 68: AC Characteristics: NV-DDR Command, Address, and Data	182
Table 69: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0 - 4	185
Table 70: AC Characteristics: NV-DDR2 Command, Address, and Data for timing modes 5 - 7	190
Table 71: Array Characteristics	195

Release: 3/26/13



List of Figures

Figure 1: Part Numbering	2
Figure 2: 152-Ball BGA (Ball-Down, Top View)	14
Figure 3: 152-Ball VBGA – 14mm x 18mm (Package Code: H6)	15
Figure 4: 152-Ball TBGA – 14mm x 18mm (Package Code: H7)	16
Figure 5: 152-Ball LBGA – 14mm x 18mm (Package Code: H8)	17
Figure 6: NAND Flash Die (LUN) Functional Block Diagram	18
Figure 7: Device Organization for Single-Die Package (BGA)	19
Figure 8: Device Organization for Two-Die Package (BGA)	19
Figure 9: Device Organization for Four-Die Package with two CE# (BGA)	20
Figure 10: Device Organization for Four-Die Package with four CE# (BGA)	21
Figure 11: Device Organization for Eight-Die Package (BGA)	22
Figure 12: Array Organization per Logical Unit (LUN)	23
Figure 13: Asynchronous Command Latch Cycle	25
Figure 14: Asynchronous Address Latch Cycle	26
Figure 15: Asynchronous Data Input Cycles	27
Figure 16: Asynchronous Data Output Cycles	28
Figure 17: Asynchronous Data Output Cycles (EDO Mode)	29
Figure 18: READ/BUSY# Open Drain	30
Figure 19: tFall and tRise ($V_{CCQ} = 2.7\text{-}3.6V$)	31
Figure 20: tFall and tRise ($V_{CCQ} = 1.7\text{-}1.95V$)	31
Figure 21: IOL vs Rp ($V_{CCQ} = 2.7\text{-}3.6V$)	32
Figure 22: IOL vs Rp ($V_{CCQ} = 1.7\text{-}1.95V$)	32
Figure 23: TC vs Rp	33
Figure 24: NV-DDR Bus Idle/Driving Behavior	36
Figure 25: NV-DDR Command Cycle	37
Figure 26: NV-DDR Address Cycle	38
Figure 27: NV-DDR Data Input Cycles	39
Figure 28: NV-DDR Data Output Cycles	41
Figure 29: Warmup Cycles for data output (2 warmup cycles)	44
Figure 30: Self-termination only ODT behavioral flow	46
Figure 31: ODT actions for LUNs on selected Volume	48
Figure 32: ODT actions for LUNs in Sniff state on unselected Volume	49
Figure 33: Non-Target ODT for Data Output, Target ODT for Data Input configuration example	52
Figure 34: Parallel Non-Target ODT configuration example	54
Figure 35: NV-DDR2 Command Cycle	56
Figure 36: NV-DDR2 Addresses Cycle	57
Figure 37: NV-DDR2 Data Input Cycles	58
Figure 38: NV-DDR2 Data Output Cycles	59
Figure 39: R/B# Power-On Behavior	60
Figure 40: Activating Interfaces	64
Figure 41: CE# Pin Reduction Topology with Single Channel	66
Figure 42: CE# Pin Reduction and Volume Addressing Topology with Dual Channel	66
Figure 43: Example of Sequential Reset Initialization	68
Figure 44: Volume Addressing Without CE# Pin Reduction Topology with Dual Channel	69
Figure 45: Volume Reversion behavioral flow	71
Figure 46: RESET (FFh) Operation	75
Figure 47: SYNCHRONOUS RESET (FCh) Operation	76
Figure 48: RESET LUN (FAh) Operation	77
Figure 49: READ ID (90h) with 00h Address Operation	78
Figure 50: READ ID (90h) with 20h Address Operation	78

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Features

Figure 51: READ ID (90h) with 40h Address Operation	78
Figure 52: READ PARAMETER (ECh) with 00h Address Operation for ONFI	80
Figure 53: READ PARAMETER (ECh) with 40h Address Operation for JEDEC	81
Figure 54: READ UNIQUE ID (EDh) Operation	100
Figure 55: SET FEATURES (EFh) Operation	102
Figure 56: GET FEATURES (EEh) Operation	102
Figure 57: VOLUME SELECT (E1h) Operation	109
Figure 58: ODT CONFIGURE (E2h) Operation	111
Figure 59: READ STATUS (70h) Operation	116
Figure 60: READ STATUS ENHANCED (78h) Operation	116
Figure 61: CHANGE READ COLUMN (05h-E0h) Operation	117
Figure 62: CHANGE READ COLUMN ENHANCED (06h-E0h) Operation	118
Figure 63: CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation	119
Figure 64: CHANGE WRITE COLUMN (85h) Operation	120
Figure 65: CHANGE ROW ADDRESS (85h) Operation	122
Figure 66: READ PAGE (00h-30h) Operation	126
Figure 67: READ PAGE CACHE SEQUENTIAL (31h) Operation	127
Figure 68: READ PAGE CACHE RANDOM (00h-31h) Operation	129
Figure 69: READ PAGE CACHE LAST (3Fh) Operation	130
Figure 70: READ PAGE MULTI-PLANE (00h-32h) Operation	132
Figure 71: Read Retry Flow Chart	134
Figure 72: PROGRAM PAGE (80h-10h) Operation	136
Figure 73: PROGRAM PAGE CACHE (80h-15h) Operation (Start)	138
Figure 74: PROGRAM PAGE CACHE (80h-15h) Operation (End)	138
Figure 75: PROGRAM PAGE MULTI-PLANE (80h-11h) Operation	140
Figure 76: ERASE BLOCK (60h-D0h) Operation	141
Figure 77: ERASE BLOCK MULTI-PLANE (60h-D1h) Operation	142
Figure 78: ERASE BLOCK MULTI-PLANE (60h-60h-D0h) Operation	142
Figure 79: COPYBACK READ (00h-35h) Operation	144
Figure 80: COPYBACK READ (00h-35h) with CHANGE READ COLUMN (05h-E0h) Operation	144
Figure 81: COPYBACK PROGRAM (85h-10h) Operation	145
Figure 82: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation	145
Figure 83: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation	146
Figure 84: PROGRAM OTP PAGE (80h-10h) Operation	148
Figure 85: PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation	149
Figure 86: PROTECT OTP AREA (80h-10h) Operation	150
Figure 87: READ OTP PAGE (00h-30h) Operation	150
Figure 88: Overshoot	162
Figure 89: Undershoot	162
Figure 90: Nominal Slew Rate for Data Setup Time (t_{DS}), NV-DDR2 only	166
Figure 91: Tangent Line for Data Setup Time (t_{DS}), NV-DDR2 only	167
Figure 92: Nominal Slew Rate for Data Hold Time (t_{DH}), NV-DDR2 only	168
Figure 93: Tangent Line for Data Hold Time (t_{DH}), NV-DDR2 only	169
Figure 94: Single-Ended requirements for Differential Signals	179
Figure 95: RESET Operation	196
Figure 96: RESET LUN Operation	196
Figure 97: READ STATUS Cycle	197
Figure 98: READ STATUS ENHANCED Cycle	197
Figure 99: READ PARAMETER PAGE	198
Figure 100: READ PAGE	198
Figure 101: READ PAGE Operation with CE# “Don’t Care”	199
Figure 102: CHANGE READ COLUMN	200

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Features

Figure 103: READ PAGE CACHE SEQUENTIAL	201
Figure 104: READ PAGE CACHE RANDOM	202
Figure 105: READ ID Operation	203
Figure 106: PROGRAM PAGE Operation	203
Figure 107: PROGRAM PAGE Operation with CE# “Don’t Care”	204
Figure 108: PROGRAM PAGE Operation with CHANGE WRITE COLUMN	204
Figure 109: PROGRAM PAGE CACHE	205
Figure 110: PROGRAM PAGE CACHE Ending on 15h	205
Figure 111: COPYBACK	206
Figure 112: ERASE BLOCK Operation	206
Figure 113: SET FEATURES Operation	207
Figure 114: READ ID Operation	208
Figure 115: GET FEATURES Operation	209
Figure 116: RESET (FCh) Operation	210
Figure 117: READ STATUS Cycle	211
Figure 118: READ STATUS ENHANCED Operation	212
Figure 119: READ PARAMETER PAGE Operation	213
Figure 120: READ PAGE Operation	214
Figure 121: CHANGE READ COLUMN	215
Figure 122: READ PAGE CACHE SEQUENTIAL (1 of 2)	216
Figure 123: READ PAGE CACHE SEQUENTIAL (2 of 2)	217
Figure 124: READ PAGE CACHE RANDOM (1 of 2)	218
Figure 125: READ PAGE CACHE RANDOM (2 of 2)	218
Figure 126: Multi-Plane Read Page (1 of 2)	219
Figure 127: Multi-Plane Read Page (2 of 2)	220
Figure 128: PROGRAM PAGE Operation (1 of 2)	221
Figure 129: PROGRAM PAGE Operation (2 of 2)	221
Figure 130: CHANGE WRITE COLUMN	222
Figure 131: Multi-Plane Program Page	223
Figure 132: ERASE BLOCK	224
Figure 133: COPYBACK (1 of 3)	224
Figure 134: COPYBACK (2 of 3)	225
Figure 135: COPYBACK (3 of 3)	225
Figure 136: READ OTP PAGE	226
Figure 137: PROGRAM OTP PAGE (1 of 2)	227
Figure 138: PROGRAM OTP PAGE (2 of 2)	227
Figure 139: PROTECT OTP AREA	228
Figure 140: SET FEATURES Operation	229
Figure 141: READ ID Operation	230
Figure 142: GET FEATURES Operation	231
Figure 143: RESET (FCh) Operation	232
Figure 144: READ STATUS Cycle	233
Figure 145: READ STATUS ENHANCED Operation	234
Figure 146: READ PARAMETER PAGE Operation	235
Figure 147: READ PAGE Operation	236
Figure 148: CHANGE READ COLUMN	237
Figure 149: READ PAGE CACHE SEQUENTIAL (1 of 2)	238
Figure 150: READ PAGE CACHE SEQUENTIAL (2 of 2)	239
Figure 151: READ PAGE CACHE RANDOM (1 of 2)	240
Figure 152: READ PAGE CACHE RANDOM (2 of 2)	240
Figure 153: Multi-Plane Read Page (1 of 2)	241
Figure 154: Multi-Plane Read Page (2 of 2)	242

Release: 3/26/13

**128Gb to 1Tb Asynchronous/Synchronous NAND Features**

Figure 155: PROGRAM PAGE Operation (1 of 2)	243
Figure 156: PROGRAM PAGE Operation (2 of 2)	243
Figure 157: CHANGE WRITE COLUMN	244
Figure 158: Multi-Plane Program Page	245
Figure 159: ERASE BLOCK	246
Figure 160: COPYBACK (1 of 3)	247
Figure 161: COPYBACK (2 of 3)	247
Figure 162: COPYBACK (3 of 3)	248
Figure 163: READ OTP PAGE	249
Figure 164: PROGRAM OTP PAGE (1 of 2)	250
Figure 165: PROGRAM OTP PAGE (2 of 2)	250
Figure 166: PROTECT OTP AREA	251

Release: 3/26/13



General Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

Some versions of this Micron NAND Flash device additionally includes a NV-DDR and/or a NV-DDR2 data interface for high-performance I/O operations. When the NV-DDR interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

Asynchronous, NV-DDR, and NV-DDR2 Signal Descriptions

Table 1: Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions

Asynchronous Signal ¹	NV-DDR Signal ¹	NV-DDR2 Signal ¹	Type	Description ²
ALE	ALE	ALE	Input	Address latch enable: Loads an address from DQx into the address register.
CE#	CE#	CE#	Input	Chip enable: Enables or disables one or more die (LUNs) in a target.
CLE	CLE	CLE	Input	Command latch enable: Loads a command from DQx into the command register.
DQx	DQx	DQx	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and command information.
-	DQS	DQS, DQS_t	I/O	Data strobe: Provides a synchronous reference for data input and output.
-	-	DQS_c	I/O	Data strobe compliment: Provides a complementary signal to the data strobe signal optionally used in the NV-DDR2 interface for synchronous reference for data input and output.
ENi	ENi	ENi	Input	Enumerate input: Input to a NAND device (if first NAND device on the daisy chain have as NC) from ENo of a previous NAND device to support CE# pin reduction functionality.
ENO	ENO	ENO	Output	Enumerate output: Output from a NAND device to the ENi of the next NAND device in the daisy chain to support CE# pin reduction functionality.



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous, NV-DDR, and NV-DDR2 Signal Descriptions

Table 1: Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions (Continued)

Asyncho- nous Signal ¹	NV-DDR Sig- nal ¹	NV-DDR2 Sig- nal ¹	Type	Description ²
RE#	W/R#	RE#, RE_t	Input	Read enable and write/read: RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the NV-DDR interface is active, W/R# controls the direction of DQx and DQS.
-	-	RE_c	Input	Read enable complement: Provides a complementary signal to the read enable signal optionally used in the NV-DDR2 interface for synchronous reference for data output.
WE#	CLK	WE#	Input	Write enable and clock: WE# transfers commands, addresses when the asynchronous and NV-DDR2 interfaces are active, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the NV-DDR interface is active, CLK latches command and address cycles.
WP#	WP#	WP#	Input	Write protect: Enables or disables array PROGRAM and ERASE operations.
R/B#	R/B#	R/B#	Output	Ready/busy: An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V _{CC}	V _{CC}	V _{CC}	Supply	V_{CC}: Core power supply
V _{CCQ}	V _{CCQ}	V _{CCQ}	Supply	V_{CCQ}: I/O power supply
V _{PP}	V _{PP}	V _{PP}	Supply	V_{PP}: The V _{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance operations (e.g., improved power efficiency).
V _{SS}	V _{SS}	V _{SS}	Supply	V_{SS}: Core ground connection
V _{SSQ}	V _{SSQ}	V _{SSQ}	Supply	V_{SSQ}: I/O ground connection
-	-	V _{REFQ}	Supply	V_{REFQ}: Reference voltage used with NV-DDR2 interface
NC	NC	NC	-	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU	DNU	-	Do not use: DNUs must be left unconnected.
RFU	RFU	RFU	-	Reserved for future use: RFUs must be left unconnected.

- Notes:
1. See Device and Array Organization for detailed signal connections.
 2. See Bus Operation - Asynchronous Interface, Bus Operation – NV-DDR Interface (page 34), and Bus Operation – NV-DDR2 Interface (page 42) for detailed asynchronous, NV-DDR, and NV-DDR2 interface signal descriptions.

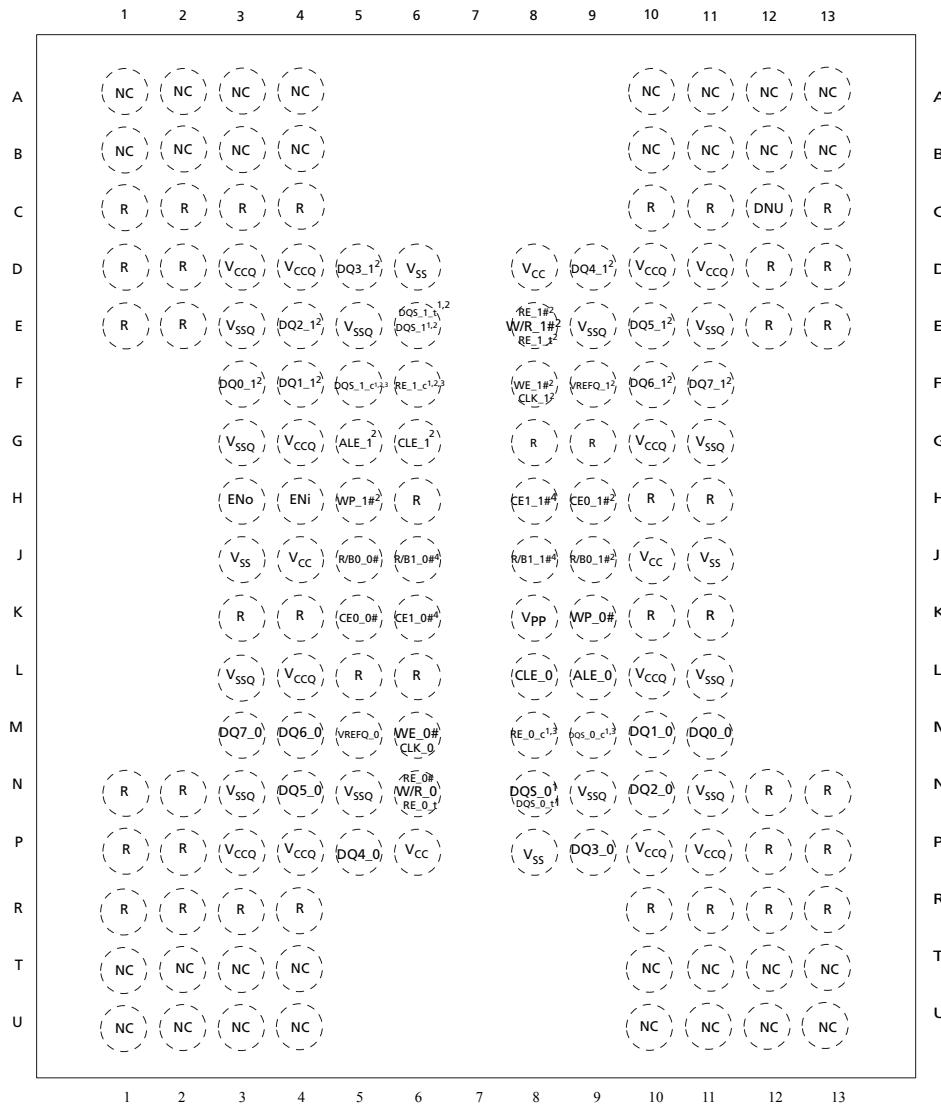
Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Signal Assignments

Signal Assignments

Figure 2: 152-Ball BGA (Ball-Down, Top View)



- Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
 2. These signals are available on dual, quad, and octal die packages. They are NC for other configurations.
 3. These signals are available when differential signaling is enabled.
 4. These signals are available on quad die four CE# or octal die packages. They are NC for other configurations.

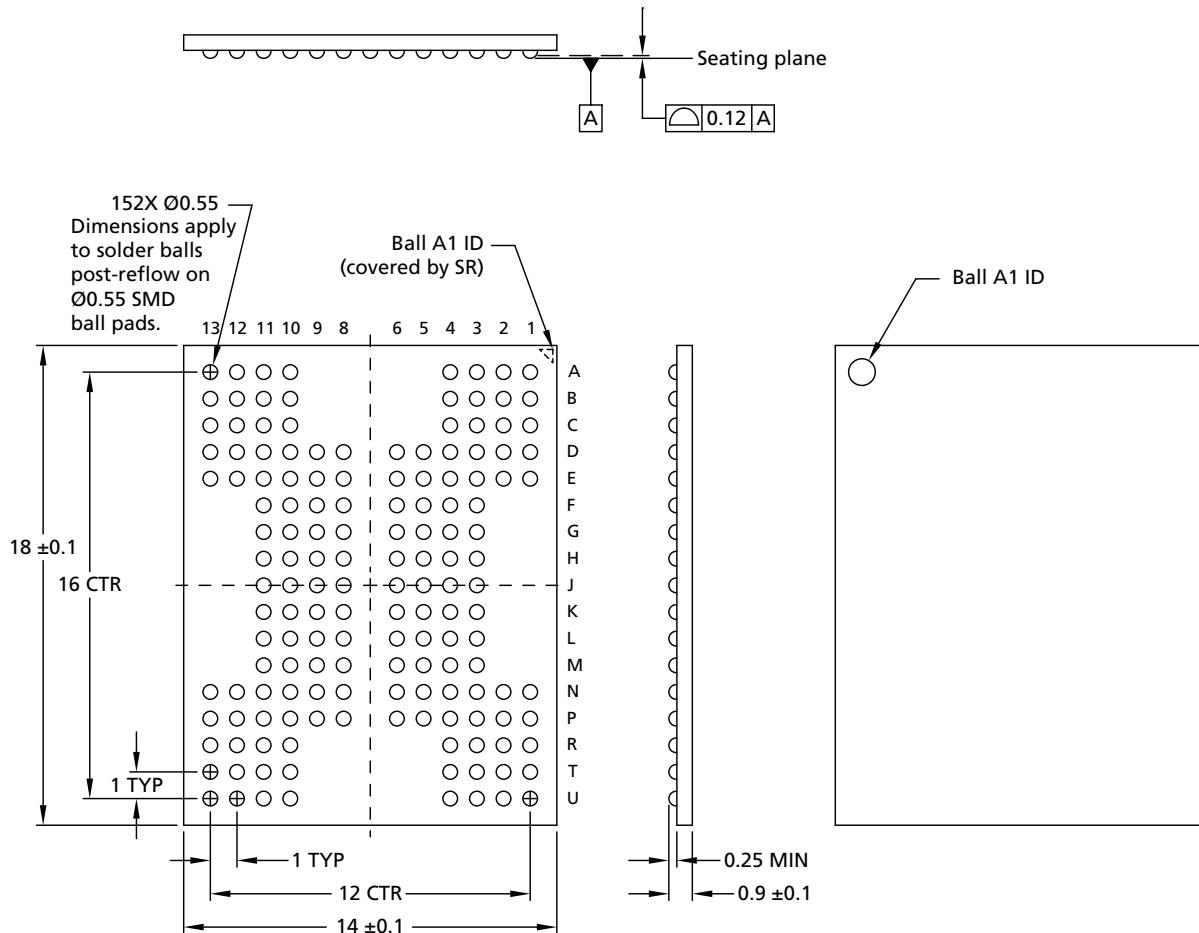
Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Package Dimensions

Package Dimensions

Figure 3: 152-Ball VBGA – 14mm x 18mm (Package Code: H6)



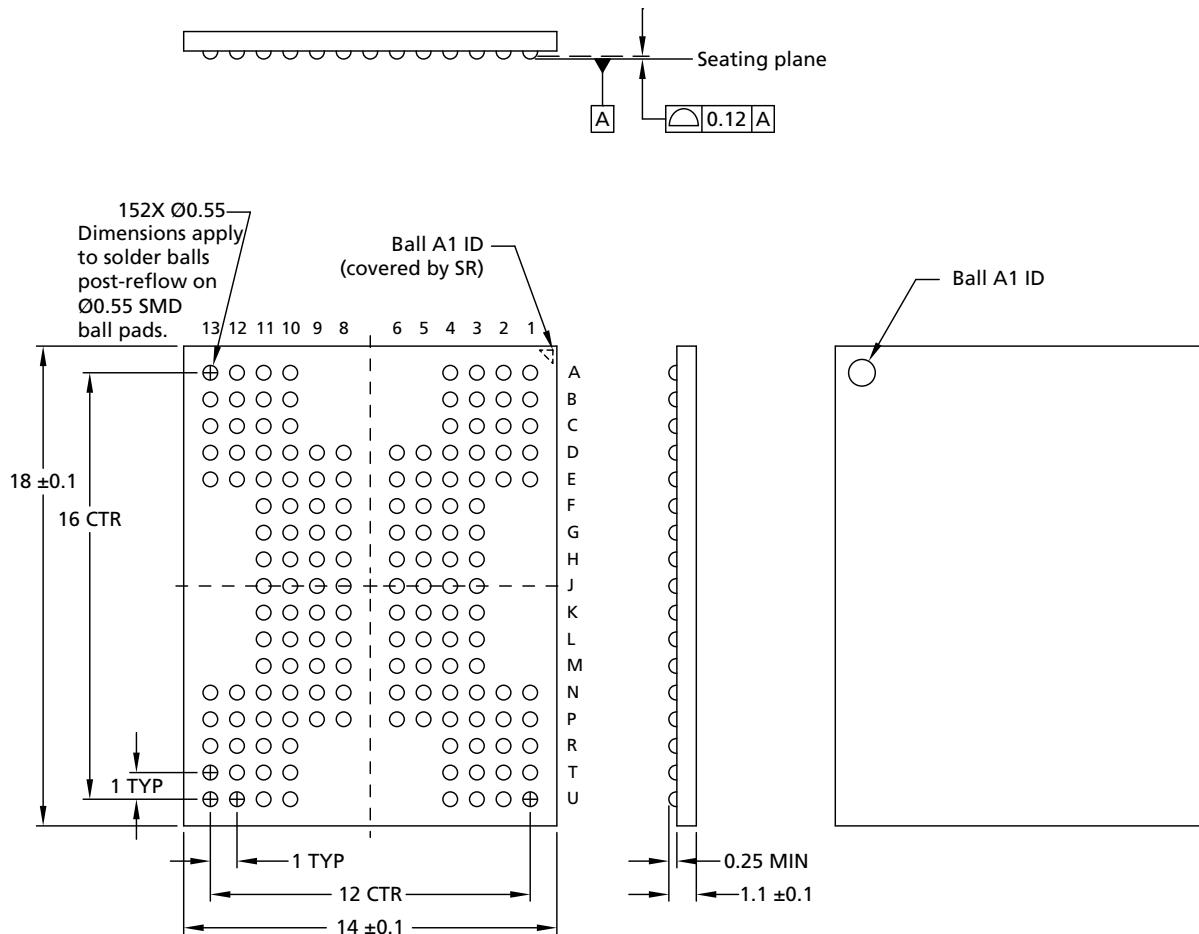
- Notes:
1. All dimensions are in millimeters.
 2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Package Dimensions

Figure 4: 152-Ball TBGA – 14mm x 18mm (Package Code: H7)



Notes:

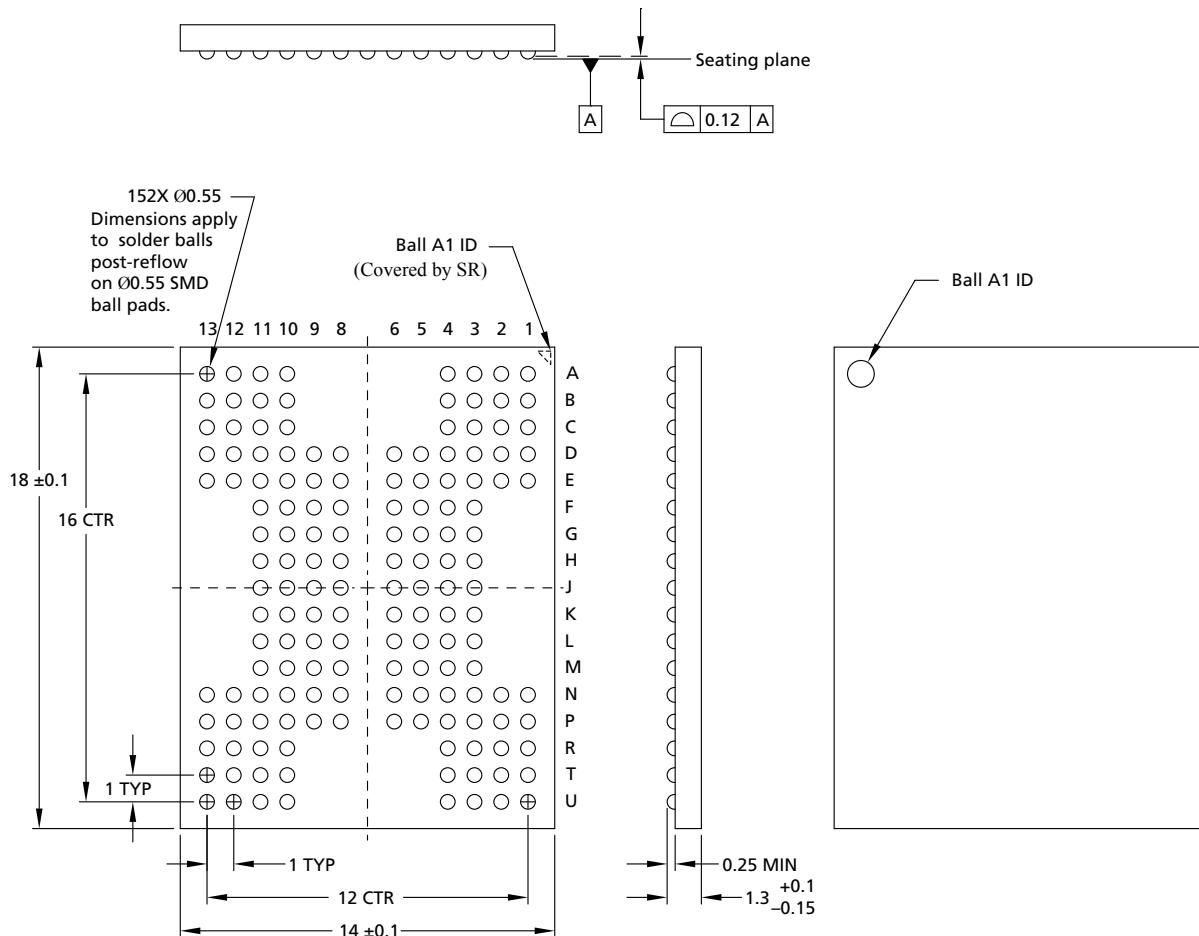
1. All dimensions are in millimeters.
2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Package Dimensions

Figure 5: 152-Ball LBGA – 14mm x 18mm (Package Code: H8)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

Release: 3/26/13



Architecture

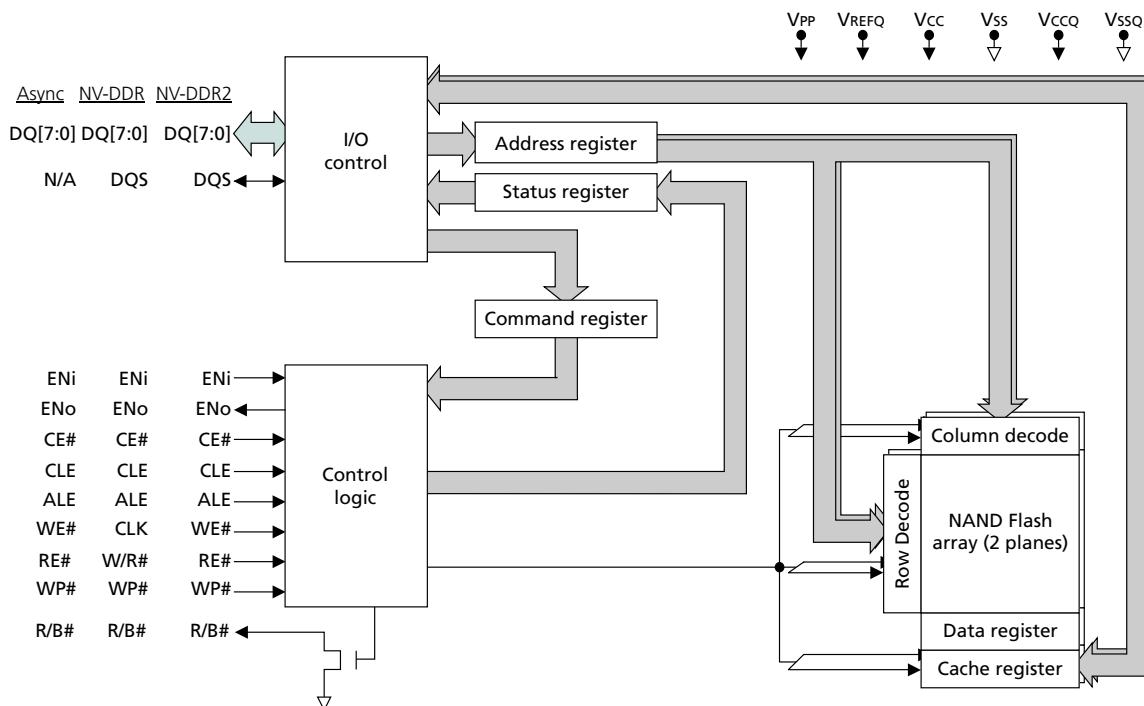
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

Figure 6: NAND Flash Die (LUN) Functional Block Diagram



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Device and Array Organization

Device and Array Organization

Figure 7: Device Organization for Single-Die Package (BGA)

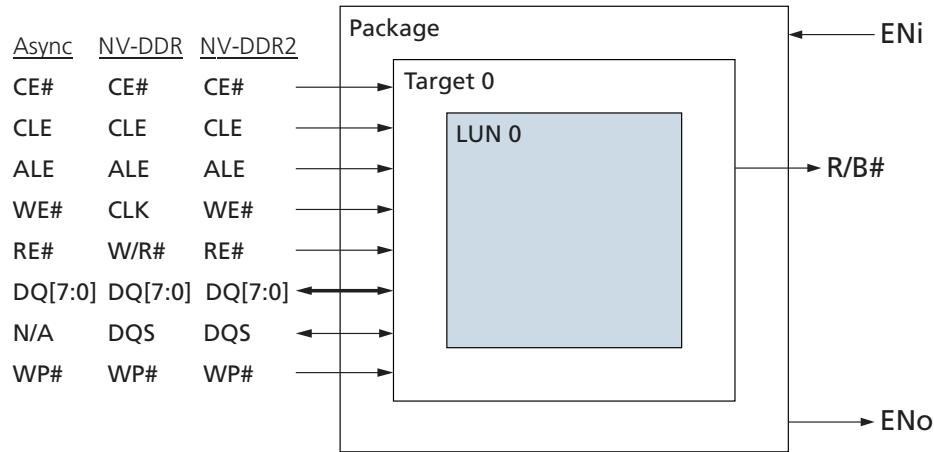
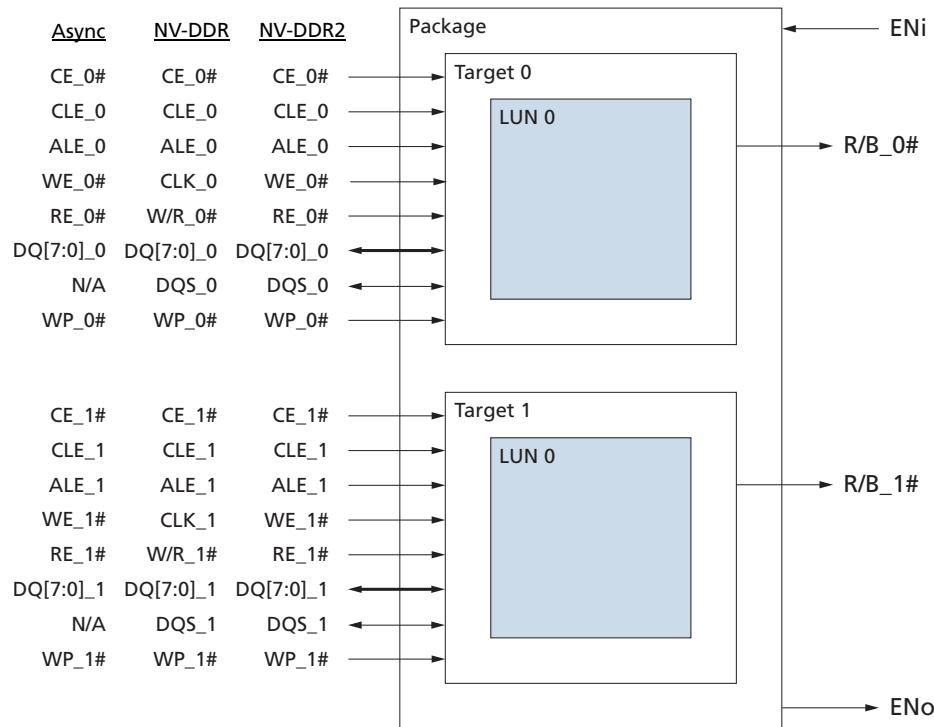


Figure 8: Device Organization for Two-Die Package (BGA)

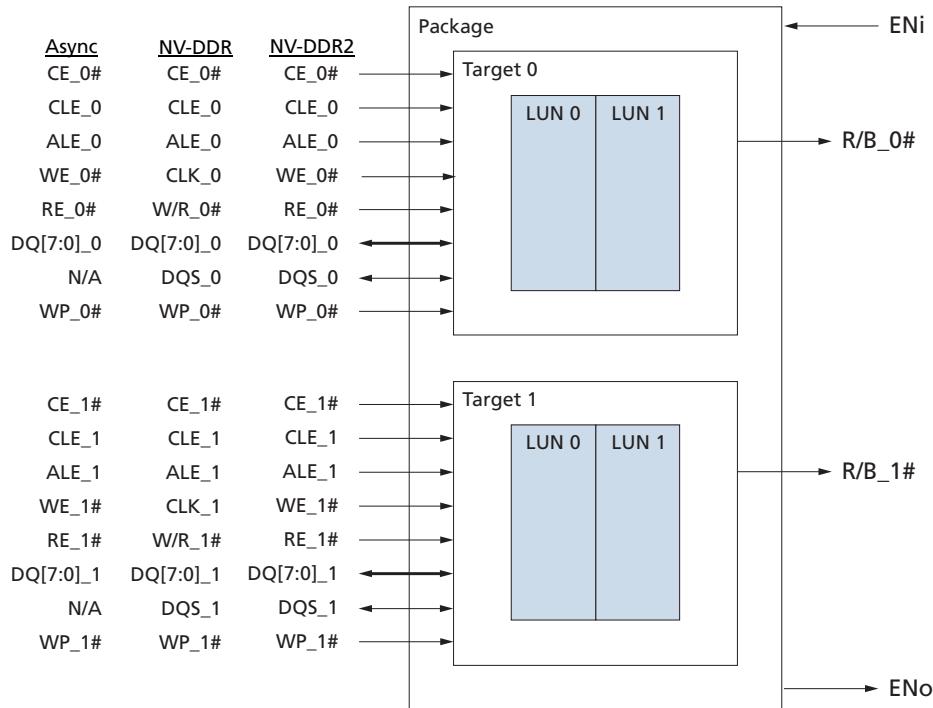


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Device and Array Organization

Figure 9: Device Organization for Four-Die Package with two CE# (BGA)

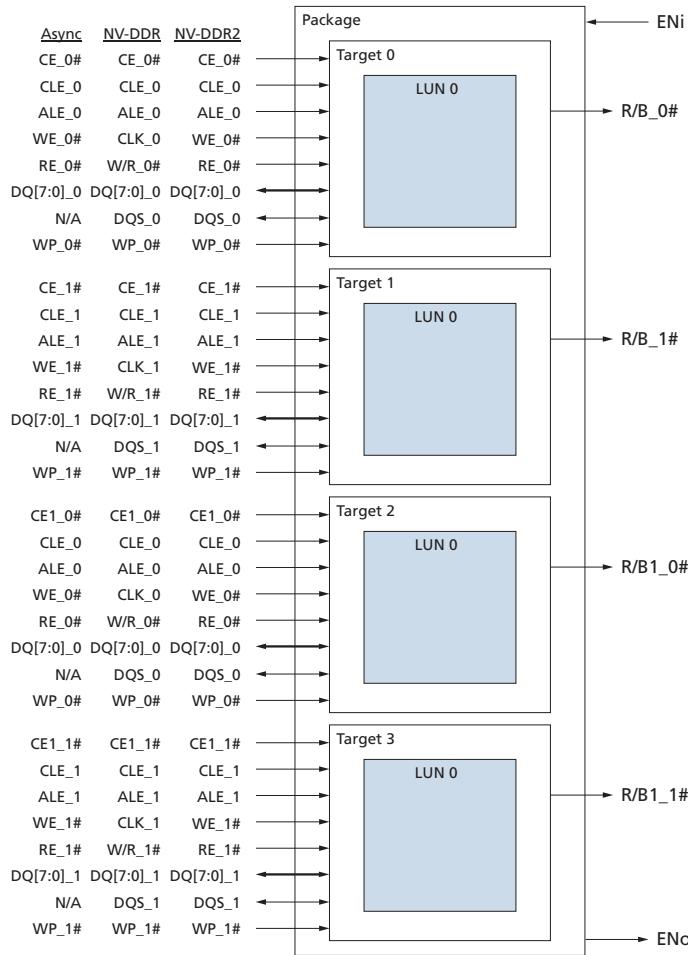


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Device and Array Organization

Figure 10: Device Organization for Four-Die Package with four CE# (BGA)

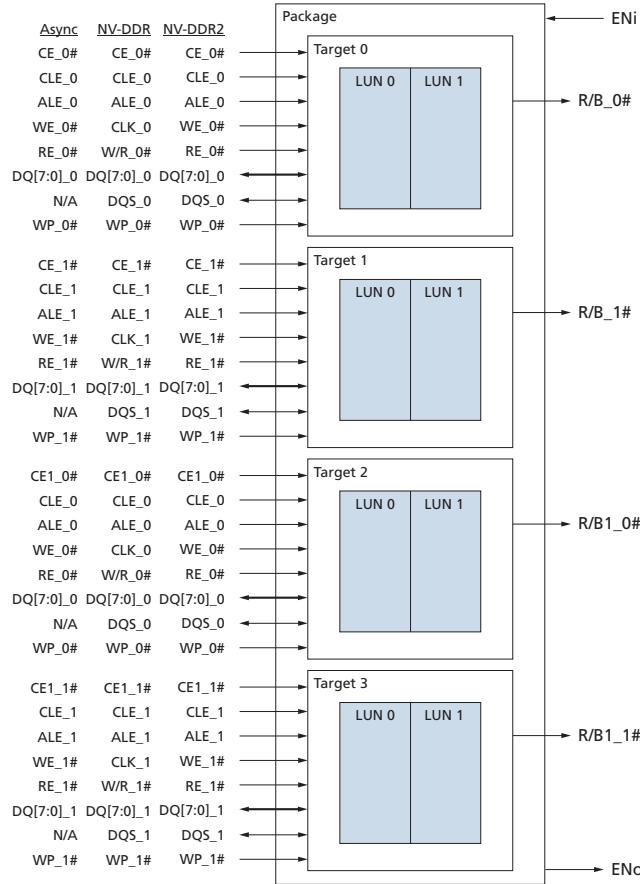


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Device and Array Organization

Figure 11: Device Organization for Eight-Die Package (BGA)



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Device and Array Organization

Figure 12: Array Organization per Logical Unit (LUN)

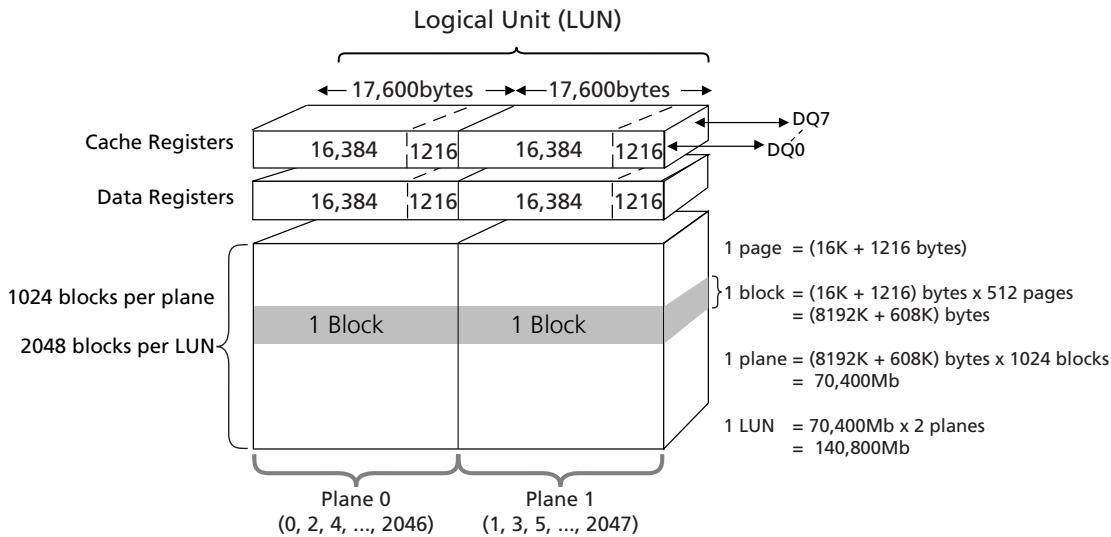


Table 2: Array Addressing for Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0 ²
Second	LOW	CA14 ³	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9 ⁴	BA8
Fifth	LOW	LOW	LOW	LA0 ⁵	BA19	BA18	BA17	BA16

- Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
 2. When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
 3. Column addresses 17,600 (44C0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
 4. BA[9] is the plane-select bit:
 - Plane 0: BA[9] = 0
 - Plane 1: BA[9] = 1
 5. LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise, it should be held LOW.
 - LUN 0: LA0 = 0
 - LUN 1: LA0 = 1

Release: 3/26/13



Bus Operation – Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on. The I/O bus, DQ[7:0], is multiplexed sharing data I/O, addresses, and commands. The DQS signal, if present, is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized below.

Table 3: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V _{CCQ} ²	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L		H	X	input	H	
Address input	L	L	H		H	X	input	H	
Data input	L	L	L		H	X	input	H	
Data output	L	L	L	H		X	output	X	
Write protect	X	X	X	X	X	X	X	L	

- Notes:
1. DQS is tri-stated when the asynchronous interface is active.
 2. WP# should be biased to CMOS LOW or HIGH for standby.
 3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Asynchronous Enable/Standby

A chip enable (CE#) signal is used to enable or disable a target. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own chip enable; the first target (Target 0) is controlled by CE#; the second target (if present) is controlled by CE2#, etc.

A target is disabled when CE# is driven HIGH, even when the target is busy. When disabled, all of the target's signals are disabled except CE#, WP#, and R/B#. This functionality is also known as CE# "Don't Care". While the target is disabled, other devices can utilize the disabled NAND signals that are shared with the NAND Flash.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when CE# is LOW, WE# is HIGH, and RE# is HIGH.

During bus idle, all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.



Asynchronous Pausing Data Input/Output

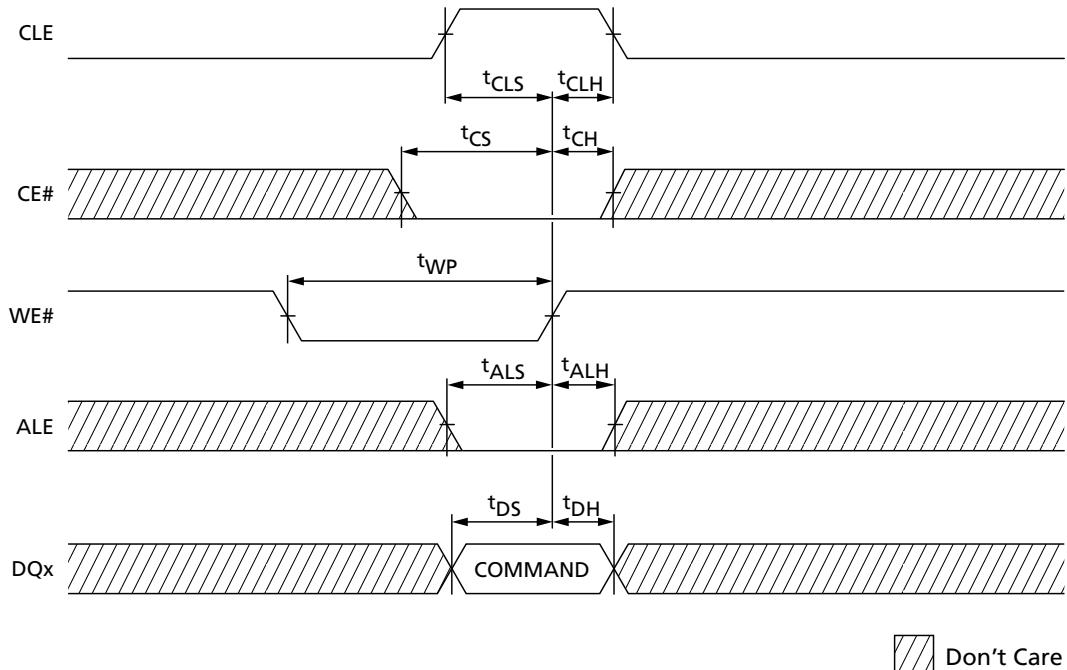
Pausing data input or data output is done by keeping WE# or RE# HIGH, respectively.

Asynchronous Commands

An asynchronous command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs) even when they are busy.

Figure 13: Asynchronous Command Latch Cycle



Release: 3/26/13



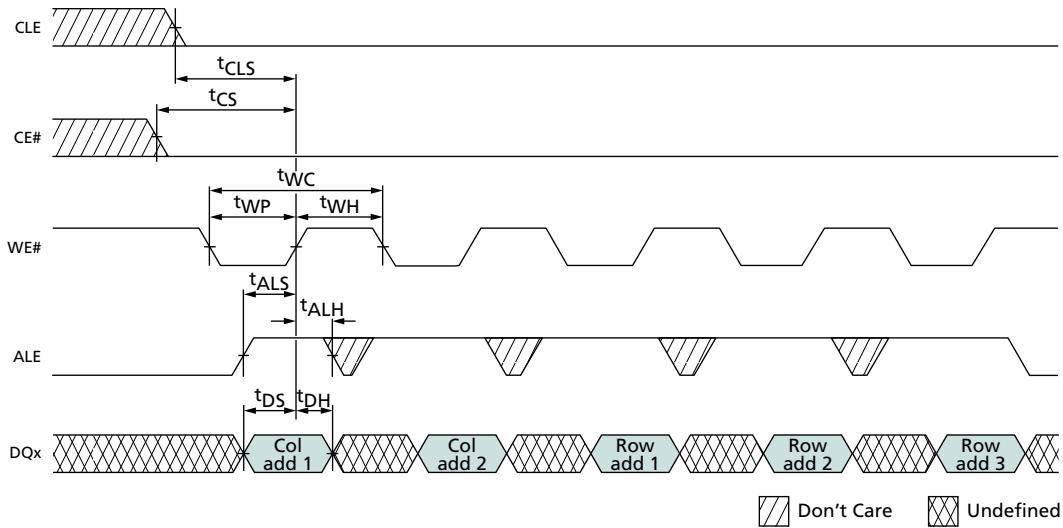
Asynchronous Addresses

An asynchronous address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Command Definitions).

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 14: Asynchronous Address Latch Cycle



Release: 3/26/13

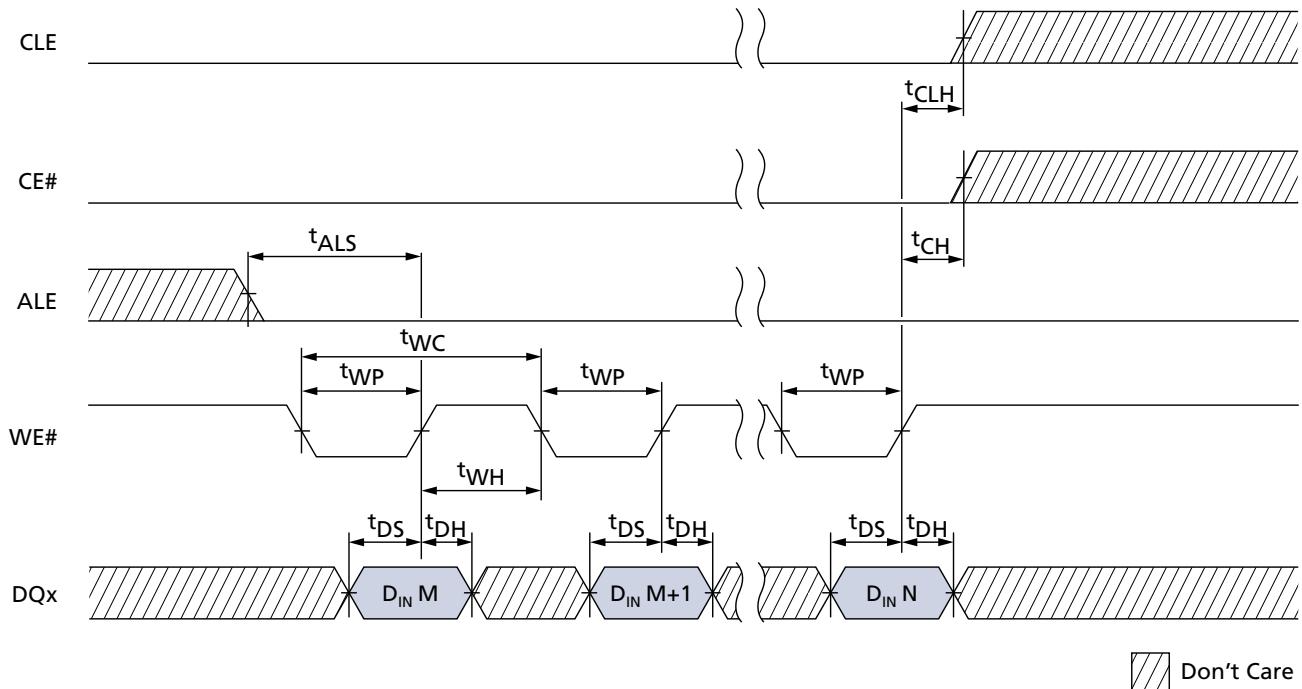


Asynchronous Data Input

Data is written from DQ[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0).

Figure 15: Asynchronous Data Input Cycles



Release: 3/26/13



Asynchronous Data Output

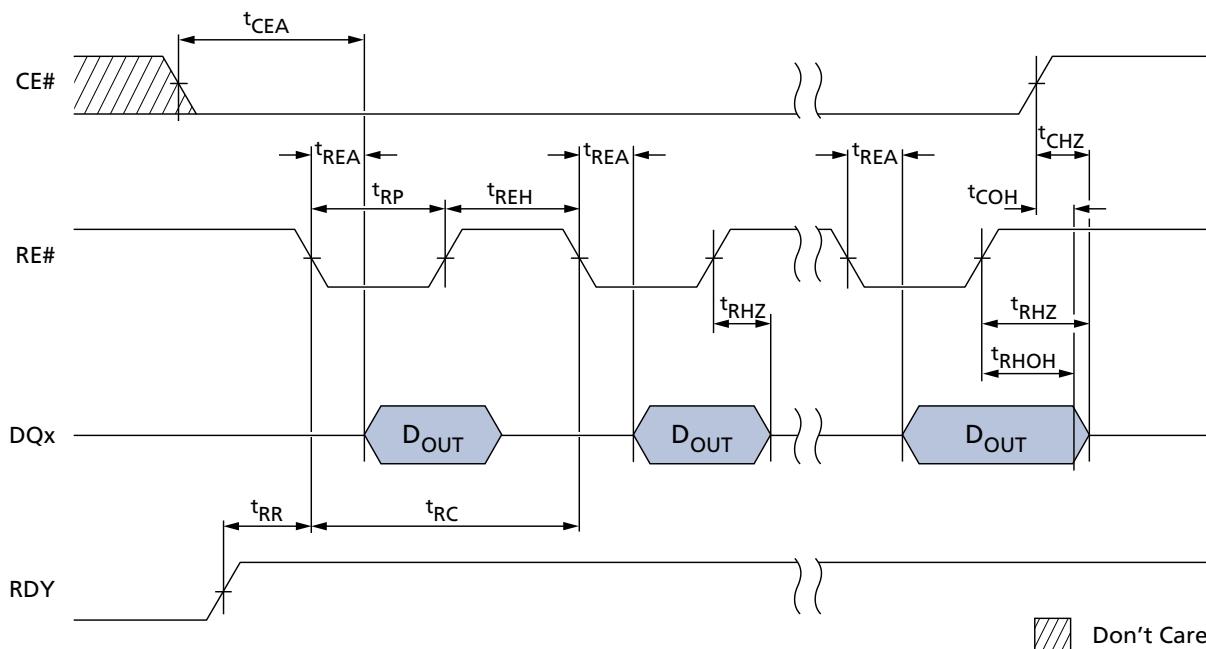
Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to DQ[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a t_{RC} of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 16 for proper timing). If the host controller is using a t_{RC} of less than 30ns, the host can latch the data on the next falling edge of RE# (see Figure 17 (page 29) for extended data output (EDO) timing).

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

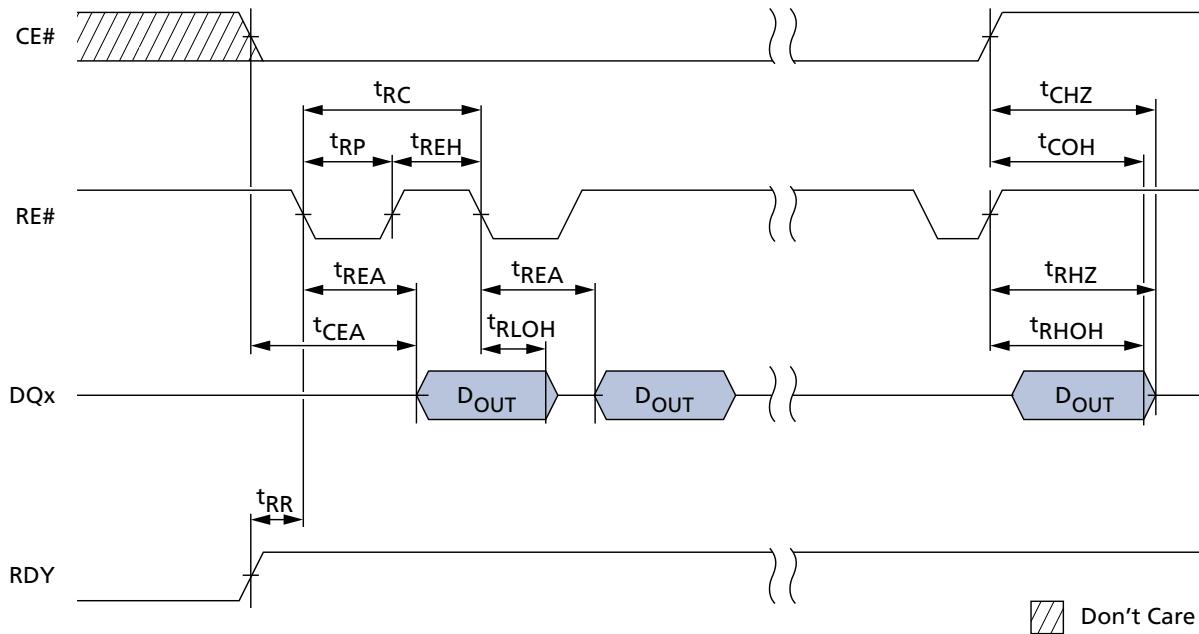
Figure 16: Asynchronous Data Output Cycles



Release: 3/26/13



Figure 17: Asynchronous Data Output Cycles (EDO Mode)



Write Protect

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc and Vccq are stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait t_{WW} before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy ($RDY = 0$). A target is ready when all of its die (LUNs) are ready ($RDY = 1$). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – Asynchronous Interface

driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 18 (page 30)).

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

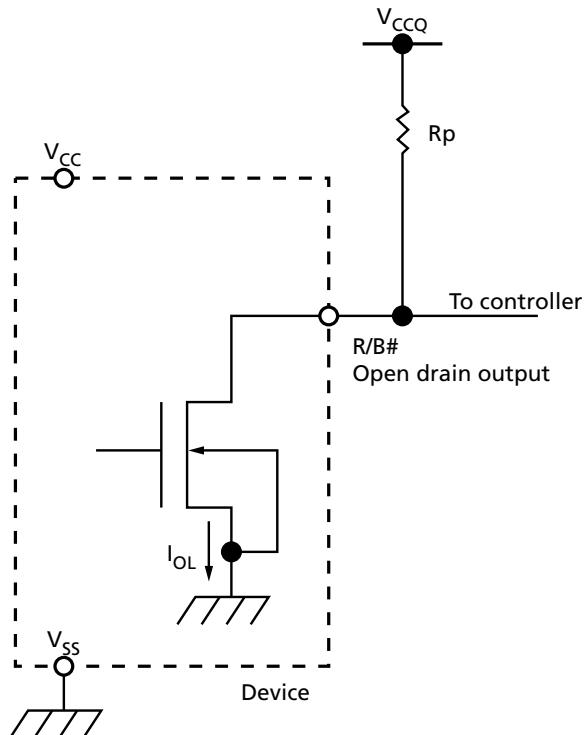
The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 23 (page 33).

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and Vccq.

$$Rp = \frac{V_{CC} (\text{MAX}) - V_{OL} (\text{MAX})}{I_{OL} + \Sigma I_l}$$

Where ΣI_l is the sum of the input currents of all devices tied to the R/B# pin.

Figure 18: READ/BUSY# Open Drain

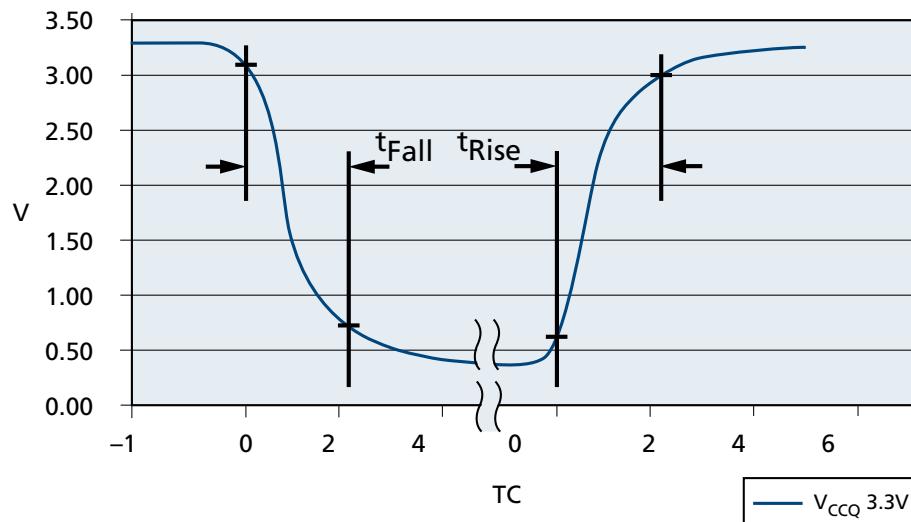


Release: 3/26/13



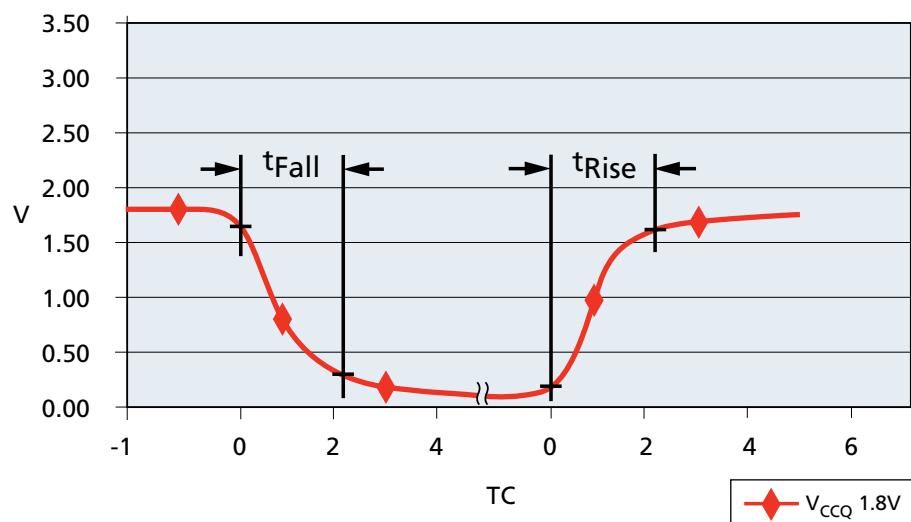
128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – Asynchronous Interface

Figure 19: t_{Fall} and t_{Rise} ($V_{CCQ} = 2.7\text{-}3.6\text{V}$)



- Notes:
1. t_{FALL} is $V_{OH(DC)}$ to $V_{OL(AC)}$ and t_{RISE} is $V_{OL(DC)}$ to $V_{OH(AC)}$.
 2. t_{Rise} dependent on external capacitance and resistive loading and output transistor impedance.
 3. t_{Rise} primarily dependent on external pull-up resistor and external capacitive loading.
 4. $t_{Fall} = 10\text{ns}$ at 3.3V
 5. See TC values in Figure 23 (page 33) for approximate R_p value and TC.

Figure 20: t_{Fall} and t_{Rise} ($V_{CCQ} = 1.7\text{-}1.95\text{V}$)



- Notes:
1. t_{FALL} is $V_{OH(DC)}$ to $V_{OL(AC)}$ and t_{RISE} is $V_{OL(DC)}$ to $V_{OH(AC)}$.
 2. t_{Rise} is primarily dependent on external pull-up resistor and external capacitive loading.
 3. $t_{Fall} \approx 7\text{ns}$ at 1.8V .
 4. See TC values in Figure 23 (page 33) for TC and approximate R_p value.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – Asynchronous Interface

Figure 21: IOL vs Rp ($V_{CCQ} = 2.7\text{-}3.6V$)

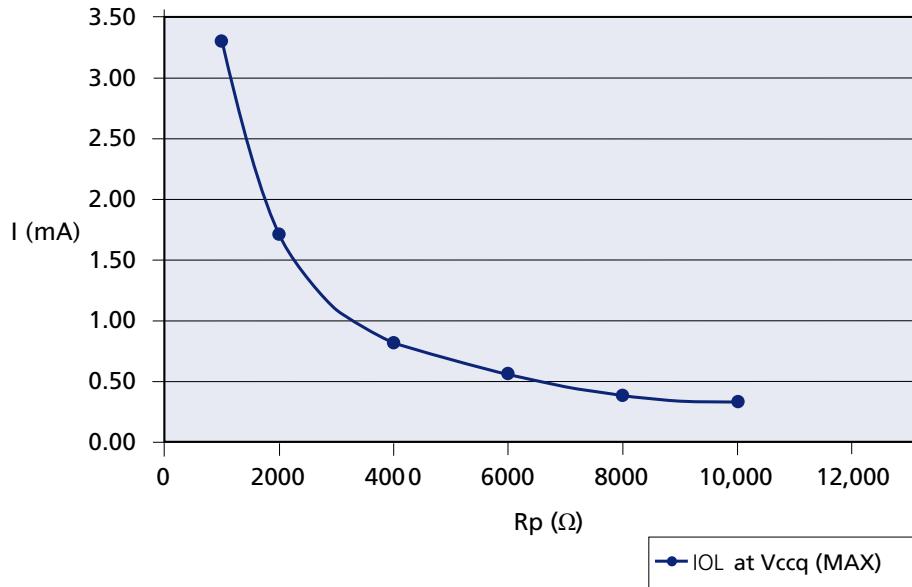
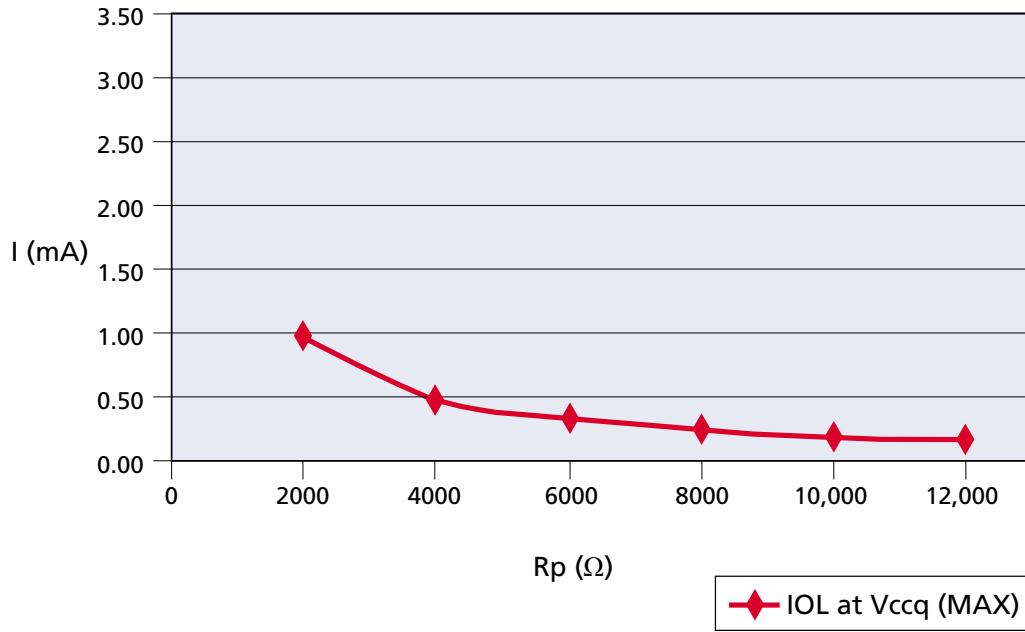
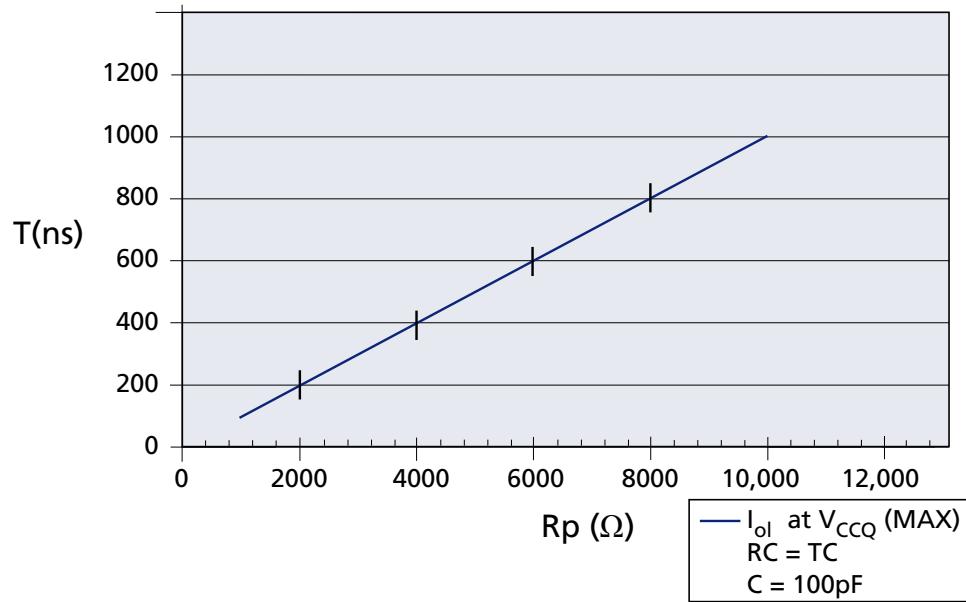


Figure 22: IOL vs Rp ($V_{CCQ} = 1.7\text{-}1.95V$)



Release: 3/26/13

**128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – Asynchronous Interface****Figure 23: TC vs Rp**

Release: 3/26/13



Bus Operation – NV-DDR Interface

These NAND Flash devices have two interfaces—a synchronous interface for fast data (NV-DDR) I/O transfer and an asynchronous interface that is backward compatible with existing NAND Flash devices.

The NAND Flash command protocol for both the asynchronous and NV-DDR interfaces is identical. However, there are some differences between the asynchronous and NV-DDR interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

When the NV-DDR interface is activated on a target (see Activating Interfaces), the target is capable of high-speed NV-DDR data transfers. Existing signals are redefined for high-speed NV-DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#. CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

Transition from the NV-DDR interface to the NV-DDR2 interface is not permitted.

The NV-DDR interface bus modes are summarized below.

Table 4: NV-DDR Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V _{CCQ}	1, 2
Bus idle	L	L	L		H	X	X	X	
Bus driving	L	L	L		L	output	output	X	
Command input	L	H	L		H	X	input	H	3
Address input	L	L	H		H	X	input	H	3
Data input	L	H	H		H		input	H	4
Data output	L	H	H		L	See Note 5	output	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H		L	output	output	X	
Undefined	L	H	L		L	output	output	X	

Notes: 1. CLK can be stopped when the target is disabled, even when R/B# is LOW.

2. WP# should be biased to CMOS LOW or HIGH for standby.

3. Commands and addresses are latched on the rising edge of CLK.



4. During data input to the device, DQS is the “clock” that latches the data in the cache register.
5. During data output from the NAND Flash device, DQS is an output generated from CLK after t_{DQSCK} delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL} .

NV-DDR Enable/Standy

In addition to the description found in Asynchronous Enable/Standy, the following requirements also apply when the NV-DDR interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until t_{CS} completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

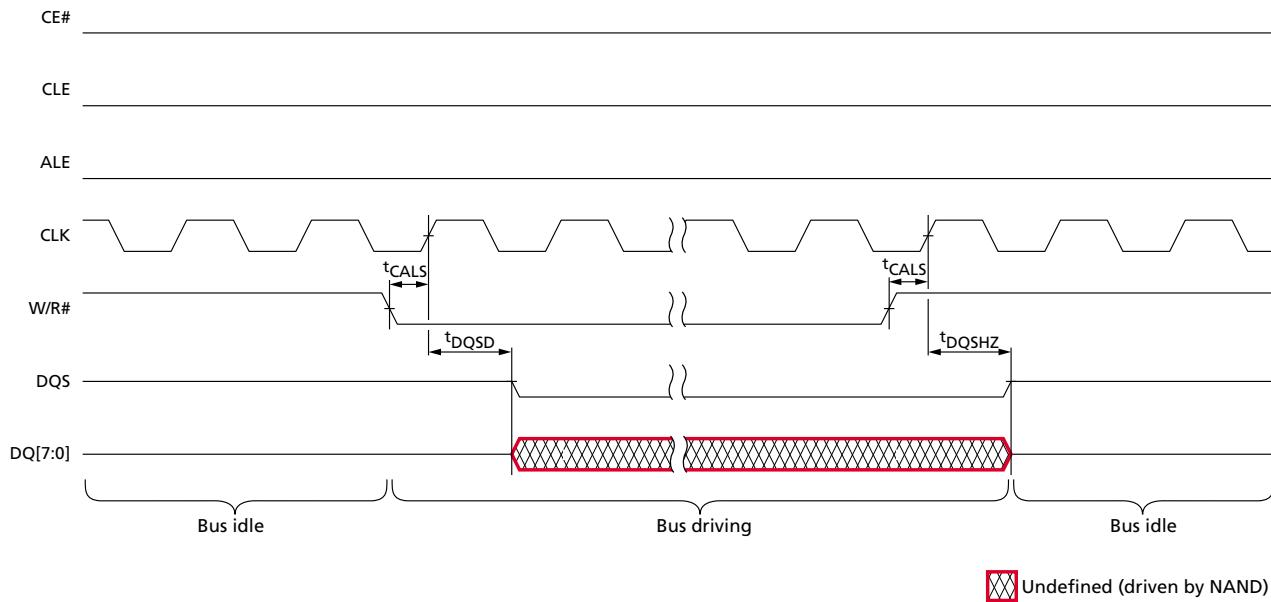
NV-DDR Bus Idle/Driving

A target's bus is idle or driving when CLK is running, CE# is LOW, ALE is LOW, and CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of t_{CAD} before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and NV-DDR data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and NV-DDR data output.

Release: 3/26/13

**Figure 24: NV-DDR Bus Idle/Driving Behavior**

Undefined (driven by NAND)

Note: 1. Only the selected die (LUN) drives DQS and DQ[7:0]. During an interleaved die (multi-LUN) operation, the host must use the READ STATUS ENHANCED (78h) to prevent data output contention.

NV-DDR Pausing Data Input/Output

Pausing data input or data output is done by setting ALE and CLE to LOW. The host may continue data transfer by setting ALE and CLE to HIGH after the applicable t_{CAD} time has passed.

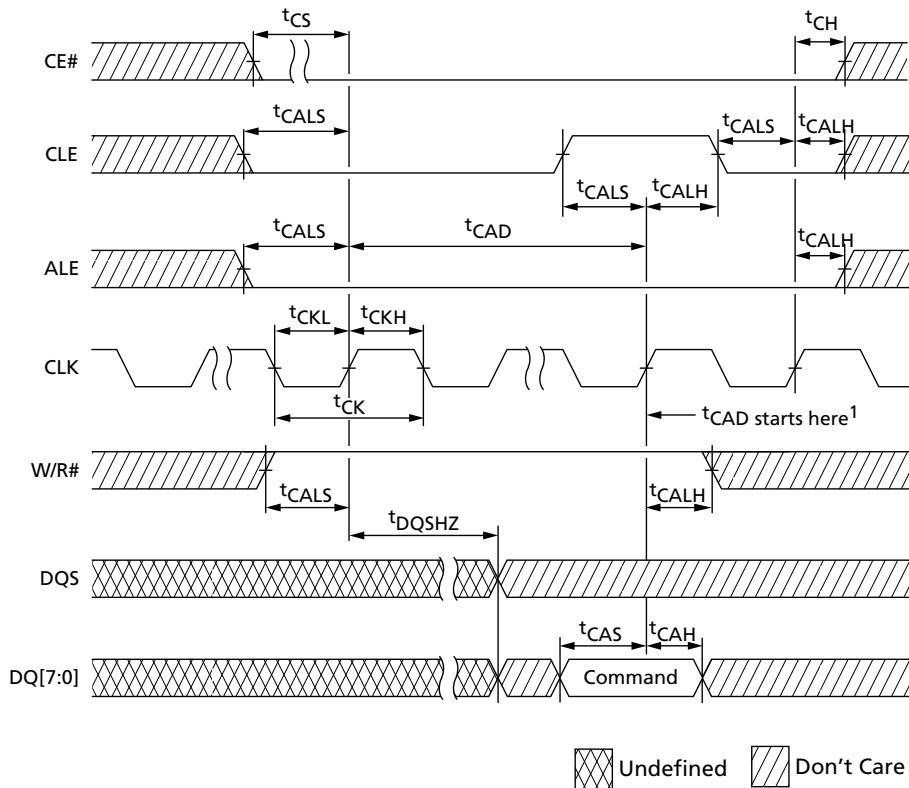
NV-DDR Commands

A command is written from DQ[7:0] to the command register on the rising edge of CLK when CE# is LOW, ALE is LOW, CLE is HIGH, and W/R# is HIGH.

After a command is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, t_{CK} , is greater than t_{CAD} .

Commands are typically ignored by die (LUNs) that are busy ($RDY = 0$); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Release: 3/26/13

**Figure 25: NV-DDR Command Cycle**

Note: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR Addresses

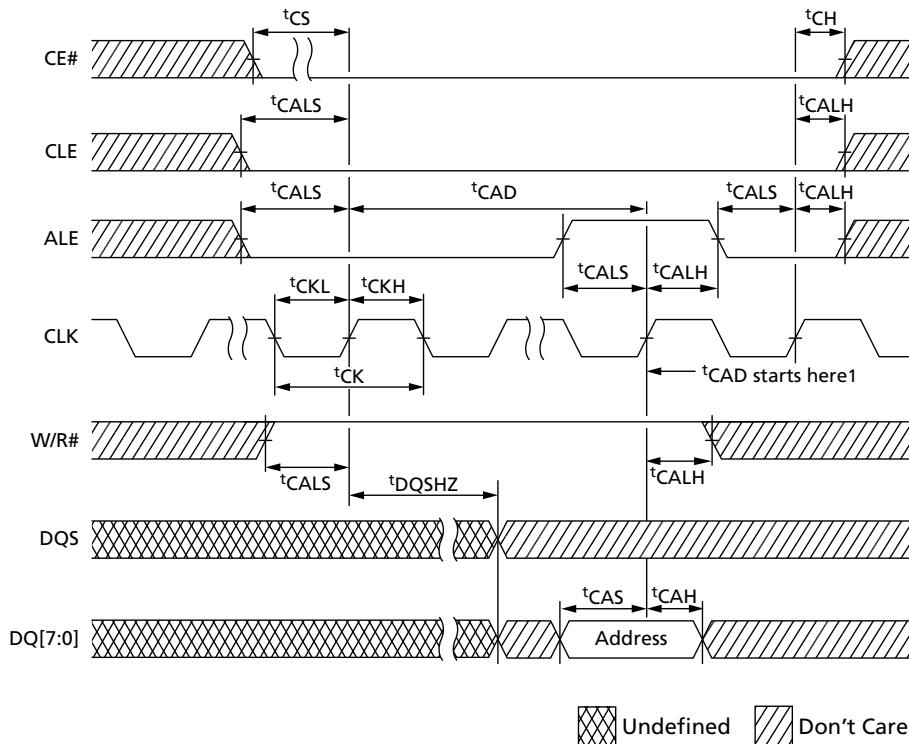
A NV-DDR address is written from DQ[7:0] to the address register on the rising edge of CLK when CE# is LOW, ALE is HIGH, CLE is LOW, and W/R# is HIGH.

After an address is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, t_{CK} , is greater than t_{CAD} .

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Release: 3/26/13

**Figure 26: NV-DDR Address Cycle**

Note: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR DDR Data Input

To enter the NV-DDR data input mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is HIGH
- t_{CAD} is met
- DQS is LOW
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the NV-DDR data input mode after t_{DQSS} , data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CLK is running and the DQS to CLK skew meets t_{DSH} and t_{DSS} , CE# is LOW, W/R# is HIGH, and ALE and CLE are HIGH on the rising edge of CLK.

To exit NV-DDR data input mode, the following conditions must be met:

- CLK is running and the DQS to CLK skew meets t_{DSH} and t_{DSS}
- CE# is LOW
- W/R# is HIGH
- ALE and CLE are latched LOW on the rising edge of CLK



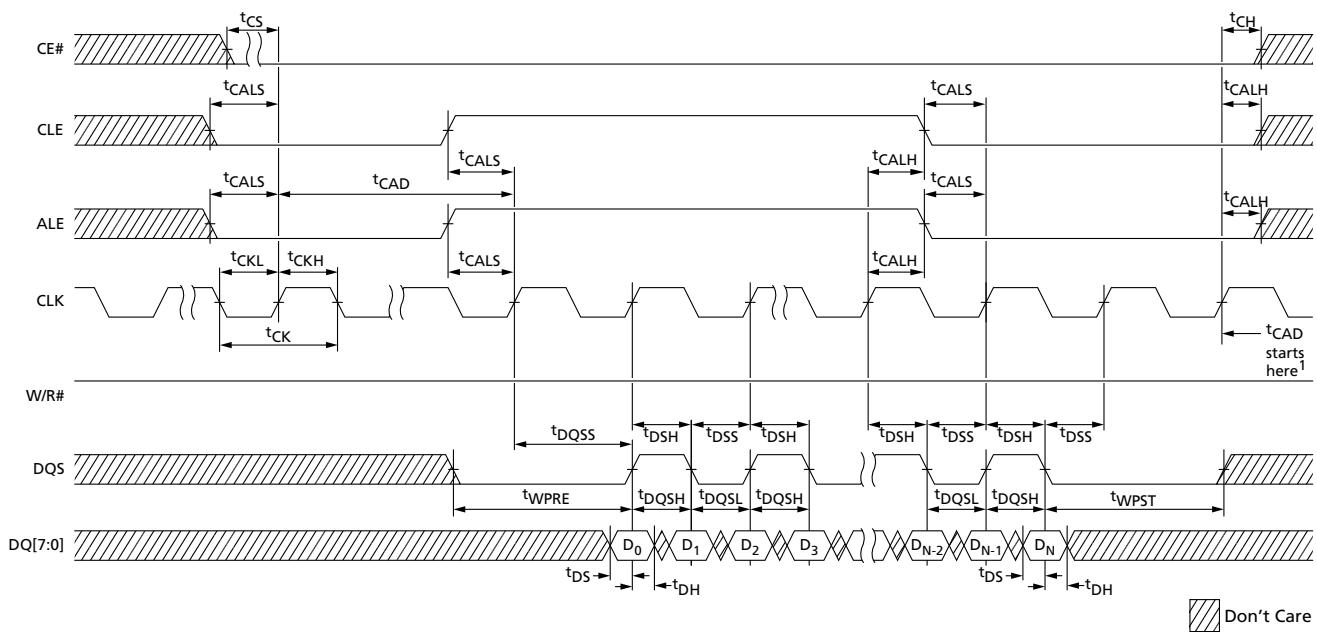
128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR Interface

- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence in which ALE and CLE are latched HIGH.
- DQS is held LOW for t_{WPST} (after the final falling edge of DQS)

Following t_{WPST} , the bus enters bus idle mode and t_{CAD} begins on the next rising edge of CLK. After t_{CAD} starts, the host can disable the target if desired.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 27: NV-DDR Data Input Cycles



- Notes:
- When CE# remains LOW, t_{CAD} begins at the first rising edge of the clock after t_{WPST} completes.
 - t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
 - t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).

NV-DDR Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- W/R# is latched LOW on the rising edge of CLK to enable the selected die (LUN) to take ownership of the DQ[7:0] bus and DQS within t_{WRCK}
- t_{CAD} is met
- ALE and CLE are HIGH on the rising edge of CLK



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR Interface

Upon entering the NV-DDR data output mode, DQS will toggle HIGH and LOW with a delay of t_{DQSCK} from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than t_{AC} .

NV-DDR data output mode continues as long as CLK is running, CE# is LOW, W/R# is LOW, and ALE and CLE are HIGH on the rising edge of CLK.

To exit NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is LOW
- ALE and CLE are latched LOW on the rising edge of CLK

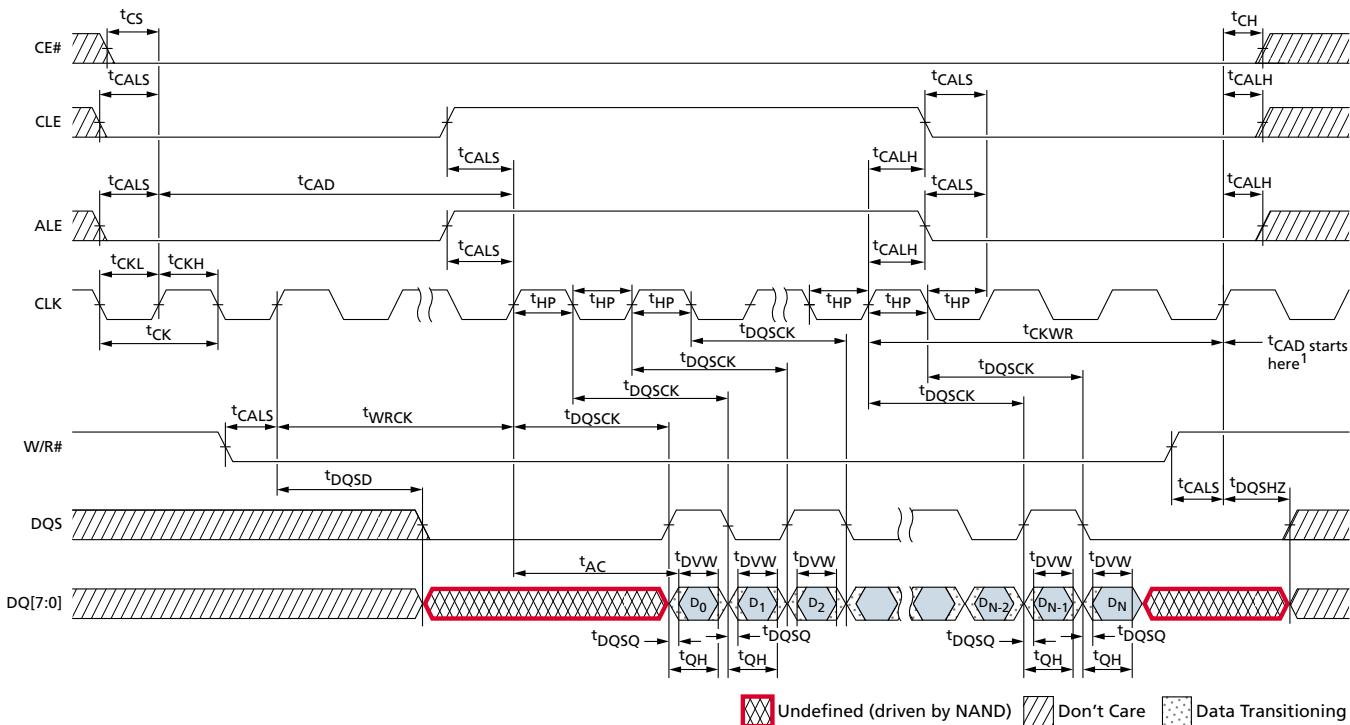
The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur t_{DQSCK} after the last cycle in the data output sequence in which ALE and CLE are latched HIGH. After t_{CKWR} , the bus enters bus idle mode and t_{CAD} begins on the next rising edge of CLK. Once t_{CAD} starts the host can disable the target if desired.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Release: 3/26/13



Figure 28: NV-DDR Data Output Cycles



- Notes:
1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock after t_{CKWR} for subsequent command or data output cycle(s).
 2. See Figure 25 (page 37) for details of W/R# behavior.
 3. t_{AC} is the DQ output window relative to CLK and is the long-term component of DQ skew.
 4. For W/R# transitioning HIGH, DQ[7:0] and DQS go to tri-state.
 5. For W/R# transitioning LOW, DQ[7:0] drives current state and DQS goes LOW.
 6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See Write Protect under Bus Operations - Asynchronous Interface.

Ready/Busy#

See Ready/Busy# under Bus Operations - Asynchronous Interface.

Release: 3/26/13



Bus Operation – NV-DDR2 Interface

When the NV-DDR2 interface is activated on a target (see Activating Interfaces), the target is capable of high-speed DDR data transfers. and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

For operations in NV-DDR2 mode, the NV-DDR2 interface must be selected (see Activating Interfaces (page 63)). The capabilities that NV-DDR2 operations offers beyond NV-DDR operations include:

- Supported only at 1.8VV_{CCQ}
- Support for speeds beyond 200MT/s
- Support for differential signaling for the RE# and/or DQS signals (RE_c, DQS_c)
- Support for Warmup Cycles
- Support for On-die Termination (ODT)
- Support for V_{REFQ}

Use of differential signaling and V_{REFQ} is optional for interface speeds 200MT/s or slower and required for interface speeds faster than 200MT/s. Devices tested in NV-DDR2 mode are with differential signaling enabled which is needed to guarantee AC timings in the NV-DDR2 mode at faster speeds. If not using the differential signaling, statements about those signal types can be ignored.

Transition from the NV-DDR2 interface to the NV-DDR interface is not permitted.

The NV-DDR2 interface bus modes are summarized below:

Table 5: NV-DDR2 Interface Mode Selection

Mode	CE#	CLE	ALE	RE# (RE_t)	DQS (DQS_t)	DQ[7:0] ¹	WE#	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V _{CCQ}	1, 2
Idle	L	L	L	H	H	X	H	X	5
Command input	L	H	L	H	H	input		H	3
Address input	L	L	H	H	X	input		H	3
Data input	L	L	L	H		input	H	H	2, 3
Data output	L	L	L			output	H	X	2, 3, 4
Write protect	X	X	X	X	X	X	X	L	

- Notes:
1. The current state of the device is data input, data output, or neither based on the commands issued.
 2. There are two data input/output cycles from the rising edge of DQS/RE# to the next rising edge of DQS/RE#.
 3. ODT may be enabled as part of the data input and data output cycles.

Release: 3/26/13



4. At the beginning of a data output burst, DQS shall be held HIGH for t_{DQSRH} after RE# transitions LOW to begin data output.
5. WE# is set HIGH during the Idle state.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL} .

Differential Signaling

An enabler for higher speed operation is differential signaling for the RE# and DQS signals. A complementary RE# and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE# is referred to as RE_t and DQS is referred to as DQS_t, i.e., the "true" versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling shall only be enabled for use when the NV-DDR2 data interface is selected.

A device may support differential RE# and/or differential DQS signaling. The support for differential RE# and/or DQS is reported in the parameter page. Complementary RE# (i.e., RE_c) and complementary DQS (i.e., DQS_c) signals are individually configured/ enabled. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the NV-DDR2 Configuration feature address.

To begin using differential signaling, the host shall issue a SET FEATURES (EFh) command to the Timing Mode feature address that sets the Data Interface from asynchronous to NV-DDR2 operation. Then issue a SET FEATURES (EFh) command to the NV-DDR2 Configuration feature address to activate differential RE# and/or differential DQS signaling. The differential signaling is then enabled after CE# is brought HIGH.

To change from differential signaling to single-ended signaling, the host shall configure the device using the NV-DDR2 Configuration feature address to disable differential signaling. The differential signaling is disabled after CE# is brought HIGH.

A RESET (FFh) command will disable differential signaling. The SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) commands have no effect on differential signaling.

Warmup Cycles

In order to support higher speed operation, warmup cycles for data output and data input may be provided. Warmup cycles shall only be enabled for use when the NV-DDR2 data interface is selected.

Warmup cycles for data output provides extra RE# and corresponding DQS transitions at the beginning of a data output burst. These extra RE#/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 configuration feature address.

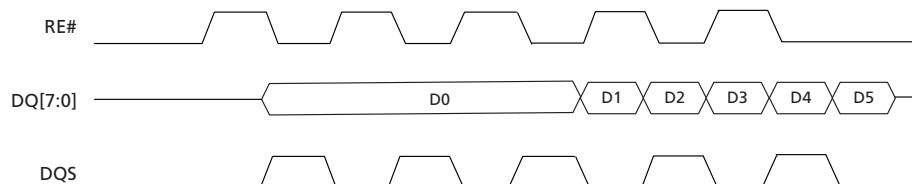
Warmup cycles for data input provides extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 Configuration feature address. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands. Warmup cycles are initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without



exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE, or CE# HIGH without latching with WE#. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without warmup cycles.

Figure 29: Warmup Cycles for data output (2 warmup cycles)



On-die Termination (ODT)

On-die termination may be required at higher speeds depending on system topology. On-die termination applies to the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. On-die termination is an optional capability that may be employed to meet higher speeds in particular topologies. If power needs to be optimized in a particular condition, then on-die termination may be disabled and the topology may be run at a slower timing mode. On-die termination shall only be enabled for use in the NV-DDR2 data interface.

On-die termination settings are configured during device initialization. The host may configure the ODT in a self-termination only configuration, or matrix termination which enables a combination of Target and non-Target termination to be specified.

For the more flexible matrix termination the host configures a matrix that defines the LUN(s) that terminate for a particular Volume. This matrix is configured using the ODT CONFIGURE (E2h) command. After the on-die termination matrix is defined, ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command, and address cycles). On-die termination applies for data input and output cycles for all command types, including both single data rate (SDR) and double data rate (DDR) transfers.

Volume addressing is required for use of non-Target on-die termination (ODT) functionality. See Configuration Operations for how to appoint Volume addresses. Once volume addresses have been appointed they can be selected with the VOLUME SELECT (E1h) command. For Target only termination, no ODT termination matrix is required.

The on-die termination configuration matrix and control mechanism utilize Volume addresses. Volume addressing is a required capability to utilize non-Target on-die termination.

When on-die termination is enabled via the NV-DDR2 Configuration feature address, the default is Target termination. For non-Target termination or termination topologies that use multiple terminators, the Volume address mechanism shall be used and the on-die termination configuration matrix shall be specified using the ODT CONFIGURE (E2h) command. As part of the ODT CONFIGURE (E2h) command, R_{TT} settings may be specified on a per LUN basis with individual values for:

- RE#
- DQ[7:0] and DQS for data output
- DQ[7:0] and DQS for data input



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

On-die termination is enabled when ALE, CLE and CE# transition from HIGH to LOW.
 On-die termination is disabled when ALE, CLE or CE# transitions from LOW to HIGH.

Table 6: On-die Termination DC Electrical Characteristics

Mode	Symbol	Min	Typ	Max	Units	Notes
R _{TT} effective impedance value for 50 Ohm setting	R _{TT2(EFF)}	32.5	50	67.5	Ohms	1
R _{TT} effective impedance value for 75 Ohm setting	R _{TT3(EFF)}	48.7	75	101.3	Ohms	1
R _{TT} effective impedance value for 100 Ohm setting	R _{TT4(EFF)}	65	100	135	Ohms	1
R _{TT} effective impedance value for 150 Ohm setting	R _{TT5(EFF)}	97.5	150	202.5	Ohms	1
Deviation of VM with respect to V _{CCQ} / 2	ΔVM	-7	-	7	Percent	2

Notes:

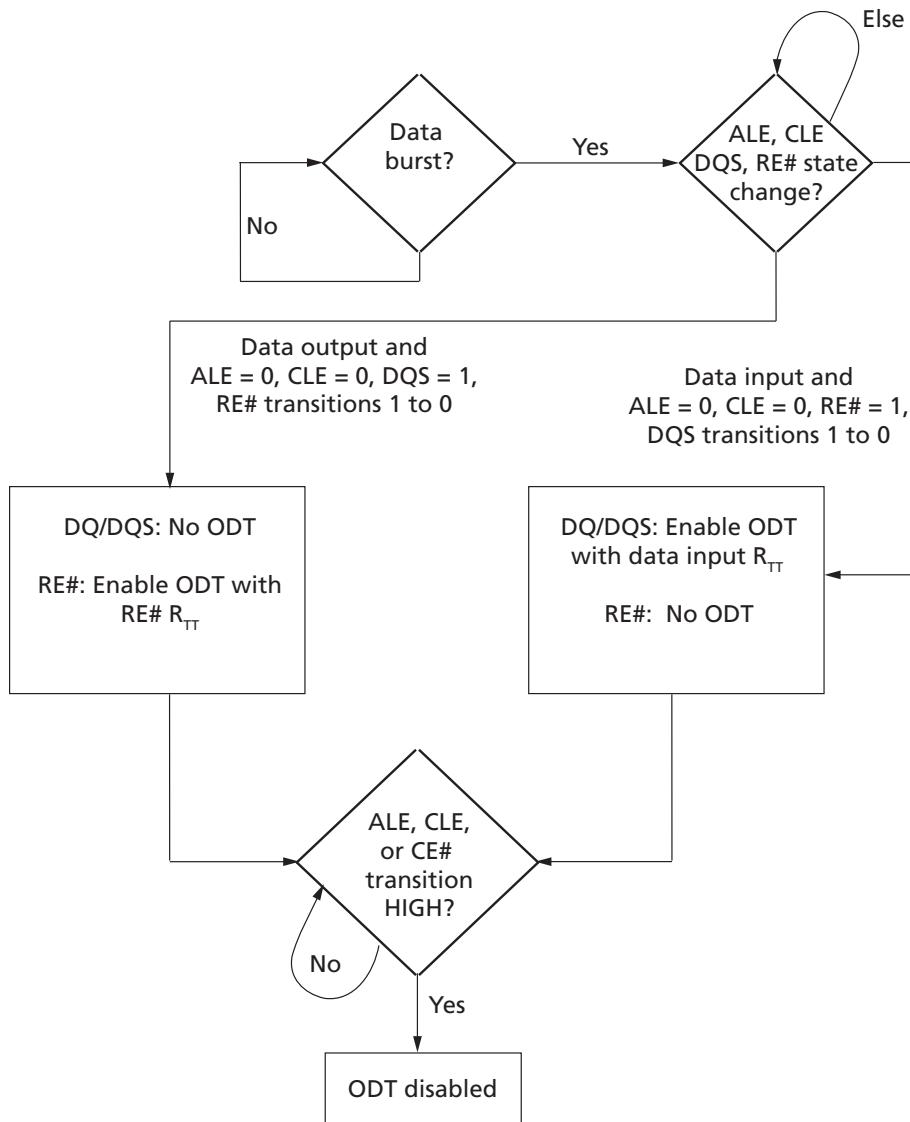
1. R_{TT2 (EFF)}, R_{TT3 (EFF)}, R_{TT4 (EFF)}, and R_{TT5 (EFF)} are determined by separately applying V_{IH(AC)} and V_{IL(AC)} to the signal being tested, and then measuring current I(V_{IH[AC]}) and I(V_{IL[AC]}), respectively. R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]}) / (I(V_{IH[AC]}) - I(V_{IL[AC]}))
2. Measure voltage (VM) at the tested signal with no load. ΔVM = [(2 x VM) / V_{CCQ}] x 100.

Self-termination On-die Termination (ODT)

When self-termination is enabled, the LUN that is executing the command provides on-die termination. Figure 30 (page 46) defines the self-termination only ODT enable and disable requirements for the LUN that is executing the command when ODT is selected for use via SET FEATURES (EFh) command. If the ODT CONFIGURE (E2h) command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to matrix termination.

Self-termination is applied to DQS and DQ[7:0] signals during data input operations and RE# during data output operations.

Release: 3/26/13

**Figure 30: Self-termination only ODT behavioral flow**

Matrix Termination

A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT CONFIGURE (E2h) command) may be located on the selected Volume as the Volume it is terminating for (Target termination) or a unselected Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in Table 7.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

Table 7: LUN state for Matrix Termination

LUN is on selected Volume?	Terminator for selected Volume?	LUN state	ODT actions defined
Yes	N/A	Selected	Figure 31
No	Yes	Sniff	Figure 32
No	No	Deselected	No ODT actions

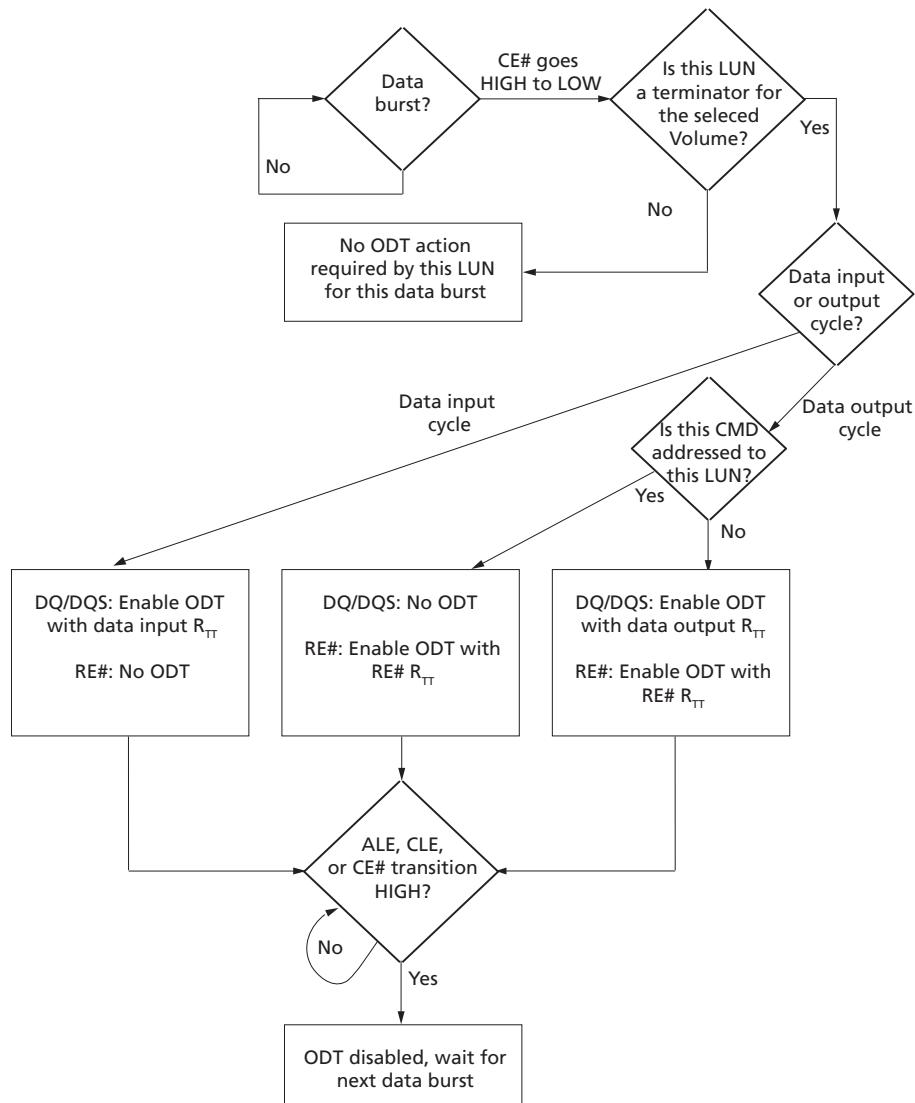
The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. Figure 31 (page 48) defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE# signals.

Release: 3/26/13



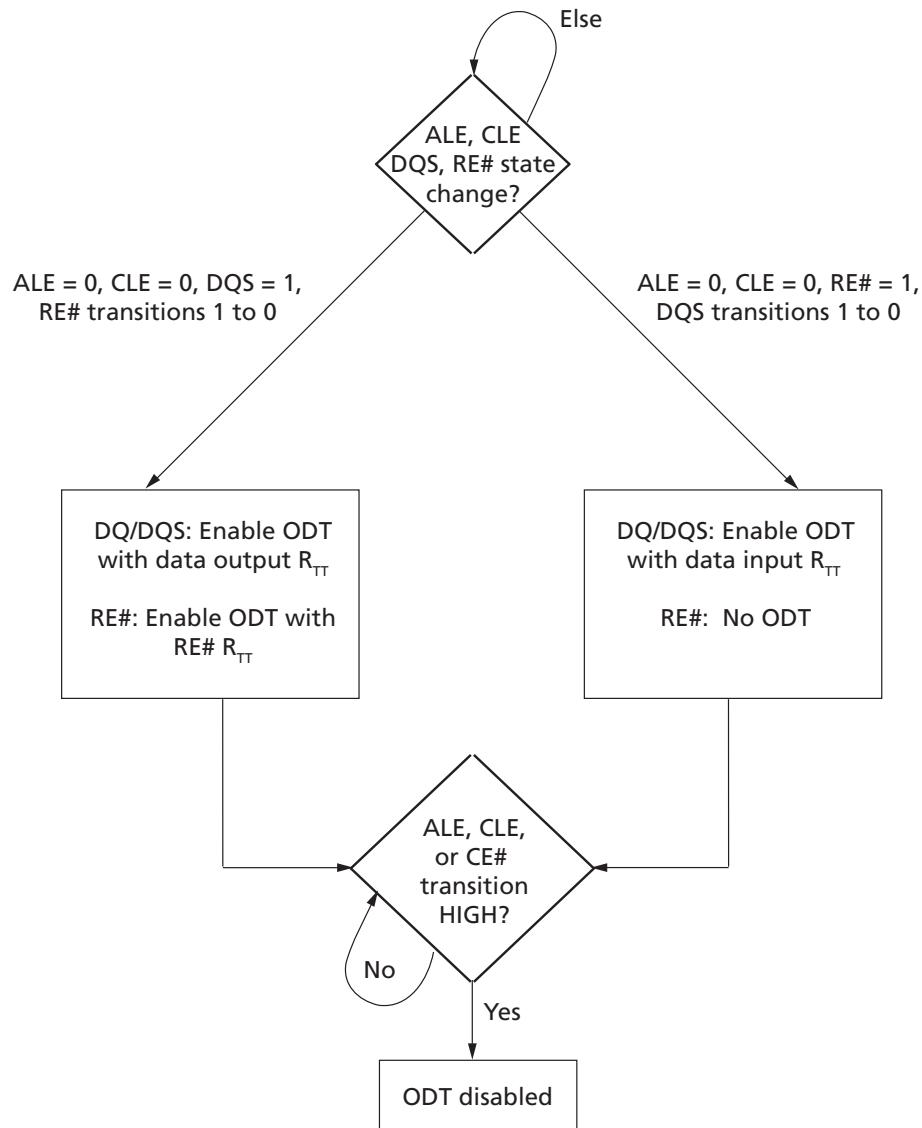
128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

Figure 31: ODT actions for LUNs on selected Volume



The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE# signals to determine when to enable or disable ODT. Figure 32 (page 49) defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

Release: 3/26/13

**Figure 32: ODT actions for LUNs in Sniff state on unselected Volume**

Matrix Termination Examples

This section describes two examples of on-die termination configurations using matrix termination. In both examples, each Volume consists of two LUNs, referred to as H0N_n-LUN0 and H0N_n-LUN1. The following Volume addresses were appointed at initialization.

Table 8: Volume appointment for Matrix Termination example

Volume	Appointed Volume Address
H0N0	0
H0N1	1
H0N2	2



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

Table 8: Volume appointment for Matrix Termination example (Continued)

Volume	Appointed Volume Address
H0N3	3

For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination R_{TT} values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Table 9: Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example

Input values for ODT CONFIGURE (E2h)					
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	Notes
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS
H0N0-LUN1	01h	00h	02h	03h	Terminates for Volume 0 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN0	02h	00h	02h	03h	Terminates for Volume 1 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN1	04h	00h	02h	03h	Terminates for Volume 2 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N3-LUN0	08h	00h	02h	03h	Terminates for Volume 3 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

Table 9: Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example (Continued)

		Input values for ODT CONFIGURE (E2h)				
LUN	Byte M0	Byte M1	Byte R _{TT1}	Byte R _{TT2}	Notes	
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R _{TT} value 50 Ohms for DQ[7:0]/DQS	

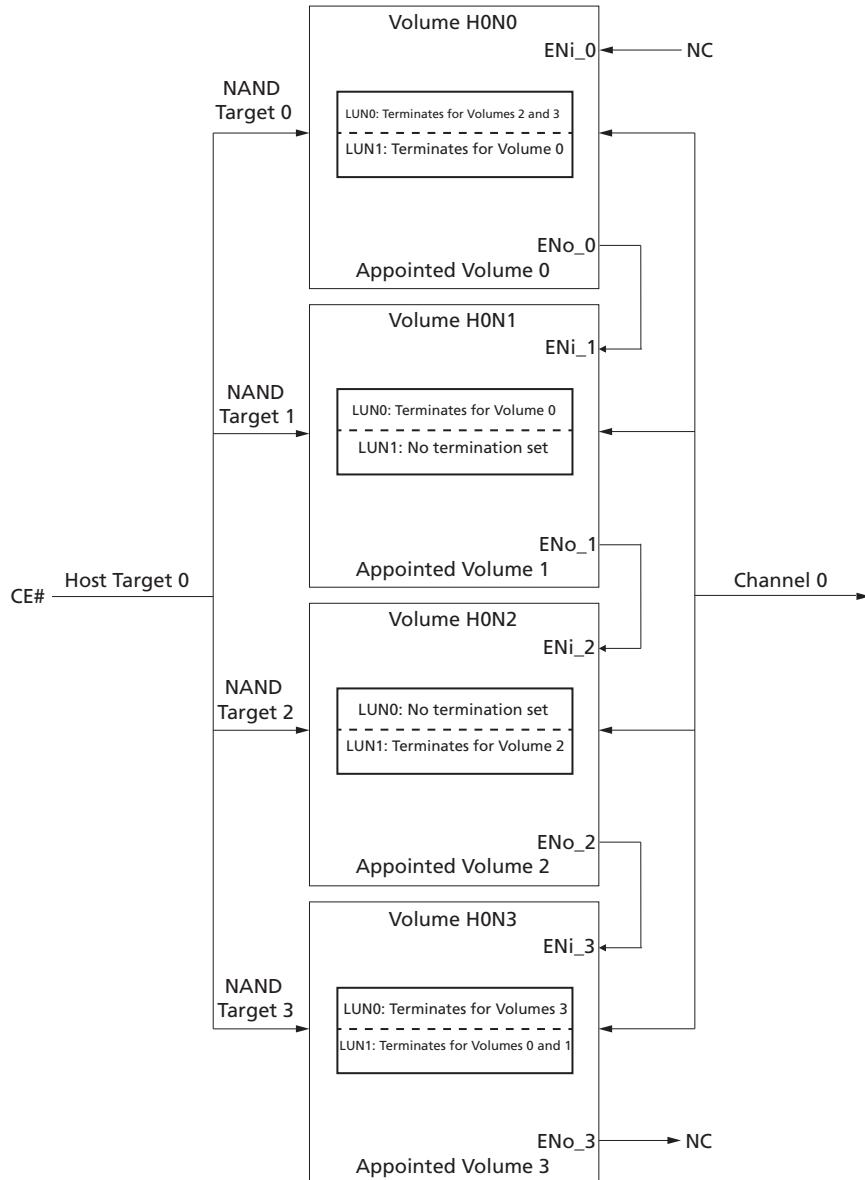
Note: 1. See ODT CONFIGURE (E2h) (page 111) for details on input values for ODT CONFIGURE (E2h).

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

Figure 33: Non-Target ODT for Data Output, Target ODT for Data Input configuration example



The second example uses parallel non-Target termination to achieve a stronger effective R_{TT} value for both data output and data input operations. For data output, two 50 Ohm terminators are used in parallel to achieve an effective 25 Ohms non-Target termination value. For data input, two 100 Ohm terminators are used in parallel to achieve an effective 50 Ohms non-Target termination value. This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate R_{TT} values with the use of different R_{TT} values for parallel LUNs. For example, if one terminator was configured for 75 Ohms and another terminator was configured for 100 Ohms for the same Volume then an effective R_{TT} value of 43 Ohms is achieved. In this example, parallel termination is used for data input and data output for

Release: 3/26/13



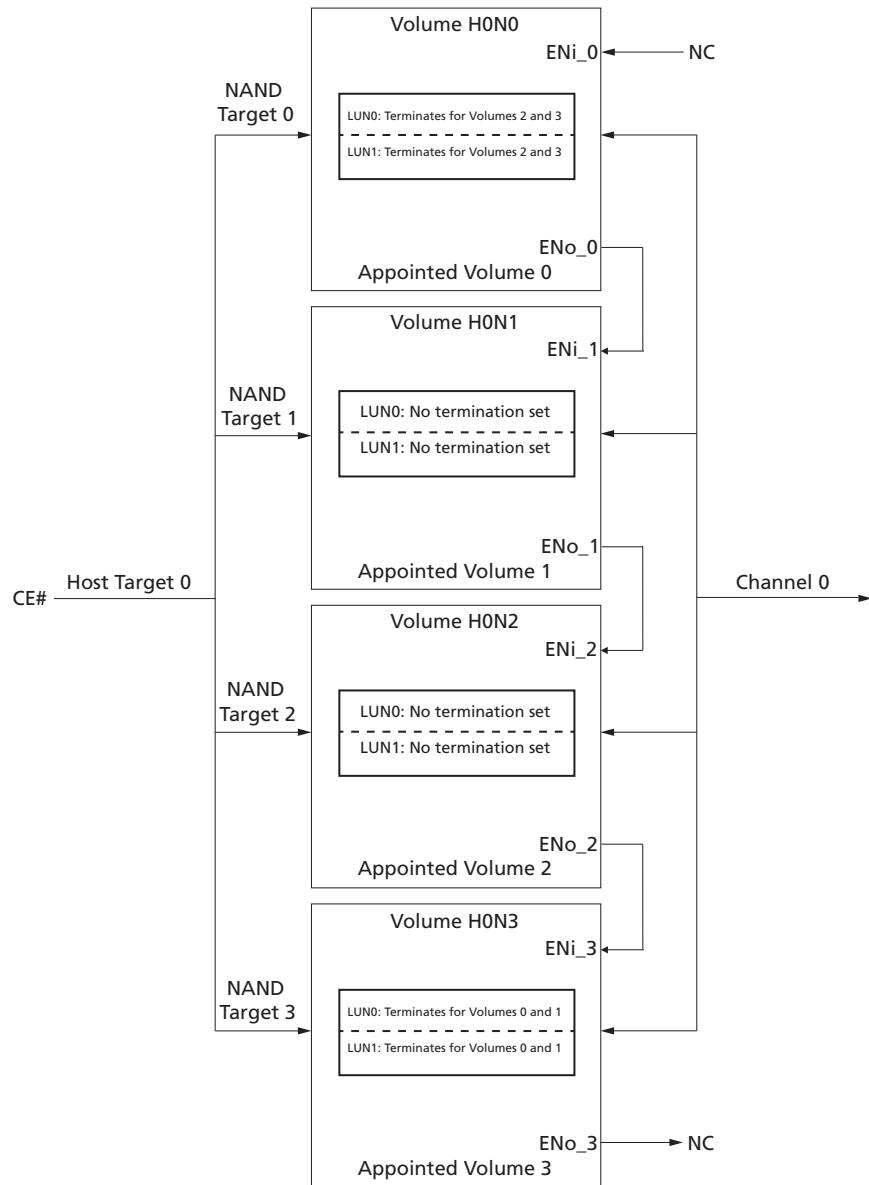
128Gb to 1Tb Asynchronous/Synchronous NAND Bus Operation – NV-DDR2 Interface

DQ[7:0]/DQS, however, RE# is non-Target terminated with 100 Ohms using a single LUN.

Table 10: Parallel Non-Target ODT settings configuration example

LUN	Input values for ODT CONFIGURE (E2h)				Notes
	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	
H0N0-LUN0	0Ch	00h	42h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R _{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an R _{TT} value of 100 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	0Ch	00h	42h	01h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R _{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R _{TT} value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) with an R _{TT} value of 150 Ohms for RE#.
H0N1-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N1-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N3-LUN0	03h	00h	42h	01h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R _{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R _{TT} value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) with an R _{TT} value of 150 Ohms for RE#.
H0N3-LUN1	03h	00h	42h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R _{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R _{TT} value of 100 Ohms for DQ[7:0]/DQS.

Release: 3/26/13


Figure 34: Parallel Non-Target ODT configuration example


NV-DDR2 Standby

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

Release: 3/26/13



NV-DDR2 Idle

A target's bus is idle when CE# is LOW, ALE is LOW, CLE is LOW, RE# is HIGH, and DQS is HIGH and no internal LUN operations are ongoing or data being inputted or outputted from the target. DQS is driven HIGH to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Pausing Data Input/Output

Pausing data input or data output may be done by placing the bus in an Idle state. The pausing of data output may also be done by pausing RE# and holding the signal(s) static HIGH or LOW until the data burst is resumed. The pausing of data input may also be done by pausing DQS and holding the signal(s) static HIGH or LOW until the data burst is resumed. WE# shall be held HIGH during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause. The host will be required to exit the data burst if it wishes to disable ODT or re-issue warmup cycles when re-starting. If the host wishes to end the data burst, after exiting the data burst, a new command is issued.

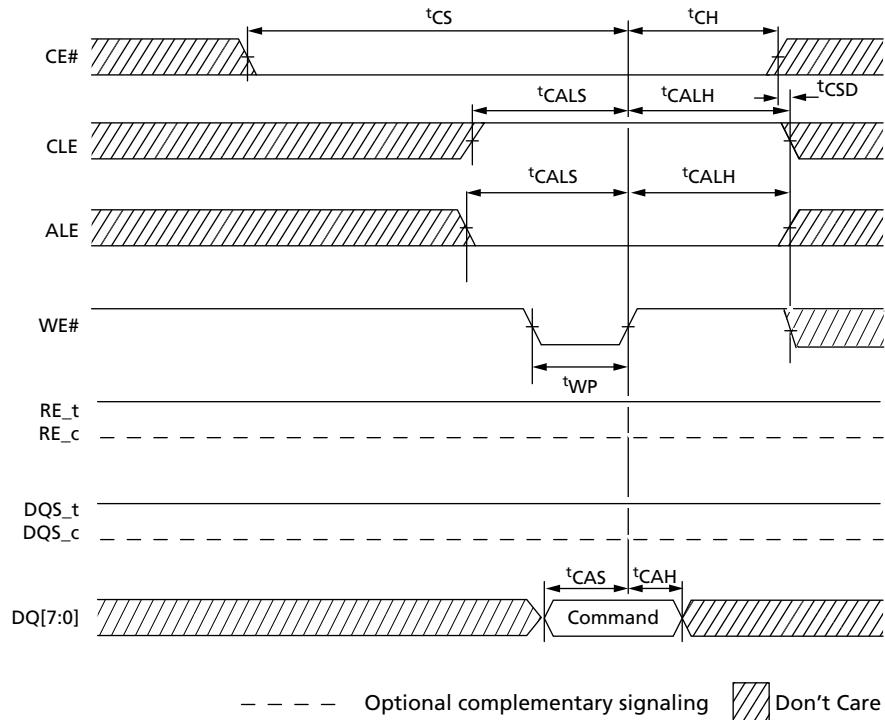
During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Release: 3/26/13

**Figure 35: NV-DDR2 Command Cycle**

NV-DDR2 Addresses

A NV-DDR2 address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

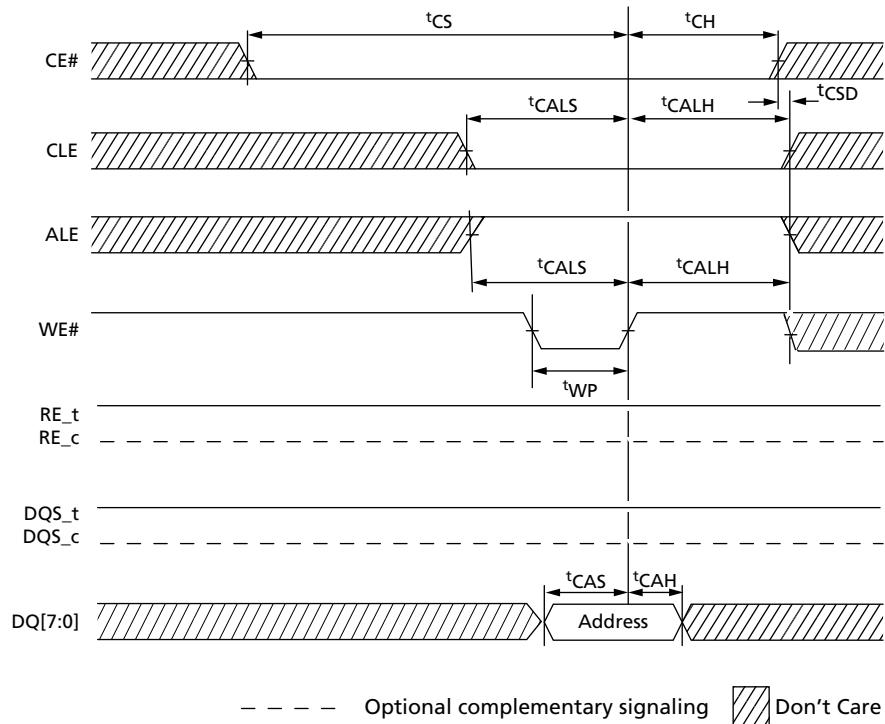
Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Release: 3/26/13



Figure 36: NV-DDR2 Addresses Cycle



NV-DDR2 Data Input

To enter the NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- t_{WPRE} is met
- DQS is LOW

Upon entering the NV-DDR2 data input mode after t_{WPRE} , data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CE# is LOW, RE# is HIGH, and ALE and CLE are LOW.

To exit NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence
- DQS is held LOW for t_{WPST} (after the final falling edge of DQS)

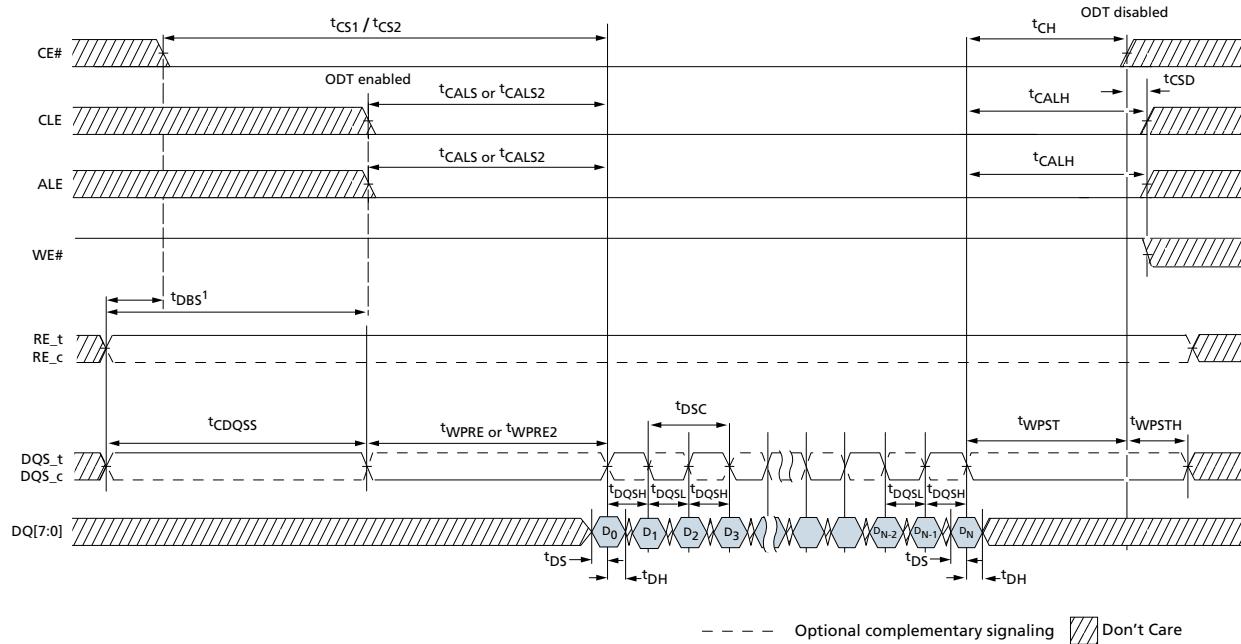
Following t_{WPST} , the bus enters bus idle mode.

Release: 3/26/13



Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 37: NV-DDR2 Data Input Cycles



Note: 1. ODT may not be required to be used for data input. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.

NV-DDR2 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

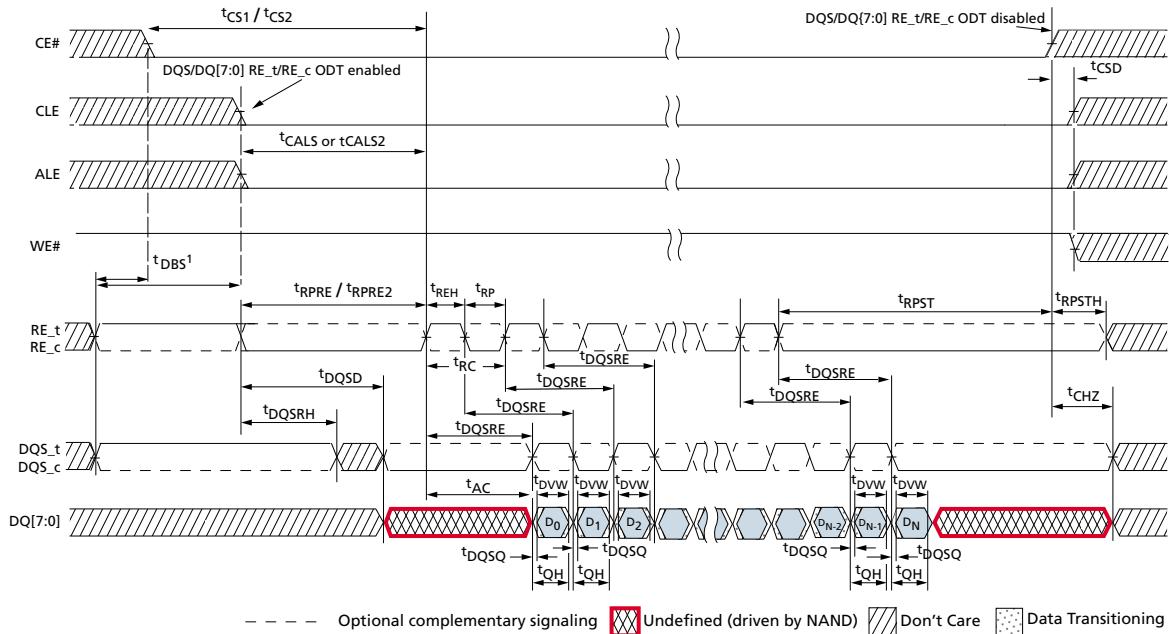
To enter the NV-DDR2 data output mode, the following conditions must be met:

- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- ALE and CLE are LOW
- t_{RPRE} is met

Upon entering the NV-DDR2 data output mode, DQS will toggle HIGH and LOW with a delay of t_{DQSRE} from the respective rising and falling edges of RE#. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than t_{AC}.

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur t_{DQSRE} after the last cycle in the data output sequence. The host must hold RE# for t_{RPST} after the last RE# falling edge for data output.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

**Figure 38: NV-DDR2 Data Output Cycles**

Note: 1. ODT may not be required to be used for data output. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.

Write Protect

See Write Protect under Bus Operations - Asynchronous Interface.

Ready/Busy#

See Ready/Busy# under Bus Operations - Asynchronous Interface.

Release: 3/26/13



Device Initialization

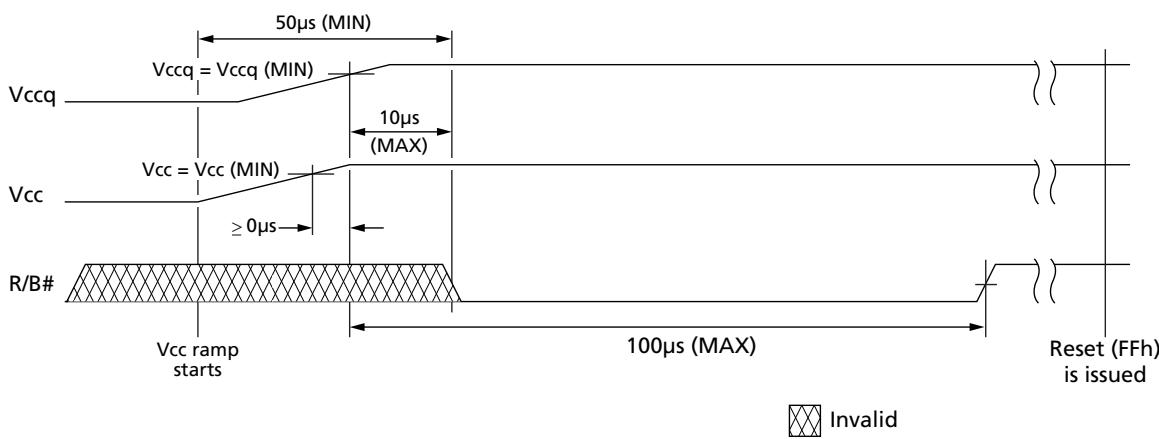
Some NAND Flash devices do not support V_{CCQ}. For these devices all references to V_{CCQ} are replaced with V_{CC}.

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. Ramp V_{CCQ}. V_{CCQ} must not exceed V_{CC}.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 39). The R/B# signal becomes valid when 50μs has elapsed since the beginning the V_{CC} ramp, and 10μs has elapsed since V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN).
4. If not monitoring R/B#, the host must wait at least 100μs after V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
5. The asynchronous interface is active by default for each target. Each LUN draws less than an average of I_{ST} measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for t_{POR} after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
7. The device is now initialized and ready for normal operation.

At power-down, V_{CCQ} must go LOW, either before, or simultaneously with, V_{CC} going LOW.

Figure 39: R/B# Power-On Behavior



Note: 1. Disregard V_{CCQ} for devices that use only V_{CC}.

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corre-



128Gb to 1Tb Asynchronous/Synchronous NAND Device Initialization

sponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETET PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

Release: 3/26/13



V_{PP} Initialization

Some NAND Flash devices do not support V_{PP}.

Micron NAND Flash devices support the V_{PP} signal as a way for the host system to enhance NAND array operations by improving power efficiency. When ramping V_{PP}, use the following procedure to initialize the V_{PP} functionality:

1. V_{CC} must be successfully ramped prior to the start of ramping V_{PP}.
2. Ramp V_{PP}.
3. V_{PP} must be within its valid range prior to the SET FEATURES (EFh) command to enable the V_{PP} functionality.
4. After V_{PP} is successfully ramped and before V_{PP} functionality can be carried out the V_{PP} feature must be activated via a SET FEATURE (EFh) command. See the Configurations Operations section for more details.

At power-down, V_{PP} must reach 0V before V_{CC} (MIN) is reached.

Release: 3/26/13



Activating Interfaces

After performing the steps under (page 0), the asynchronous interface is active for all targets on the device.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface, then steps under Activating the Asynchronous Interface are performed to re-synchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, once the synchronous interface is active, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for t_{RST} .
4. After t_{ITC} , and during t_{RST} , the device enters the asynchronous NAND interface. READ STATUS (70h) and READ STATUS ENHANCED (78h) are the only commands that can be issued.
5. After t_{RST} , R/B# goes HIGH. Timing mode feature address (01h), subfeature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

For further details, see Reset Operations.

Activating the NV-DDR Interface

To activate the NV-DDR NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 1Xh, where "X" is the timing mode used in the NV-DDR interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for t_{ITC} . The host should pull CE# HIGH. During t_{ITC} , the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After t_{ITC} , R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Activating the NV-DDR2 Interface

Transitions from NV-DDR directly to NV-DDR2 (or vice versa) is not supported. In this case, the host should transition to the asynchronous interface and then select the desired synchronous interface

Prior to selecting the NV-DDR2 interface, it is recommended that settings for the NV-DDR2 interface be configured. Specifically:



128Gb to 1Tb Asynchronous/Synchronous NAND Activating Interfaces

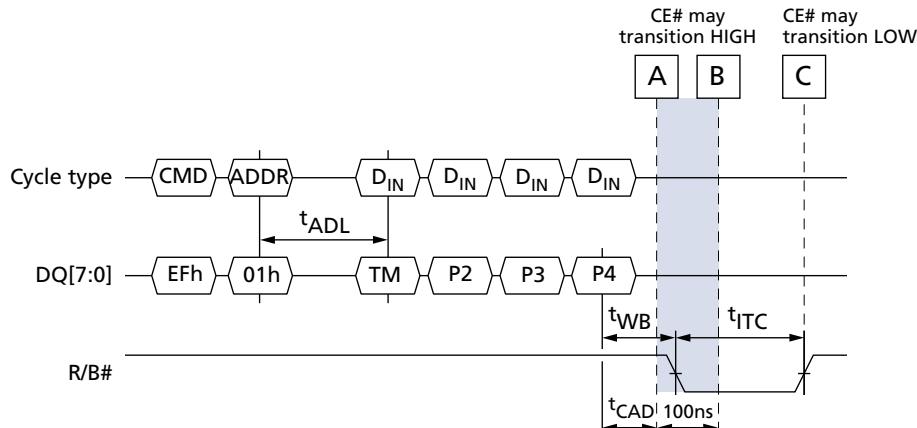
- SET FEATURES (EFh) command should be used to configure the NV-DDR2 Configuration feature address.
- If on-die termination (ODT) is used, the appropriate ODT CONFIGURE (E2) commands should be issued.

These actions should be completed prior to selecting the NV-DDR2 interface. If these settings are modified when the NV-DDR2 interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

To activate the NV-DDR2 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 2Xh, where "X" is the timing mode used in the NV-DDR2 interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for t_{ITC} . The host should pull CE# HIGH. During t_{ITC} , the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After t_{ITC} , R/B# goes HIGH and the NV-DDR2 interface is enabled.

Figure 40: Activating Interfaces



Note: 1. TM = Timing mode.

Release: 3/26/13



CE# Pin Reduction and Volume Addressing

In higher density capacity implementations there may be a significant number of CE# pins required for a host to support where there are many NAND packages with two to four CE# pins per package. The CE# pin reduction mechanism enables a single CE# pin from the host to be shared by multiple NAND targets, thus enabling a significant reduction in the number of CE# pins required by the host system. The CE# pin reduction mechanism may be utilized with any data interface (asynchronous, NV-DDR, NV-DDR2).

In the CE# pin reduction mechanism, each NAND package is appointed a volume address during the initialization sequence. After initialization is complete, the host may address a particular volume (NAND target) by using the VOLUME SELECT (E1h) command. See VOLUME SELECT (E1h) for more details.

ENi and ENo pins are added to each NAND package and a daisy chain is created between NAND packages. The first NAND package in the chain has the ENi pin as not connected. All other NAND packages have their ENi pin connected to the previous package's ENo pin in a daisy chain configuration.

At power-on, the ENo pins are driven LOW by the NAND device. ENo shall be High-Z when all CE# signals on the NAND package are HIGH. When a NAND target has had a volume address appointed with the SET FEATURES (EFh) command, then the ENo pin shall be pulled HIGH by the NAND target when the corresponding CE# is LOW. This enables the next NAND target on a subsequent package in the daisy chain to accept commands because the ENi pin pulls HIGH when ENo is no longer pulling LOW. After a volume address has been appointed to a volume (i.e., NAND target), that volume shall become deselected and ignores the ENi pin until the next power cycle.

The state of ENi determines whether the NAND package is able to accept commands. If the ENi pin is HIGH and CE# is LOW for the NAND target, then the NAND target shall accept commands. If the ENi pin is LOW or CE# is HIGH for the NAND Target, then the NAND Target shall not accept commands.

To be selected to process a command, the VOLUME SELECT command shall be issued to the host target using the volume address that was previously appointed for a particular NAND target. After the CE# signal is pulled HIGH for tCEH time, all LUNs on a volume revert to their previous states.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND CE# Pin Reduction and Volume Addressing

Figure 41: CE# Pin Reduction Topology with Single Channel

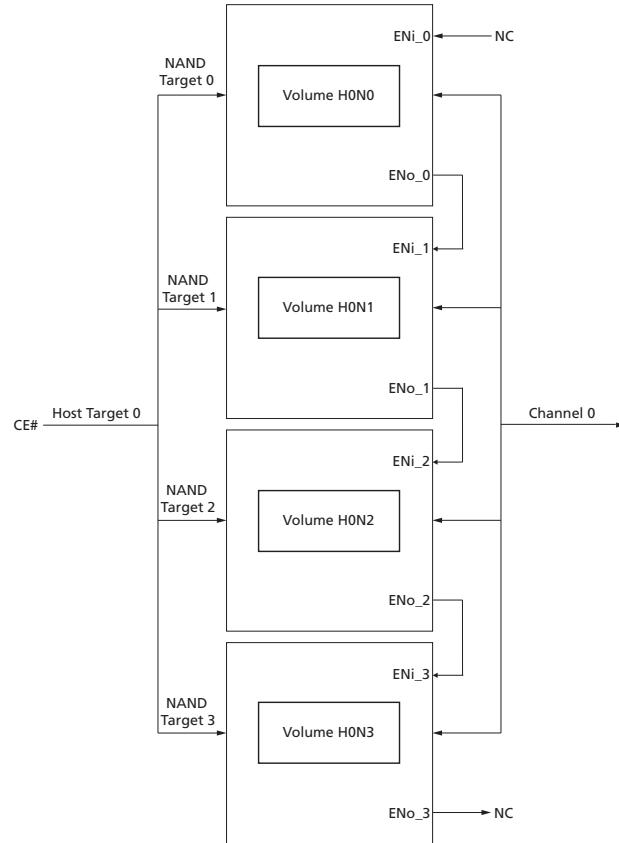
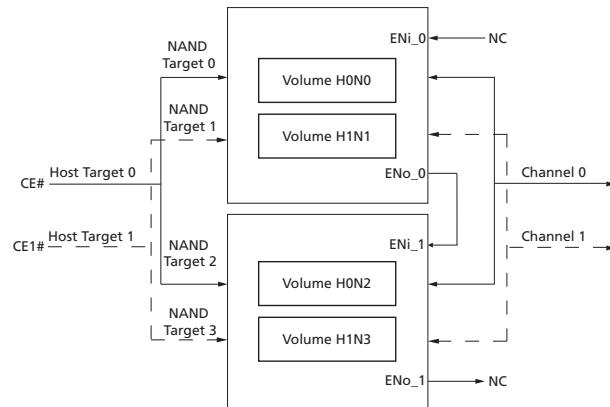


Figure 42: CE# Pin Reduction and Volume Addressing Topology with Dual Channel



Release: 3/26/13



Initialization Sequence

The host may issue a RESET (FFh) to all targets in parallel on the selected host target, or the host may sequentially issue RESET (FFh) to each target. The methodology chosen depends on host requirements for maximum current draw. To reset all targets in parallel, the host issues a RESET (FFh) as the first command issued to the NAND device(s). To reset targets sequentially, the host issues a READ STATUS (70h) command as the first command issued to all NAND targets on the selected host target.

During initialization when addressing a newly selected NAND target with an initial command, the host shall wait for the ENo signal to be propagated to the ENi of the subsequent target. Before addressing a new target, the host shall wait ($t_{ENo} + t_{ENi}$) and should also include signal propagation time.

In cases where there are multiple NAND targets within a package (multiple CE#), those NAND targets share the same ENo signal, and the host shall not stagger SET FEATURES (EFh) commands that appoint the volume addresses. If the SET FEATURES (EFh) commands are not issued simultaneously, then the host shall wait until volume appointment for previous NAND target(s) is complete before issuing the next SET FEATURES (EFh) command to appoint the volume address for the next NAND target that shares the ENo within a package.

After issuing the SET FEATURE (EFh) command to appoint the volume address, the host shall not issue another command to any NAND target on the associated host target (including status commands) until after the t_{FEAT} time has elapsed. This is to ensure that the proper NAND target responds to the next command, allowing for the proper ENo/ENi signal levels to be reflected.

The initialization sequence when utilizing the CE# reduction functionality is as follows:

1. The host powers on the NAND device(s).
2. The host pulls CE# LOW.
3. If resetting all NAND targets in parallel, then the host issues the RESET (FFh) command. This command is accepted by all NAND targets connected to the CE# (host target).
4. If resetting each NAND target sequentially, then:
 - a. The host issues the READ STATUS (70h) command to check for ready status. Issuing the READ STATUS (70h) command prior to any other command indicates sequential RESET (FFh) of each NAND target. The host then issues the RESET (FFh) command, which is only accepted by NAND devices with ENi set HIGH.
5. R/B# goes LOW for t_{RST} and can be monitored by the host by issuing READ STATUS (70h) commands and monitoring
6. The host configures the NAND target via commands necessary to perform that function (READ PARAMETER PAGE (ECh) command, SET FEATURES (EFh) command, etc.).
7. The host issues SET FEATURES (EFh) command to the volume configuration feature address to appoint the volume address for the NAND target. The volume address specified shall be unique amongst all NAND targets. After the SET FEATURE (EFh) command completes, ENo is set to one and the volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the volume. The host shall not issue another command to a NAND target connected to the associated host target until after t_{FEAT} time has elapsed.
8. For each NAND target connected to a host target, steps 4–7 are repeated for sequential initialization, and steps 5–7 are repeated for parallel initialization.



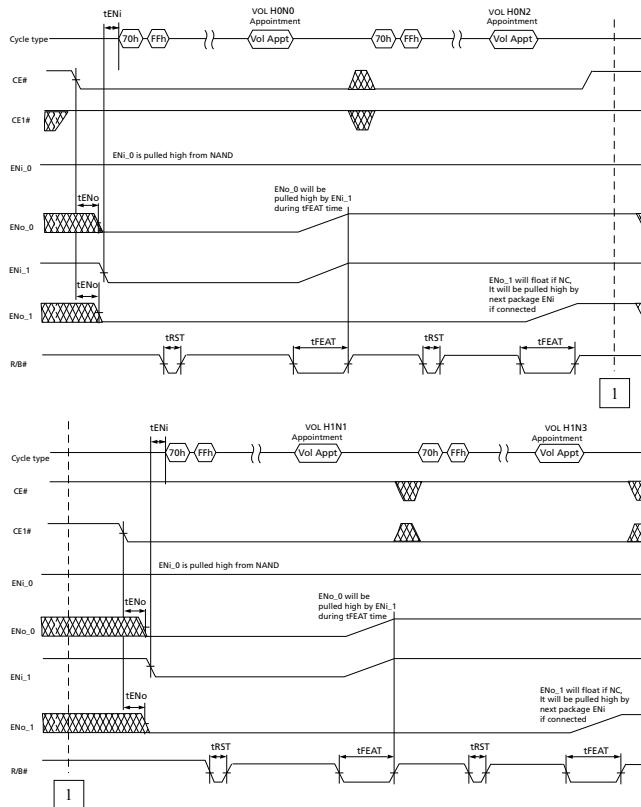
128Gb to 1Tb Asynchronous/Synchronous NAND CE# Pin Reduction and Volume Addressing

9. When no further NAND targets are found connected to the host target, then repeat steps 2–8 for the next host target (i.e., host CE# pin).
10. To complete the initialization process, a VOLUME SELECT (E1h) command is issued to select the next volume that is going to execute a command.

After volume addresses have been appointed to all NAND targets, the host may complete any additional initialization tasks (for example, configure on-die termination (ODT) for NV-DDR2 mode) and then proceed with normal operation. Prior to issuing a command to a volume, the VOLUME SELECT (E1h) command shall be issued.

Figure 43 (page 68) is an example of sequential reset initialization for the CE# pin reduction topology of Figure 42 (page 66).

Figure 43: Example of Sequential Reset Initialization



Volume Appointment Without CE# Pin Reduction

If CE# pin reduction is not used (for example, if ENI and ENo are not connected) and the host desires to have the terminator on a package that does not share a CE# with the selected NAND target, then each package that shares the CE# must have a volume appointed at initialization using the SET FEATURE (EFh) command using the volume configuration feature.

Each CE# must have a unique volume address appointed. Once all NAND targets have volume addresses appointed, the appointed volume addresses may be used for termination selection. Volume addressing is not required for operation due to discrete CE#.

Release: 3/26/13

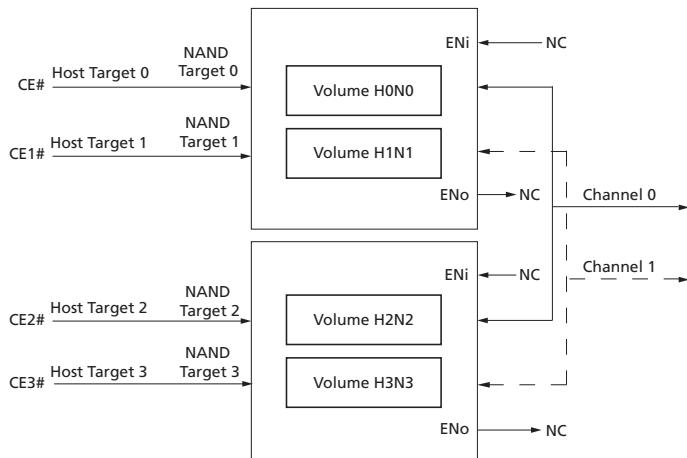


Release: 3/26/13

signals; however, the VOLUME SELECT (E1h) command is required for terminator selection when using non-target termination schemes.

During operation, the CE# signal for the selected Volume and for any NAND targets assigned as a terminator for the selected volume need to be brought LOW. When CE# is brought LOW for an unselected volume, all LUNs that are not assigned as terminators for the selected volume are deselected.

Figure 44: Volume Addressing Without CE# Pin Reduction Topology with Dual Channel



Appointing Volume Addresses

To appoint a volume address, the SET FEATURE command is issued with a feature address of volume configuration. The volume address is not retained across power cycles; thus, if volume addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s).

Selecting a Volume

After volume addresses have been appointed, every NAND target (and associated LUN) is selected when the associated CE# is pulled LOW. The host issues a VOLUME SELECT (E1h) command to indicate the volume (NAND target) that shall execute the next command issued.

Multiple Volume Operation Restrictions

Volumes are independent entities. A multiple volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected volume, CE# shall be pulled HIGH for a minimum of tCEH, and the VOLUME SELECT (E1h) command shall then be issued to select the volume to issue a command to next. While commands (including multi-LUN operations) are being performed on the selected volume, a VOLUME SELECT (E1h) command is not required.

Issuing the same command to multiple volumes at the same time is not supported.

For a LUN level command (e.g., READ, PROGRAM), the host may select a different volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command. When re-selecting a Volume and as-



Release: 3/26/13

sociated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall issue a CHANGE ROW ADDRESS (85h) command prior to resuming data input.
- Data output: The host shall issue a CHANGE READ COLUMN ENHANCED (06h-E0h) or RANDOM DATA OUT (00h-05h-E0h) command prior to resuming data output.

For a target level command (GET FEATURES (EEh), SET FEATURES (EFh)), the host shall complete all data input or data output operations associated with that command prior to selecting a new volume.

A VOLUME SELECT command shall not be issued during the following atomic portions of the COPYBACK, READ, PROGRAM, and ERASE operations:

- READ operations:
 - READ PAGE (00h-30h)
 - COPYBACK READ (00h-35h)
 - READ PAGE MULTI-PLANE (00h-32h)
 - READ PAGE CACHE RANDOM (00h-31h)
- PROGRAM operations, note: The VOLUME SELECT (E1h) command may be issued prior to the 10h, 11h, or 15h command if the next command to this volume is CHANGE ROW ADDRESS (85h):
 - PROGRAM PAGE (80h-10h)
 - PROGRAM PAGE MULTI-PLANE (80h/81h-11h)
 - PROGRAM PAGE CACHE (80h-15h)
 - COPYBACK PROGRAM (85h-10h)
 - COPYBACK PROGRAM MULTI-PLANE (85h-11h)
- ERASE operations:
 - ERASE BLOCK (60h-D0h)
 - ERASE BLOCK MULTI-PLANE (60h-D1h or 60h-60h-D0h)

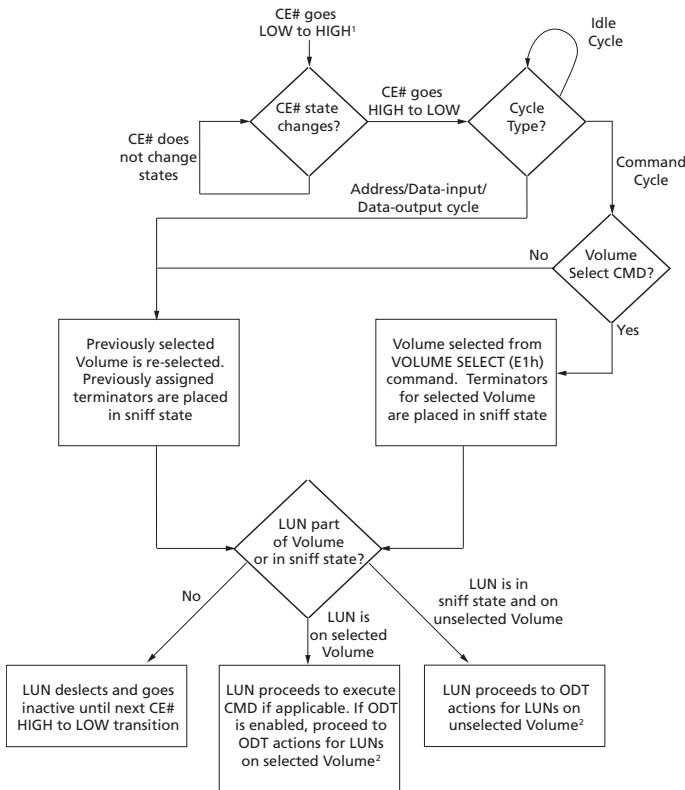
Volume Reversion

When using volume addressing, the LUNs shall support Volume reversion. Specifically, if CE# is transitioned from HIGH to LOW and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states based on the last specified volume address. If on-die termination is enabled when using the NV-DDR2 data interface there are additional actions described within On Die Termination (ODT).



128Gb to 1Tb Asynchronous/Synchronous NAND CE# Pin Reduction and Volume Addressing

Figure 45: Volume Reversion behavioral flow



- Notes:
1. This state is entered asynchronously when CE# transitions from LOW to HIGH.
 2. ODT actions for LUNs on a selected Volume are specified in Figure 31 (page 48). ODT actions for LUNs on an unselected Volume are specified in Figure 32 (page 49).

Release: 3/26/13



Command Definitions

Table 11: Command Set

Command	Com-mand Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Com-mand Cycle #2	Number of Valid Address Cycles #2	Com-mand Cycle #3	Valid While Seเลcted LUN is Busy ¹	Valid While Other LUNs are Busy ²	Notes
Reset Operations									
RESET	FFh	0	–	–	–	–	Yes	Yes	
SYNCHRONOUS RE-SET	FCh	0	–	–	–	–	Yes	Yes	
RESET LUN	FAh	3	–	–	–	–	Yes	Yes	
Identification Operations									
READ ID	90h	1	–	–	–	–			3
READ PARAMETER PAGE	ECh	1	–	–	–	–			
READ UNIQUE ID	EDh	1	–	–	–	–			
Configuration Operations									
VOLUME SELECT	E1h	1	–	–	–	–			
ODT CONFIGURE	E2h	1	4	–	–	–			
GET FEATURES	EEh	1	–	–	–	–			3
SET FEATURES	EFh	1	4	–	–	–			4
Status Operations									
READ STATUS	70h	0	–	–	–	–	Yes		
READ STATUS EN-HANCED	78h	3	–	–	–	–	Yes	Yes	
Column Address Operations									
CHANGE READ COL-UMN	05h	2	–	E0h	–	–		Yes	
CHANGE READ COL-UMN ENHANCED (ONFI)	06h	5	–	E0h	–	–		Yes	
CHANGE READ COL-UMN ENHANCED (JEDEC)	00h	5	–	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	–	–	–		Yes	
CHANGE ROW AD-DRESS	85h	5	Optional	11h (Op-tional)	–	–		Yes	5
Read Operations									
READ MODE	00h	0	–	–	–	–		Yes	
READ PAGE	00h	5	–	30h	–	–		Yes	6

Release: 3/26/13

**Table 11: Command Set (Continued)**

Command	Com- mand Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Com- mand Cycle #2	Number of Valid Address Cycles #2	Com- mand Cycle #3	Valid While Se- lected LUN is Busy¹	Valid While Oth- er LUNs are Busy²	Note s
READ PAGE MULTI- PLANE	00h	5	–	32h	–	–		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	–	–		Yes	7
READ PAGE CACHE RANDOM	00h	5	–	31h	–	–		Yes	6,7
READ PAGE CACHE LAST	3Fh	0	–	–	–	–		Yes	7
Program Operations									
PROGRAM PAGE	80h	5	Yes	10h				Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5	Yes	11h				Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h				Yes	8
Erase Operations									
ERASE BLOCK	60h	3	–	D0h				Yes	
ERASE BLOCK MULTI-PLANE (ON- FI)	60h	3	–	D1h				Yes	
ERASE BLOCK MUL- TI-PLANE (JEDEC)	60h	3	–	60h	3	D0h		Yes	
Copyback Operations									
COPYBACK READ	00h	5	–	35h				Yes	6
COPYBACK PRO- GRAM	85h	5	Optional	10h				Yes	
COPYBACK PRO- GRAM MULTI- PLANE	85h	5	Optional	11h				Yes	

- Notes:
1. Busy means RDY = 0.
 2. These commands can be used for interleaved die (multi-LUN) operations.
 3. The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
 4. The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
 5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) (page 121) for more details.
 6. This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
 7. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Command Definitions

8. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.

Release: 3/26/13



Reset Operations

RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are busy.

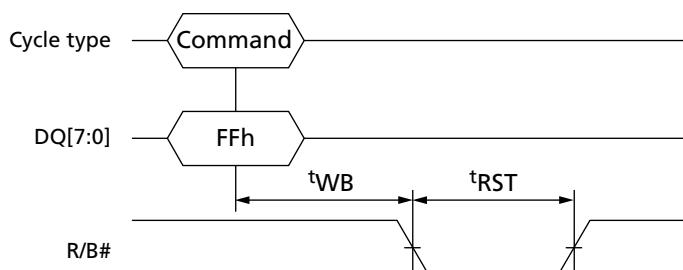
When FFh is written to the command register, the target goes busy for t_{RST} . During t_{RST} , the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

RESET must be issued as the first command to each target following power-up (see Device Initialization). Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when the target is ready, use READ STATUS (70h).

If the RESET (FFh) command is issued when the synchronous interface is enabled, the target's interface is changed to the asynchronous interface and the timing mode is set to 0. The RESET (FFh) command can be issued asynchronously when the synchronous interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during t_{ITC} . After t_{ITC} , and during or after t_{RST} , the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after t_{RST} , the host can poll each LUN's status register.

Figure 46: RESET (FFh) Operation





SYNCHRONOUS RESET (FCh)

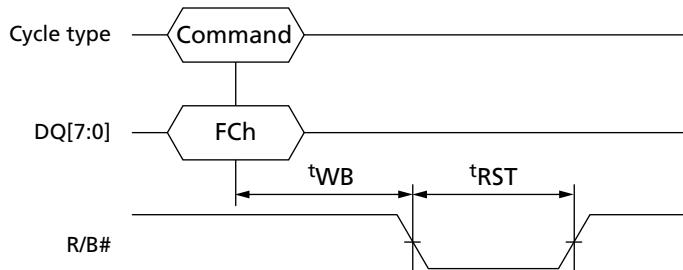
When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are BUSY.

When FCh is written to the command register, the target goes busy for t_{RST} . During t_{RST} , the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid and the synchronous interface remains active.

During or after t_{RST} , the host can poll each LUN's status register.

SYNCHRONOUS RESET is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.

Figure 47: SYNCHRONOUS RESET (FCh) Operation



Release: 3/26/13



RESET LUN (FAh)

The RESET LUN (FAh) command is used to put a particular LUN on a target into a known condition and to abort command sequences in progress. This command is accepted by only the LUN addressed by the RESET LUN (FAh) command, even when that LUN is busy.

When FAh is written to the command register, the addressed LUN goes busy for t_{RST} . During t_{RST} , the selected LUN discontinues all array operations. All pending single- and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on the addressed LUN, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

If the RESET LUN (FAh) command is issued when the synchronous interface is enabled, the target's interface remains in synchronous mode.

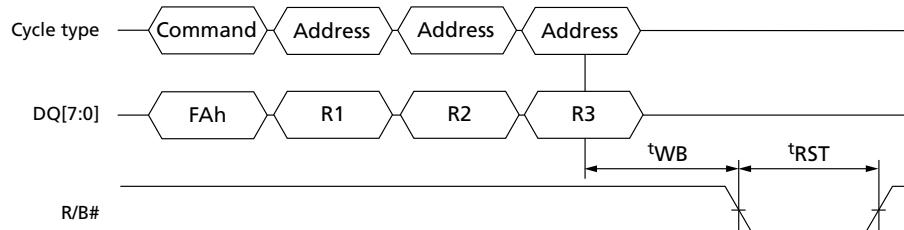
If the RESET LUN (FAh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode.

During or after t_{RST} , the host can poll each LUN's status register.

The RESET LUN (FAh) command is prohibited when not in the default array operation mode.

The RESET LUN (FAh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up.

Figure 48: RESET LUN (FAh) Operation





Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

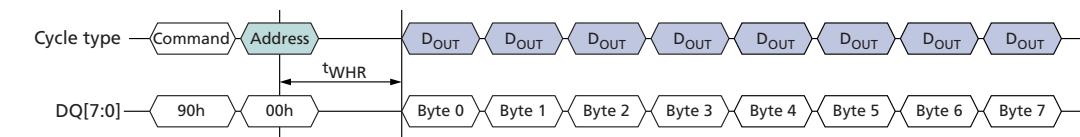
When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

When the 90h command is followed by a 40h address cycle, the target returns the 5-byte JEDEC identifier code.

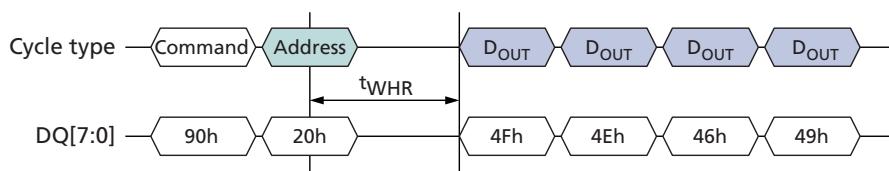
After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 49: READ ID (90h) with 00h Address Operation



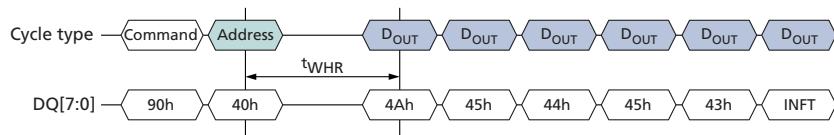
Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 50: READ ID (90h) with 20h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 51: READ ID (90h) with 40h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

READ ID Parameter Tables

Table 12: Read ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
MT29F128G08CBCAB	2Ch	84h	64h	3Ch	A5h	00h	00h	00h
MT29F128G08CBEAB	2Ch	84h	64h	3Ch	A5h	00h	00h	00h
MT29F256G08CECAB	2Ch	84h	64h	3Ch	A5h	00h	00h	00h
MT29F256G08CEEAB	2Ch	84h	64h	3Ch	A5h	00h	00h	00h
MT29F512G08CKCAB	2Ch	A4h	E5h	3Ch	A5h	00h	00h	00h
MT29F512G08CKEAB	2Ch	A4h	E5h	3Ch	A5h	00h	00h	00h
MT29F512G08CMCAB	2Ch	84h	64h	3Ch	A5h	00h	00h	00h
MT29F512G08CMEAB	2Ch	84h	64h	3Ch	A5h	00h	00h	00h
MT29F1T08CUCAB	2Ch	A4h	E5h	3Ch	A5h	00h	00h	00h
MT29F1T08CUEAB	2Ch	A4h	E5h	3Ch	A5h	00h	00h	00h

Note: 1. h = hexadecimal.

Table 13: Read ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
All	4Fh	4Eh	46h	49h	XXh

Notes: 1. h = hexadecimal.
2. XXh = Undefined.

Table 14: Read ID Parameters for Address 40h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Asynchronous or Synchronous	4Ah	45h	44h	45h	43h	05h

Note: 1. h = hexadecimal.

Release: 3/26/13



READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI or JEDEC parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h or 40h address cycle, the target goes busy for t^R . If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

After t^R completes, the host enables data output mode to read the parameter page. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

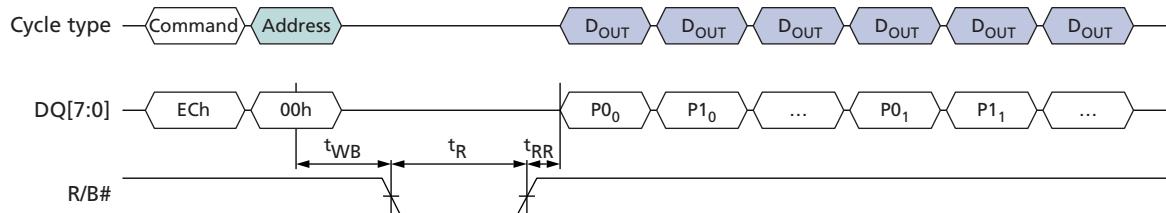
A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h) command is prohibited.

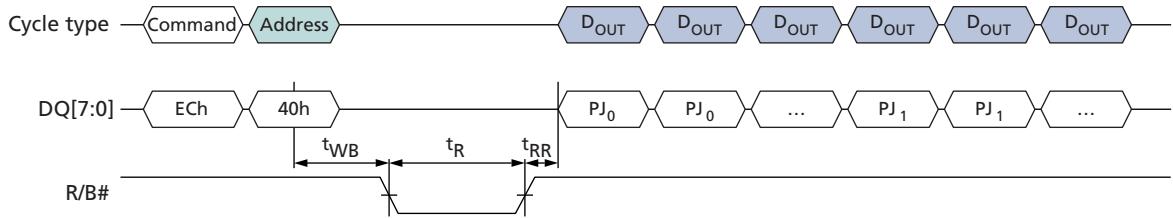
The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. Parameter pages returned by the target may have invalid CRC values; however, bit-wise majority may be used to recover the contents of the parameter page. The host may use bit-wise majority or other techniques to recover the contents of the parameter page from the parameter page copies present.

Release: 3/26/13

Figure 52: READ PARAMETER (ECh) with 00h Address Operation for ONFI



**128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations****Figure 53: READ PARAMETER (ECh) with 40h Address Operation for JEDEC**

Release: 3/26/13


Parameter Page Data Structure Tables
Table 15: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:7]: Reserved (0) Bit 6: 1 = supports ONFI version 3.0 Bit 5: 1 = supports ONFI version 2.3 Bit 4: 1 = supports ONFI version 2.2 Bit 3: 1 = supports ONFI verion 2.1 Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	7Eh, 00h
6–7	Features supported Bit[15:13]: Reserved (0) Bit 12: 1 = supports external V _{PP} Bit 11: 1 = supports Volume addressing Bit 10: 1 = supports NV-DDR2 interface Bit 9: 0 = Reserved Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports extended parameter page Bit 6: 1 = supports interleaved (multi-plane) read operations Bit 5: 1 = supports NV-DDR interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F128G08CBCAB MT29F128G08CBEAB MT29F256G08CECAB MT29F256G08CEEAB MT29F512G08CMCAB MT29F512G08CMEAB MT29F512G08CKCAB MT29F512G08CKEAB MT29F1T08CUCAB MT29F1T08CUEAB	F8h, 1Dh FAh, 1Dh

Release: 3/26/13

**Table 15: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
8–9	Optional commands supported Bit[15:12]: Reserved (0) Bit 11: 1 = supports ODT CONFIGURE Bit 10: 1 = supports VOLUME SELECT Bit 9: 1 = supports RESET LUN Bit 8: 1 = supports small data move Bit 7: 1 = supports CHANGE ROW ADDRESS Bit 6: 1 = supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports READ STATUS ENHANCED Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE	–	FFh, 0Fh
10	ONFI-JEDEC JTG primary advanced command support Bit[7:4]: Reserved (0) Bit 3: 1 = supports ERASE BLOCK MULTI-PLANE Bit 2: 1 = supports COPYBACK PROGRAM MULTI-PLANE Bit 1: 1 = supports PROGRAM PAGE MULTI-PLANE Bit 0: 1 = supports CHANGE READ COLUMN	–	0Fh
11	Reserved (0)	–	All 00h
12–13	Extended parameter page length	–	03h, 00h
14	Number of parameter pages	–	39h
15–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F128G08CBACBH6	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 42h, 43h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F128G08CBCEBH6	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 42h, 45h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F256G08CECABH6	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 45h, 43h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F256G08CEEABH6	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 45h, 45h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F512G08CKCABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Bh, 43h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F512G08CKEABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Bh, 45h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F512G08CMCABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Bh, 43h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F512G08CMEABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Dh, 45h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F1T08CUCABH8	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 43h, 55h, 43h, 41h, 42h, 48h, 38h, 20h, 20h, 20h, 20h
		MT29F1T08CUEABH8	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 43h, 55h, 45h, 41h, 42h, 48h, 38h, 20h, 20h, 20h, 20h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	C0h, 04h
86–91	Reserved (0)	–	All 00h
92–95	Number of pages per block	–	00h, 02h, 00h, 00h
96–99	Number of blocks per LUN	–	00h, 08h, 00h, 00h
100	Number of LUNs per chip enable	MT29F128G08CBCAB	01h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CMCAB	
		MT29F512G08CMEAB	02h
		MT29F512G08CKCAB	
		MT29F512G08CKEAB	
		MT29F1T08CUCAB	
		MT29F1T08CUEAB	
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	02h
103–104	Bad blocks maximum per LUN	–	32h, 00h
105–106	Block endurance	–	03h, 03h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h
110	Number of programs per page	–	01h
111	Reserved (0)	–	00h
112	Number of bits ECC correctability	–	FFh
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	01h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
114	Interleaved operation attributes Bit[7:6]: Reserved (0) Bit 5: Reserved Bit 4: 1 = supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = supports program cache Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	1Eh
115–127	Reserved (0)	–	All 00h
Electrical parameters block			
128	I/O pin capacitance per chip enable	MT29F128G08CBCAB	05h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	05h
		MT29F256G08CEEAB	
		MT29F512G08CMCAB	05h
		MT29F512G08CMEAB	
		MT29F512G08CKCAB	0Ah
		MT29F512G08CKEAB	
		MT29F1T08CUCAB	09h
		MT29F1T08CUEAB	
129–130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	3Fh, 00h
131–132	Reserved (0)	–	All 00h
133–134	^t PROG Maximum PROGRAM PAGE time (μs)	–	B8h, 0Bh
135–136	^t BERS Maximum BLOCK ERASE time (μs)	–	E0h, 2Eh
137–138	^t R Maximum PAGE READ time (μs)	–	73h, 00h
139–140	^t CCS Minimum change column setup time (ns)	–	2Ch, 01h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
141	NV-DDR timing mode support Bit[7:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	MT29F128G08CBEAB	1Fh
		MT29F256G08CEEAB	
		MT29F512G08CKEAB	
		MT29F512G08CMEAB	
		MT29F1T08CUEAB	
		MT29F128G08CBCAB	
		MT29F256G08CECAB	
		MT29F512G08CKCAB	
		MT29F512G08CMCAB	
		MT29F1T08CUCAB	
142	NV-DDR2 timing mode support Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	MT29F128G08CBEAB	0Fh
		MT29F256G08CEEAB	
		MT29F512G08CKEAB	
		MT29F512G08CMEAB	
		MT29F1T08CUEAB	
		MT29F128G08CBCAB	
		MT29F256G08CECAB	
		MT29F512G08CKCAB	
		MT29F512G08CMCAB	
		MT29F1T08CUCAB	
143	NV-DDR/NV-DDR2 features Bit[7:3]: Reserved (0) Bit 2: 1 = devices support CLK stopped for data input Bit 1: 1 = typical capacitance values present Bit 0: 0 = use $t_{CAD\ MIN}$ value	MT29F128G08CBCAB	02h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CMCAB	
		MT29F512G08CMEAB	
		MT29F512G08CKCAB	
		MT29F512G08CKEAB	
		MT29F1T08CUCAB	
		MT29F1T08CUEAB	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
144–145	CLK input pin capacitance, typical	MT29F128G08CBCAB	2Ah, 00h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	22h, 00h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	11h, 00h
		MT29F512G08CMEAB	
		MT29F1T08CUCAB	1Dh, 00h
		MT29F1T08CUEAB	
146–147	I/O pin capacitance, typical	MT29F128G08CBCAB	32h, 00h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	2Bh, 00h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	15h, 00h
		MT29F512G08CMEAB	
148–149	Input capacitance, typical	MT29F1T08CUCAB	26h, 00h
		MT29F1T08CUEAB	
		MT29F128G08CBCAB	2Eh, 00h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	26h, 00h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	13h, 00h
		MT29F512G08CMEAB	
		MT29F1T08CUCAB	21h, 00h
		MT29F1T08CUEAB	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
150	Input pin capacitance, maximum	MT29F128G08CBCAB	05h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	04h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	02h
		MT29F512G08CMEAB	
		MT29F1T08CUCAB	03h
		MT29F1T08CUEAB	
151	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports 18 Ohm drive strength Bit 1: 1 = Supports 25 Ohm drive strength Bit 0: 1 = Supports driver strength settings	–	07h
152–153	^t R maximum interleaved (multi-plane) page read time (μs)	–	73h, 00h
154–155	^t ADL program page register clear enhancement value (ns)	–	46h, 00h
156–157	Reserved (0)	–	All 00h
158	NV-DDR2 features Bit[7:5]: Reserved (0) Bit 4: 1 = supports differential signaling for DQS Bit 3: 1 = supports differential signaling for RE# Bit 2: 1 = supports ODT value of 30 ohms Bit 1: 1 = supports matrix termination ODT Bit 0: 1 = supports self-termination ODT	–	1Fh
159	NV-DDR2 warmup cycles Bit[7:4]: Data input warmup cycles support Bit[3:0]: Data output warmup cycles support	–	44h
160–163	Reserved (0)	–	All 00h
Vendor block			
164–165	Vendor-specific revision number	–	03h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific read cache function	–	00h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific READ UNIQUE ID	–	00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	–	00h
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable DQ output impedance settings	–	04h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	02h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	–	1Eh
179	OTP Feature Address	–	90h
180	Read Retry Options Bit[7:4]: Reserved (0) Bit[3:0] = Number of Read Retry options supported	–	08h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
181–184	Read Retry Options available. A value of '1' in a bit position shows that Read Retry option is available for use. A value of '0' in a bit position shows that Read Retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	—	FFh, 00h, 00h, 00h
185–252	Reserved (0)	—	All 00h
253	Parameter page revision	MT29F128G08CBEAB	01h
		MT29F256G08CEEAB	
		MT29F512G08CKEAB	
		MT29F512G08CMEAB	
		MT29F1T08CUEAB	
		MT29F128G08CBCAB	04h
		MT29F256G08CECAB	
		MT29F512G08CKCAB	
		MT29F512G08CMCAB	
		MT29F1T08CUCAB	
254–255	Integrity CRC	MT29F128G08CBCABH6	43h, 1Dh
		MT29F128G08CBEABH6	90h, 58h
		MT29F256G08CECABH6	A5h, B7h
		MT29F256G08CEEABH6	76h, F2h
		MT29F512G08CKCABH7	EEh, 50h
		MT29F512G08CKEABH7	3Dh, 15h
		MT29F512G08CMCABH7	73h, 70h
		MT29F512G08CMEABH7	A0h, 35h
		MT29F1T08CUCABH8	B6h, 86h
		MT29F1T08CUEABH8	BAh, 72h
Redundant parameter pages			
256–511	Value of bytes 0–255	—	See bytes 0–255
512–767	Value of bytes 0–255	—	See bytes 0–255
...	...	—	...
14,080–14,335	Value of bytes 0–255	—	See bytes 0–255

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 15: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
14,336– 14,591	Value of bytes 0–255	–	See bytes 0–255
Extended parameter pages			
14,592– 14,593	Extended parameter page Integrity CRC	–	4Ah, 87h
14,594– 14,597	Extended parameter page signature Byte 0: 45h, "E" Byte 1: 50h, "P" Byte 2: 50h, "P" Byte 3: 53h, "S"	–	45h, 50h, 50h, 53h
14,598– 14,607	Reserved (0)	–	All 00h
14,608	Section 0 type	–	02h
14,609	Section 0 length	–	01h
14,610–14, 623	Reserved (0)	–	All 00h
14,624	Number of bits ECC correctability	–	28h
14,625	ECC codeword size	–	0Ah
14,626– 14,627	Bad blocks maximum per LUN	–	32h, 00h
14,628– 14,629	Block endurance	–	03h, 03h
14,630– 14,639	Reserved (0)	–	All 00h
Redundant extended parameter pages			
14,640– 14,687	Value of bytes 14,592–14,639	–	See bytes 14,592–14,639
14,688– 14,735	Value of bytes 14,592–14,639	–	See bytes 14,592–14,639
...	...	–	...
17,232– 17,279	Value of bytes 14,592–14,639	–	See bytes 14,592–14,639
17,280– 17,327	Value of bytes 14,592–14,639	–	See bytes 14,592–14,639
17,328 to end of page	Reserved (FFh)	–	All FFh

Table 16: JEDEC Parameter Page Definition

Byte	Description	Device	Values
Revision Information and Features Block			

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 16: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
0–3	Parameter page signature Byte 0: 4Ah, "J" Byte 1: 45h, "E" Byte 2: 53h, "S" Byte 3: 44h, "D"	–	4Ah, 45h, 53h, 44h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports JEDEC version 1.0 Bit 1: 1 = supports vendor specific parameter page Bit 0: Reserved (0)	–	06h, 00h
6–7	Features supported Bit[15:9]: Reserved (0) Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports external V _{PP} Bit 6: 1 = supports Toggle Mode DDR Bit 5: 1 = supports Synchronous DDR Bit 4: 1 = supports multi-plane read operations Bit 3: 1 = supports multi-plane program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F128G08CBCAB	B8h, 01h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CMCAB	
		MT29F512G08CMEAB	
		MT29F512G08CKCAB	BAh, 01h
		MT29F512G08CKEAB	
		MT29F1T08CUCAB	
		MT29F1T08CUEAB	
8–10	Features supported Bit[23:11]: Reserved (0) Bit 10: 1 = supports Synchronous Reset Bit 9: 1 = supports Reset LUN (Primary) Bit 8: 1 = supports Small Data Move Bit 7: 1 = supports Multi-plane Copyback Program (Primary) Bit 6: 1 = supports Random Data Out (Primary) Bit 5: 1 = supports Read Unique ID Bit 4: 1 = supports Copyback Bit 3: 1 = supports Read Status Enhanced (Primary) Bit 2: 1 = supports Get Features and Set Features Bit 1: 1 = supports Read Cache commands Bit 0: 1 = supports Page Cache Program command	–	FFh, 07h, 00h

Release: 3/26/13

**Table 16: JEDEC Parameter Page Defintion (Continued)**

Byte	Description	Device	Values
11–12	Secondary commands supported Bit[15:8]: Reserved (0) Bit 7: 1 = supports secondary Read Status Enhanced Bit 6: 1 = supports secondary Multi-plane Block Erase Bit 5: 1 = supports secondary Multi-plane Copyback Program Bit 4: 1 = supports secondary Multi-plane Program Bit 3: 1 = supports secondary Random Data Out Bit 2: 1 = supports secondary Multi-plane Copyback Read Bit 1: 1 = supports secondary Multi-plane Read Cache Random Bit 0: 1 = supports secondary Multi-plane Read	–	58h, 00h
13	Number of Parameter Pages	–	22h
14–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 16: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F128G08CBAABH6	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 42h, 41h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F128G08CBCABH6	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 42h, 43h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F256G08CEAABH6	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 45h, 41h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F256G08CECABH6	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 45h, 43h, 41h, 42h, 48h, 36h, 20h, 20h
		MT29F512G08CKAABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Bh, 41h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F512G08CKCABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Bh, 43h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F512G08CMAABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Dh, 41h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F512G08CMCABH7	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Dh, 43h, 41h, 42h, 48h, 37h, 20h, 20h
		MT29F1T08CUCABH8	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 43h, 55h, 43h, 41h, 42h, 48h, 38h, 20h, 20h, 20h, 20h
		MT29F1T08CUEABH8	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 43h, 55h, 45h, 41h, 42h, 48h, 38h, 20h, 20h, 20h, 20h
64–69	JEDEC manufacturer ID	–	2Ch, 00h, 00h, 00h
70–71	Reserved (0)	–	All 00h
72–79	Reserved (0)	–	All 00h
Memory organization block			

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 16: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	C0h, 04h
86–89	Number of data bytes per partial page	–	00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page	–	4Ch, 00h
92–95	Number of pages per block	–	00h, 02h, 00h, 00h
96–99	Number of blocks per LUN	–	00h, 08h, 00h, 00h
100	Number of LUNs per chip enable	MT29F128G08CBCAB	01h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CMCAB	
		MT29F512G08CMEAB	02h
		MT29F512G08CKCAB	
		MT29F512G08CKEAB	
		MT29F1T08CUCAB	
		MT29F1T08CUEAB	
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	02h
103	Number of programs per page	–	01h
104	Multi-plane operation addressing Bit[7:4]: Reserved (0) Bit[3:0]: Number of plane address bits	–	01h
105	Multi-plane operation attributes Bit[7:3]: Reserved (0) Bit 2: 1 = Address restrictions for cache operations Bit 1: 1 = Read cache operations supported Bit 0: 1 = Program cache operations supported	–	07h
106–143	Reserved (0)	–	All 00h
Electrical parameters block			
144–145	Asynchronous SDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	3Fh, 00h
146–147	Reserved (0)	–	00h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 16: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
148–149	Synchronous DDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	MT29F128G08CBEAB	1Fh, 00h
		MT29F256G08CEEAB	
		MT29F512G08CMEAB	
		MT29F512G08CKEAB	
		MT29F1T08CUEAB	
		MT29F128G08CBCAB	
		MT29F256G08CECAB	
		MT29F512G08CMCAB	
		MT29F512G08CKCAB	
		MT29F1T08CUCAB	
150	Asynchronous SDR features Bit[7:0]: Reserved (0)	–	00h
151	Reserved (0)	–	00h
152	Synchronous DDR features Bit[7:2]: Reserved (0) Bit 1: 1 = devices leave CLK running for data input Bit 0: 0 = use ^t CAD MIN value	–	00h
153–154	^t PROG Maximum PROGRAM PAGE time (μs)	–	B8h, 0Bh
155–156	^t BERS Maximum BLOCK ERASE time (μs)	–	E0h, 2Eh
157–158	^t R Maximum PAGE READ time (μs)	–	73h, 00h
159–160	^t R Maximum Multi-PLANE PAGE READ time (μs)	–	73h, 00h
161–162	^t CCS Minimum change column setup time (ns)	–	2Ch, 01h
163–164	I/O pin capacitance, typical	MT29F128G08CBCAB	32h, 00h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	2Bh, 00h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	15h, 00h
		MT29F512G08CMEAB	
		MT29F1T08CUCAB	26h, 00h
		MT29F1T08CUEAB	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 16: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
165–166	Input capacitance, typical	MT29F128G08CBCAB	2Eh, 00h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	26h, 00h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	13h, 00h
		MT29F512G08CMEAB	
		MT29F1T08CUCAB	21h, 00h
		MT29F1T08CUEAB	
167–168	CLK input pin capacitance, typical	MT29F128G08CBCAB	2Ah, 00h
		MT29F128G08CBEAB	
		MT29F256G08CECAB	
		MT29F256G08CEEAB	
		MT29F512G08CKCAB	22h, 00h
		MT29F512G08CKEAB	
		MT29F512G08CMCAB	11h, 00h
		MT29F512G08CMEAB	
		MT29F1T08CUCAB	1Dh, 00h
		MT29F1T08CUEAB	
169	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports 18 Ohm drive strength Bit 1: 1 = Supports 25 Ohm drive strength Bit 0: 1 = Supports driver strength settings	–	07h
170–207	Reserved (0)	–	00h
ECC and endurance block			
208	Guaranteed valid blocks at beginning of target	–	01h
209–210	Block endurance for guaranteed valid blocks	–	00h, 00h
211	Number of bits ECC correctability	–	28h
212	ECC codeword size	–	0Ah
213–214	Bad blocks maximum per LUN	–	32h, 00h
215–216	Block endurance	–	03h, 03h
217–218	Reserved (0)	–	All 00h
219–271	Reserved (0)	–	All 00h
Reserved			
272–419	Reserved (0)	–	All 00h
Vendor specific block			
420–421	Vendor-specific revision number	–	05h, 00h

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Identification Operations

Table 16: JEDEC Parameter Page Definition (Continued)

Byte	Description	Device	Values
422	Read Retry Options Bit[7:4]: Reserved (0) Bit[3:0] = Number of Read Retry options supported	—	08h
423–426	Read Retry Options available. A value of '1' in a bit position shows that Read Retry option is available for use. A value of '0' in a bit position shows that Read Retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	—	FFh, 00h, 00h, 00h
427–509	Reserved (0)	—	All 00h
CRC for Parameter Page			
510–511	Integrity CRC	MT29F128G08CBCABH6	69h, 54h
		MT29F128G08CBEABH6	DDh, 69h
		MT29F256G08CECABH6	5Eh, 34h
		MT29F256G08CEEABH6	EAh, 09h
		MT29F512G08CKCABH6	76h, 87h
		MT29F512G08CKEABH7	C2h, BAh
		MT29F512G08CMCABH7	38h, 49h
		MT29F512G08CMEABH7	8Ch, 1Fh
		MT29F1T08CUCABH8	CDh, B4h
		MT29F1T08CUEABH8	71h, 8Eh
Redundant JEDEC Parameter Pages			
512–1023	See byte values 0–511	—	See bytes 0–511
1024–1535	See byte values 0–511	—	See bytes 0–511
...	...	—	...
16,384–16,895	See byte values 0–511	—	See bytes 0–511
16,896–17,407	See byte values 0–511	—	See bytes 0–511
17,408 to end of page	Reserved (FFh)	—	All FFh

Note: 1. h = hexadecimal.

Release: 3/26/13



READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

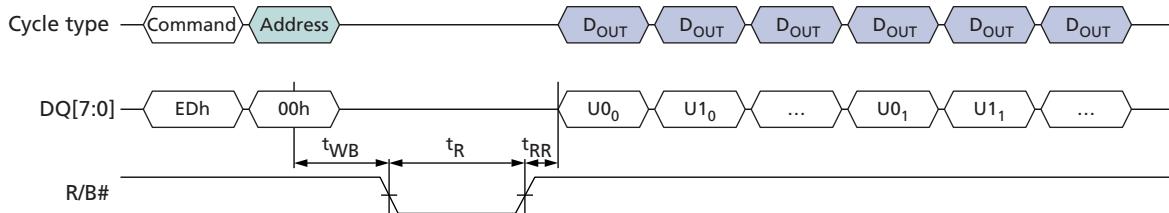
Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When the EDh command is followed by a 00h address cycle, the target goes busy for t^R . If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After t^R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte for each rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

Figure 54: READ UNIQUE ID (EDh) Operation



Release: 3/26/13



Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in . The SET FEATURES (EFh) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specified, the values of the feature addresses do not change when RESET (FAh, FFh, FCh) is issued by the host.

Table 17: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h	NV-DDR2 configuration
03h–0Fh	Reserved
10h	Programmable output drive strength
11h–2Fh	Reserved
30h	V _{PP} configuration
31h–57h	Reserved
58h	Volume configuration
59h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–88h	Reserved
89h	Read Retry
8Ah–8Fh	Reserved
90h	Array operation mode
91h–FFh	Reserved

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address as specified in Table 17. The host waits for 'ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the NV-DDR or NV-DDR2 interface is active, one subfeature parameter is latched per rising edge of DQS_t. The data on the falling edge of DQS_t should be identical to the

Release: 3/26/13



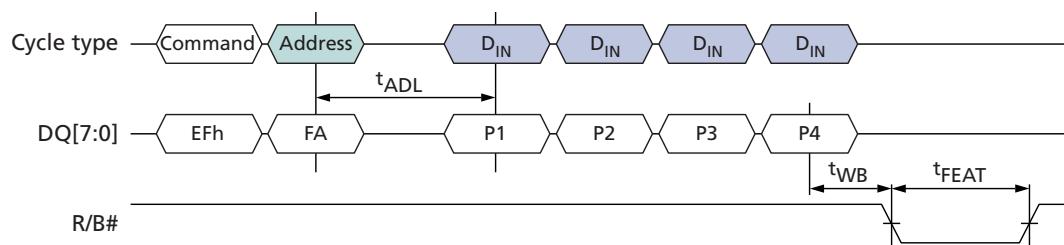
128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

subfeature parameter input on the previous rising edge of DQS_t. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for t_{FEAT} . The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (Timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for t_{ITC} . See Activating Interfaces (page 63) for details.

Figure 55: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

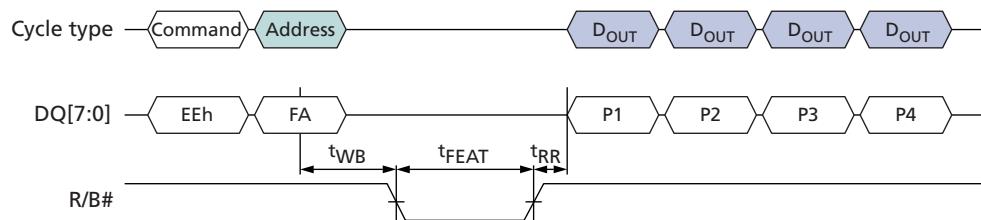
The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for t_{FEAT} . If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After t_{FEAT} completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE_# toggle. When the NV-DDR or NV-DDR2 interface is active, one subfeature parameter is output per DQS_t toggle on rising or falling edge of DQS_t.

Figure 56: GET FEATURES (EEh) Operation



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 18: Feature Address 01h: Timing mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
	Mode 6					0	1	1	0	x6h	
	Mode 7					0	1	1	1	x7h	
	Reserved					1	x	x	x	-	
Data interface	Asynchronous (de-default)			0	0					0xh	1
	NV-DDR			0	1					1xh	
	NV-DDR2			1	0					2xh	
	Reserved			1	1					3xh	
Program clear	Program command clears all cache registers on a target (default)		0							0b	
	Program command clears only addressed LUN cache register on a target		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

- Notes:
1. Asynchronous timing mode 0 is the default, power-on value.
 2. If the NV-DDR or NV-DDR2 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued. Transition from the NV-DDR interface to the NV-DDR2 interface or vice versa is not permitted.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 19: Feature Address 02h: NV-DDR2 configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Voltage Reference (VEN)	External V _{REFQ} is disabled and internal voltage is used as reference for DQ signals(default)								0	0b	1, 2
	External V _{REFQ} is enabled and used as reference for DQ signals								1	1b	
Complementary DQS (CMPD)	DQS_c signal disabled (default)							0		0b	
	DQS_c signal enabled							1		1b	
Complementary RE# (CMPPR)	RE_c signal disabled (default)						0			0b	
	RE_c signal enabled						1			1b	
Reserved	-					0				0b	
DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c ODT enable	ODT disabled (default)	0	0	0	0					0h	
	ODT enabled with R _{TT} of 150 Ohms	0	0	0	1					1h	
	ODT enabled with R _{TT} of 100 Ohms	0	0	1	0					2h	
	ODT enabled with R _{TT} of 75 Ohms	0	0	1	1					3h	
	ODT enabled with R _{TT} of 50 Ohms	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
P2											

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 19: Feature Address 02h: NV-DDR2 configuration (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Warmup RE_t/ RE_c and DQS cycles for data output	0 cycles (default)					0	0	0	0	0h	
	1 warmup cycle					0	0	0	1	1h	
	2 warmup cycles					0	0	1	0	2h	
	Reserved					0	0	1	1	3h	
	4 warmup cycles					0	1	0	0	4h	
	Reserved					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
Warmup DQS cycles for data input	0 cycles (default)	0	0	0	0					0h	
	1 warmup cycle	0	0	0	1					1h	
	2 warmup cycles	0	0	1	0					2h	
	Reserved	0	0	1	1					3h	
	4 warmup cycles	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

- Notes:
1. R_{TT} settings may be specified separately for DQ[7:0], DQS, RE_t, and RE_c signals. The DQ[7:0], DQS signals may be specified separate for data input versus data output operation. See
 2. If the NV-DDR2 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued.
 3. Number of warmup cycles for DQS during data input and RE_t/RE_c and DQS_t/DQS_c for data output. The number of initial "dummy" RE_t/RE_c cycles at the start of data output operations. There are corresponding "dummy" DQS_t/DQS_c cycles to the "dummy" RE_t/RE_c cycles that the host shall ignore during data output.

Table 20: Feature Address 30h: V_{PP}

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 20: Feature Address 30h: V_{PP} (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
External V _{PP} configuration	Disabled (default)								0	00h	
	Enabled								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This setting controls whether external V_{PP} is enabled. This setting is retained across RESET (FAh, FCh, FFh) commands.

Table 21: Feature Address 58h: Volume configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Volume Address	Field used to assign a value for a given Volume Address					X	X	X	X		1
Reserved	-	0	0	0	0					0h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. After the Volume Address is appointed, the ENo pin for that Volume is set to one, the ENi pin for that Volume is ignored until the next power cycle, and the Volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the associated Volume. The host shall only set this feature once per power cycle for each Volume. The address specified is then used in VOLUME SELECT (E1h) command for accessing this NAND Target. This setting is retained across RESET (FAh, FCh, FFh) commands.

Table 22: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 22: Feature Addresses 10h and 80h: Programmable Output Drive Strength (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Output drive strength	18 Ohms							0	0	00h	1
	25 Ohms							0	1	01h	
	35 Ohms (default)							1	0	02h	
	50 Ohms							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. See Output Drive Impedance for details.

Table 23: Feature Address 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 24: Feature Addresses 89h: Read Retry

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 24: Feature Addresses 89h: Read Retry (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Read Retry	Disable (default)						0	0	0	00h	
	Option 1						0	0	1	01h	
	Option 2						0	1	0	02h	
	Option 3						0	1	1	03h	
	Option 4						1	0	0	04h	2
	Option 5						1	0	1	05h	
	Option 6						1	1	0	06h	
	Option 7						1	1	1	07h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:

- See Read Retry Operation for details.
- tR will be longer with selected option. See Electrical Specifications - Array Characteristics section for details. Cache Read functions are not supported with these selected options.

Table 25: Feature Address 90h: Array Operation Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:

- See One-Time Programmable (OTP) Operations for details.
- A RESET (FFh) command will cause the bits of the array operation mode to change to their default values.

Release: 3/26/13



VOLUME SELECT (E1h)

The Volume Select function is used to select a particular Volume based on the address specified. VOLUME SELECT (E1h) command is required to be used when CE# pin reduction is used or when matrix termination is used.

This command is accepted by all Targets that share a particular CE# pin. The command may be executed with any LUN on the Volume in any state. The VOLUME SELECT (E1h) command may only be issued as the first command after CE# is pulled LOW; CE# shall have remained HIGH for t_{CEH} in order for the VOLUME SELECT (E1h) command to be properly received by all NAND Targets connected to the Host Target.

If Volumes that share a Host Target are configured to use different data interfaces, then the host shall issue the VOLUME SELECT (E1h) command using the Asynchronous data interface.

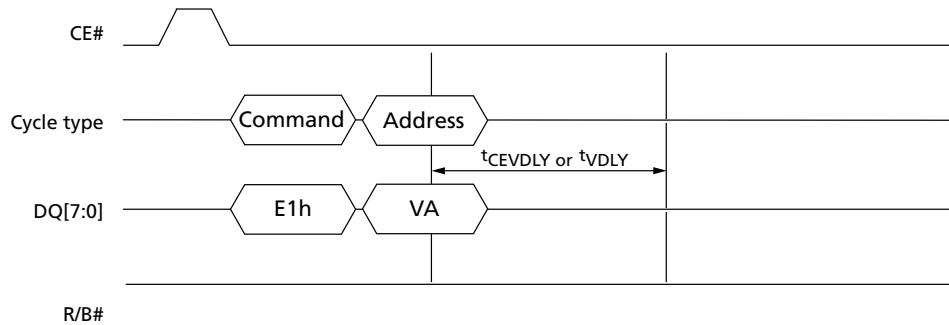
When the VOLUME SELECT (E1h) command is issued, all NAND Targets that have a Volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE# pulled HIGH). If one of the LUNs in an unselected Volume is the assigned terminator for the Volume addressed, then that LUN will enter the sniff state.

If the Volume address specified does not correspond to any appointed Volume address, then all NAND Targets shall be deselected until a subsequent VOLUME SELECT (E1h) command is issued. If the VOLUME SELECT (E1h) command is not the first command issued after CE# is pulled LOW, then the NAND Targets revert to their previous selected, deselected, or sniff states.

The host shall not issue new commands to any LUN on any Volume until after t_{VDLY} . This delay is required to ensure the appropriate Volume is selected for the next command issued. Also the host shall not bring CE# HIGH on any Volume until after t_{CEVDLY} . This delay is required to ensure the appropriate Volume is selected based on the previously issued VOLUME SELECT (E1h) command.

The Volume address is retained across all RESET (FAh, FCh, FFh) commands.

Figure 57: VOLUME SELECT (E1h) Operation





128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 26: Volume Address

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Volume Address											
VA										Volume Address	-
Reserved		0	0	0	0					-	

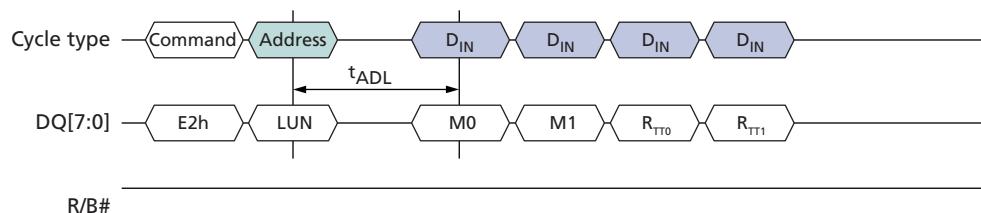
Release: 3/26/13



ODT CONFIGURE (E2h)

The ODT CONFIGURE (E2h) command is used to configure on-die termination. Specifically, ODT CONFIGURE (E2h) specifies whether a particular LUN is a terminator for a Volume(s) and the R_{TT} settings. If the LUN is specified as a terminator for one or more Volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the Volume(s) it is acting as a terminator for depending on the settings of Table 27. The on-die termination settings are retained across all RESET (FAh, FCh, FFh) commands.

Figure 58: ODT CONFIGURE (E2h) Operation



The LUN address correspond to the same structure as the last address cycle for the NAND device which determines which LUN will act as the terminator.

The ODT Configuration Matrix structure is defined in Table 27. For the Volume Address fields M0 and M1, if a bit is set to one then the LUN shall act as the terminator for the corresponding Volume(s) (Vn) where n corresponds to the Volume address.

The ODT CONFIGURE (E2h) command is only available while in the NV-DDR2 interface operation mode.

Table 27: ODT Configuration Matrix

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
M0											
Volume Address	Volumes that will be terminated by selected LUN	V7	V6	V5	V4	V3	V2	V1	V0	-	
M1											
Volume Address	Volumes that will be terminated by selected LUN	V15	V14	V13	V12	V11	V10	V9	V8	-	
R_{TTO}											



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 27: ODT Configuration Matrix (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
DQ[7:0]/DQS_t/ DQS_c R _{TT} and ODT enable for data input	ODT disabled (default)					0	0	0	0	0h	
	ODT enabled with R _{TT} of 150 Ohms					0	0	0	1	1h	
	ODT enabled with R _{TT} of 100 Ohms					0	0	1	0	2h	
	ODT enabled with R _{TT} of 75 Ohms					0	0	1	1	3h	
	ODT enabled with R _{TT} of 50 Ohms					0	1	0	0	4h	
Reserved						0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
DQ[7:0]/DQS_t/ DQS_c R _{TT} and ODT enable for data output	ODT disabled (default)	0	0	0	0					0h	
	ODT enabled with R _{TT} of 150 Ohms	0	0	0	1					1h	
	ODT enabled with R _{TT} of 100 Ohms	0	0	1	0					2h	
	ODT enabled with R _{TT} of 75 Ohms	0	0	1	1					3h	
	ODT enabled with R _{TT} of 50 Ohms	0	1	0	0					4h	
Reserved		0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
R_{TT1}											

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Configuration Operations

Table 27: ODT Configuration Matrix (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
RE_t and RE_c R _{TT} ODT enable	ODT disabled (default)					0	0	0	0	0h	
	ODT enabled with R _{TT} of 150 Ohms					0	0	0	1	1h	
	ODT enabled with R _{TT} of 100 Ohms					0	0	1	0	2h	
	ODT enabled with R _{TT} of 75 Ohms					0	0	1	1	3h	
	ODT enabled with R _{TT} of 50 Ohms					0	1	0	0	4h	
Reserved	-					0	1	0	1	5h	
	-					0	1	1	0	6h	
	-					0	1	1	1	7h	
	-					1	X	X	X	8h-Fh	
Reserved	-	0	0	0	0					0h	

Release: 3/26/13



Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the synchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles while ALE and CLE are HIGH.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (tR) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see READ MODE (00h) (page 125)).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations (page 152)).

Table 28: Status Register Definition

SR Bit	Definition	Independent per Plane ¹	Description
7	WP#	–	Write Protect: 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O: 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET (FFh), SYNCHRONOUS RESET (FCh), READ STATUS (70h), and READ STATUS ENHANCED (78h). This bit applies only to the selected die (LUN).
5	ARDY	–	Ready/Busy Array: 0 = Busy 1 = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).
4	–	–	Reserved (0)
3	–	–	Reserved (0)

**Table 28: Status Register Definition (Continued)**

SR Bit	Definition	Independent per Plane¹	Description
2	–	–	Reserved (0)
1	FAILC	Yes	Pass/Fail (N-1): 0 = Pass 1 = Fail This bit is set if the previous operation on the selected die (LUN) failed. This bit is valid only when RDY (SR bit 6) is 1. It applies to PROGRAM-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 85h-10h). This bit is not valid following an ERASE-series or READ-series operation.
0	FAIL	Yes	Pass/Fail (N): 0 = Pass 1 = Fail This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1. It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

Note: 1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command is issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.

READ STATUS (70h)

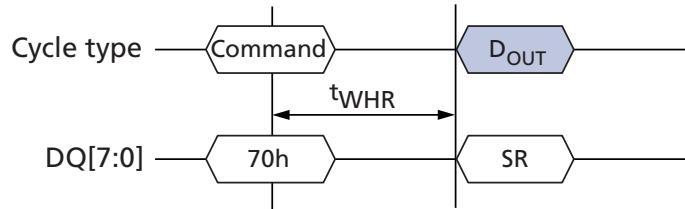
The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Release: 3/26/13

**Figure 59: READ STATUS (70h) Operation**

READ STATUS ENHANCED (78h)

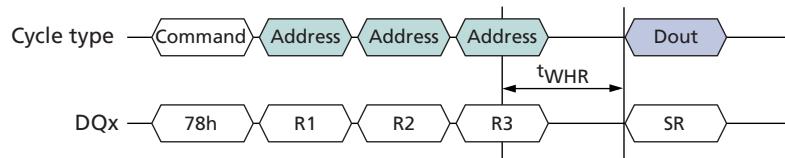
The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 60: READ STATUS ENHANCED (78h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

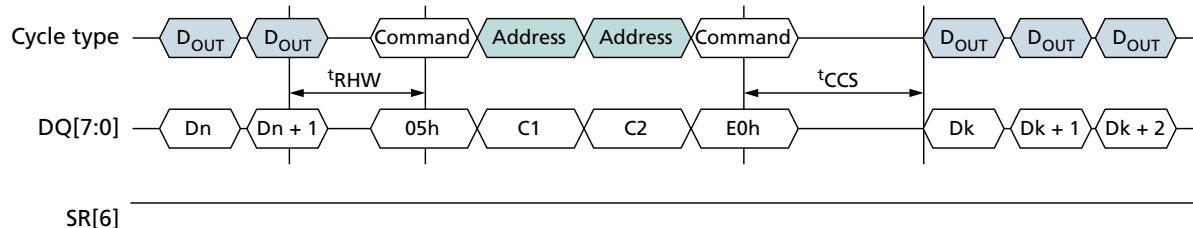
CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least t_{CCS} before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 61: CHANGE READ COLUMN (05h-E0h) Operation





CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. After the E0h command cycle is issued, the host must wait at least t_{CCS} before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

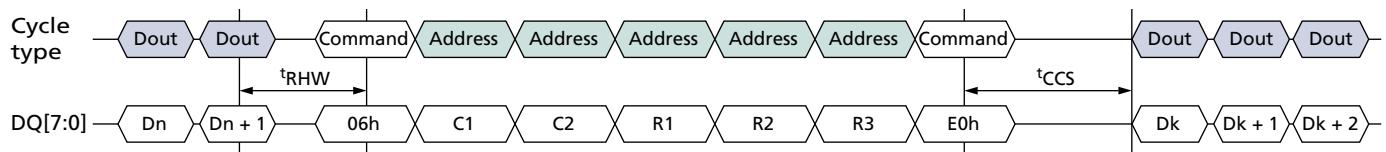
Following a multi-plane read page operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) read operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED (06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

Figure 62: CHANGE READ COLUMN ENHANCED (06h-E0h) Operation



Release: 3/26/13

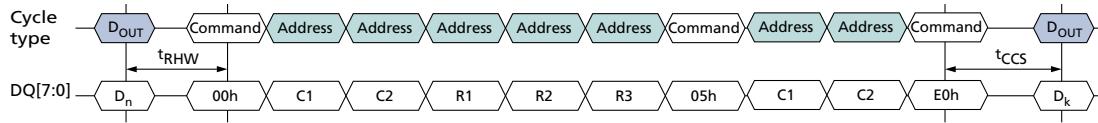


128Gb to 1Tb Asynchronous/Synchronous NAND Column Address Operations

CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation

This operation behaves the same as the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

Figure 63: CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation



Release: 3/26/13



CHANGE WRITE COLUMN (85h)

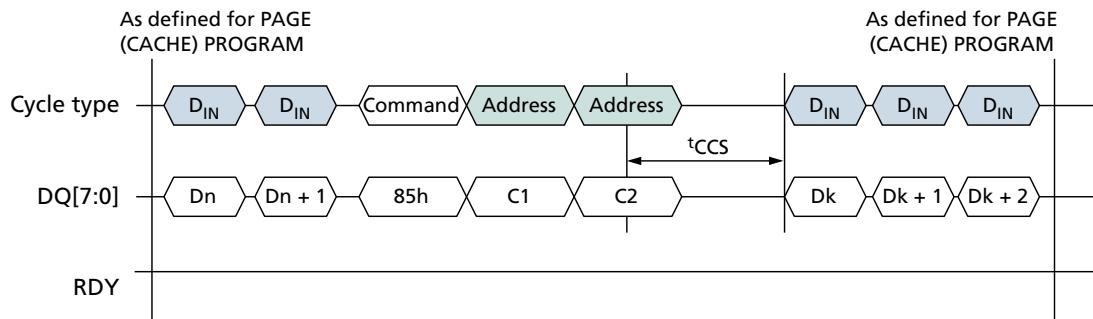
The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least t_{CCS} before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 64: CHANGE WRITE COLUMN (85h) Operation





CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least t_{CCS} before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

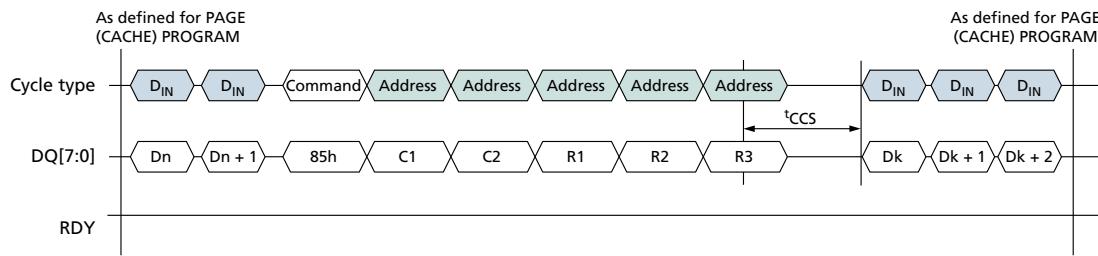
The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting t_{DBSY} , and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.



128Gb to 1Tb Asynchronous/Synchronous NAND Column Address Operations

Figure 65: CHANGE ROW ADDRESS (85h) Operation



Release: 3/26/13



Read Operations

Read operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command.

R/B# goes LOW during t^R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After t^R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h)—copies the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for t^{RCBSY} while the next page begins copying data from the array to the data register. After t^{RCBSY} , R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for t^{RCBSY} while the data register is copied into the cache register. After t^{RCBSY} , R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, t^{RCBSY} , when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status opera-



128Gb to 1Tb Asynchronous/Synchronous NAND Read Operations

tions (70h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh).

Multi-Plane Read Operations

Multi-plane read page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Multi-Plane Operations for details.

Multi-Plane Read Cache Operations

Multi-plane read cache operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

To begin a multi-plane read page cache sequence, begin by issuing a MULTI-PLANE READ PAGE operation using the READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) commands. R/B# goes LOW during t_R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After t_R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE MULTI-PLANE (00h-32h) commands, if desired, followed by the READ PAGE CACHE RANDOM (00h-31h) command—copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for t_{RCBSY} while the next pages begin copying data from the array to the data registers. After t_{RCBSY} , R/B# goes HIGH and the LUN's status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional MULTI-PLANE READ CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for t_{RCBSY} while the data registers are copied into the cache registers. After t_{RCBSY} , R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the



128Gb to 1Tb Asynchronous/Synchronous NAND Read Operations

CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, t_{RCBSY}, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), multi-plane read cache-series (31h, 00h-32h, 00h-31h), CHANGE READ COLUMN (05h-E0h, 06h-E0h), and RESET (FFh, FCh).

See Multi-Plane Operations for additional multi-plane addressing requirements.

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 3Fh, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

Release: 3/26/13



READ PAGE (00h-30h)

The READ PAGE (00h-30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, the write five address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for t_R as data is transferred.

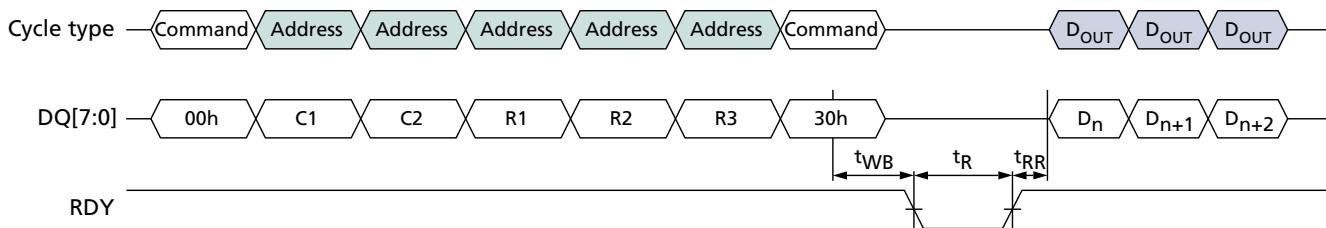
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the CHANGE READ COLUMN (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the last even plane addressed. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to enable data output in the other cache registers. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 66: READ PAGE (00h-30h) Operation





READ PAGE CACHE SEQUENTIAL (31h)

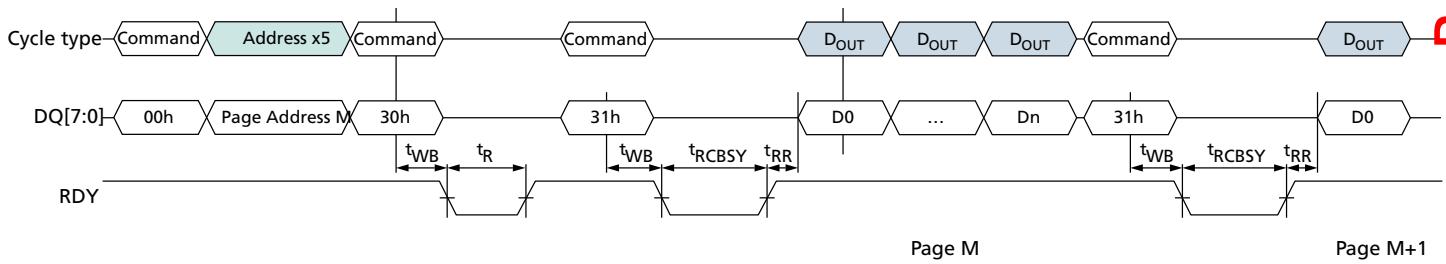
The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY. After tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), the next sequential pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 67: READ PAGE CACHE SEQUENTIAL (31h) Operation



Release: 3/26/13

**READ PAGE CACHE RANDOM (00h-31h)**

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^tRCBSY. After ^tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

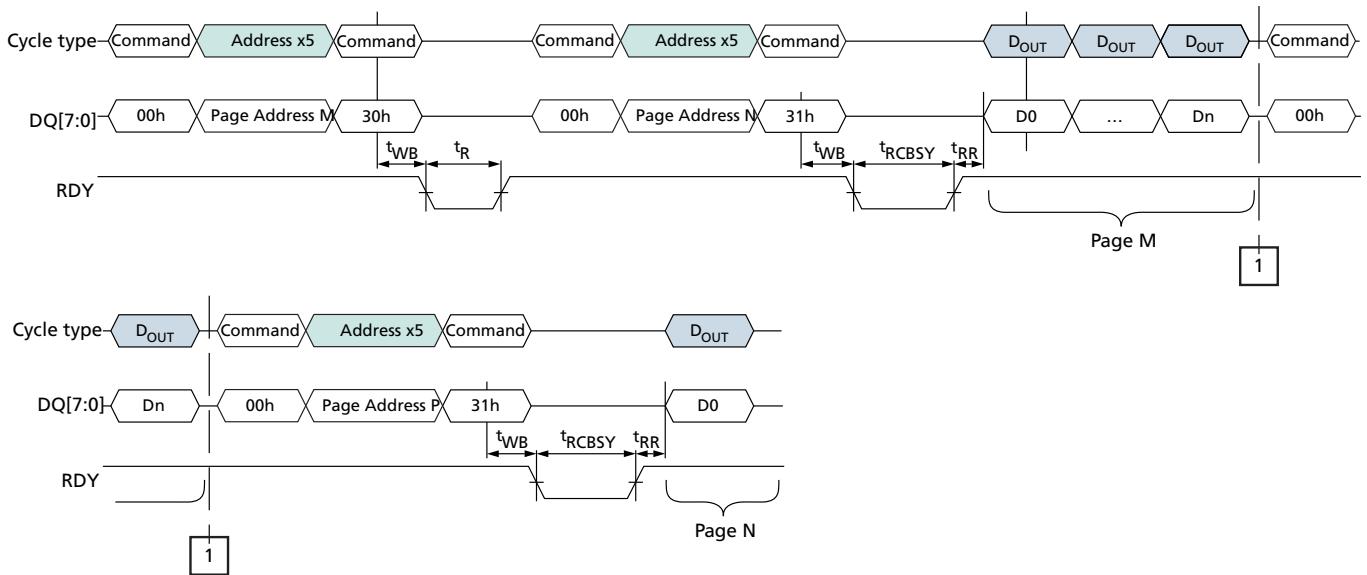
If a MULTI-PLANE CACHE RANDOM (00h-32h, 00h-31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), then the addressed pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Read Operations

Figure 68: READ PAGE CACHE RANDOM (00h-31h) Operation



Release: 3/26/13



READ PAGE CACHE LAST (3Fh)

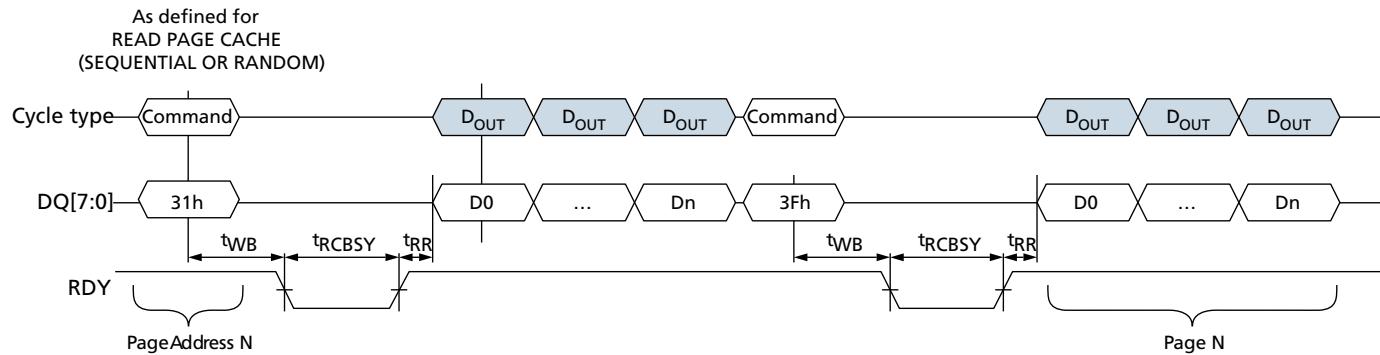
The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for t_{RCBSY} . After t_{RCBSY} , R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If the READ PAGE CACHE LAST (3Fh) command is issued after a MULTI-PLANE READ PAGE CACHE operation (31h; 00h-32h, 00h-30h), the die (LUN) goes busy until the pages are copied from the data registers to the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 69: READ PAGE CACHE LAST (3Fh) Operation



Release: 3/26/13



READ PAGE MULTI-PLANE (00h-32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for t_{DBSY} . After t_{DBSY} , R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane. During t_{DBSY} , the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following t_{DBSY} , to continue the MULTI-PLANE READ operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), READ PAGE (00h-30h), and READ PAGE CACHE RANDOM (00h-31h).

Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the last even plane addressed. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE SEQUENTIAL (31h) is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from each plane to each cache register and then data is transferred from the NAND Flash array for all previously addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE RANDOM (00h-31h) command is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from the data register to the cache register and then data is transferred from the NAND Flash array for all of the addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ

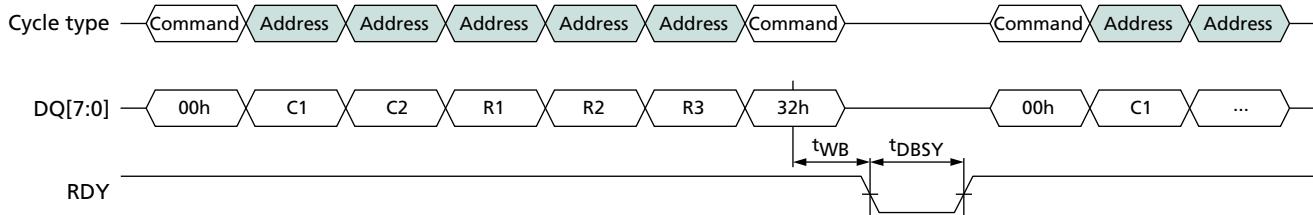


128Gb to 1Tb Asynchronous/Synchronous NAND Read Operations

COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 70: READ PAGE MULTI-PLANE (00h-32h) Operation



Release: 3/26/13



Read Retry Operations

Read retry operations are used as an additional method to recover from bit errors beyond the ECC correction threshold.

Read Retry Operations

The read retry operations are a coordination of read operations and SET FEATURES (EFh) with feature address 89h, selecting different internal read settings in attempt to recover data that is beyond the ECC correction threshold. Using the read retry operations with any array read operation commands is allowed. See Configuration Operations and Feature Address 89h: Read Retry for details.

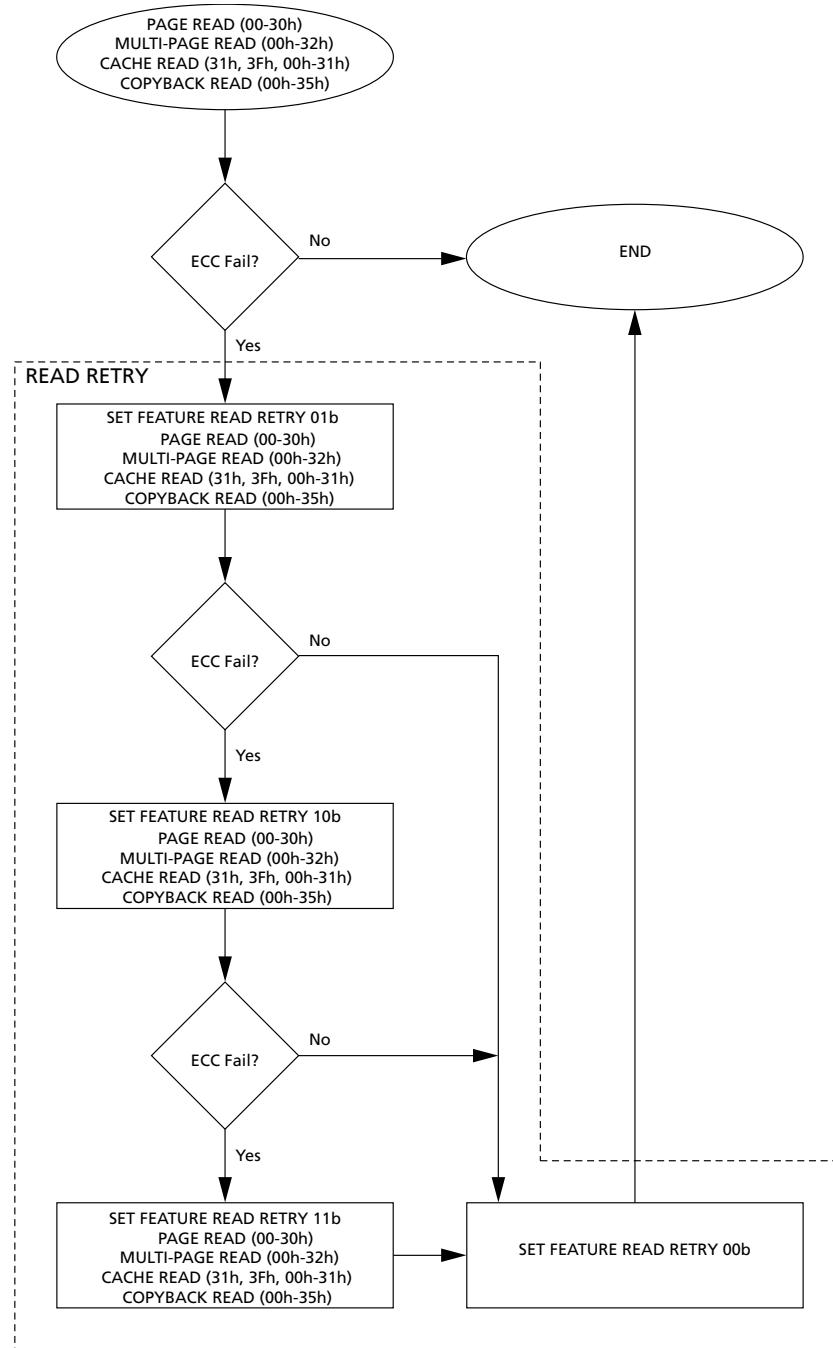
If reading a page has failed for bit errors beyond the ECC correction threshold, the host issues the SET FEATURE (EFh) command to feature address 89h with P1 subfeature set to a read retry option, as defined in that feature address. A new NAND array READ operation can now be performed. If the read still fails for bit errors beyond the ECC correction threshold, issue the SET FEATURES (EFh) command with the read retry (89h) feature address to select the next consecutive read retry option and repeat read retry operations until the data is correctable or the last option has been attempted. If the re-read is now correctable within the ECC threshold limits, the next read retry option should be set to its default value before the next NAND array READ operation. See Figure 71 (page 134) for flow diagram of read retry operations.

When the user writes to the read retry feature address, all subsequent reads use the internal NAND settings associated with that value until either the read retry feature address is rewritten or the device is powered down. This feature should not be used with the following commands: READ PARAMETER PAGE (ECh), READ UNIQUE ID (EDh), READ OTP PAGE (00h-30h).

Release: 3/26/13



Figure 71: Read Retry Flow Chart



Note: 1. There may be more read retry options than are shown in the figure for this NAND device. See Configuration Operations and Read Retry (89h) feature address for details.



Program Operations

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, 3, ...). Programming pages out of order within a block is prohibited.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0). While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE-series (80h-15h) operations, during the die (LUN) busy times, ^tCBSY and ^tLPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and reset (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and reset (FFh, FCh).

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See Multi-Plane Operations for details.

Multi-Plane Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See Multi-Plane Operations for details.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN)



128Gb to 1Tb Asynchronous/Synchronous NAND Program Operations

when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

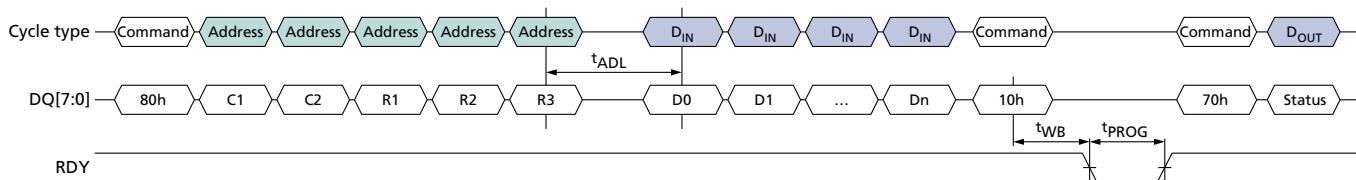
To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for tPROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 72: PROGRAM PAGE (80h-10h) Operation





PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^tCBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of ^tCBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^tCBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.



128Gb to 1Tb Asynchronous/Synchronous NAND Program Operations

Figure 73: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

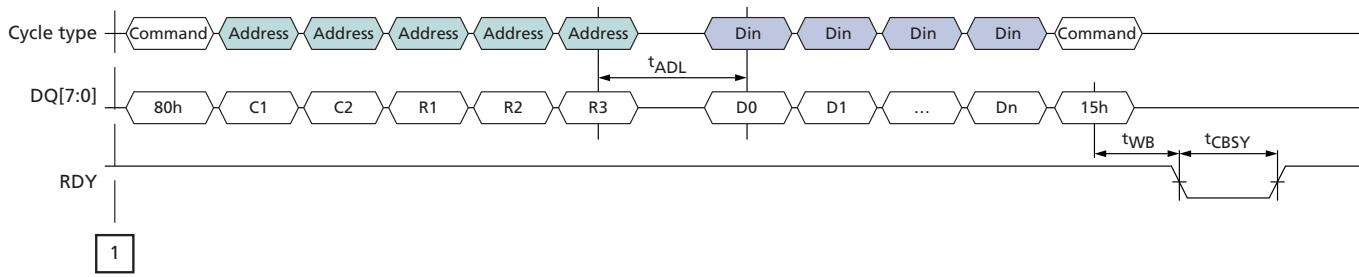
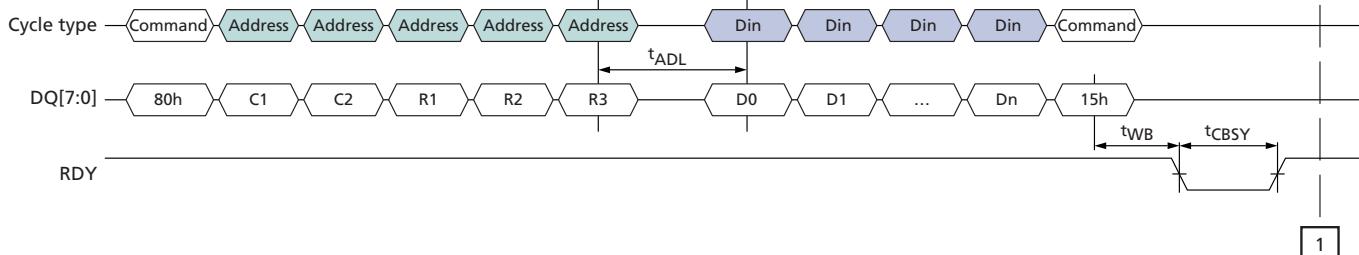
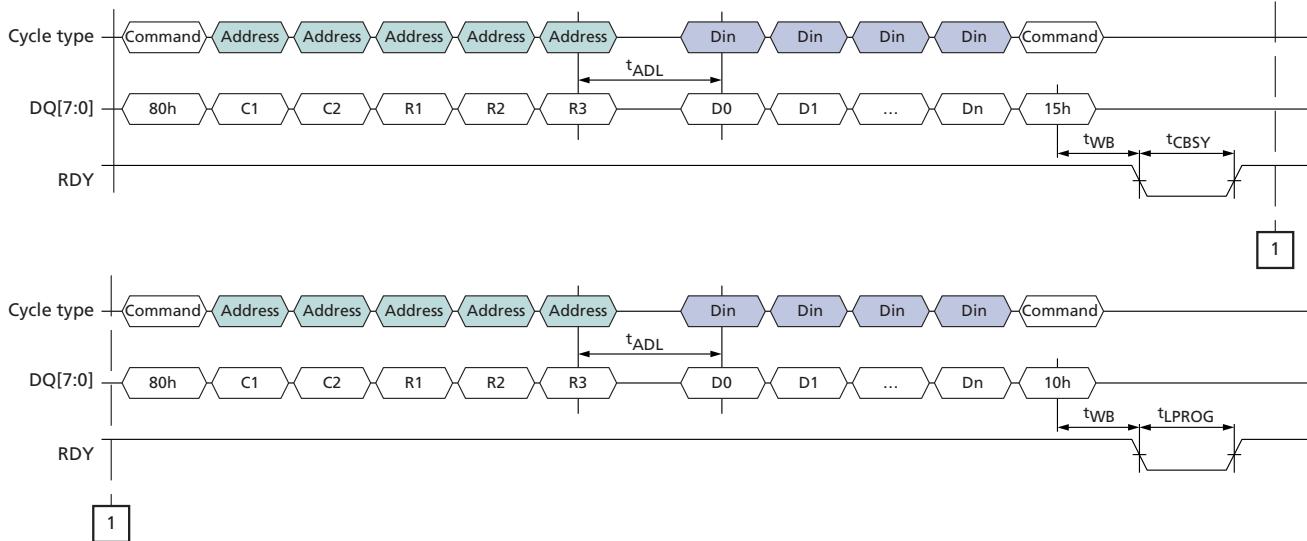


Figure 74: PROGRAM PAGE CACHE (80h–15h) Operation (End)

As defined for
PAGE CACHE PROGRAM



Release: 3/26/13



PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by an 11h command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for 'DBSY.

To determine the progress of 'DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1), additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during 'PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

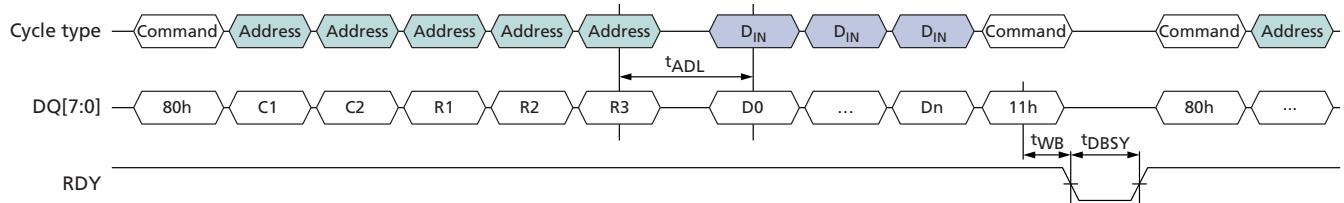
When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a MULTI-PLANE PROGRAM CACHE operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during 'CBSY. After 'CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Multi-Plane Operations for multi-plane addressing requirements.



128Gb to 1Tb Asynchronous/Synchronous NAND Program Operations

Figure 75: PROGRAM PAGE MULTI-PLANE (80h-11h) Operation



For JEDEC compliance the PROGRAM PAGE MULTI-PLANE (81h-11h) command is also supported. This would also include the last command 81h-10h to conclude a PROGRAM PAGE MULTI-PLANE sequence and 81h-15h to conclude a PROGRAM PAGE CACHE MULTI-PLANE sequence.

Release: 3/26/13



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Multi-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

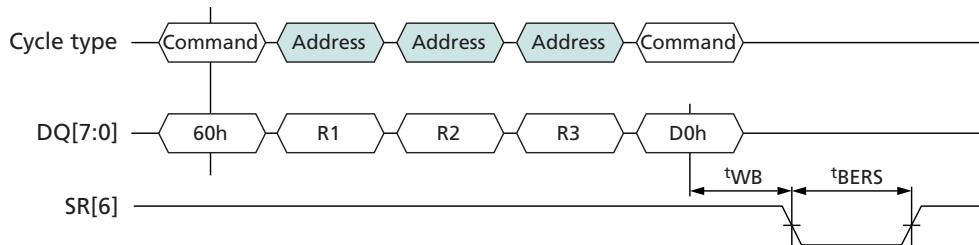
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for t_{BERS} while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 76: ERASE BLOCK (60h-D0h) Operation





ERASE BLOCK MULTI-PLANE (60h-D1h)

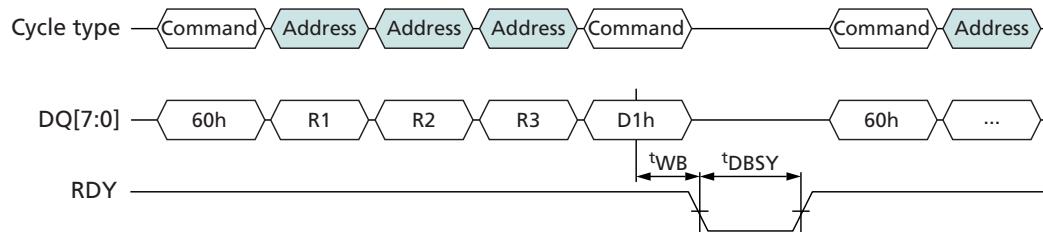
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tDBSY.

To determine the progress of tDBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

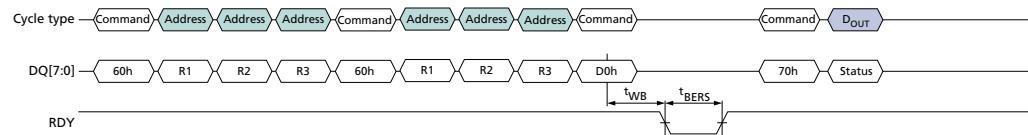
Figure 77: ERASE BLOCK MULTI-PLANE (60h-D1h) Operation



ERASE BLOCK MULTI-PLANE (60h-60h-D0h)

This operation behaves the same as the ERASE BLOCK MULTI-PLANE (60h-D1h) command followed by a ERASE BLOCK (60h-D0h) command.

Figure 78: ERASE BLOCK MULTI-PLANE (60h-60h-D0h) Operation





Copyback Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: status operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). Reset operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

Multi-Plane Copyback Operations

Multi-plane copyback read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Multi-Plane Operations for details.



128Gb to 1Tb Asynchronous/Synchronous NAND Copyback Operations

COPYBACK READ (00h-35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See READ PAGE (00h-30h) (page 126) for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 79: COPYBACK READ (00h-35h) Operation

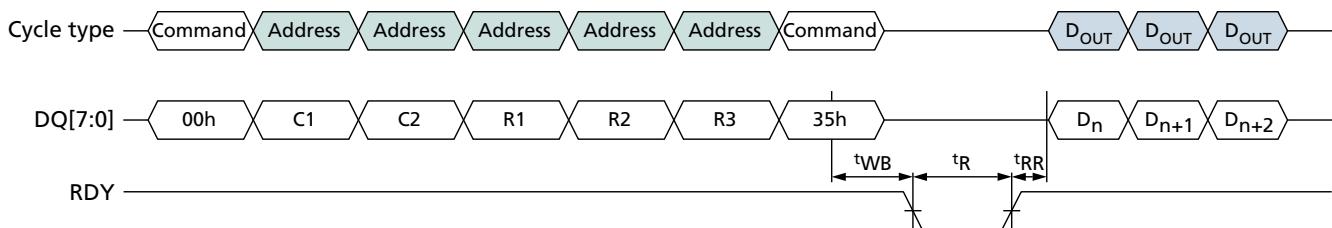
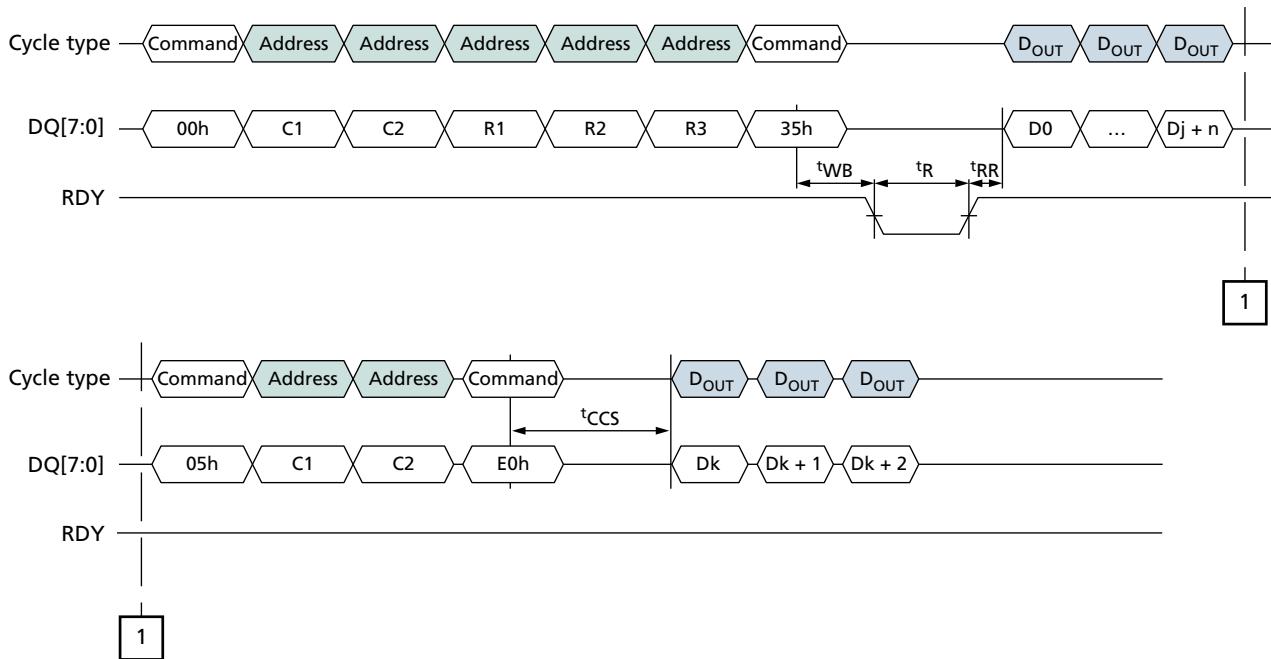


Figure 80: COPYBACK READ (00h-35h) with CHANGE READ COLUMN (05h-E0h) Operation





128Gb to 1Tb Asynchronous/Synchronous NAND Copyback Operations

COPYBACK PROGRAM (85h-10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE (80h-10h) for further details.

Figure 81: COPYBACK PROGRAM (85h-10h) Operation

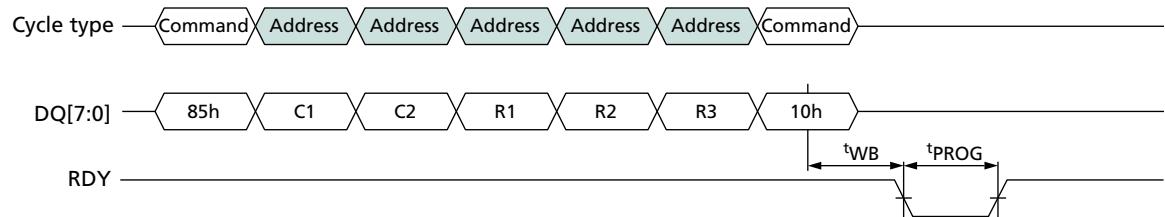
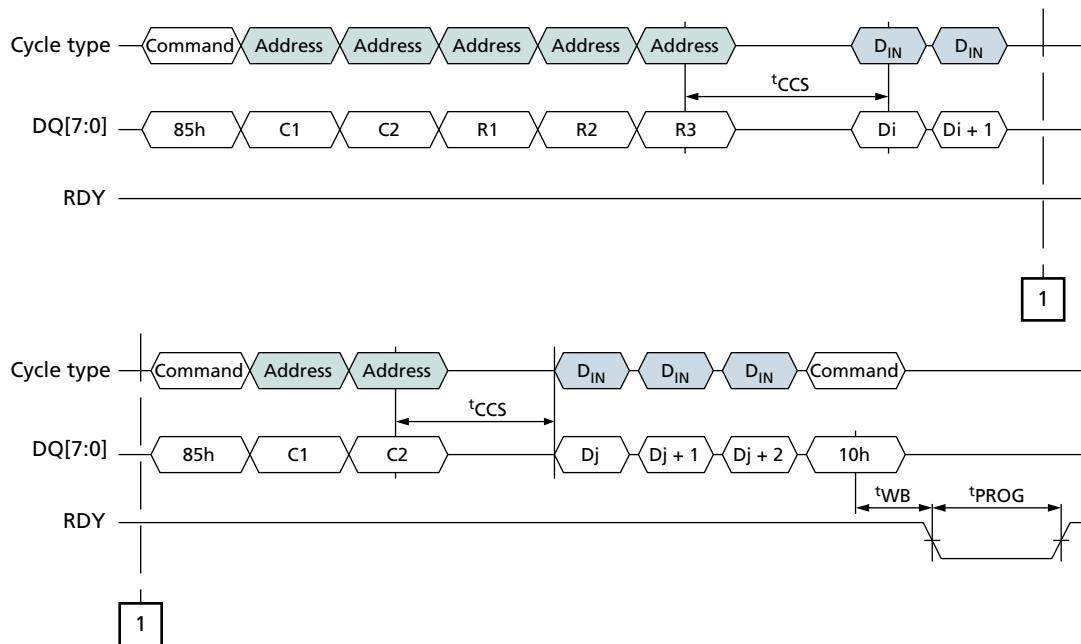


Figure 82: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation



COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MULTI-PLANE is 00h-32h-00h-35h. See READ PAGE MULTI-PLANE (00h-32h) (page 131) for further details.

Release: 3/26/13

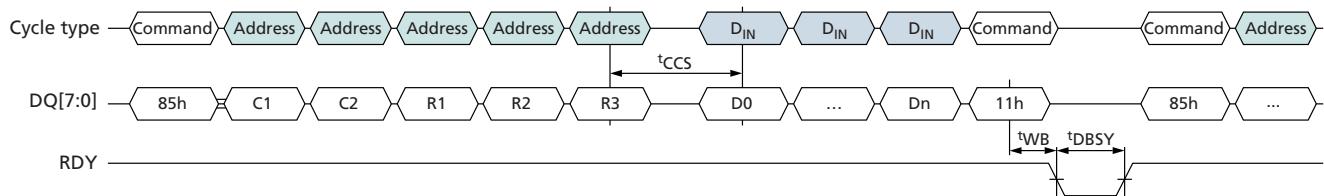


128Gb to 1Tb Asynchronous/Synchronous NAND Copyback Operations

COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE MULTI-PLANE (80h-11h) for further details.

Figure 83: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation



Release: 3/26/13



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Each target has a an OTP area with a range of OTP pages (see Table 29 (page 148)); the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an erased state (all bits are 1). Programming an OTP page changes bits that are 1 to 0, but cannot change bits that are 0 to 1. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area prevents further programming of the pages in the OTP area.

Enabling the OTP Operation Mode

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2 through P4.

When the target is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area.

ERASE commands are not valid while the target is in OTP operation mode.

Programming OTP Pages

Each page in the OTP area is programming using the PROGRAM OTP PAGE (80h-10h) command. Each page can be programmed more than once, in sections, up to the maximum number allowed (see NOP in Table 29 (page 148)). The pages in the OTP area must be programmed in ascending order.

If the host issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the target will be busy for 'OBSY and the WP# status register bit will be 0, meaning that the page is write-protected.

Protecting the OTP Area

To protect the OTP area, issue the OTP PROTECT (80h-10h) command to the OTP Protect Page. When the OTP area is protected it cannot be programmed further. It is not possible to unprotect the OTP area after it has been protected.

Reading OTP Pages

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ (00h-30h) command.

If the host issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid. To determine whether the target is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the READ STATUS ENHANCED (78h) command is prohibited while the OTP operation is in progress.

Returning to Normal Array Operation Mode

To exit OTP operation mode and return to normal array operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the RESET (FFh) command is issued while in OTP operation mode, the target will exit OTP operation mode and enter normal operating mode. If the synchronous interface is active, the target will exit OTP operation and enable the asynchronous interface.



128Gb to 1Tb Asynchronous/Synchronous NAND One-Time Programmable (OTP) Operations

If the SYNCHRONOUS RESET (FCh) command is issued while in the OTP operation mode, the target will exit OTP operation mode and the synchronous interface remains active.

Table 29: OTP Area Details

Description	Value
Number of OTP pages	30
OTP protect page address	01h
OTP start page address	02h
Number of partial page programs (NOP) to each OTP page	2

PROGRAM OTP PAGE (80h-10h)

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. To program data in the OTP area, the target must be in OTP operation mode.

To use the PROGRAM OTP PAGE (80h-10h) command, issue the 80h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, t_{PROG} . The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine whether the operation passed or failed (see Status Operations).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGEWRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, then R/B# goes LOW for t_{OBSY} . After t_{OBSY} , the status register is set to 60h.

Figure 84: PROGRAM OTP PAGE (80h-10h) Operation

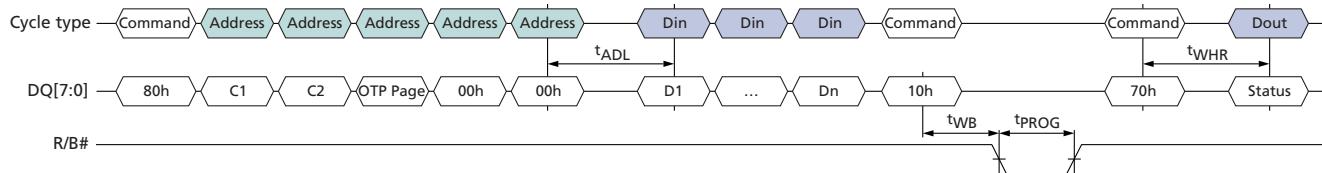
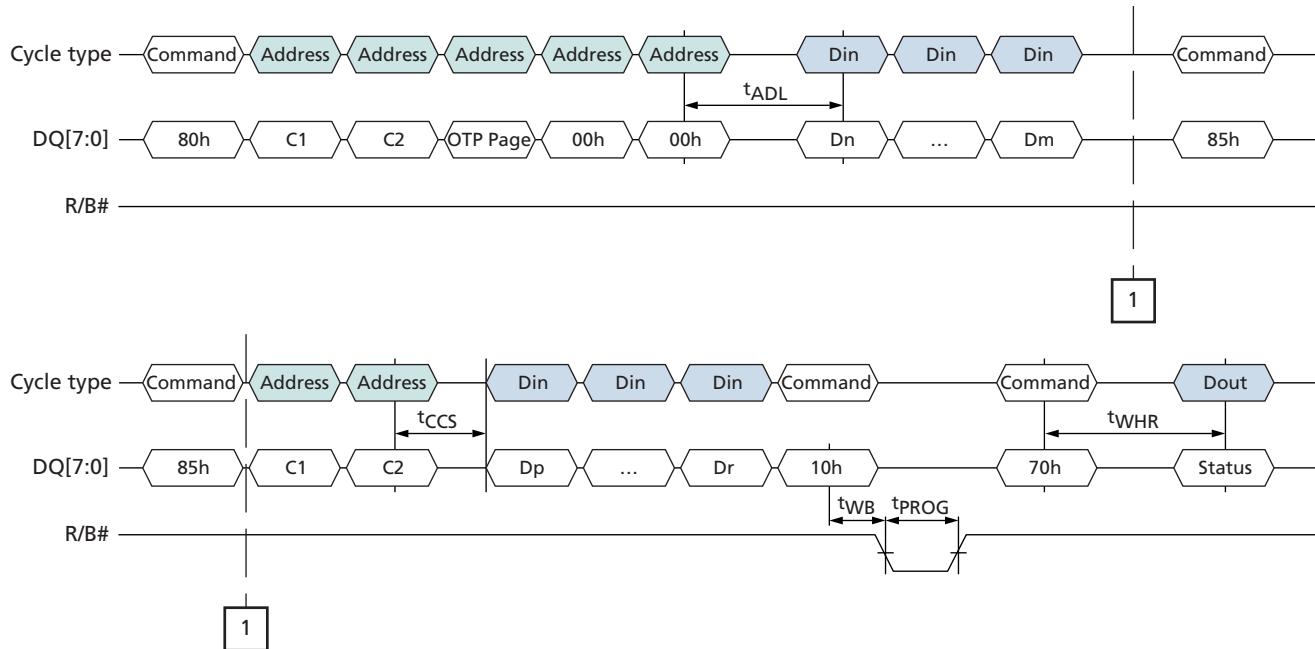



Figure 85: PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation


PROTECT OTP AREA (80h-10h)

The PROTECT OTP AREA (80h-10h) command is used to prevent further programming of the pages in the OTP area. To protect the OTP area, the target must be in OTP operation mode.

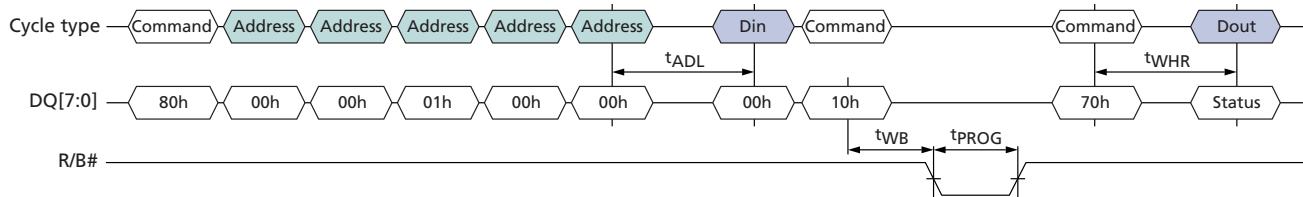
To protect all data in the OTP area, issue the 80h command. Issue five address cycles including the column address, OTP protect page address and block address; the column and block addresses are fixed to 0. Next, write 00h data for the first byte location and issue the 10h command.

R/B# goes LOW for the duration of the array programming time, t_{PROG} . The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Status Operations).

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for t_{OBSY} . After t_{OBSY} , the status register is set to 60h.

Release: 3/26/13


Figure 86: PROTECT OTP AREA (80h-10h) Operation


Note: 1. OTP data is protected following a status confirmation.

READ OTP PAGE (00h-30h)

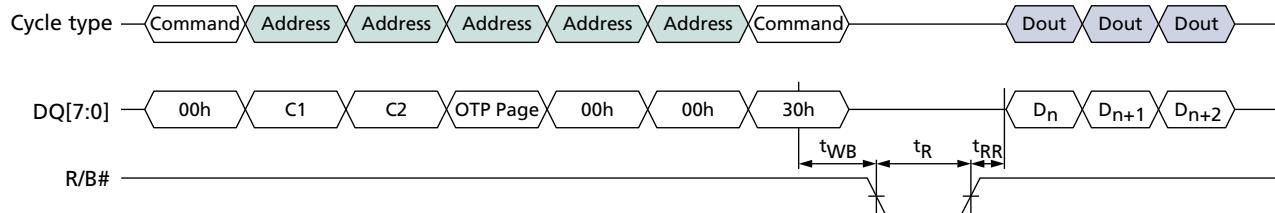
The READ OTP PAGE (00h-30h) command is used to read data from the pages in the OTP area. To read data in the OTP area, the target must be in OTP operation mode.

To use the READ OTP PAGE (00h-30h) command, issue the 00h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, issue the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for t_R as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command can be used. If the status operations are used to monitor the die's (LUN's) status, when the die (LUN) is ready (RDY = 1, ARDY = 1) the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

Additional pages within the OTP area can be read by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the READ STATUS ENHANCED (78h) and CHANGE READ COLUMN ENHANCED (06h-E0h) commands are prohibited.

Figure 87: READ OTP PAGE (00h-30h) Operation




Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM or ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require an address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[9], must be different for each issued address.
- The page address bits, PA[8:0], must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single die (LUN).

Release: 3/26/13



Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see Multi-Plane Operations for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

When issuing combinations of commands to multiple die (LUNs) (e.g. Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), after the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command shall be issued prior to any data output from the selected die (LUN).

Release: 3/26/13



Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 30: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	1998
Total available blocks per LUN	2048
First spare area location	Byte 16,384
Bad-block mark	00h
Minimum required ECC	40-bit ECC per 1100 bytes of data

Release: 3/26/13



Shared Pages

In MLC NAND Flash devices, each memory cell contains two bits of data. These bits are distributed across two NAND pages. Pages within a NAND block that share the same NAND memory cells are referred to as shared pages. If any program operation is interrupted (e.g. power loss or reset), data in previously programmed shared pages can also be corrupted.

The least significant numbered shared page must be programmed before the most significant numbered page of that pair can be programmed.

Table 31: Shared Pages

Shared Pages		Shared Pages	
0	6	1	7
2	-	3	-
4	10	5	11
8	14	9	15
12	18	13	19
16	22	17	23
20	26	21	27
24	30	25	31
28	34	29	35
32	38	33	39
36	42	37	43
40	46	41	47
44	50	45	51
48	54	49	55
52	58	53	59
56	62	57	63
60	66	61	67
64	70	65	71
68	74	69	75
72	78	73	79
76	82	77	83
80	86	81	87
84	90	85	91
88	94	89	95
92	98	93	99
96	102	97	103
100	106	101	107
104	110	105	111
108	114	109	115
112	118	113	119

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Shared Pages

Table 31: Shared Pages (Continued)

Shared Pages		Shared Pages	
116	122	117	123
120	126	121	127
124	130	125	131
128	134	129	135
132	138	133	139
136	142	137	143
140	146	141	147
144	150	145	151
148	154	149	155
152	158	153	159
156	162	157	163
160	166	161	167
164	170	165	171
168	174	169	175
172	178	173	179
176	182	177	183
180	186	181	187
184	190	185	191
188	194	189	195
192	198	193	199
196	202	197	203
200	206	201	207
204	210	205	211
208	214	209	215
212	218	213	219
216	222	217	223
220	226	221	227
224	230	225	231
228	234	229	235
232	238	233	239
236	242	237	243
240	246	241	247
244	250	245	251
248	254	249	255
252	258	253	259
256	262	257	263
260	266	261	267
264	270	265	271

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Shared Pages

Table 31: Shared Pages (Continued)

Shared Pages		Shared Pages	
268	274	269	275
272	278	273	279
276	282	277	283
280	286	281	287
284	290	285	291
288	294	289	295
292	298	293	299
296	302	297	303
300	306	301	307
304	310	305	311
308	314	309	315
312	318	313	319
316	322	317	323
320	326	321	327
324	330	325	331
328	334	329	335
332	338	333	339
336	342	337	343
340	346	341	347
344	350	345	351
348	354	349	355
352	358	353	359
356	362	357	363
360	366	361	367
364	370	365	371
368	374	369	375
372	378	373	379
376	382	377	383
380	386	381	387
384	390	385	391
388	394	389	395
392	398	393	399
396	402	397	403
400	406	401	407
404	410	405	411
408	414	409	415
412	418	413	419
416	422	417	423

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Shared Pages

Table 31: Shared Pages (Continued)

Shared Pages		Shared Pages	
420	426	421	427
424	430	425	431
428	434	429	435
432	438	433	439
436	442	437	443
440	446	441	447
444	450	445	451
448	454	449	455
452	458	453	459
456	462	457	463
460	466	461	467
464	470	465	471
468	474	469	475
472	478	473	479
476	482	477	483
480	486	481	487
484	490	485	491
488	494	489	495
492	498	493	499
496	502	497	503
500	506	501	507
504	-	505	-
508	-	509	-
510	-	511	-

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Output Drive Impedance

Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers: 18 ohms, 25 ohms, 35 ohms, and 50 ohms.

The 35 ohm output drive strength setting is the power-on default value. The host can select a different drive strength setting using the SET FEATURES (EFh) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 32: Output Drive Strength Conditions ($V_{CCQ} = 1.7\text{--}1.95V$)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	T_A (MIN)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	T_A (MAX)

Table 33: Output Drive Strength Impedance Values ($V_{CCQ} = 1.7\text{--}1.95V$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
18 Ohms	Rpd	$V_{CCQ} \times 0.2$	8.2	14.0	23.8	ohms
		$V_{CCQ} \times 0.5$	11.7	18.0	24.3	ohms
		$V_{CCQ} \times 0.8$	14.0	23.0	34.5	ohms
	Rpu	$V_{CCQ} \times 0.2$	14.0	23.0	34.5	ohms
		$V_{CCQ} \times 0.5$	11.7	18.0	24.3	ohms
		$V_{CCQ} \times 0.8$	8.2	14.0	23.8	ohms
25 Ohms	Rpd	$V_{CCQ} \times 0.2$	11.4	20.0	32.0	ohms
		$V_{CCQ} \times 0.5$	16.3	25.0	33.7	ohms
		$V_{CCQ} \times 0.8$	20.0	31.0	49.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	20.0	31.0	49.0	ohms
		$V_{CCQ} \times 0.5$	16.3	25.0	33.7	ohms
		$V_{CCQ} \times 0.8$	11.4	20.0	32.0	ohms
35 Ohms	Rpd	$V_{CCQ} \times 0.2$	16.0	27.5	44.5	ohms
		$V_{CCQ} \times 0.5$	22.7	35.0	47.3	ohms
		$V_{CCQ} \times 0.8$	28.0	45.0	69.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	28.0	45.0	69.0	ohms
		$V_{CCQ} \times 0.5$	22.7	35.0	47.3	ohms
		$V_{CCQ} \times 0.8$	16.0	27.5	44.5	ohms

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Output Drive Impedance

Table 33: Output Drive Strength Impedance Values ($V_{CCQ} = 1.7\text{--}1.95V$) (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 Ohms	Rpd	$V_{CCQ} \times 0.2$	24.0	40.0	63.0	ohms
		$V_{CCQ} \times 0.5$	32.5	50.0	67.5	ohms
		$V_{CCQ} \times 0.8$	40.0	64.0	98.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	40.0	64.0	98.0	ohms
		$V_{CCQ} \times 0.5$	32.5	50.0	67.5	ohms
		$V_{CCQ} \times 0.8$	24.0	40.0	63.0	ohms

Table 34: Output Drive Strength Conditions ($V_{CCQ} = 2.7\text{--}3.6V$)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	3.6V	T_A (MIN)
Nominal	Typical-Typical	3.3V	+25°C
Maximum	Slow-Slow	2.7V	T_A (MAX)

Table 35: Output Drive Strength Impedance Values ($V_{CCQ} = 2.7\text{--}3.6V$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
18 Ohms	Rpd	$V_{CCQ} \times 0.2$	7.0	16.2	28.7	ohms
		$V_{CCQ} \times 0.5$	9.0	18.0	36.0	ohms
		$V_{CCQ} \times 0.8$	11.8	21.0	50.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	11.8	21.0	50.0	ohms
		$V_{CCQ} \times 0.5$	9.0	18.0	36.0	ohms
		$V_{CCQ} \times 0.8$	7.0	14.0	28.7	ohms
25 Ohms	Rpd	$V_{CCQ} \times 0.2$	9.3	22.3	40.0	ohms
		$V_{CCQ} \times 0.5$	12.6	25.0	50.0	ohms
		$V_{CCQ} \times 0.8$	16.3	29.0	68.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	16.3	29.0	68.0	ohms
		$V_{CCQ} \times 0.5$	12.6	25.0	50.0	ohms
		$V_{CCQ} \times 0.8$	9.3	19.0	40.0	ohms
35 Ohms	Rpd	$V_{CCQ} \times 0.2$	12.8	32.0	58.0	ohms
		$V_{CCQ} \times 0.5$	18.0	35.0	70.0	ohms
		$V_{CCQ} \times 0.8$	23.0	40.0	95.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	23.0	40.0	95.0	ohms
		$V_{CCQ} \times 0.5$	18.0	35.0	70.0	ohms
		$V_{CCQ} \times 0.8$	12.8	32.0	58.0	ohms

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Output Drive Impedance

Table 35: Output Drive Strength Impedance Values ($V_{CCQ} = 2.7\text{--}3.6V$) (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 Ohms	Rpd	$V_{CCQ} \times 0.2$	18.4	45.0	80.0	ohms
		$V_{CCQ} \times 0.5$	25.0	50.0	100.0	ohms
		$V_{CCQ} \times 0.8$	32.0	57.0	136.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	32.0	57.0	136.0	ohms
		$V_{CCQ} \times 0.5$	25.0	50.0	100.0	ohms
		$V_{CCQ} \times 0.8$	18.4	45.0	80.0	ohms

Table 36: Pull-Up and Pull-Down Output Impedance Mismatch for Asynchronous and NV-DDR

Drive Strength	Minimum	Maximum	Unit	Notes
18 Ohms	0	6.3	ohms	1, 2
25 Ohms	0	8.8	ohms	1, 2
35 Ohms	0	12.3	ohms	1, 2
50 Ohms	0	17.5	ohms	1, 2

Notes: 1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
 2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, $T_A = T_{OPER}$.

Table 37: Pull-Up and Pull-Down Output Impedance Mismatch for NV-DDR2

Drive Strength	Minimum	Maximum	Unit	Notes
18 Ohms	0	3.2	ohms	1, 2
25 Ohms	0	4.4	ohms	1, 2
35 Ohms	0	6.2	ohms	1, 2
50 Ohms	0	8.8	ohms	1, 2

Notes: 1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
 2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, $T_A = T_{OPER}$.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND AC Overshoot/Undershoot Specifications

AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host.

Table 38: Asynchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V _{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area below V _{SSQ}	3	3	3	3	3	3	V-ns

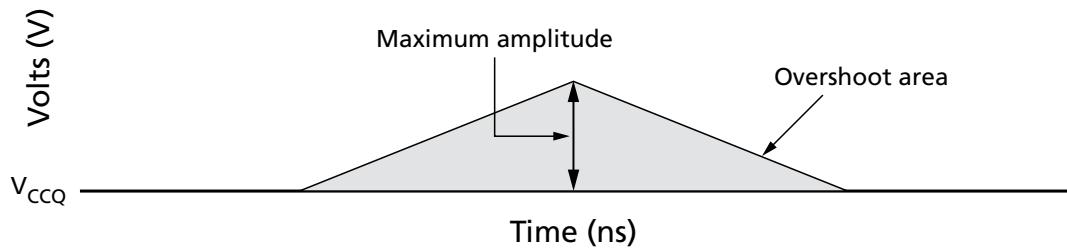
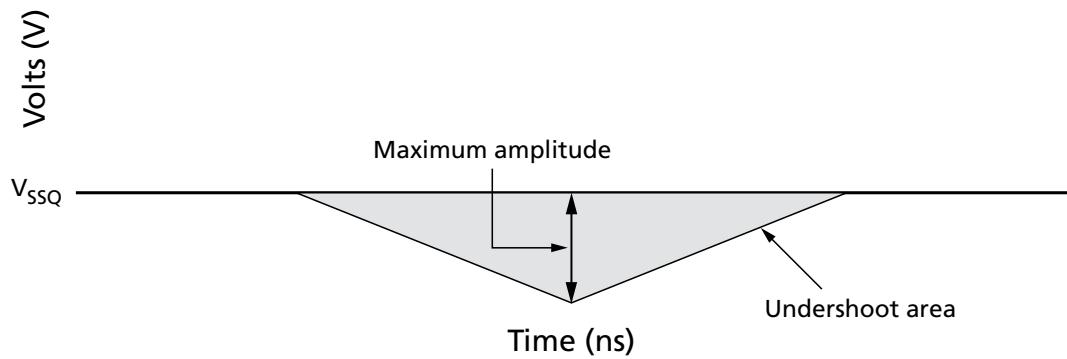
Table 39: NV-DDR Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V _{CCQ}	3	3	3	2.25	1.8	1.5	V-ns
Maximum undershoot area below V _{SSQ}	3	3	3	2.25	1.8	1.5	V-ns

Table 40: NV-DDR2 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode								Unit
		0	1	2	3	4	5	6	7	
Maximum peak amplitude provided for overshoot area	-	1	1	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	-	1	1	1	1	1	1	1	1	V
Maximum overshoot area above V _{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	
Maximum undershoot area below V _{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	

Release: 3/26/13

**128Gb to 1Tb Asynchronous/Synchronous NAND
AC Overshoot/Undershoot Specifications****Figure 88: Overshoot****Figure 89: Undershoot**

Release: 3/26/13



Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 41: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge	$V_{IL(DC)}$ To $V_{IH(AC)}$ for NV-DDR and $V_{IL(AC)}$ To $V_{IH(AC)}$ for NV-DDR2
Falling edge	$V_{IH(DC)}$ To $V_{IL(AC)}$ for NV-DDR and $V_{IH(AC)}$ To $V_{IL(AC)}$ for NV-DDR2
Temperature range	T_A

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 42: NV-DDR Maximum and Minimum Input Slew Rate

Description	Timing Modes 0-5	Unit
Input slew rate (min)	0.5	V/ns
Input slew rate (max)	4.5	V/ns

Table 43: Input Slew Rate derating for NV-DDR ($V_{CCQ} = 1.7\text{--}1.95V$)

Command/ Address and DQ V/ns	CLK/DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)} = 540mV$, $V_{IH(DC)}/V_{IL(DC)} = 360mV$																Unit	
	1		0.9		0.8		0.7		0.6		0.5		0.4		0.3			
	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold		
1	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	ps	
0.9	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	ps	
0.8	-	-	0	0	0	0	0	-	-	-	-	-	-	-	-	-	ps	
0.7	-	-	-	-	0	0	0	0	0	-	-	-	-	-	-	-	ps	
0.6	-	-	-	-	-	-	0	0	0	0	0	0	-	-	-	-	ps	
0.5	-	-	-	-	-	-	-	-	0	0	0	0	180	180	-	-	ps	
0.4	-	-	-	-	-	-	-	-	-	-	180	180	360	360	660	660	ps	
0.3	-	-	-	-	-	-	-	-	-	-	-	-	660	660	920	920	ps	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Input Slew Rate

Table 44: Input Slew Rate derating for NV-DDR/NV-DDR2 ($V_{CCQ} = 2.7\text{--}3.6\text{V}$)

Command/ Address and DQ V/ns	CLK/DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)} = 990\text{mV}$, $V_{IH(DC)}/V_{IL(DC)} = 660\text{mV}$																Unit	
	1		0.9		0.8		0.7		0.6		0.5		0.4		0.3			
	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold		
1	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	ps	
0.9	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	ps	
0.8	-	-	0	0	0	0	0	0	-	-	-	-	-	-	-	-	ps	
0.7	-	-	-	-	0	0	0	0	0	0	-	-	-	-	-	-	ps	
0.6	-	-	-	-	-	0	0	0	0	0	0	0	-	-	-	-	ps	
0.5	-	-	-	-	-	-	-	-	0	0	0	0	330	330	-	-	ps	
0.4	-	-	-	-	-	-	-	-	-	-	330	330	660	660	1210	1210	ps	
0.3	-	-	-	-	-	-	-	-	-	-	-	-	1210	1210	1760	1760	ps	

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR2 operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 45: NV-DDR2 Maximum and Minimum Input Slew Rate

Description	Single Ended	Differential	Unit
	Timing Modes 0-7	Timing Modes 0-7	
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

For DQ signals when used for input, the total data setup time (t^{DS}) and data hold time (t^{DH}) required is calculated by adding a derating value to the t^{DS} and t^{DH} values indicated for the timing mode. To calculate the total data setup time, t^{DS} is incremented by the appropriate Δ set derating value. To calculate the total data hold time, t^{DH} is incremented by the appropriate Δ hold derating value. Table 46 (page 165) provides the derating values when differential DQS (DQS_t/DQS_c) is used. Table 47 (page 165) provides the derating values when single-ended DQS is used.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between the shaded ' $V_{REFQ(DC)}$ to AC region', then the derating value uses the nominal slew rate shown in Figure 90 (page 166). If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REFQ(DC)}$ to AC region', then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 91 (page 167).

The hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$. The hold nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the nominal slew rate shown in Figure 92 (page 168). If the actual signal is earlier than the

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Input Slew Rate

nominal slew rate line anywhere between the shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the $V_{REFQ(DC)}$ level shown in Figure 93 (page 169).

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses $V_{REFQ(DC)}$, not the actual signal (refer to Figure 91 (page 167) and Figure 93 (page 169)).

For slew rates not explicitly listed in Table 46 (page 165) and Table 47 (page 165), the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

Table 46: Input Slew Rate derating for NV-DDR2 single-ended ($V_{CCQ} = 1.7\text{--}1.95V$)

DQ					DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)} = 250\text{mV}$, $V_{IH(DC)}/V_{IL(DC)} = 125\text{mV}$																Unit
	2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3		
	V/ns	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold		
2	0	0	0	0	0	14	0	31	0	54	0	83	0	125	0	188	0	292	0	ps	
1.5	0	0	0	0	0	14	0	31	0	54	0	83	0	125	0	188	0	292	0	ps	
1	0	0	0	0	0	14	0	31	0	54	0	83	0	125	0	188	0	292	0	ps	
0.9	14	0	14	0	14	0	28	0	45	0	67	0	97	0	139	0	201	0	306	0	ps
0.8	31	0	31	0	31	0	45	0	63	0	85	0	115	0	156	0	219	0	324	0	ps
0.7	54	0	54	0	54	0	67	0	85	0	107	0	137	0	179	0	241	0	346	0	ps
0.6	83	0	83	0	83	0	97	0	115	0	137	0	167	0	208	0	271	0	376	0	ps
0.5	125	0	125	0	125	0	139	0	156	0	179	0	208	0	250	0	313	0	418	0	ps
0.4	188	0	188	0	188	0	201	0	219	0	241	0	271	0	313	0	375	0	480	0	ps
0.3	292	0	292	0	292	0	306	0	324	0	346	0	376	0	418	0	480	0	594	0	ps

Table 47: Input Slew Rate derating for NV-DDR2 differential ($V_{CCQ} = 1.7\text{--}1.95V$)

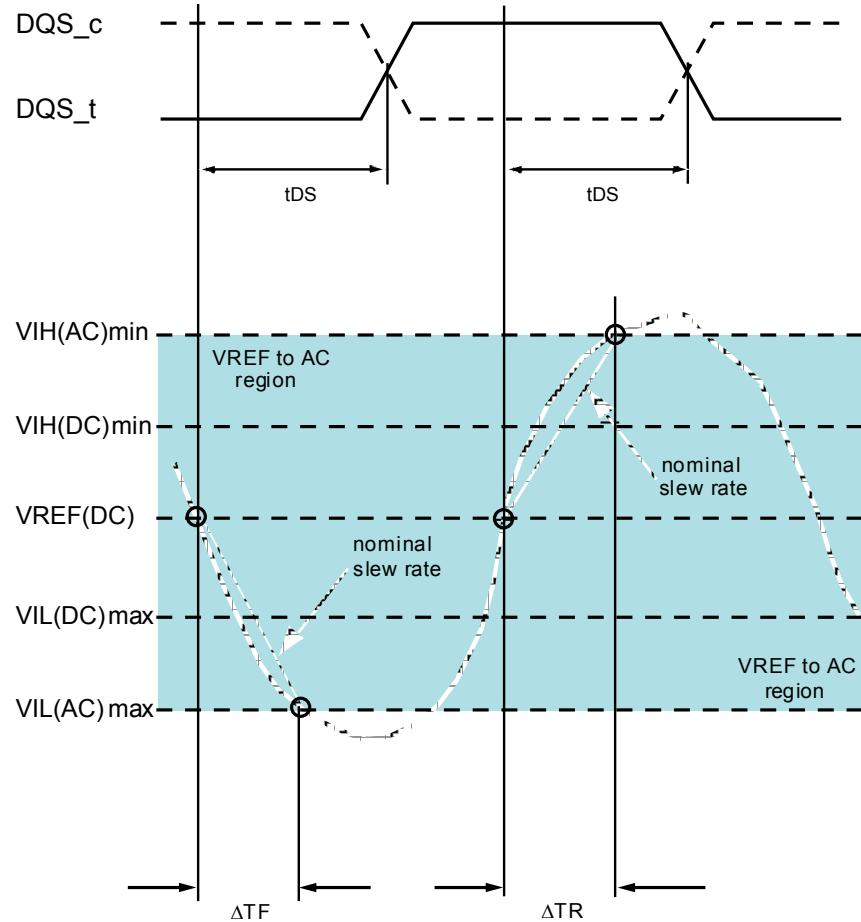
DQ	DQS_t/DQS_c Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)} = 250\text{mV}$, $V_{IH(DC)}/V_{IL(DC)} = 125\text{mV}$																Unit
	2		1.8		1.6		1.4		1.2		1		0.8		0.6		
	V/ns	set	hold														
2	0	0	7	0	16	0	27	0	42	0	63	0	93	0	144	0	ps
1.5	0	0	7	0	16	0	27	0	42	0	63	0	93	0	144	0	ps
1	0	0	7	0	16	0	27	0	42	0	63	0	93	0	144	0	ps
0.9	14	0	21	0	30	0	41	0	56	0	76	0	106	0	157	0	ps
0.8	31	0	38	0	47	0	58	0	73	0	94	0	124	0	175	0	ps
0.7	54	0	61	0	69	0	80	0	95	0	116	0	146	0	197	0	ps
0.6	83	0	90	0	99	0	110	0	125	0	146	0	176	0	227	0	ps
0.5	125	0	132	0	141	0	152	0	167	0	188	0	218	0	269	0	ps
0.4	188	0	194	0	203	0	214	0	229	0	250	0	282	0	333	0	ps
0.3	292	0	299	0	308	0	319	0	334	0	355	0	385	0	436	0	ps

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Input Slew Rate

Figure 90: Nominal Slew Rate for Data Setup Time (t_{DS}), NV-DDR2 only



$$\text{Setup Slew Rate}_{\text{Falling Signal}} = \frac{V_{REF(DC)} - V_{IL(AC)\max}}{\Delta TF} \quad \text{Setup Slew Rate}_{\text{Rising Signal}} = \frac{V_{IL(AC)\min} - V_{REF(DC)}}{\Delta TR}$$

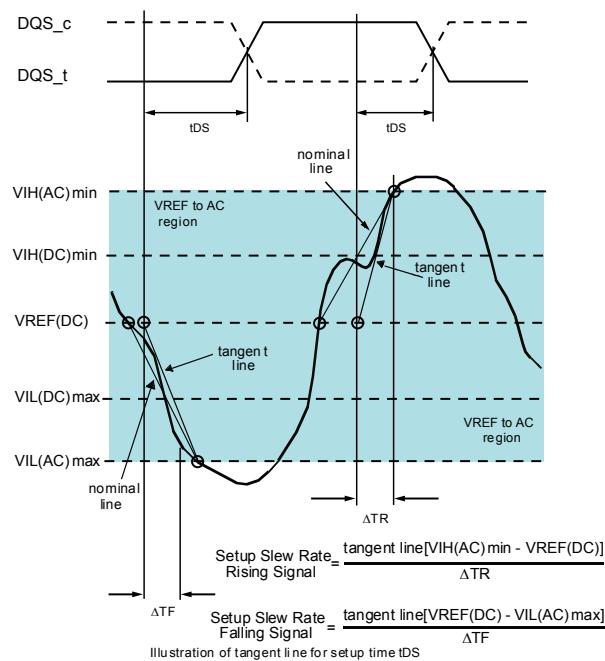
Illustration of nominal slew rate for setup time t_{DS}

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Input Slew Rate

Figure 91: Tangent Line for Data Setup Time (t_{DS}), NV-DDR2 only

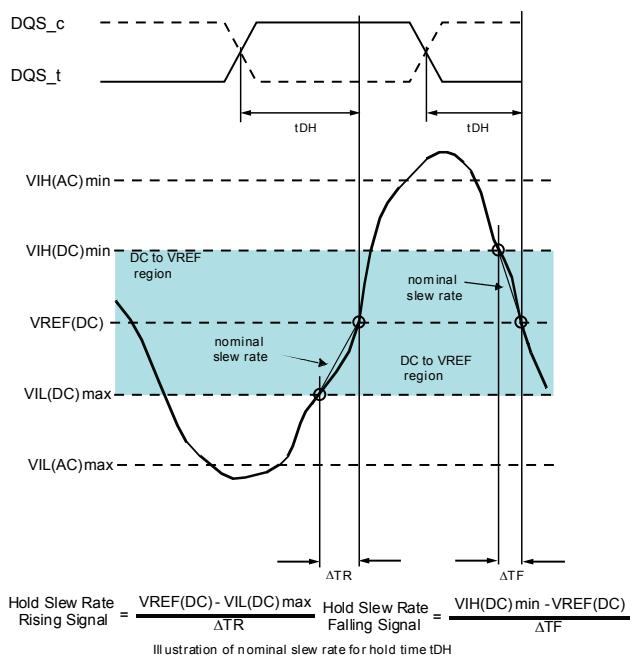


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Input Slew Rate

Figure 92: Nominal Slew Rate for Data Hold Time (t_{DH}), NV-DDR2 only

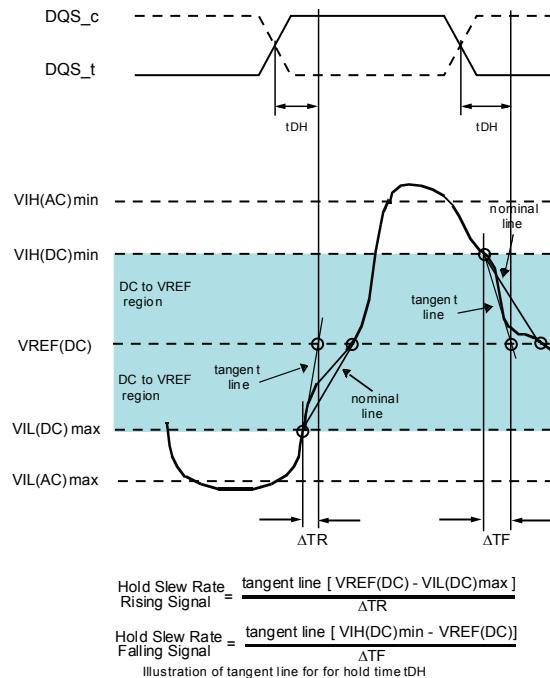


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Input Slew Rate

Figure 93: Tangent Line for Data Hold Time (t_{DH}), NV-DDR2 only



Release: 3/26/13



Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 48: Test Conditions for Output Slew Rate

Parameter	Asynchronous/NV-DDR Interface	NV-DDR2 Single-Ended ¹	NV-DDR2 Differential ¹
$V_{OL(DC)}$	$0.4 \times V_{CCQ}$	-	-
$V_{OH(DC)}$	$0.6 \times V_{CCQ}$	-	-
$V_{OL(AC)}^2$	$0.3 \times V_{CCQ}$	$V_{TT} - (V_{CCQ} * 0.15)$	-
$V_{OH(AC)}^2$	$0.7 \times V_{CCQ}$	$V_{TT} + (V_{CCQ} * 0.15)$	-
$V_{OLdiff(AC)}$	-	-	$-0.3 \times V_{CCQ}$
$V_{OHdiff(AC)}$	-	-	$0.3 \times V_{CCQ}$
Rising edge (t_{RISE})	$V_{OL(DC)}$ to $V_{OH(AC)}$	$V_{OL(AC)}$ to $V_{OH(AC)}$	-
Falling edge (t_{FALL})	$V_{OH(DC)}$ to $V_{OL(AC)}$	$V_{OH(AC)}$ to $V_{OL(AC)}$	-
Differential rising edge ($t_{RISEdiff}$)	-	-	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Differential falling edge ($t_{FALLdiff}$)	-	-	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	$[V_{OH(AC)} - V_{OL(DC)}] / t_{RISE}$	$[V_{OH(AC)} - V_{OL(AC)}] / t_{RISE}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / t_{RISEdiff}$
Output slew rate falling edge	$[V_{OH(DC)} - V_{OL(AC)}] / t_{FALL}$	$[V_{OH(AC)} - V_{OL(AC)}] / t_{FALL}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}] / t_{FALLdiff}$
Output reference load ²	50 Ohm to V_{TT}	50 Ohm to V_{TT}	50 Ohm to V_{TT}
Temperature range	T_A	T_A	T_A

Notes:

1. 1.8V V_{CCQ} is required for NV-DDR2 operations.
2. V_{TT} is 0.5 x V_{CCQ} .

Table 49: Output Slew Rate for Asynchronous and NV-DDR ($V_{CCQ} = 2.7\text{--}3.6V$)

Output Drive Strength	Min	Max	Unit
18 Ohms	1.5	10	V/ns
25 Ohms	1.5	9	V/ns
35 Ohms	1.2	7	V/ns
50 Ohms	1	5.5	V/ns

Table 50: Output Slew Rate for Single-Ended NV-DDR or NV-DDR2 ($V_{CCQ} = 1.7\text{--}1.95V$)

Output Drive Strength	Min	Max	Unit
18 Ohms	1	5.5	V/ns
25 Ohms	0.85	5	V/ns

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Output Slew Rate

Table 50: Output Slew Rate for Single-Ended NV-DDR or NV-DDR2 ($V_{CCQ} = 1.7\text{--}1.95V$) (Continued)

Output Drive Strength	Min	Max	Unit
35 Ohms	0.75	4	V/ns
50 Ohms	0.6	4	V/ns

Table 51: Output Slew Rate for Differential NV-DDR2 ($V_{CCQ} = 1.7\text{--}1.95$)

Output Drive Strength	Min	Max	Unit
18 Ohms	2.0	11.0	V/ns
25 Ohms	1.7	10.0	V/ns
35 Ohms	1.5	8.0	V/ns
50 Ohms	1.2	8.0	V/ns

Table 52: Output Slew Rate Matching Ratio for NV-DDR2

Drive Strength	Minimum	Maximum
Output Slew Rate matching ratio (pull-up to pull-down)	0.7	1.4

- Notes:
1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
 2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Release: 3/26/13



Power Cycle Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 53: Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	ns

Release: 3/26/13



Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 54: Absolute Maximum Ratings by Device

Parameter	Symbol	Min ¹	Max ¹	Unit
Voltage input	V _{IN}	-0.6	4.6	V
V _{CC} supply voltage	V _{CC}	-0.6	4.6	V
V _{CCQ} supply voltage	V _{CCQ}	-0.6	4.6	V
V _{PP} supply voltage	V _{PP}	-0.6	16	V
V _{REFQ} supply voltage	V _{REFQ}	-0.6	4.6	V
Storage temperature	T _{STG}	-65	+150	°C

Note: 1. Voltage on any pin relative to V_{SS}.

Table 55: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature	T _A	0	–	+70	°C
Industrial		-40	–	+85	
V _{CC} supply voltage	V _{CC}	2.7	3.3	3.6	V
V _{CCQ} supply voltage (3.3V)	V _{CCQ}	2.7	3.3	3.6	V
V _{CCQ} supply voltage (1.8V)		1.7	1.8	1.95	V
V _{PP} supply voltage (12V)	V _{PP}	10.8	12.0	13.2	V
V _{REFQ} supply voltage (0.9V)	V _{REFQ}	0.49 x V _{CCQ}	0.5 x V _{CCQ}	0.51 x V _{CCQ}	V
V _{SS} ground voltage	V _{SS}	0	0	0	V

Table 56: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	1998	2048	Blocks	1

Note: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications

Table 57: Capacitance: 152-Ball BGA Package

Description	Symbol	Single Die/Dual Die Package			Quad Die Package			Octal Die Package			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input capacitance (CLK/WE#)	C _{CK}	3.2	4.2	5.2	5.2	6.7	8.2	9.6	11.6	13.6	pF	3
Input capacitance (ALE, CLE, RE#/RE_t, RE_c, W/R#)	C _{IN}	3.6	4.6	5.6	6.0	7.5	9.0	11.2	13.2	15.2	pF	3
Input/output capacitance (DQ[7:0], DQS/DQS_t, DQS_c)	C _{IO}	4.0	5.0	6.0	7.0	8.5	10.0	13.2	15.2	17.2	pF	3
Input capacitance (CE#, WP#)	C _{OTHER}	—	—	5	—	—	8	—	—	12	pF	
Delta input capacitance	DC _{IN}	—	—	1.4	—	—	1.7	—	—	2	pF	
Delta input/output capacitance	DC _{IO}	—	—	1.4	—	—	1.7	—	—	2	pF	

Notes:

1. Verified in device characterization; not 100% tested.
2. Test conditions: T_A = 25°C, f = 100 MHz, V_{IN} = 0V.
3. Values for C_{CK}, C_{IN} and C_{IO} (TYP) are estimates.

Table 58: Test Conditions

Parameter	Asynchronous and NV-DDR	NV-DDR2 single-ended	NV-DDR2 differential	Notes
Rising input transition	V _{IL(DC)} to V _{IH(AC)}	V _{IL(DC)} to V _{IH(AC)}	V _{ILdiff(DC)} max to V _{IH-diff(AC)min}	1
Falling input transition	V _{IH(DC)} to V _{IL(AC)}	V _{IH(DC)} to V _{IL(AC)}	V _{IHdiff(DC)} max to V _{IL-diff(AC)max}	1
Input rise and fall slew rates	1 V/ns	1 V/ns	2 V/ns	—
Input timing levels	V _{CCQ} /2	V _{REFQ}	cross-point	—
Output timing levels	V _{CCQ} /2	V _{TT}	cross-point	
Output load: Nominal output drive strength	50 Ohm to V _{TT}	50 Ohm to V _{TT}	50 Ohm to V _{TT}	2, 3, 4

Notes:

1. The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
2. Transmission line delay is assumed to be very small.
3. This test setup applies to all package configurations.
4. V_{TT} is 0.5 x V_{CCQ}.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Table 59: DC Characteristics and Operating Conditions (Asynchronous Interface)

Parameter	Conditions	Symbol	Min ¹	Typ ¹	Max ¹	Unit
Array read current (active)	–	I _{CC1_A}	–	25	50	mA
Array program current (active)	–	I _{CC2_A}	–	25	50	mA
Erase current (active)	–	I _{CC3_A}	–	25	50	mA
I/O burst read current	$t_{RC} = t_{RC} (\text{MIN})$; I _{OUT} = 0mA	I _{CC4R_A}	–	7	10	mA
		I _{CC4QR_A}	–	TBD	TBD	mA
I/O burst write current	$t_{WC} = t_{WC} (\text{MIN})$	I _{CC4w_A}	–	8	10	mA
		I _{CC4QW_A}	–	TBD	TBD	mA
Bus idle current	–	I _{CC5_A}	–	5	7	mA
Current during first RESET command after power-on	–	I _{CC6}	–	–	10	mA
V _{PP} current (active)	During I _{CC1_A} or I _{CC2_A}	I _{PPA}	–	–	5	mA
V _{PP} current (idle)	V _{PP} is supplied and not enabled	I _{PPi}	–	–	10	μA
Standby current - V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	–	15	75	μA
Standby current - V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	–	3	10	μA
Staggered power-up current	$t_{RISE} = 1\text{ms}$; C _{LINE} = 0.1uF	I _{ST}	–	–	10	mA

Note: 1. All values are per die (LUN) unless otherwise specified.

Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 60: DC Characteristics and Operating Conditions (NV-DDR and NV-DDR2 Interface)

Parameter	Conditions	Symbol	Min ¹	Typ ¹	Max ¹	Unit
Array read current (active)	CE# = V _{IL} ; t _{CK} = t _{CK} (MIN) NV-DDR	I _{CC1_S}	–	25	50	mA
Array program current (active)	t _{CK} = t _{CK} (MIN) NV-DDR	I _{CC2_S}	–	25	50	mA
Erase current (active)	t _{CK} = t _{CK} (MIN) NV-DDR	I _{CC3_S}	–	25	50	mA
I/O burst read current	t _{CK} = t _{CK} (MIN) NV-DDR; t _{RC} = t _{RC} (MIN) NV-DDR2; I _{OUT} = 0mA	I _{CC4R_S}	–	16 ²	20 ²	mA
		25 ³	30 ³			
		I _{CC4QR_S}	–	TBD ²	TBD ²	mA
				TBD ³	TBD ³	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 60: DC Characteristics and Operating Conditions (NV-DDR and NV-DDR2 Interface) (Continued)

Parameter	Conditions	Symbol	Min ¹	Typ ¹	Max ¹	Unit
I/O burst write current	$t_{CK} = t_{CK}$ (MIN) NV-DDR; $t_{DSC} = t_{DSC}$ (MIN) NV-DDR2	I_{CC4W_S}	–	16 ²	20 ²	mA
				25 ³	30 ³	
	$t_{CK} = t_{CK}$ (MIN) NV-DDR2	I_{CC4QW_S}	–	TBD ²	TBD ²	mA
				TBD ³	TBD ³	
Bus idle current	$t_{CK} = t_{CK}$ (MIN) NV-DDR	I_{CC5_S}	–	6	10	mA
V_{PP} current (active)	During I_{CC1_S} or I_{CC2_S}	I_{PPA}	–	–	5	mA
V_{PP} current (idle)	V_{PP} is supplied and not enabled	I_{PPI}	–	–	10	μA
Standby current - V_{CC}	$CE\# = V_{CCQ} - 0.2V$; $WP\# = 0V/V_{CCQ}$	I_{SB}	–	15	75	μA
Standby Current - V_{CCQ}	$CE\# = V_{CCQ} - 0.2V$; $WP\# = 0V/V_{CCQ}$	I_{SBQ}	–	3	10	μA

Notes:

1. All values are per die (LUN) unless otherwise specified.
2. For speeds up to 200MT/s.
3. For speeds greater than 200MT/s.

Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 61: Asynchronous/NV-DDR DC Characteristics and Operating Conditions (3.3V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH(AC)}$	$0.8 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
AC input low voltage		$V_{IL(AC)}$	-0.3	–	$0.2 \times V_{CCQ}$	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#)	$V_{IH(DC)}$	$0.7 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$0.3 \times V_{CCQ}$	V	
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	± 10	μA	1
Output leakage current	DQ are disabled; $V_{OUT} = 0V$ to V_{CCQ}	I_{LO}	–	–	± 10	μA	1
Output low current (R/B#)	$V_{OL} = 0.4V$	I_{OL} (R/B#)	8	10	–	mA	2

Notes:

1. All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.
2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See (page 0) for additional details.

Table 62: Asynchronous/NV-DDR DC Characteristics and Operating Conditions (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH(AC)}$	$0.8 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
AC input low voltage		$V_{IL(AC)}$	-0.3	–	$0.2 \times V_{CCQ}$	V	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 62: Asynchronous/NV-DDR DC Characteristics and Operating Conditions (1.8V V_{CCQ}) (Continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
DC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH(DC)}$	$0.7 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$0.3 \times V_{CCQ}$	V	
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	± 10	μA	1
Output leakage current	DQ are disabled; $V_{out} = 0V$ to V_{CCQ}	I_{LO}	–	–	± 10	μA	1
Output low current (R/B#)	$V_{OL} = 0.2V$	I_{OL} (R/B#)	3	4	–	mA	2

Notes:

1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.
2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See on page for additional details.

Table 63: NV-DDR2 DC Characteristics and Operating Conditions for Single-Ended signals (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(AC)}$	$V_{REFQ} + 0.250$	–	–	V	
AC input low voltage		$V_{IL(AC)}$	–	–	$V_{REFQ} - 0.250$	V	
AC input high voltage	CE#, WP#	$V_{IH(AC)}$	$0.8 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
AC input low voltage		$V_{IL(AC)}$	-0.3	–	$0.2 \times V_{CCQ}$	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(DC)}$	$V_{REFQ} + 0.125$	–	$V_{CCQ} + 0.3$	V	2
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$V_{REFQ} - 0.125$	V	2
DC input high voltage	CE#, WP#	$V_{IH(DC)}$	$0.7 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$0.3 \times V_{CCQ}$	V	
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	± 10	μA	1
Output leakage current	DQ are disabled; $V_{out} = 0V$ to V_{CCQ}	I_{LO}	–	–	± 10	μA	1
Output low current (R/B#)	$V_{OL} = 0.2V$	I_{OL} (R/B#)	3	4	–	mA	3
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	–	± 5	μA	

Notes:

1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Configuration Operations (page 101) for additional details.

Table 64: NV-DDR2 DC Characteristics and Operating Conditions for Differential signals(1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(AC)}$	$2 \times [V_{IH(DC)} - V_{REF}]$	–	See Note	V	2
Differential AC input low voltage		$V_{ILdiff(AC)}$	See Note	–	$2 \times [V_{REF} - V_{IL(AC)}]$	V	2
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(DC)}$	$2 \times [V_{IH(DC)} - V_{REF}]$	–	See Note	V	2
Differential DC input low voltage		$V_{ILdiff(DC)}$	See Note	–	$2 \times [V_{REF} - V_{IL(DC)}]$	V	2
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	± 10	μA	1
Output leakage current	DQ are disabled; $Vout = 0V$ to V_{CCQ}	I_{LO}	–	–	± 10	μA	1
Output low current (R/B#)	$V_{OL} = 0.2V$	I_{OL} (R/B#)	3	4	–	mA	3
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	–	± 5	μA	

- Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.
 2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
 3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Configuration Operations (page 101) for additional details.

Single-Ended Requirements for Differential signals

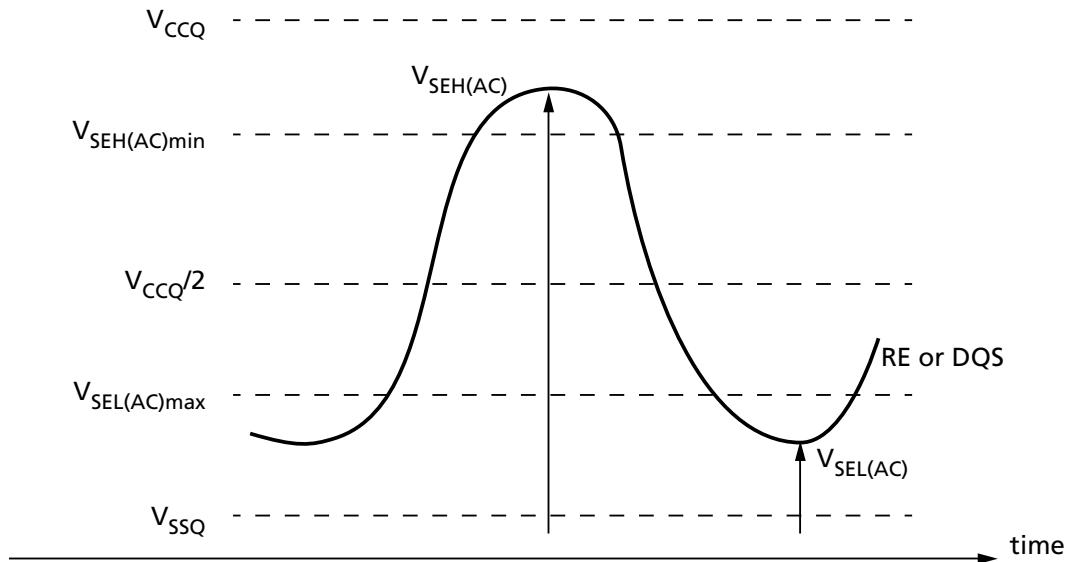
Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle preceding and following a valid transition.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Figure 94: Single-Ended requirements for Differential Signals



While control (e.g., ALE, CLE) and DQ signal requirements are with respect to V_{REFQ} , the single-ended components of differential signals have a requirement with respect to $V_{CCQ}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)}$ Max, $V_{SEH(AC)}$ Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 65: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c (1.8V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-Ended high level	$V_{SEH(AC)}$	$V_{CCQ}/2 + 0.250$	See note	V	1
Single-Ended low level	$V_{SEL(AC)}$	See note	$V_{CCQ}/2 - 0.250$	V	1

Note: 1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 66: Differential AC Input/Ouput Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to $V_{CCQ} / 2$	$V_{IX(AC)}$	$0.5 \times V_{CCQ} - 0.175$	$0.5 \times V_{CCQ} + 0.175$	V	1
AC differential output cross-point voltage	$V_{OX(AC)}$	$0.5 \times V_{CCQ} - 0.2$	$0.5 \times V_{CCQ} + 0.2$	V	2, 3, 4

Notes: 1. The typical value of $V_{IX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ} . $V_{IX(AC)}$ indicates the voltage at which differential input signals shall cross.
 2. The typical value of $V_{OX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ} . $V_{OX(AC)}$ indicates the voltage at which differential output signals shall cross.
 3. $V_{OX(AC)}$ is measured with $\frac{1}{2}$ DQ signals per data byte driving logic HIGH and $\frac{1}{2}$ DQ signals per data byte driving logic LOW.



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

4. $V_{OX(AC)}$ is verified by design and characterization; it may not be subject to production testing.

Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 67: AC Characteristics: Asynchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max												
Clock period		100		50		35		30		25		20		ns	
Frequency		\approx 10		\approx 20		\approx 28		\approx 33		\approx 40		\approx 50		MHz	
ALE to data start	t_{ADL}	200	–	100	–	100	–	100	–	70	–	70	–	ns	1
ALE hold time	t_{ALH}	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	t_{ALS}	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	t_{AR}	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	t_{CEA}	–	100	–	45	–	30	–	25	–	25	–	25	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	t_{CEH}	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CE# hold time	t_{CH}	20	–	10	–	10	–	5	–	5	–	5	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	t_{CEVDLY}	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# HIGH to output High-Z	t_{CHZ}	–	100	–	50	–	50	–	50	–	30	–	30	ns	2
CLE hold time	t_{CLH}	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	t_{CLR}	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	t_{CLS}	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# HIGH to output hold	t_{COH}	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	t_{CS}	70	–	35	–	25	–	25	–	20	–	15	–	ns	
Data hold time	t_{DH}	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	t_{DS}	40	–	20	–	15	–	10	–	10	–	7	–	ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENO}	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Output High-Z to RE# LOW	t_{IR}	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	t_{RC}	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	t_{REA}	–	40	–	30	–	25	–	20	–	20	–	16	ns	3

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 67: AC Characteristics: Asynchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max												
RE# HIGH hold time	t_{REH}	30	–	15	–	15	–	10	–	10	–	7	–	ns	3
RE# HIGH to output hold	t_{RHOH}	0	–	15	–	15	–	15	–	15	–	15	–	ns	3
RE# HIGH to WE# LOW	t_{RHW}	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# HIGH to output High-Z	t_{RHZ}	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# LOW to output hold	t_{RLOH}	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	t_{RP}	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# LOW	t_{RR}	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t_{WB}	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	t_{WC}	100	–	45	–	35	–	30	–	25	–	20	–	ns	
WE# HIGH hold time	t_{WH}	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# HIGH to RE# LOW	t_{WHR}	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	t_{WP}	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to WE# LOW	t_{WW}	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	t_{VDLY}	50	–	50	–	50	–	50	–	50	–	50	–	ns	

- Notes:
1. Timing for t_{ADL} begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input.
 2. Data transition is measured $\pm 200\text{mV}$ from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
 3. AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
 4. Do not issue a new command during t_{WB} , even if R/B# or RDY is ready.

Release: 3/26/13



**128Gb to 1Tb Asynchronous/Synchronous NAND
Electrical Specifications – AC Characteristics and Operating
Conditions (NV-DDR and NV-DDR2)**

Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 68: AC Characteristics: NV-DDR Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		50		30		20		15		12		10		ns	
Frequency		≈20		≈33		≈50		≈67		≈83		≈100		MHz	
Access window of DQ[7:0] from CLK	^t AC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data loading time	^t ADL	100	–	100	–	70	–	70	–	70	–	70	–	ns	
Command, address data delay	^t CAD	25	–	25	–	25	–	25	–	25	–	25	–	ns	1
DQ hold – command, address	^t CAH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# hold	^t CALH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# setup	^t CALS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ setup – command, address	^t CAS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^t CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^t CEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	^t CH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
Average CLK cycle time	^t CK (avg)	50	100	30	50	20	30	15	20	12	15	10	12	ns	2
Absolute CLK cycle time, from rising edge to rising edge	^t CK (abs)	$\text{tCK (abs) MIN} = \text{tCK (avg)} + \text{tJIT (per) MIN}$ $\text{tCK (abs) MAX} = \text{tCK (avg)} + \text{tJIT (per) MAX}$												ns	
CLK cycle HIGH	^t CKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^t CK	3
CLK cycle LOW	^t CKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^t CK	3

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 68: AC Characteristics: NV-DDR Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data output end to W/R# HIGH	t_{CKWR}	$t_{CKWR}(\text{MIN}) = \text{RoundUp}[(t_{DQSCK}(\text{MAX}) + t_{CK})/t_{CK}]$												t_{CK}	
CE# setup	t_{CS}	35	–	25	–	15	–	15	–	15	–	15	–	ns	
Data In hold	t_{DH}	5	–	2.5	–	1.7	–	1.3	–	1.1	–	0.9	–	ns	
Access window of DQS from CLK	t_{DQSCK}	–	20	–	20	–	20	–	20	–	20	–	20	ns	
DQS, DQ[7:0] Driven by NAND	t_{DQSD}	–	18	–	18	–	18	–	18	–	18	–	18	ns	
DQS, DQ[7:0] to tri-state	t_{DQSHZ}	–	20	–	20	–	20	–	20	–	20	–	20	ns	4
DQS input high pulse width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS input low pulse width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS-DQ skew	t_{DQSQ}	–	5	–	2.5	–	1.7	–	1.3	–	1.0	–	0.85	ns	
Data input	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data In setup	t_{DS}	5	–	3	–	2	–	1.5	–	1.1	–	0.9	–	ns	
DQS falling edge from CLK rising – hold	t_{DSH}	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	t_{CK}	
DQS falling to CLK rising – set-up	t_{DSS}	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	t_{CK}	
Data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$												ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Half clock period	t_{HP}	$t_{HP} = \text{Min}(t_{CKH}, t_{CKL})$												ns	
The deviation of a given t_{CK} (abs) from a t_{CK} (avg)	$t_{JIT}(\text{per})$	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	-0.5	0.5	ns	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 68: AC Characteristics: NV-DDR Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^t QH	${\sup t}QH = {\sup t}HP - {\sup t}QHS$												ns	
Data hold skew factor	^t QHS	-	6	-	3	-	2	-	1.5	-	1.2	-	1	ns	
Data output to command, address, or data input	^t RHW	100	-	100	-	100	-	100	-	100	-	100	-	ns	
Ready to data output	^t RR	20	-	20	-	20	-	20	-	20	-	20	-	ns	
CLK HIGH to R/B# LOW	^t WB	-	100	-	100	-	100	-	100	-	100	-	100	ns	
Command cycle to data output	^t WHR	80	-	80	-	80	-	80	-	80	-	80	-	ns	
DQS write preamble	^t WPRE	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	^t CK	
DQS write post-preamble	^t WPST	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	^t CK	
W/R# LOW to data output cycle	^t WRCK	20	-	20	-	20	-	20	-	20	-	20	-	ns	
WP# transition to command cycle	^t WW	100	-	100	-	100	-	100	-	100	-	100	-	ns	
Delay before next command after a Volume is selected	^t VDLY	50	-	50	-	50	-	50	-	50	-	50	-	ns	

- Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
 2. ^tCK(avg) is the average clock period over any consecutive 200-cycle window.
 3. ^tCKH(abs) and ^tCKL(abs) include static offset and duty cycle jitter.
 4. ^tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
 5. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5μs.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 69: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0 - 4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max										
Clock period		30		25		15		12		10		ns	
Frequency		≈33		≈40		≈66		≈83		≈100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# LOW or RE_t / RE_c	t_{AC}	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data loading time	t_{ADL}	100	–	100	–	100	–	100	–	70	–	ns	
ALE to RE# LOW or RE_t / RE_c	t_{AR}	10	–	10	–	10	–	10	–	10	–	ns	
DQ hold – command, address	t_{CAH}	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	t_{CALH}	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	t_{CALS}	15	–	15	–	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	t_{CALS2}	25	–	25	–	25	–	25	–	25	–	ns	
DQ setup – command, address	t_{CAS}	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	t_{CEH}	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	t_{CEVDLY}	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	t_{CH}	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH to output Hi-Z	t_{CHZ}	–	30	–	30	–	30	–	30	–	30	ns	1
CLE HIGH to output Hi-Z	t_{CLHZ}	–	30	–	30	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t / RE_c	t_{CLR}	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c	t_{CR}	10	–	10	–	10	–	10	–	10	–	ns	
CE# setup	t_{CS}	20	–	20	–	20	–	20	–	20	–	ns	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 69: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max										
CE# setup for data output with ODT disabled	^t CS1	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	^t CS2	40	–	40	–	40	–	40	–	40	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^t CSD	10	–	10	–	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	^t ENi	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	^t ENo	–	50	–	50	–	50	–	50	–	50	ns	
Ready to data output	^t RR	20	–	20	–	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	^t WB	–	100	–	100	–	100	–	100	–	100	ns	
WE# cycle time	^t WC	25	–	25	–	25	–	25	–	25	–	ns	
WE# pulse width	^t WH	11	–	11	–	11	–	11	–	11	–	ns	
Command cycle to data output	^t WHR	80	–	80	–	80	–	80	–	80	–	ns	
WP# transition to command cycle	^t WP	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to command cycle	^t WW	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^t VDLY	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													
The deviation of a given ^t DQS (abs) / ^t DSC (abs) from a ^t DQS (avg) / ^t DSC (avg)	^t JITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	-0.8	0.8	ns	3, 5, 7

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 69: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
The deviation of a given t_{RC} (abs) / t_{DSC} (abs) from a t_{RC} (avg) / t_{DSC} (avg)	t_{JITper} (RE#)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	-0.6	0.6	ns	3, 5, 7
Cycle to cycle jitter for DQS	t_{JITcc} (DQS)	4.8	–	4.0	–	2.4	–	2.0	–	1.6	–	ns	3, 6
Cycle to cycle jitter for RE#	t_{JITcc} (RE#)	3.6	–	3.0	–	1.8	–	1.5	–	1.2	–	ns	3, 6
Data Input													
DQS setup time for data input start	t_{CDQSS}	30	–	30	–	30	–	30	–	30	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH set-up to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	5	–	5	–	ns	
Data In hold	t_{DH}	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
Data In setup	t_{DS}	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
DQS input high pulse width	t_{DQSH}	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	t_{DSC} (avg)	
DQS input low pulse width	t_{DQL}	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	t_{DSC} (avg)	
Average DQS cycle time	t_{DSC} (avg) or t_{DSC}	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	t_{DSC} (abs)	t_{DSC} (abs) MIN = t_{DSC} (avg) + t_{JITper} (DQS) MIN t_{DSC} (abs) MAX = t_{DSC} (avg) + t_{JITper} (DQS) MAX		t_{DSC} (abs) MIN = t_{DSC} (avg) + t_{JITper} (DQS) MIN t_{DSC} (abs) MAX = t_{DSC} (avg) + t_{JITper} (DQS) MAX								ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENO}	–	50	–	50	–	50	–	50	–	50	ns	

Release: 3/26/13



**128Gb to 1Tb Asynchronous/Synchronous NAND
Electrical Specifications – AC Characteristics and Operating
Conditions (NV-DDR and NV-DDR2)**

Table 69: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS write pre-amble with ODT disabled	t_{WPRE}	15	–	15	–	15	–	15	–	15	–	ns	
DQS write pre-amble with ODT enabled	t_{WPRE2}	25	–	25	–	25	–	25	–	25	–	ns	
DQS write post-amble	t_{WPST}	6.5	–	6.5	–	6.5	–	6.5	–	6.5	–	ns	
DQS write post-amble hold time	t_{WPSTH}	5	–	5	–	5	–	5	–	5	–	ns	
Data Output													
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH set-up to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	5	–	5	–	ns	
DQS-DQ skew	t_{DQSQ}	–	2.5	–	2.0	–	1.4	–	1.0	–	0.8	ns	
Access window of DQS from RE# or RE_t / RE_c	t_{DQSRE}	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	t_{DQSD}	5	18	5	18	5	18	5	18	5	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	t_{DQSRH}	5	–	5	–	5	–	5	–	5	–	ns	
Data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$								$t_{DVW} = t_{QH} - t_{DQSQ}$		ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t_{QH}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	t_{RC} (avg)	9
DQS (DQS_t / DQS_c) output HIGH time	t_{QSH}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	t_{RC} (avg)	9

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 69: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS (DQS_t / DQS_c) output LOW time	t_{QSL}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	t_{RC} (avg)	9
Average RE# cycle time	t_{RC} (avg) or t_{RC}	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute RE# cycle time	t_{RC} (abs)	t_{RC} (abs) MIN = t_{RC} (avg) + $t_{JITper(RE\#)}$ MIN t_{RC} (abs) MAX = t_{RC} (avg) + $t_{JITper(RE\#)}$ MAX								t_{RC} (abs) MIN = t_{RC} (avg) + $t_{JITper(RE\#)}$ MIN t_{RC} (abs) MAX = t_{RC} (avg) + $t_{JITper(RE\#)}$ MAX		ns	
Average RE# HIGH hold time	t_{REH} (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (avg)	4
Absolute RE# HIGH hold time	t_{REH} (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	t_{RC} (avg)	
Data output to command, address, or data input	t_{RHW}	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	t_{RP} (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (avg)	4
Average RE# pulse width	t_{RP} (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (avg)	4
Absolute RE# pulse width	t_{RP} (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	t_{RC} (avg)	
Read preamble with ODT disabled	t_{RPRE}	15	–	15	–	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	t_{RPRE2}	25	–	25	–	25	–	25	–	25	–	ns	
Read postamble	t_{RPST}	t_{DQS} RE + 0.5 * t_{RC}	–	t_{DQS} RE + 0.5 * t_{RC}	–	t_{DQS} RE + 0.5 * t_{RC}	–	t_{DQS} RE + 0.5 * t_{RC}	–	t_{DQS} RE + 0.5 * t_{RC}	–	ns	
Read postable hold time	t_{RPSTH}	5	–	5	–	5	–	5	–	5	–	ns	

Notes: 1. t_{CHZ} and t_{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

2. The parameters $t_{RC}(\text{avg})$ and $t_{DSC}(\text{avg})$ are the average over any 200 consecutive periods and $t_{RC}(\text{avg}) / t_{DSC}(\text{avg})$ min are the smallest rates allowed, with the exception of a deviation due to t_{JIT} (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. $t_{REH}(\text{avg})$ and $t_{RP}(\text{avg})$ are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter t_{JIT} (per) is the maximum deviation in the t_{RC} or t_{DSC} period from the average or nominal t_{RC} or t_{DSC} period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t_{JITper} . As long as the absolute minimum half period ($t_{RP}(\text{abs})$, $t_{REH}(\text{abs})$, t_{DQSH} or t_{DQL}) is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual t_{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The t_{DS} and t_{DH} times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.

Table 70: AC Characteristics: NV-DDR2 Command, Address, and Data for timing modes 5 - 7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		7.5		6		5		ns	
Frequency		≈ 133		≈ 166		≈ 200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t / RE_c	t_{AC}	3	25	3	25	3	25	ns	
ALE to data loading time	t_{ADL}	70	–	70	–	70	–	ns	
ALE to RE# LOW or RE_t / RE_c	t_{AR}	10	–	10	–	10	–	ns	
DQ hold – command, address	t_{CAH}	5	–	5	–	5	–	ns	
ALE, CLE hold	t_{CALH}	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	t_{CALS}	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	t_{CALS2}	25	–	25	–	25	–	ns	
DQ setup – command, address	t_{CAS}	5	–	5	–	5	–	ns	
CE# HIGH hold time	t_{CEH}	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	t_{CEVDLY}	50	–	50	–	50	–	ns	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 70: AC Characteristics: NV-DDR2 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CE# hold	t_{CH}	5	–	5	–	5	–	ns	
CE# HIGH to output Hi-Z	t_{CHZ}	–	30	–	30	–	30	ns	1
CLE HIGH to output Hi-Z	t_{CLHZ}	–	30	–	30	–	30		1
CLE to RE# LOW or RE_t / RE_c	t_{CLR}	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c	t_{CR}	10	–	10	–	10	–	ns	
CE# setup	t_{CS}	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	t_{CS1}	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	t_{CS2}	40	–	40	–	40	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	t_{CSD}	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	t_{ENO}	–	50	–	50	–	50	ns	
Ready to data output	t_{RR}	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	t_{WB}	–	100	–	100	–	100	ns	
WE# cycle time	t_{WC}	25	–	25	–	25	–	ns	
WE# pulse width	t_{WH}	11	–	11	–	11	–	ns	
Command cycle to data output	t_{WHR}	80	–	80	–	80	–	ns	
WP# transition to command cycle	t_{WP}	11	–	11	–	11	–	ns	
WP# transition to command cycle	t_{WW}	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	t_{VDLY}	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given t_{DQS} (abs) / t_{DSC} (abs) from a t_{DQS} (avg) / t_{DSC} (avg)	t_{JITper} (DQS)	-0.6	0.6	-0.48	0.48	-0.40	0.40	ns	3, 5, 7

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 70: AC Characteristics: NV-DDR2 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
The deviation of a given t_{RC} (abs) / t_{DSC} (abs) from a t_{RC} (avg) / t_{DSC} (avg)	t_{JITper} (RE#)	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns	3, 5, 7
Cycle to cycle jitter for DQS	t_{JITcc} (DQS)	1.2	–	0.96	–	0.80	–	ns	3, 6
Cycle to cycle jitter for RE#	t_{JITcc} (RE#)	0.9	–	0.72	–	0.60	–	ns	3, 6
Data Input									
DQS setup time for data input start	t_{CDQSS}	30	–	30	–	30	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	ns	
Data In hold	t_{DH}	0.6	–	0.55	–	0.40	–	ns	10
Data In setup	t_{DS}	0.6	–	0.55	–	0.40	–	ns	10
DQS input high pulse width	t_{DQSH}	0.43	–	0.43	–	0.43	–	t_{DSC} (avg)	
DQS input low pulse width	t_{DQLS}	0.43	–	0.43	–	0.43	–	t_{DSC} (avg)	
Average DQS cycle time	t_{DSC} (avg) or t_{DSC}	7.5	–	6	–	5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	t_{DSC} (abs)	t_{DSC} (abs) MIN = t_{DSC} (avg) + t_{JITper} (DQS) MIN t_{DSC} (abs) MAX = t_{DSC} (avg) + t_{JITper} (DQS) MAX						ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	t_{ENO}	–	50	–	50	–	50	ns	
DQS write preamble with ODT disabled	t_{WPRE}	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	t_{WPRE2}	25	–	25	–	25	–	ns	
DQS write postamble	t_{WPST}	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	t_{WPSTH}	5	–	5	–	5	–	ns	
Data Output									
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	3	25	ns	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 70: AC Characteristics: NV-DDR2 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^t DBS	5	–	5	–	5	–	ns	
DQS-DQ skew	^t DQSQ	–	0.6	–	0.5	–	0.4	ns	
Access window of DQS from RE# or RE_t / RE_c	^t DQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^t DQSD	5	18	5	18	5	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	^t DQSRH	5	–	5	–	5	–	ns	
Data valid window	^t DVW	$\text{tDVW} = \text{tQH} - \text{tDQSQ}$						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^t QH	0.37	–	0.37	–	0.37	–	^t RC (avg)	9
DQS (DQS_t / DQS_c) output HIGH time	^t QSH	0.37	–	0.37	–	0.37	–	^t RC (avg)	9
DQS (DQS_t / DQS_c) output LOW time	^t QSL	0.37	–	0.37	–	0.37	–	^t RC (avg)	9
Average RE# cycle time	^t RC (avg) or ^t RC	7.5	–	6	–	5	–	ns	2
Absolute RE# cycle time	^t RC (abs)	$\begin{aligned} \text{tRC (abs) MIN} &= \text{tRC (avg)} + \text{tJITper(Re#) MIN} \\ \text{tRC (abs) MAX} &= \text{tRC (avg)} + \text{tJITper(Re#) MAX} \end{aligned}$						ns	
Average RE# HIGH hold time	^t REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^t RC (avg)	4
Absolute RE# HIGH hold time	^t REH (abs)	0.43	–	0.43	–	0.43	–	^t RC (avg)	
Data output to command, address, or data input	^t RHW	100	–	100	–	100	–	ns	
Average RE# pulse width	^t RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	^t RC (avg)	4
Absolute RE# pulse width	^t RP (abs)	0.43	–	0.43	–	0.43	–	^t RC (avg)	
Read preamble with ODT disabled	^t RPRE	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	^t RPRE2	25	–	25	–	25	–	ns	
Read postamble	^t RPST	^t DQSRE + 0.5 * ^t RC	–	^t DQSRE + 0.5 * ^t RC	–	^t DQSRE + 0.5 * ^t RC	–	ns	

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR and NV-DDR2)

Table 70: AC Characteristics: NV-DDR2 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read postable hold time	t_{RPSTH}	5	-	5	-	5	-	ns	

- Notes:
1. t_{CHZ} and t_{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.
 2. The parameters $t_{RC}(\text{avg})$ and $t_{DSC}(\text{avg})$ are the average over any 200 consecutive periods and $t_{RC}(\text{avg}) / t_{DSC}(\text{avg})$ min are the smallest rates allowed, with the exception of a deviation due to t_{JIT} (per).
 3. Input jitter is allowed provided it does not exceed values specified.
 4. $t_{REH}(\text{avg})$ and $t_{RP}(\text{avg})$ are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
 5. The period jitter t_{JIT} (per) is the maximum deviation in the t_{RC} or t_{DSC} period from the average or nominal t_{RC} or t_{DSC} period. It is allowed in either the positive or negative direction.
 6. The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next.
 7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t_{JITper} . As long as the absolute minimum half period ($t_{RP}(\text{abs})$, $t_{REH}(\text{abs})$, t_{DQSH} or t_{DQL}) is not less than 43 percent of the average cycle.
 8. All timing parameter values assume differential signaling for RE# and DQS is used.
 9. When the device is operated with input clock jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual t_{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
 10. The t_{DS} and t_{DH} times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.

Release: 3/26/13



Electrical Specifications – Array Characteristics

Table 71: Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	t_{BERS}	3	12	ms	
Cache busy	t_{CBSY}	1100	3000	μs	
Change column setup time to data in/out or next command	t_{CCS}	–	300	ns	
Dummy busy time	t_{DBSY}	0.5	1	μs	
Busy time for SET FEATURES and GET FEATURES operations	t_{FEAT}	–	1	μs	
Busy time for interface change	t_{ITC}	–	1	μs	2
LAST PAGE PROGRAM operation time	t_{LPROG}	–	–	μs	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	t_{OBSY}	–	50	μs	
Power-on reset time	t_{POR}	–	2	ms	
PROGRAM PAGE operation time	t_{PROG}	1600	3000	μs	
READ PAGE operation time	t_R	–	115	μs	5
Cache read busy time	t_{RCBSY}	26	115	μs	6
Device reset time (Read/Program/Erase)	t_{RST}	–	5/10/500	μs	4

- Notes:
1. The pages in the OTP Block have an NOP of 2.
 2. t_{ITC} (MAX) is the busy time when the interface changes from asynchronous to synchronous using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the t_{ITC} time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.
 3. $t_{LPROG} = t_{PROG}$ (last page) + t_{PROG} (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
 4. If RESET command is issued when the target is READY, the target goes busy for a maximum of 5 μs .
 5. For Read Retry options 4 to 7, t_R Max may be up to 285 μs .
 6. For Read Retry options 4 to 7, Cache read is not supported.

Release: 3/26/13



Asynchronous Interface Timing Diagrams

Figure 95: RESET Operation

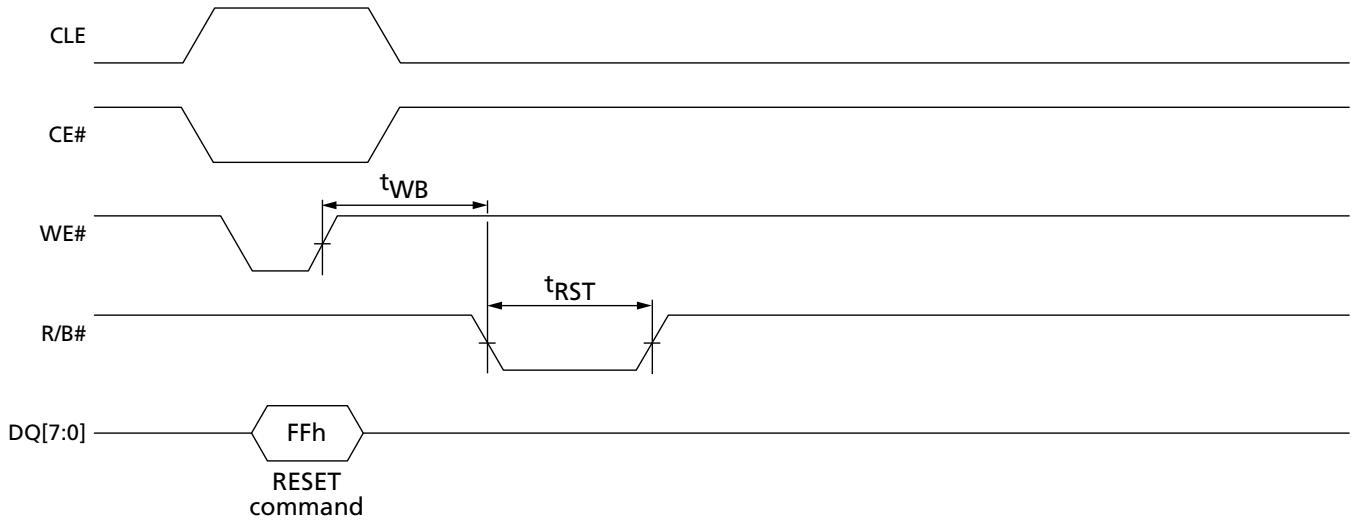
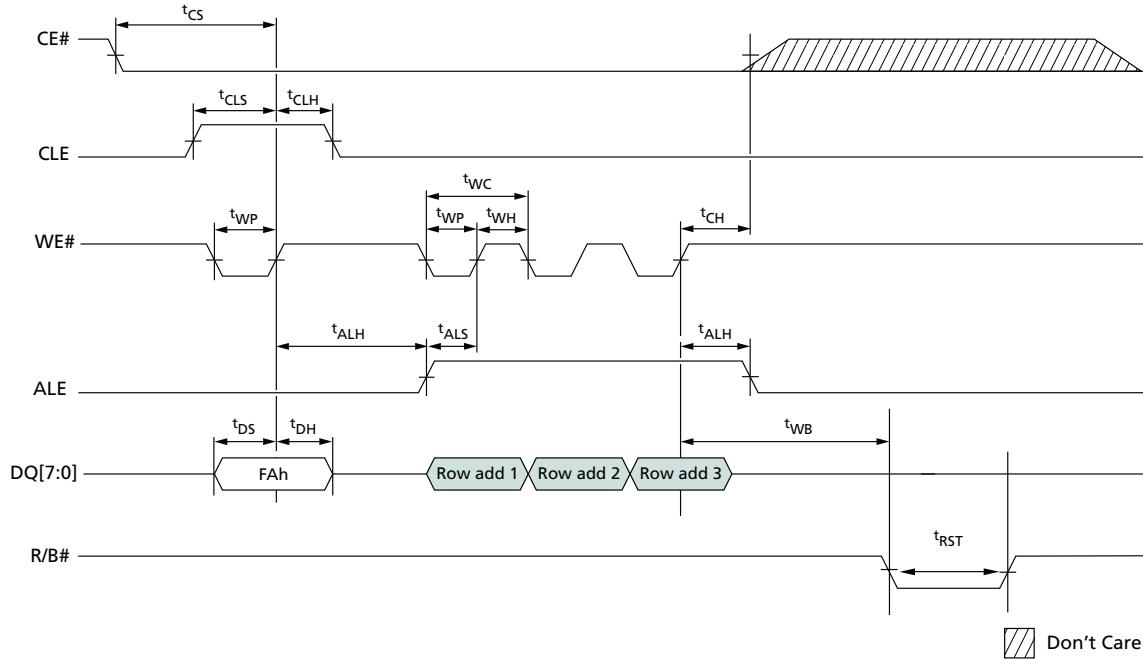


Figure 96: RESET LUN Operation



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 97: READ STATUS Cycle

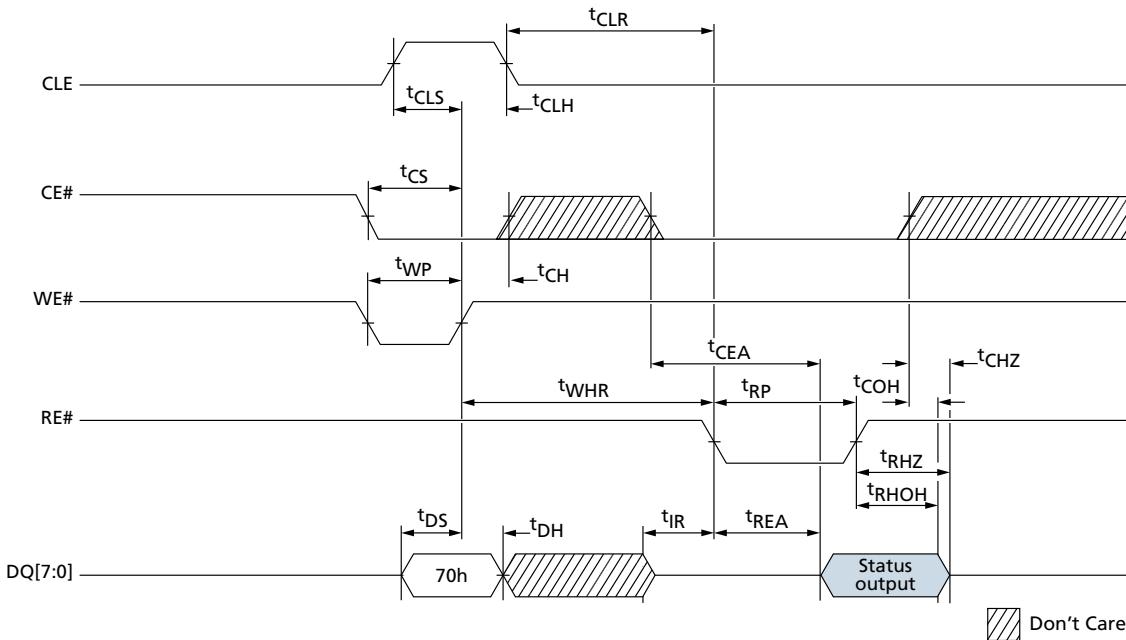
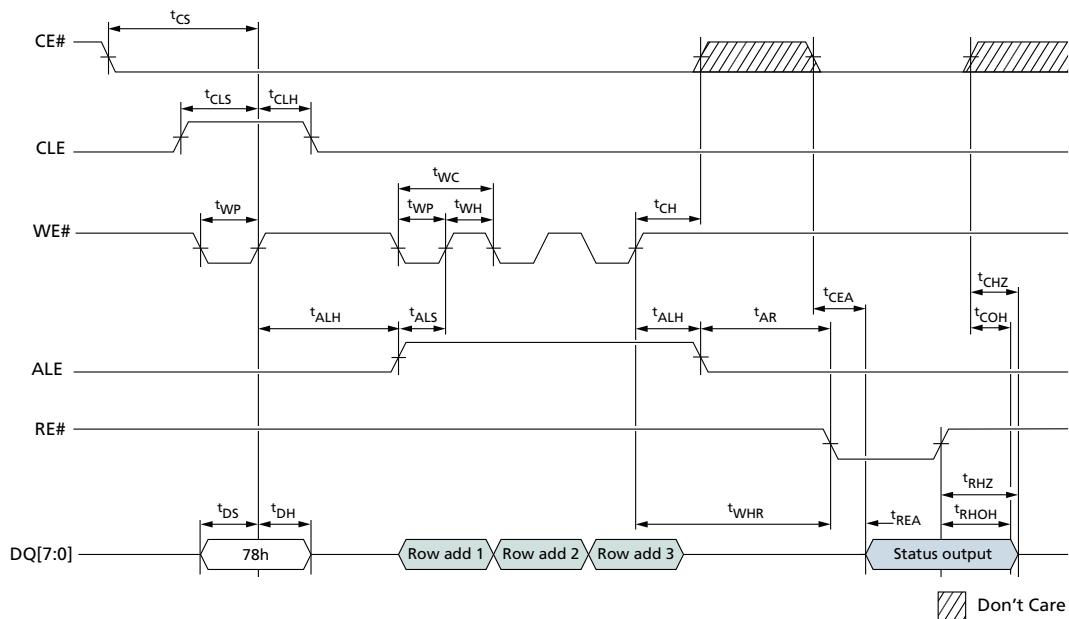


Figure 98: READ STATUS ENHANCED Cycle



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 99: READ PARAMETER PAGE

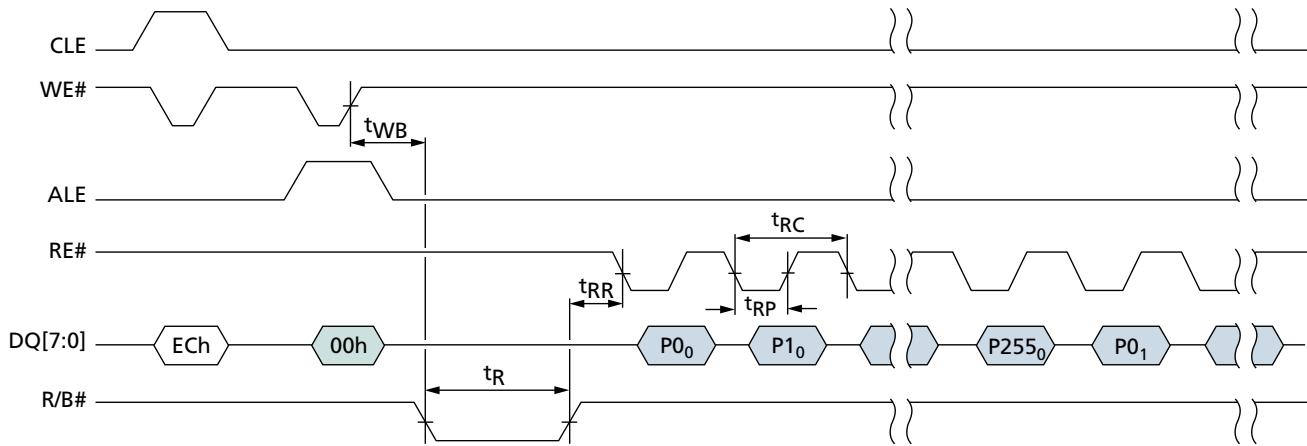
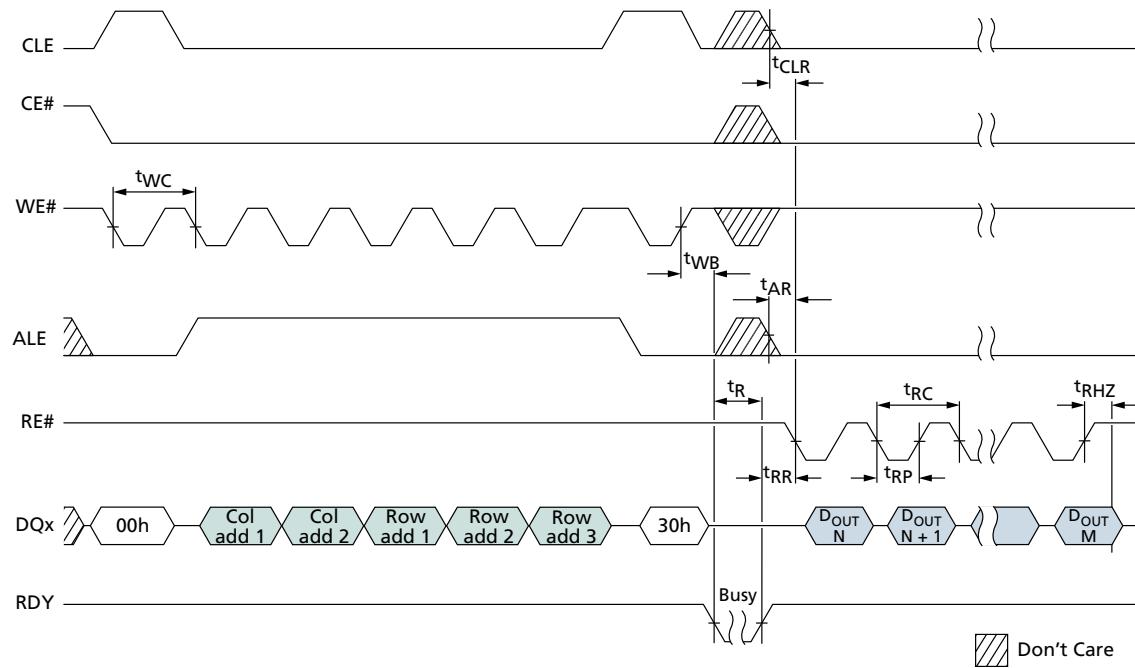


Figure 100: READ PAGE

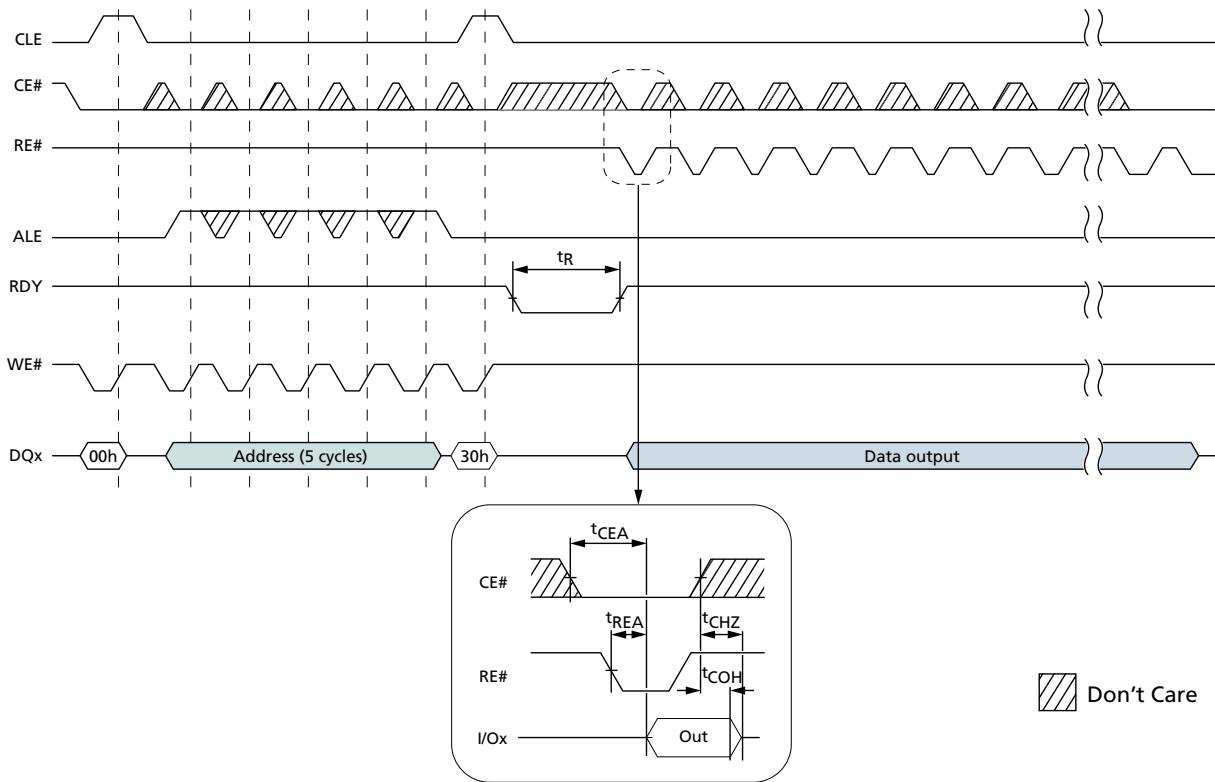


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 101: READ PAGE Operation with CE# “Don’t Care”

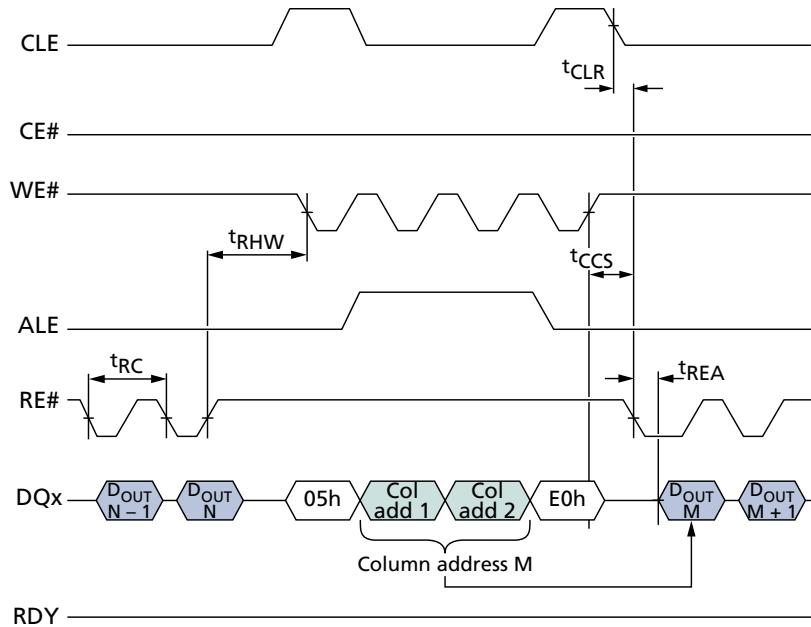


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 102: CHANGE READ COLUMN

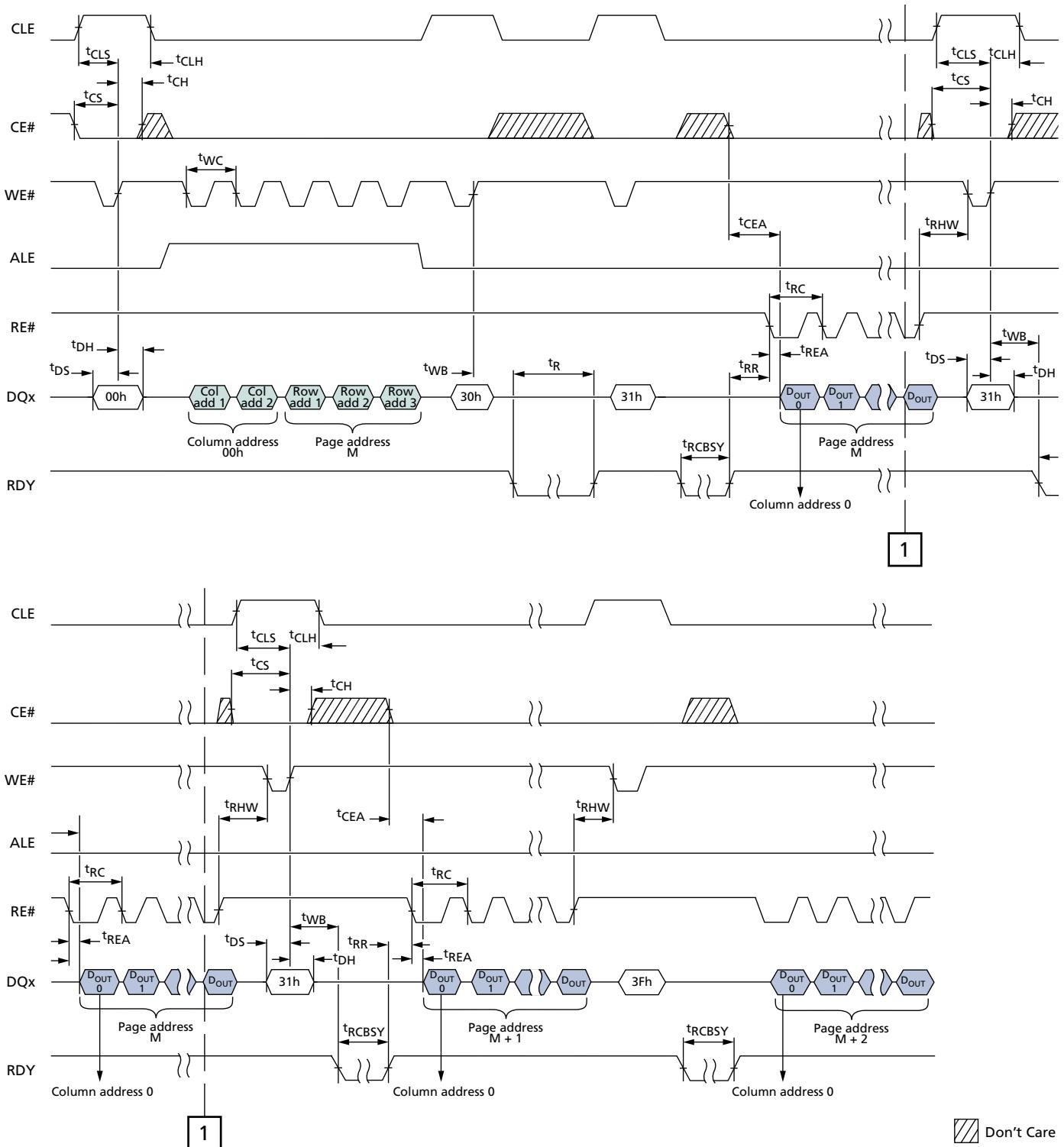


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 103: READ PAGE CACHE SEQUENTIAL

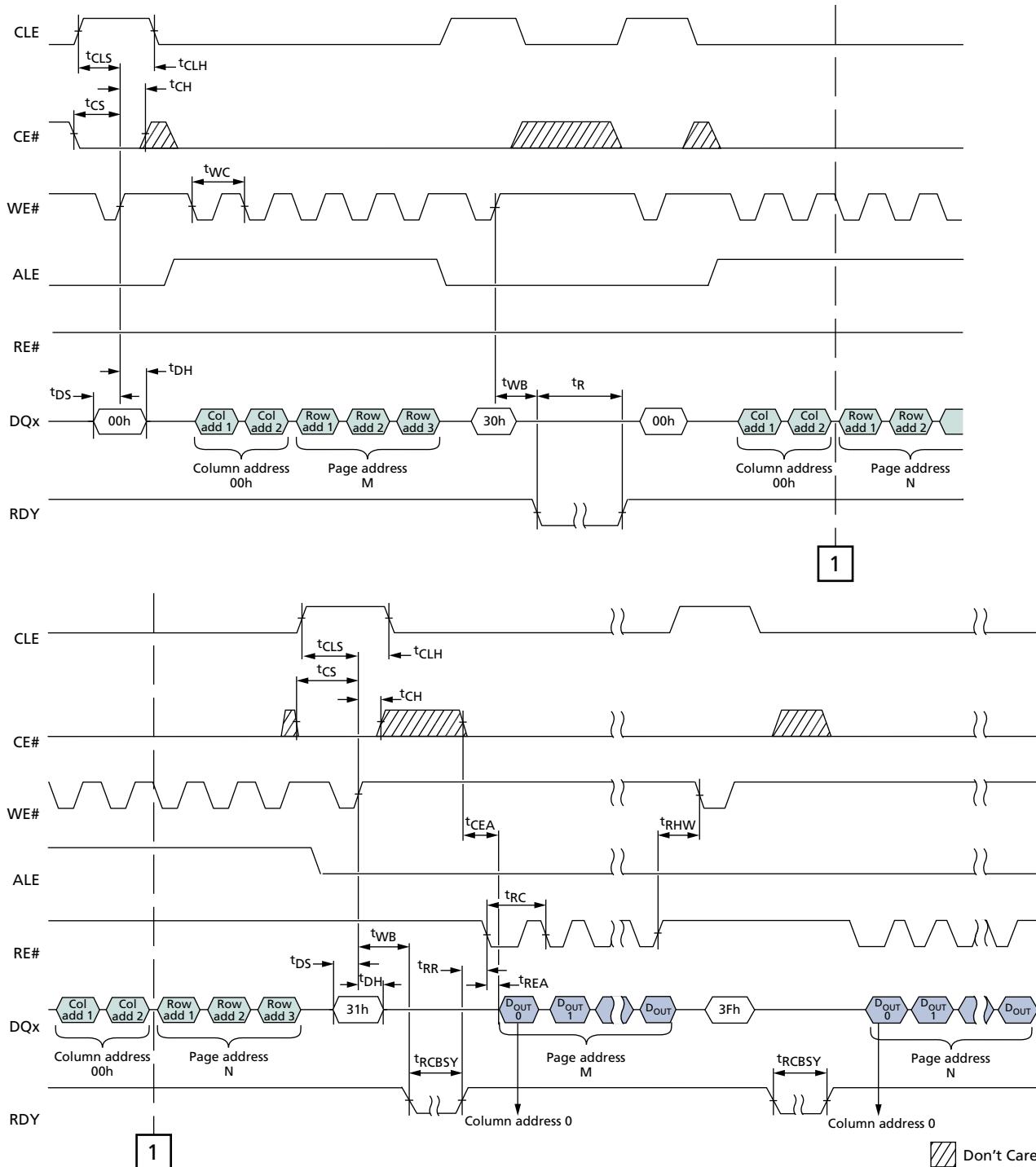


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 104: READ PAGE CACHE RANDOM



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 105: READ ID Operation

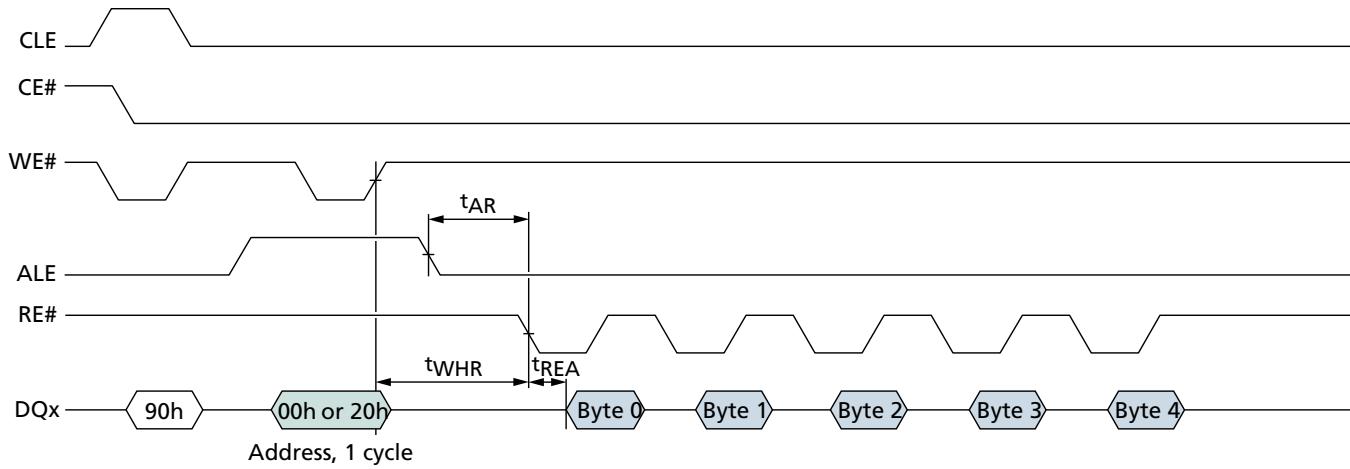
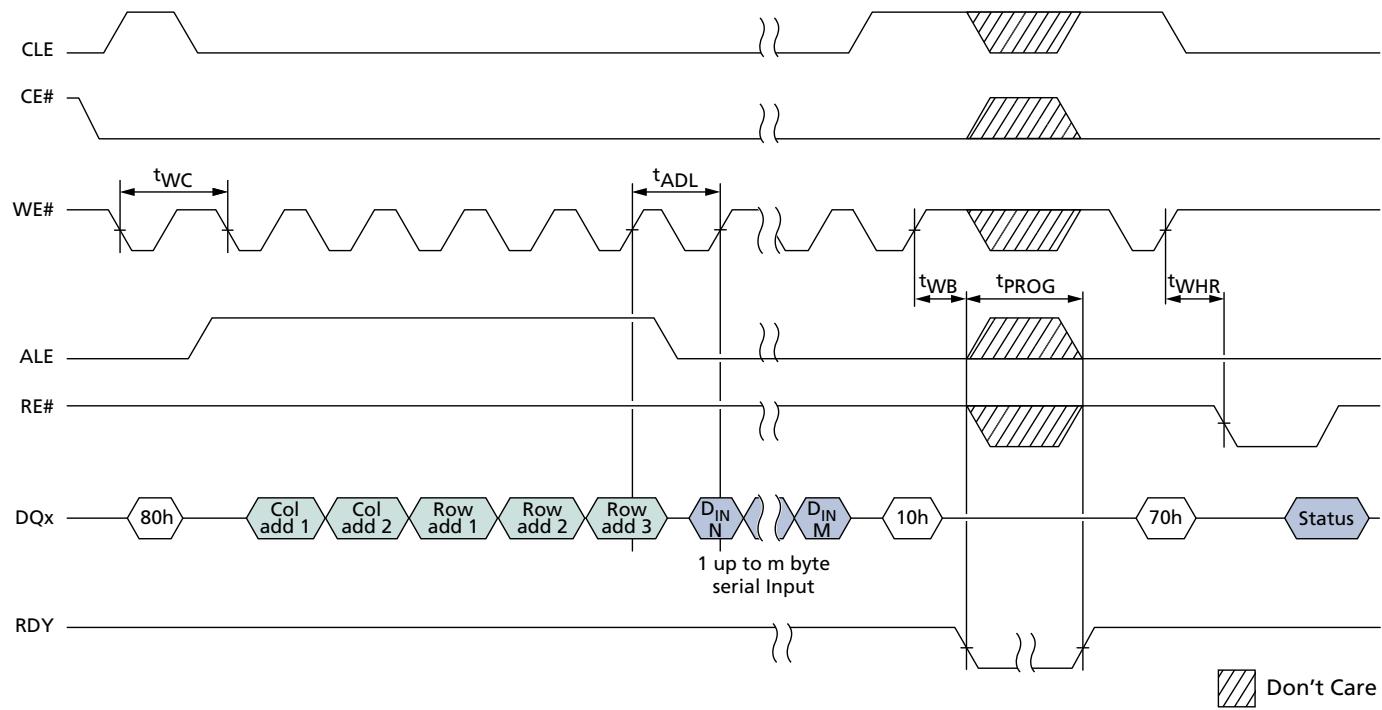


Figure 106: PROGRAM PAGE Operation



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 107: PROGRAM PAGE Operation with CE# “Don’t Care”

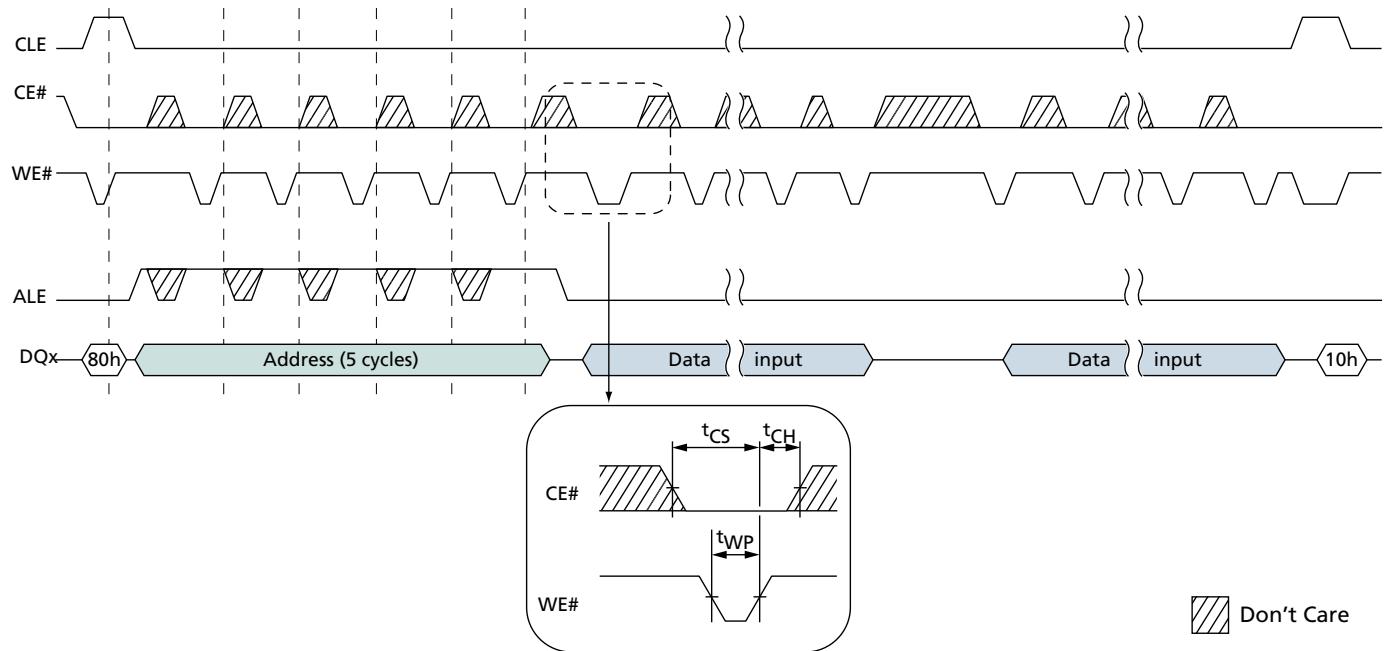
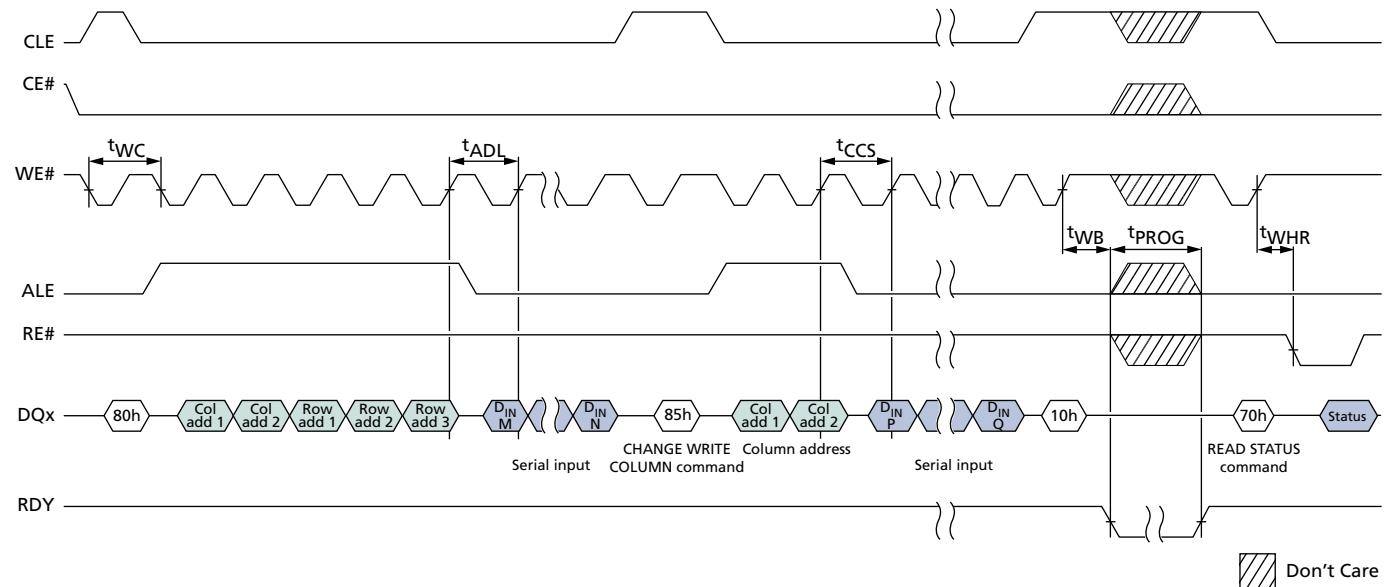


Figure 108: PROGRAM PAGE Operation with CHANGE WRITE COLUMN



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 109: PROGRAM PAGE CACHE

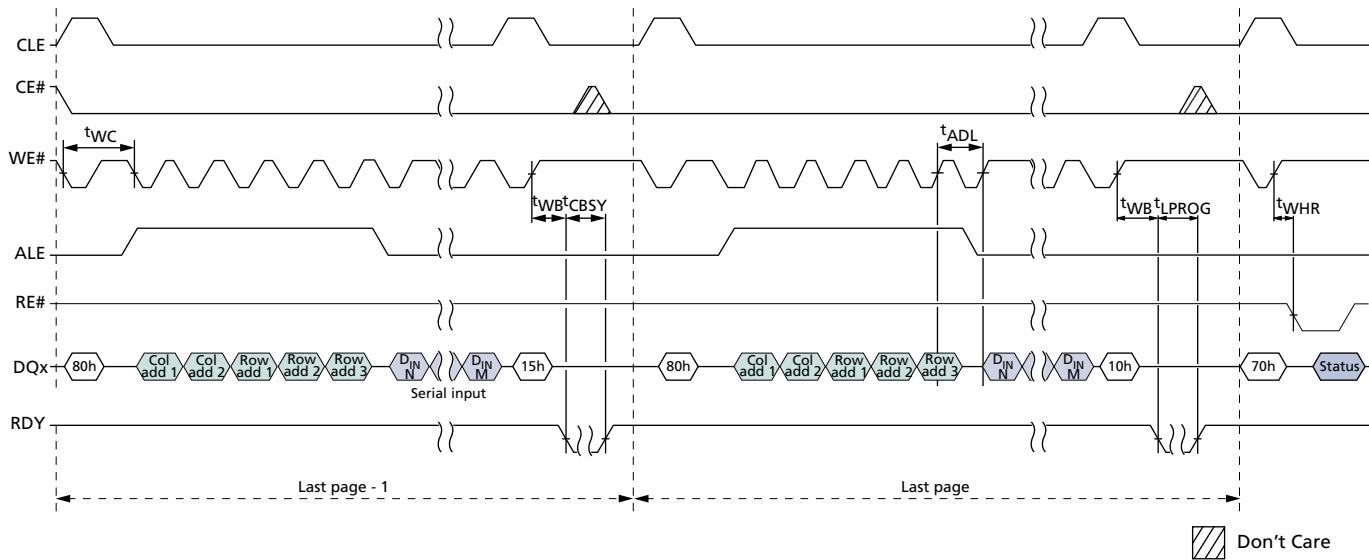
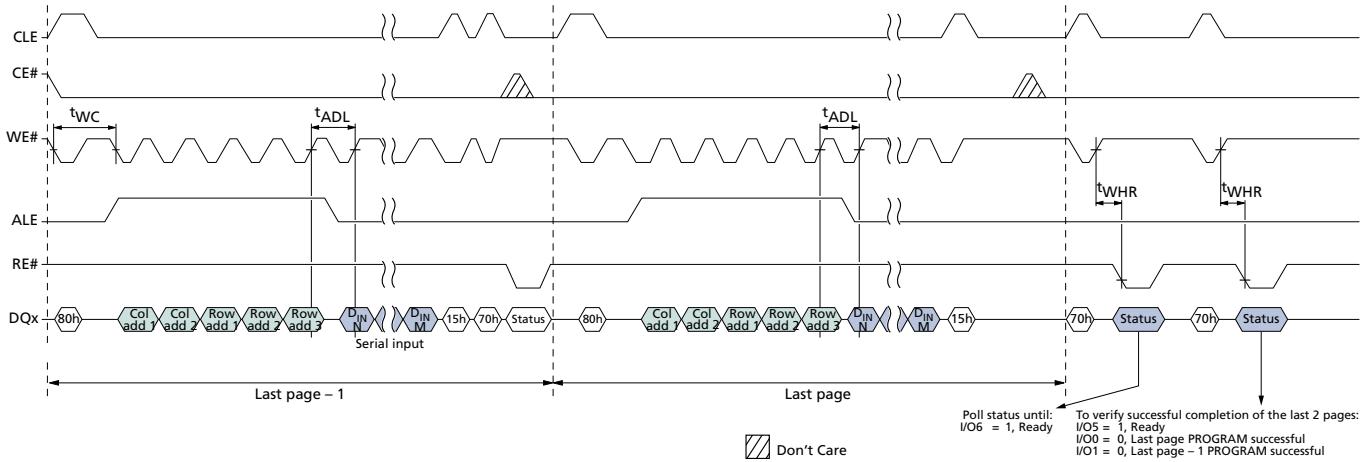


Figure 110: PROGRAM PAGE CACHE Ending on 15h



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND Asynchronous Interface Timing Diagrams

Figure 111: COPYBACK

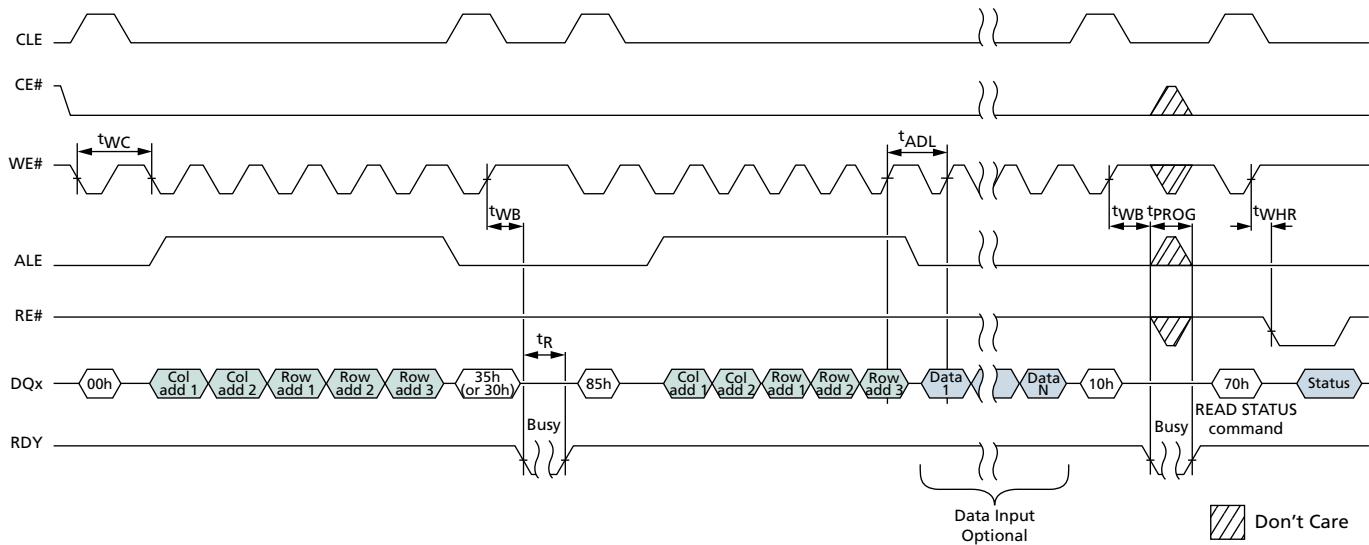
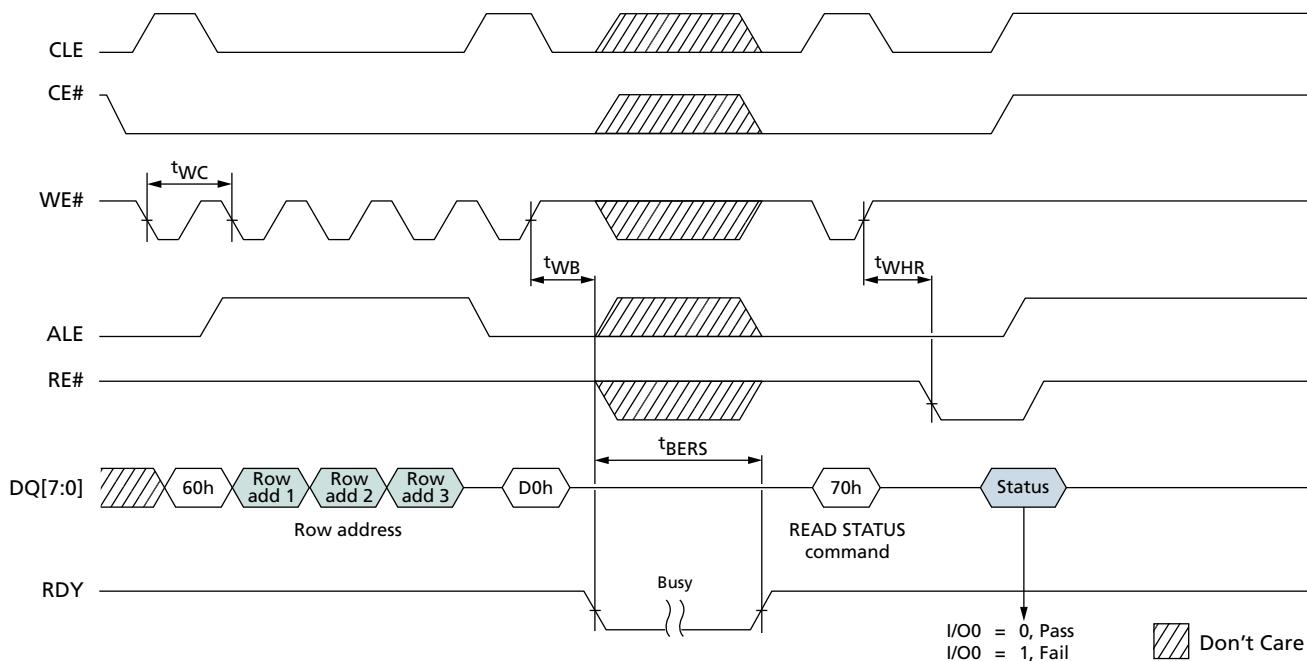


Figure 112: ERASE BLOCK Operation

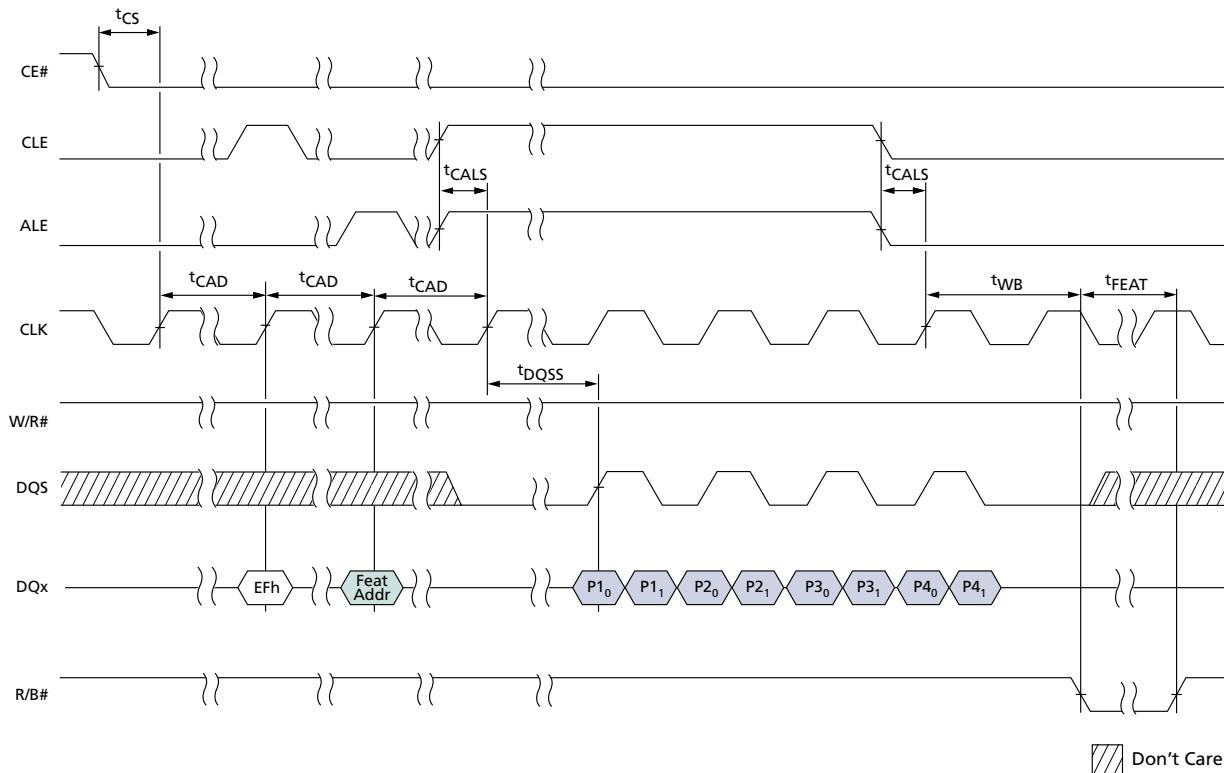


Release: 3/26/13



NV-DDR Interface Timing Diagrams

Figure 113: SET FEATURES Operation



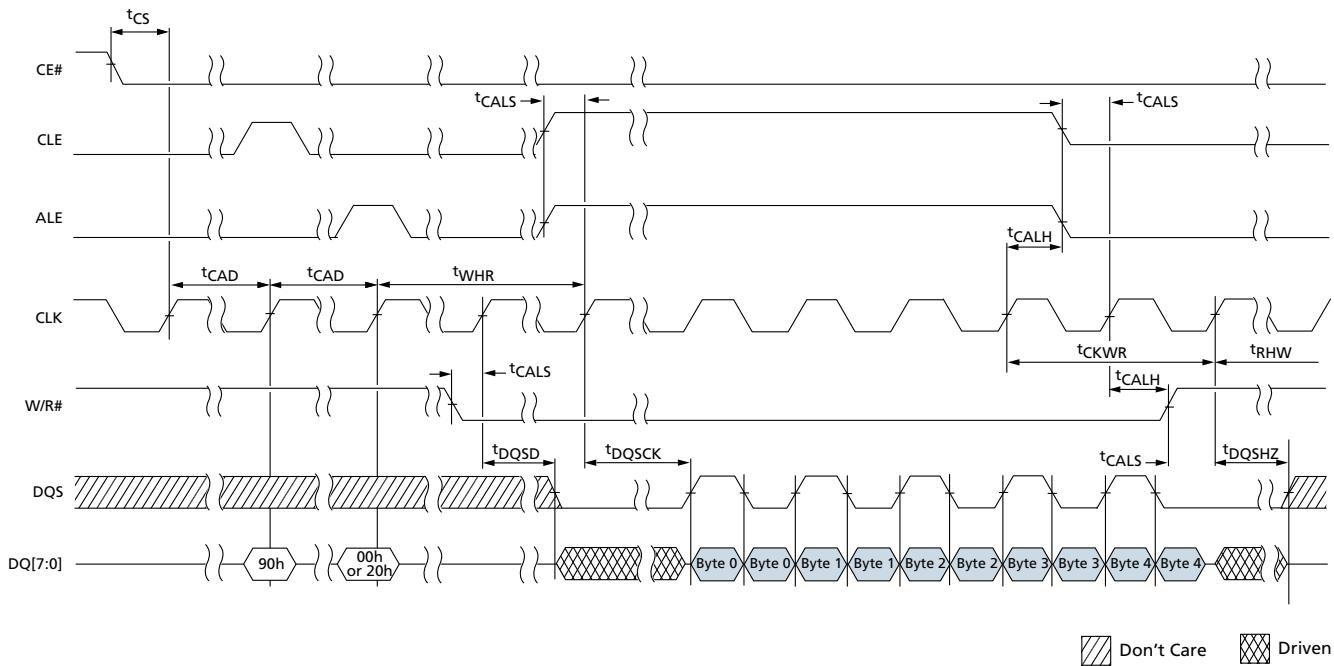
- Notes:
1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
 2. t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
 3. t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).
 4. The cycle that t_{CAD} is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 114: READ ID Operation

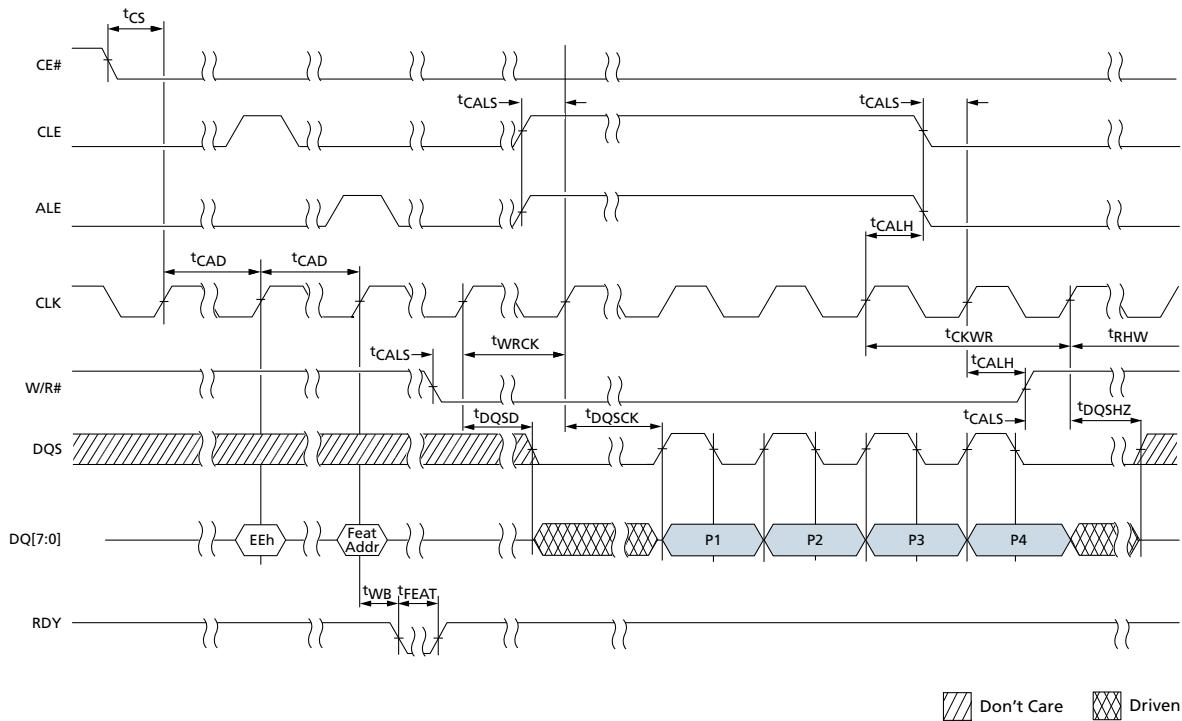


Release: 3/26/13

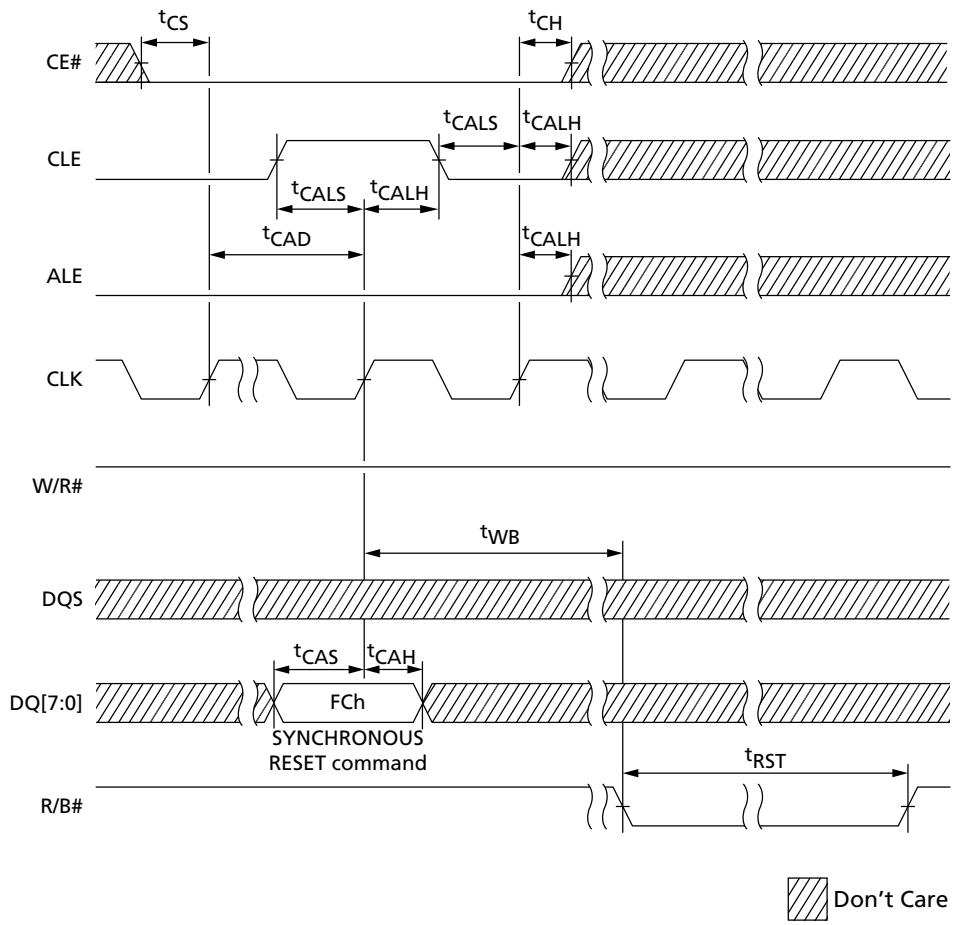


128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 115: GET FEATURES Operation



Release: 3/26/13

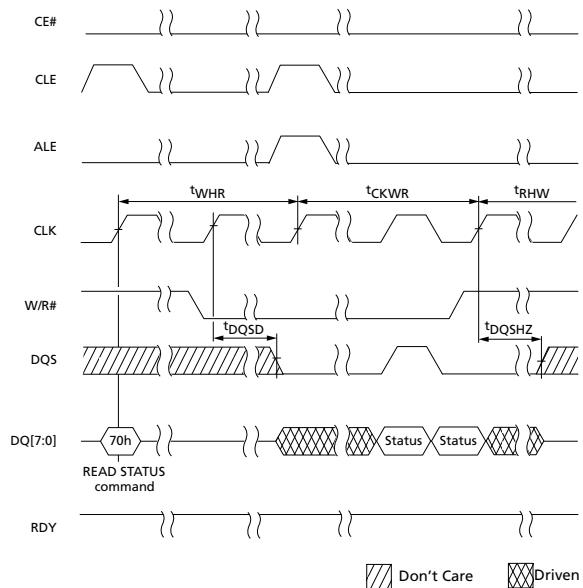
**Figure 116: RESET (FCh) Operation**

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 117: READ STATUS Cycle

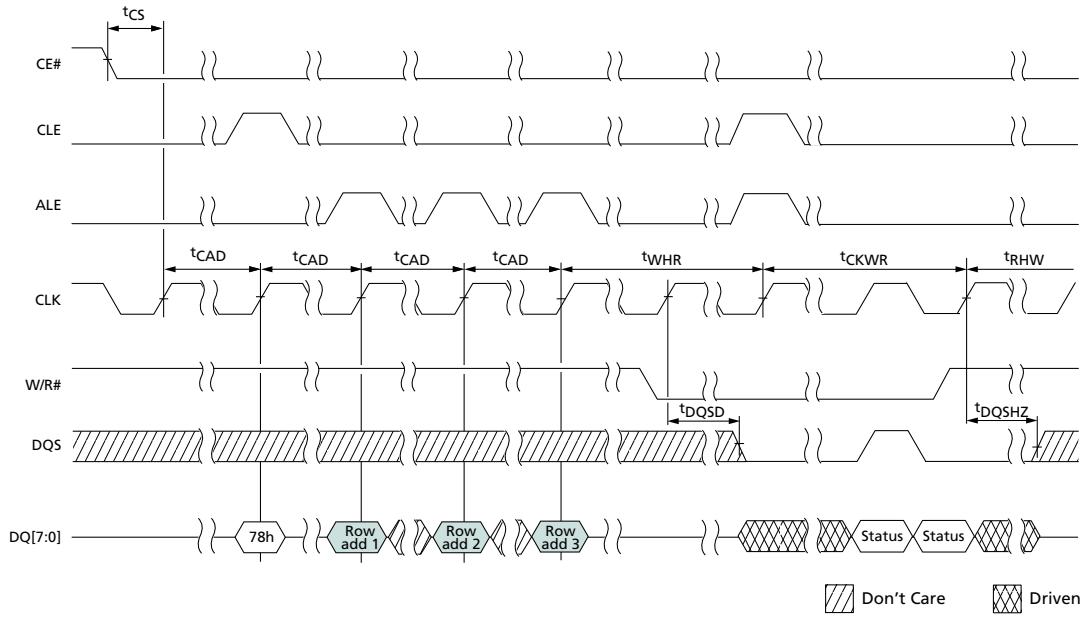


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 118: READ STATUS ENHANCED Operation

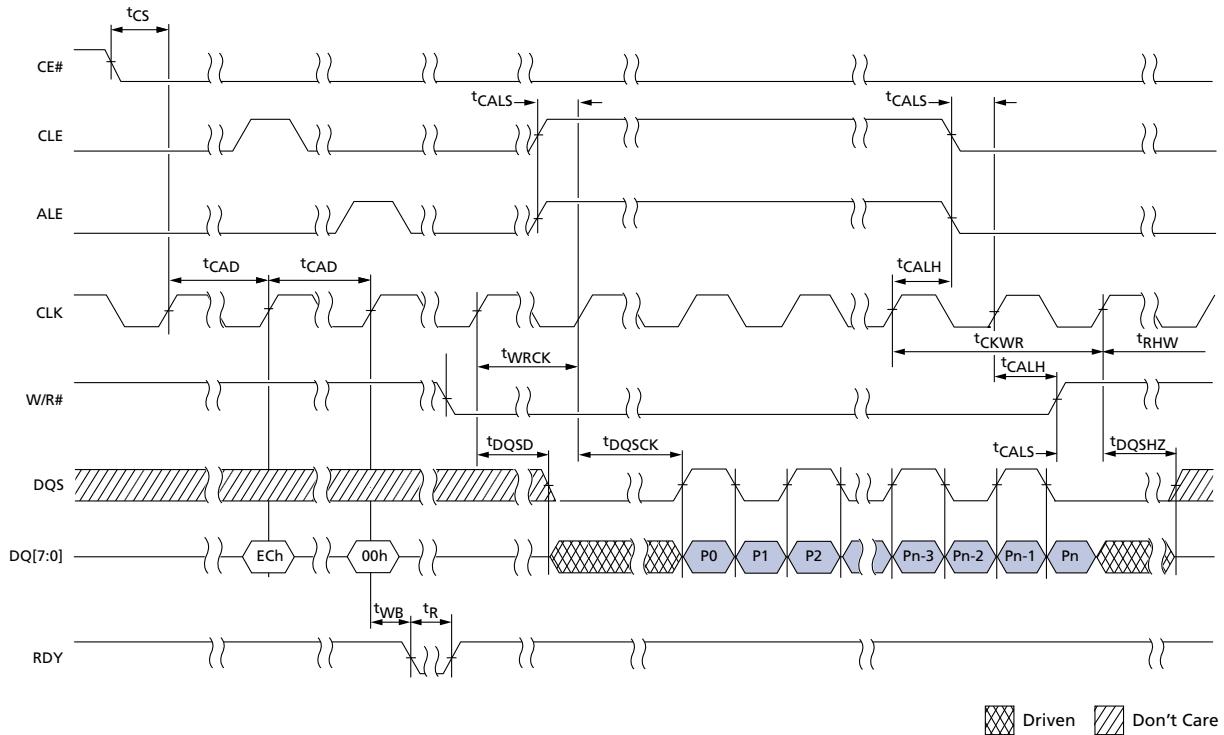


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 119: READ PARAMETER PAGE Operation

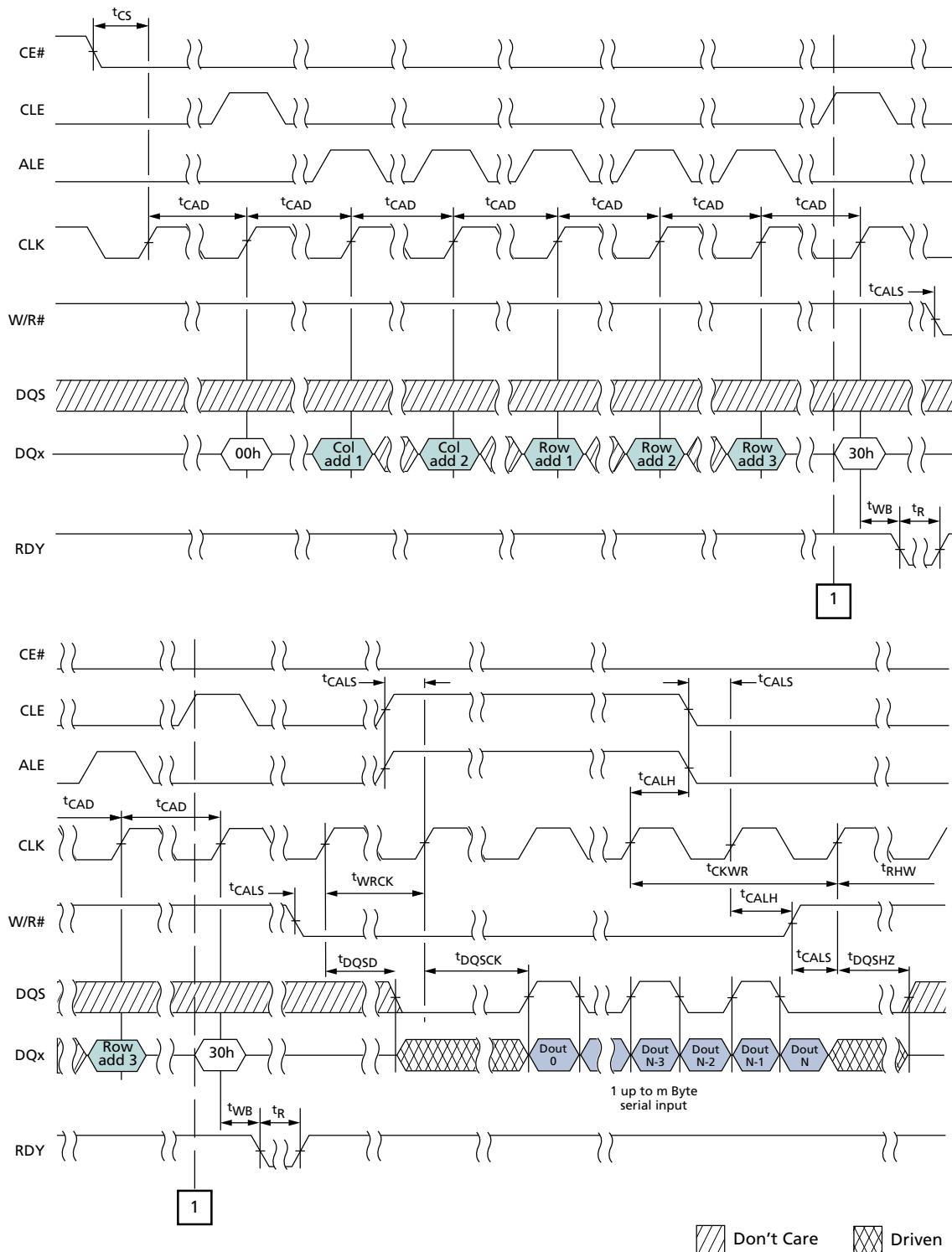


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 120: READ PAGE Operation

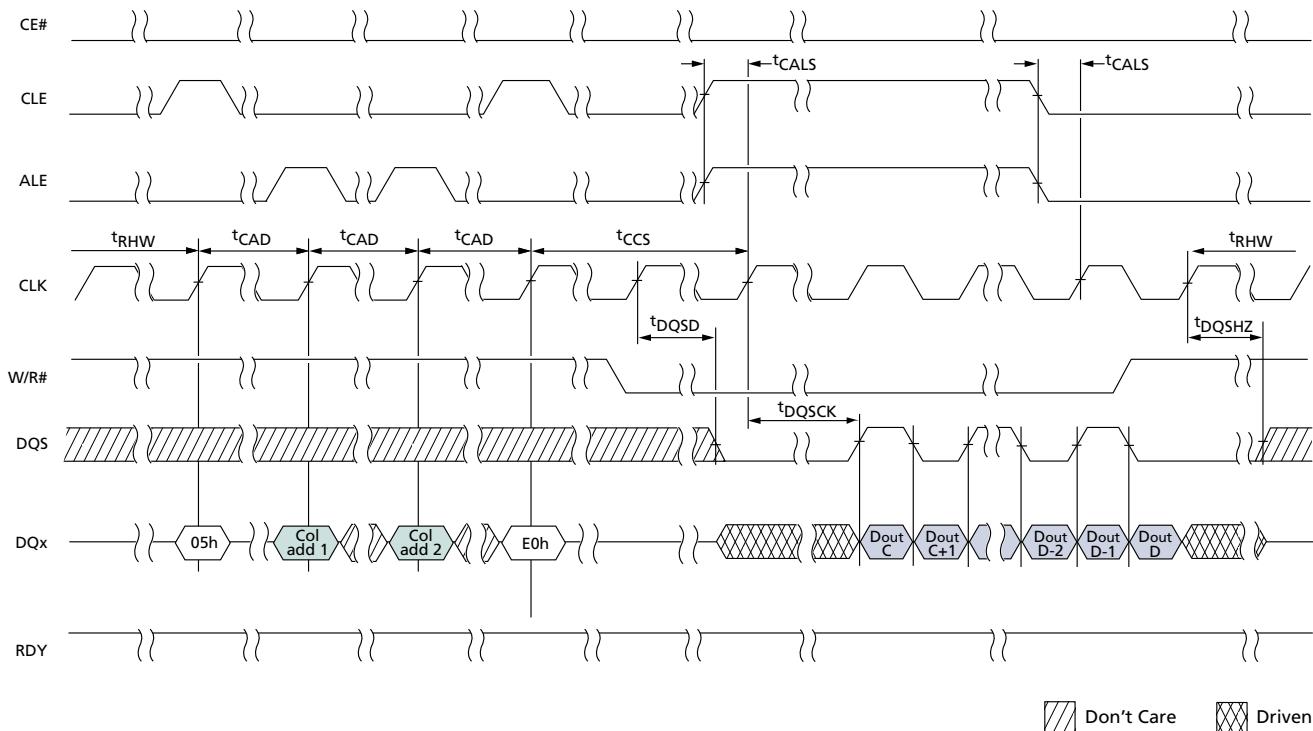


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 121: CHANGE READ COLUMN

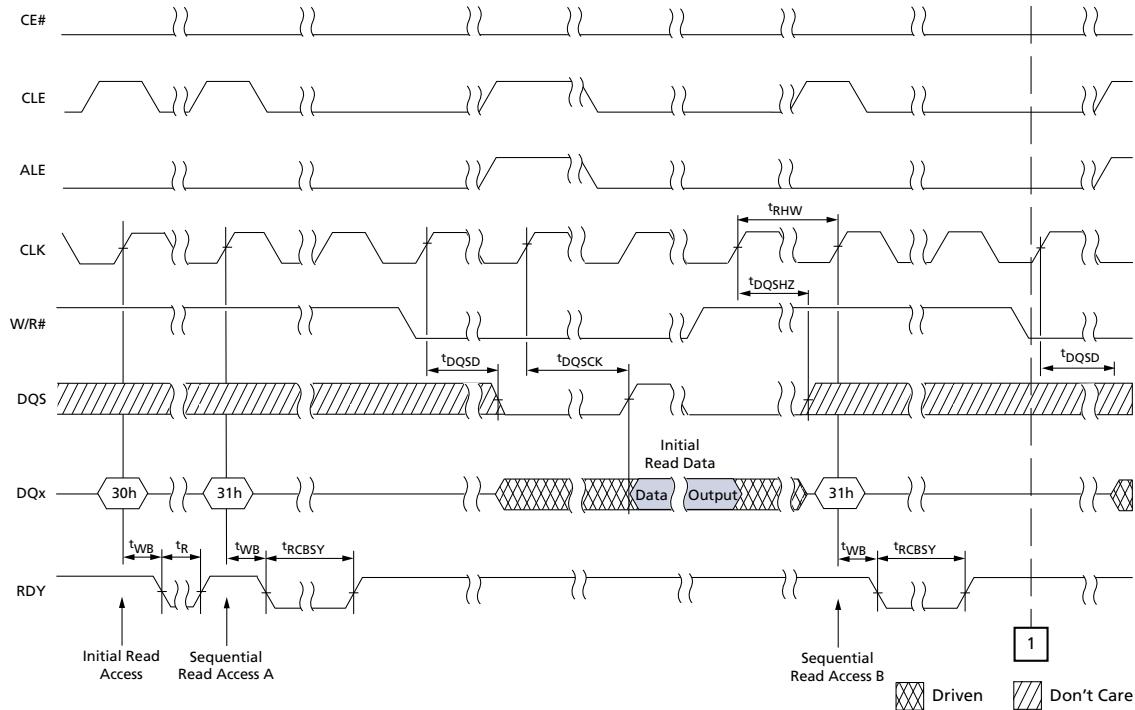


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 122: READ PAGE CACHE SEQUENTIAL (1 of 2)

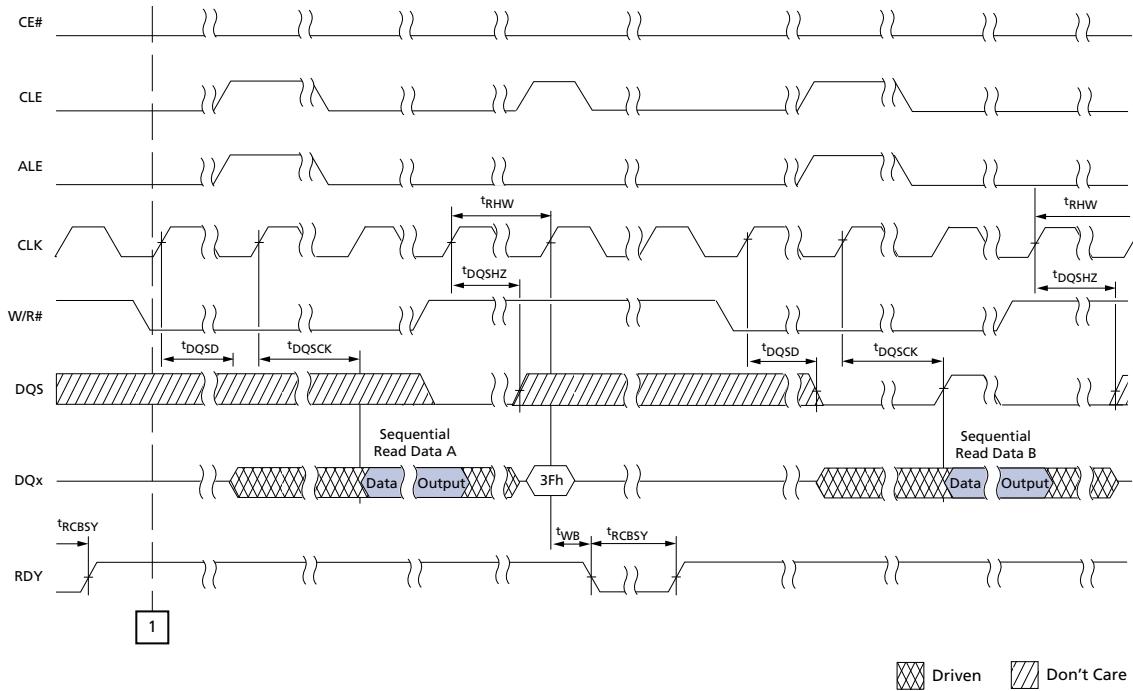


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 123: READ PAGE CACHE SEQUENTIAL (2 of 2)



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 124: READ PAGE CACHE RANDOM (1 of 2)

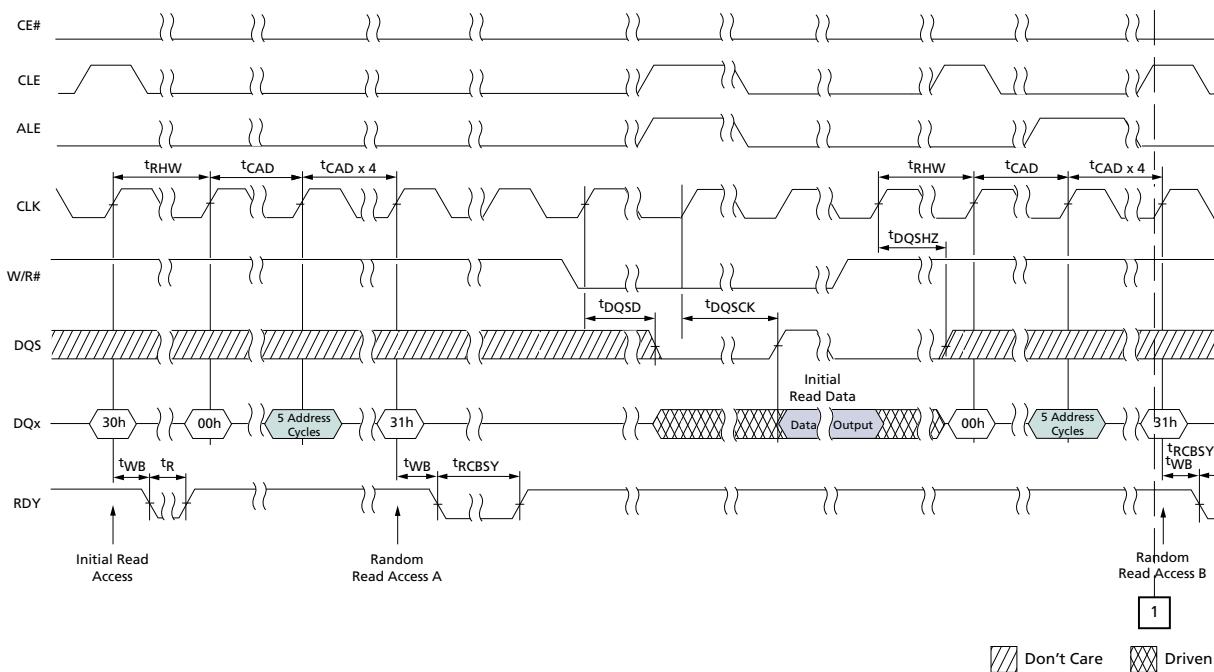
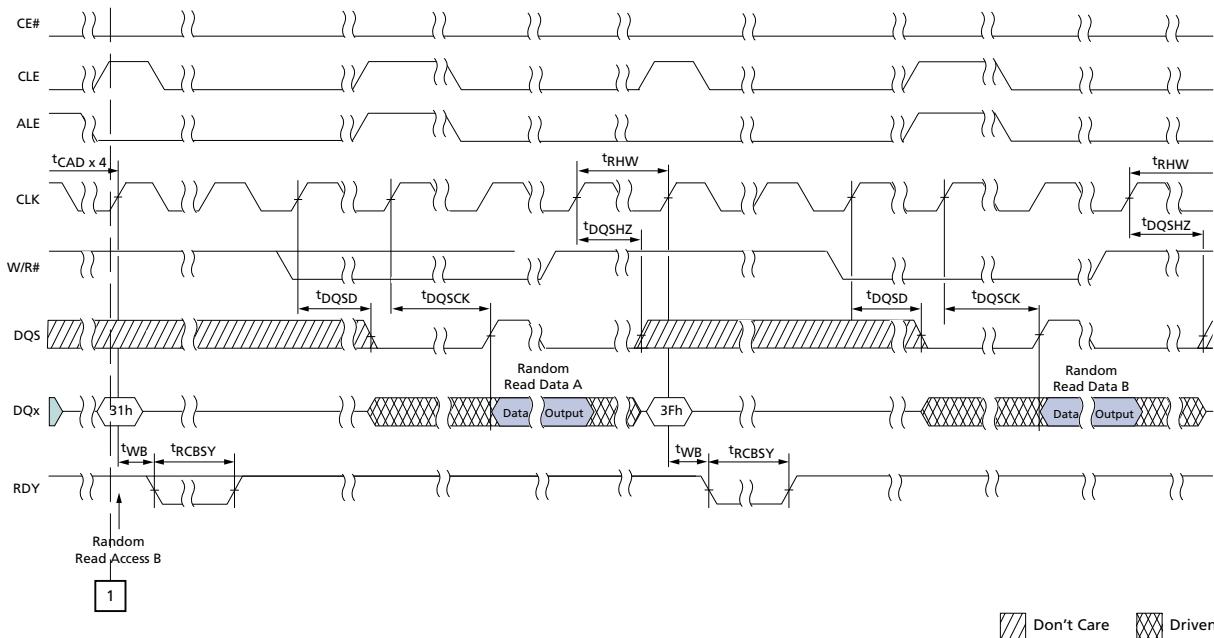


Figure 125: READ PAGE CACHE RANDOM (2 of 2)

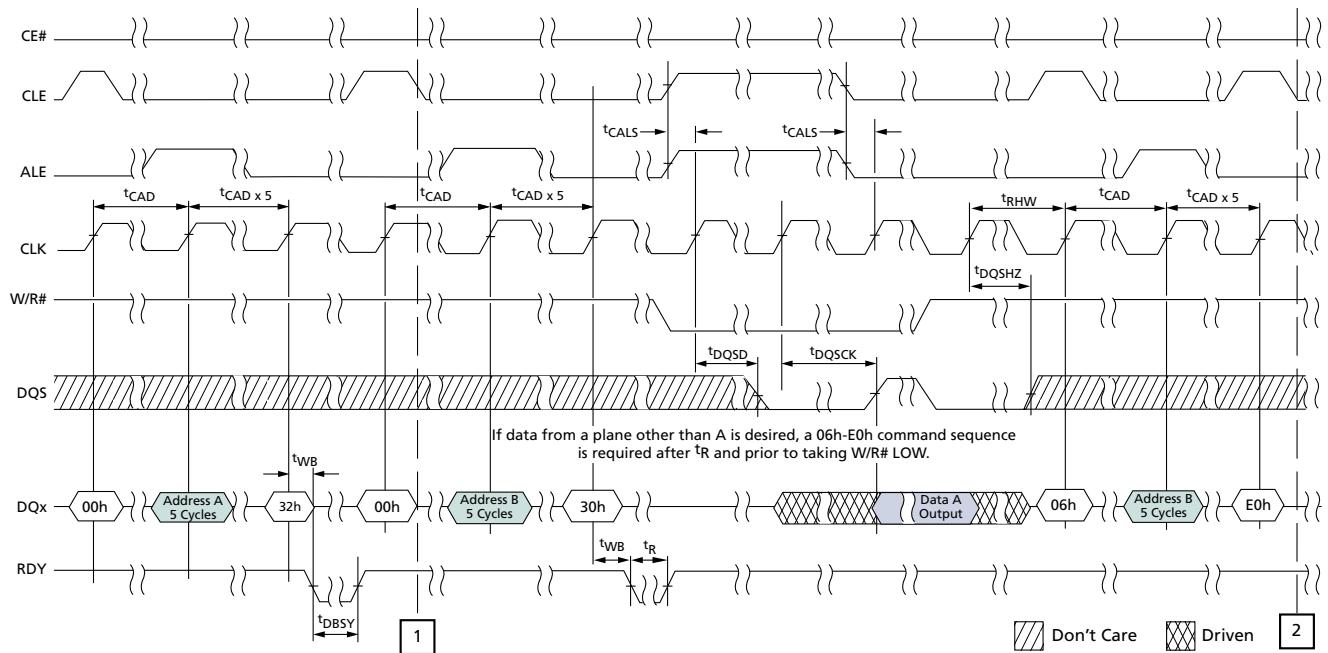


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 126: Multi-Plane Read Page (1 of 2)

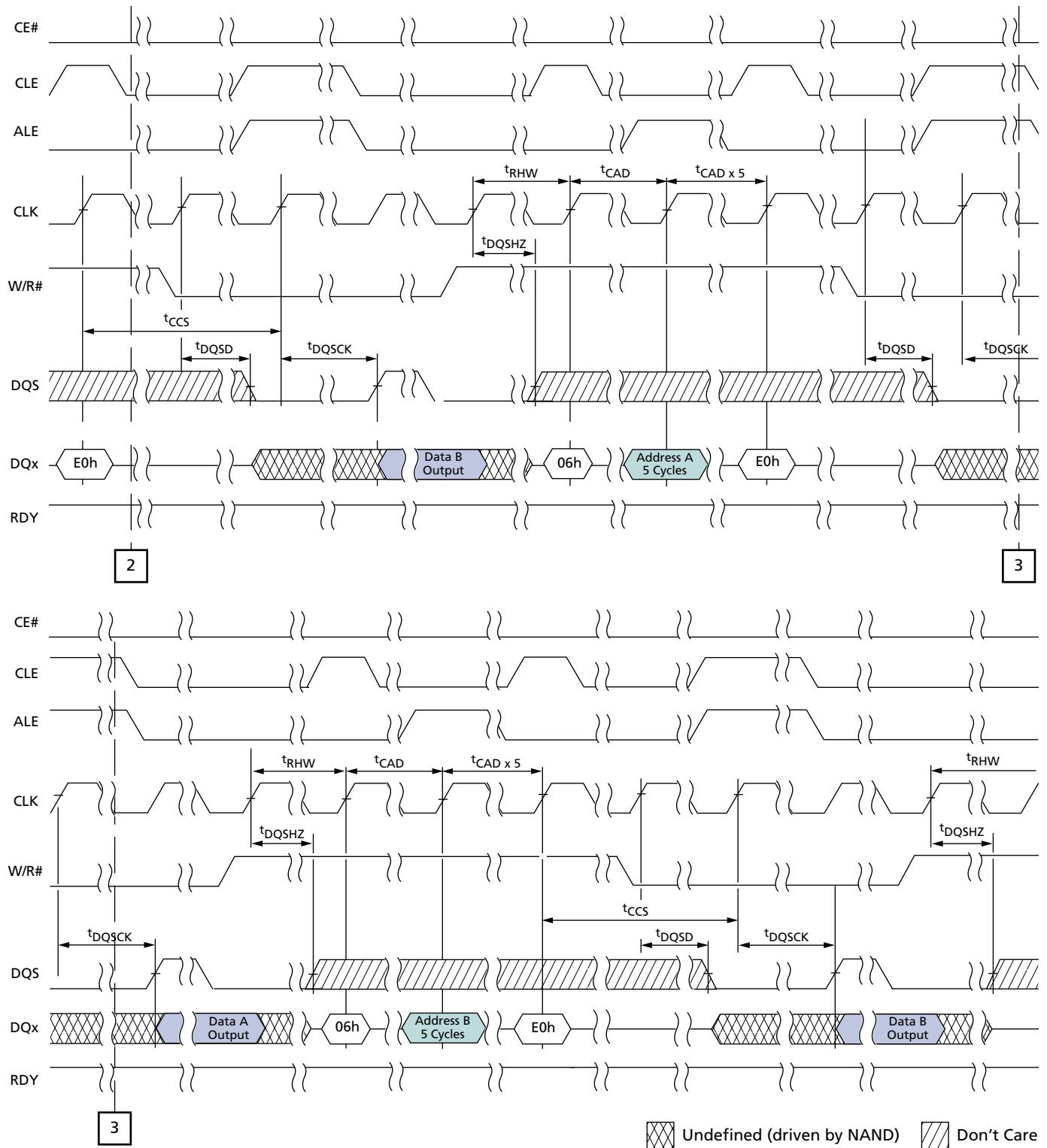


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 127: Multi-Plane Read Page (2 of 2)

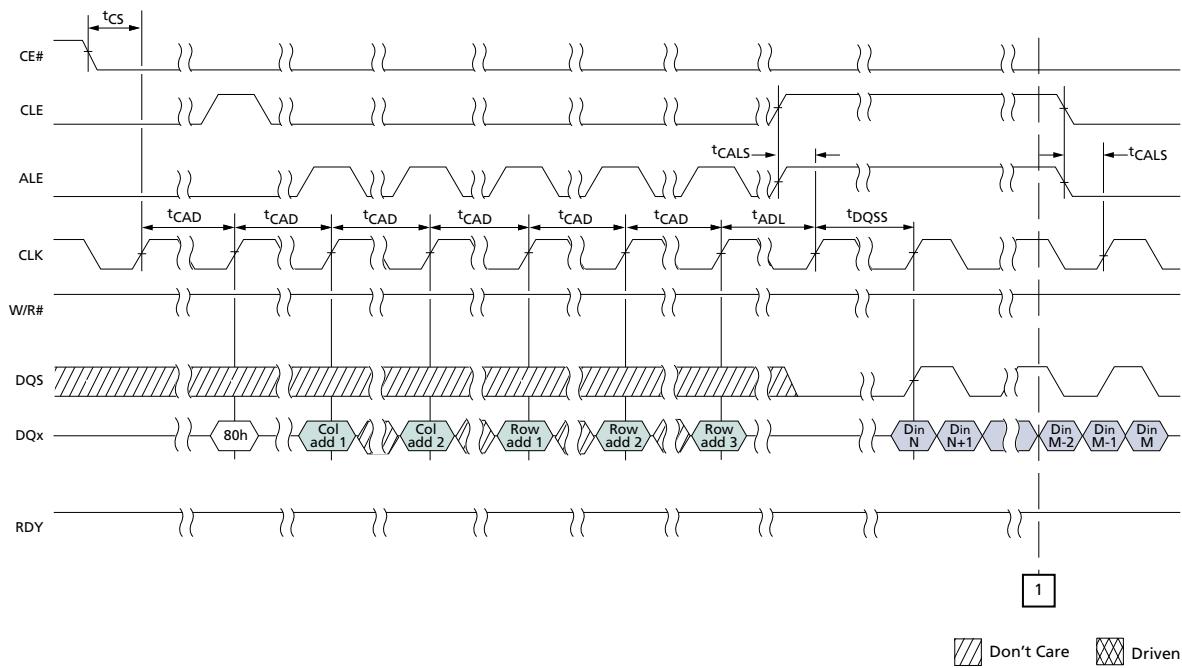


Release: 3/26/13



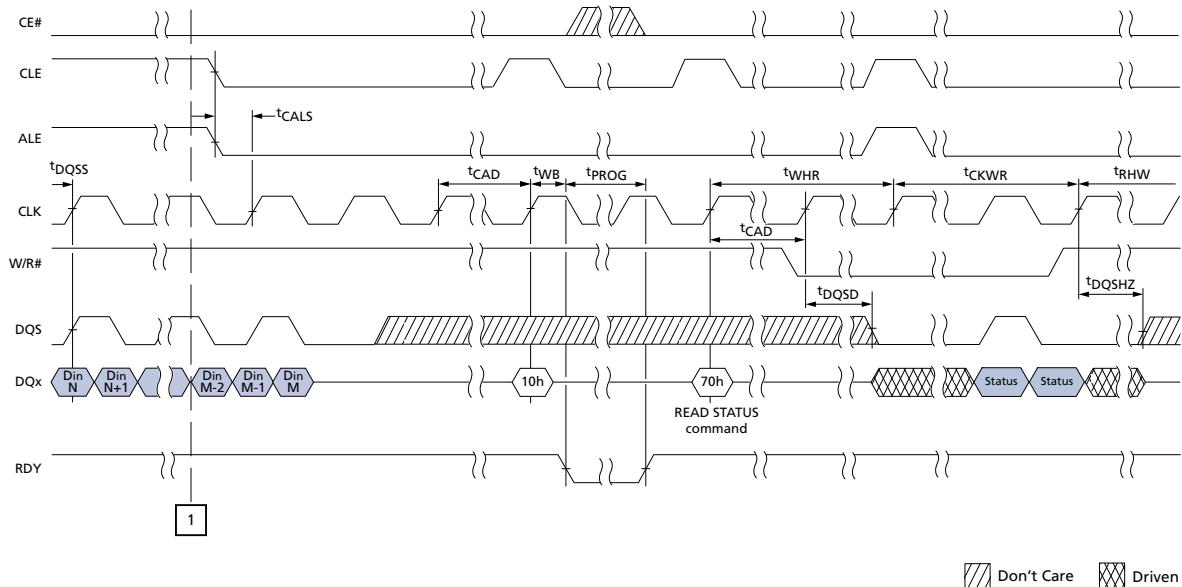
128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 128: PROGRAM PAGE Operation (1 of 2)



Don't Care Driven

Figure 129: PROGRAM PAGE Operation (2 of 2)



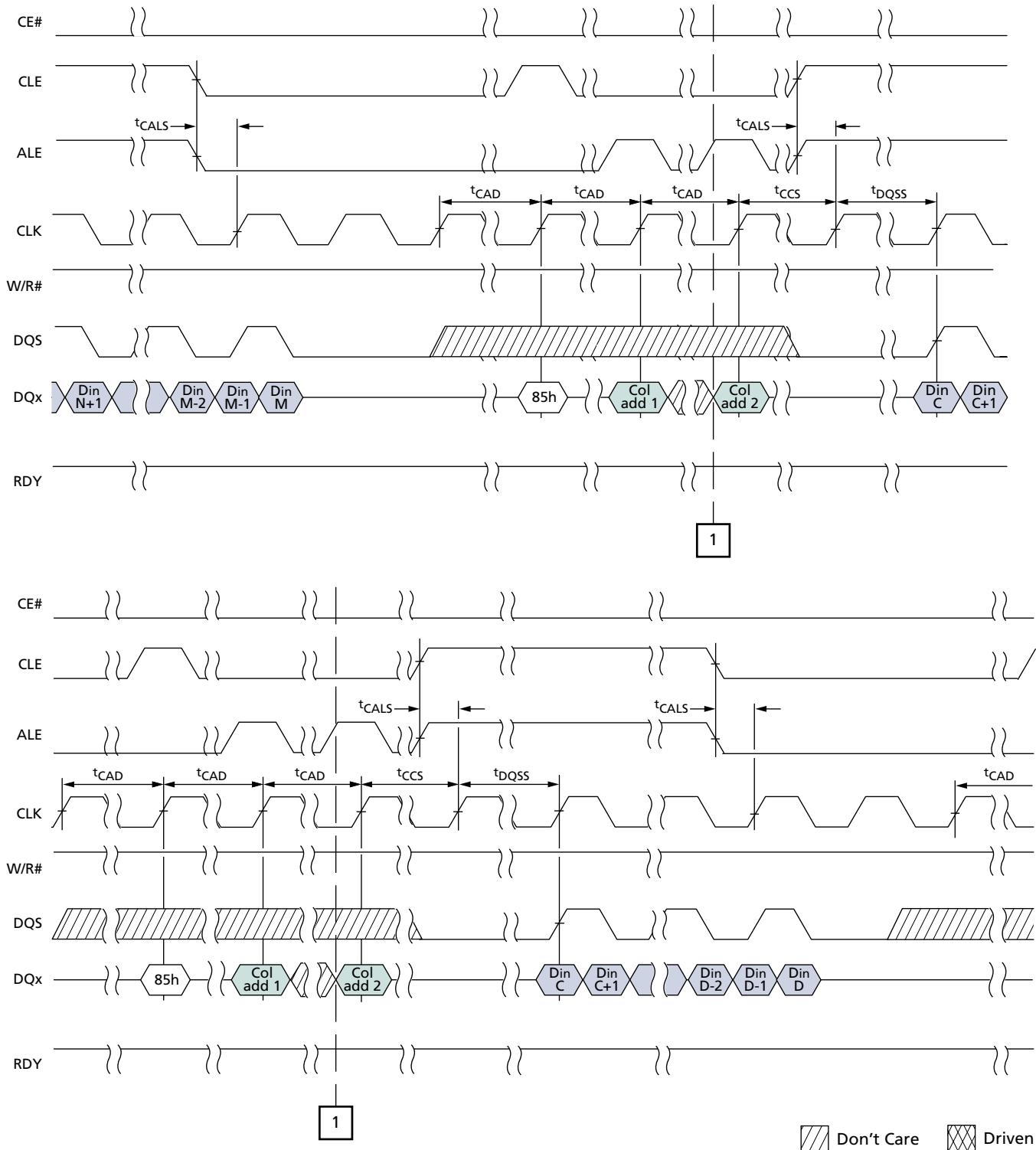
Don't Care Driven

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 130: CHANGE WRITE COLUMN

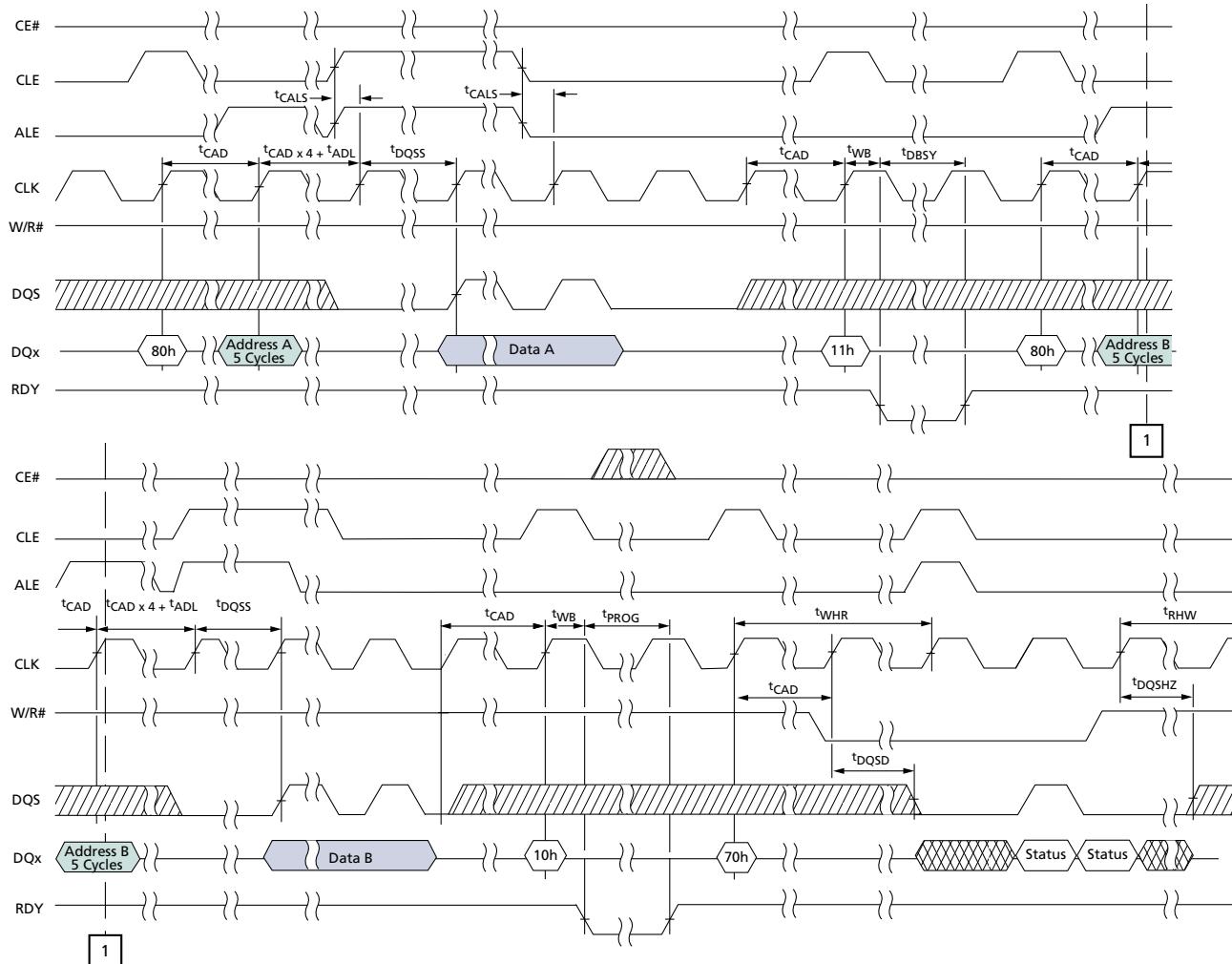


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 131: Multi-Plane Program Page



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 132: ERASE BLOCK

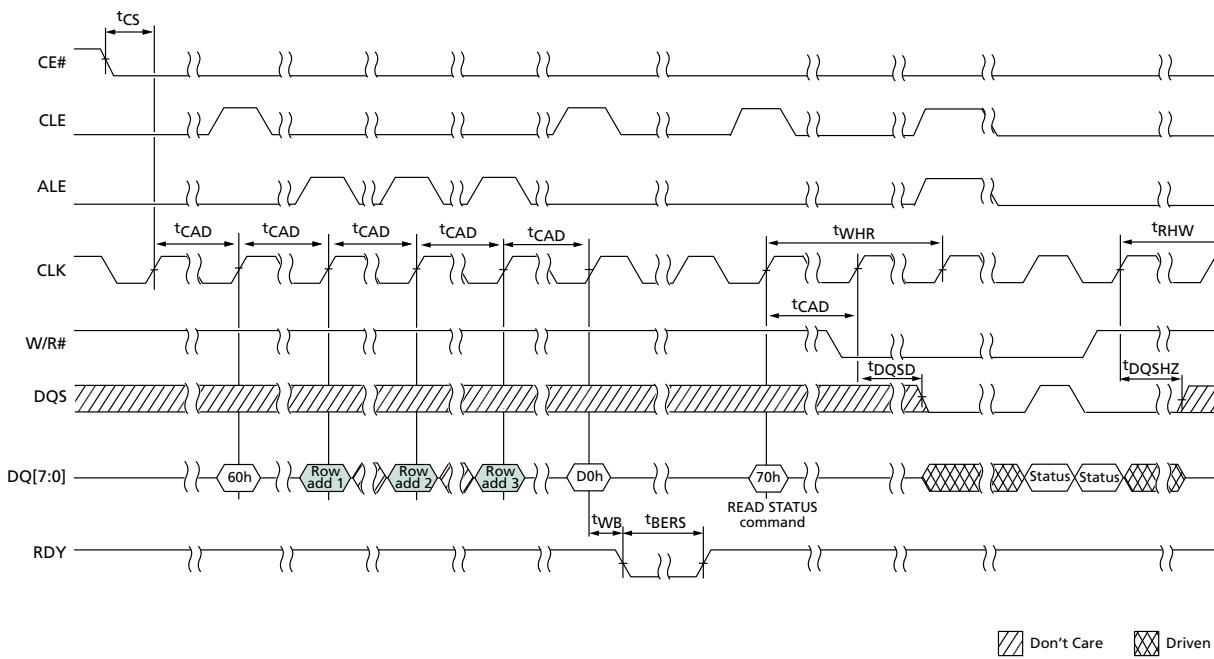
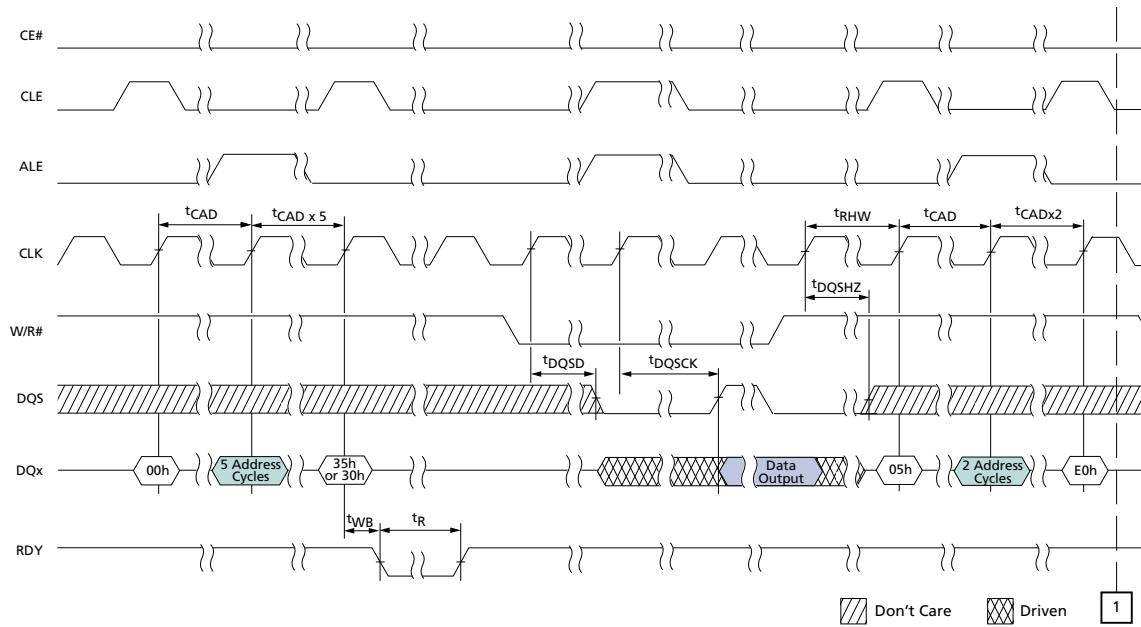


Figure 133: COPYBACK (1 of 3)



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 134: COPYBACK (2 of 3)

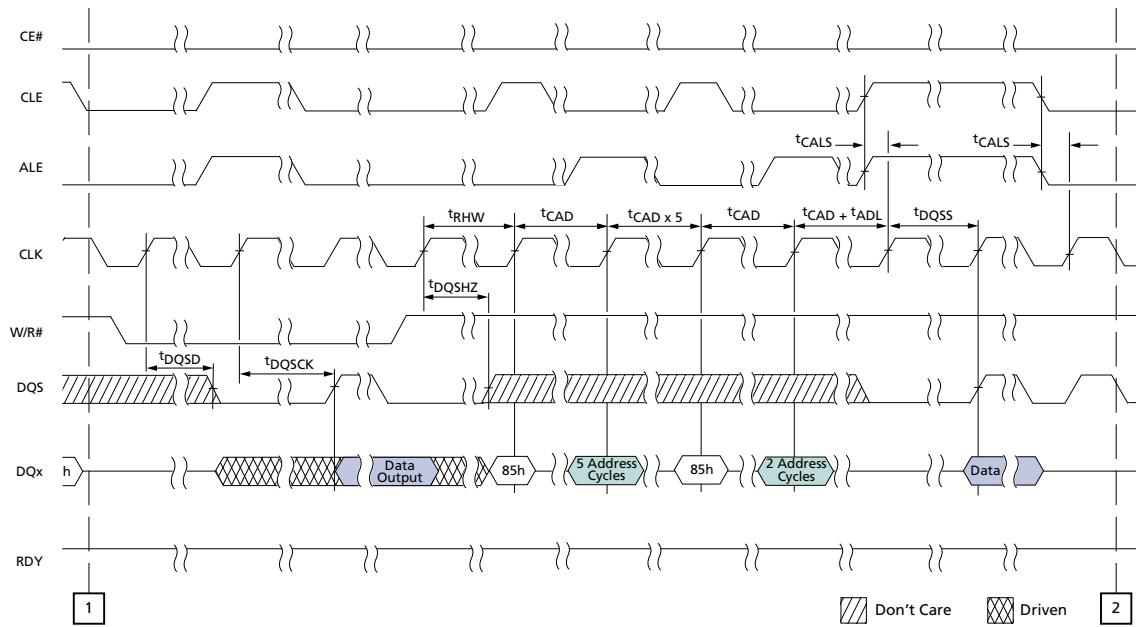
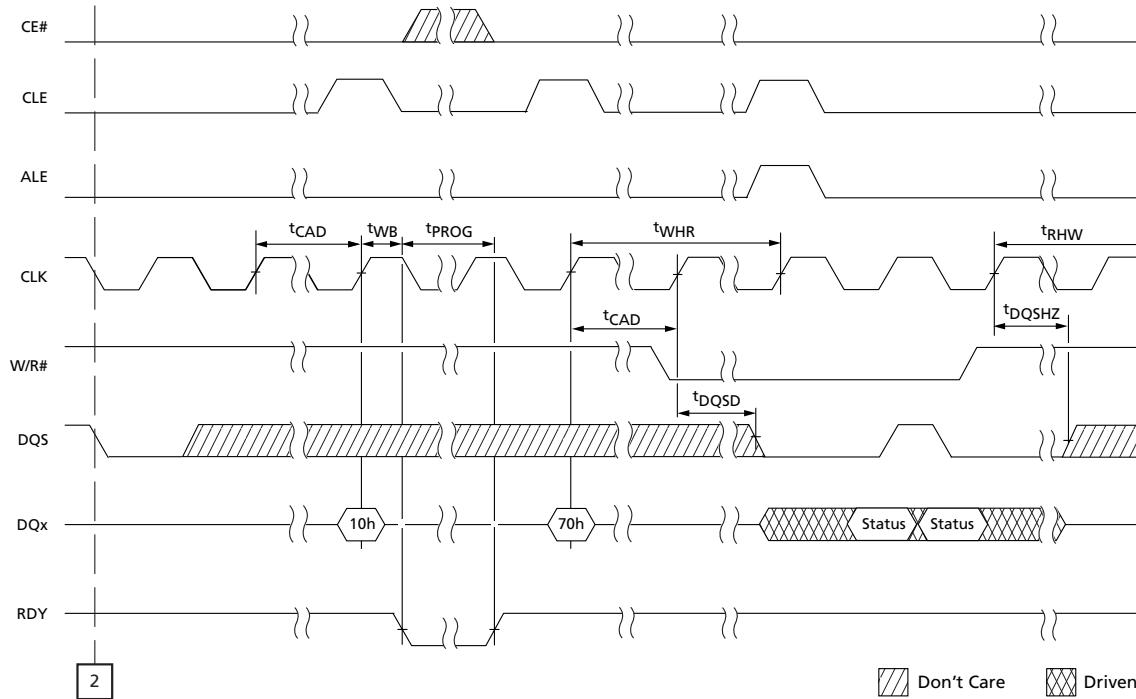


Figure 135: COPYBACK (3 of 3)

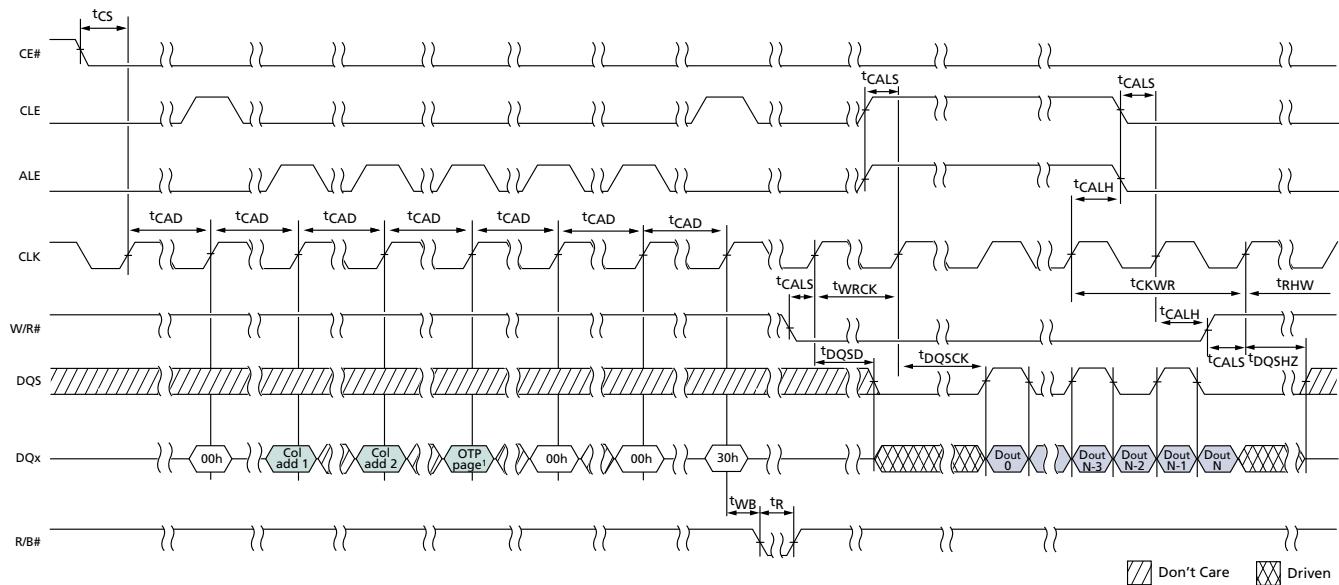


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 136: READ OTP PAGE



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 137: PROGRAM OTP PAGE (1 of 2)

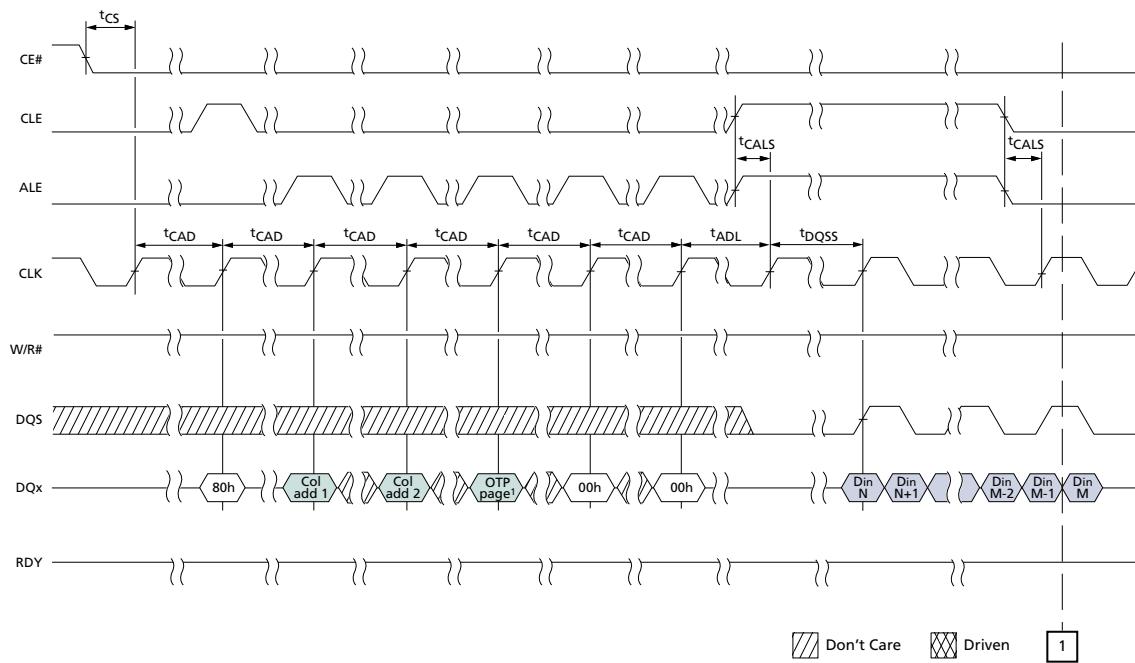
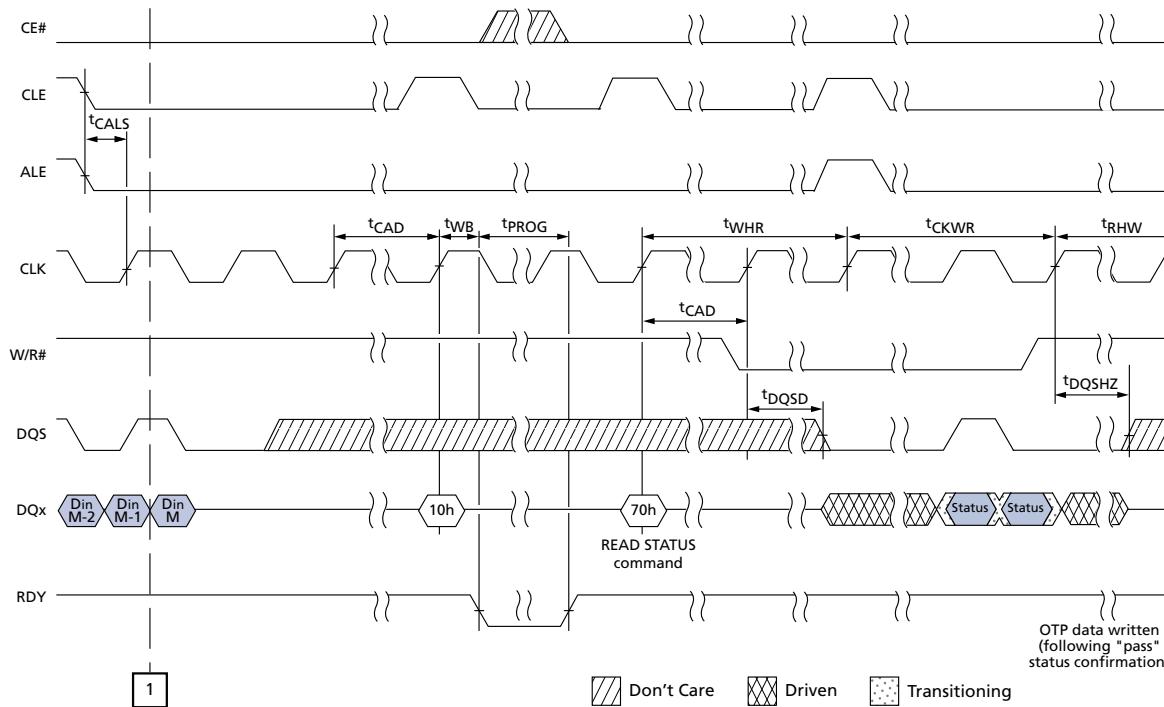


Figure 138: PROGRAM OTP PAGE (2 of 2)

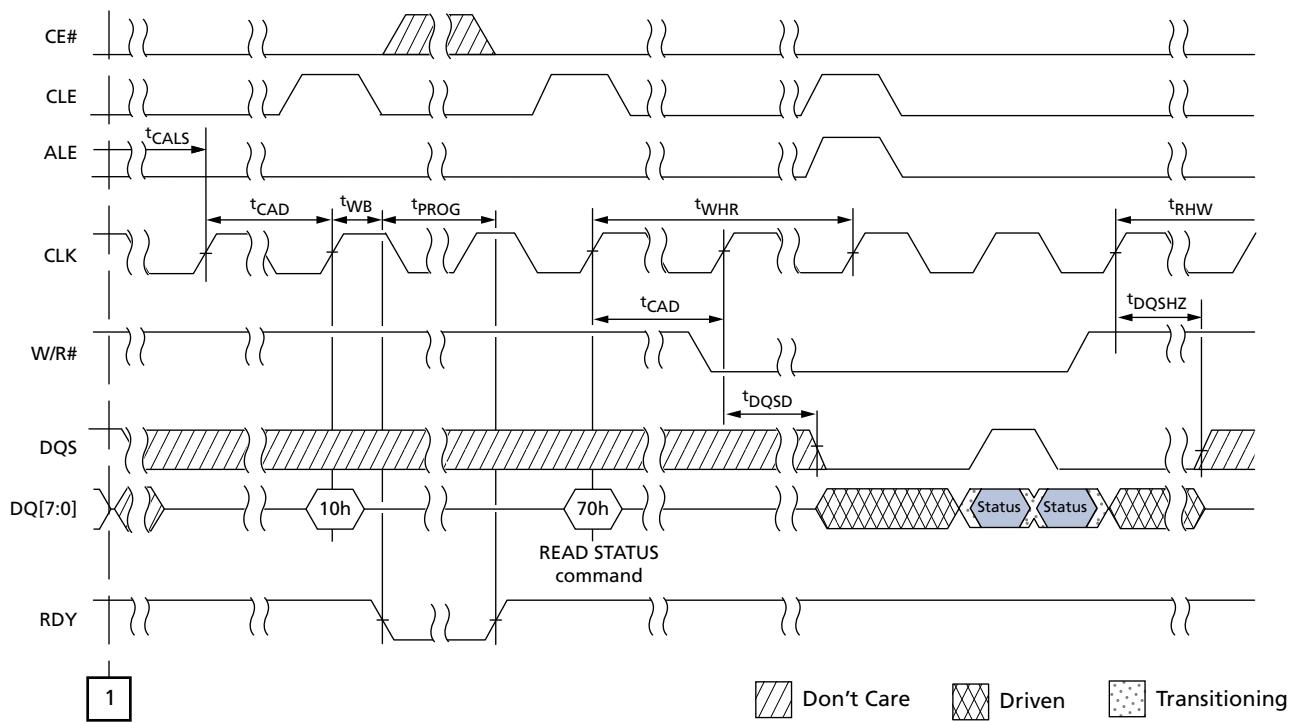
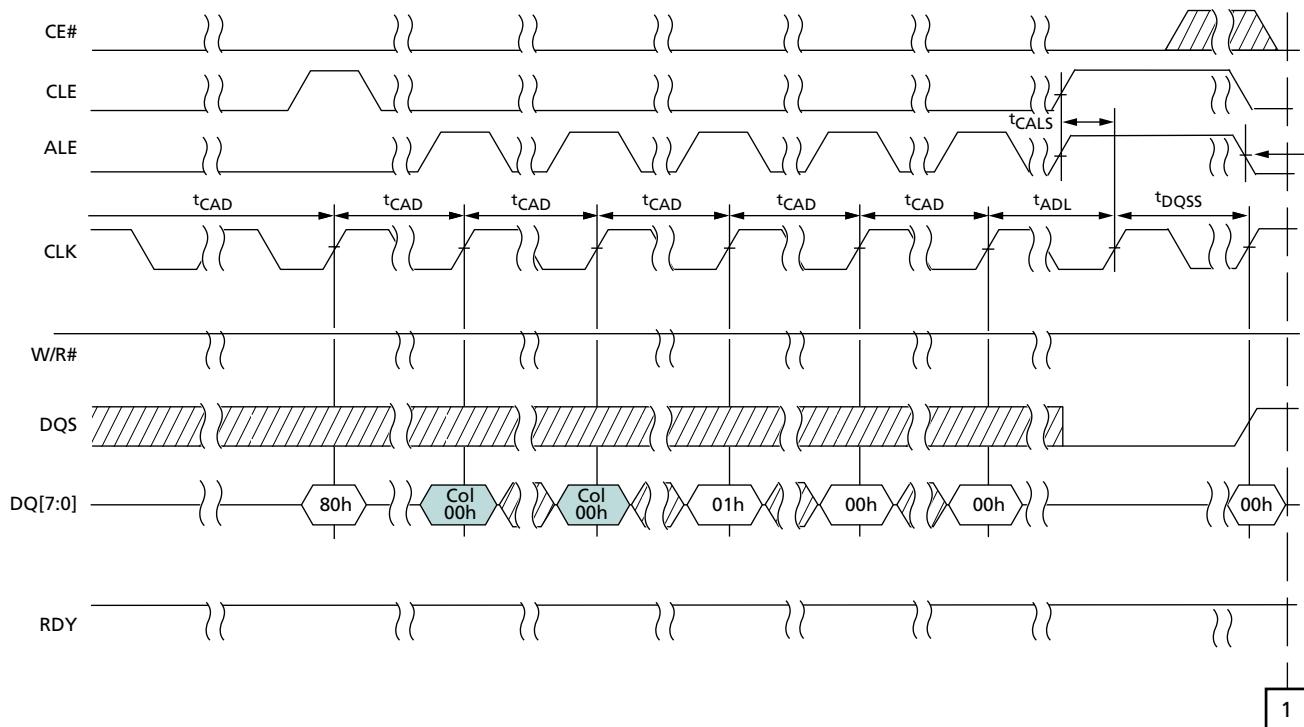


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR Interface Timing Diagrams

Figure 139: PROTECT OTP AREA

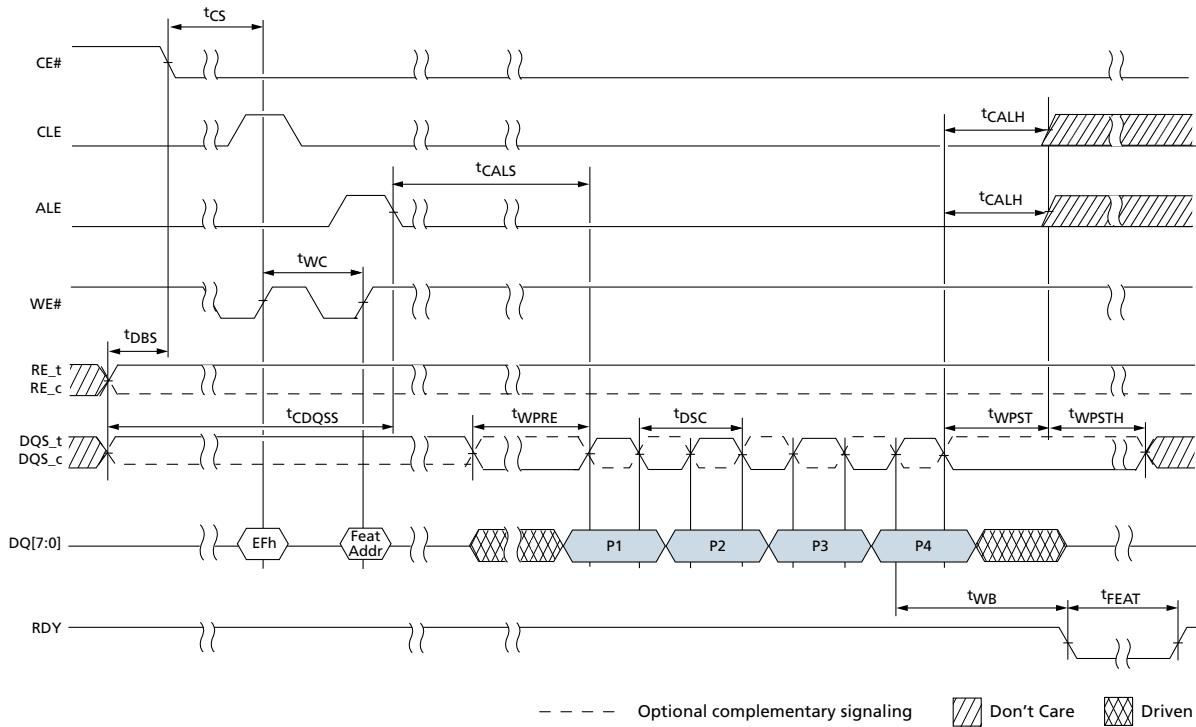


Release: 3/26/13



NV-DDR2 Interface Timing Diagrams

Figure 140: SET FEATURES Operation

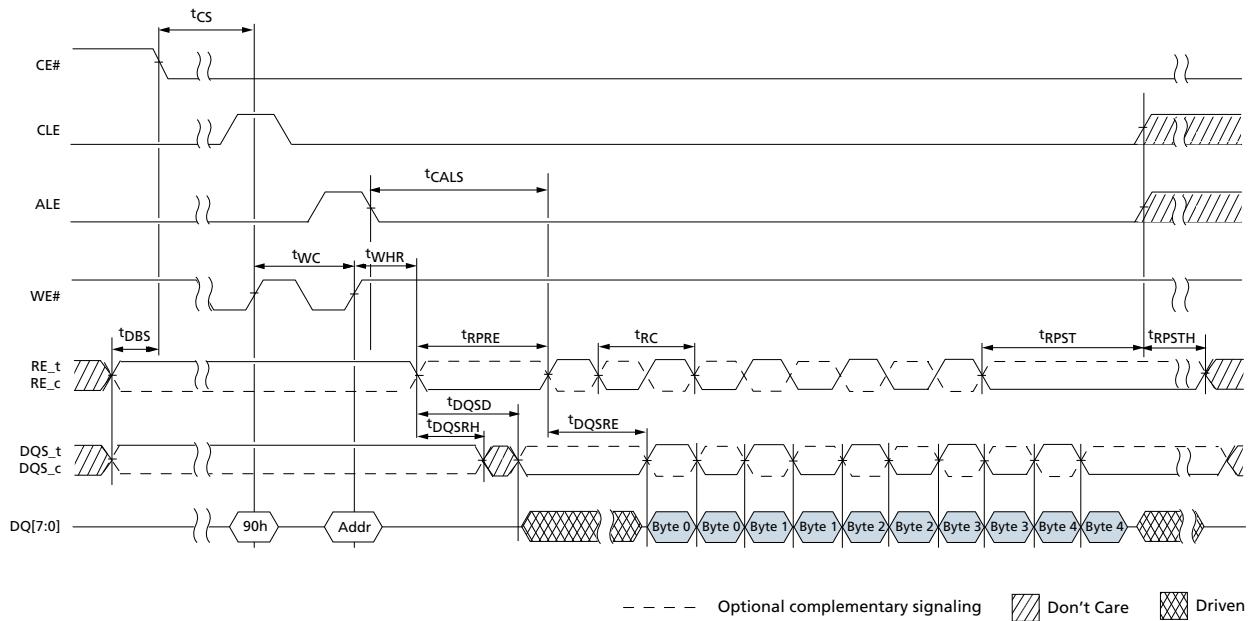


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 141: READ ID Operation

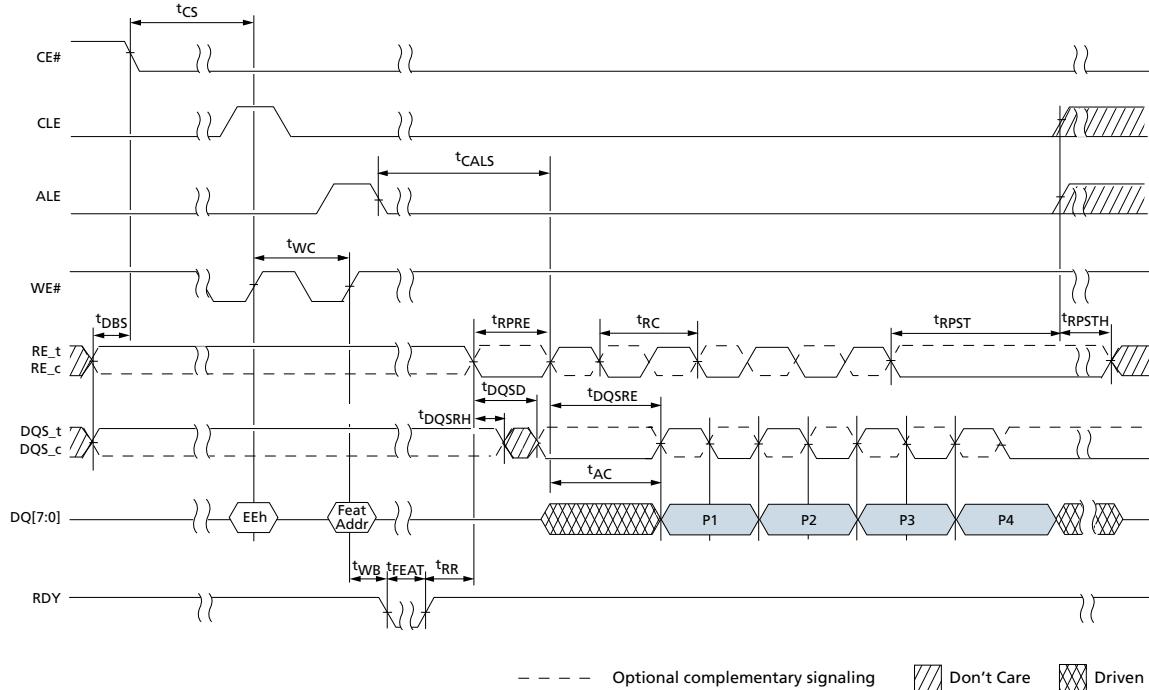


Release: 3/26/13

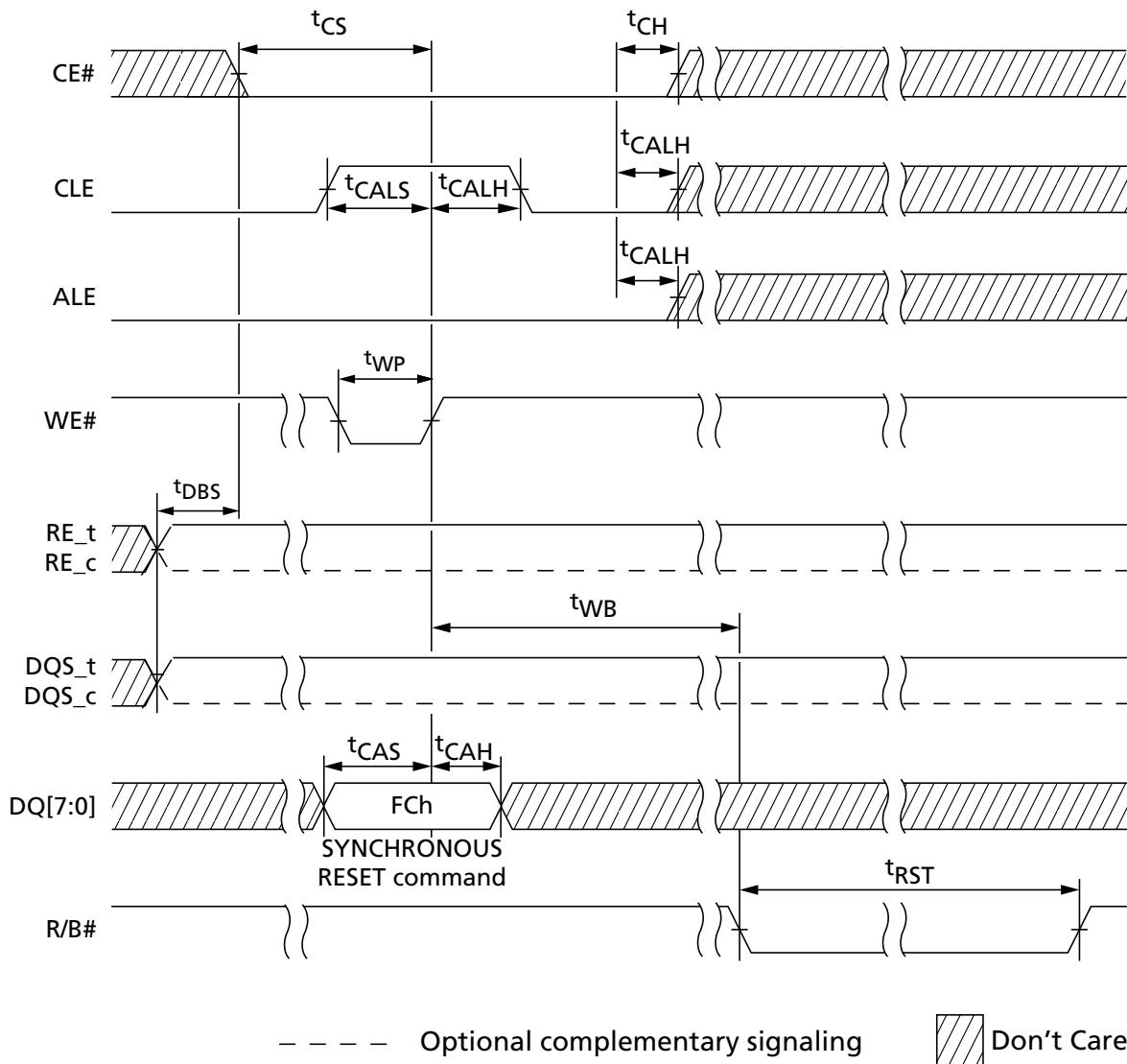


128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

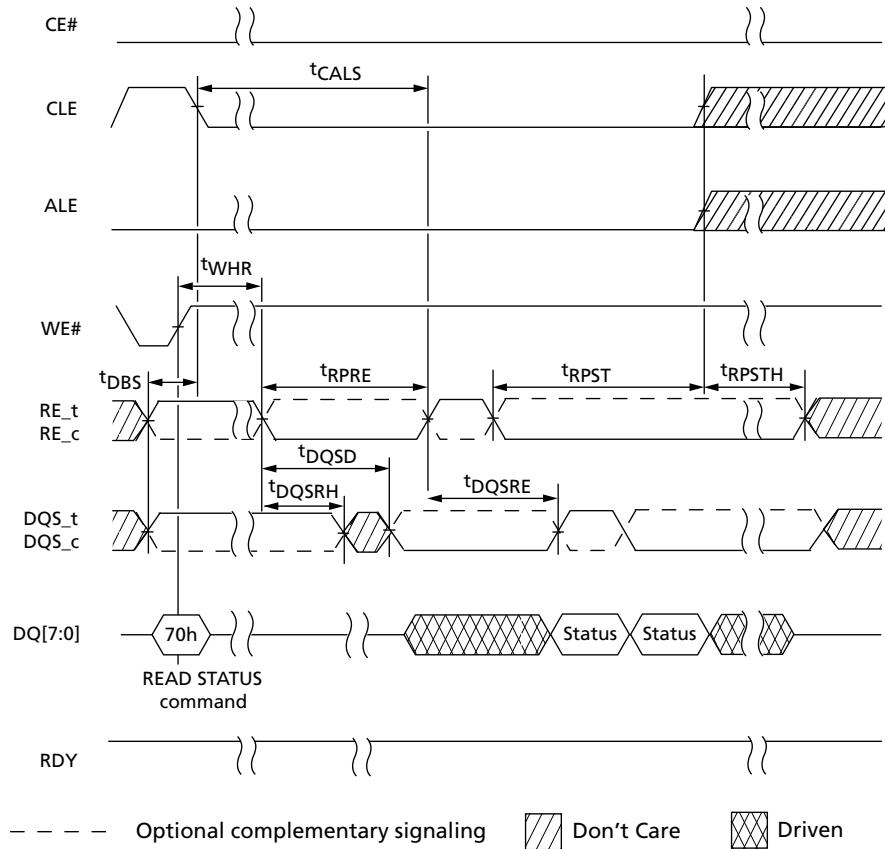
Figure 142: GET FEATURES Operation



Release: 3/26/13

**Figure 143: RESET (FCh) Operation**

Release: 3/26/13

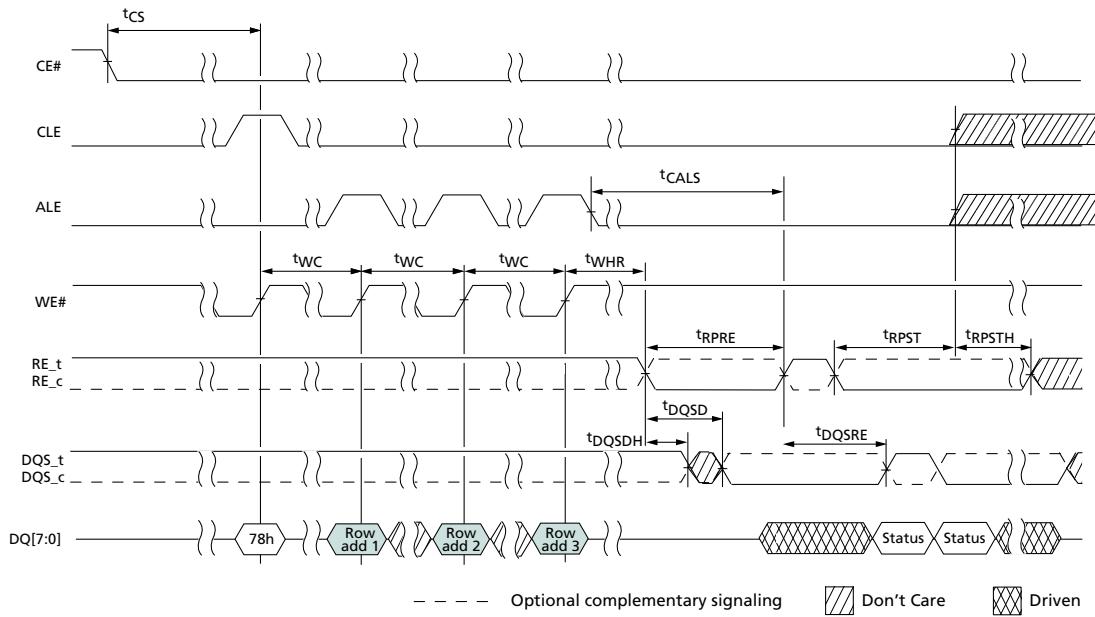
**Figure 144: READ STATUS Cycle**

Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 145: READ STATUS ENHANCED Operation

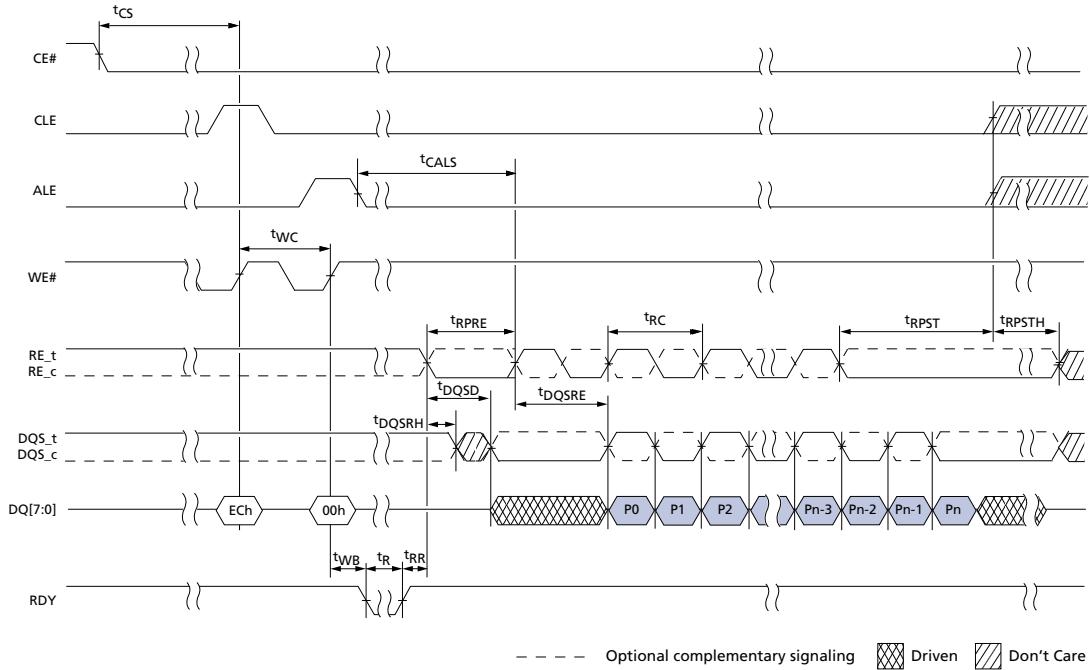


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 146: READ PARAMETER PAGE Operation

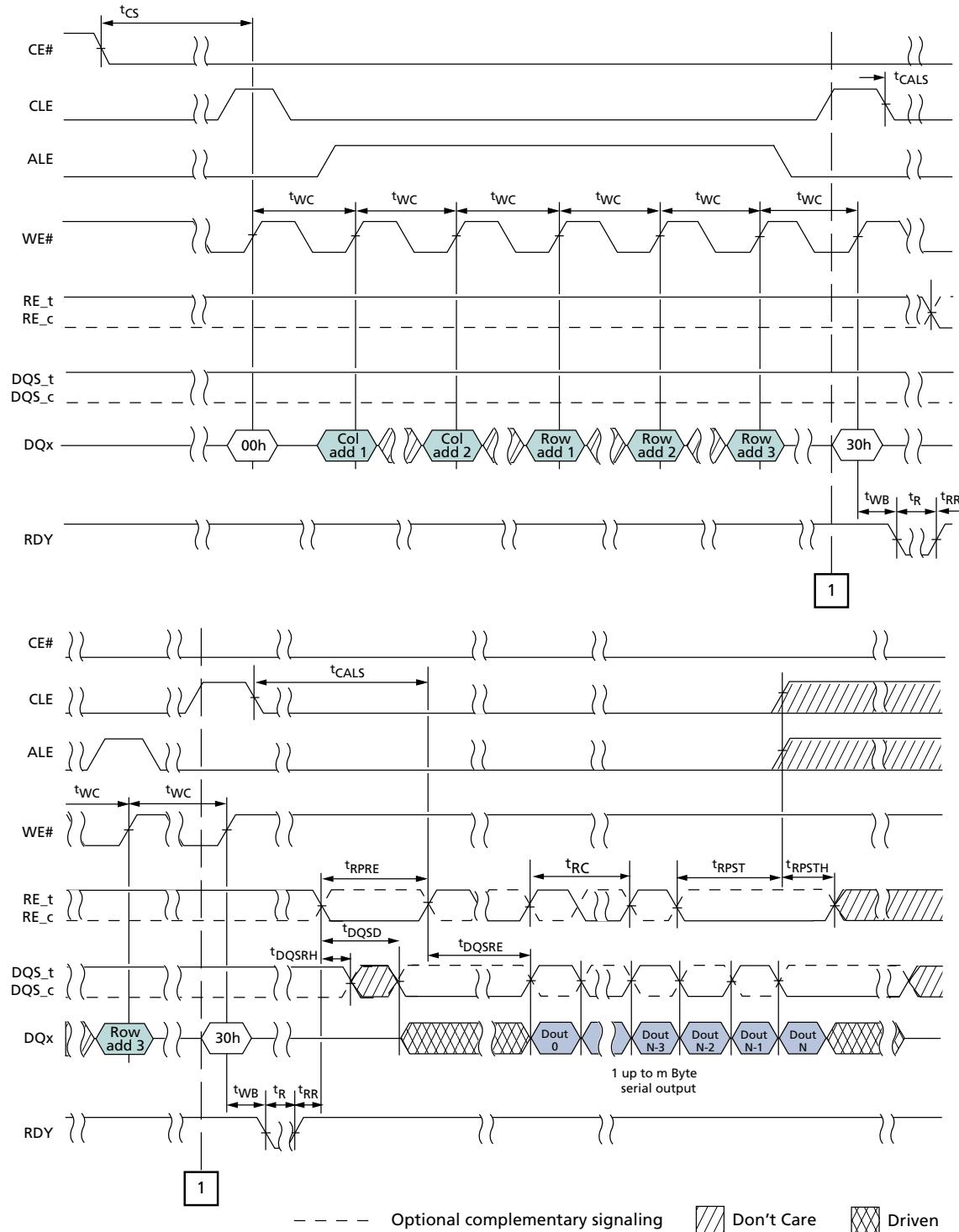


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 147: READ PAGE Operation

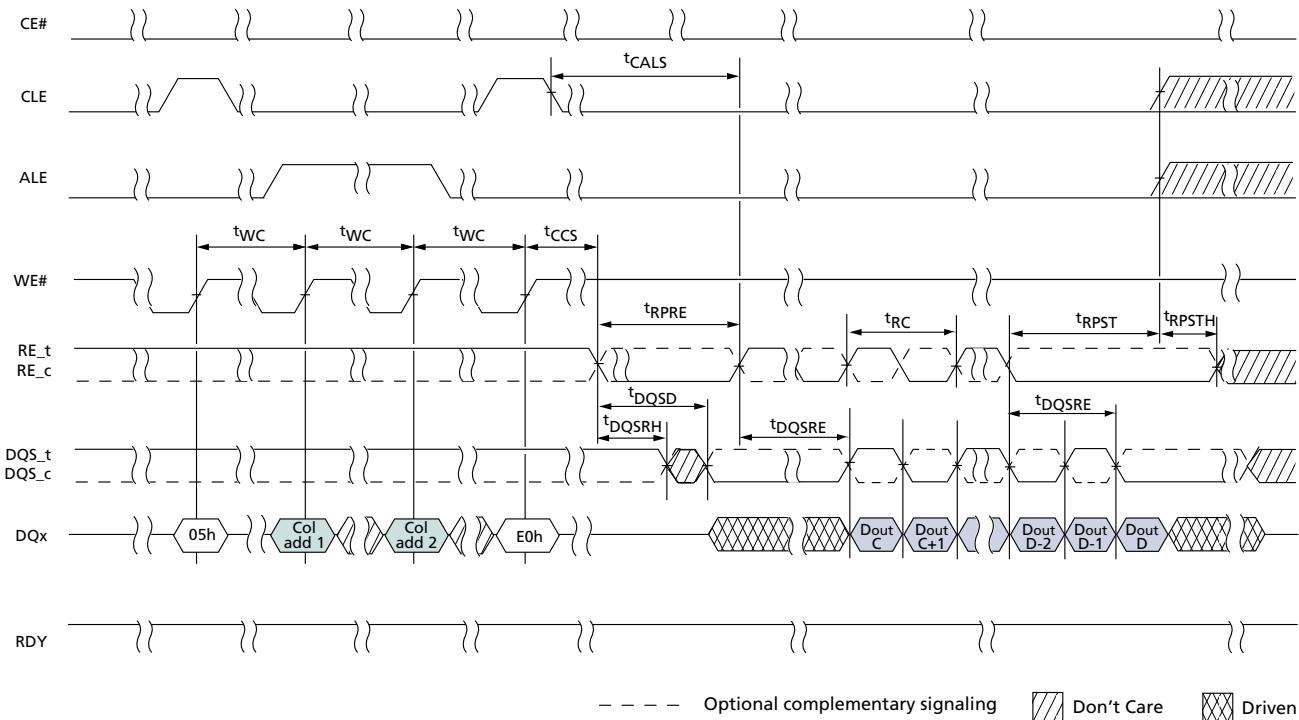


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 148: CHANGE READ COLUMN

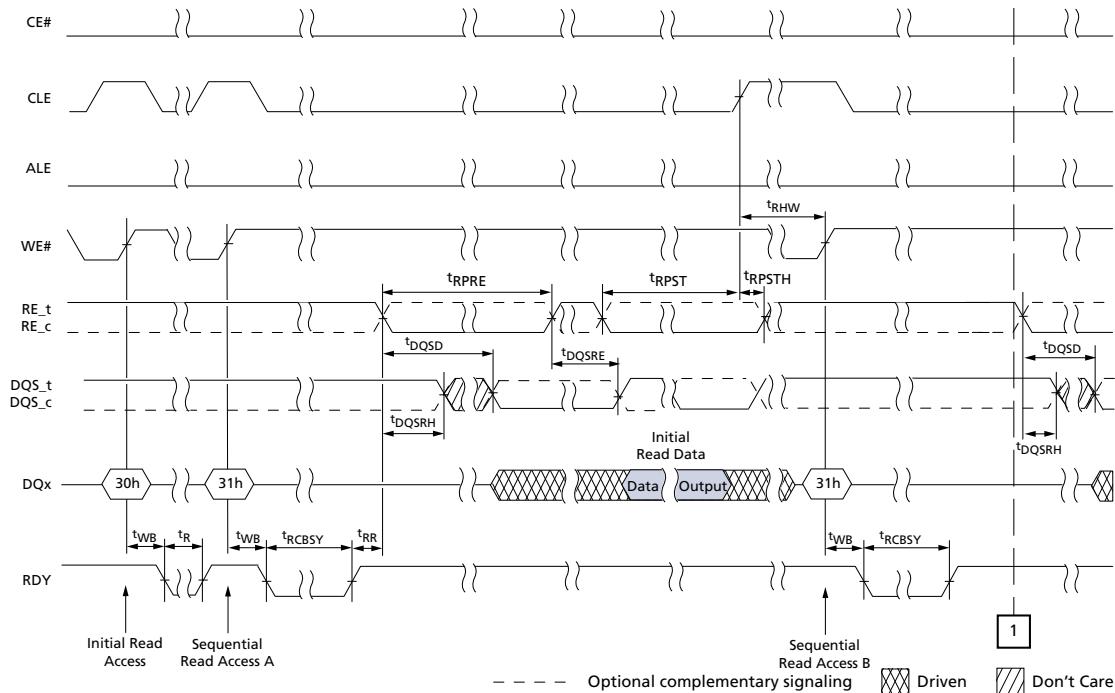


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 149: READ PAGE CACHE SEQUENTIAL (1 of 2)

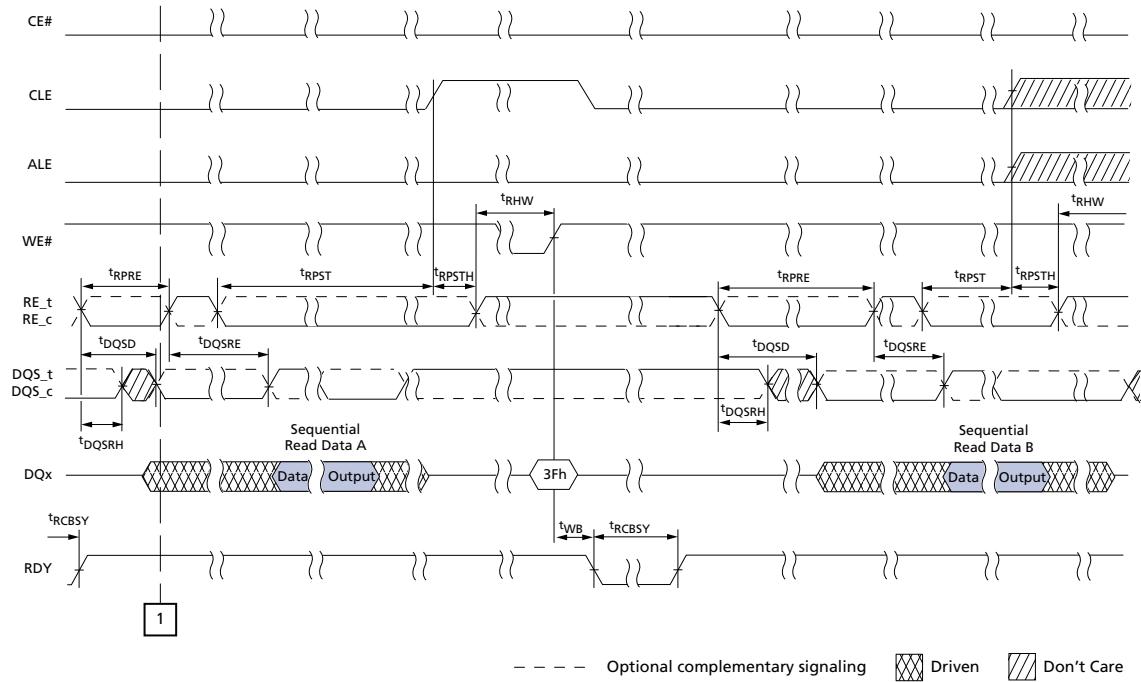


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 150: READ PAGE CACHE SEQUENTIAL (2 of 2)



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 151: READ PAGE CACHE RANDOM (1 of 2)

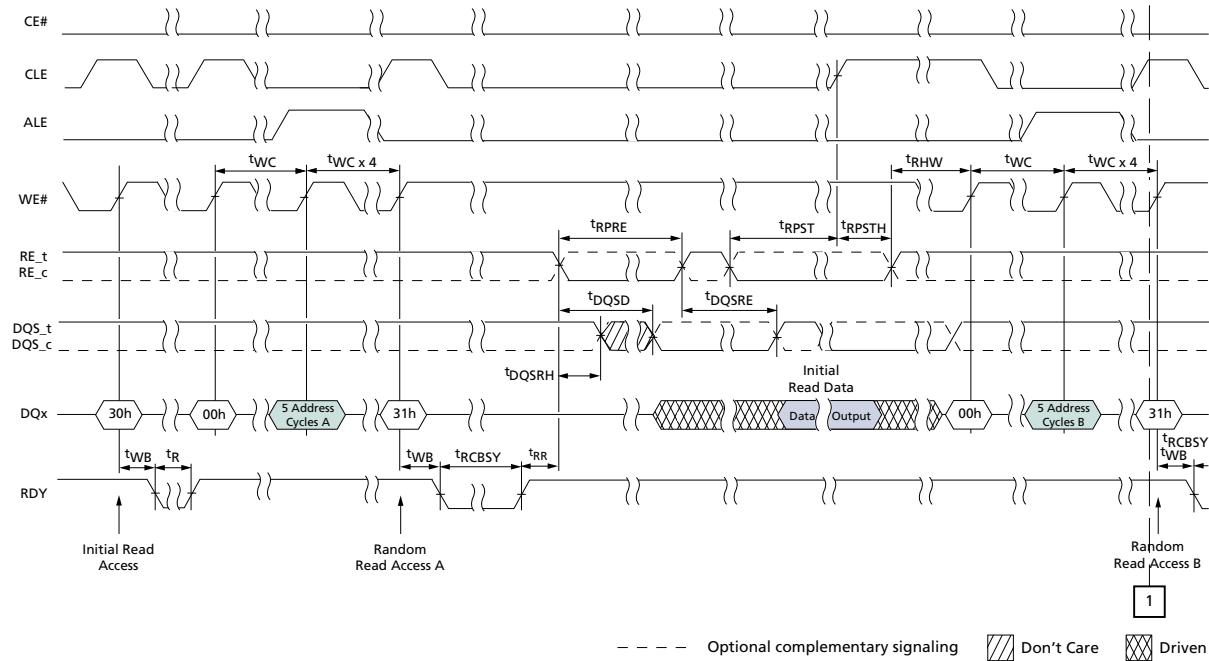
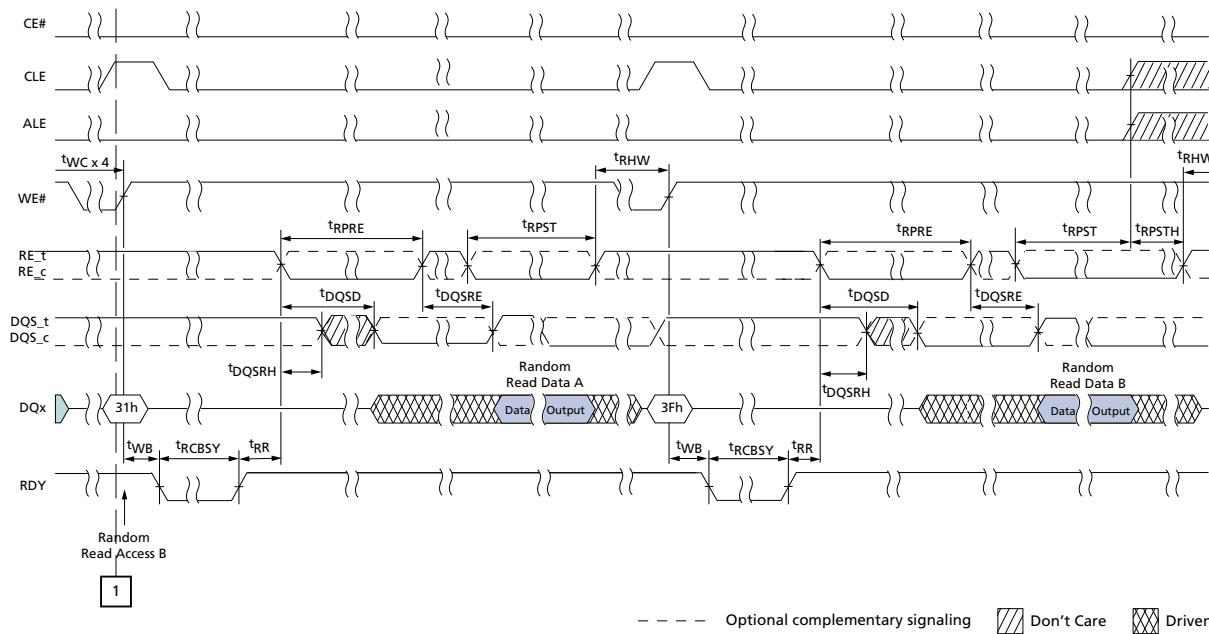


Figure 152: READ PAGE CACHE RANDOM (2 of 2)

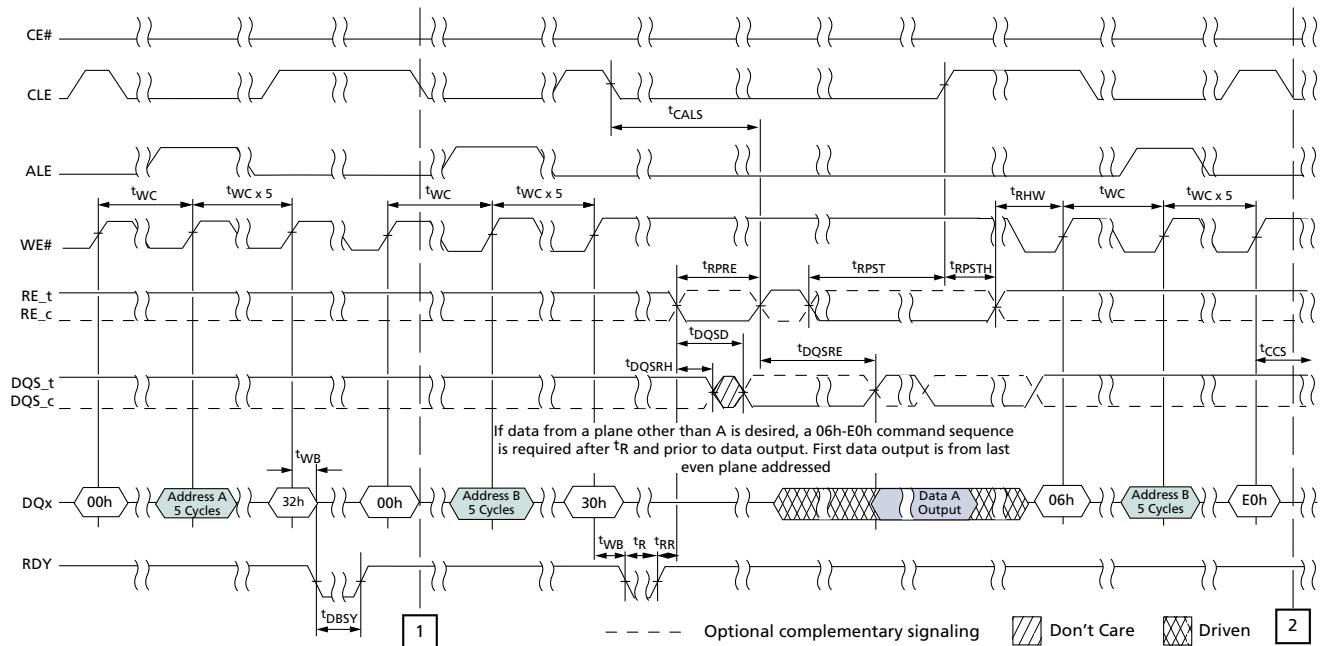


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 153: Multi-Plane Read Page (1 of 2)

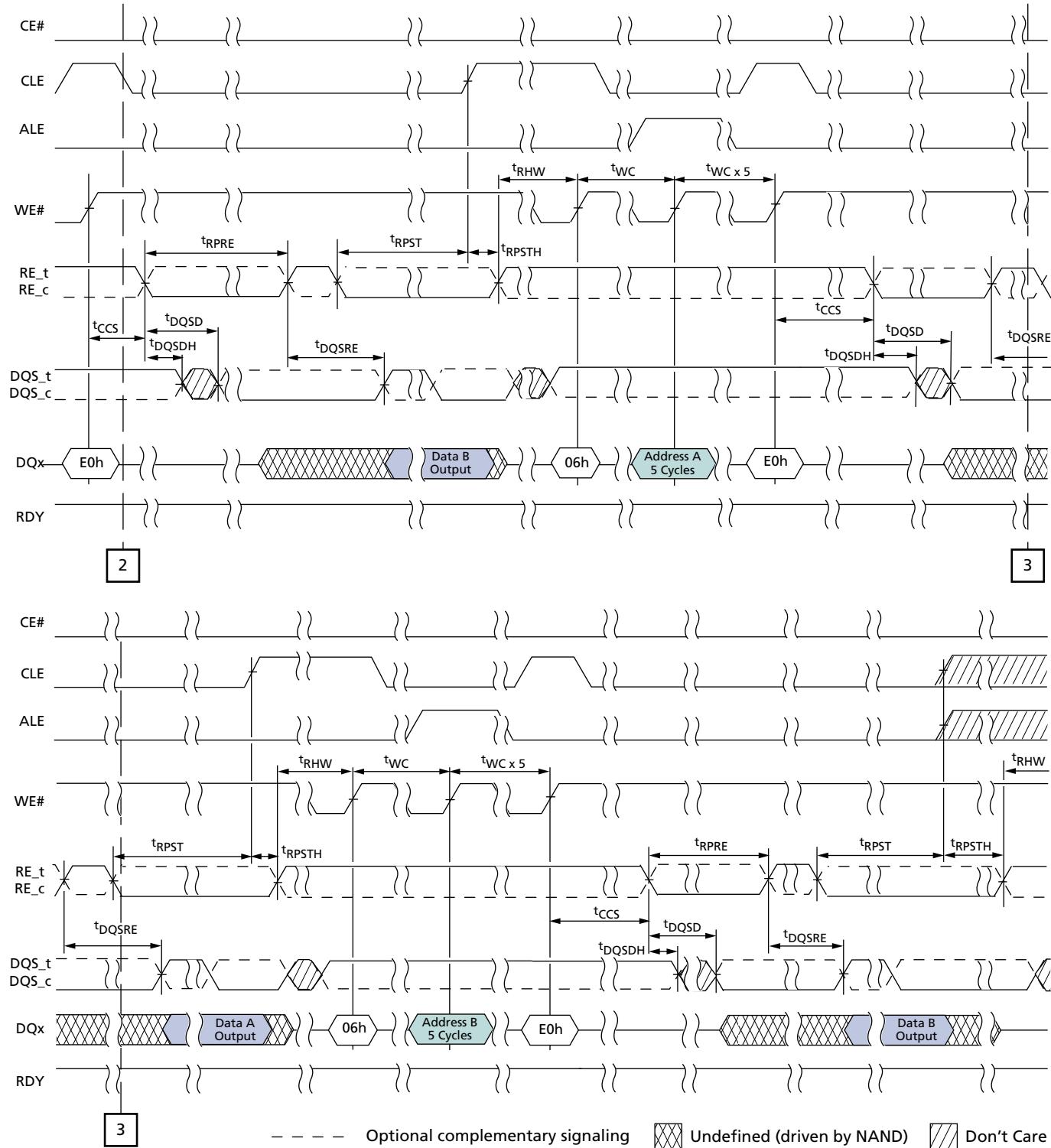


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 154: Multi-Plane Read Page (2 of 2)



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 155: PROGRAM PAGE Operation (1 of 2)

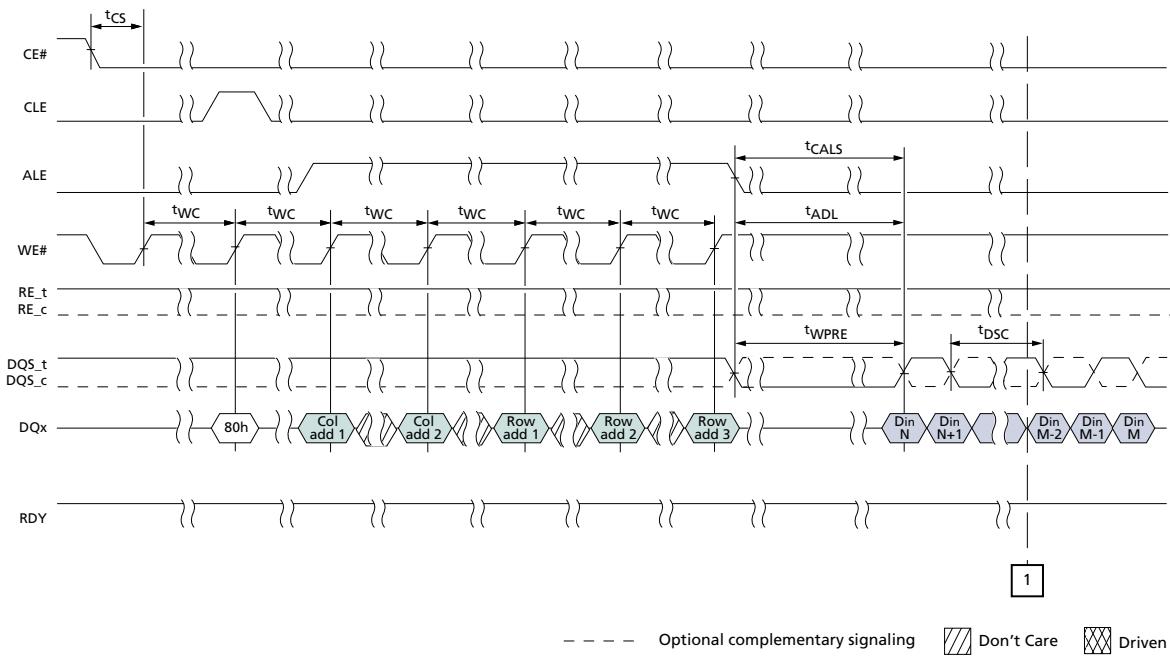
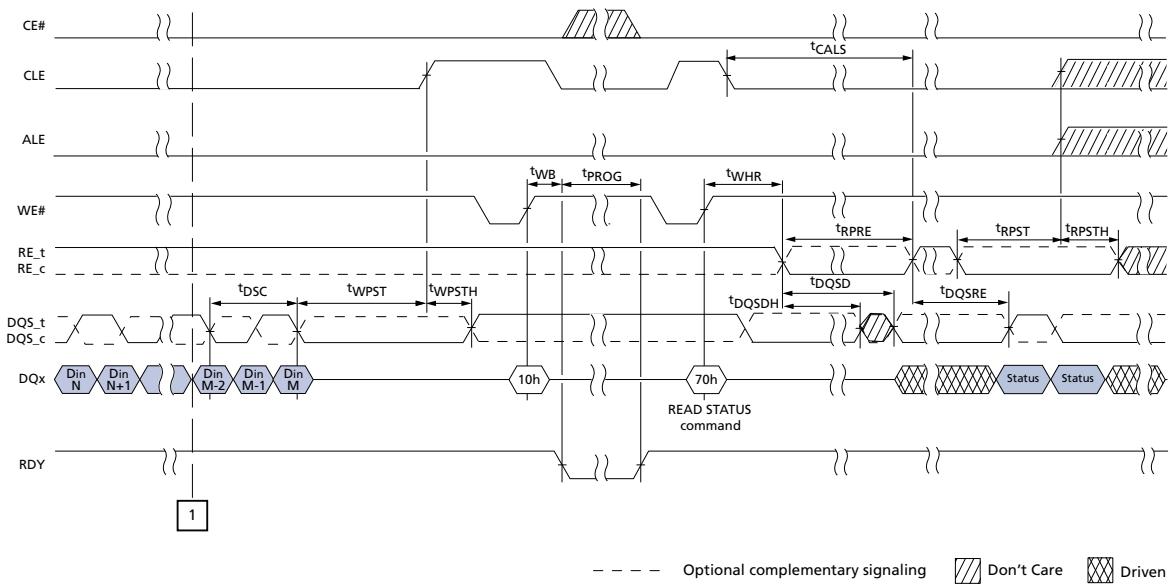


Figure 156: PROGRAM PAGE Operation (2 of 2)

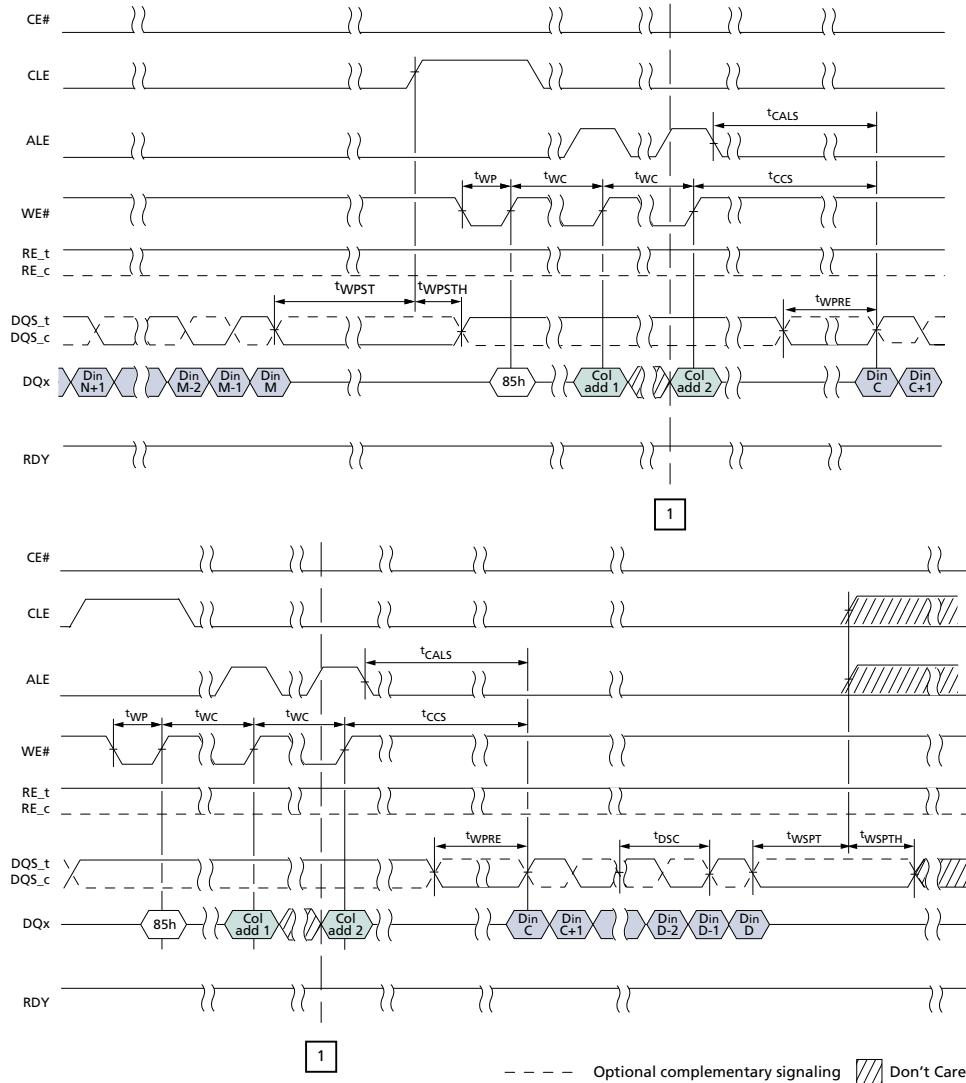


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 157: CHANGE WRITE COLUMN

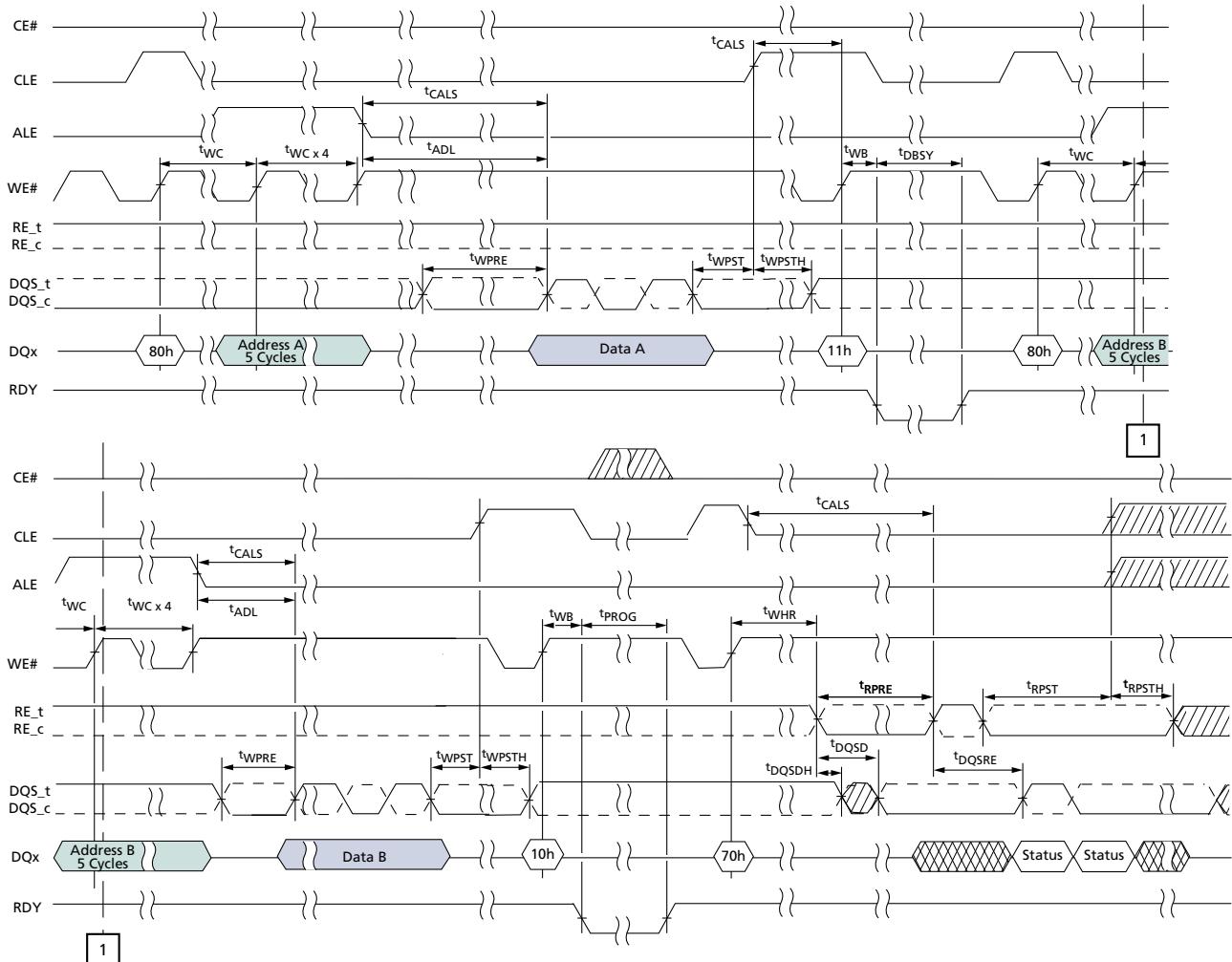


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 158: Multi-Plane Program Page

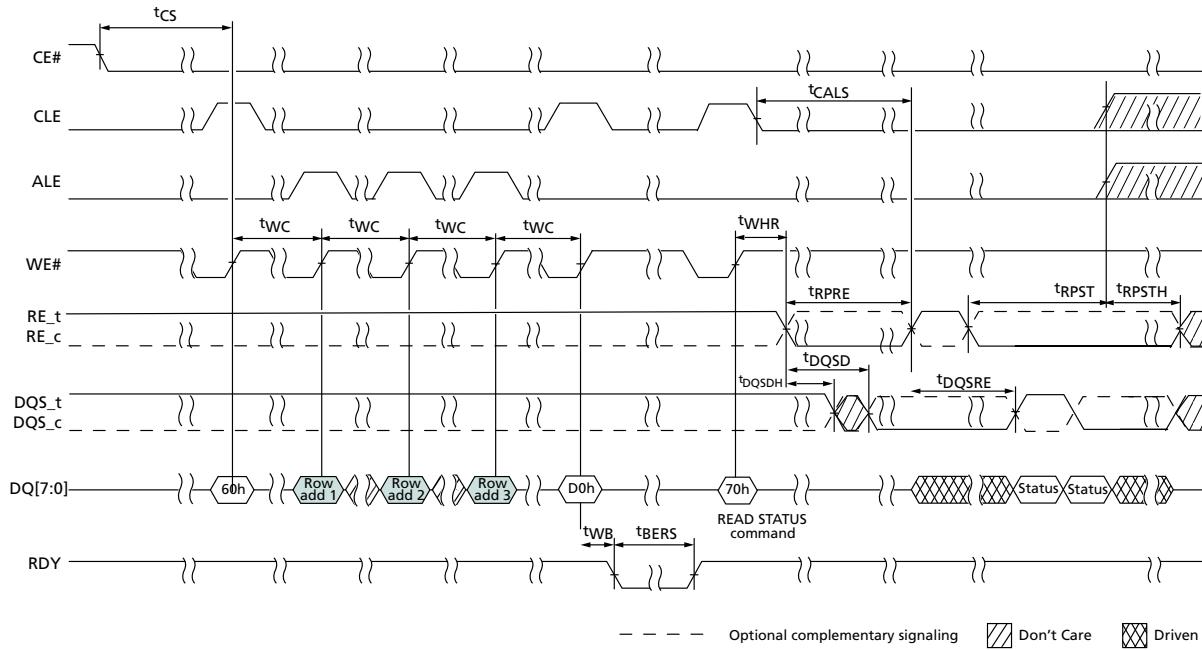


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 159: ERASE BLOCK



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 160: COPYBACK (1 of 3)

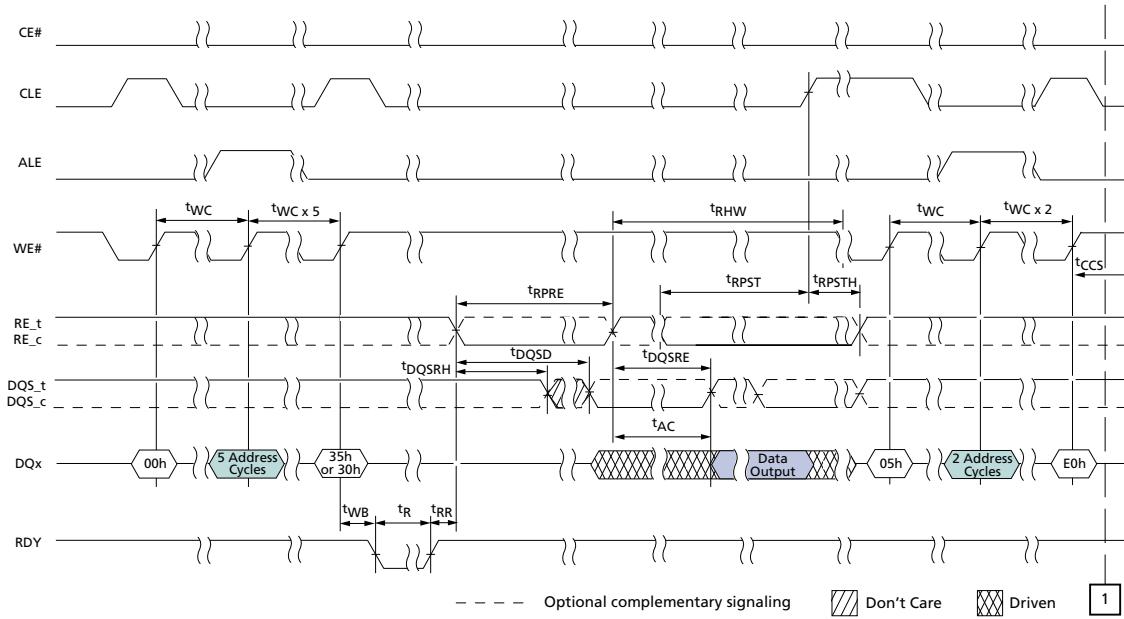
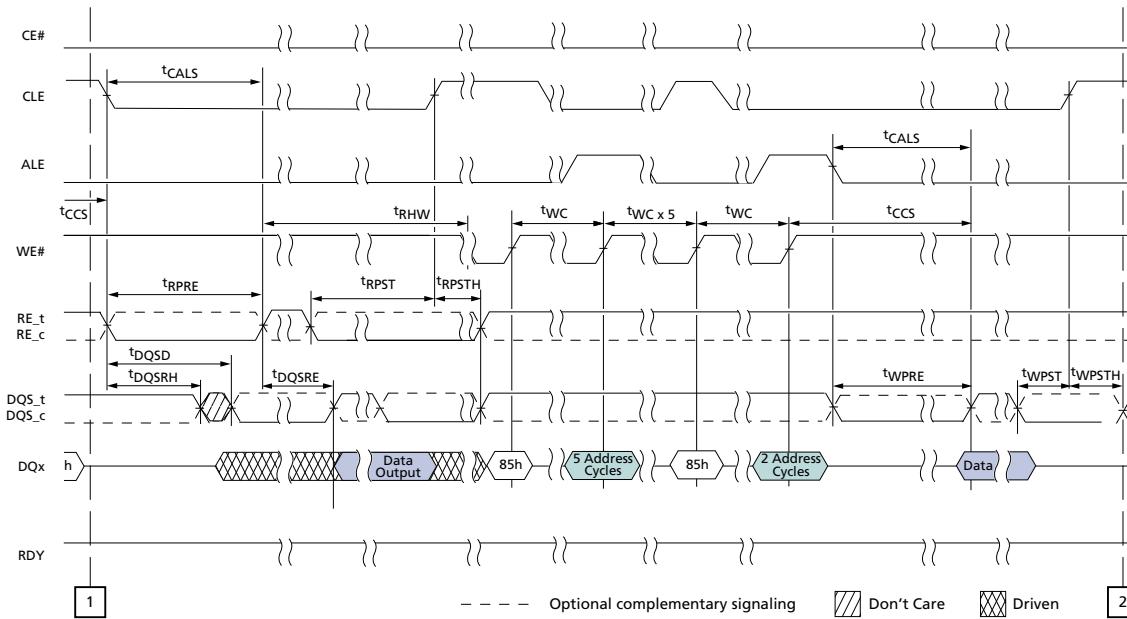


Figure 161: COPYBACK (2 of 3)

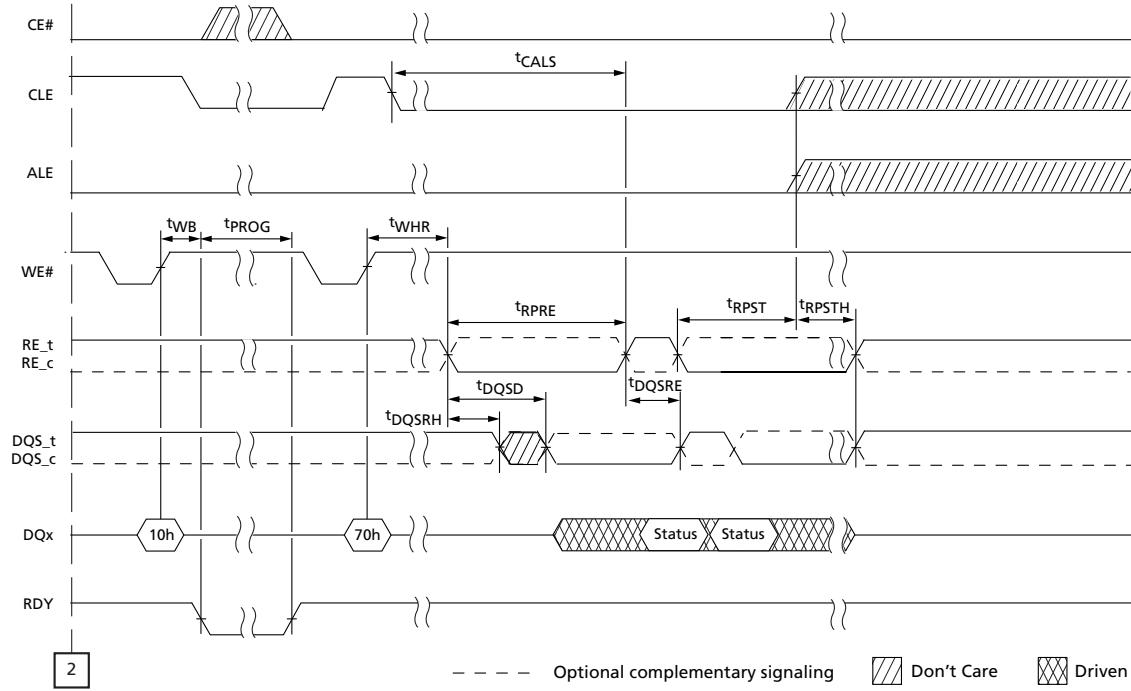


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 162: COPYBACK (3 of 3)

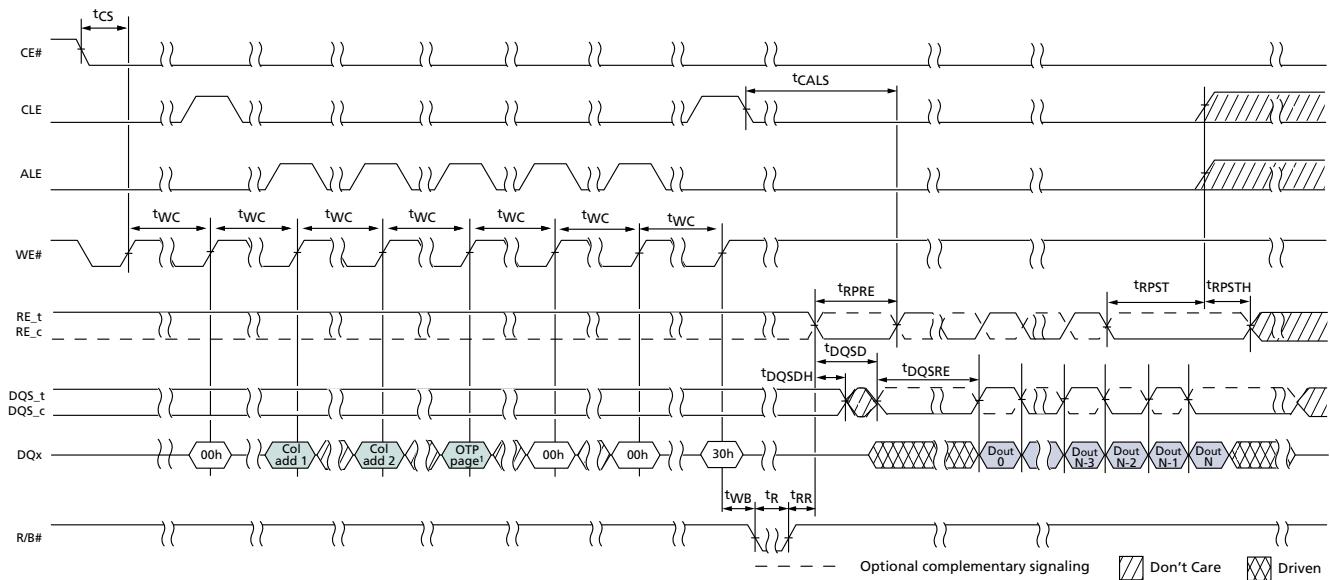


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 163: READ OTP PAGE



Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 164: PROGRAM OTP PAGE (1 of 2)

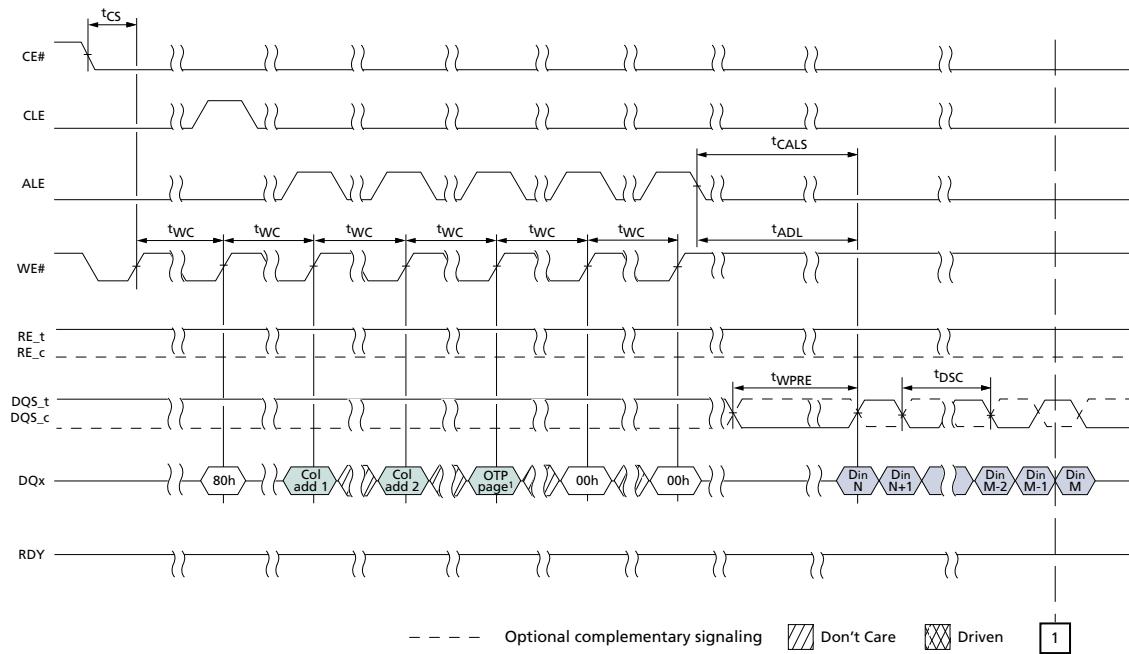
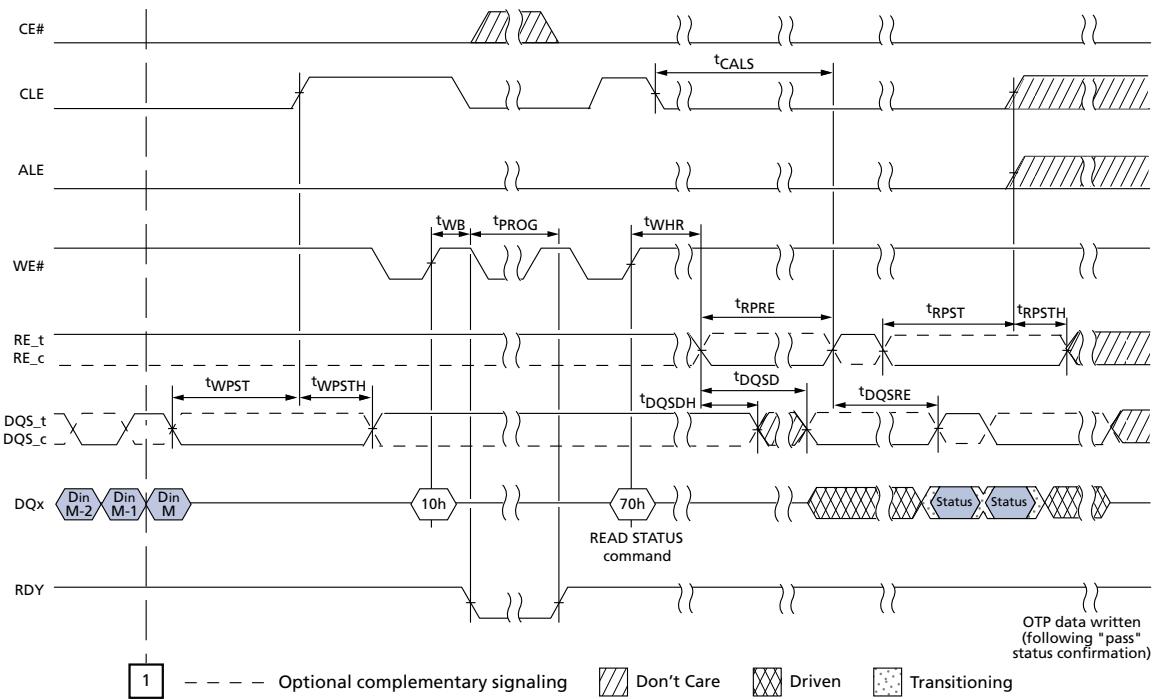


Figure 165: PROGRAM OTP PAGE (2 of 2)

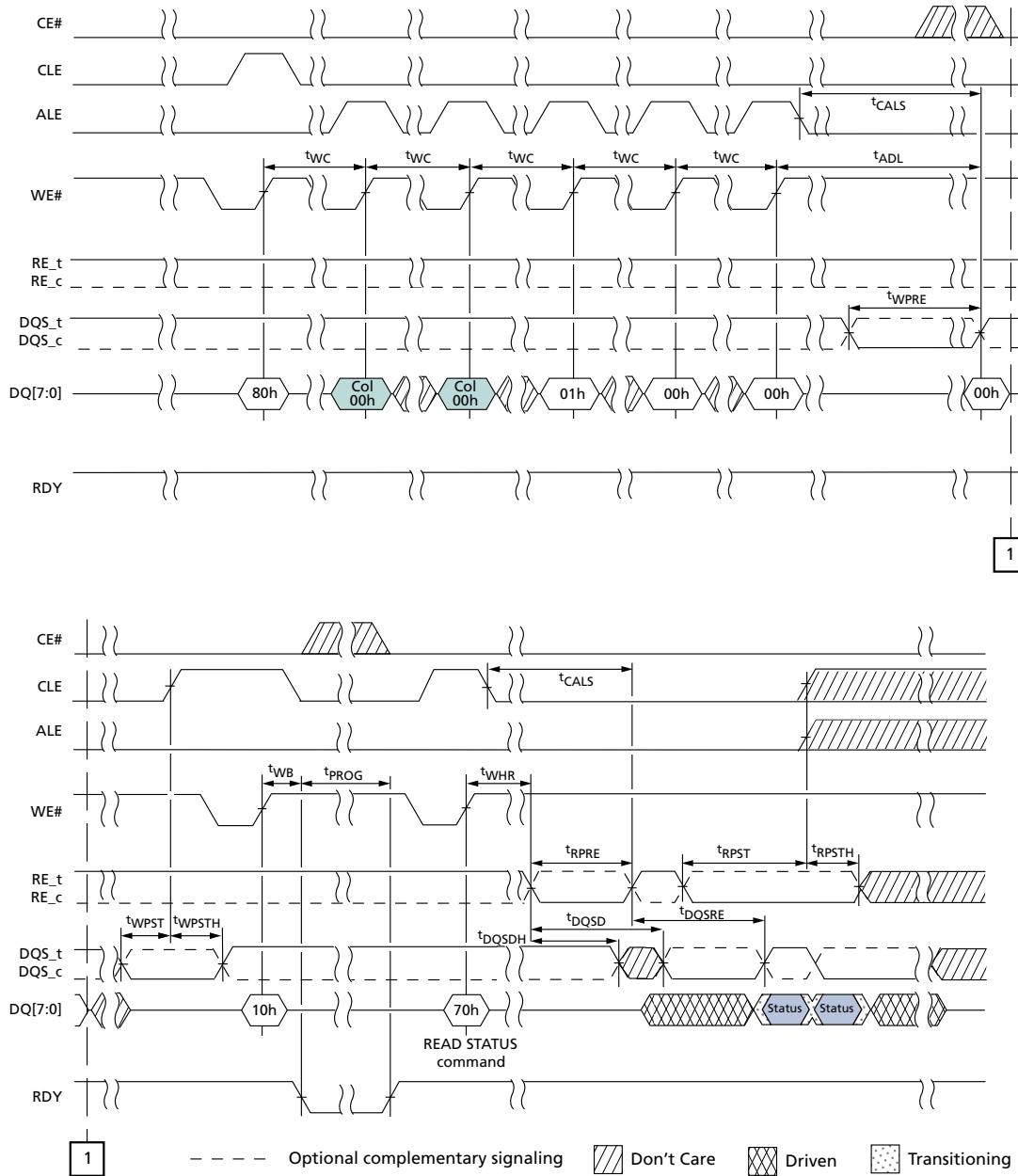


Release: 3/26/13



128Gb to 1Tb Asynchronous/Synchronous NAND NV-DDR2 Interface Timing Diagrams

Figure 166: PROTECT OTP AREA



Release: 3/26/13



Revision History

Rev. G – 3/13

- Updated Input Slew Rate derating tables for NV-DDR2 with respect to hold
- Updated t_{DH} and t_{DS} values for NV-DDR2 timing modes 5, 6, and 7
- Updated the following parameters in Electrical Characteristics section:
 - Added I_{CC4QR_A} , I_{CC4QW_A} , I_{CC4QR_S} , and I_{CC4QW_S} parameters
 - I_{CC5_A} TYP to 5mA and Max to 7mA

Rev. F – 2/13

- Added support for 1.8V/3.3VV_{CCQ} device and related information
- Changed BGA package solder ball material definition to SAC405
- Updated 152-Ball LBGA – 14mm x 18mm (Package Code: H8) mechanical drawing
- Changes to ONFI/JEDEC Read Parameter Pages for BGA package capacitance, t_{PROG} Max, Vendor specific block section, and JEDEC Read Parameter Page additional byte definitions
- Updated Output Drive Strength Impedance Values ($V_{CCQ} = 1.7\text{--}1.95V$) table
- Defined V_{PP} Absolute Min and Max to -0.6V and 16V respectively
- Expanded V_{PP} operational range to 10.8V Min and 13.2V Max
- Updated Capacitance: 152-Ball BGA Package table values
- Updated the following parameters in Electrical Characteristics section:
 - I_{CC4R_A} TYP to 7mA
 - I_{CC4W_A} TYP to 8mA
 - I_{SB} Max to 75 μ A
 - I_{CC4R_S} TYP to 16mA for speeds up to 200MT/s
 - I_{CC4R_S} TYP to 25mA and Max to 30mA for speeds greater than 200MT/s
 - I_{CC4W_S} TYP to 16mA for speeds up to 200MTs
 - I_{CC4W_S} TYP to 25mA and Max to 30mA for speeds greater than 200MT/s
 - I_{CC5_S} TYP to 6mA
- Updated the following parameters in Array Characteristics section:
 - t_{CBSY} TYP to 1100 μ s
 - t_{CBSY} and t_{PROG} Max to 3000 μ s

Rev. E – 8/12

- Changed MT29F1024G08CUCAB part number to MT29F1T08CUCAB
- Updated VBGA, TBGA, and LBGA package drawings in Package Dimensions section for 0.55mm solder ball dimension
- Changed parameter I_{PP} to I_{PPA} and added parameter I_{PPI}
- Corrected V_{REFQ} Typ from 1.8V to 0.5 x V_{CCQ}
- Updated t_R and t_{RCBSY} Max to 115 μ s
- Updated t_{RCBSY} Typ to 26 μ s
- Updated t_{OBSY} Max to 50 μ s

Release: 3/26/13



- Changes to ONFI/JEDEC Read Parameter Pages:
 - Bytes 44–63 in ONFI and JEDEC Read Parameter Pages for new MT29F1T08CUCAB part number
 - Bytes 137–138/152–153 in ONFI and 157–158/159–160 in JEDEC Read Parameter pages for changes to tR Max

Rev. D – 2/12

- Increased page size to 17,600 bytes; updated array addressing figures accordingly
- Updated byte 3 of the Read ID for Address 00h to 3Ch
- Changes to ONFI/JEDEC Read Parameter Pages for:
 - Bytes 84–85 in ONFI and 84–85, 90–91 in JEDEC Read Parameter Pages for changes to page size
- Corrected typo in Share Pages table

Rev. C – 12/11

- Corrected 152-Ball BGA (Ball-Down, Top View) signal assignment figure K11 position to R
- Added address bit BA19 to Array Addressing for Logical Unit (LUN) table
- Added figure 'Example of Sequential Initialization' under CE# Pin Reduction and Volume Addressing section
- Added statement on bit-wise majority recovery of parameter pages under Read Parameter Page (ECh)
- Changes to ONFI/JEDEC Read Parameter Pages for:
 - Bytes 135–136 in ONFI and 155–156 in JEDEC Read Parameter Pages for $tBERS$ Max to 12ms

Added byte definition to byte 180 of the ONFI Read Parameter Page and byte 422 of the JEDEC Read Parameter Page for number of Read Retry settings supported
- Added 4 options (Options 4 to 7) to Feature Address 89h: Read Retry
- Added clarification regarding Volumes that share a Host Target which are configured to use different data interfaces under VOLUME SELECT (E1h) section
- Added parameter 'CEVDLY' in relation to VOLUME SELECT (E1h) command
- Updated Shared Pages table information
- Updated Output Drive Strength Impedance Values ($V_{CCQ} = 1.7\text{-}1.95V$) table
- Updated Output Slew Rates for $V_{OL(DC)}$, $V_{OH(DC)}$, $V_{OL(AC)}$, and $V_{OH(AC)}$ for Asynchronous/NV-DDR Interface
- Updated I_{SB} TYP to $15\mu A$ and Max to $70\mu A$
- Added I_{VREFQ} parameter
- Changed RE#/RE_t, RE_c, and W/R# signal definitions from Inputs to Inputs/Outputs for purposes of capacitance in table Capacitance: 152-Ball BGA Package
- Changes to Array Characteristics:
 - Changed NOP for OTP operations to 2
 - Changed $tBERS$ Max to 12ms
 - Changed $tPOR$ Max to 2ms

Release: 3/26/13

**128Gb to 1Tb Asynchronous/Synchronous NAND Revision History**

- Added note for tR Max for options 4 to 7 of Read Retry

Rev. B – 8/11

- Corrected 152-Ball BGA (Ball-Down, Top View) signal assignment figure C12 position to DNU
- Added Read Retry options

Rev. A – 7/11

- Initial release

Release: 3/26/13

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
www.micron.com/productsupport Customer Comment Line: 800-932-4992
Micron and the Micron logo are trademarks of Micron Technology, Inc.
All other trademarks are the property of their respective owners.
This data sheet contains initial descriptions of products still under development.