KLE TECHNOLOGICAL UNIVERSITY

School
of
Electronics and Communication Engineering

Minor Project
on

12-BIT SUCCESSIVE APPROXIMATION REGISTER ADC

By:

1. **Divya Hegde** USN:01FE20BEC091
2. **Kavya Hegde** USN:01FE20BEC093
3. **Soumya H J** USN:01FE20BEC097
4. **Vaishnavi Shetti** USN:01FE20BEC101

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Under the Guidance of

Dr.Sujata S Kotabagi

K.L.E SOCIETY'S
KLE Technological University,
HUBBALLI-580031

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School of Electronics and Communication Engineering

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Dr.Sujata Kotabagi	Dr.Nalini Iyer	Dr.Basavaraj Anami
Guide	Head of School	Registrar

External Viva:

Name of Examiners	Signature with date
1. Sujata Kotabagi	12/06/2023
2. Shashidhar N	

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-Divya Hegde , Kavya Hegde , Soumya H J , Vaishnavi Shetti

ABSTRACT

The project presents a 12 bit , 100MSPs successive approximation resistor analog to digital converter(SAR ADC). It uses bootstrapped switch for sampling the input signal and resistive DAC for converting digital signal back to analog signal. In sample and hold circuit, the bootstrapping action reduces the distortion and improves the speed with minimal power penalty. The input voltage range achieved is 0V to 0.7V. The comparator circuit used in ADC is designed using 7 pack opamp of 150 MHz. Two levels of shift registor are used to design SAR logic circuit for 12 bits. Individual processing blocks are sequentially arranged for simulation. Measurement result showed that the ADC could work for given input range with variation of 6 percent variation in the result. The SAR ADC prototype is implemented in 180nm CMOS technology.

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Chapter 1

Introduction

Digital blocks have become more popular than analog blocks in IC designs because to their ease of processing, simplicity in design, precision, and low power consumption. ADCs are practically always used for converting, processing, and storing an analog signal as a digital signal. Different ADC architectures are in use. Flash ADC, SAR ADC, Sigma Delta ADC, Pipeline ADC, etc. are some examples of ADC architectures. SAR ADC seems to work well because it is fast, power-efficient, and has good resolution. For the architecture's DAC, the SAR Register generates an approximated digital value. The DAC converts the estimated digital value, and the resulting analog values are contrasted using a comparator. Low area consumption, moderate resolution, and reduced complexity are just a few benefits of SAR ADCs. The typical sample rate and resolution of SAR ADCs are 10 MSPS and 8–16 bits, respectively. Utilising 180nm Cadence Technology, 12 bit ADC design is completed.

1.1 Motivation

Due to a rise in bandwidth demand brought on by quicker on-chip processing and denser circuitry, serial input/output (I/O) data rates have topped 10Gbits/second (Gb/s). Analog-to-digital converter (ADC) based receivers with digital signal processing (DSP) are becoming more popular. In addition to ADCs, digital-to-analog converters (DAC) are in high demand.DACs convert discrete digital signals into continuous analogue impulses. Capacitive DACs are the preferred DAC architecture because of its simplified power, improved matching, and simpler construction. Capacitive DACs are only recommended over resistive and current steering DACs in situations needing medium to high resolution. The Capacitive DAC-based approach has a lot of benefits, but there are still issues with parasitic capacitance, capacitor mismatch, and capacitor sizing that affect DAC performance. Digital solutions will become more flexible and portable between IC fabrication processes as technology develops, which will ultimately result in lower power and cost.

1.2 Objectives

- To design a low power 12 bit SAR ADC with high conversion speed in 180nm technology.
- The SAR ADC has to be designed supporting low input voltage range.

1.3 Literature survey

In order to understand the existing works in the context of the proposed idea, some papers are discussed below.

[1]The cited work describes a differential non-linearity calibration technique to make up for the parasitic capacitance of the bridge capacitor's linearity loss.

[2]The paper presents a widely reconfigurable piecewise-linear ADC for information-aware quantization. Here, a two-step SAR-ADC with a highly customizable transfer function is given in order to analyse the trade-offs between adaptability, acquired resolution, and resource overhead.

[3]The selected work presents important SAR ADC optimising techniques. Some recent improvements in the speed and/or power of the SAR ADC design.Numerous studies attempted to enhance the parameters of SAR ADCs bySome increased their speed and energy efficiency by including CDAC, while others fixed their low SNDR problem by designing their amplifiers.This document has been enhanced as a result.

[4]In the cited paper, a High Speed 180nm CMOS Cryogenic SAR ADC is proposed. Here, an 8-bit SAR ADC is intended for space communications transceivers.The proposed SAR ADC's integer-based DAC architecture provides fast speed and great linearity.

[5]An Uncalibrated The cited publication also contains 12-bit 50-MS/s Full-Analog SAR ADC With Feedback Zero-Crossing Detectors. The study reported here incorporates comparator, SAR logic, and DAC switches into a multiple feedback zero crossing detector to provide a 12 bit, 50 MS/s complete analogue SAR ADC in 40 nm CMOS. The ADC is displayed without calibration.

[6] The mentioned research presents a 26uW 8 bit 10MS/s Asynchronous SAR ADC for low energy radios. a versatile, low-energy radio that features an asynchronous SAR ADC.Here, a variety of power-saving techniques are introduced in order to achieve good power efficiency for a moderate resolution.

[7]The article describes a DTMOS-based 16 bit 100 MS/s SAR ADC for biomedical implant systems with a 1V power supply. DTMOS logic uses little electricity.This device consists of a digital SAR logic with low leakage, an R-2R DAC, and a low power comparator.

[8]The cited research presents a 130nm 4GS/s 8-bit time-interleaved SAR ADC with an energy-efficient architecture. Here, an efficient SAR ADC implementation is achieved by the use of an optimised comparator architecture that includes background dc offset calibration, noise and asynchronous clock control, and noise reduction.

1.4 Problem statement

"Design a 12-bit , 100MS/s Successive Approximation Reigister Analog to Digital Converter (SAR ADC) using bootstrapped switch in 180nm technology for low power application."

1.5 ADC Performance Parameters

- Resolution: The smallest incremental voltage that an ADC can detect and consequently produce a change in digital output is referred to as the resolution of the ADC. It is referred to as the amount of bits the ADC outputs.

- Offset Error :It is visible when the DAC produces an output while the input is 00000000. Because of this, the output curve and the ideal output curve are not regularly matched.

- Gain error :Once the offset error has been removed, the difference between the ideal and actual curves at full scale is referred to as the gain error.

- Accuracy :How many bits are reproducible from conversion to conversion is referred to as a converter's accuracy. In other words, accuracy measures how accurately the ADC's output corresponds to the input.

- Integral nonlinearity Error: The integral nonlinearity error is defined as the deviation from the ideal straight line after offset and gain errors have been taken into account. Traditionally, the "best fit" straight line linking the first and last code transition endpoints is used to establish the straight(ideal) line.

- Differential nonlinearity error (DNL): It is the difference between the actual code width of an ideal converter and that of a non-ideal converter.

- Missing codes: The output code that is missing from the transfer function when no input voltage value can produce the intended output code is known as the missing code.

- Dynamic Range: The ratio of the converter's largest output signal to its smallest output signal (1LSB) is known as the dynamic range. The following equation can be used to represent dynamic range as ahown:

  Dynamic rang=20log10(ratio).

- Signal to noise ratio(SNR):The ratio of the strength of the fundamental to the overall noise power minus the hormonic components is known as the signal to noise ratio. It is written in database. The SNR covers all of the Nyquist interval's noise. It might be influenced by the incoming signal's frequency.

  It can be mathematically written as:

  SNR=10log(SignalPower/total noise floor power)

- Signal to Noise plus Distortion(SNDR):The fundamental to total noise plus harmonic power ratio is known as the SNDR.It is written in database. Mathematically it can be written as

  SNDR=10log(SignalPower/noise+Harmonic Power)

- Effective Number of Bits(ENOB):The highest signal to noise + distortion ratio is calculated by ENOB using bits.The relation between SNDR in db and ENOB is

  ENOB=(SINADdb-1.76)/6.02

- Total Harmonic Distortion(THD):THD is defined as the fundamental power divided by the total power of harmonic distortion.It is expressed in db.

  THD=10log(SignalPower)/(noise +Total Harmonic Power)

- Spurious Free Dynamic Range(SFDR):The difference between the strength of the signal and the strongest spurious frequency component is used to determine the SFDR.The SFDR is often stated in db. Mathematically it can be expressed as

  SFDR=10log(Signal Power)/(Power of largest spurious frequency)

1.6 Advantages of SAR ADC

SAR ADC is superior to other types of converters in the following ways:

- When compared to other designs, SAR ADC has a high speed.
- The SAR ADC's power consumption is extremely low due to the architecture's design.
- Because of these characteristics, ADCs are perfect for a wide range of applications, including data capture for medical imaging, industrial process control, battery-powered equipment, and many more.

1.7 Applications of SAR ADC

- Consumer electronics, communications, and the automotive industries all use SAR ADCs.
- The SAR ADC architecture is a popular choice for data acquisition systems that are widely utilised in optical communication, industrial process control, and medical imaging.

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Chapter 2

System design

The overview and functionality of individual components of SAR ADC has been discussed in this chapter.

2.1 Functional Block Diagram

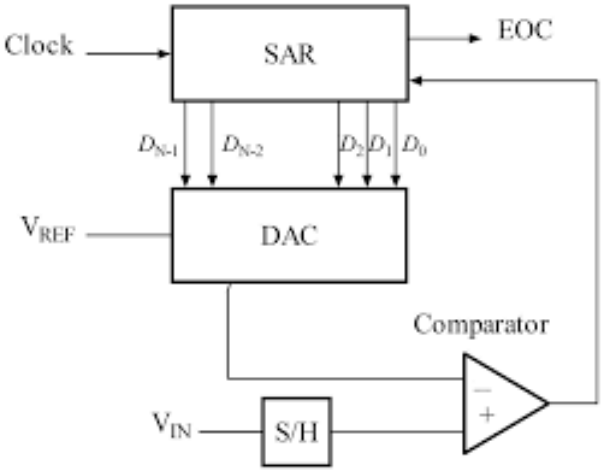

Figure 2.1: Functional Block Diagram [8]

Approximation Successive The suggested design uses a 12-bit register ADC. The voltage at the analog input is maintained by the Sample and Hold circuit. The SAR ADC makes use of the binary search methodology. First, a value with the MSB bit high is allocated to the 12-bit register. Consequently, the output of the DAC will match the reference voltage. A comparison is performed if the input voltage is either smaller than or greater than the DAC output. If the input voltage is greater than the DAC output, the comparator output is a logic 1 or high, and the MSB of the N-bit register remains 1. If the input voltage is lower than the DAC output, the comparator output is a logic 0 or low, and the register's MSB is cleared. The SAR control logic initially pushes the next bit to repeat the previous step before moving on to the next one. This has been true up until the LSB. The conversion is complete after the last cycle, and the register now holds a 12-bit digital word. The design as a whole consists of 5 blocks. The SAR logic block, Comparator, Digital to Analog Converter (DAC), Shift Register, and Sample and Hold Circuit are specifically mentioned.

2.2 Functional Block Diagram

It consist of 4 main blocks

1. Sample and Hold Circuit
2. Comparator
3. DAC
4. SAR Logic Block

2.2.1 Sample and Hold Circuit

An essential part of analog-to-digital converters (ADCs) are bootstrapped samplers. With little power loss, the bootstrapping procedure lowers the distortion and increases speed. The Sample and Hold circuit shown in the figure 2.2 is an electronic device that creates voltage samples from input and then holds those samples for a set period of time. The sampling time refers to the period of time when the sample and hold circuit generates a sample of the input signal. Similar to this, holding time refers to how long the circuit keeps the sampled value in memory. The switch links the capacitor to the output of a buffer amplifier to sample the input signal. The capacitor is charged or discharged by the buffer amplifier to make the voltage across the capacitor almost equal to or proportional to the input voltage. The switch separates the capacitor from the buffer when it is in hold mode. The circuit is intrinsically volatile because the capacitor is always depleted by its own leakage currents and usable load currents, but for all but the most demanding applications, the voltage drop within a given hold period is still within an acceptable error margin.

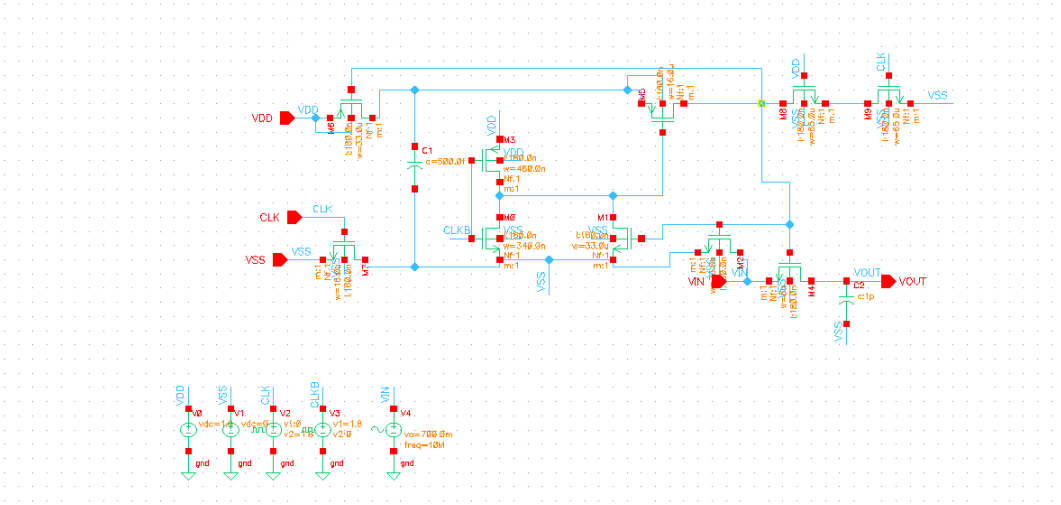

Figure 2.2: Bootstrapped Circuit

2.2.2 Comparator

Basically, the comparison of voltages requires this block. Vin and the voltage from the output of the internal DAC are the two voltages that it typically compares. The SAR register block receives the comparator output. The block represented in the figure 2.3 is incredibly important to the suggested architecture. Vref and Vin are the two voltages. Vin is the voltage that the Sample and Hold circuit gives to the comparator, and Vref is the input that the DAC block feeds to the comparator. The SAR logic block receives the comparator's output. The following

situation is simulated by this block: The comparator outputs '1' as vin surpasses Vref. A value of '0' is returned by the comparator if vin is less than Vref.

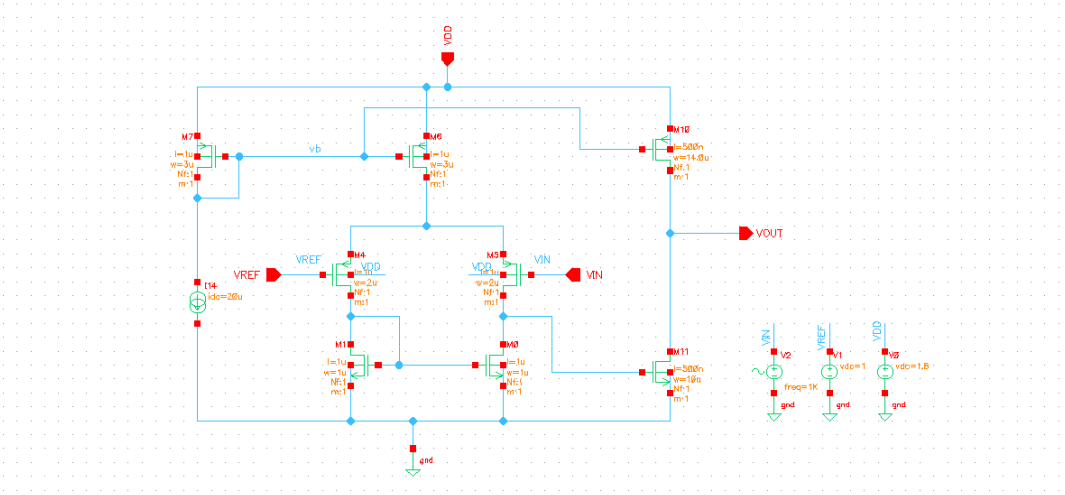

Figure 2.3: Comparator

2.2.3 Binary Weighted Capacitive DAC

Using binary weighted capacitors shown in the figure 2.4, a capacitive digital-to-analog converter is created. The DAC circuit diagram for ADC is shown in Fig. 4. When using a binary weighted capacitive DAC, each capacitor leg's value rises from C to 2N-1 C as you move from the LSB to the MSB. The method chosen to apply DAC produces the most accurate design out of all the possibilities that are available. Additionally, it can operate without op-amps. Additionally,there are other types of capacitive DAC, but only the binary weighted arrangement is used due to its output linearity. Compared to resistors, capacitors are much simpler to manufacture and can be duplicated much more precisely. Because this will raise the overall area of the DAC and subsequently the area of the ADC, the area of capacitors cannot be taken extremely large. Thermal noise value (KT/C) determines the lower limit of the capacitor area. The LSB of this noise should not exceed 50 percentage in order for the DAC to operate properly.

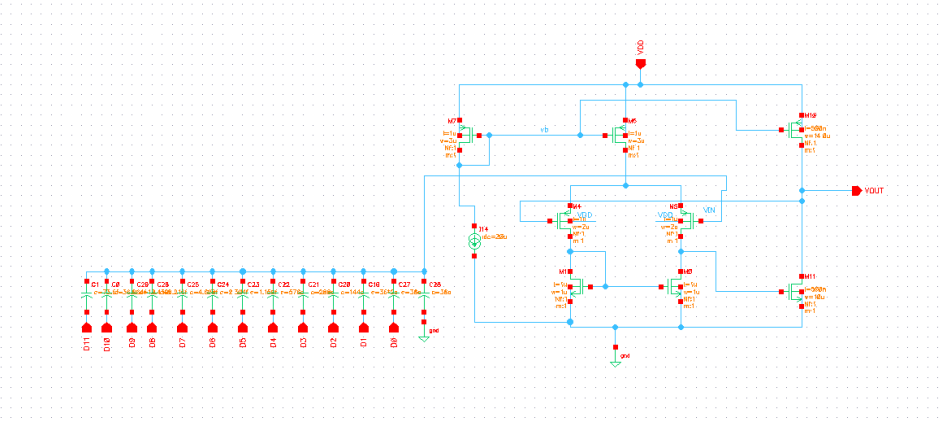

Figure 2.4: Binary Weigthed Capacitive DAC

2.2.4 R-2R DAC

Only two resistive values are used in the R-2R resistive ladder network. No matter how many bits are used to construct the ladder network, one resistor has the base value "R" and the second resistor has twice that value, or "2R".

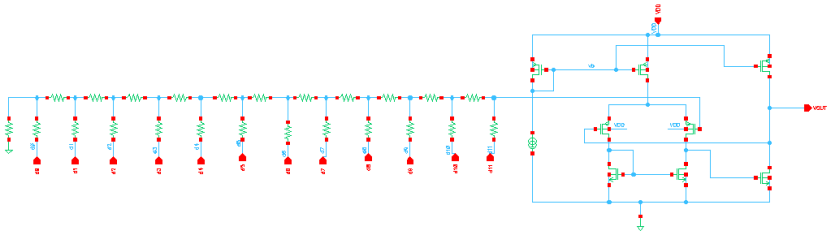

Figure 2.5: R-2R DAC

2.2.5 SAR Logic

The SAR logic block in figure 2.5, which consists of the D flip flop in figure 2.6, provides the approximate digital values for the DAC's digital input. The SAR logic block is built on the binary search algorithm. The clock rate of the SAR block is determined by the sampling frequency rate.

SAR block needs a clock frequency of 10 kHz to operate. The input signal (Vin) is sampled using sample and hold, and the sampled output is used as the comparator input. The MSB bit value is now set to "1" while the remaining bits are converted to "0" by the SAR circuit. The DAC transforms SAR digital bits into analog output voltage Vout (half of the reference voltage). The comparator's reference input is the analogue output from the DAC. The Vin sampled is put up against the Vout of the DAC. '1' is the comparator's output if Vin is greater than Vout of the DAC and '0' otherwise. SAR now establishes the MSB value and produces the resulting approximation bits based on the comparator's output. The loop is repeated until the LSB bit is found.

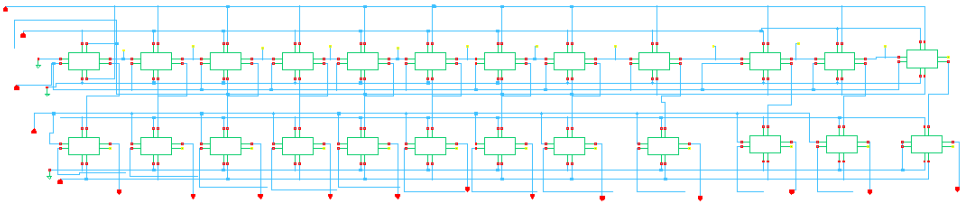

Figure 2.6: SAR Logic

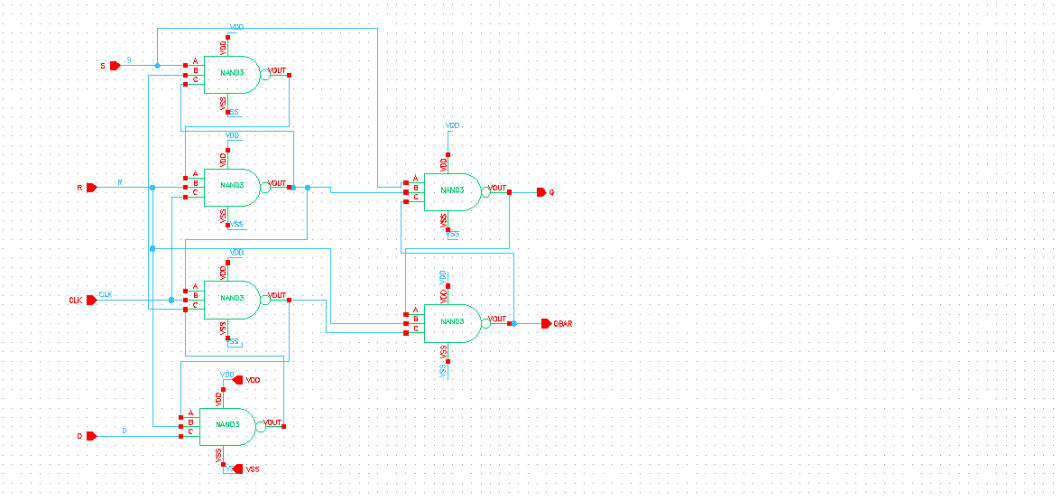

Figure 2.7: D flip flop

Chapter 3

Implementation details

This chapter contains specifications taken for design of SAR ADC,design algorithm and complete working of SAR ADC.

3.1 Specifications

- Design Specifications:
  - Sampling Rate -100MS/s
  - Resolution -12 bits
  - Power Supply -1.8V

3.2 Design Algorithm

- Sample and Hold:A sample and hold circuit captures the input voltage(vin) by holding the input signals for a period of time before delivering the output.Here we have used Bootstrapped sample and hold which serves as an integral component of analog-to-digital converters(ADCs).The bootstraping action reduces the distortion and improves the speed with minimal power penalty.
- Comparator: Compares sampled input voltage and the output of the DAC.When the output voltage of the DAC is greater than the input voltage,MSB of SAR changes accordingly.
- SAR: A SAR(Successive Approximation Register)circuit is implemented to supply an approximate digital code of vin to the DAC.The DAC receives the output from SAR logic as binary code,which is based on the current bit under inspection and the previously approximated bits.
- DAC:The DAC receives input from the SAR logic block and it converts digital data into analog.The output of DAC is again given to the input of the comparator.

3.3 Working of SAR ADC

Operation performed for each sample while designing ADC

1.Sample and hold circuit samples the analog input signal(vin).

2.The SAR logic block generates a binary code for each bit and sends it to the DAC block,which is normally based on the current bit and approximates the previous bit.

3.The comparator compares the two voltages and produce the result.

4.The End of Conversion(EOC) will be set to HIGH after all the bits have been approximated.

Chapter 4

Flow chart

4.1 Flow chart of the implementation of the project.

The flow chart shown in figure 4.1 gives the picture of sequential processes in data conversion. As the process starts the input analog voltage is sampled and at the same time the MSB of SAR logic is made high which is given as input to the DAC. The sampled value then is compared with DAC output to decide whether to keep the MSB high or low. The previous bit to MSB is then made high to compare with the input signal and the cycle continues until all the bits are checked to give corresponding digital value for the input analog signal. The process ends once the digital output is taken.

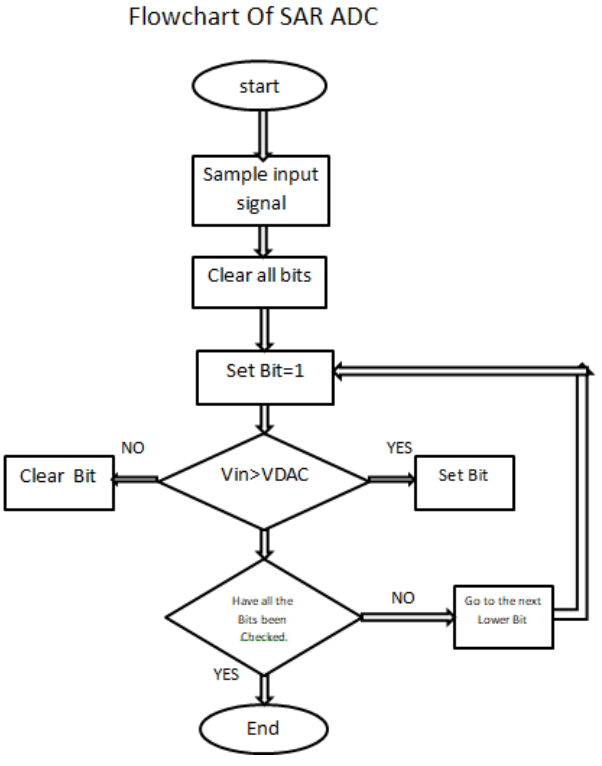

figure 4.1: Flow chart

Chapter 5

Results and discussions

The result of individual blocks have been discussed here.

5.1 Output of Sample and Hold

Here output functionality of sample and hold circuit is shown in figure 5.1. which is having sinusoidal input of 10MHz frequency sampled at the rate of 100MSPS and sample time of 5ns.

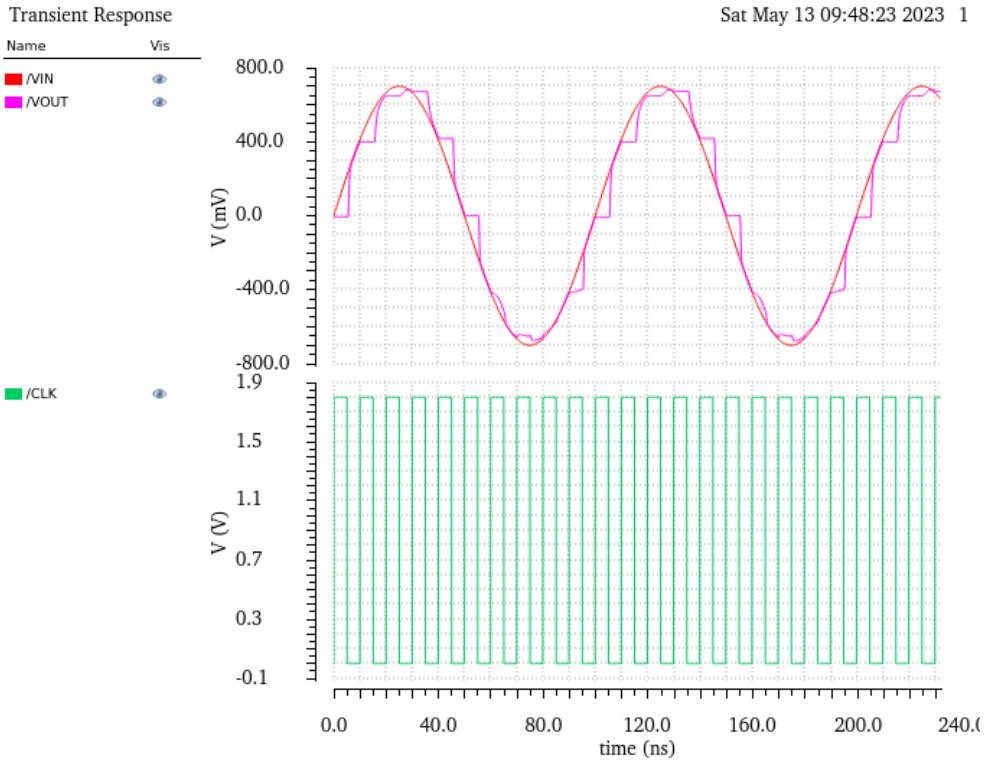

Figure 5.1: Sample and hold output

5.2 Output of Comparator

The Output of the comparator shown in the figure 5.2, which compares the input voltage with reference voltage with very minimal offset error .

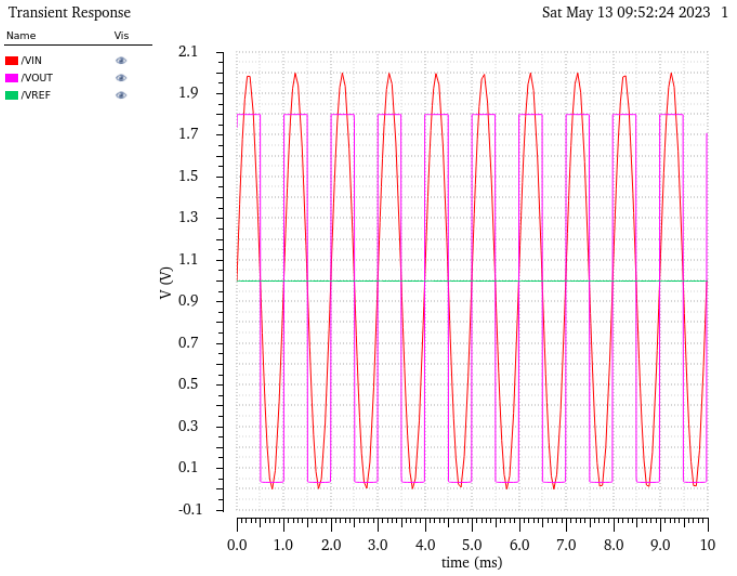

Figure 5.2: Comparator output

5.3 Output of DAC

The Binary Weighted Capacitive DAC output represented in figure 5.3, which converts digital data into analog signal.

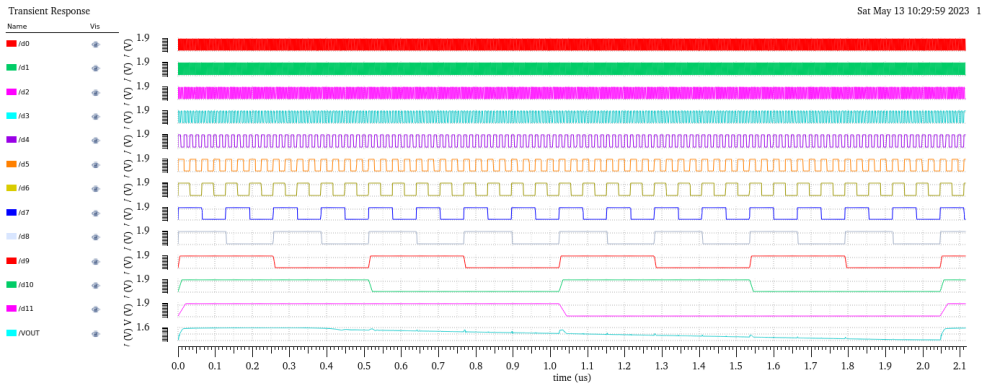

Figure 5.3: DAC output

5.4 Output of R-2R DAC

The Binary Weighted Capacitive DAC output represented in figure 5.3, which converts digital data into analog signal.

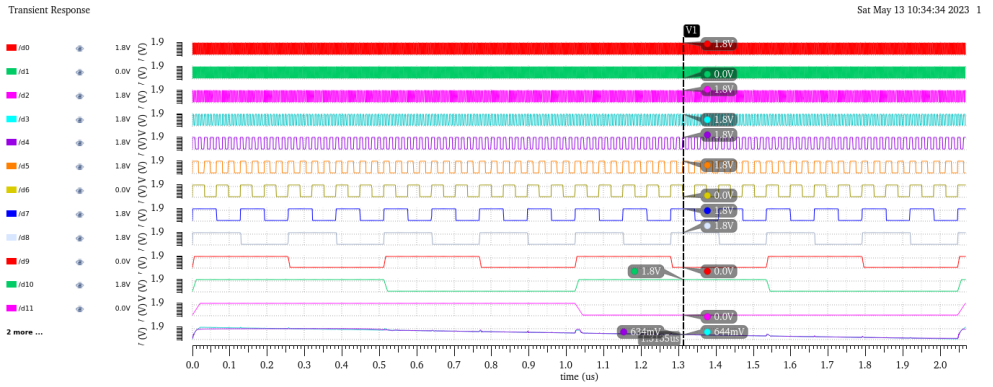

Figure 5.4: R-2R DAC output

5.5 Output of SAR logic block

The SAR logic output result represented in the figure 5.4 determines the digital output of the MSB based on the comparison result of the comparator.

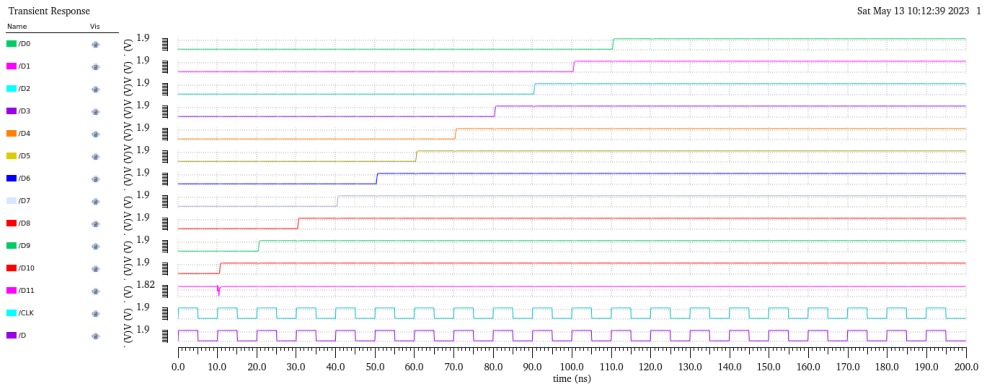

Figure 5.5: SAR logic output

5.6 Output of Complete SAR ADC

The figure 5.5 represents complete Output of SAR ADC, Converts analog input into appropriate digital data.

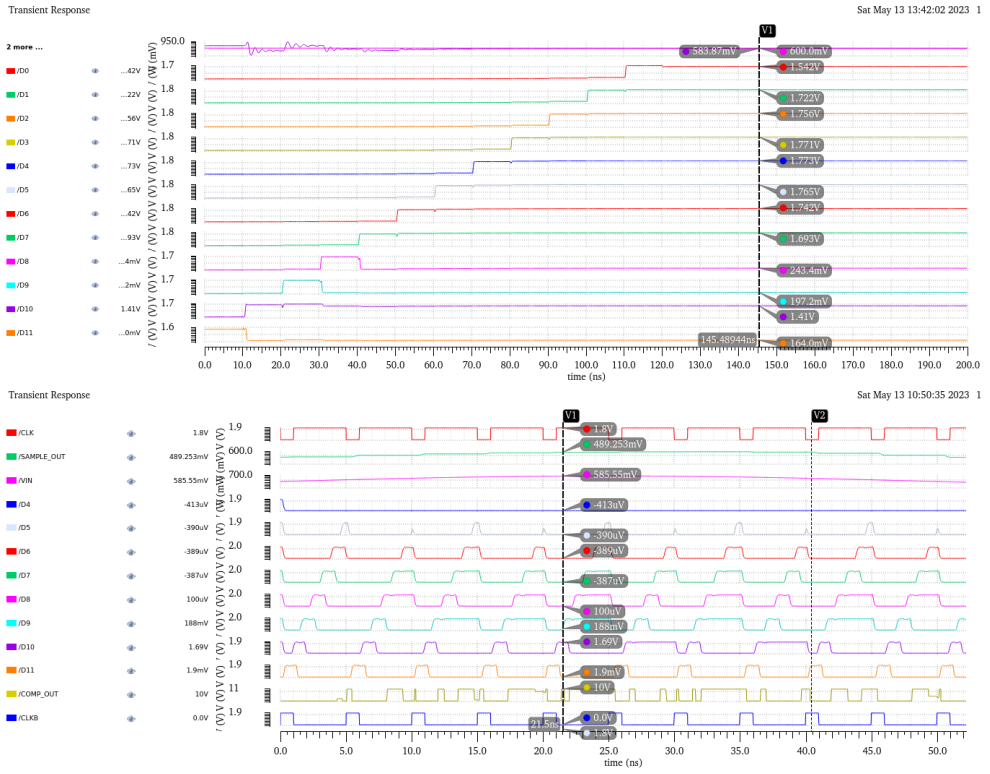

Figure 5.6: SAR ADC output

Chapter 6

Conclusions and Future scope

This chapter discusses about the conclusion and the future scope of the current project.

6.1 Conclusion

- In this project , a 12-bit, 100 MS/s SAR ADC is proposed.The design includes Bootstrapped Sample and Hold circuit and binary weighted capacitive DAC.
- In sample and hold circuit,the bootstraping action reduces the distortion and improves the speed with minimal power penalty which is the major requirement in today's industries.

6.2 Future Scope

- The design of Bootstrapped sample and hold circuit and resistive DAC are the critical aspects of SAR ADC design.
- In sample and hold circuit,the bootstraping action reduces the distortion and improves the speed with minimal power penalty which is the major requirement in today's industries.
- There are just a few methods that could potentially improve the performance of data converters. The input signal bandwidth for the entire ADC circuit will grow with further operational amplifier optimisation. Additionally, the digital sub-circuits can be optimised to use less power while maintaining good accuracy.
- Utilising a sample and hold buffer will result in a better sampled signal that can drive heavy loads. The data converter's sample rate can also be increased by using the time interleaved technique.

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