Name: Soumya H J
USN:01FE20BEC097
Project: 7 pack opamp design

Design Details

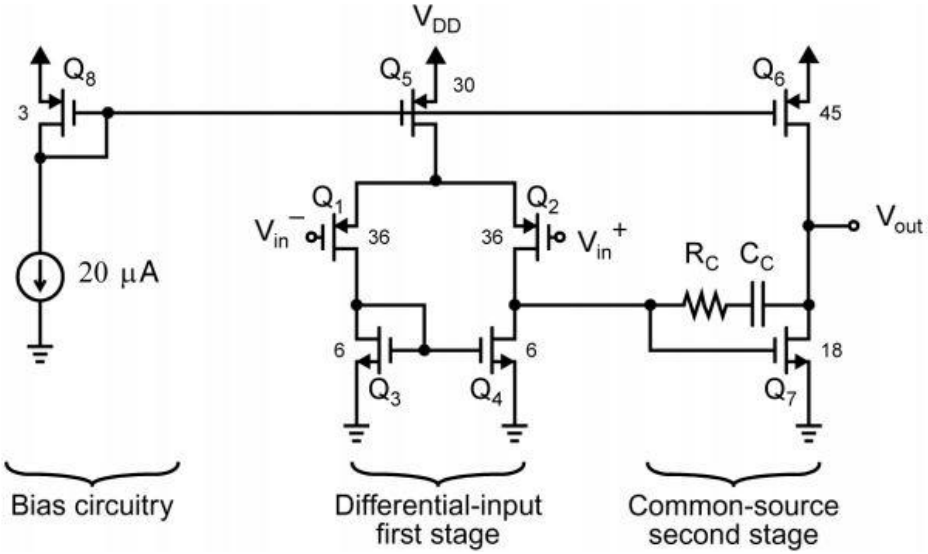
Cell Name	7_pack_opamp
Test Bench Name	7_pack_opamp_test
Technology	180nm TECHNOLOGY UMC_18_CMOS
Devices	MOSFET, CAPACITORS, VOLTAGE AND CURRENT SOURCE
Simulation Area	CADENCE
Design Owner	Soumya H J
Reviewed By	-
Acknowledging	Dr. SUJATA KOTABAGI , SCHOOL OF ELECTRONICS AND COMMUNICATION

Contents

- Design Details
- Pin Description
- Simulation plan
- SCM
- Schematic
  - Test bench
  - DC analysis
  - AC analysis

Two Stage Amplifier

- High gain and high output swing
- 1st stage : Differential amplifier
- 2nd stage: Common source with PMOS load , capacitive load
- Overall gain Av=A1*A2

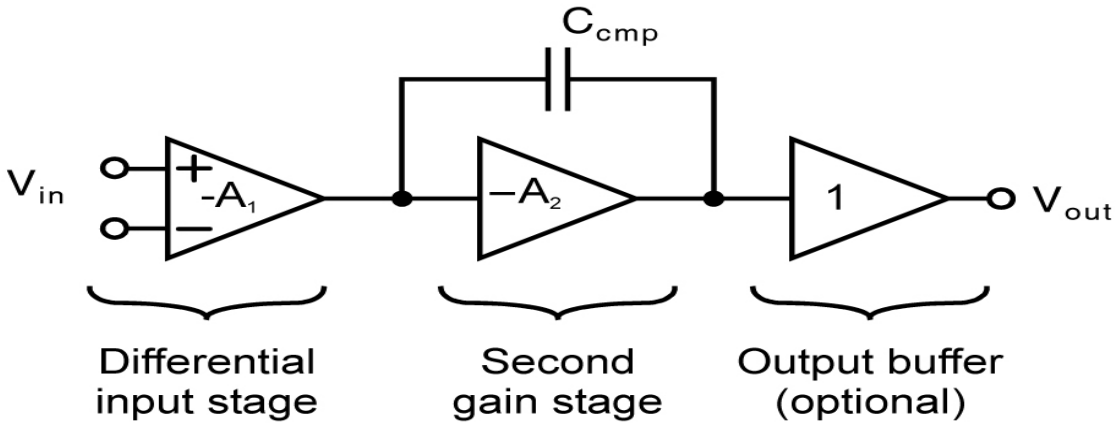


- Negative feedback increases oscillations
- Need for greater PM

Two Stage Amplifier

OP-AMP COMPENSATION :

- 2 pole system
- PM closes zero
- Millers Compensation
- C_c between the outputs of two stages
- Pole splitting
- Dominant pole compensation

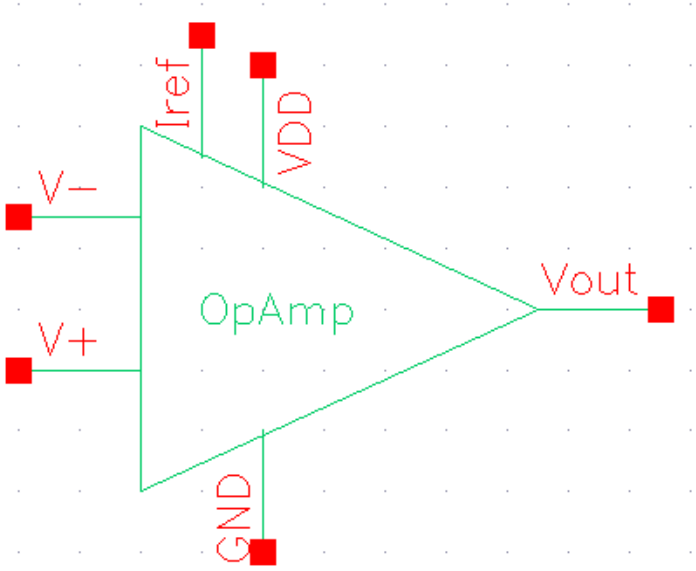


- $P1=1 \div g_{m7}R_1R_2C_c$

Pin Description

THE MAIN PURPOSE IS TO SHOW THE BASIC METHODS FOR DESIGNING A TWO STAGE OP-AMP BASED ON CADENCE, AND DC SCHEMATIC PLOT AND AC ANALYSIS SIMULATION.

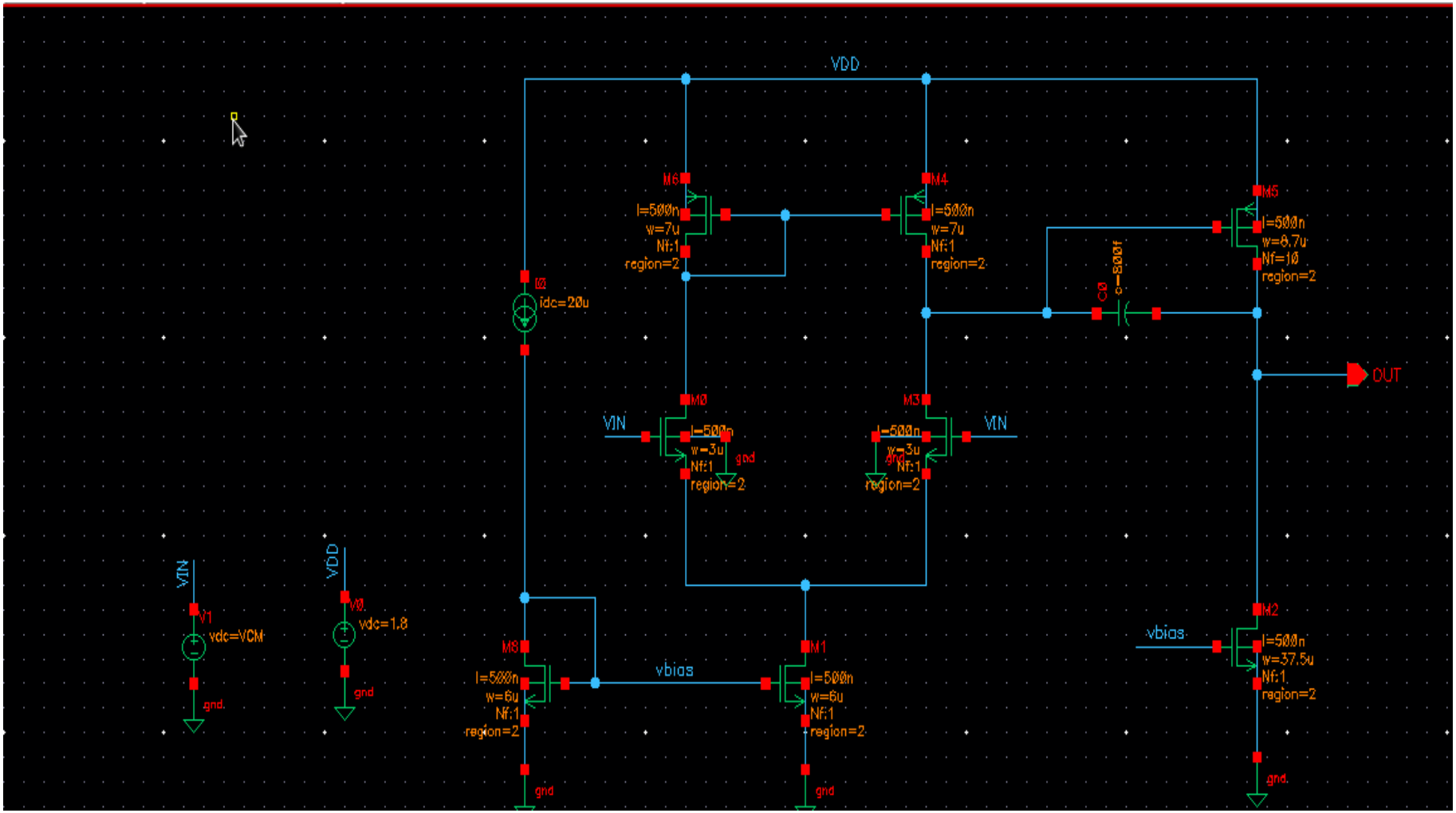
Sl.No	Pin Name	Description	Input/Output/Supply
1	V_{DD}	Supply pin V_{DD}	Supply
2	GND	Supply pin GND	Supply
4	I_{ref}	20μA of reference current	Input
5	V_{+}	+ve Input	Input
6	V_{-}	-ve Input	Input
7	V_{OUT}	Output voltage	Output



7_pack SCM

7_pack SCM								
Specification Compliance Matrix								
Parameter	Unit	Specification			PVT			Comment
		Min	Typ	Max	Min	Typ	Max	
V_{DD}	V	1.8	1.8	1.8	1.8	1.8	1.8	Supply Voltage
TEMP	°C	-40	27	125	-40	27	125	Temperature
I_{ref}	µA	20	10	20	20	10	20	Reference Current
ICMR	V	0.8	0.7	1.6	0.8	0.7	1.6	Input Common Mode Range(ICMR)
C_L	pF	-	2	-	-	2	-	Load Capacitance
Gain	dB	-	60	-	66	60	60.74	DC gain
PM	deg	-	60	-	57	55	58.34	Phase Margin
GBW	MHz	-	30	-	32.2	30	32.76	Gain Bandwidth Product

Schematic



HAND CALCULATIONS ARE BEEN DONE TO OBTAIN THE DESIGN PARAMETERS (I.E.(W/L) RATIO).

Bias Parameters

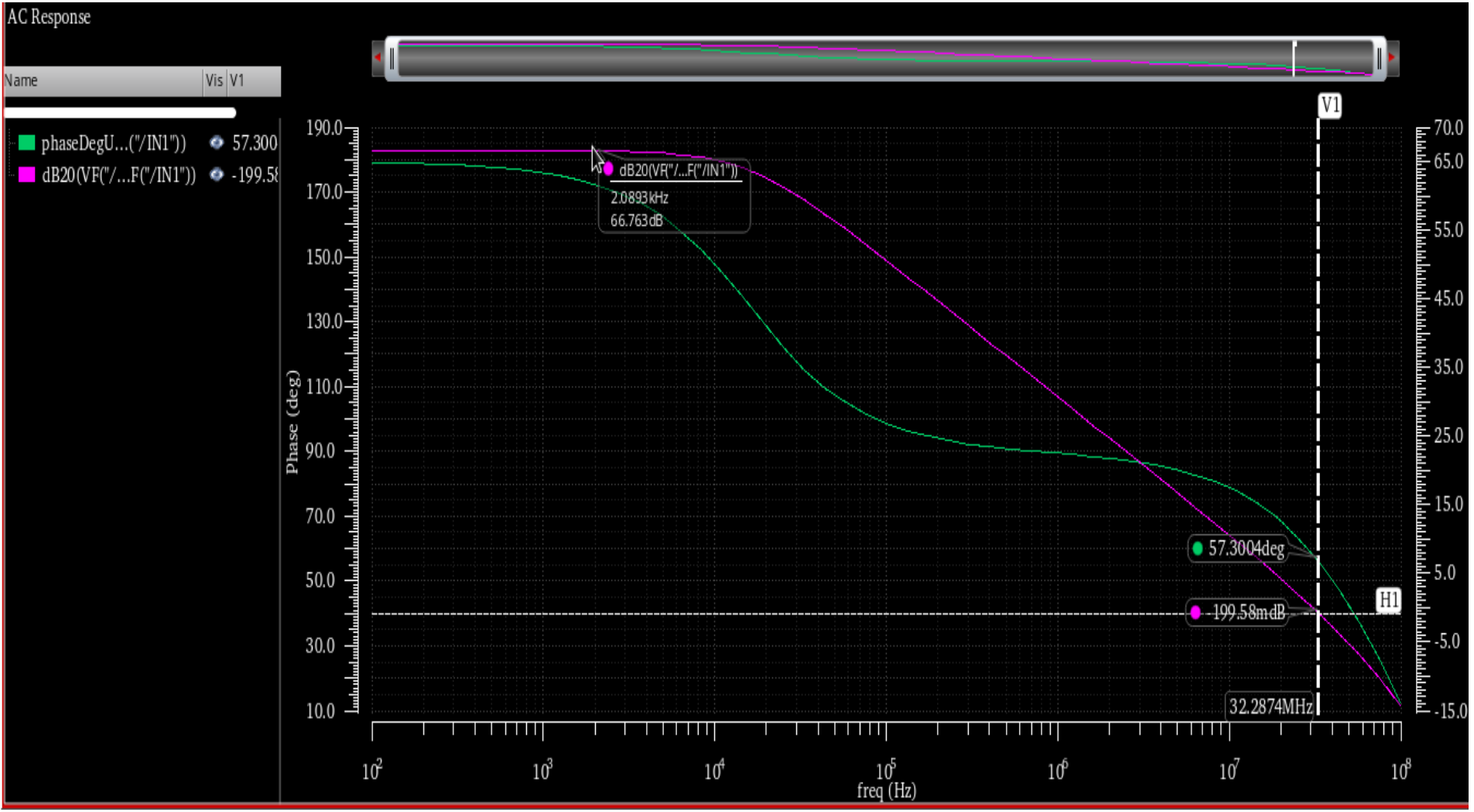
Parameter	M1	M2	M3	M4	M5	M6	M7	M8
W (μm)	3	3	7	7	12	87	75	12
L (nm)	500	500	500	500	1000	500	1000	1000
V_{gs} (V)								
V_{ds} (V)								

Bias parameters

AC Analysis

Gain-Phase Plot-Vin=0.8V

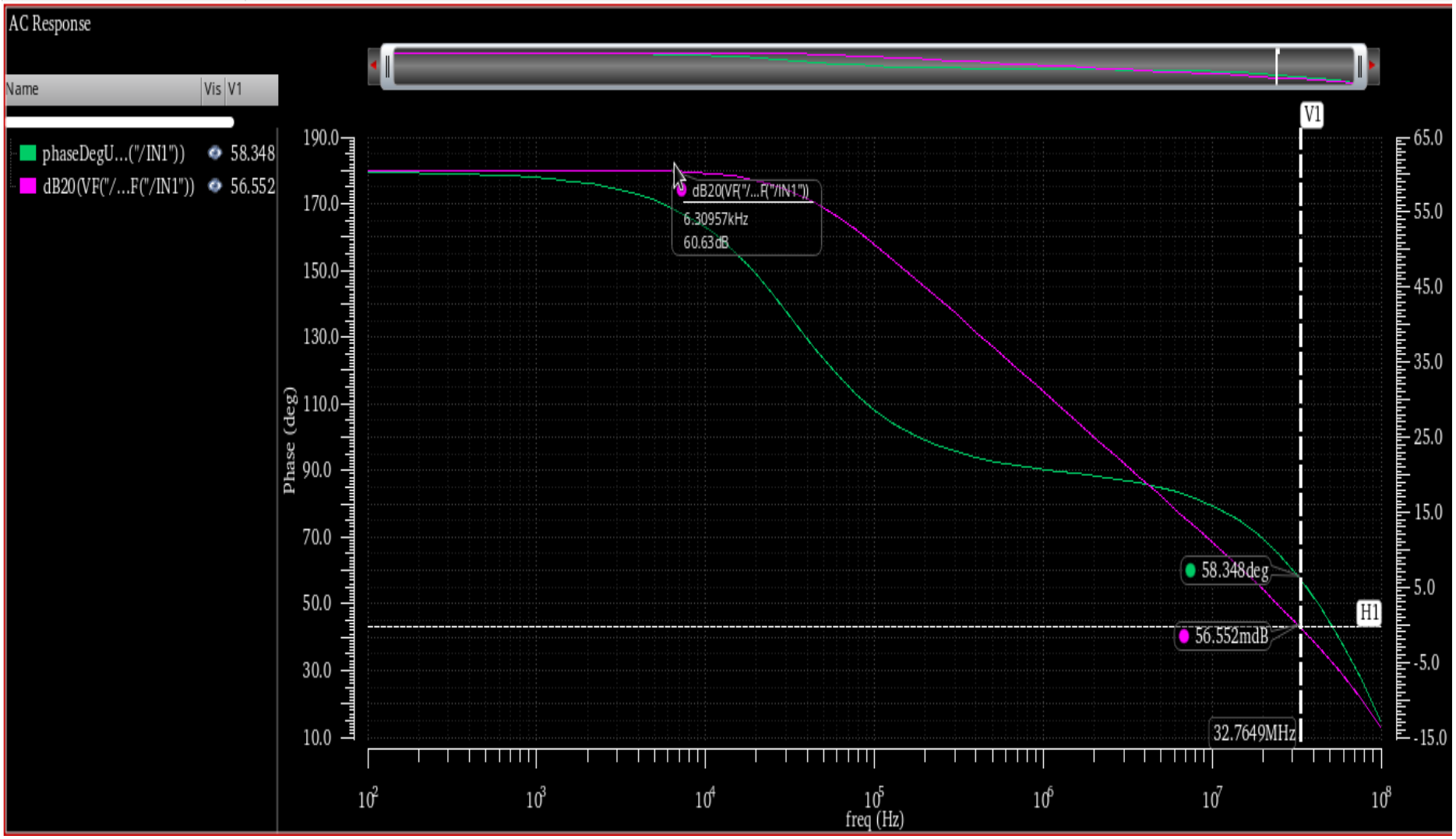
Gain=66dB,BW=32.20MHz,PM=57degree



AC Analysis

Gain-Phase Plot-Vin=1.6V

Gain=60.74dB,BW=32.76MHz,PM=58.34degree



Power Dissipation

Total Power=Vdd*Sum of all currents

=1.8*(125+20)

=261uW

- For Vin=0.8V

  Power=273.53uW

- For Vin=1.6V

  Power=297.88uW

Thank You