| | Port Name / | Group | Macro Cell | Pin Number | Locked | Bank Name | I/O Standard |
|---|---|---|---|---|---|---|---|
| 1 | ADC_CLK | | ADLIB:OUT... | A17 | ☒ | Bank0 | LVTTL |
| 2 | ADC_S1 | | ADLIB:OUT... | D18 | ☒ | Bank0 | LVTTL |
| 3 | CLKC | | ADLIB:INBUF | E3 | ☒ | Bank5 | LVTTL |
| 4 | DAC_CLK | | ADLIB:OUT... | A18 | ☒ | Bank0 | LVTTL |
| 5 | DAC_DACEN | | ADLIB:OUT... | F1 | ☒ | Bank5 | LVTTL |
| 6 | DAC_DOUT[0] | | ADLIB:OUT... | E1 | ☒ | Bank5 | LVTTL |
| 7 | DAC_DOUT[1] | | ADLIB:OUT... | F3 | ☒ | Bank5 | LVTTL |
| 8 | DAC_DOUT[2] | | ADLIB:OUT... | G4 | ☒ | Bank5 | LVTTL |
| 9 | DAC_DOUT[3] | | ADLIB:OUT... | H5 | ☒ | Bank5 | LVTTL |
| 10 | DAC_DOUT[4] | | ADLIB:OUT... | H6 | ☒ | Bank5 | LVTTL |
| 11 | DAC_DOUT[5] | | ADLIB:OUT... | J6 | ☒ | Bank5 | LVTTL |
| 12 | DAC_DOUT[6] | | ADLIB:OUT... | B22 | ☒ | Bank1 | LVTTL |
| 13 | DAC_DOUT[7] | | ADLIB:OUT... | C22 | ☒ | Bank1 | LVTTL |
| 14 | DAC_PD | | ADLIB:OUT... | G2 | ☒ | Bank5 | LVTTL |
| 15 | GPIO_8_OUT | | ADLIB:OUT... | T3 | ☒ | Bank4 | LVTTL |
| 16 | GPIO_9_OUT | | ADLIB:OUT... | V3 | ☒ | Bank4 | LVTTL |
| 17 | GPIO_10_O... | | ADLIB:OUT... | U3 | ☒ | Bank4 | LVTTL |
| 18 | GPIO_11_O... | | ADLIB:OUT... | T4 | ☒ | Bank4 | LVTTL |
| 19 | GPIO_12_O... | | ADLIB:OUT... | AA2 | ☒ | Bank4 | LVTTL |
| 20 | GPIO_13_O... | | ADLIB:OUT... | AB2 | ☒ | Bank4 | LVTTL |
| 21 | GPIO_14_O... | | ADLIB:OUT... | AB3 | ☒ | Bank4 | LVTTL |
| 22 | GPIO_15_O... | | ADLIB:OUT... | Y3 | ☒ | Bank4 | LVTTL |
| 23 | in_phase[0] | | ADLIB:INBUF | C21 | ☒ | Bank1 | LVTTL |
| 24 | in_phase[1] | | ADLIB:INBUF | D21 | ☒ | Bank1 | LVTTL |
| 25 | in_phase[2] | | ADLIB:INBUF | B20 | ☒ | Bank0 | LVTTL |
| 26 | in_phase[3] | | ADLIB:INBUF | C19 | ☒ | Bank0 | LVTTL |
| 27 | in_phase[4] | | ADLIB:INBUF | G19 | ☒ | Bank1 | LVTTL |
| 28 | in_phase[5] | | ADLIB:INBUF | F19 | ☒ | Bank1 | LVTTL |
| 29 | in_phase[6] | | ADLIB:INBUF | G21 | ☒ | Bank1 | LVTTL |
| 30 | in_phase[7] | | ADLIB:INBUF | G20 | ☒ | Bank1 | LVTTL |
| 31 | LED[0] | | ADLIB:OUT... | J20 | ☒ | Bank1 | LVTTL |
| 32 | LED[1] | | ADLIB:OUT... | J19 | ☒ | Bank1 | LVTTL |
| 33 | LED[2] | | ADLIB:OUT... | K20 | ☒ | Bank1 | LVTTL |
| 34 | LED[3] | | ADLIB:OUT... | K21 | ☒ | Bank1 | LVTTL |

| | Port Name / | Group | Macro Cell | Pin Number | Locked | Bank Name | I/O Standard |
|---|---|---|---|---|---|---|---|
| 35 | LED[4] | | ADLIB:OUT... | L20 | ☒ | Bank1 | LVTTL |
| 36 | LED[5] | | ADLIB:OUT... | L21 | ☒ | Bank1 | LVTTL |
| 37 | LED[6] | | ADLIB:OUT... | K18 | ☒ | Bank1 | LVTTL |
| 38 | LED[7] | | ADLIB:OUT... | K19 | ☒ | Bank1 | LVTTL |
| 39 | MAC_0_CR... | MAC_0... | ADLIB:INBU... | W4 | ☒ | Bank4 | LVTTL |
| 40 | MAC_0_MDC | MAC_0... | ADLIB:OUT... | AA3 | ☒ | Bank4 | LVTTL |
| 41 | MAC_0_MDIO | MAC_0... | ADLIB:BIBU... | V4 | ☒ | Bank4 | LVTTL |
| 42 | MAC_0_RX... | MAC_0... | ADLIB:INBU... | V5 | ☒ | Bank4 | LVTTL |
| 43 | MAC_0_RX... | MAC_0... | ADLIB:INBU... | U5 | ☒ | Bank4 | LVTTL |
| 44 | MAC_0_RXER | MAC_0... | ADLIB:INBU... | AA4 | ☒ | Bank4 | LVTTL |
| 45 | MAC_0_TX... | MAC_0... | ADLIB:OUT... | AA5 | ☒ | Bank4 | LVTTL |
| 46 | MAC_0_TX... | MAC_0... | ADLIB:OUT... | W5 | ☒ | Bank4 | LVTTL |
| 47 | MAC_0_TXEN | MAC_0... | ADLIB:OUT... | Y4 | ☒ | Bank4 | LVTTL |
| 48 | MAINXIN | -- | ADLIB:MSS... | AA16 | ☒ | -- | |
| 49 | MSS_RESE... | | ADLIB:INBU... | R1 | ☒ | Bank4 | LVTTL |
| 50 | quad_phase[0] | | ADLIB:INBUF | K17 | ☒ | Bank1 | LVTTL |
| 51 | quad_phase[1] | | ADLIB:INBUF | J17 | ☒ | Bank1 | LVTTL |
| 52 | quad_phase[2] | | ADLIB:INBUF | F21 | ☒ | Bank1 | LVTTL |
| 53 | quad_phase[3] | | ADLIB:INBUF | F20 | ☒ | Bank1 | LVTTL |
| 54 | quad_phase[4] | | ADLIB:INBUF | G18 | ☒ | Bank1 | LVTTL |
| 55 | quad_phase[5] | | ADLIB:INBUF | G17 | ☒ | Bank1 | LVTTL |
| 56 | quad_phase[6] | | ADLIB:INBUF | E18 | ☒ | Bank1 | LVTTL |
| 57 | quad_phase[7] | | ADLIB:INBUF | F17 | ☒ | Bank1 | LVTTL |
| 58 | RF_CLK | | ADLIB:OUT... | L22 | ☒ | Bank1 | LVTTL |
| 59 | RF_CS | | ADLIB:OUT... | H20 | ☒ | Bank1 | LVTTL |
| 60 | RF_DOUT | | ADLIB:OUT... | J22 | ☒ | Bank1 | LVTTL |
| 61 | RF_GAIN[0] | | ADLIB:OUT... | D7 | ☒ | Bank0 | LVTTL |
| 62 | RF_GAIN[1] | | ADLIB:OUT... | E8 | ☒ | Bank0 | LVTTL |
| 63 | RF_GAIN[2] | | ADLIB:OUT... | C4 | ☒ | Bank0 | LVTTL |
| 64 | RF_GAIN[3] | | ADLIB:OUT... | C5 | ☒ | Bank0 | LVTTL |
| 65 | RF_GAIN[4] | | ADLIB:OUT... | D8 | ☒ | Bank0 | LVTTL |
| 66 | RF_GAIN[5] | | ADLIB:OUT... | C7 | ☒ | Bank0 | LVTTL |
| 67 | RF_GAIN[6] | | ADLIB:OUT... | C8 | ☒ | Bank0 | LVTTL |
| 68 | RF_RXTX | | ADLIB:OUT... | L18 | ☒ | Bank1 | LVTTL |

| | Port Name / | Group | Macro Cell | Pin Number | Locked | Bank Name | I/O Standard |
|---|---|---|---|---|---|---|---|
| 69 | RF_SHDN | | ADLIB:OUT... | M18 | ☒ | Bank1 | LVTTL |
| 70 | RSSI_CLK | | ADLIB:OUT... | H18 | ☒ | Bank1 | LVTTL |
| 71 | RSSI_CS | | ADLIB:OUT... | H17 | ☒ | Bank1 | LVTTL |
| 72 | RSSI_DIN | | ADLIB:INBUF | H22 | ☒ | Bank1 | LVTTL |
| 73 | SPI_1_CLK | SPI_1 | ADLIB:BIBU... | AA22 | ☒ | Bank2 | LVTTL |
| 74 | SPI_1_DI | SPI_1 | ADLIB:INBU... | V19 | ☒ | Bank2 | LVTTL |
| 75 | SPI_1_DO | SPI_1 | ADLIB:TRIB... | T17 | ☒ | Bank2 | LVTTL |
| 76 | SPI_1_SS | SPI_1 | ADLIB:BIBU... | W21 | ☒ | Bank2 | LVTTL |
| 77 | SW1 | | ADLIB:INBUF | J21 | ☒ | Bank1 | LVTTL |
| 78 | SW2 | | ADLIB:INBUF | B19 | ☒ | Bank0 | LVTTL |
| 79 | SW3 | | ADLIB:INBUF | D15 | ☒ | Bank0 | LVTTL |
| 80 | SW4 | | ADLIB:INBUF | E14 | ☒ | Bank0 | LVTTL |
| 81 | TEST_PTS[0] | | ADLIB:OUT... | N6 | ☒ | Bank5 | LVTTL |
| 82 | TEST_PTS[1] | | ADLIB:OUT... | M6 | ☒ | Bank5 | LVTTL |
| 83 | TEST_PTS[2] | | ADLIB:OUT... | P1 | ☒ | Bank5 | LVTTL |
| 84 | TEST_PTS[3] | | ADLIB:OUT... | P2 | ☒ | Bank5 | LVTTL |
| 85 | TEST_PTS[4] | | ADLIB:OUT... | N3 | ☒ | Bank5 | LVTTL |
| 86 | TEST_PTS[5] | | ADLIB:OUT... | N2 | ☒ | Bank5 | LVTTL |
| 87 | TEST_PTS[6] | | ADLIB:OUT... | M2 | ☒ | Bank5 | LVTTL |
| 88 | TEST_PTS[7] | | ADLIB:OUT... | M1 | ☒ | Bank5 | LVTTL |
| 89 | TEST_PTS[8] | | ADLIB:OUT... | M4 | ☒ | Bank5 | LVTTL |
| 90 | TEST_PTS[9] | | ADLIB:OUT... | L3 | ☒ | Bank5 | LVTTL |
| 91 | TEST_PTS[10] | | ADLIB:OUT... | L2 | ☒ | Bank5 | LVTTL |
| 92 | TEST_PTS[11] | | ADLIB:OUT... | L1 | ☒ | Bank5 | LVTTL |
| 93 | TEST_PTS[12] | | ADLIB:OUT... | L5 | ☒ | Bank5 | LVTTL |
| 94 | TEST_PTS[13] | | ADLIB:OUT... | K4 | ☒ | Bank5 | LVTTL |
| 95 | TEST_PTS[14] | | ADLIB:OUT... | L6 | ☒ | Bank5 | LVTTL |
| 96 | TEST_PTS[15] | | ADLIB:OUT... | K6 | ☒ | Bank5 | LVTTL |
| 97 | UART_0_RXD | UART_0 | ADLIB:INBU... | U18 | ☒ | Bank2 | LVTTL |
| 98 | UART_0_TXD | UART_0 | ADLIB:OUT... | Y22 | ☒ | Bank2 | LVTTL |