SmartFusion SOM (System-On-Module)

Hardware Architecture

Version 1.04

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1. Introduction

This document describes the hardware architecture of the Emcraft Systems SmartFusion SOM (System-On-Module).

The SmartFusion SOM is intended to provide a flexible platform for embedded applications that require rich connectivity, low power and flexibility of the SmartFusion cSoC (configurable System-on-Chip) device coupled with a full-fledged Linux software execution environment running on the ARM Cortex-M3 SmartFusion processor core.

The SmartFusion SOM is based on the Microsemi SmartFusion versatile, low-power, high-integration microcontroller. The uClinux kernel and applications execute on the 100 MHz 32-bit ARM Cortex-M3 processor core, while the integrated controllers, FPGA fabric and programmable analog of the SmartFusion cSoC are used to implement various communication interfaces and protocols.

Using a miniature mezzanine form factor, the SmartFusion SOM is specifically designed to provide the primary SmartFusion cSoC-based intelligence on various boards targeting industrial automation, system and power management, wireless networking / sensors and other embedded applications. SmartFusion SOM hardware and software are architected to ensure flexibility in customizing its functionality for the needs of particular products and/or customers.

2. Hardware Platform

This section defines the hardware platform of the SmartFusion SOM.

2.1. Hardware Platform Overview

The following are the key hardware features of the SmartFusion SOM:

- Compact (30 mm x 57 mm) mezzanine module;
- External interface using two 80-pin 0.4 mm-pitch connectors;
- Mounting hole reducing the risk of connector-to-PCB intermittence;
- Compliant with the Restriction of Hazardous Substances (RoHS) directive;
- SmartFusion cSoC in FG484 package capable of running the system clock at up to 100 MHz;
- JTAG interface to SmartFusion cSoC;
- Powered from single +3.3 V power supply;
- Low-power mode with fast wake-up times;
- Deep-sleep power mode with ultra-low power consumption profiles;
- On-module clocks;
- 16 MBytes PSRAM;
- 16 MBytes NOR Flash;
- Serial console interface at UART CMOS levels;
- 802.3 Ethernet interface;
- Watchdog Timer (WDT);
- Real-Time Clock (RTC);
- Almost all otherwise uncommitted interfaces of the SmartFusion cSoC available on the interface connectors.

2.2. Functional Block Diagram

The following figure is a functional block diagram of the SmartFusion SOM:

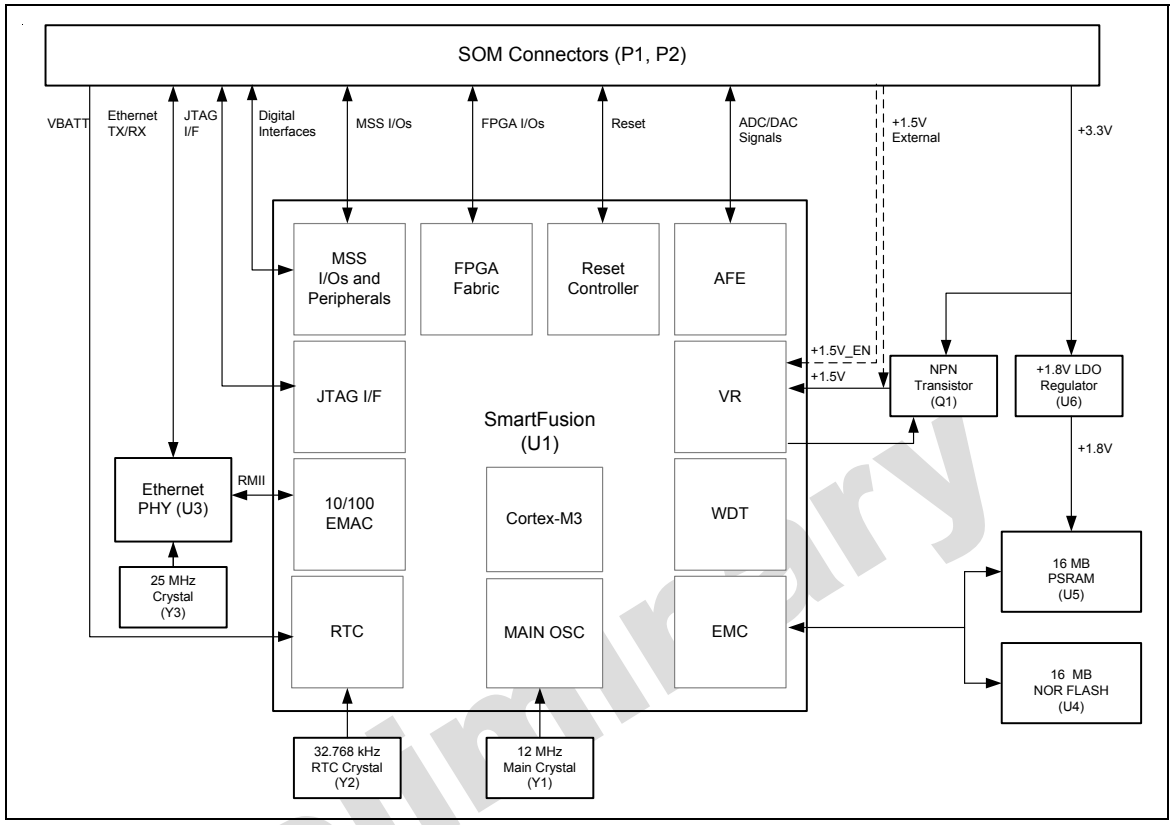

Figure 1: SmartFusion SOM Functional Block Diagram

2.3. Microcontroller

2.3.1. Microcontroller Device

The architecture of the SmartFusion SOM is built around the Microsemi SmartFusion cSoC that combines a 32-bit ARM Cortex-M3 processor core with a wide range of the integrated peripheral controllers as well as the FPGA fabric and a sophisticated analog engine.

The SmartFusion cSoC is implemented using the FG484 package.

2.3.2. Microcontroller Configuration

The SmartFusion SOM supports build-time selection of the following SmartFusion cSoC devices:

- Capacity:
  - A2F200 (4608 tiles, 256 KB eNVM, 64 KB SRAM) or
  - A2F500 (11520 tiles, 512 KB eNVM, 64 KB SRAM)
- Speed Grade:
  - Standard Grade (80 MHz) or
  - Grade-1 (100 MHz)
- Temperature Range:
  - Commercial (0 to +85°C) or
  - Industrial (–40 to +100°C).

Selection of any of the options above in an actual assembled unit does not affect the other sections of the hardware architecture. For those configuration options that affect software functionality, software running on the SmartFusion SOM is expected to determine the specific microprocessor configuration at run-time and adjust its operation accordingly.

2.4. JTAG Interface

The SmartFusion SOM provides a FlashPro-3/4-compatible JTAG interface on the interface connectors. The JTAG interface is routed to the corresponding signals of the SmartFusion cSoC.

2.5. FPGA

2.5.1. SmartFusion On-Chip Configuration and FPGA Design

Customers of the SmartFusion SOM are provided with a SmartFusion on-chip configuration and FPGA design suitable for the intended operation of the SmartFusion SOM.

The SmartFusion SOM on-chip configuration and FPGA design can be viewed as an extension of the SmartFusion SOM hardware design. It contains a logical definition of the internal SmartFusion architecture, which consists of the Microcontroller Subsystem (MSS) configuration, as well as a number of IP blocks developed by Microsemi and Emcraft Systems. It also describes an electrical interface between the SmartFusion device and external components, such as the SmartFusion device pin configuration and assignment.

2.5.2. Libero Project

The SmartFusion SOM on-chip configuration and FPGA design is provided as a Libero IDE project. It is expected that customers will use this project as a starting point for their application-specific FPGA development.

Note: *It is assumed that the reader is familiar with the Microsemi FPGA development process using the Libero IDE and Libero SoC tools. For more information on these and other Microsemi development tools, refer to the Microsemi SoC Product Group web page at http://www.actel.com.*

Note: *The Libero project files included in this release of the SmartFusion SOM are intended to be used with Libero SoC v10.0. Using these files with any other release of the Libero IDE or Libero SoC software (earlier or later) may require manual adaptation of the FPGA design.*

In addition to the Libero project files customers are provided with a resulting `.pdb` file. This `.pdb` file is installed on every SmartFusion SOM unit shipped to customers.

The `.pdb` file is provided for convenience, allowing the original design to be re-programmed into the SmartFusion device using the Microsemi FlashPro programming tool, if necessary. Here is how the `.pdb` file can be installed onto SmartFusion cSoC using the FlashPro tool:

1. Start FlashPro on a Windows host;
2. From the FlashPro IDE, create a new project with an arbitrary name;
3. From the main FlashPro window, push `Configure Device`;
4. Push `Browse` next to `load existing programming file`. Browse to the `.pdb` file and choose it;
5. Push `Program` at the top of the main window to program the project onto the SmartFusion device and wait for the programming procedure to complete. If the programming completes successfully, a next reset should bring the U-Boot start-up messages and the command line interface onto the serial console interface on the SmartFusion SOM.

2.5.3. FPGA IP Programming Interfaces

The Libero project installs the following IP blocks to the FPGA fabric of the SmartFusion:

Address Range	IP	Tiles	Description	Mandatory/Optional
0x40050000- 0x400500FF	CoreInterrupt	68	Flexible interrupt controller for AMBA–Based Systems, supporting up to 4 IRQ sources	Optional - is required only if there are multiple FPGA slaves triggering interrupts to the MSS core
0x40050100- 0x400501FF	VersionROM	20	Provides an APB register-based interface ROM used for storing FPGA design type and version information	Mandatory
0x40050200- 0x400502FF	CoreGPIO_0	180*	Provides an APB register-based interface to 32 GPIOs	Optional – is required only if the FPGA-based GPIO is needed
0x40050300- 0x400503FF	PSRAM_CR_0	470	Custom IP used to configure external PSRAM and to place it into Page Mode	Mandatory

Table 1: IP Blocks

* - *Assessment value based on the CoreGPIO datasheet.*

2.6. Power

2.6.1. Power Source

The SmartFusion SOM is run from a single +3.3 V power source provided through multiple pins on the interface connectors.

2.6.2. Power Conversion, Sequencing and Configuration

The SmartFusion SOM provides two options for converting the +3.3 V input power to a +1.5 V power source required by the SmartFusion SOM circuitry, as described below. Choice of one of the two power conversion configuration options is made by a baseboard designer using a dedicated input (`1.5V_EN`) provided on the interface connectors.

- Cost-optimized mode. This mode makes use of the built-in +1.5 V voltage regulator of SmartFusion cSoC combined with an on-module transistor. This option provides the lowest-cost and easy-to-implement solution but it is less efficient in terms of the power consumption characteristics of the SmartFusion SOM.

  To enable the cost-optimized mode, a baseboard must drive `1.5V_EN` high or leave it floating, thus enabling the on-module power conversion and sequencing logic. When this configuration is enabled, no additional power conversion and sequencing logic is required on a baseboard.

  When in the cost-optimized mode, the SmartFusion SOM provides the on-module power-supply sequencing to ensure that the internal +1.5 V voltage regulator is turned on (the

PUN input of the SmartFusion cSoC is driven low) only after a stable +3.3 V power supply is applied to the SmartFusion cSoC. For this purpose the SmartFusion SOM uses special circuitry that includes a Richtek RT9818C-29GV voltage detector and a Fairchild 2N7002 MOSFET. This logic ensures that PUN is driven high and the internal +1.5 V voltage regulator is not enabled until the 3.3 V has stayed at levels above +2.9 V for at least 143 ms.

- Power-optimized mode. This mode makes use of an external (off-module) switching regulator (DC/DC) converter to implement an external +1.5 V power source for the SmartFusion cSoC. This option results in a solution that reduces the power consumption of the SmartFusion SOM by about 70 mA at the cost of using more expensive external components.

  To enable the power-optimized mode, a baseboard must drive 1.5V_EN low thus disabling the on-module power conversion and sequencing logic the on-module power conversion logic. In this mode, a baseboard is responsible for providing power conversion and sequencing logic optimized for optimal power consumption. Specifically, the following circuitry is recommended on a baseboard in this mode: TBD - provide a snapshot of recommended baseboard schematics as well as a brief description of what this circuitry does exactly.

2.6.3. Power Supervising and Fault Recovery

The SmartFusion SOM provides power supply fault detection and recovery using the built-in Power Supply Monitor (PSM) of the SmartFusion cSoC.

The PSM keeps the SmartFusion cSoC in reset during power-up until the +1.5 V supply has gone above +1.3 V. During power-down or when a power fault occurs, resulting in the +1.5 V supply going down below +0.65 V, the PSM resets the SmartFusion cSoC.

Additionally, the PSM asserts BROWNOUT3_3VINT (when the +3.3 V supply falls below +2.5 V) and BROWNOUT1_5VINT (when the +1.5 V supply falls below +1.3 V). The assertion of these signals can be configured by software to trigger an interrupt to the Cortex-M3 core and then used as a brown-out indicator for software.

2.6.4. Power Modes

The SmartFusion SOM supports the following power modes:

- Full-power mode. This is the normal mode of operation where both the MSS and the FPGA fabric are operational. FCLK is running and the Cortex-M3 is active running RTOS and/or application code. All memory controllers are enabled.

  Software is configured to enable only those SmartFusion cSoC sub-systems that are used by installed device drivers; all other sub-systems are in reset and do not consume power. If the Ethernet interface is not enabled by a corresponding device driver, the Ethernet PHY is in a low power mode (refer to section 2.12.5). If software is not using the external Flash at a particular time, the Flash device is automatically switched to a low power mode (refer to section 2.10.2).

- Low-power mode. This is the mode of operation the Linux software may be configured to enter when the SmartFusion SOM is idle from the software perspective. To elaborate, this mode may be entered when Linux has no active processes to run and is running the so-called "idle process". When Linux finds itself in the idle state, it transitions the SmartFusion cSoC to the Standby mode, which is intended by the SmartFusion cSoC architecture for applications that intend to put the device into a low-power state but be ready to respond to an interrupt sourced from the MSS, the FPGA or the analog front-end. Software transitions into this mode by executing a "wait for interrupt" (WFI) instruction in the Cortex-M3, causing FCLK to be gated off to the Cortex-M3 processor. This disables the majority of the Cortex-M3 logic. In the Standby mode, the SmartFusion device is active, but running off of a lower frequency clock than what is used for normal system operation. For example, the 32 KHz oscillator can be used to clock the MSS. Peripherals not being used can be put into a low-power state by asserting their individual resets. In addition, if the analog front-end is not needed during this state, software can turn off portions or the entire analog block.

To put external devices into a low-power mode, the SmartFusion SOM provides a dedicated output signal intended as a control for switching off-board devices to low-power modes. This active-low signal is implemented using a FPGA I/O of the SmartFusion cSoC and is available as FPGA_GPIO37N on the interface connectors.

When switching the system to the low-power mode, software activates the low-power mode signal. Various on-board and off-board devices are expected to react to activation of that signal by switching themselves to low-power modes. Conversely, when software is switching back to the full-power mode, it de-asserts the low-power mode signal indicating to on-board and off-board devices that they are expected to switch back to the full-power mode.

- Deep-sleep mode. This mode of operation is intended for applications that have ultra low-power requirements for the control unit, such as the SmartFusion SOM, at static times. Example of such an application would be a remote sensor data collecting unit with an "energy harvesting" type of a power supply. In such applications, it is assumed that the SmartFusion SOM is "asleep" most of the time and needs to run only when an RTC alarm or an external event input triggers.

  To achieve ultra low-power patterns for such applications using the SmartFusion SOM, the following architecture is suggested to a baseboard designer. An Epson RX-TBD Real-Time Clock (RTC) device is placed on a baseboard on the I^2C bus of the SmartFusion SOM. This RTC features an integrated 32.768 kHz oscillator, an RTC alarm function, two maskable event inputs and has extremely low power requirements at static times (TBDnA, typical). The event inputs are used to implement application specific "SmartFusion SOM wake-up events" such as, for instance, a voltage sensing trigger, GPIO input trigger or whatever makes sense in a particular application. The output of the RTC device is used as the "SmartFusion SOM power supply enable" signal and is connected to a low-power switch controller such as the Linear Technology LTC1982 device, that provides the shutdown power consumption of only 1 uA.

  The above power management logic is always enabled and resides in a power domain separate from the +3.3 V SmartFusion SOM power domain drawing as little as 1uA or less at static times. By being able to access the RTC device on the I^2C bus, software running on the SmartFusion SOM is given an interface to shutdown itself by switching off the +3.3 V power supply and, at the same time, to ensure that the +3.3 V power supply is switched on and the SmartFusion SOM is "waken up" whenever an RTC alarm or an external input event triggers.

2.7. System Reset

2.7.1. Reset Architecture Overview

The SmartFusion SOM implements a sophisticated reset architecture that ensures that the SmartFusion cSoC is reset as appropriate on various hardware and software events.

Software running on the SmartFusion SOM is expected to configure the MSS_RESET_N signal of the SmartFusion cSoC as an output making it a reset request signal for on-board and off-board devices. The SmartFusion SOM ensures that the on-board PHY and Flash devices are reset as soon as the SmartFusion SOM is subjected to a reset by connecting this signal to the reset input of the respective devices.

Those off-board devices that require synchronizing their resets with SmartFusion SOM resets must connect the active-low MSS_RESET_N signal to the reset input of a respective device.

2.7.2. Types of System Resets

The following types of reset are implemented by the SmartFusion SOM:

- Power-on reset. This type of reset occurs when the SmartFusion SOM is being powered-up. More specifically, this type of reset is implemented as follows. As explained in Section 2.6.2, the SmartFusion SOM drives the PUN input of the SmartFusion SOM high and therefore does not enable the internal +1.5 V voltage regulator of the SmartFusion cSoC until the 3.3 V power supply has not reached +2.9 V. Further, the integrated PSM keeps the SmartFusion cSoC in reset until the +1.5 V supply has gone above +1.3 V. Until such time, the SmartFusion cSoC is not running.

The MSS_RESET_N signal of the SmartFusion cSoC is in underfined state; the state of on-board and off-board external devices is defined by their respective power-up characteristics. As soon as the +1.5 V power supply has reached a valid state, the SmartFusion cSoC is taken out of reset and software starts to run, proceeding to configure MSS_RESET_N and the integrated reset controller of the SmartFusion cSoC for normal operation as described in Section 2.7.1.

- Power down or power supply fault reset. The integrated PSM triggers the power-on reset sequence as soon as the +1.5 V supply has gone below +0.65 V.
- Brown-out reset. In case the +3.3 V supply falls below +2.5 V or the +1.5 V supply falls below +1.3 V, the integrated PSM may be configured by software to trigger a brown-out interrupt to the Cortex-M3 processor core. Software running on the SmartFusion SOM may chose to handle such an event by initiating the software reset sequence.
- Software reset. This type of reset is activated by software running on the SmartFusion SOM through performing the SmartFusion cSoC software reset sequence.
- WDT reset. This type of reset is activated when the integrated WDT of the SmartFusion cSoC expires.
- Manual reset. To activate this type of reset, a baseboard drives low the nRESET signal.

2.8. System Clocks

The SmartFusion SOM provides a 12 MHz quartz crystal as a reference to the internal oscillator of the SmartFusion cSoC.

The SmartFusion cSoC contains integrated PLLs driven by the above oscillator from which the various clocks required by the SmartFusion subsystems are derived. More specifically, the SmartFusion on-chip configuration and FPGA design (refer to section 2.5.1) provide the following clocks for the various SmartFusion domains:

Clock	Frequency (MHz)	Purpose
FCLK	80	Main MSS clock
PCLK0	20	APB bus APB_0 clock
PCLK1	20	APB bus APB_1 clock
ACLK	40	APB bus APB_2 clock (ACE clock)
FAB_CLK	40	FPGA fabric clock

Table 2: System Clocks

In addition to the 12 MHz crystal, the SmartFusion SOM provides a dedicated clock reference for the Ethernet sub-section (refer to section 2.12.3).

2.9. PSRAM

2.9.1. PSRAM Architecture

The SmartFusion SOM provides 16 MBytes of 70 ns PSRAM memory using the Micron MT45W8MW16 device. The PSRAM memory resides at chip select EMC_CS0_N of the integrated memory controller of the SmartFusion cSoC.

2.9.2. PSRAM Operational Mode

The SmartFusion SOM provides a dedicated PSRAM_CR IP block implemented in the FPGA fabric of the SmartFusion cSoC as an interface to the configuration registers of the PSRAM memory.

Using the software interfaces implemented by that IP block, software may configure the PSRAM for operation in a performance-optimized mode. More specifically, the PSRAM may be

configured to run in the Asyncronous Page mode, which requires 70 ns for a first 16-bit access and then only 20 ns for up to 16 sequential accesses within the same page.

2.9.3. PSRAM Low-Power Mode

When not accessed, the PSRAM power consumption is only 200 uA.

2.10. Flash

2.10.1. Flash Architecture

The SmartFusion SOM provides 8 MBytes of NOR Flash memory, using the Spansion S29GL064N90 device. The Flash memory resides at chip select `EMC_CS1_N` of the integrated memory controller of the SmartFusion cSoC.

2.10.2. Flash Low-Power Mode

When not accessed, the Flash power consumption is only 5 uA.

2.11. Serial

2.11.1. UART Controller

The SmartFusion SOM provides an UART serial interface at CMOS levels (no RS-232 buffer) using the integrated UART0 controller of the SmartFusion cSoC on the interface connectors.

This interface is intended as the console interface for the U-Boot and Linux software.

2.11.2. Serial Baud Rate

The UART controller features an internal divider that allows this serial interface to operate at standard baud rates up to 921,6 Kbps.

2.12. Ethernet

2.12.1. Ethernet Controller

The SmartFusion SOM provides a full-featured, configurable Ethernet interface capable of 10/100 Mbps data rates using the integrated 802.3 controller of the SmartFusion cSoC.

2.12.2. Ethernet Physical Layer

The physical layer of the Ethernet port is implemented using the Micrel KSZ8051RNL PHY device to provide a full-featured, 10/100 Mps 802.3 interface.

2.12.3. Ethernet Clock

The SmartFusion SOM provides a 25 MHz quartz crystal as a clock reference to the Ethernet PHY device.

The KSZ8051RNL PHY device drives a 50 MHz clock input of the integrated Ethernet MAC interface of the SmartFusion cSoC.

2.12.4. Ethernet Status LEDs

The SmartFusion SOM provides two status signals for the Ethernet channel on the interface connectors for controlling off-module Ethernet LEDs. The functionality of these signals is as follows:

- `LED_ACT`, used to indicate link status (Link when low, No Link when high) and the RX activity when toggling;

- LED_SPD, used to indicate the 10/100 Mbit link status (100 Mbit when low, 10 Mbit when high).

On a baseboard, the status LEDs must be connected between the SmartFusion SOM output signals and a +3.3 V plane.

2.12.5. Ethernet Low Power Mode

When not accessed, the PHY can be switched to the Power-Down mode under software control. When in the Power-Down mode, the PHY current consumption is only 2 mA.

2.13. WDT

The SmartFusion SOM provides a hardware watchdog function using the integrated WDT module of the SmartFusion cSoC.

If the WDT is enabled and software fails to strobe the WDT within the predefined period of time, the watchdog triggers reset.

The WDT timeout period is defined by software.

The WDT is clocked from the internal RC oscillator of the SmartFusion cSoC (Section 2.14), which guarantees reliable timeout detection even if the main clock reference fails.

2.14. RTC

The SmartFusion SOM supports Real-Time Clock (RTC) functionality using the SmartFusion Real-Time Counter System.

The Real-Time Counter is clocked from the low-power 32.768 KHz oscillator of the SmartFusion cSOC.

The battery switching circuitry continuously compares the battery voltage (VBATT on the interface connectors) with the voltage on the VCCLPXTAL pin of the SmartFusion and automatically powers the RTC and the low-power crystal oscillator from the battery whenever the battery voltage is approximately 0.4 V or more above the VCCLPXTAL pin voltage. That allows both the Real-Time Counter and the low-power crystal oscillator to function when the +3.3 V power supply has been removed.

2.15. External Interface

2.15.1. Interface Connectors

The external interfaces of the SmartFusion SOM are routed through two 80-pin Hirose DF40 series 0.4 mm-pitch board-to-board connectors.

2.15.2. Connectors Pin-Out

The following table details the allocation of the external interface connectors pins on the P1 connector:

Pin	Name	Type	Description	Notes
Power (18 pins)				
2, 3, 5, 8, 9, 11, 14, 57, 75, 76	GND	Power	SOM ground	Must be connected to GND on a baseboard.
77, 79	VCC3	Power	+3.3 V power supply	An external +3.3 V+/- 5% power supply must be applied to these pins.

Pin	Name	Type	Description	Notes
78, 80	VCC1V5	Power	+1.5 V power supply	An external +1.5 V+/- 5% power supply can be applied to these pins (in this case the 1V5_EN signal must be connected to ground). If no external power is applied to these pins, they should be left unconnected.
72	1V5_EN	Input	The on-module +1.5 V LDO regulator control signal	Must be left floating or driven high if the on-module LDO regulator is used. To disable the on-module LDO regulator, this signal must be connected to ground.
74	VBATT	Power	SmartFusion RTC backup power	An external backup power supply of +2.7 V to +3.63 V can be applied to this pin.
13	nRESET_IN	Input	SOM reset input	Active-low hardware reset to the SOM.
15	nRESET_OUT	Output	SOM reset output	Active-low reset from the SOM to external devices.
JTAG (7 pins)				
20	JTAG_TCK	Input	JTAG clock signal to the SmartFusion	
22	JTAGSEL	Input	SmartFusion JTAG controller mode selection	When driven high, the SmartFusion JTAG controller is in the FPGA programming mode. When driven low, the SmartFusion JTAG controller is in the Cortex-M3 debug mode.
24	JTAG_TMS	Input	JTAG mode select	
36	JTAG_nTRST	Input	JTAG controller reset	Active-low
38	JTAG_TDO	Output	JTAG data output from the SmartFusion	
47	JTAG_TDI	Input	JTAG data input to the SmartFusion	

Pin	Name	Type	Description	Notes
62	VJTAG_VPP	Power	SmartFusion programming voltage and SmartFusion JTAG controller power supply	An external +3.3 V+/- 5% power supply must be applied to this pin. When the SmartFusion JTAG controller is not needed this pin can be driven low or left floating.
Serial (4 pins)				
28	UART_1_TXD	Output	SmartFusion MSS UART1 transmit data output/ GPIO	
29	UART_0_TXD	Output	SmartFusion MSS UART0 transmit data output/ GPIO	Used for the software console interface.
30	UART_0_RXD	Input	SmartFusion MSS UART0 receive data input/ GPIO	Used for the software console interface.
31	UART_1_RXD	Input	SmartFusion MSS UART1 receive data input/ GPIO	
Ethernet (6 pins)				
1	LED_ACT	Output	Ethernet Link/Activity status	Low – Link, High – No Link, Toggling – RX activity.
4	TD_P	Output	Ethernet differential positive transmit signal	TD_N and TD_P signals should be routed on a baseboard with a 100 Ohm differential impedance.
6	TD_N	Output	Ethernet differential negative transmit signal	
7	LED_SPD	Output	Ethernet 10/100Mbit link status	Low – 100 Mbit, High – 10 Mbit.
10	RD_P	Input	Ethernet differential positive receive signal	RD_N and RD_P signals should be routed on a baseboard with a 100 Ohm differential impedance.
12	RD_N	Input	Ethernet differential negative receive signal	
GPIO (14 pins)				
16	FPGA_GPIO37N	Output	SmartFusion MSS GPIO	Unconnected on the SOM-A2F200
17	MSS_GPIO_0	Input/Output	SmartFusion MSS GPIO	
18	FPGA_GPIO82N	Input/Output	SmartFusion FPGA I/O	
19	MSS_GPIO_1	Input/Output	SmartFusion MSS GPIO	

Pin	Name	Type	Description	Notes
21	MSS_GPIO_2	Input/Output	SmartFusion MSS GPIO	
23	MSS_GPIO_3	Input/Output	SmartFusion MSS GPIO	
32	FPGA_GPIO37P	Input/Output	SmartFusion FPGA I/O	Unconnected on the A2F200-SOM
34	FPGA_GPIO82P	Input/Output	SmartFusion FPGA I/O	
35	FPGA_GPIO73P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
37	FPGA_GPIO73N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
39	FPGA_GPIO74P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
41	FPGA_GPIO74N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
43	FPGA_GPIO75P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
45	FPGA_GPIO75N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
I^2C (4 pins)				
25	I2C_1_SCL	Input/Output	SmartFusion MSS I2C1 bus serial clock input/output/ GPIO	
26	I2C_1_SDA	Input/Output	SmartFusion MSS I2C1 bus serial data input/output/ GPIO	
27	I2C_0_SDA	Input/Output	SmartFusion MSS I2C0 bus serial clock input/output/ GPIO	This interface is explicitly committed on the connector to allow a baseboard connecting an off-module I^2C RTC device.
33	I2C_0_SCL	Input/Output	SmartFusion MSS I2C0 bus serial clock input/output/ GPIO	This interface is explicitly committed on the connector to allow a baseboard connecting an off-module I^2C RTC device.
Analog signals (19 pins)				
40	ABPS1	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.

Pin	Name	Type	Description	Notes
42	TM1	Input	SmartFusion AFE low side of current monitor/ direct ADC input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
44	ADC2	Input	SmartFusion AFE direct ADC input/ LVTTL input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
46	ADC3	Input/Output	SmartFusion AFE direct ADC input/ LVTTL input/ DAC output	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
48	ABPS2	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
49	ADC7	Input/Output	SmartFusion AFE direct ADC input/ LVTTL input/ DAC output	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
50	CM1	Input	SmartFusion AFE high side of current monitor/ direct ADC input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
51	ADC6	Input	SmartFusion AFE direct ADC input/ LVTTL input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
52	ABPS6	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
53	CM2	Input	SmartFusion AFE high side of current monitor/ direct ADC input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.

Pin	Name	Type	Description	Notes
54	ADC5	Input/Output	SmartFusion AFE direct ADC input/ LVTTL input/ DAC output	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
55	ABPS3	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
56	ADC4	Input	SmartFusion AFE direct ADC input/ LVTTL input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
58	TM2	Input	SmartFusion AFE low side of current monitor/ direct ADC input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
60	ADC1	Input/Output	SmartFusion AFE direct ADC input/ LVTTL input/ DAC output	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
64	ABPS7	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
66	ABPS4	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin
68	ABPS5	Input	SmartFusion AFE active bipolar prescaler input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.
70	ADC0	Input	SmartFusion AFE direct ADC input/ LVTTL input	RC filter (1 kOhm, 2.2 nF) is installed on the SOM between this pin and the corresponding SmartFusion pin.

Pin	Name	Type	Description	Notes
SPI (8 pins)				
59	SPI1_DO	Output	SmartFusion MSS SPI1 serial data output/ GPIO	
61	SPI1_DI	Input	SmartFusion MSS SPI1 serial data input/ GPIO	
63	SPI0_DO	Output	SmartFusion MSS SPI0 serial data output/ GPIO	
65	SPI0_DI	Input	SmartFusion MSS SPI0 serial data input/ GPIO	
67	SPI1_CLK	Output	SmartFusion MSS SPI1 serial clock output/ GPIO	
69	SPI1_nSS	Output	SmartFusion MSS SPI1 slave select/ GPIO	
71	SPI0_CLK	Output	SmartFusion MSS SPI0 serial clock output/ GPIO	
73	SPI0_nSS	Output	SmartFusion MSS SPI0 slave select/ GPIO	

Table 3: SmartFusion SOM P1 Connector

The following table details the allocation of the external interface connectors pins on the P2 connector:

Pin	Name	Type	Description	Notes
Power (1 pin)				
80	FPGA_GPIO83P	Output	Low-power mode control signal	When low, enables a low-power mode of external devices. If the low-power mode control signal is not needed, this pin can be used as an FPGA I/O signal.
GPIO (80 pins)				
1	FPGA_GPIO84P	Input/Output	SmartFusion FPGA I/O	
2	FPGA_GPIO84N	Input/Output	SmartFusion FPGA I/O	
3	FPGA_GPIO81P	Input/Output	SmartFusion FPGA I/O	
4	FPGA_GPIO85P	Input/Output	SmartFusion FPGA I/O	
5	FPGA_GPIO81N	Input/Output	SmartFusion FPGA I/O	

Pin	Name	Type	Description	Notes
6	FPGA_GPIO85N	Input/Output	SmartFusion FPGA I/O	
7	MSS_GPIO_4	Input/Output	SmartFusion MSS GPIO	
8	FPGA_GPIO70P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
9	MSS_GPIO_5	Input/Output	SmartFusion MSS GPIO	
10	FPGA_GPIO70N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
11	MSS_GPIO_6	Input/Output	SmartFusion MSS GPIO	
12	FPGA_GPIO69P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
13	MSS_GPIO_7	Input/Output	SmartFusion MSS GPIO	
14	FPGA_GPIO69N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
15	MSS_GPIO_8	Input/Output	SmartFusion MSS GPIO	
16	FPGA_GPIO68P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
17	MSS_GPIO_9	Input/Output	SmartFusion MSS GPIO	
18	FPGA_GPIO68N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
19	MSS_GPIO_10	Input/Output	SmartFusion MSS GPIO	
20	FPGA_GPIO42P	Input/Output	SmartFusion FPGA I/O	
21	MSS_GPIO_11	Input/Output	SmartFusion MSS GPIO	
22	FPGA_GPIO42N	Input/Output	SmartFusion FPGA I/O	
23	MSS_GPIO_12	Input/Output	SmartFusion MSS GPIO	
24	FPGA_GPIO41P	Input/Output	SmartFusion FPGA I/O	
25	MSS_GPIO_13	Input/Output	SmartFusion MSS GPIO	
26	FPGA_GPIO41N	Input/Output	SmartFusion FPGA I/O	
27	MSS_GPIO_14	Input/Output	SmartFusion MSS GPIO	
28	FPGA_GPIO40P	Input/Output	SmartFusion FPGA I/O	
29	MSS_GPIO_15	Input/Output	SmartFusion MSS GPIO	

Pin	Name	Type	Description	Notes
30	FPGA_GPIO40N	Input/Output	SmartFusion FPGA I/O	
31	FPGA_GPIO27P	Input/Output	SmartFusion FPGA I/O	
32	FPGA_GPIO39P	Input/Output	SmartFusion FPGA I/O	
33	FPGA_GPIO27N	Input/Output	SmartFusion FPGA I/O	
34	FPGA_GPIO39N	Input/Output	SmartFusion FPGA I/O	
35	FPGA_GPIO26P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
36	FPGA_GPIO38P	Input/Output	SmartFusion FPGA I/O	
37	FPGA_GPIO26N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
38	FPGA_GPIO38N	Input/Output	SmartFusion FPGA I/O	
39	FPGA_GPIO25P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
40	FPGA_GPIO36P	Input/Output	SmartFusion FPGA I/O	
41	FPGA_GPIO25N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
42	FPGA_GPIO36N	Input/Output	SmartFusion FPGA I/O	
43	FPGA_GPIO24P	Input/Output	SmartFusion FPGA I/O	
44	FPGA_GPIO35P	Input/Output	SmartFusion FPGA I/O	
45	FPGA_GPIO24N	Input/Output	SmartFusion FPGA I/O	
46	FPGA_GPIO35N	Input/Output	SmartFusion FPGA I/O	
47	FPGA_GPIO23P	Input/Output	SmartFusion FPGA I/O	
48	FPGA_GPIO34P	Input/Output	SmartFusion FPGA I/O	
49	FPGA_GPIO23N	Input/Output	SmartFusion FPGA I/O	
50	FPGA_GPIO34N	Input/Output	SmartFusion FPGA I/O	
51	FPGA_GPIO22P	Input/Output	SmartFusion FPGA I/O	
52	FPGA_GPIO31P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
53	FPGA_GPIO22N	Input/Output	SmartFusion FPGA I/O	

Pin	Name	Type	Description	Notes
54	FPGA_GPIO31N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
55	FPGA_GPIO16P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
56	FPGA_GPIO30P	Input/Output	SmartFusion FPGA I/O	
57	FPGA_GPIO16N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
58	FPGA_GPIO30N	Input/Output	SmartFusion FPGA I/O	
59	FPGA_GPIO04P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
60	FPGA_GPIO29P	Input/Output	SmartFusion FPGA I/O	
61	FPGA_GPIO04N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
62	FPGA_GPIO29N	Input/Output	SmartFusion FPGA I/O	
63	FPGA_GPIO03P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
64	FPGA_GPIO33P	Input/Output	SmartFusion FPGA I/O	
65	FPGA_GPIO03N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
66	FPGA_GPIO33N	Input/Output	SmartFusion FPGA I/O	
67	FPGA_GPIO01P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
68	FPGA_GPIO28P	Input/Output	SmartFusion FPGA I/O	
69	FPGA_GPIO01N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
70	FPGA_GPIO28N	Input/Output	SmartFusion FPGA I/O	
71	FPGA_GPIO00P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
72	FPGA_GPIO32P	Input/Output	SmartFusion FPGA I/O	
73	FPGA_GPIO00N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
74	FPGA_GPIO32N	Input/Output	SmartFusion FPGA I/O	
75	FPGA_GPIO71N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
76	FPGA_GPIO72N	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
77	FPGA_GPIO71P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200

Pin	Name	Type	Description	Notes
78	FPGA_GPIO72P	Input/Output	SmartFusion FPGA I/O	Unconnected on the SOM-A2F200
79	FPGA_GPIO83N	Input/Output	SmartFusion FPGA I/O	
80	FPGA_GPIO83P	Input/Output	SmartFusion FPGA I/O	

Table 4: SmartFusion SOM P2 Connector

2.15.3. Unavailable Signals of SmartFusion cSoC

The following signals of the SmartFusion cSoC are not available on the interface connectors. These signals are unused and left unconnected a the SmartFusion SOM:

Pin	Name	Type	Description	Notes
DAC (3 pins)				
V7	SDD0	Output	SmartFusion AFE dedicated DAC signal	
Y17	SDD1	Output	SmartFusion AFE dedicated DAC signal	
W6	SDD2	Output	SmartFusion AFE dedicated DAC signal	Unavailable on the SOM-A2F200
ADC (10 pins)				
Y13	ABPS8	Input	SmartFusion AFE active bipolar prescaler input	Unavailable on the SOM-A2F200
W14	ABPS9	Input	SmartFusion AFE active bipolar prescaler input	Unavailable on the SOM-A2F200
V14	ADC8	Input	SmartFusion AFE direct ADC input/ LVTTL input	Unavailable on the SOM-A2F200
AA14	ADC9	Input/Output	SmartFusion AFE direct ADC input/ LVTTL input/ DAC output	Unavailable on the SOM-A2F200
AA13	ADC10	Input	SmartFusion AFE direct ADC input/ LVTTL input	Unavailable on the SOM-A2F200
U14	ADC11	Input/Output	SmartFusion AFE direct ADC input/ LVTTL input/ DAC output	Unavailable on the SOM-A2F200
AA11	CM3	Input	SmartFusion AFE high side of current monitor/ direct ADC input	
W13	CM4	Input	SmartFusion AFE high side of current monitor/ direct ADC input	Unavailable on the SOM-A2F200

Pin	Name	Type	Description	Notes
Y12	TM3	Input	SmartFusion AFE low side of current monitor/ direct ADC input	
T13	TM4	Input	SmartFusion AFE low side of current monitor/ direct ADC input	Unavailable on the SOM-A2F200

Table 5: Unavailable Signals of SmartFusion cSoC

3. Mechanical Specifications

3.1. SmartFusion SOM Mechanicals

The SmartFusion SOM is implemented as a miniature 30 x 57 x 4.8 mm module.

The SmartFusion SOM PCB thickness is 1.6+/- 0.16 mm. The maximum height of the SOM components is 1.6 mm.

The SmartFusion SOM includes a mounting hole so that the module can be mechanically secured to a baseboard, reducing the risk of connector-to-PCB intermittence that might occur during NEBS vibration and earthquake testing (or during the real events those tests simulate).

The following figure shows the location of the mounting hole and the SOM connectors on the module:

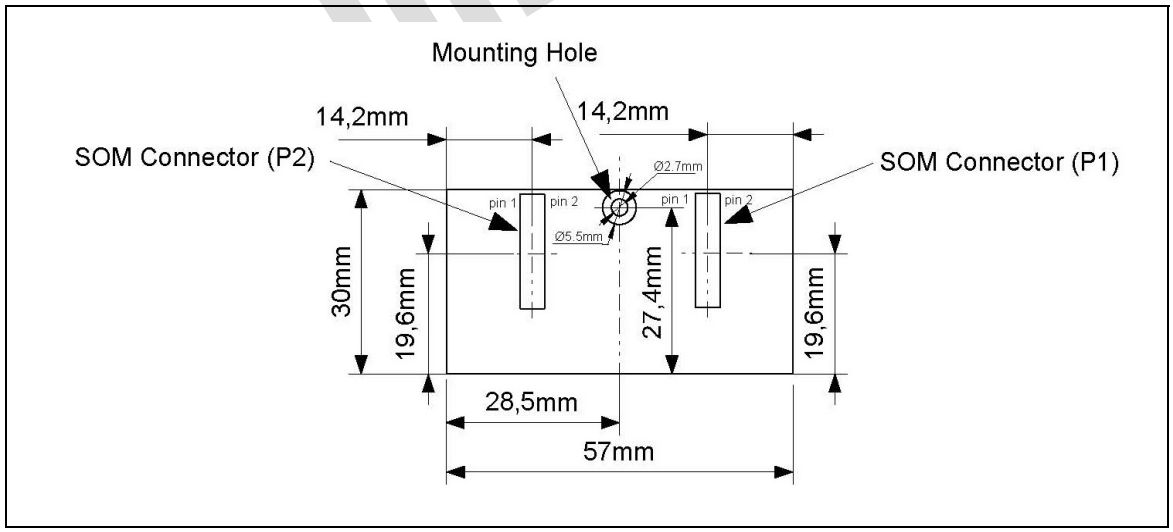

Figure 2: SmartFusion SOM Bottom View

3.2. SmartFusion SOM Connector Mechanicals

On a baseboard, the SmartFusion SOM is installed into two 80-pin Hirose DF40 series 0.4 mm-pitch board-to-board connectors. The exact part number of the connectors is Hirose DF40C-80DP-0.4V(51).

The recommended mating connectors for a baseboard are the Hirose DF40HC(4.0)-80DS-0.4V connector, which provides 4 mm stacking height for the SmartFusion SOM. The maximum height of the SOM above a baseboard for 4 mm stacking height is 7.6 mm.

4. Electrical Specifications

4.1. Power Consumption

The SmartFusion SOM is run from a single +3.3 V power source.

The following table provides the power consumption of the SmartFusion SOM at dynamic (full-power) and static (low-power) times:

TBD

5. Environment Specifications

5.1. Recommended Operating Conditions

The following table lists the recommended operating conditions of the SmartFusion SOM:

Symbol	Parameter	Range
T_A	Ambient temperature	-40 to +85 ºC
VCC3	+3.3 V power supply	+3.3 V +/-5%
VCC1V5	Optional +1.5 V power supply	+1.5 V +/-5%

Table 6: Recommended Operating Conditions

6. Orderable Configurations

TBD